1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD DATE
A	0000865868	PRODUCTION RELEASED	2010-02-26

SCHEM MLB K86

ITCHY

2/25/2010

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-8407	1	SCHEM,MLB,K86	SCH	CRITICAL	
820-2807	1	PCBF,MLB,K86	PCB	CRITICAL	

DRAWING TITLE: SCHEM,MLB,K86

Apple Inc.

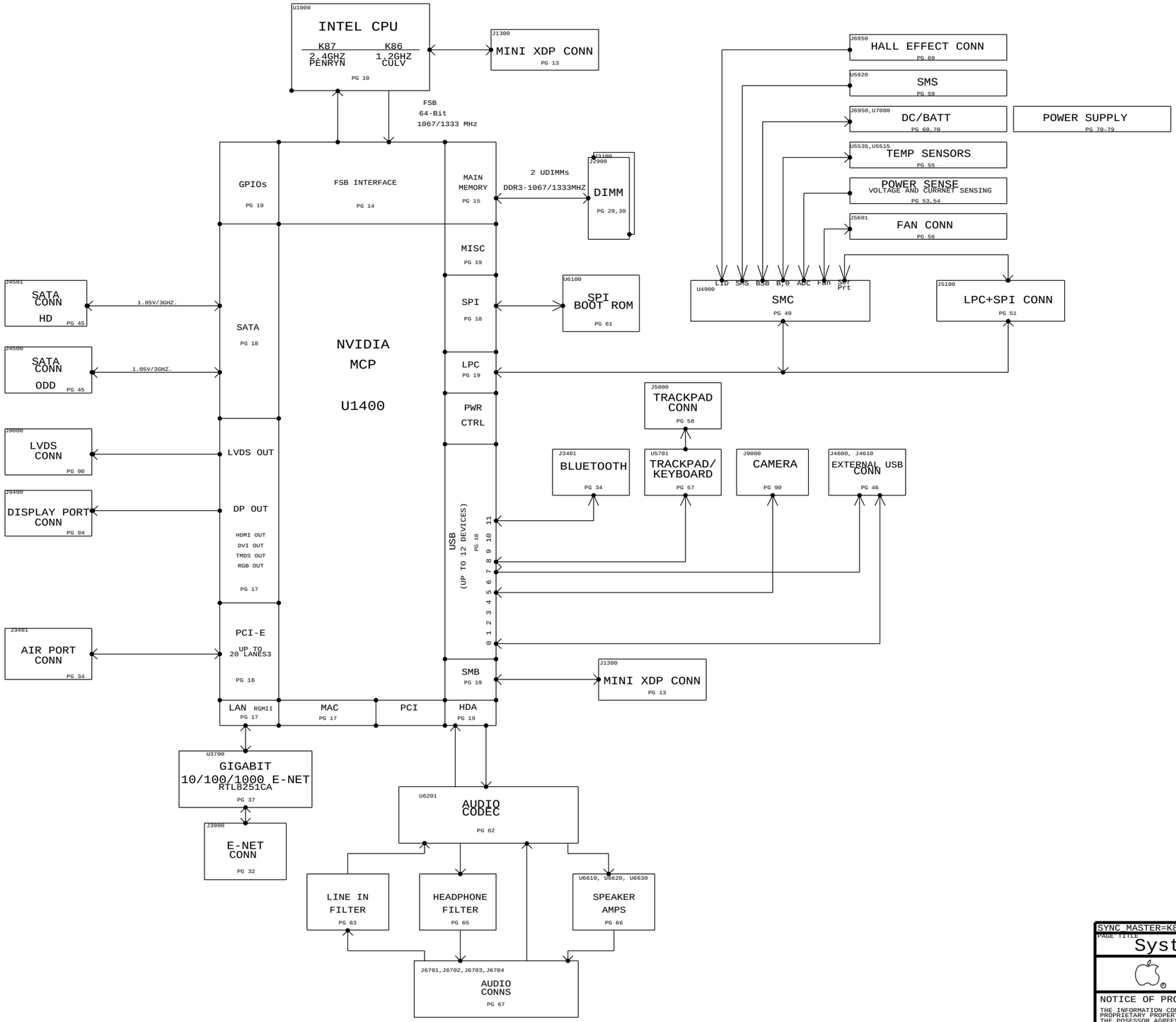
DRAWING NUMBER: 051-8407 SIZE: D

REVISION: A.0.0

BRANCH:

PAGE: 1 OF 109

SHEET: 1 OF 76



SYNC_MASTER=K87_MLB SYNC_DATE=02/26/2010

PAGE TITLE

System Block Diagram

Apple Inc.

DRAWING NUMBER 051-8407 SIZE D

REVISION A.0.0

BRANCH

PAGE 2 OF 109

SHEET 2 OF 76

K86/K87 POWER SYSTEM ARCHITECTURE

AC ADAPTER IN
DCIN(16.5V)
F6905
6A FUSE
SMC_DCIN_ISENSE
R7020
PBUS SUPPLY/ BATTERY CHARGER
ISL6259
U7000
CHGR_EN (S5)
ENABLES
VIN
VOUT
R7050
SMC_BATT_ISENSE
PP18V5_DCIN_CONN
Q7080
Q7085
PPDCIN_G3H_OR_PBUS
PBUS_VSENSE
ENABLE
3.425V G3HOT
LT3470
U6990
PP3V42_G3H_REG
SMC PWRGD
RN5VD30A-F
U5010
8A FUSE
F7040
PPVBAT_G3H_CHGR_REG
PPBUS_G3H
Q5315
PBUS_G3H_VSENSE
CPUVTTS0_EN (S0)
EN_PSV
CPUVTT
(1.05V)
TPS51117
U7600
PP1V05_S0
(8A MAX CURRENT)
CPUVTTS0_PGOOD
SMC_CPU_VSENSE
CPU VCORE
ISL9504B
U7100
IMVP_VR_ON_R
VR_ON
PGOOD
SMC_CPU_ISENSE
PPVCORE_S0_CPU
(44A MAX CURRENT)
VR_PWRGOOD_DELAY
J6950
3S2P
(9 TO 12.6V)
PPVBAT_G3H_CONN
Q7055
PPVBAT_G3H_CHGR_R
CHGR_BGATE
MCP89
U1400
PWRBTN*
PLTRST*
RSMRST*
CPUPWRGD(GPIO49)
CPU_RESET#
LPC_RESET_L
CPU_PWRGD
MCP_PS_PWRGD
PWRGD
U2850
CPU
PWRGOOD
RESET*
U1000
FSB_CPURST_L
PPBUS_G3H
Q7948
PP5V_S0_FET
P5VS0_EN
MCP89
U1400
PM_SLP_S4_L
PM_SLP_S3_L
PM_SLP_RMGT_L
P3V3S3_EN
DDRREG_EN
P5VS3_EN_L
RC DELAY
SMC
U4900
P16
P60
SMC_PM_G2_EN (S5)
U7840
P5VS3_EN_L
P3V3S5_EN_L
5V (RT)
3.3V
TPS51125
U7201
PGOOD1,2
VREG3
P5V3V3_PGOOD
PP5V_S3_REG
(13A MAX CURRENT)
PP3V3_S5_REG
(5.5A MAX CURRENT)
Q7910
Q3450
PP3V3_S3_FET
PP3V3_S3_WLAN
P3V3ENET_EN_L
4.5V AUDIO
MAX8840
U6200
PP4V5_AUDIO_ANALOG
Q7930
Q7960
1.05V
NCP1529
U7710
PP1V05_S0_REG
P3V3S0_EN
PM_SLP_RMGT_L
AP_PWR_EN
Q7890
PM_WLAN_EN_L
Q7890,Q7891
PM_SLP_S3_L
SMC_ADAPTER_EN
P0V9S5_EN
ISL8009B
U7750
PP0V9_S5_REG
PP0V9_ENET_FET
P0V9_ENET_EN
MC34845
U9700
BKLT_EN
PPVOUT_SW_LCDBKLT
PP3V3_S0_FET
1.8V
TPS62202
U7760
PP1V8_S0_REG
1.5V
FDC638P
Q7920
PP1V5_S0_FET
1.05V
TPS74701
U7740
PP1V05_S0_MCP_PLL_OR
Q7930
PP1V5R1V35_SW_MCP
=DDRREG_EN
=DDTVTT_EN
1.5V
0.75V
TPS51116
U7300
PP1V5_S3_REG
(12A MAX CURRENT)
PP0V75_S0_REG
(1A MAX CURRENT)
MCP_CORE
ISL9563A
U7500
MCPCORES0_EN
PPMCPCORE_S0_R
(25A MAX CURRENT)
R7525 PPMCPCORE_S0_REG
BKLT_EN
ALL_SYS_PWRGD
RSMRST_PWRGD
SMC_ONOFF_L
SMC
RSMRST_OUT(P15)
PWRGD(P12)
99ms DLY
RSMRST_IN(P13)
PWR_BUTTON(P90)
P17(BTN_OUT)
PLT_RST*
RST*
PM_RSMRST_L
IMVP_VR_ON_R
PM_PWRBTN_L
SMC_RESET_L
SLP_S5_L
SLP_S4_L
SLP_S3_L
SLP_S5_L(P95)
SLP_S4_L(P94)
SLP_S3_L(P93)
U4900
P5V3V3_PGOOD
MCPCORES0_PGOOD
CPUVTTS0_PGOOD
MCPPLLDO_PGOOD
S0PGOOD_RST_L
RST*
PP3V3_S0
PP1V5_S0
PP1V05_S0
V1
V2
V3
U7870
ISL88042
PBUSVSENS_EN (S0)
P5VS0_EN (S0)
CPUVTTS0_EN
DDRVTT_EN
MCPCORES0_EN
P3V3S0_EN
P1V8S0_EN
P1V5S0_EN

SYNC_MASTER=K87_MLB
SYNC_DATE=02/26/2010
PAGE TITLE
Power Block Diagram
Apple Inc.
DRAWING NUMBER 051-8407
SIZE D
REVISION A.0.0
BRANCH
PAGE 3 OF 109
SHEET 3 OF 76

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-0708	PCBA,MLB,FOXCONN,K86	K86_K87_COMMON,K86_SPECIFIC,FOX_DDR_CONN,EEE:E3T
639-1059	PCBA,MLB,MOLEX,K86	K86_K87_COMMON,K86_SPECIFIC,MOLEX_DDR_CONN,EEEE:DCV3
085-1154	K86 MLB DEVELOPMENT BOM	K86_K87_DEVELOPMENT_ONLY,K86_K87_DEBUG:DEV

Development BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-1154	1	K86 MLB DEVELOPMENT BOM	DEVEL	CRITICAL	DEVELOPMENT_BOM

BOM Groups (always-present)

BOM GROUP	BOM OPTIONS
K86_K87_COMMON	K86_K87_COMMON1,PROJECT_PHASE:PROD,COMMON,ALTERNATE,BOOTROM:PROG,WELLSPRING:PROG,MCP_T_DIODE_SENSOR
K86_K87_COMMON1	DP_ESD,MIKEY,MCPPLL_R:REG,ENET1V05:INT,LED:K86_K87,S0PGOOD_BJT,ENET_ESD,VFRQ:SLPS3,SMC_DEBUG:YES,SPI:25MHZ,LPCPLUS,XDP,OLD_AUDIO_SWITCH
K87_SPECIFIC	CPU:2.4GHZ,IMVP6:2PHASE,SMC:PROG_K87,MCP89M:A02
K86_SPECIFIC	CPU:1.2GHZ,IMVP6:1PHASE,SMC:PROG_K86,MCP83M

BOM Groups (project phase-dependent)

BOM GROUP	BOM OPTIONS
PROJECT_PHASE:DEV	DEVELOPMENT_BOM
PROJECT_PHASE:PROD	K86_K87_DEBUG:PROD
K86_K87_DEVELOPMENT_ONLY	DEBUG_ADC,LPCPLUS_CON,S0PGOOD_ISL,EFI_DEBUG,MCPPLL_LDO,EXT1V05,XDP_CON
K86_K87_DEBUG:DEV	VREFMRGN:YES,BMON:ENG,BKLT:ENG,SENS_R:ENG
K86_K87_DEBUG:PROD	VREFMRGN:NO,BMON:PROD,BKLT:PROD,SENS_R:PROD

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3680	1	PDC,LGDZ,PRQ,2.40,25W,1066,R0,3M,BGA	U1000	CRITICAL	CPU:2.4GHZ
337S3792	1	CDC,SLGYW,PRQ,1.2,10W,800,R0,1M,BGA	U1000	CRITICAL	CPU:1.2GHZ
337S3797	1	IC,MCP89M-A01,31X31MM,BGA1168	U1400	CRITICAL	MCP89M:A01
337S3866	1	IC,MCP89M-A02,31X31MM,BGA1168	U1400	CRITICAL	MCP89M:A02
337S3876	1	IC,MCP83M-A02,31X31MM,BGA1168	U1400	CRITICAL	MCP83M
516S0706	1	CONN,204P,SODIMM,SOCKET,DDR3,RAM,BGA	J3100	CRITICAL	FOX_DDR_CONN
516-0201	1	CONN,204P,SODIMM,P=0.6MM	J2900	CRITICAL	FOX_DDR_CONN
516S0790	1	CONN,204P,SODIMM,SOCKET,DDR3,RAM,BGA	J3100	CRITICAL	MOLEX_DDR_CONN
516-0213	1	CONN,204P,SODIMM,P=0.6MM	J2900	CRITICAL	MOLEX_DDR_CONN
452-1708	4	SCR.M1.6X0.35X6.0,D4,HO.3,BLK,M97	SCREW1,SCREW2,SCREW3,SCREW4	CRITICAL	
870-1940	4	POGO PIN,MED,NOISE-IMPROVED,SILVER,K87	ZS0900,ZS0901,ZS0902,ZS0903	CRITICAL	
870-1940	3	POGO PIN,MED,NOISE-IMPROVED,SILVER,K87	ZS0908,ZS0909,ZS0911	CRITICAL	
870-1939	5	POGO PIN,TALL,NOISE-IMPROVED,SILVER,K87	ZS0904,ZS0905,ZS0906,ZS0907,ZS0910	CRITICAL	
870-1939	5	POGO PIN,TALL,NOISE-IMPROVED,SILVER,K87	ZS0912,ZS0913,ZS0914,ZS0915,ZS0919	CRITICAL	
870-1938	3	POGO PIN,THIN,NOISE-IMPROVED,SILVER,K87	ZS0917,ZS0918,ZS0916	CRITICAL	

353S2718 IS NEW INTERSIL PART FOR FIXING B4 DONGLE ISSUE
514-0704 IS CLOUD GREY 4/LB3 PLASTIC W/PDNI PLATING VERSION OF 514-0692 PART FOR RJ45 CONNECTOR
514-0705 IS CLOUD GREY 4/LB3 PLASTIC W/PDNI PLATING VERSION OF 514-0689 PART FOR USB CONNECTORS
514-0706 IS CLOUD GREY 4/LB3 PLASTIC W/PDNI PLATING VERSION OF 514-0691 PART FOR MINI DP CONNECTOR
514-0718 IS CLOUD GREY 4/LB3 PLASTIC W/PDNI PLATING VERSION OF 514-0694 PART FOR AUDIO CONNECTOR

Programmable Parts

LOCKED BOOTROM APN IS 341S2488 (QL: old info?)

338S0563	1	IC,SMC,HS8/2117,9X9MM,TLP,HF	U4900	CRITICAL	SMC:BLANK
341T0252	1	SUBASSY, IC, SMC, K87	U4900	CRITICAL	SMC:PROG_K87
341T0250	1	SUBASSY, IC, SMC, K86	U4900	CRITICAL	SMC:PROG_K86
335S0610	1	IC,FLASH,SPI,32MBIT,3.3V,86MHZ,8-SOP	U6100	CRITICAL	BOOTROM:BLANK
341T0251	1	SUBASSY, IC, BOOT ROM, K86/K87	U6100	CRITICAL	BOOTROM:PROG
337S2983	1	IC,PSOC+ W/ USB,56 PIN,MLF,CY8C24794	U5701	CRITICAL	WELLSPRING:BLANK
341S2677	1	IC,WELLSPRING CONTROLLER,K87	U5701	CRITICAL	WELLSPRING:PROG

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S0693	152S0778		ALL	DALE/VISHAY, MAGLAYERS AS ALTERNATE
152S0796	152S0685		ALL	CYNTEC AS ALTERNATE
157S0058	157S0055		ALL	DELTA AS ALTERNATE
138S0603	138S0602		ALL	MURATA AS ALTERNATE
128S0093	128S0218		ALL	KEMET AS ALTERNATE
152S0874	152S0516		ALL	MAGLAYERS AS ALTERNATE
152S0847	152S0586		ALL	MAGLAYERS AS ALTERNATE
104S0018	104S0023		ALL	DALE/VISHAY AS ALTERNATE
353S2811	353S1832		ALL	NEW IMPROVED INTERSIL PART AS ALTERNATE

Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE_E1A]	CRITICAL	EEE:E1A
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE_E3T]	CRITICAL	EEE:E3T
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCV2]	CRITICAL	EEEE:DCV2
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCV3]	CRITICAL	EEEE:DCV3

Part Substitutions (differences with K6/K69)

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0125	1	RES,MTL FILM,1/16W,113 OHM,1,0402,SMD,LF	R5714		LED:K86_K87

K86/K87 BOARD STACK-UP

TOP	SIGNAL
2	GROUND
3	SIGNAL(High Speed)
4	SIGNAL(High Speed)
5	GROUND
6	POWER
7	POWER
8	GROUND
9	SIGNAL(High Speed)
10	SIGNAL(High Speed)
11	GROUND
BOTTOM	SIGNAL

SYNC_MASTER=K87_MLB SYNC_DATE=01/19/2010

PAGE TITLE: BOM Configuration

Apple Inc.

DRAWING NUMBER: 051-8407 SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 4 OF 109
SHEET: 4 OF 76

Revision History NOTE: All page numbers are .csa, not PDF. See page 1 for .csa -> PDF mapping.

10/1/2009:INTITIAL RELEASE 0.0.1
- ALL PAGES SYNC'ED FROM K94
- REPLACED K84 MCP AND CPU PAGES WITH K6 PAGES
- UPDATED SCHEMATIC AND PCB PART NUMBER INFO

2009-12-03: Proto 0 release 1.0.0

2009-12-04: 1.1.0
csa 5: Updated CPU block text to include CPU description for both K86 and K87
csa 3: Updated text note to include "K86" in title
csa 4: Added BOM entry under Module Parts table to include CULV processor (337S3779) to minimize delta on this page between K86 and K87 per Diana

2009-12-07: 1.2.0
csa 74: Component value changes per Leo (Intersil):
R7417 from 5.36K => 6.34K, 1% (11450296)
C7434 from 0.12uF => 0.022uF, 10% (132S0102)
Implemented different stuffing options for 1-phase vs 2-phase:
Added IMVP6:2PHASE to the following components:
R7417, C7428, R7409, R7411, C7406, R7414, C7414, C7413
Added BOM table to insert the following APNs for IMVP6:1PHASE:
R7417 = 7.68K 1% (114S0304)
C7428 = 0.22uF 10% (132S0102)
R7409 = 1.58K 1% (114S0236)
R7411 = 255 1% (114S0160)
C7406 = 470pF 10% (132S4720)
R7414 = 97.6K 1% (114S0410)
C7414 = 1000pF 10% (132S0045)
C7413 = 100pF 5% (131S1027)
Updated table to add new values for 1phase (PWM freq., Max current, Load line)

STILL NEED TO UPDATE VALUE OF C7428!

2009-12-08: 1.3.0
csa 45: Added passive deemphasis to SATA_HDD_D2R lines:
Added R4585, R4586 (5.1 ohm, 1%, 114S0093) and OMITted
Added C4585, C4586 (10pF, 5%, 131S0029) and NOSTUFFed
Added BOM table to stuff 0-ohms until we get go-ahead for filter

2009-12-08: 1.4.0
csa 8: Deleted net properties for the following nets:
=PP3V3_S0_CPUVTTISNS'
=PD5V_S0_HDD'
=PD5V_S0_MCPREG'
=PP1V05_S0_MCP_AVDD_UF'
=PPSPD_S0_MEM_B'
=PP3V3_S0_PWRCTL'
=PP3V3_S0_DPCONN'
csa 34: Deleted net properties for =PP3V3_S3_WLAN
csa 74: Changed C7434 from NOSTUFF to IMVP6:2PHASE per Intersil
Added IMVP6:2PHASE to R7413 per Intersil
Changed C7428 from 0.47uF => 0.33uF (132S0101) per Intersil
Changed component color to Green
Cosmetic cleanup
csa 90: Deleted net properties for =PD5V_S3_CAMERA
csa 98: Deleted net properties for =PPBUS_S0_LCDBKLT
csa 108: Added NET_PHYSICAL property to SATA_HDD_D2R_FILT_P and _N

2009-12-09: 1.5.0
multiple: Added parentheses for SYNC_DATE property on all pages that have broken sync.
csa 4: Deleted entry in Module Parts table for R6612, R6617, R6630, R6633 since they were removed when we switched from piezo to dynamic speakers
csa 69: Changed J6955 symbol to K87 Hall effect assembly (339S0114)

2009-12-10: 1.6.0
csa 69: Added OMIT to J6955, BOM table to stuff K84 Hall effect connector

2009-12-11: 1.7.0
csa 45: Added PLACEMENT_NOTE for passive deemphasis circuit.
csa 74: Changed 1PHASE BOM table to correctly call out 132S0080 (0.22uF) instead of 0.022uF

2009-12-16: 1.8.0
*** Resynced all synced pages and picked up the following (change notes from T27):
csa 18: T27: Swapped USB_EXTB and USB_EXTD for NVRN-612340 (pg. 18). <radar:7416825> Ensure USB_EXTB is on ports 8-11 (NVRN-612340)
T27: Changed USB_RBIAS from 931-ohms to 887-ohms per DG v1.3 (pg. 18). <radar:7459260 > Design Guide v1.3 updates
csa 20: T27: Added CKPLUS_WAIVE properties to dismiss false errors (pg. 20). <radar:7368529> TASK: Waive false CheckPlus errors
*** Started syncing the following pages:
csa 29,31: Began syncing from T27 per <radar:7424246 > BOM: K87 needs omit on J3100 and J2900 from T27
T27: Added BOMOPTIONs and APNs for Foxconn and Molex SO-DIMM connectors (pg. 29, 31).
csa 54: Began syncing from T27 per <radar:7432091 > BATT_ISENSE filter change to address lower max sink current on ISL6259 BMON pin (K17 auto-shutdown issue)
C5490 changed from CAP_402-0.022UF_10%_16V_CERM-X5R to CAP_402-0.022UF_20%_16V_CERM
T27: Added CKPLUS_WAIVE properties to dismiss false errors (pg. 54).
T27: Added gain note for US402 and SMC_BATT_ISENSE (pg. 54).
T27: Changed RC balance on BATT_ISENSE, same time constant (pg. 54).
csa 57: Began syncing from T27 per <radar:7304029 > T27 schematic bom option for R5714 & R5030 to keep K87 in sync
R5714 has BOMOPTION_LED:K6_K69, and we need to substitute a different part on csa 4
*** Made the following changes to follow T27 on the following unsynced pages:
csa 25: T27: Removed R2575 & R2580 per DG v1.3 (pg. 25). per <radar:7459260 > Design Guide v1.3 updates
*** Other changes
csa 4: Added BOM table to substitute in parts that have BOMOPTION xxx:K6_K69 (to allow sync with T27)
Added R5714 (114S0125) to table with BOMOPTION LED:K86_K87

2009-12-17: 1.9.0
csa 4: Added BOM table entry for MCP89-A02 per <radar:7416858 > Task: Get part numbers for A02 rev.
Changed K87 MCP BOM group to call out MCP89-A02
csa 34: Changed U3440 from AP002 part to AP016 (343S0511) per <radar:7459498> BOM: APN updates for FPF1009 and SAK parts
Changed R3454 to 100k, 1% (114S0411) to match T27 and K69
Updated DLY text note for U3440 to match T27
Changed R3440 color to green, deleted WF text note about needing PU
csa 72: Changed L7220 from 152S0693 to 152S0778 per <rdar://problem/7347216> K69 L7260 combo footprint
Alternates table on csa 4 already has 152S0778 as alternate to 152S0693

2009-12-22: 1.10.0
csa 4: Per <rdar://problem/7473229> K86: Move to MCP83
Added BOM table entry for MCP83M (337S3876)
This is for K86 ONLY. Adding entry to minimize delta on csa 4 between K87 and K86
BOMOPTION is "MCP83M"
Per <rdar://problem/7495072> K87: Call out LED:K86_K87 BOMOPTION in the K87_MISC BOM group
Added LED:K86_K87 BOMOPTION to the K87_MISC BOM group
Per <rdar://problem/7495116> K87: remove ON Semi alternate for Q2300 (376S0624)
Removed table entry that says 376S0608 is an alternate for 376S0624
Per <rdar://problem/7495021> K86/K87: Replace "S" APNs with "T" APNs for programmed SMC and BR
Changed BOOTROM:PROG to call out 341T0251 (SUBASSY, IC, BOOT ROM, K86/K87)
Created SMC:PROG_K87 pointing to 341T0252 (SUBASSY, IC, SMC, K87)
Created SMC:PROG_K86 pointing to 341T0250 (SUBASSY, IC, SMC, K86)
Changed K87_PROGPARTS BOM group to point to SMC:PROG_K87
csa 69: Per <rdar://problem/7494087> K87: remove OMIT from J6955 and delete BOM table
Deleted BOM table for Hall effect assembly
Changed text note to say "HALL EFFECT ASSEMBLY"
Deleted OMIT BOMOPTION from J6955
Added text note with part numbers for components of the assembly
"Assembly APN: 339S0114
- BOM: 639-0680
- PCBF: 820-2861
- MCO: 056-3515
- Conn APN:518S0788"
csa 74: Cosmetic change, moved R7413, C7406 BOMOPTION label so they don't look like wire name
csa 78: Per <rdar://problem/7495008> K87: Add NOSTUFF to R7872 to disconnect U7870 from ALL_SYS_PWRGD
Changed BOMOPTION for R7872 from S0PGOOD_ISL to NOSTUFF

2010-01-06: 1.11.0
csa 7: Per <rdar://problem/7517432> K86/K87 functional net property needed on signals in schematics
Added the following functional test points under the J5100 LPC+SPI CONN FUNC_TEST group
LPCPLUS_GPIO
LPC_SERIRQ
SMC_TMS

2010-01-07: 1.12.0
csa 23: *** BROKE SYNC WITH T27
Per <rdar://problem/7519025> K86/K87: update all instances of 376S0786 schematic symbols
Updated Q2355 and Q2356 with new schematic symbols
Need to resync with T27 once the change has been made there
csa 70: Per <rdar://problem/7519048> K86/K87: Change U7000 to 353S2929
Changed U7000 from 353S2392 to 353S2929
Updated APN text note

2010-01-08: 2.0.0
csa 45: Per <rdar://problem/7524364> K86/K87: change SATA HDD D2R passive EQ values
Removed NOSTUFF from C4585, C4586
Removed OMIT from R4585, R4586
Deleted BOM table that stuffsdel the bypass option
Changed R4585, R4586 to 114S0065 (27.4 ohm, 1%)
Changed C4585, C4586 to 131S4713 (47pF, 5%)

2010-01-13: 2.1.0
csa 4: Per <rdar://problem/7540383> K86: Update CPU part number to 337S3792
Changed U1000 CPU:1.2GHZ BOMOPTION from 337S3779 to 337S3792

2010-01-13: 2.2.0
csa 4: Cosmetic: changed text sizes and alignment
Per <rdar://problem/7540522> K86/K87: Production Debug Components
Changed 085-1093 to call out K87_DEVEL_PVT instead of K87_DEVEL_ENG
Changed K87_COMMON to call out K87_DEBUG_PVT instead of K87_DEBUG_ENG
Diff from the two changes above:
Toggled:
VREFMRGN:YES ==> VREFMRGN:NO
BMON:ENG ==> BMON:PROD
BKLT:ENG ==> BKLT:PROD
SENS_R:ENG ==> SENS_R:PROD
Removed:
DEBUG_ADC, S0PGOOD_ISL, EFI_DEBUG, MCPPLL_LDO, EXT1V05, MCP_T_DIODE_SENSOR, XDP_CON
Unchanged:
LPCPLUS, DEVEL_BOM, SMC_DEBUG:YES, XDP
Added LPCPLUS_CON to K87_DEVEL_ENG (does not change BOM for DVT)
Changed all instances of K87_DEBUG_xxxx to K87_DEBUG:xxxx
Changed all instances of K87_DEVEL_xxxx to K87_DEVEL:xxxx
csa 51: (Per <rdar://problem/7540522> K86/K87: Production Debug Components)
Changed J5100 BOMOPTION from LPCPLUS to LPCPLUS_CON to unstuff connector at DVT

2010-01-15: 2.3.0
csa 74: Per <rdar://7525313 > K86 CPU loadline, OCP update
Keeping K86 and K87 pgs identical for CSA 74, modifying BOM table for IMVP 1 phase on K87's schematic to reflect changes for K86.
IMVP6:1PHASE BOM Table:
R7417 changed to 7.87K (APN 114S0305)
R7416 added to BOM Table, 16.9K, (APN 114S0236)
Added IMVP6:2PHASE BOM option to R7416 for K87's 13.7K

csa 74, csa 79: Per <rdar://7542674 > K86/K87 Text note change
Cleaned up text notes for 1phase, 2phase, and edp #s per radar request.

2010-01-18: 2.4.0
csa 4: Per <rdar://problem/7549122> K86/K87: Switch to new BOM group structure
Reverted back to ENG BOM, no longer PROD BOM (i.e. reverted much of 2.2.0 changes)
Changed BOM group structure to match that in the radar (see PDF attached to radar)
Net change was to move LPCPLUS to the 639 (from the 085)
Switching from Engineering to Production BOM should only require changing PROJECT_PHASE:DEV to PROJECT_PHASE:PROD
Per <rdar://problem/7544629> K86/K87: Update MCP83 description on csa_4
Changed description for 337S3876 to "IC,MCP83M-A02,31X31MM,BGA116A"
csa 23: Per <rdar://problem/7544657> K86/K87: Fix schematic symbol for Q2355, Q2356
*** Started syncing with K6
Syncing with K6 to pick up new symbols for Q2355 and Q2356
Should switch syncing back to T27 once it is updated there
csa 37: Per <rdar://problem/7548726> K86/K87 Ethernet series R's need to be 0 ohmed
Changed R3790-R3795 to 116S0004 (0-ohm, 0402) from 22-ohm

2010-01-19: 2.5.0
csa 37: Per <rdar://problem/7554342> K86/K87: Change L3720 to 152S1182
Changed L3720 to 152S1182 (IND,PWR,SHD,4.7UH,20%,0.91A,31X31X12MM) for lower ESR

2010-01-22: 2.6.0
csa 4: Per <rdar://problem/7571786> K86/K87: Add E3T EEE code for K86 to schematic
Added row to EEE table for E3T
Changed BOMOPTIONs to be mutually exclusive (changed "_" to ":")

2010-01-29: 2.7.0
*** Resynced with T27 and K6 (no differences)
*** Resynced Audio pages with the following changes:
-pg. 62, Changed R6211 to 22 Ohms
-pg. 66, added C6602
-pg. 67, no stuffed R6712 and R6713
csa 45: Per <rdar://problem/7561001> K87:EMC: Radiated Emissions: Right Audio emissions fail
Changed L4530, L4531 (APN 155S0137) to SIL connector pins
csa 97: Per <rdar://problem/7589365> K86/K87: Compensation settings change to provide more phase margin, reduce ripple
Changed R9725 from 22k to 10k (114S0315), and removed NOSTUFF
Changed C9705 from 8.2nF to 33nF (132S0131)
Changed C9706 from 120pF to 220pF (131S2225)

2010-02-02: 2.8.0
*** Resynced with T27 and K6 (no differences)
*** Resynced Audio pages with the following changes:
-pg. 67, added BOM options for U6700, R6712, and R6713 to support MAX14560 and MAX14504
csa 97: Changed R9710 from 7.32K 0402 1% to 7.68K (APN 114S0304) to support old K84 panel
csa 4: Added OLD_AUDIO_SWITCH BOM OPTION to K86_K87_COMMON1

2010-02-15: 2.9.0
2010-02-15: 2.10.0
csa 54: Broke sync with T27. Per <rdar://problem/7605797> K69/K86/K87 sensor IN1C unreliable
U5400 changed from OPA348 to OPA330. C5434 changed to NOSTUFF

2010-02-16: 2.11.0
Resync with T27 and K6. Clean up and rerelease schematic.

2010-02-18: 2.12.0
Per <rdar://7644836> K87 power component update
CSA 74: R7417 changed to 5.90K, C7428 changed to 0.47uF, C7434 changed to 0.033uF
CSA 75: R7572 changed to 147k
CSA 70: R7015 changed to 56.2K, C7015 changed to 1000pF, C7042 changed to 0.068uF

Per <rdar://7634730> K86/K87: add an RC on the LVDS_IG_BKL_PWM
CSA 97: R9725 changed to 200ohm, C9799 of 47pF added. R9726.1 connection moved to LVDS_IG_BKLPWM

2010-02-18: 2.16.0
Per <rdar://7676934> K86/K87: Hall eff documentation change. Substitute 607-6831 for doc purposes
CSA 69: J6955 BOMOPTION change to OMIT. Added BOM table with 607-6831 for J6955

Per <rdar://7488543> K86/K86 Task: Measure each Power supply in MLB
CSA 74: For K86 only: C7434 = 0.1uF added. R7417 changed to 8.25kohm
CSA 12: For K86 only: C1272 = 330uF added.

Per <rdar://7685202> K86/K87 schematic: change U9700 to 353S2965 for Freescale backlight issue
CSA 97: U9700 changed to APN 353S2965

2010-02-18: 2.17.0
Per <rdar://7696179> K86/K87: Switch cap jack part number for new connector cap
CSA 67: J6700 changed from APN 514-0718 to 514-0750

2010-02-25: 2.18.0
Per <rdar://7685811> K86/K87 schematic: add additional 639 for differentiation between Foxconn and Molex_DIMM connectors
CSA 4: MOLEX_DDR_CONN added to Module Parts, removed from Alternate table. Added second 639 and EEEE # to BOM table

2010-02-25: 2.19.0
Per <rdar://7678515> K87:EMC:ESD: System hangs on air/contact discharge to MPM connector
CSA 69: C6970, C6971, C6972 of 1000pF (APN 131S0222) added

SYNC_MASTER=K87_MLB SYNC_DATE=02/26/2010

PAGE TITLE
Revision History

Apple Inc.

DRAWING NUMBER 051-8407 SIZE D
REVISION A.0.0
BRANCH
PAGE 5 OF 109
SHEET 5 OF 76

NOTE: All page numbers are .csa, not PDF. See page 1 for .csa -> PDF mapping.

SYNC_MASTER=K87_MLB SYNC_DATE=02/26/2010

PAGE TITLE: Revision History

Apple Inc.

DRAWING NUMBER: 051-8407 SIZE: D

REVISION: A.0.0

BRANCH:

PAGE: 6 OF 109

SHEET: 6 OF 76

Functional Test Points

FAN CONNECTORS FUNC_TEST

TP12	TRUE	PP5V_S0	7 8 62
TP15	TRUE	FAN_RT_PWM	42
TP16	TRUE	FAN_RT_TACH	42

(NEED TO ADD 1 GND TP)

MIC FUNC_TEST

TP231	TRUE	BI_MIC_N	52 53 75
TP233	TRUE	BI_MIC_P	52 53 75
TP235	TRUE	BI_MIC_SHIELD	52 53

SPEAKER FUNC_TEST

TP227	TRUE	SPKRAMP_L_N_OUT	51 52
TP226	TRUE	SPKRAMP_L_P_OUT	51 52
TP228	TRUE	SPKRAMP_R_N_OUT	51 52
TP230	TRUE	SPKRAMP_R_P_OUT	51 52
TP229	TRUE	SPKRAMP_SUB_N_OUT	51 52
TP231	TRUE	SPKRAMP_SUB_P_OUT	51 52

LVDS FUNC_TEST

TP258	TRUE	PP3V3_S0_LCD_DDC_F	64
TP417	TRUE	PP3V3_SW_LCD_PANEL_F	7 64 (NEED 2 TP)
TP260	TRUE	PPVOUT_S0_LCDBKLT	7 46 64 67 (NEED 2 TP)
TP245	TRUE	LVDS_IG_DDC_CLK	9 64
TP262	TRUE	LVDS_IG_DDC_DATA	9 64
TP261	TRUE	LVDS_IG_A_DATA_N<0>	9 64 71
TP256	TRUE	LVDS_IG_A_DATA_P<0>	9 64 71
TP257	TRUE	LVDS_IG_A_DATA_N<1>	9 64 71
TP255	TRUE	LVDS_IG_A_DATA_P<1>	9 64 71
TP252	TRUE	LVDS_IG_A_DATA_N<2>	9 64 71
TP253	TRUE	LVDS_IG_A_DATA_P<2>	9 64 71
TP254	TRUE	LVDS_IG_A_CLK_F_N	64 75
TP250	TRUE	LVDS_IG_A_CLK_F_P	64 75
TP251	TRUE	LED_RETURN_1	64 67
TP313	TRUE	LED_RETURN_2	64 67
TP246	TRUE	LED_RETURN_3	64 67
TP247	TRUE	LED_RETURN_4	64 67
TP248	TRUE	LED_RETURN_5	64 67
TP249	TRUE	LED_RETURN_6	64 67
TP305	TRUE	PP5V_S3_CAMERA_F	7 64
TP297	TRUE	USB_CAMERA_CONN_P	64 75
TP294	TRUE	USB_CAMERA_CONN_N	64 75

(NEED TO ADD 5 GND TP)

SATA ODD CONN FUNC_TEST

TP264	TRUE	PP5V_SW_ODD	7 33 46 (NEED 4 TP)
TP268	TRUE	SMC_ODD_DETECT	33 35
TP269	TRUE	SATA_ODD_D2R_C_P	33 71
TP267	TRUE	SATA_ODD_D2R_C_N	33 71
TP265	TRUE	SATA_ODD_R2D_P	33 71
TP266	TRUE	SATA_ODD_R2D_N	33 71

(NEED TO ADD 4 GND TP)

SATA HDD/SIL FUNC_TEST

TP312	TRUE	PP5V_S0_HDD_FLT	7 33 (NEED 4 TP)
TP314	TRUE	SATA_HDD_R2D_P	33 71
TP315	TRUE	SATA_HDD_R2D_N	33 71
TP316	TRUE	SATA_HDD_D2R_C_P	33 71
TP317	TRUE	SATA_HDD_D2R_C_N	33 71
TP307	TRUE	SYS_LED_ANODE_R	33

(NEED TO ADD 4 GND TP)

BATT POWER CONN FUNC_TEST

TP322	TRUE	PPVBAT_G3H_CONN	54 55 (NEED 3 TP)
TP321	TRUE	SMBUS_SMC_BSA_SCL	38 74
TP320	TRUE	SMBUS_SMC_BSA_SDA	38 74
TP305	TRUE	SYS_DETECT_L	54

(NEED TO ADD 3 GND TP)

HALL EFFECT CONNECTOR FUNC_TEST

TP309	TRUE	PP3V42_G3H	7 8 (NEED 2 TP)
TP308	TRUE	SMC_LID_R	54

(NEED TO ADD 3 GND TP)

X16 WIRELESS CONN FUNC_TEST

TP383	TRUE	PP3V3_S3_BT_F	30
TP381	TRUE	CONN_PCIE_MINI_D2R_P	9 30 75
TP382	TRUE	CONN_PCIE_MINI_D2R_N	9 30 75
TP386	TRUE	CONN_PCIE_MINI_R2D_P	9 30 75
TP385	TRUE	CONN_PCIE_MINI_R2D_N	9 30 75
TP236	TRUE	PCIE_CLK100M_MINI_CONN_P	30 75
TP237	TRUE	PCIE_CLK100M_MINI_CONN_N	30 75
TP238	TRUE	PP3V3_WLAN (NEED 4 TP)	7 30
TP232	TRUE	PCIE_WAKE_L	16 30
TP240	TRUE	CONN_USB2_BT_P	30 75
TP239	TRUE	CONN_USB2_BT_N	30 75
TP273	TRUE	AP_CLKREQ_Q_L	30
TP389	TRUE	AP_RESET_CONN_L	30

(NEED TO ADD 4 GND TP)

IPD_FLEX_CONN FUNC_TEST

TP410	TRUE	PP3V3_S3	7 8
TP374	TRUE	PP18V5_S3	7 44
TP372	TRUE	Z2_CS_L	43 44
TP376	TRUE	Z2_DEBUG3	43 44
TP371	TRUE	Z2_MOSI	43 44
TP369	TRUE	Z2_MISO	43 44
TP368	TRUE	Z2_SCLK	43 44
TP361	TRUE	Z2_BOOST_EN	44
TP366	TRUE	Z2_HOST_INTN	43 44
TP365	TRUE	Z2_CLKIN	43 44
TP363	TRUE	Z2_KEY_ACT_L	43 44
TP364	TRUE	Z2_RESET	43 44
TP362	TRUE	PSOC_MISO	43 44
TP360	TRUE	PSOC_MOSI	43 44
TP359	TRUE	PSOC_SCLK	43 44
TP357	TRUE	SMBUS_SMC_A_S3_SDA	38 74
TP358	TRUE	SMBUS_SMC_A_S3_SCL	38 74
TP377	TRUE	PSOC_F_CS_L	43 44
TP378	TRUE	PICKB_L	43 44

(NEED TO ADD 2 GND TP)

KEYBOARD CONN FUNC_TEST

TP354	TRUE	PP3V3_S3	7 8
TP355	TRUE	PP3V42_G3H	7 8
TP344	TRUE	WS_KBD1	43
TP345	TRUE	WS_KBD2	43
TP346	TRUE	WS_KBD3	43
TP347	TRUE	WS_KBD4	43
TP349	TRUE	WS_KBD5	43
TP348	TRUE	WS_KBD6	43
TP350	TRUE	WS_KBD7	43
TP352	TRUE	WS_KBD8	43
TP351	TRUE	WS_KBD9	43
TP353	TRUE	WS_KBD10	43
TP327	TRUE	WS_KBD11	43
TP328	TRUE	WS_KBD12	43
TP329	TRUE	WS_KBD13	43
TP343	TRUE	WS_KBD14	43
TP342	TRUE	WS_KBD15_CAP	43
TP341	TRUE	WS_KBD16_NUM	43
TP339	TRUE	WS_KBD17	43
TP340	TRUE	WS_KBD18	43
TP338	TRUE	WS_KBD19	43
TP336	TRUE	WS_KBD20	43
TP337	TRUE	WS_KBD21	43
TP333	TRUE	WS_KBD22	43
TP335	TRUE	WS_KBD23	43
TP334	TRUE	WS_KBD_ONOFF_L	43
TP332	TRUE	WS_LEFT_SHIFT_KBD	43
TP330	TRUE	WS_LEFT_OPTION_KBD	43
TP331	TRUE	WS_CONTROL_KBD	43

(NEED TO ADD 1 GND TP)

DC POWER CONN FUNC_TEST

TP312	TRUE	PP18V5_DCIN_FUSE (NEED 2 TP)	54
TP304	TRUE	ADAPTER_SENSE	54

(NEED TO ADD 2 GND TP)

POWER NETS FUNC_TEST

TP287	TRUE	PPVCORE_S0_CPU	8 39
TP285	TRUE	PPVCORE_S0_MCP	8 39
TP288	TRUE	PP1V05_S0	8 62
TP281	TRUE	PP1V5_S0	8 62 75
TP282	TRUE	PP1V8_S0	8
TP276	TRUE	PP5V_S0	7 8 62
TP302	TRUE	PP5V_S0	7 8 62
TP283	TRUE	PP3V3_S0	8 62 75
TP279	TRUE	PP1V5R1V35_S3	8 75
TP278	TRUE	PP3V3_S3	7 8
TP270	TRUE	PP5V_S3	8
TP272	TRUE	PP3V3_S5	8 62 75
TP273	TRUE	PP3V42_G3H	7 8
TP274	TRUE	PPBUS_G3H	8 39
TP275	TRUE	PP0V9_ENET	8
TP277	TRUE	PP3V3_ENET	8
TP418	TRUE	PP3V3_G3_RTC	8 19 20 23
TP303	TRUE	PP3V3_WLAN	7 30
TP392	TRUE	PP5V_SW_ODD	7 33 46
TP391	TRUE	PP5V_S0_HDD_FLT	7 33
TP390	TRUE	PP3V3_S5_AVREF_SMC	35 36
TP389	TRUE	PP18V5_S3	7 44
TP388	TRUE	PP3V3_SW_LCD_PANEL_F	7 64
TP386	TRUE	PPVOUT_S0_LCDBKLT	7 46 64 67
TP385	TRUE	PP4V5_AUDIO_ANALOG	48
TP383	TRUE	SMC_PM_G2_EN	35 62
TP382	TRUE	PM_SLP_S4_L	19 35 36 62
TP381	TRUE	PM_SLP_S3_L	19 35 62 66
TP380	TRUE	PP5V_S3_CAMERA_F	7 64
TP397	TRUE	PP0V9_S5	8
TP409	TRUE	PPDDRVTT_S0	8
TP412	TRUE	PP1V05_S0_MCP_PLL_UF	8
TP411	TRUE	PPVTT_S3_DDR_BUF	8
TP413			

(NEED TO ADD 6 GND TP)

J5100 LPC+SPI CONN FUNC_TEST

TP423	TRUE	PP3V42_G3H	7 8
TP442	TRUE	SPI_CLK	37 72
TP440	TRUE	SPI_CS0_L	37 72
TP439	TRUE	SPI_MISO	19 37 72
TP441	TRUE	SPI_MOSI	37 72
TP443	TRUE	SPIROM_USE_MLB	19 37 47
TP437	TRUE	LPCPLUS_GPIO	19 37
TP438	TRUE	LPC_SERIRQ	19 35 37
TP436	TRUE	SMC_TMS	35 36 37

(NEED TO ADD 2 GND TP)

FSB SIGNALS WITH NOTEST

TP490	NO TEST=TRUE	FSB_A_L<35..3>	10 14 69
TP489	NO TEST=TRUE	FSB_ADS_L	10 14 69
TP486	NO TEST=TRUE	FSB_ADSTB_L<1..0>	10 14 69
TP491	NO TEST=TRUE	FSB_D_L<63..0>	10 14 69
TP492	NO TEST=TRUE	FSB_DINV_L<3..0>	10 14 69
TP494	NO TEST=TRUE	FSB_DSTB_L_N<3..0>	10 14 69
TP495	NO TEST=TRUE	FSB_DSTB_L_P<3..0>	10 14 69
TP496	NO TEST=TRUE	FSB_HIT_L	10 14 69
TP498	NO TEST=TRUE	FSB_HITM_L	10 14 69
TP497	NO TEST=TRUE	FSB_LOCK_L	10 14 69
TP488	NO TEST=TRUE	FSB_REQ_L<4..0>	10 14 69

SYNC_MASTER=K87_MLB SYNC_DATE=02/26/2010

PAGE TITLE: FUNC TEST

Apple Inc.

DRAWING NUMBER: 051-8407 SIZE: D

REVISION: A.0.0

BRANCH:

PAGE: 7 OF 109

SHEET: 7 OF 76

"S0,S0M" RAILS

58 =PPVCORE_S0_CPU_REG — (CPU VCORE PWR)
PPVCORE_S0_CPU — 7 39
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.3 MM
VOLTAGE=1.25V
MAKE_BASE=TRUE
=PPVCORE_S0_CPU — 11 12

60 =PPCPUVTT_S0_REG
PP1V05_S0 — 7 62
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PP1V05_S0_CPU — 10 11 12 13
=PP1V05_S0_MCP_FSB — 14 20 23
=PP1V05_S0_MCP_PE_DVDD — 8 23
=PP1V05_S0_MCP_AVDD_UF — 23
=PP1V05_S0_MCP_SATA_DVDD — 20 23
=PP1V05_S0_MCP_PLL_UF_R — 61
=PP1V05_S0_MCP_M2CLK_DLL — 15 23
=PP1V05_S0_MCP_PLL_IFP — 17 24
=PP1V05_S0_MCP_DP0_VDD — 17 24
=PP1V05_SW_MCP_FSB — 20 23

59 =PPMCPCORE_S0_REG — (MCP VCORE AFTER SENSE RES)
PPVCORE_S0_MCP — 7 39
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PPVCORE_S0_MCP — 20 23
=PPVCORE_S0_MCPGFXFET — 22

LVDDR VRef/VTT (0.75V/0.675V) Rails

57 =PPVTT_S0_DDR_LDO
PPDDRVTT_S0 — 7
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0.75V
MAKE_BASE=TRUE
=PPDDRVTT_S0_MEM_A — 26
=PPDDRVTT_S0_MEM_B — 27

57 29 =PPVTT_S3_DDR_BUF
PPVTT_S3_DDR_BUF — 7
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0.75V
MAKE_BASE=TRUE

63 =PP1V5_S0_FET
PP1V5_S0 — 7 62 75
MIN_LINE_WIDTH=1.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE
=PP1V5_S0_CPU — 11 12
=PP1V5_S0_MCP_PLL_VLDO — 61
=PP1V8R1V5_S0_AUDIO — 48
=PP3V3R1V5_S0_AUDIO — 48
=PP3V3R1V5_S0_MCP_HDA — 19 23

61 =PP1V8_S0_REG
PP1V8_S0 — 7
MIN_LINE_WIDTH=0.10MM
MIN_NECK_WIDTH=0.10MM
VOLTAGE=1.8V
MAKE_BASE=TRUE
=PP3V3R1V8_S0_MCP_IFP_VDD — 17 24

61 =PP1V05_S0_MCP_PLL_OR
PP1V05_S0_MCP_PLL_UF — 7
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PP1V05_S0_MCP_PLL_UF — 23

UNUSED MCP PE0[3:0] AVDD/DVDD

20 =PP1V05_S0_MCP_PE_DVDD0
20 =PP1V05_S0_MCP_PE_AVDD0
(SINCE PE0[3:0] IS NOT USED ON K6)

(CONNECTS TO MCP BALLS) 20 =PP1V05_S0_MCP_PE_DVDD1 — =PP1V05_S0_MCP_PE_DVDD — 8 23 (CONNECTS TO THE DECAPS)
(CONNECTS TO MCP BALLS) 20 =PP1V05_S0_MCP_PE_AVDD1 — PP1V05_S0_MCP_PE_AVDD — 23 (CONNECTS TO THE DECAPS)
MAKE_BASE=TRUE

63 =PP5V_S0_FET
PP5V_S0 — 7 62
MIN_LINE_WIDTH=0.30 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=5V
MAKE_BASE=TRUE
=PP5V_S0_HDD — 33
=PP5V_S0_MCPREG — 59
=PP5V_S0_MCPFSBFET — 22
=PP5VR3V3_S0_DPCADET — 66
=PP5V_S0_CPUVTTS0 — 60
=PP5V_S0_LPCPLUS — 37
=PP5V_S0_FAN_RT — 42
=PP5V_S0_CPU_IMVP — 58

63 =PP3V3_S0_FET
PP3V3_S0 — 7 62 75
MIN_LINE_WIDTH=0.30MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_S0_XDP — 13
=PP3V3_S0_MCP — 20 23
=PP3V3_S0_ODD — 33
=PP3V3_S0_SMBUS_SMC_0_S0 — 38
=PP3V3_S0_SMBUS_SMC_B_S0 — 38
=PP3V3_S0_SMBUS_MCP_0 — 38
=PP3V3_S0_FAN_RT — 42
=PP3V3_S0_AUDIO — 48 52 53
=PP3V3_S0_IMVP — 58
=PP3V3_S0_LCD_DDC — 64
=PP3V3_S0_MCP_GPIO — 17 18 19
=PP3V3_S0_MCP_PLL_UF — 23
=PP3V3_S0_MCP_HVDD — 20 23
=PP3V3_S0_SMC — 36
=PP3V3_S0_MCPTHMSNS — 41
=PP3V3_S0_CPUTHMSNS — 41
=PP3V3_S0_DPCONN — 66
=PPSPD_S0_MEM_A — 26
=PPSPD_S0_MEM_B — 27
=PP3V3_S0_PWRCTL — 62
=PP3V3_S0_CPUVTTISNS — 40
=PP3V3_S0_SMBUS_MCP_1 — 38
=PP3V3_S0_P1V8S0 — 61
=PP3V3_S0_MCP_PLL_VLDO — 61
=PP3V3_S0_MCPDDRISNS — 40
=PP3V3_S0_DEBUGROM — 37
=PP3V3_S0_MCPCOREISNS — 40

"ENET" RAILS

63 62 61 9 =PP3V3_ENET_FET
PP3V3_ENET — 7
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_ENET_PHY — 9 31
=PP3V3_ENET_MCP_PLL_MAC — 23
=PP3V3_ENET_MCP_RMGT — 9 18 20 23

ENET1V05:INT
R0814
0
1 2
5% 1/10W MF-LF 402
PP3V3_ENET_PHY_VDDREG
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_ENET_PHY_VDDREG — 31

63 =PP0V9_ENET_FET
PP0V9_ENET — 7
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.9V
MAKE_BASE=TRUE
=PP0V9_ENET_MCP_RMGT — 20 23

RTL8211_REGOUT
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2mm
VOLTAGE=1.05V
31 =RTL8211_REGOUT

ENET1V05:INT
R0812
0
1 2
402 5% 1/10W MF-LF
MAKE_BASE=TRUE
VOLTAGE=1.05V
PP1V05_ENET
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2mm

PP1V05_S0_REG
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2mm
VOLTAGE=1.05V
61 =PP1V05_S0_REG

ENET1V05:EXT
R0813
0
1 2
402 5% 1/10W MF-LF
=PP1V05_ENET_PHY — 31

FIX ME!! OUTPUT OF REGULATOR VALUES

"S3" RAILS

63 57 =PPDDR_S3_REG
PP1V5R1V35_S3
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.17 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE
=PPLVDDR_S3_MEM_A — 26
=PPLVDDR_S3_MEM_B — 27
0 MA =PP1V5R1V35_S3_MCP_MEM — 15
4250 MA =PP1V5R1V35_S0_MCPDDRFET — 21
=PPVIN_S0_DDRREG_LDO — 57

63 =PP3V3_S3_FET
PP3V3_S3 — 7
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_S3_SMBUS_SMC_A_S3 — 38
=PP3V3_S3_PDCISENS
=PP3V3_S3_VREFMRGN — 29
=PP3V3_S3_WLAN — 30
=PP3V3_S3_MCP_GPIO — 19
=PP3V3_S3_TPAD — 43 44
=PP3V3_S3_SMS — 45
=PP3V3_S3_BT — 30
=PP3V3_S3_SMBUS_SMC_MGMT — 38

56 =PP5V_S3_REG
PP5V_S3 — 7
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V
MAKE_BASE=TRUE
=PP5V_S3_EXTUSB — 34
=PP5V_S3_CAMERA — 64
=PP5V_S3_AUDIO_AMP — 51
=PP5V_S3_MCPDDRFET — 21
=PP5V_S3_AUDIO — 48 50 52
=PP5V_S3_DEBUG_ISNS — 46
=PP5V_S3_SYSLED — 36
=PP5V_S3_TPAD — 44
=PP5V_S3_ODD — 33
=PP5V_S3_DEBUG_ADC_AVDD — 46
=PP5V_S3_DEBUG_ADC_DVDD — 46
=PP5V_S3_P5VS0FET — 63
=PP5V_S3_DDRREG — 57

"S5" RAILS

61 =PP0V9_S5_REG
PP0V9_S5 — 7
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
105/241 MA =PP0V9_S5_MCP_VDD_AUXC — 20 23
=PP0V9_ENET_P0V9ENETFET — 63

56 =PP3V3_S5_REG
PP3V3_S5 — 7 62 75
MIN_LINE_WIDTH=0.30MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_S5_MCP_GPIO — 18 19
=PP3V3_S5_ROM — 47
=PP3V3_S0_LCD_PANEL — 64
=PP3V3_S5_MCP — 20 23
=PP3V3_S5_MCPPWRGD — 25
=PP3V3_S5_P3V3S3FET — 63
=PP3V3_S5_P3V3S0FET — 63
=PP3V3_S5_P0V9S5 — 61
=PP3V3_S5_P3V3ENETFET — 63
=PP3V3_S5_DP_PORT_PWR — 66
=PP3V3_S5_VMON — 62
=PP3V3_S5_P0V9ENETFET — 63

"G3H" RAILS

54 =PP3V42_G3H_REG
PP3V42_G3H — 7
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.42V
MAKE_BASE=TRUE
=PPVIN_S5_SMCVREF — 36
=PP3V42_G3H_SMBUS_SMC_BSA — 38
=PP3V42_G3H_PWRCTL — 62
=PP3V42_G3H_CHGR — 55 62
=PP3V42_G3H_SMCUSBMUX — 34
=PP3V42_G3H_TPAD — 43
=PP3V3_S5_SMC — 35 36
=PP3V3_S5_LPCPLUS — 37
PP3V3_G3_RTC — 7 19 20 23
=PP3V42_G3H_ONEWIRE — 54
=PP3V42_G3H_HALL — 54
=PP3V42_G3H_BMON_ISNS — 40

54 =PP18V5_DCIN_CONN
PP18V5_G3H
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.3 MM
VOLTAGE=18.5V
MAKE_BASE=TRUE
=PPDCIN_S5_CHGR — 55

55 =PPBUS_G3H
PPBUS_G3H — 7 39
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V
MAKE_BASE=TRUE
=PPVIN_S0_MCPCORE — 59
=PPBUS_S0_LCDBKLT — 68
=PPVIN_S5_3V3S5 — 56
=PPVIN_S3_5VS3 — 56
=PPBUS_S5_CPUREGS_ISNS_R — 40
=PPVIN_S3_DDRREG — 57

40 =PPBUS_S5_CPUREGS_ISNS
PPBUS_S5_IMVP_VTT_ISNS
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.3 MM
VOLTAGE=12.6V
MAKE_BASE=TRUE
=PPVIN_S0_CPUVTTS0 — 60
=PPVIN_S5_CPU_IMVP — 58

DIGITAL GROUND
GND
MIN_LINE_WIDTH=0.50MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=0V

SYNC_MASTER=K87_MLB — SYNC_DATE=02/26/2010
PAGE TITLE: Power Aliases
Apple Inc.
DRAWING NUMBER: 051-8407 — SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 8 OF 109
SHEET: 8 OF 76

HEATSINK STANDOFFS

Z0902
STDOFF-4.50D.98H-1.1-3.48-TH
LEFT OF CPU

Z0901
STDOFF-4.50D.98H-1.1-3.48-TH
ABOVE CPU

Z0903
STDOFF-4.50D.98H-1.1-3.48-TH
BELOW MCP

Z0904
STDOFF-4.50D.98H-1.1-3.48-TH
BELOW CPU

FAN STANDOFF

OMIT
Z0905
3P2R2P7

MLB MOUNTING (TO C. BRACKET) SCREW HOLES

OMIT
Z0906
3P2R2P7

OMIT
Z0907
3P2R2P7

MLB MOUNTING (TO TOPCASE) SCREW HOLES

OMIT
Z0911
3P2R2P7

OMIT
Z0910
3P2R2P7

LVDS CONNECTOR HOLE

OMIT
Z0913
3P2R2P7

EMI IO MEDIUM POGO PINS (870-1794)

OMIT
ZS0900
2.0DIA-MED-EMI-MLB-K84
SM

OMIT
ZS0901
2.0DIA-MED-EMI-MLB-K84
SM

OMIT
ZS0902
2.0DIA-MED-EMI-MLB-K84
SM

OMIT
ZS0908
2.0DIA-MED-EMI-MLB-K84
SM

OMIT
ZS0909
2.0DIA-MED-EMI-MLB-K84
SM

OMIT
ZS0911
2.0DIA-MED-EMI-MLB-K84
SM

OMIT
ZS0903
2.0DIA-MED-EMI-MLB-K84
SM

EMI TALL POGO PINS (870-1698)

OMIT
ZS0904
2.0DIA-TALL-EMI-MLB-M97-M98
SM

OMIT
ZS0905
2.0DIA-TALL-EMI-MLB-M97-M98
SM

OMIT
ZS0906
2.0DIA-TALL-EMI-MLB-M97-M98
SM

OMIT
ZS0907
2.0DIA-TALL-EMI-MLB-M97-M98
SM

OMIT
ZS0910
2.0DIA-TALL-EMI-MLB-M97-M98
SM

OMIT
ZS0912
2.0DIA-TALL-EMI-MLB-M97-M98
SM

OMIT
ZS0913
2.0DIA-TALL-EMI-MLB-M97-M98
SM

OMIT
ZS0914
2.0DIA-TALL-EMI-MLB-M97-M98
SM

OMIT
ZS0915
2.0DIA-TALL-EMI-MLB-M97-M98
SM

OMIT
ZS0919
2.0DIA-TALL-EMI-MLB-M97-M98
SM

EMI THINBC POGO PINS (870-1820)

OMIT
ZS0917
2.0DIA-MLB-THIN-BC-K84
SM

OMIT
ZS0918
2.0DIA-MLB-THIN-BC-K84
SM

OMIT
ZS0916
2.0DIA-MLB-THIN-BC-K84
SM

NOSTUFF
ZS0920
2.0DIA-MLB-THIN-BC-K84
SM

PCI-E ALIASES

30	PCIE_MINI_R2D_C_P	PCIE_AP_R2D_C_P	16 71
30	PCIE_MINI_R2D_C_N	PCIE_AP_R2D_C_N	16 71
75 30 7	CONN_PCIE_MINI_D2R_P	PCIE_AP_D2R_P	16 71
75 30 7	CONN_PCIE_MINI_D2R_N	PCIE_AP_D2R_N	16 71
30	PCIE_CLK100M_MINI_P	PCIE_CLK100M_AP_P	16 71
30	PCIE_CLK100M_MINI_N	PCIE_CLK100M_AP_N	16 71
75 30 7	CONN_PCIE_MINI_R2D_P	PCIE_AP_R2D_P	71
75 30 7	CONN_PCIE_MINI_R2D_N	PCIE_AP_R2D_N	71

MAKE_BASE=TRUE

UNUSED GPU LANES

16	=PEG_D2R_N<15:0>	NC_PEG_D2R_N<15:0>	
16	=PEG_D2R_P<15:0>	NC_PEG_D2R_P<15:0>	
16	=PEG_R2D_C_N<15:0>	NC_PEG_R2D_C_N<15:0>	
16	=PEG_R2D_C_P<15:0>	NC_PEG_R2D_C_P<15:0>	
71 16	PEG_CLK100M_P	TP_PEG_CLK100M_P	
71 16	PEG_CLK100M_N	TP_PEG_CLK100M_N	
16	PEG_CLKREQ_L	TP_PCIE_CLKREQ_L	

NO_TEST=TRUE
MAKE_BASE=TRUE

UNUSED FIREWIRE LANE

71 16	PCIE_FW_D2R_P	TP_PCIE_FW_D2R_P
71 16	PCIE_FW_D2R_N	TP_PCIE_FW_D2R_N
71 16	PCIE_FW_R2D_C_P	TP_PCIE_FW_R2D_C_P
71 16	PCIE_FW_R2D_C_N	TP_PCIE_FW_R2D_C_N
16	FW_PWR_EN	TP_FW_PWR_EN
16	FW_CLKREQ_L	TP_FW_CLKREQ_L
16	FW_PME_L	TP_FW_PME_L
71 16	PCIE_CLK100M_FW_P	TP_PCIE_CLK100M_FW_P
71 16	PCIE_CLK100M_FW_N	TP_PCIE_CLK100M_FW_N

MAKE_BASE=TRUE

UNUSED ETHERNET LANE

16	ENET_CLKREQ_L	TP_ENET_CLKREQ_L
71 16	PCIE_CLK100M_ENET_P	TP_PCIE_CLK100M_ENET_P
71 16	PCIE_CLK100M_ENET_N	TP_PCIE_CLK100M_ENET_N
71 16	PCIE_ENET_D2R_P	TP_PCIE_ENET_D2R_P
71 16	PCIE_ENET_D2R_N	TP_PCIE_ENET_D2R_N
71 16	PCIE_ENET_R2D_C_P	TP_PCIE_ENET_R2D_C_P
71 16	PCIE_ENET_R2D_C_N	TP_PCIE_ENET_R2D_C_N

MAKE_BASE=TRUE

R0970
100K
5%
1/16W
MF-LF
402

18 IN ENET_ENERGY_DET — 1 — 2 — =PP3V3_ENET_FET OUT 8 61 62 63

USB ALIASES

UNUSED USB PORTS

72 18	USB_EXTD_P	TP_USB_EXTD_P	
72 18	USB_EXTD_N	TP_USB_EXTD_N	
72 18	USB_EXTC_P	TP_USB_EXTC_P	
72 18	USB_EXTC_N	TP_USB_EXTC_N	
72 18	USB_MINI_P	TP_USB_MINI_P	
72 18	USB_MINI_N	TP_USB_MINI_N	
72 18	USB_SDCARD_P	TP_USB_SDCARD_P	
72 18	USB_SDCARD_N	TP_USB_SDCARD_N	
72 18	USB_WM_P	TP_USB_WM_P	
72 18	USB_WM_N	TP_USB_WM_N	
72 18	USB_IR_N	TP_USB_IR_N	
72 18	USB_IR_P	TP_USB_IR_P	
72 18	USB_T57_P	TP_USB_T57_P	
72 18	USB_T57_N	TP_USB_T57_N	

MAKE_BASE=TRUE

LVDS ALIASES

17	IN =MCP_IFPA_TXD_P<0..2>	LVDS_IG_A_DATA_P<0..2>	OUT 7 64 71
17	IN =MCP_IFPA_TXD_N<0..2>	LVDS_IG_A_DATA_N<0..2>	OUT 7 64 71
17	IN =MCP_IFPAB_DDC_CLK	LVDS_IG_DDC_CLK	OUT 7 64
17	BI =MCP_IFPAB_DDC_DATA	LVDS_IG_DDC_DATA	BI 7 64
17	IN =MCP_IFPA_TXD_P<3>	NC_LVDS_IG_A_DATA_P3	
17	IN =MCP_IFPA_TXD_N<3>	NC_LVDS_IG_A_DATA_N3	
17	IN =MCP_IFPB_TXC_P	NC_LVDS_IG_B_CLK_P	
17	IN =MCP_IFPB_TXC_N	NC_LVDS_IG_B_CLK_N	
17	IN =MCP_IFPB_TXD_P<0..3>	NC_LVDS_IG_B_DATA_P<0..3>	
17	IN =MCP_IFPB_TXD_N<0..3>	NC_LVDS_IG_B_DATA_N<0..3>	
17	IN LCD_IG_BKLT_PWM	LVDS_IG_BKL_PWM	OUT 67 68
17	IN LCD_IG_BKLT_EN	LVDS_IG_BKL_ON	OUT 68
17	IN LCD_IG_PWR_EN	LVDS_IG_PANEL_PWR	OUT 64
17	IN =MCP_IFPA_TXC_P	LVDS_IG_A_CLK_P	OUT 64 71
17	IN =MCP_IFPA_TXC_N	LVDS_IG_A_CLK_N	OUT 64 71

NO_TEST=TRUE
MAKE_BASE=TRUE

DISPLAY PORT ALIASES

17	IN DP_IG_ML0_P<0..3>	DP_EXT_ML_P<0..3>	OUT 66 75
		DP_IG_ML_P<0..3>	OUT 71
17	IN DP_IG_ML0_N<0..3>	DP_EXT_ML_N<0..3>	OUT 66 75
		DP_IG_ML_N<0..3>	OUT 71
17	BI DP_IG_AUX_CH0_P	DP_IG_AUX_CH_P	BI 65 71
17	BI DP_IG_AUX_CH0_N	DP_IG_AUX_CH_N	BI 65 71
17	IN DP_IG_ML1_P<0..3>	TP_DP_IG_ML1P<0..3>	
17	IN DP_IG_ML1_N<0..3>	TP_DP_IG_ML1N<0..3>	
17	BI DP_IG_AUX_CH1_P	TP_DP_IG_AUX_CH1P	
17	BI DP_IG_AUX_CH1_N	TP_DP_IG_AUX_CH1N	
17	OUT DP_IG_HPD0	DP_EXT_HPD	IN 66
65	BI DP_AUX_CH_C_N	DP_EXT_AUX_CH_C_N	BI 66 75
65	BI DP_AUX_CH_C_P	DP_EXT_AUX_CH_C_P	BI 66 75
65	OUT DP_CA_DET	DP_EXT_CA_DET	IN 66

MAKE_BASE=TRUE

R0940
100K
5%
1/16W
MF-LF
402

17 DP_IG_HPD1 — 1 — 2

MCP89 MISC ALIASES

19 IN MCP_MEM_VDD_SEL_1V5 — TP_MCP_MEM_VDD_SEL_1V5
MAKE_BASE=TRUE

ETHERNET ALIASES

18	TP_ENET_RESET_L	ENET_RESET_L	31 73
18	TP_MCP_CLK25M_BUF0_R	MCP_CLK25M_BUF0_R	MAKE_BASE=TRUE 31 73
18	TP_ENET_MDC	ENET_MDC	MAKE_BASE=TRUE 31 73
18	TP_ENET_TX_CTRL	ENET_TX_CTRL	MAKE_BASE=TRUE 31 73
18	TP_ENET_CLK125M_TXCLK	ENET_CLK125M_TXCLK	MAKE_BASE=TRUE 31 73
18	TP_ENET_TXD<0..3>	ENET_TXD<0..3>	MAKE_BASE=TRUE 31 73

MAKE_BASE=TRUE

31 8 =PP3V3_ENET_PHY

ENET1V05:INT
R0915
0
5%
1/16W
MF-LF
402

RTL8211_ENSWREG
MIN_LINE_WIDTH=0.4MM MIN_NECK_WIDTH=0.2mm MAKE_BASE=TRUE

ENET1V05:EXT
R0916
0
5%
1/16W
MF-LF
402

=RTL8211_ENSWREG OUT 31

MCP89 ETHERNET VREF

23 20 18 8 =PP3V3_ENET_MCP_RMGT

R0957
1.47K
1%
1/16W
MF-LF
402

MCP_RGMII_VREF OUT 18

R0958
1.47K
1%
1/16W
MF-LF
402

C0958
0.1UF
20%
10V
CERM
402

CPU FSB FREQUENCY STRAPS

69 10 IN CPU_BSEL<0:2> MAKE_BASE=TRUE — =MCP_BSEL<0:2> OUT 14

14 CPU_PECI_MCP — TP_CPU_PECI_MCP
MAKE_BASE=TRUE

BSEL<2..0>	FSB MHZ
0 0 0	266
0 0 1	133
0 1 0	200
0 1 1	(166)
1 0 0	333
1 0 1	100
1 1 0	(400)
1 1 1	(RSVD)

SMC ALIASES

35 SMC_SYS_KBDLED — TP_SMC_SYS_KBDLED
MAKE_BASE=TRUE

CHARGER SIGNAL

55 IN =CHGR_ACOK — SMC_BC_ACOK
MAKE_BASE=TRUE OUT 35 36 54

CPU VCORE ALIASES

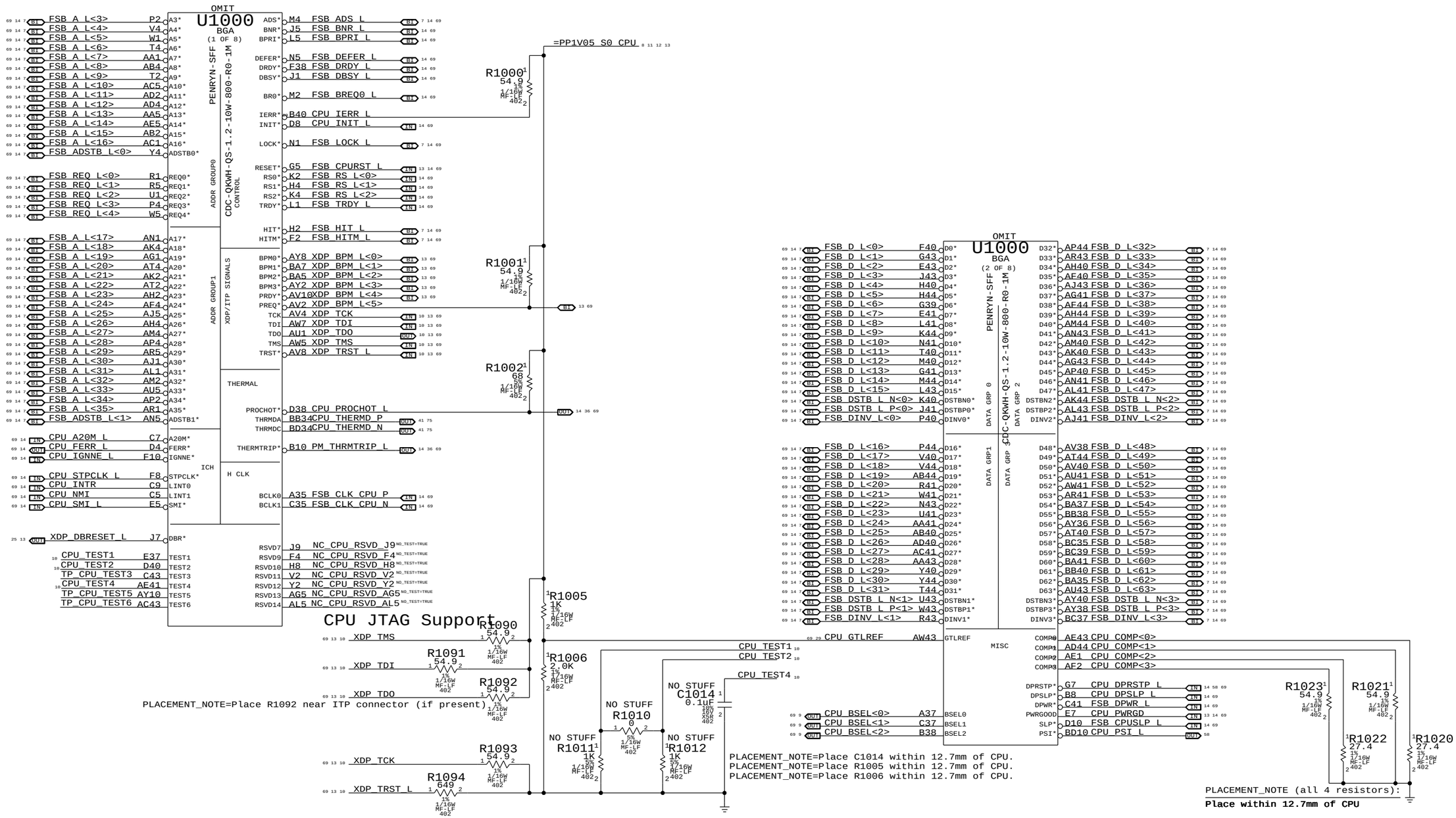
58 IN IMVP6_VR_TT — TP_IMVP6_VR_TT
58 IN IMVP6_NTC — TP_IMVP6_NTC
MAKE_BASE=TRUE

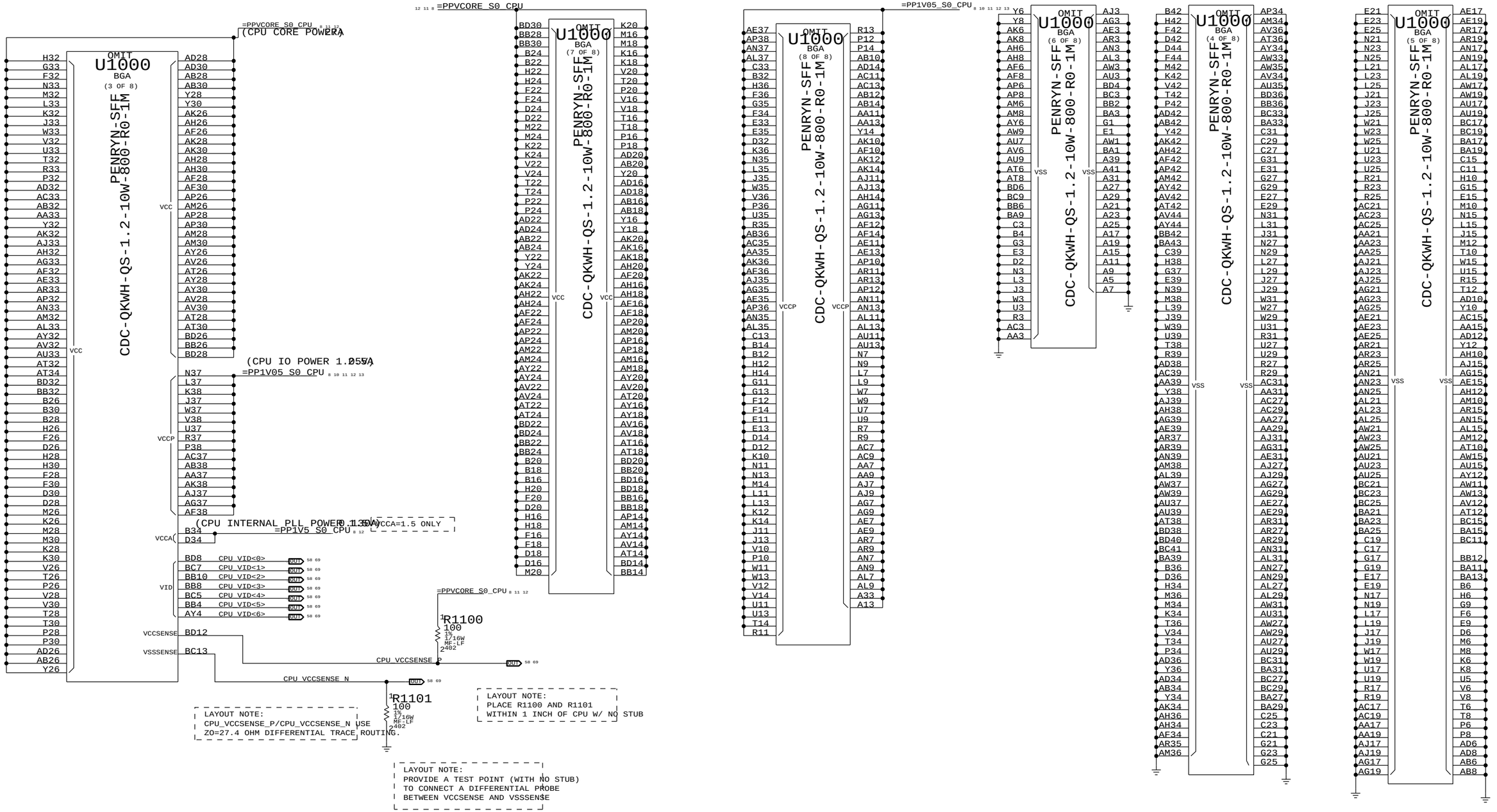
SYNC_MASTER=K87_MLB SYNC_DATE=02/26/2010

PAGE TITLE
SIGNAL ALIAS

Apple Inc.

DRAWING NUMBER 051-8407 SIZE D
REVISION A.0.0
BRANCH
PAGE 9 OF 109
SHEET 9 OF 76





SYNC MASTER=K83_MLB SYNC DATE=02/26/2010

PAGE TITLE

CPU Power & Ground

Apple Inc.

DRAWING NUMBER	051-8407
SIZE	D
REVISION	A.0.0
BRANCH	
PAGE	11 OF 109
SHEET	11 OF 76

CPU VCore HF and Bulk Decoupling

2X 470UF. 10X 22UF 0805 , 55X 4.7UF 0402

11 8 =PPVCORE_S0_CPU

PLACEMENT_NOTE (C1200-C1209):

Place inside socket cavity on secondary side.

CRITICAL C1200 22UF 20% 6.3V CERM-X5R 805
CRITICAL C1201 22UF 20% 6.3V CERM-X5R 805
CRITICAL C1202 22UF 20% 6.3V CERM-X5R 805
CRITICAL C1203 22UF 20% 6.3V CERM-X5R 805
CRITICAL C1204 22UF 20% 6.3V CERM-X5R 805
CRITICAL C1205 22UF 20% 6.3V CERM-X5R 805
CRITICAL C1206 22UF 20% 6.3V CERM-X5R 805
CRITICAL C1207 22UF 20% 6.3V CERM-X5R 805
CRITICAL C1208 22UF 20% 6.3V CERM-X5R 805
CRITICAL C1209 22UF 20% 6.3V CERM-X5R 805

Place inside socket cavity on secondary side.

CRITICAL C1210 4.7UF 20% 4V X5R-1 402
CRITICAL C1211 4.7UF 20% 4V X5R-1 402
CRITICAL C1212 4.7UF 20% 4V X5R-1 402
CRITICAL C1213 4.7UF 20% 4V X5R-1 402
CRITICAL C1214 4.7UF 20% 4V X5R-1 402
CRITICAL C1215 4.7UF 20% 4V X5R-1 402
CRITICAL C1216 4.7UF 20% 4V X5R-1 402
CRITICAL C1217 4.7UF 20% 4V X5R-1 402
CRITICAL C1218 4.7UF 20% 4V X5R-1 402
CRITICAL C1219 4.7UF 20% 4V X5R-1 402
CRITICAL C1220 4.7UF 20% 4V X5R-1 402

Place inside socket cavity on secondary side.

CRITICAL C1221 4.7UF 20% 4V X5R-1 402
CRITICAL C1222 4.7UF 20% 4V X5R-1 402
CRITICAL C1223 4.7UF 20% 4V X5R-1 402
CRITICAL C1224 4.7UF 20% 4V X5R-1 402
CRITICAL C1225 4.7UF 20% 4V X5R-1 402
CRITICAL C1226 4.7UF 20% 4V X5R-1 402
CRITICAL C1227 4.7UF 20% 4V X5R-1 402
CRITICAL C1228 4.7UF 20% 4V X5R-1 402
CRITICAL C1229 4.7UF 20% 4V X5R-1 402
CRITICAL C1230 4.7UF 20% 4V X5R-1 402
CRITICAL C1231 4.7UF 20% 4V X5R-1 402

Place inside socket cavity on secondary side.

CRITICAL C1232 4.7UF 20% 4V X5R-1 402
CRITICAL C1233 4.7UF 20% 4V X5R-1 402
CRITICAL C1234 4.7UF 20% 4V X5R-1 402
CRITICAL C1235 4.7UF 20% 4V X5R-1 402
CRITICAL C1236 4.7UF 20% 4V X5R-1 402
CRITICAL C1237 4.7UF 20% 4V X5R-1 402
CRITICAL C1238 4.7UF 20% 4V X5R-1 402
CRITICAL C1239 4.7UF 20% 4V X5R-1 402
CRITICAL C1240 4.7UF 20% 4V X5R-1 402
CRITICAL C1241 4.7UF 20% 4V X5R-1 402
CRITICAL C1242 4.7UF 20% 4V X5R-1 402

Place inside socket cavity on secondary side.

CRITICAL C1243 4.7UF 20% 4V X5R-1 402
CRITICAL C1244 4.7UF 20% 4V X5R-1 402
CRITICAL C1245 4.7UF 20% 4V X5R-1 402
CRITICAL C1246 4.7UF 20% 4V X5R-1 402
CRITICAL C1247 4.7UF 20% 4V X5R-1 402
CRITICAL C1248 4.7UF 20% 4V X5R-1 402
CRITICAL C1249 4.7UF 20% 4V X5R-1 402
CRITICAL C1250 4.7UF 20% 4V X5R-1 402
CRITICAL C1251 4.7UF 20% 4V X5R-1 402
CRITICAL C1252 4.7UF 20% 4V X5R-1 402
CRITICAL C1253 4.7UF 20% 4V X5R-1 402

Place inside socket cavity on secondary side.

CRITICAL C1254 4.7UF 20% 4V X5R-1 402
CRITICAL C1255 4.7UF 20% 4V X5R-1 402
CRITICAL C1256 4.7UF 20% 4V X5R-1 402
CRITICAL C1257 4.7UF 20% 4V X5R-1 402
CRITICAL C1258 4.7UF 20% 4V X5R-1 402
CRITICAL C1259 4.7UF 20% 4V X5R-1 402
CRITICAL C1260 4.7UF 20% 4V X5R-1 402
CRITICAL C1261 4.7UF 20% 4V X5R-1 402
CRITICAL C1262 4.7UF 20% 4V X5R-1 402
CRITICAL C1263 4.7UF 20% 4V X5R-1 402
CRITICAL C1264 4.7UF 20% 4V X5R-1 402

PLACEMENT_NOTE (C1240-C1243):

CRITICAL C1270 330UF-0.0045OHM 20% 2V POLY CASE-D2-SM
CRITICAL C1271 330UF-0.0045OHM 20% 2V POLY CASE-D2-SM
CRITICAL C1272 330UF-0.0045OHM 20% 2V POLY CASE-D2-SM

VCCA (CPU AVdd) DECOUPLING

1x 10uF, 1x 0.01uF

11 8 =PP1V5_S0_CPU

BYPASS=U1000.B26::4MM

C1280 10uF 20% 6.3V X5R 603
C1281 0.01UF 10% 16V CERM 402

VCCP (CPU I/O) DECOUPLING

1x 330uF, 6x 0.1uF 0402

13 11 10 8 =PP1V05_S0_CPU

CRITICAL C1290 330UF 20% 2.5V TANT CASE-B2-SM
C1291 0.1UF 20% 10V CERM 402
C1292 0.1UF 20% 10V CERM 402
C1293 0.1UF 20% 10V CERM 402
C1294 0.1UF 20% 10V CERM 402
C1295 0.1UF 20% 10V CERM 402
C1296 0.1UF 20% 10V CERM 402

SYNC MASTER=K83_MLB SYNC DATE=12/09/2009

PAGE TITLE: CPU Decoupling

Apple Inc.

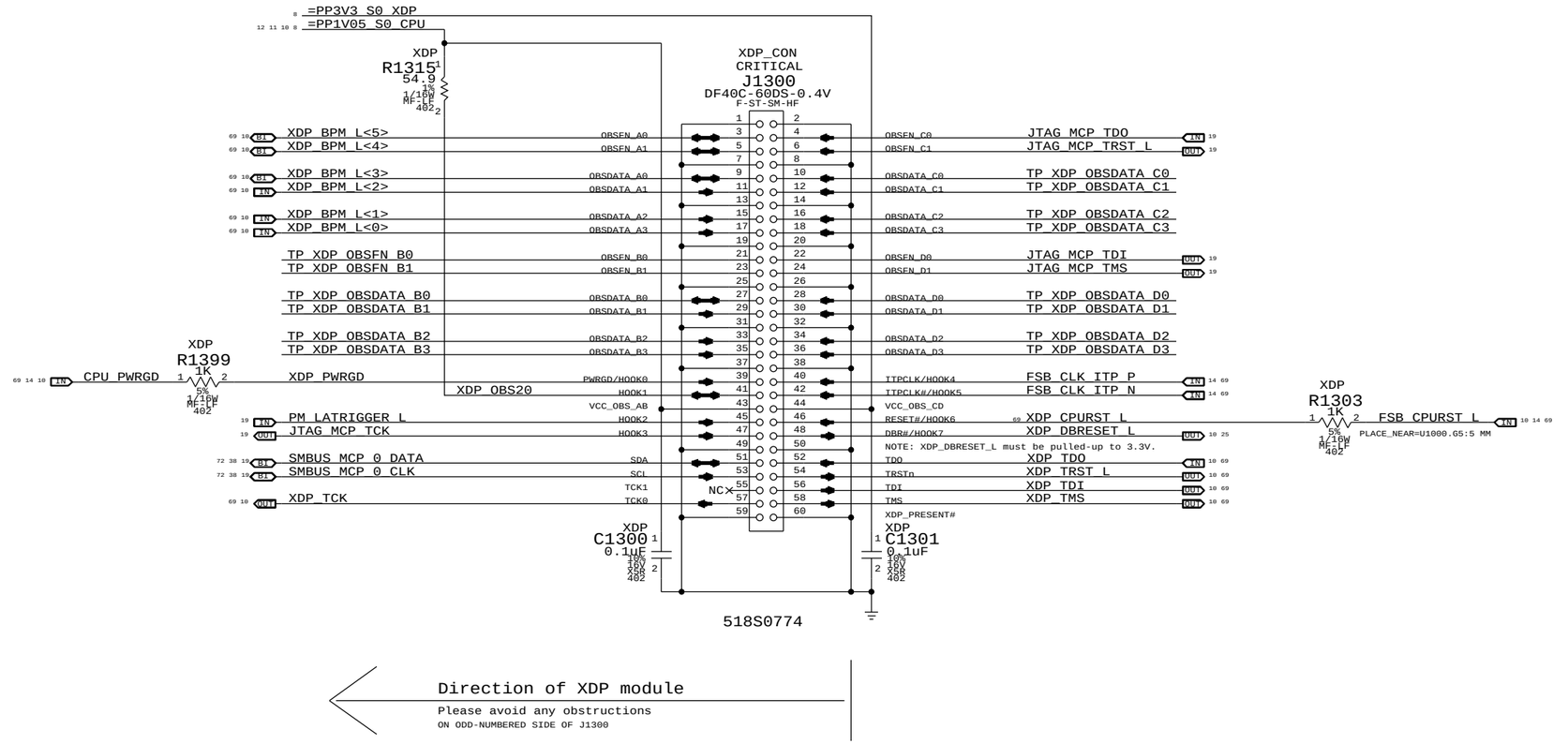
DRAWING NUMBER: 051-8407
SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 12 OF 109
SHEET: 12 OF 76

Mini-XDP Connector

NOTE: This is not the standard XDP pinout.

USE WITH 920-0782 ADAPTER FLEX TO SUPPORT CPU, MCP DEBUGGING.

MCP89-SPECIFIC PINOUT



518S0774

Direction of XDP module

Please avoid any obstructions

ON ODD-NUMBERED SIDE OF J1300

SYNC_MASTER=K87_MLB SYNC_DATE=12/09/2009

PAGE TITLE: eXtended Debug Port(MiniXDP)

Apple Inc.

DRAWING NUMBER: 051-8407 SIZE: D

REVISION: A.0.0

BRANCH:

PAGE: 13 OF 109

SHEET: 13 OF 76

OMIT

U1400
MCP89M-A01
FBGA
(1 OF 11)

FSB

FSB_DSTB_L_P<0>	K34	CPU_DSTBP0*	
FSB_DSTB_L_N<0>	K35	CPU_DSTBN0*	
FSB_DINV_L<0>	L37	CPU_DBI0*	
FSB_DSTB_L_P<1>	T31	CPU_DSTBP1*	
FSB_DSTB_L_N<1>	T30	CPU_DSTBN1*	
FSB_DINV_L<1>	P28	CPU_DBI1*	
FSB_DSTB_L_P<2>	K33	CPU_DSTBP2*	
FSB_DSTB_L_N<2>	K32	CPU_DSTBN2*	
FSB_DINV_L<2>	N35	CPU_DBI2*	
FSB_DSTB_L_P<3>	C36	CPU_DSTBP3*	
FSB_DSTB_L_N<3>	D36	CPU_DSTBN3*	
FSB_DINV_L<3>	A35	CPU_DBI3*	
FSB_A_L<3>	U38	CPU_A3*	
FSB_A_L<4>	U34	CPU_A4*	
FSB_A_L<5>	U35	CPU_A5*	
FSB_A_L<6>	T34	CPU_A6*	
FSB_A_L<7>	W37	CPU_A7*	
FSB_A_L<8>	W38	CPU_A8*	
FSB_A_L<9>	T37	CPU_A9*	
FSB_A_L<10>	Y38	CPU_A10*	
FSB_A_L<11>	W35	CPU_A11*	
FSB_A_L<12>	Y36	CPU_A12*	
FSB_A_L<13>	U33	CPU_A13*	
FSB_A_L<14>	W34	CPU_A14*	
FSB_A_L<15>	Y37	CPU_A15*	
FSB_A_L<16>	Y35	CPU_A16*	
FSB_A_L<17>	AF38	CPU_A17*	
FSB_A_L<18>	AB35	CPU_A18*	
FSB_A_L<19>	Y34	CPU_A19*	
FSB_A_L<20>	AE38	CPU_A20*	
FSB_A_L<21>	AC36	CPU_A21*	
FSB_A_L<22>	AF36	CPU_A22*	
FSB_A_L<23>	AC38	CPU_A23*	
FSB_A_L<24>	AB36	CPU_A24*	
FSB_A_L<25>	AB38	CPU_A25*	
FSB_A_L<26>	AB37	CPU_A26*	
FSB_A_L<27>	AC34	CPU_A27*	
FSB_A_L<28>	AE36	CPU_A28*	
FSB_A_L<29>	AF37	CPU_A29*	
FSB_A_L<30>	AC37	CPU_A30*	
FSB_A_L<31>	AC35	CPU_A31*	
FSB_A_L<32>	AE37	CPU_A32*	
FSB_A_L<33>	AE35	CPU_A33*	
FSB_A_L<34>	AE33	CPU_A34*	
FSB_A_L<35>	AE34	CPU_A35*	
FSB_ADSTB_L<0>	W36	CPU_ADSTB0*	
FSB_ADSTB_L<1>	AB34	CPU_ADSTB1*	
FSB_REQ_L<0>	U36	CPU_REQ0*	
FSB_REQ_L<1>	T36	CPU_REQ1*	
FSB_REQ_L<2>	U37	CPU_REQ2*	
FSB_REQ_L<3>	T38	CPU_REQ3*	
FSB_REQ_L<4>	T35	CPU_REQ4*	
FSB_ADS_L	AE31	CPU_ADS*	
FSB_BNR_L	AE32	CPU_BNR*	
FSB_BREQ0_L	AE30	CPU_BR0*	
FSB_DBSY_L	AE29	CPU_DBSY*	
FSB_DRDY_L	U29	CPU_DRDY*	
FSB_HIT_L	W32	CPU_HIT*	
FSB_HITM_L	AB31	CPU_HITM*	
FSB_LOCK_L	AC32	CPU_LOCK*	
FSB_TRDY_L	AC29	CPU_TRDY*	
CPU_PECI_MCP	AH34	CPU_PECI	
CPU_PROCHOT_L	U28	CPU_PROCHOT*	
	W33	CPU_THERMTRIP*	
	AB32	CPU_FERR*	
	B34	CPU_BSEL2	
	C34	CPU_BSEL1	
	A34	CPU_BSEL0	
FSB_RS_L<0>	AB29	CPU_RS0*	
FSB_RS_L<1>	AC33	CPU_RS1*	
FSB_RS_L<2>	AC31	CPU_RS2*	
MCP_BCLK_VML_COMP_VDD	AH37	BCLK_VML_COMP_VDD	
MCP_BCLK_VML_COMP_GND	AH38	BCLK_VML_COMP_GND	
MCP_CPU_COMP_VCC	AH36	CPU_COMP_VCC	
MCP_CPU_COMP_GND	AH35	CPU_COMP_GND	

CPU_D0*	N38	FSB_D_L<0>	
CPU_D1*	N36	FSB_D_L<1>	
CPU_D2*	P36	FSB_D_L<2>	
CPU_D3*	L36	FSB_D_L<3>	
CPU_D4*	N34	FSB_D_L<4>	
CPU_D5*	L35	FSB_D_L<5>	
CPU_D6*	P37	FSB_D_L<6>	
CPU_D7*	P38	FSB_D_L<7>	
CPU_D8*	N36	FSB_D_L<8>	
CPU_D9*	L34	FSB_D_L<9>	
CPU_D10*	K37	FSB_D_L<10>	
CPU_D11*	K36	FSB_D_L<11>	
CPU_D12*	K38	FSB_D_L<12>	
CPU_D13*	N37	FSB_D_L<13>	
CPU_D14*	H37	FSB_D_L<14>	
CPU_D15*	L38	FSB_D_L<15>	
CPU_D16*	N28	FSB_D_L<16>	
CPU_D17*	U30	FSB_D_L<17>	
CPU_D18*	N29	FSB_D_L<18>	
CPU_D19*	P34	FSB_D_L<19>	
CPU_D20*	T29	FSB_D_L<20>	
CPU_D21*	T32	FSB_D_L<21>	
CPU_D22*	U32	FSB_D_L<22>	
CPU_D23*	T33	FSB_D_L<23>	
CPU_D24*	P31	FSB_D_L<24>	
CPU_D25*	P30	FSB_D_L<25>	
CPU_D26*	N30	FSB_D_L<26>	
CPU_D27*	P33	FSB_D_L<27>	
CPU_D28*	N31	FSB_D_L<28>	
CPU_D29*	T28	FSB_D_L<29>	
CPU_D30*	P35	FSB_D_L<30>	
CPU_D31*	P29	FSB_D_L<31>	
CPU_D32*	H33	FSB_D_L<32>	
CPU_D33*	G34	FSB_D_L<33>	
CPU_D34*	L30	FSB_D_L<34>	
CPU_D35*	L31	FSB_D_L<35>	
CPU_D36*	L33	FSB_D_L<36>	
CPU_D37*	P32	FSB_D_L<37>	
CPU_D38*	N32	FSB_D_L<38>	
CPU_D39*	N33	FSB_D_L<39>	
CPU_D40*	H35	FSB_D_L<40>	
CPU_D41*	K31	FSB_D_L<41>	
CPU_D42*	H34	FSB_D_L<42>	
CPU_D43*	K30	FSB_D_L<43>	
CPU_D44*	L32	FSB_D_L<44>	
CPU_D45*	G33	FSB_D_L<45>	
CPU_D46*	H32	FSB_D_L<46>	
CPU_D47*	G35	FSB_D_L<47>	
CPU_D48*	C37	FSB_D_L<48>	
CPU_D49*	D37	FSB_D_L<49>	
CPU_D50*	H38	FSB_D_L<50>	
CPU_D51*	G38	FSB_D_L<51>	
CPU_D52*	G37	FSB_D_L<52>	
CPU_D53*	G36	FSB_D_L<53>	
CPU_D54*	B35	FSB_D_L<54>	
CPU_D55*	E35	FSB_D_L<55>	
CPU_D56*	B36	FSB_D_L<56>	
CPU_D57*	E36	FSB_D_L<57>	
CPU_D58*	C35	FSB_D_L<58>	
CPU_D59*	D34	FSB_D_L<59>	
CPU_D60*	E38	FSB_D_L<60>	
CPU_D61*	D38	FSB_D_L<61>	
CPU_D62*	E34	FSB_D_L<62>	
CPU_D63*	E37	FSB_D_L<63>	
CPU_BPRI*	Y31	FSB_BPRI_L	
CPU_DEFER*	Y30	FSB_DEFER_L	
BCLK_OUT_CPU_N	AF32	FSB_CLK_CPU_N	
BCLK_OUT_CPU_P	AF33	FSB_CLK_CPU_P	
BCLK_OUT_ITP_N	AF35	FSB_CLK_ITP_N	
BCLK_OUT_ITP_P	AF34	FSB_CLK_ITP_P	
BCLK_OUT_NB_N	AF28	FSB_CLK_MCP_N	
BCLK_OUT_NB_P	AF29	FSB_CLK_MCP_P	
BCLK_IN_P	AF30		
BCLK_IN_N	AF31		
CPU_A20M*	W30	CPU_A20M_L	
CPU_IGNNE*	AB30	CPU_IGNNE_L	
CPU_INIT*	AB28	CPU_INIT_L	
CPU_INTR	W31	CPU_INTR	
CPU_NMI	AC30	CPU_NMI	
CPU_SMI*	AC28	CPU_SMI_L	
CPU_PWRGD	Y32	CPU_PWRGD	
CPU_RESET*	AE28	FSB_CPURST_L	
CPU_DPRSLPVR	G1	PM_DPRSLPVR	
CPU_SLP*	Y33	FSB_CPUSLP_L	
CPU_DPSLP*	AB33	CPU_DPSLP_L	
CPU_DPWR*	U31	FSB_DPWR_L	
CPU_STPCLK*	Y29	CPU_STPCLK_L	
CPU_DPRSTP*	W29	CPU_DPRSTP_L	

=PP1V05_S0_MCP_FSB

R1410 54.9 1% 1/16W MF-LF 402
R1415 62 5% 1/16W MF-LF 402
R1430 49.9 1% 1/16W MF-LF 402
R1435 49.9 1% 1/16W MF-LF 402
R1431 49.9 1% 1/16W MF-LF 402
R1436 49.9 1% 1/16W MF-LF 402

PM_THRMTRIP_L
CPU_FERR_L
=MCP_BSEL<2>
=MCP_BSEL<1>
=MCP_BSEL<0>

Loop-back clock for delay matching.

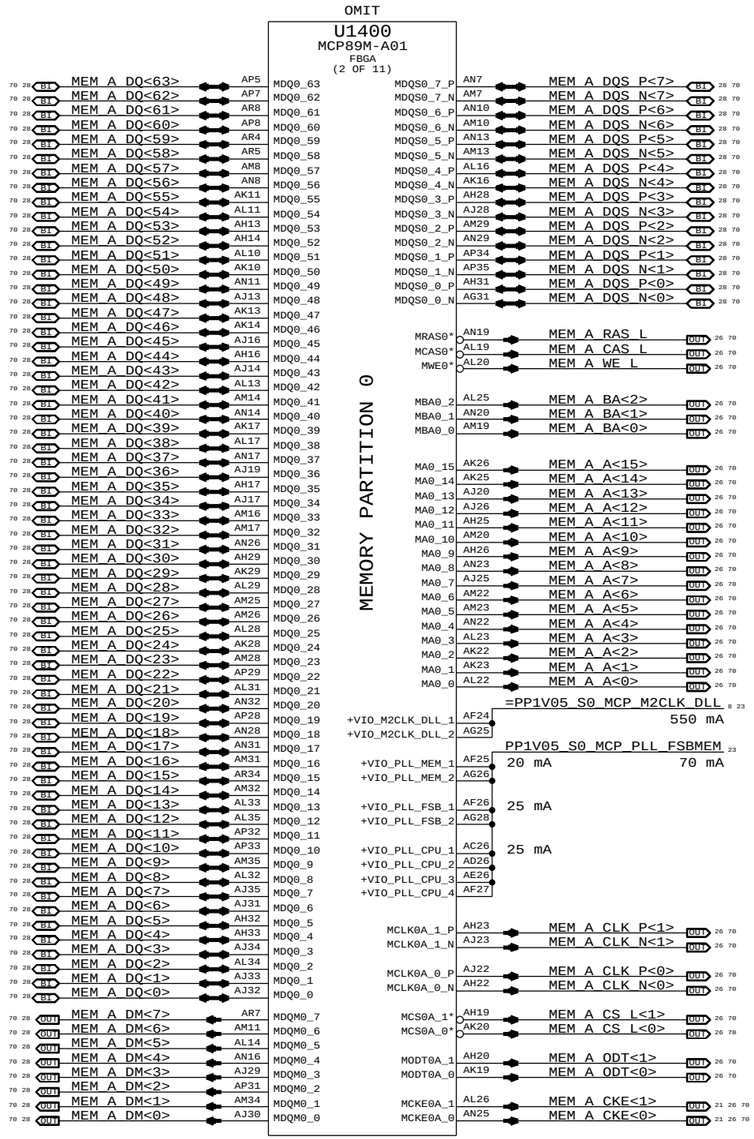
NO STUFF
R1440 150 5% 1/16W MF-LF 402

SYNC_MASTER=K87_MLB SYNC_DATE=02/26/2010

PAGE TITLE
MCP CPU Interface

Apple Inc.

DRAWING NUMBER 051-8407
SIZE D
REVISION A.0.0
BRANCH
PAGE 14 OF 109
SHEET 14 OF 76



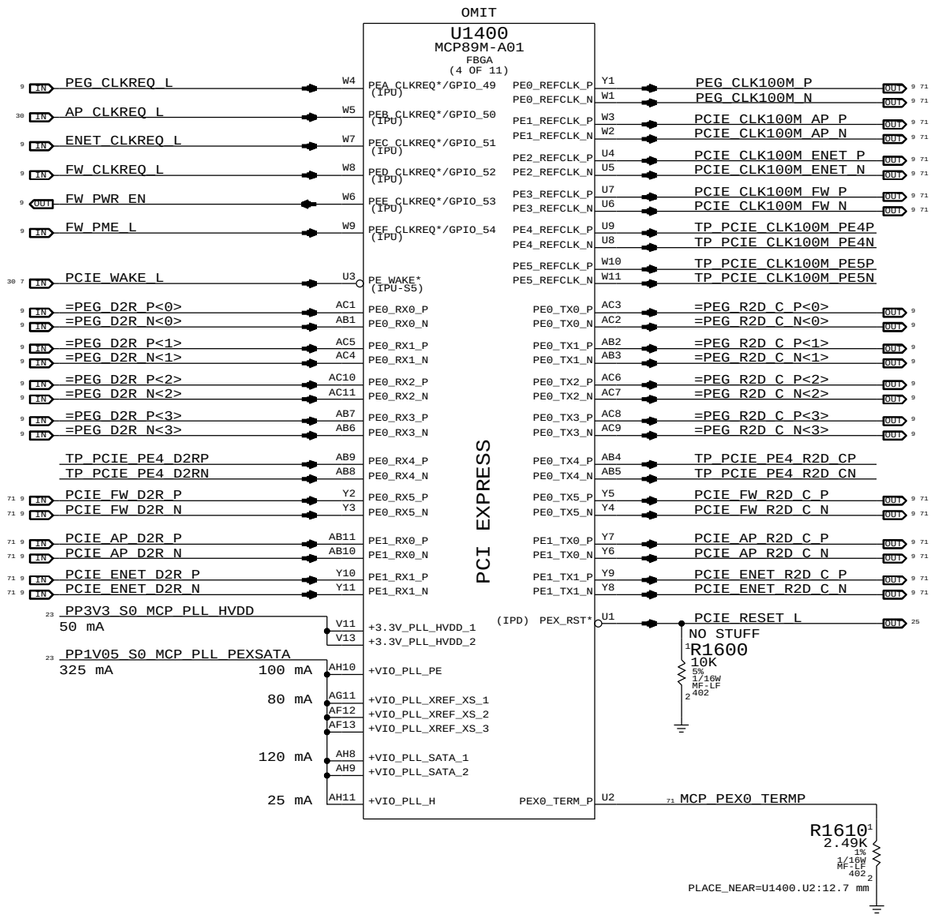
Current numbers from MCP89 A01 Bring-Up Support document (MCP89_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

SYNC_MASTER=K87_MLB SYNC_DATE=02/26/2010

PAGE TITLE
MCP Memory Interface

Apple Inc.

DRAWING NUMBER 051-8407 SIZE D
REVISION A.0.0
BRANCH
PAGE 15 OF 109
SHEET 15 OF 76



PE0 ports are Gen2-capable. 4 RCs: 4x, x2, x1, x1
PE1 ports are Gen1-only. 2 RCs: x1, x1

If PE0[3:0] are not used,
+VIO_PE_AVDD0 and +VIO_PE_DVDD0 can be GND

If PE0[4:5] and PE1[0:1] are not used,
+VIO_PE_AVDD1 and +VIO_PE_DVDD1 can be GND

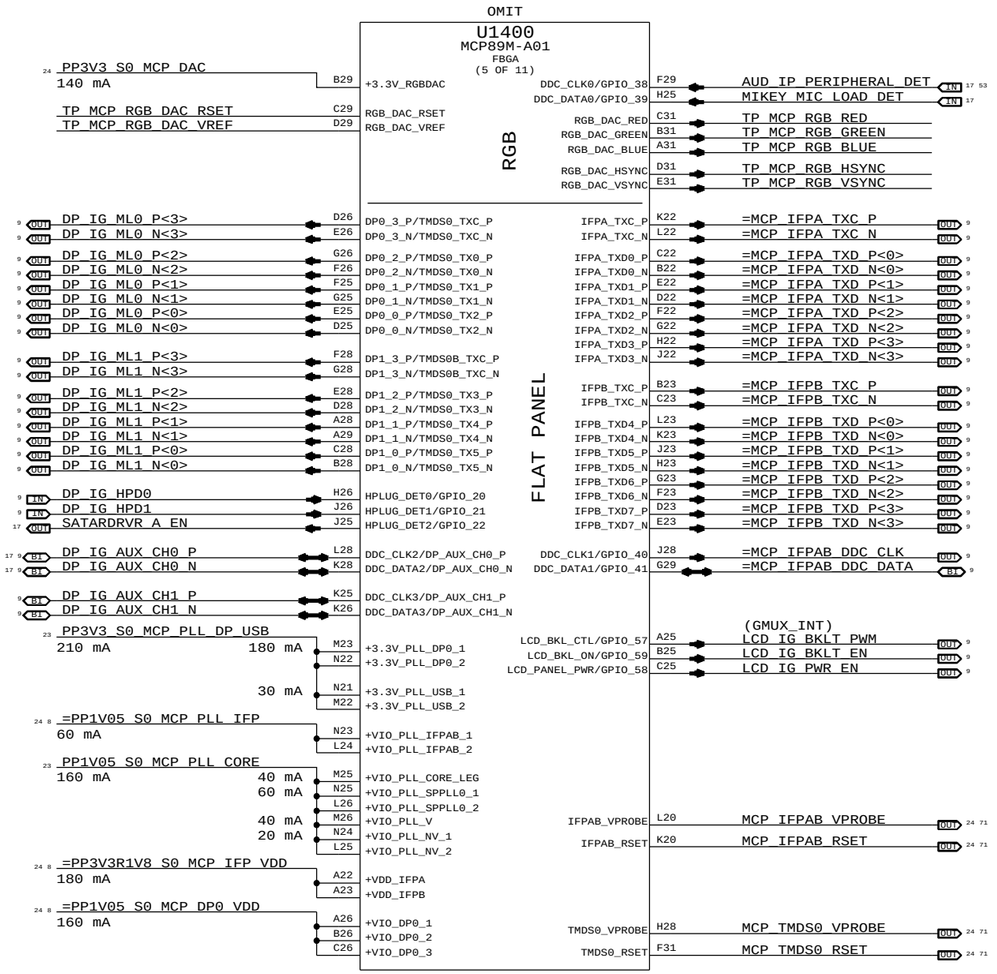
Current numbers from MCP89 A01 Bring-Up Support document (MCP89_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

SYNC_MASTER=K87_MLB SYNC_DATE=02/26/2010

PAGE TITLE: MCP PCIe Interfaces

Apple Inc.

DRAWING NUMBER: 051-8407 SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 16 OF 109
SHEET: 16 OF 76



NOTE: 100K pull-downs required if HPLUG_DET0/HPLUG_DET1 are not used.

RGB DAC Disable:

Okay to float all RGB_DAC signals.
DDC_CLK0/DDC_DATA0 pull-ups still required (or use as GPIOs).
Connect +3.3V_RGBDAC pin to GND.

NOTE: No Composite/S-Video/Component Video support on MCP89

Interface Mode

MCP Signal	TMDS/HDMI	LVDS
=MCP_IFPA_TXC_P/N	TMDS_IG_TXC_P/N	LVDS_IG_A_CLK_P/N
=MCP_IFPA_TXD_P/N<0>	TMDS_IG_TXD_P/N<0>	LVDS_IG_A_DATA_P/N<0>
=MCP_IFPA_TXD_P/N<1>	TMDS_IG_TXD_P/N<1>	LVDS_IG_A_DATA_P/N<1>
=MCP_IFPA_TXD_P/N<2>	TMDS_IG_TXD_P/N<2>	LVDS_IG_A_DATA_P/N<2>
=MCP_IFPA_TXD_P/N<3>	(UNUSED)	LVDS_IG_A_DATA_P/N<3>
=MCP_IFPB_TXC_P/N	(UNUSED)	LVDS_IG_B_CLK_P/N
=MCP_IFPB_TXD_P/N<0>	TMDS_IG_TXD_P/N<3>	LVDS_IG_B_DATA_P/N<0>
=MCP_IFPB_TXD_P/N<1>	TMDS_IG_TXD_P/N<4>	LVDS_IG_B_DATA_P/N<1>
=MCP_IFPB_TXD_P/N<2>	TMDS_IG_TXD_P/N<5>	LVDS_IG_B_DATA_P/N<2>
=MCP_IFPB_TXD_P/N<3>	(UNUSED)	LVDS_IG_B_DATA_P/N<3>
=MCP_IFPAB_DDC_CLK	TMDS_IG_DDC_CLK	LVDS_IG_DDC_CLK
=MCP_IFPAB_DDC_DATA	TMDS_IG_DDC_DATA	LVDS_IG_DDC_DATA

LVDS: Power +VDD_IFPx at 1.8V
TMDS: Power +VDD_IFPx at 3.3V

NOTE: TMDS/HDMI not supported on IFPA/B for MCP89 A01.

DDC Mode Pull-downs

NOTE: DP_AUX_CH1 also requires pull-downs if used for dual-mode DisplayPort (DP++). If unused no pulls are necessary, if used for TMDS/HDMI only then only pull-ups are necessary.

R1710 100K 5% 1/16W MF-LF 402 DP_IG_AUX_CH0_P
R1711 100K 5% 1/16W MF-LF 402 DP_IG_AUX_CH0_N

GPIO Pull-Ups

=PP3V3_S0_MCP_GPIO

R1780 10K 5% 1/16W MF-LF 402 SATARDRVR_A_EN
R1781 10K 5% 1/16W MF-LF 402 AUD_IP_PERIPHERAL_DET
R1782 10K 5% 1/16W MF-LF 402 MIKEY_MIC_LOAD_DET

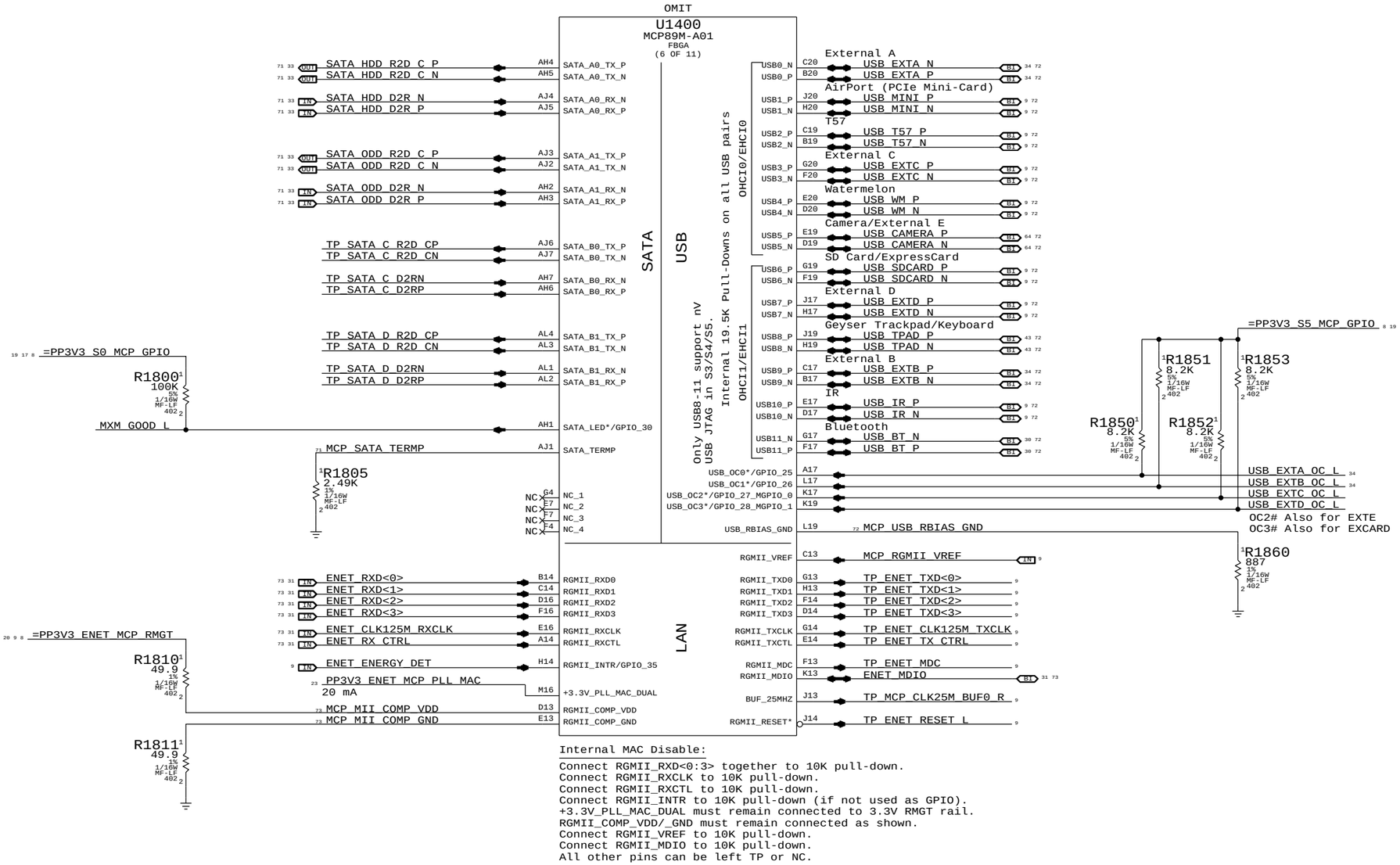
Current numbers from MCP89 A01 Bring-Up Support document (MCP89_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

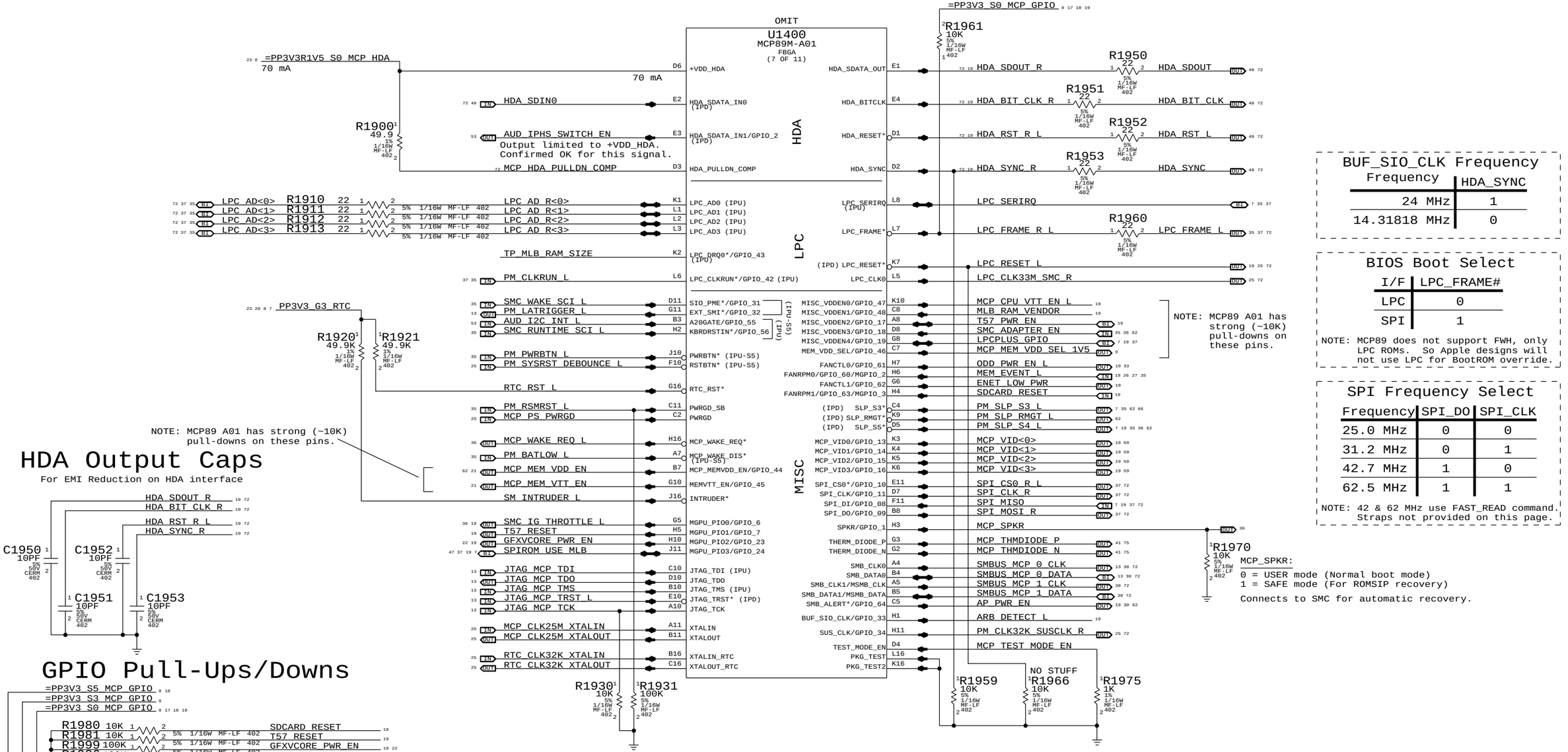
SYNC_MASTER=K87_MLB SYNC_DATE=02/26/2010

PAGE TITLE: MCP Graphics

Apple Inc.

DRAWING NUMBER: 051-8407 SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 17 OF 109
SHEET: 17 OF 76





Current numbers from MCP89 A01 Bring-Up Support document (MCP89_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

NOTE: "SW" rails are dynamically switched in the S0 state as needed, controlled by MCP89 GPIOs.

OMIT

U1400
MCP89M-A01
FBGA
(8 OF 11)
POWER I

G32	+VTT_CPU_1	+VDD_MEM_1	AG14
K29	+VTT_CPU_2	+VDD_MEM_2	AL7
D32	+VTT_CPU_3	+VDD_MEM_3	AF18
L29	+VTT_CPU_4	+VDD_MEM_4	AF21
Y26	+VTT_CPU_5	+VDD_MEM_5	AM1
V26	+VTT_CPU_6	+VDD_MEM_6	AM4
P27	+VTT_CPU_7	+VDD_MEM_7	AK8
T27	+VTT_CPU_8	+VDD_MEM_8	AG13
J29	+VTT_CPU_9	+VDD_MEM_9	AF16
N27	+VTT_CPU_10	+VDD_MEM_10	AF22
P26	+VTT_CPU_11	+VDD_MEM_11	AG20
F32	+VTT_CPU_12	+VDD_MEM_12	AM5
A32	+VTT_CPU_13	+VDD_MEM_13	AG19
H29	+VTT_CPU_14	+VDD_MEM_14	AF23
W26	+VTT_CPU_15	+VDD_MEM_15	AJ9
U27	+VTT_CPU_16	+VDD_MEM_16	AF19
G31	+VTT_CPU_17	+VDD_MEM_17	AG17
C32	+VTT_CPU_18	+VDD_MEM_18	AL6
E32	+VTT_CPU_19	+VDD_MEM_19	AG16
M28	+VTT_CPU_20	+VDD_MEM_20	AH12
H30	+VTT_CPU_21	+VDD_MEM_21	AM2
U26	+VTT_CPU_22	+VDD_MEM_22	AF15
T26	+VTT_CPU_23	+VDD_MEM_23	AM3
H31	+VTT_CPU_24	+VDD_MEM_24	AL5
B32	+VTT_CPU_25	+VDD_MEM_25	AL8
R26	+VTT_CPU_26	+VDD_MEM_26	AF17
N26	+VTT_CPU_27	+VDD_MEM_27	AJ11
		+VDD_MEM_28	AJ8
		+VDD_MEM_29	AF14
		+VDD_MEM_30	AJ10
		+VDD_MEM_31	AF20

23 8 =PP1V05_SW_MCP_FSB
2000 mA

=PP1V5R1V35_SW_MCP_MEM 15 21 23
4300 mA

23 14 8 =PP1V05_S0_MCP_FSB
200 mA

W27	+VTT_CPU2_1	
W28	+VTT_CPU2_2	
Y27	+VTT_CPU2_3	
Y28	+VTT_CPU2_4	

OMIT

U1400
MCP89M-A01
FBGA
(9 OF 11)
POWER II

T3	+VDD_COREA_1	+VDD_COREB_1	M4
AB22	+VDD_COREA_2	+VDD_COREB_2	M2
AB20	+VDD_COREA_3	+VDD_COREB_3	P4
R13	+VDD_COREA_4	+VDD_COREB_4	N12
R7	+VDD_COREA_5	+VDD_COREB_5	N4
T6	+VDD_COREA_6	+VDD_COREB_6	N14
T13	+VDD_COREA_7	+VDD_COREB_7	V20
R11	+VDD_COREA_8	+VDD_COREB_8	N10
AB17	+VDD_COREA_9	+VDD_COREB_9	P3
R10	+VDD_COREA_10	+VDD_COREB_10	P1
AB18	+VDD_COREA_11	+VDD_COREB_11	N11
T1	+VDD_COREA_12	+VDD_COREB_12	N6
T2	+VDD_COREA_13	+VDD_COREB_13	P6
AB21	+VDD_COREA_14	+VDD_COREB_14	N2
R4	+VDD_COREA_15	+VDD_COREB_15	N9
AB19	+VDD_COREA_16	+VDD_COREB_16	N8
P13	+VDD_COREA_17	+VDD_COREB_17	M10
R2	+VDD_COREA_18	+VDD_COREB_18	N3
T8	+VDD_COREA_19	+VDD_COREB_19	N1
R8	+VDD_COREA_20	+VDD_COREB_20	M5
T4	+VDD_COREA_21	+VDD_COREB_21	M7
R5	+VDD_COREA_22	+VDD_COREB_22	P2
T7	+VDD_COREA_23	+VDD_COREB_23	M8
T5	+VDD_COREA_24	+VDD_COREB_24	M11
T9	+VDD_COREA_25	+VDD_COREB_25	V19
U22	+VDD_COREA_26	+VDD_COREB_26	N7
V22	+VDD_COREA_27	+VDD_COREB_27	N16
W22	+VDD_COREA_28	+VDD_COREB_28	P5
Y22	+VDD_COREA_29	+VDD_COREB_29	N5
AA22	+VDD_COREA_30	+VDD_COREB_30	N13
P12	+VDD_COREA_31	+VDD_COREB_31	N15
P10	+VDD_COREA_32	+VDD_COREB_32	P9
P11	+VDD_COREA_33	+VDD_COREB_33	V17
		+VDD_COREB_34	V18
		+VDD_COREB_35	M14
		+VDD_COREB_36	M13
		+VDD_COREB_37	Y19
		+VDD_COREB_38	Y20
		+VDD_COREB_39	Y17
		+VDD_COREB_40	Y18
		+VDD_COREB_41	P7
		+VDD_COREB_42	P8

23 8 =PPVCORE_S0_MCP
8450 mA (0.85V)

=PPVCORE_SW_MCP_GFX 22 24
15350 mA (0.85V)

NOTE: VDD_COREx_SENSE signals should NOT be used for remote sensing unless COREA/COREB are powered by separate regulators.
Instead connect regulator sense point as close to COREB FET as possible.

TP_MCP_VDDCOREA_SENSEP	L10	+VDD_COREA_SENSE
TP_MCP_VDDCOREA_SENSEN	L9	GND_COREA_SENSE

8 =PP1V05_S0_MCP_PE_DVDD0
200 mA (DVDD0 & DVDD1)
(PE0[3:0])
Okay to GND if not using PE0[3:0]
CKPLUS_WAIVE=PwrTerm2Gnd

AF7	+VIO_PE_DVDD0_1	
AF8	+VIO_PE_DVDD0_2	
AE9	+VIO_PE_DVDD0_3	
AE10	+VIO_PE_DVDD0_4	

8 =PP1V05_S0_MCP_PE_DVDD1
200 mA (DVDD0 & DVDD1)
(PE0[5:4], PE1[1:0])

AE6	+VIO_PE_DVDD1_1	
AE7	+VIO_PE_DVDD1_2	
AE8	+VIO_PE_DVDD1_3	

8 =PP1V05_S0_MCP_PE_AVDD0
500 mA (AVDD0 & AVDD1)
(PE0[3:0])
Okay to GND if not using PE0[3:0]
CKPLUS_WAIVE=PwrTerm2Gnd

AC13	+VIO_PE_AVDD0_1	
AB12	+VIO_PE_AVDD0_2	
AC12	+VIO_PE_AVDD0_3	
AD11	+VIO_PE_AVDD0_4	
AD13	+VIO_PE_AVDD0_5	
AB13	+VIO_PE_AVDD0_6	

8 =PP1V05_S0_MCP_PE_AVDD1
500 mA (AVDD0 & AVDD1)
(PE0[5:4], PE1[1:0])

Y12	+VIO_PE_AVDD1_1	
Y13	+VIO_PE_AVDD1_2	
AA13	+VIO_PE_AVDD1_3	
W12	+VIO_PE_AVDD1_4	
W13	+VIO_PE_AVDD1_5	

23 8 =PP3V3_S0_MCP_HVDD
30 mA

T11	+3.3V_HVDD_1	
T12	+3.3V_HVDD_2	
U13	+3.3V_HVDD_3	

23 8 =PP3V3_S0_MCP
250 mA

U11	+3.3V_1	
U12	+3.3V_2	
F5	+3.3V_3	
E29	+3.3V_4	
E5	+3.3V_5	

23 8 =PP0V9_S5_MCP_VDD_AUXC
150 mA

L11	+VDD_DUAL_AUXC_1	
M17	+VDD_DUAL_AUXC_2	
M20	+VDD_DUAL_AUXC_3	

23 19 8 7 PP3V3_G3_RTC
?? uA (G3)
5 mA (S0)

A16	+3.3V_VBAT	

	+VIO_SATA_AVDD_1	AE1
	+VIO_SATA_AVDD_2	AE2
	+VIO_SATA_AVDD_3	AE3
	+VIO_SATA_AVDD_4	AE4
	+VIO_SATA_AVDD_5	AE5
	+VIO_SATA_DVDD_1	AF1
	+VIO_SATA_DVDD_2	AF2
	+VIO_SATA_DVDD_3	AF3
	+VIO_SATA_DVDD_4	AF4
	+VIO_SATA_DVDD_5	AF5
	+VIO_SATA_DVDD_6	AF6
	+VIO_SATA_DVDD_7	AF9
	+VIO_SATA_DVDD_8	AF10
	+VIO_SATA_DVDD_9	AF11
	+VIO_SATA_DVDD_10	AE11
	+VIO_SATA_DVDD_11	AE12
	+VIO_SATA_DVDD_12	AE13
	+VDD_DUAL_RMGT_1	L12
	+VDD_DUAL_RMGT_2	L13
	+3.3V_DUAL_RMGT_1	A13
	+3.3V_DUAL_RMGT_2	B13
	+3.3V_DUAL_USB_1	A20
	+3.3V_DUAL_USB_2	A19
	+3.3V_DUAL_1	F8
	+3.3V_DUAL_2	E8
+VDD_COREB_SENSE		U10
GND_COREB_SENSE		T10

TP_MCP_VDDCOREB_SENSEP
TP_MCP_VDDCOREB_SENSEN

PP1V05_S0_MCP_SATA_AVDD 23
300 mA

=PP1V05_S0_MCP_SATA_DVDD 8 23
100 mA

=PP0V9_ENET_MCP_RMGT 8 23
140 mA

=PP3V3_ENET_MCP_RMGT 8 9 18 23
300 mA

=PP3V3_S5_MCP 8 23
200 mA 240 mA

40 mA

OMIT

U1400
MCP89M-A01
FBGA
(10 OF 11)
GND

AP21	GND_1	GND_68	AD7
M37	GND_2	GND_69	B12
AM21	GND_3	GND_70	D12
AU37	GND_4	GND_71	E12
AC27	GND_5	GND_72	G12
D18	GND_6	GND_73	A2
B1	GND_7	GND_74	AL12
AD5	GND_8	GND_75	AM6
J2	GND_9	GND_76	AD37
AT1	GND_10	GND_77	AG32
AM30	GND_11	GND_78	H12
C1	GND_12	GND_79	AR35
AT3	GND_13	GND_80	H9
AP24	GND_14	GND_81	G24
AM33	GND_15	GND_82	V10
AE27	GND_16	GND_83	V5
AJ24	GND_17	GND_84	AL30
AH18	GND_18	GND_85	G7
AA8	GND_19	GND_86	V29
AM18	GND_20	GND_87	AP15
B6	GND_21	GND_88	AN2
J32	GND_22	GND_89	AJ12
AJ21	GND_23	GND_90	AR15
AK35	GND_24	GND_91	N20
H15	GND_25	GND_92	D21
D33	GND_26	GND_93	E21
B18	GND_27	GND_94	G21
M32	GND_28	GND_95	H21
B2	GND_29	GND_96	AR27
E6	GND_30	GND_97	AM27
J5	GND_31	GND_98	AP27
K18	GND_32	GND_99	AM15
AN34	GND_33	GND_100	AA31
AD10	GND_34	GND_101	AM9
F34	GND_35	GND_102	AH24
V8	GND_36	GND_103	K12
R35	GND_37	GND_104	J31
AR9	GND_38	GND_105	E30
AA2	GND_39	GND_106	AK7
AA10	GND_40	GND_107	V7
R32	GND_41	GND_108	M31
AG29	GND_42	GND_109	AU12
H8	GND_43	GND_110	AP6
AP12	GND_44	GND_111	B37
AM12	GND_45	GND_112	A36
AH21	GND_46	GND_113	F35
V32	GND_47	GND_114	L27
AR33	GND_48	GND_115	D35
J7	GND_49	GND_116	AL24
AA32	GND_50	GND_117	AP30
AG34	GND_51	GND_118	AH15
AK37	GND_52	GND_119	B21
K24	GND_53	GND_120	AV3
K21	GND_54	GND_121	AT38
J8	GND_55	GND_122	B38
AG8	GND_56	GND_123	AA21
AN5	GND_57	GND_124	AD4
V2	GND_58	GND_125	A37
AD32	GND_59	GND_126	AP18
AD2	GND_60	GND_127	AN4
D15	GND_61	GND_128	B24
AG2	GND_62	GND_129	D30
L15	GND_63	GND_130	V4
AK32	GND_64	GND_131	AA7
AR12	GND_65	GND_132	AD34
AN35	GND_66	GND_133	AK4
AN37	GND_67	GND_134	R37

OMIT

U1400
MCP89M-A01
FBGA
(11 OF 11)
GND

AU24	GND_135	GND_200	E33
AU15	GND_136	GND_201	M35
AG5	GND_137	GND_202	AV2
AD35	GND_138	GND_203	AK2
AJ18	GND_139	GND_204	AU6
AL18	GND_140	GND_205	F37
AR24	GND_141	GND_206	C3
AA5	GND_142	GND_207	J37
G18	GND_143	GND_208	V35
B9	GND_144	GND_209	G27
AU9	GND_145	GND_210	AA35
AM24	GND_146	GND_211	AU18
H24	GND_147	GND_212	AR6
B30	GND_148	GND_213	AV36
AR21	GND_149	GND_214	B33
D24	GND_150	GND_215	AJ27
AU30	GND_151	GND_216	G9
AK5	GND_152	GND_217	AG35
N18	GND_153	GND_218	AG7
E24	GND_154	GND_219	AD8
K15	GND_155	GND_220	AU2
M19	GND_156	GND_221	AP9
AH27	GND_157	GND_222	AD31
E18	GND_158	GND_223	V37
AA34	GND_159	GND_224	AA37
AK31	GND_160	GND_225	AG37
K11	GND_161	GND_226	AL15
AU21	GND_162	GND_227	AR18
V34	GND_163	GND_228	L14
AL21	GND_164	GND_229	K14
AA11	GND_165	GND_230	F2
M34	GND_166	GND_231	K27
B27	GND_167	GND_232	AL9
V28	GND_168	GND_233	AB26
C38	GND_169	GND_234	M29
D27	GND_170	GND_235	G30
R34	GND_171	GND_236	R28
J35	GND_172	GND_237	R29
AK34	GND_173	GND_238	R31
E15	GND_174	GND_239	U17
AR30	GND_175	GND_240	K8
AU33	GND_176	GND_241	Y21
J34	GND_177	GND_242	V31
AH30	GND_178	GND_243	U18
J4	GND_179	GND_244	W21
AU27	GND_180	GND_245	U19
AU1	GND_181	GND_246	W18
AG10	GND_182	GND_247	U20
E9	GND_183	GND_248	W17
E27	GND_184	GND_249	V21
L21	GND_185	GND_250	AA28
AU38	GND_186	GND_251	AA29
H18	GND_187	GND_252	N17
B15	GND_188	GND_253	AD28
AA4	GND_189	GND_254	AD29
AJ15	GND_190	GND_255	AG4
L18	GND_191	GND_256	W19
A3	GND_192	GND_257	W20
G15	GND_193	GND_258	AA26
AL27	GND_194	GND_259	AB27
AV37	GND_195	GND_260	AA17
D9	GND_196	GND_261	AA18
L4	GND_197	GND_262	AA19
N19	GND_198	GND_263	AA20
H27	GND_199	GND_264	U21

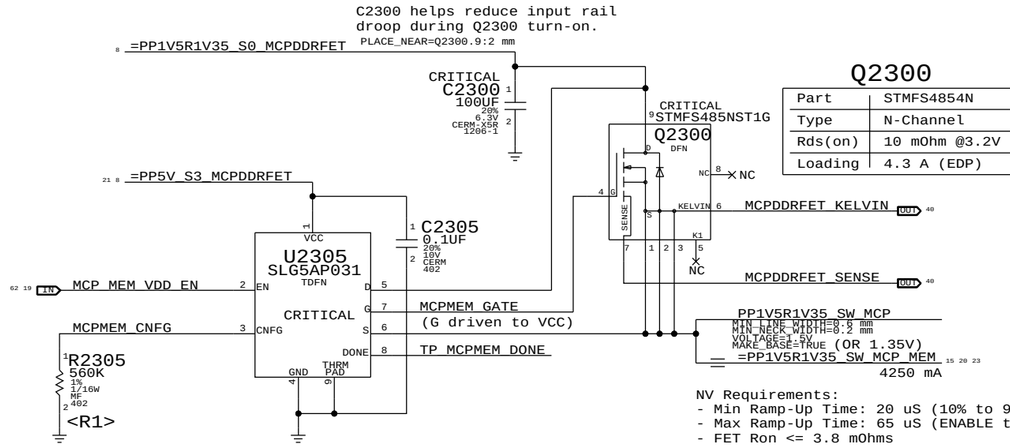
Current numbers from MCP89 A01 Bring-Up Support document (MCP89_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

SYNC_MASTER=K87_MLB SYNC_DATE=02/26/2010

PAGE TITLE
MCP Power & Ground

Apple Inc.

DRAWING NUMBER 051-8407
SIZE D
REVISION A.0.0
BRANCH
PAGE 20 OF 109
SHEET 20 OF 76

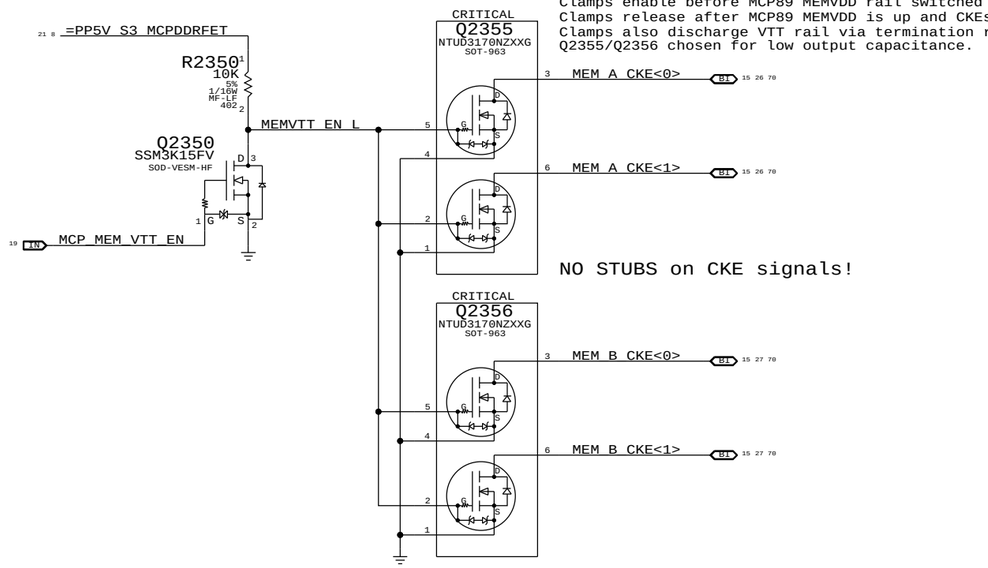


Q2300

Part	STMFS4854N
Type	N-Channel
Rds(on)	10 mOhm @3.2V
Loading	4.3 A (EDP)

DIMM CKE Clamps

CKE must be held low to keep memory in self-refresh.
Clamps enable before MCP89 MEMVDD rail switched off.
Clamps release after MCP89 MEMVDD is up and CKEs are driven by MCP89.
Clamps also discharge VTT rail via termination resistor on each CKE signal on DIMM.
Q2355/Q2356 chosen for low output capacitance.

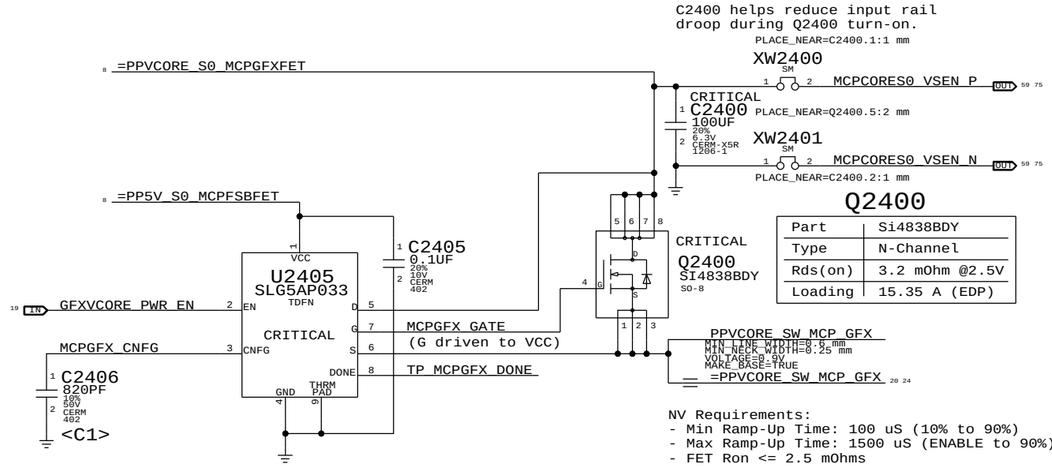


SYNC_MASTER=K87_MLB SYNC_DATE=02/26/2016

PAGE TITLE
MCP89 Memory Rail Gating

Apple Inc.

DRAWING NUMBER 051-8407 SIZE D
REVISION A.0.0
BRANCH
PAGE 23 OF 109
SHEET 21 OF 76



Q2400	
Part	Si4838BDY
Type	N-Channel
Rds(on)	3.2 mOhm @2.5V
Loading	15.35 A (EDP)

Approx. Ramp Time (EN to 1V, uS): 43.9 + 0.6943 * C1(pF)

NV Requirements:
- Min Ramp-Up Time: 100 uS (10% to 90%)
- Max Ramp-Up Time: 1500 uS (ENABLE to 90%)
- FET Ron <= 2.5 mOhms

NOTE: nVidia recommends Infineon BSC020N03MS for Q2400.

Gated Rail Savings: 860mW

SYNC_MASTER=K87_MLB SYNC_DATE=02/26/2010

PAGE TITLE
MCP89 GFX Core Rail Gating

Apple Inc.

DRAWING NUMBER 051-8407 SIZE D
REVISION A.0.0
BRANCH
PAGE 24 OF 109
SHEET 22 OF 76

MCP Non-GFX Core Power
=PPVCORE_S0_MCP
8450 mA (0.85V)
C2500 10UF 20% 6.3V X5R 603-1
C2501 4.7UF 20% 4V X5R 402
C2502 1UF 10% 10V X5R 402-1
C2503 0.22UF 20% 6.3V X5R 402
C2504 0.1UF 20% 10V CERM 402
C2505 0.1UF 20% 10V CERM 402
C2506 0.1UF 20% 10V CERM 402
C2507 0.1UF 20% 10V CERM 402
C2508 0.1UF 20% 10V CERM 402

MCP Memory Power
=PP1V5R1V35_SW_MCP_MEM
4300 mA (1.5V)
C2510 4.7UF 20% 4V X5R 402
C2511 0.1UF 20% 10V CERM 402
C2512 0.1UF 20% 10V CERM 402
C2513 0.1UF 20% 10V CERM 402
C2514 0.1UF 20% 10V CERM 402
C2515 0.1UF 20% 10V CERM 402
C2516 0.1UF 20% 10V CERM 402
C2517 0.1UF 20% 10V CERM 402
C2518 0.1UF 20% 10V CERM 402
C2519 0.1UF 20% 10V CERM 402

MCP CPU FSB (VTT) Power
=PP1V05_SW_MCP_FSB
2000 mA
C2520 10UF 20% 6.3V X5R 603-1
C2521 4.7UF 20% 4V X5R 402
C2522 1UF 10% 10V X5R 402-1
C2523 1UF 10% 10V X5R 402-1

MCP S0 FSB (VTT) Power
=PP1V05_S0_MCP_FSB
200 mA
C2524 4.7UF 20% 4V X5R 402
C2525 1UF 10% 10V X5R 402-1

MCP 0.9V AUX Core Power
=PP0V9_S5_MCP_VDD_AUXC
150 mA
C2526 0.1UF 20% 10V CERM 402
C2527 0.1UF 20% 10V CERM 402

MCP 0.9V MAC/SMU Power
=PP0V9_ENET_MCP_RMGT
140 mA
C2528 4.7UF 20% 4V X5R 402
C2529 0.1UF 20% 10V CERM 402

MCP 1.05V PCIE Digital Power
=PP1V05_S0_MCP_PE_DVDD
200 mA
C2530 2.2UF 20% 6.3V CERM 402-LF
C2531 1UF 10% 10V X5R 402-1
C2532 2.2UF 20% 6.3V CERM 402-LF
C2533 2.2UF 20% 6.3V CERM 402-LF
C2534 0.1UF 20% 10V CERM 402
C2535 0.1UF 20% 10V CERM 402

MCP 1.05V SATA Digital Power
=PP1V05_S0_MCP_SATA_DVDD
100 mA
C2536 4.7UF 20% 4V X5R 402
C2537 0.1UF 20% 10V CERM 402

MCP 1.05V Memory DLL Power
=PP1V05_S0_MCP_M2CLK_DLL
550 mA
C2540 4.7UF 20% 4V X5R 402

MCP 3.3V PCIe/SATA I/O PLL Power
=PP3V3_S0_MCP_HVDD
30 mA
C2541 4.7UF 20% 6.3V CERM 603
C2542 0.1UF 20% 10V CERM 402

MCP 3.3V I/O Power
=PP3V3_S0_MCP
250 mA
C2543 4.7UF 20% 6.3V CERM 603
C2544 0.1UF 20% 10V CERM 402
C2545 0.1UF 20% 10V CERM 402
C2546 0.1UF 20% 10V CERM 402
C2547 0.1UF 20% 10V CERM 402

MCP 3.3V/1.5V HDA Power
=PP3V3R1V5_S0_MCP_HDA
70 mA
C2548 4.7UF 20% 6.3V CERM 603
C2549 0.1UF 20% 10V CERM 402

MCP 3.3V AUX/USB Power
=PP3V3_S5_MCP
240 mA
C2550 4.7UF 20% 6.3V CERM 603
C2551 0.1UF 20% 10V CERM 402

MCP 2.0V-3.3V RTC Power
PP3V3_G3_RTC
? uA (G3)
5 mA (S0)
C2552 4.7UF 20% 6.3V CERM 603

MCP 3.3V MAC/SMU Power
=PP3V3_ENET_MCP_RMGT
300 mA
C2553 4.7UF 20% 6.3V CERM 603
C2554 0.1UF 20% 10V CERM 402

MCP 3.3V MAC PLL Power
=PP3V3_ENET_MCP_PLL_MAC
20 mA
CRITICAL
L2555 FERR-240-OHM-200MA 0402
C2555 4.7UF 20% 6.3V CERM 603
C2556 0.1UF 20% 10V CERM 402
PP3V3_ENET_MCP_PLL_MAC
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V

MCP 1.05V PCIe Analog Power
PP1V05_S0_MCP_PE_AVDD
=PP1V05_S0_MCP_AVDD_UF
800 mA
L2560 30-OHM-5A 0603
C2560 10UF 20% 6.3V X5R 603-1
C2561 4.7UF 20% 4V X5R 402
C2562 1UF 10% 10V X5R 402-1
C2563 1UF 10% 10V X5R 402-1
C2564 0.1UF 20% 10V CERM 402
C2565 0.1UF 20% 10V CERM 402
C2566 0.1UF 20% 10V CERM 402
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
500 mA

MCP 1.05V SATA Analog Power
PP1V05_S0_MCP_SATA_AVDD
L2567 30-OHM-5A 0603
C2567 10UF 20% 6.3V X5R 603-1
C2568 4.7UF 20% 4V X5R 402
C2569 0.1UF 20% 10V CERM 402
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
300 mA

MCP 1.05V CPU/FSB/MEM PLL Power
PP1V05_S0_MCP_PLL_FSBMEM
=PP1V05_S0_MCP_PLL_UF
555 mA
CRITICAL
L2570 220-OHM-2.2A 0603
C2570 4.7UF 20% 4V X5R 402
C2571 0.1UF 20% 10V CERM 402
C2572 0.1UF 20% 10V CERM 402
C2573 0.1UF 20% 10V CERM 402
R2570 0.33 5% 1/16W MF 0402
PLACE_NEAR=R2570.1:50 mil
GND_MCP_PLL_FSB
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=0V
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
70 mA

MCP 1.05V PCIe/SATA PLL Power
PP1V05_S0_MCP_PLL_PEXSATA
CRITICAL
L2575 220-OHM-2.2A 0603
C2575 4.7UF 20% 4V X5R 402
C2576 0.1UF 20% 10V CERM 402
C2577 0.1UF 20% 10V CERM 402
C2578 0.1UF 20% 10V CERM 402
C2579 0.1UF 20% 10V CERM 402
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
325 mA

MCP 1.05V Core/Misc PLL Power
PP1V05_S0_MCP_PLL_CORE
CRITICAL
L2580 220-OHM-2.2A 0603
C2580 4.7UF 20% 4V X5R 402
C2581 0.1UF 20% 10V CERM 402
C2582 0.1UF 20% 10V CERM 402
C2583 0.1UF 20% 10V CERM 402
C2584 0.1UF 20% 10V CERM 402
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
160 mA

MCP 3.3V PLL Power
PP3V3_S0_MCP_PLL_HVDD
=PP3V3_S0_MCP_PLL_UF
260 mA
CRITICAL
L2590 FERR-240-OHM-200MA 0402
C2590 4.7UF 20% 6.3V CERM 603
C2591 0.1UF 20% 10V CERM 402
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
50 mA

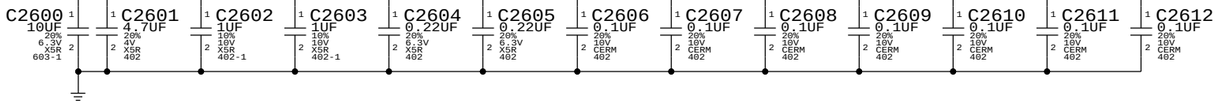
MCP 3.3V DP & USB PLL Power
PP3V3_S0_MCP_PLL_DP_USB
CRITICAL
L2595 220-OHM-2.2A 0603
C2595 4.7UF 20% 6.3V CERM 603
C2596 0.1UF 20% 10V CERM 402
C2597 0.1UF 20% 10V CERM 402
R2595 0.33 5% 1/16W MF 0402
PLACE_NEAR=R2595.1:50 mil
GND_MCP_PLL_DP_USB
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=0V
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
210 mA

DO NOT SYNC FROM T27. DECOUPLING CAP VALUES CHANGED.
Current numbers from MCP89 A01 Bring-Up Support document (MCP80_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

SYNC_MASTER=K87_MLB
SYNC_DATE=02/26/2010
PAGE TITLE
MCP Standard Decoupling
Apple Inc.
DRAWING NUMBER 051-8407
SIZE D
REVISION A.0.0
BRANCH
PAGE 25 OF 109
SHEET 23 OF 76

MCP GFX Core Power

22 20 =PPVCORE_SW_MCP_GFX
15350 mA (0.85V)



MCP 3.3V RGBDAC Power

GND_MCP_DAC_P3V3 = PP3V3_S0_MCP_DAC 17
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0V
MAKE_BASE=TRUE
140 mA

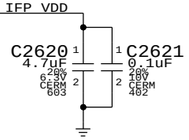
R2670 0 5% 1/16W MF-LF 402

If RGBDAC is used, requires ferrite (155S0382) plus 1x 4.7uF 0603 & 1x 0.1uF 0402 cap.

If RGBDAC is not used, tie to GND.

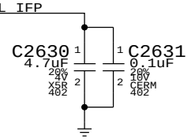
MCP 3.3V/1.8V IFP Interface Power

17 8 =PP3V3R1V8_S0_MCP_IFP_VDD
180 mA (1.8V LVDS)



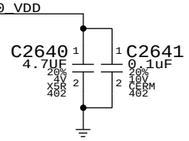
MCP 1.05V IFP PLL Power

17 8 =PP1V05_S0_MCP_PLL_IFP
60 mA

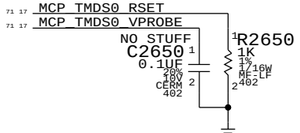


MCP 1.05V DisplayPort Power

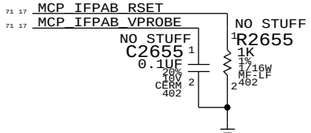
17 8 =PP1V05_S0_MCP_DP0_VDD
160 mA



71 17 MCP_TMDS0_RSET
71 17 MCP_TMDS0_VPROBE



71 17 MCP_IFPAB_RSET
71 17 MCP_IFPAB_VPROBE



Current numbers from MCP89 A01 Bring-Up Support document (MCP80_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

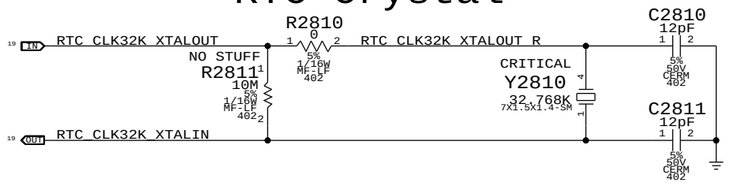
SYNC_MASTER=K87_MLB SYNC_DATE=02/26/2010

PAGE TITLE
MCP Graphics Support

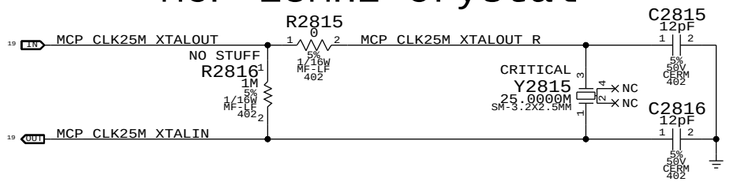
Apple Inc.

DRAWING NUMBER 051-8407 SIZE D
REVISION A.0.0
BRANCH
PAGE 26 OF 109
SHEET 24 OF 76

RTC Crystal

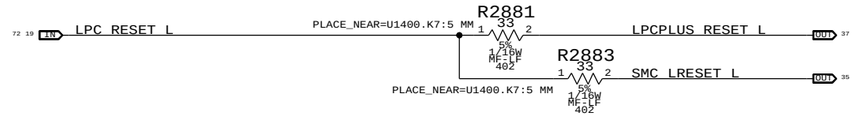


MCP 25MHz Crystal

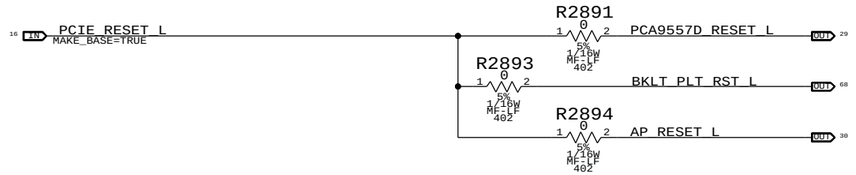


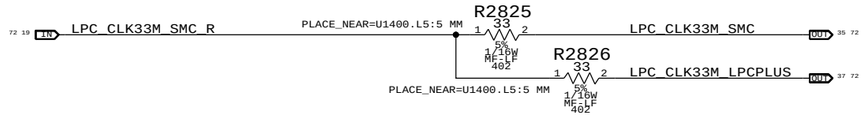
Platform Reset Connections

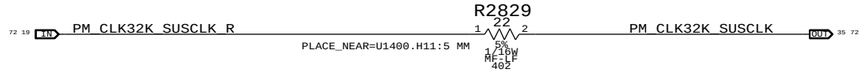
LPC Reset (Unbuffered)



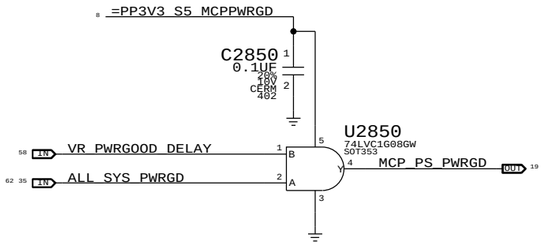
PCIE Reset (Unbuffered)



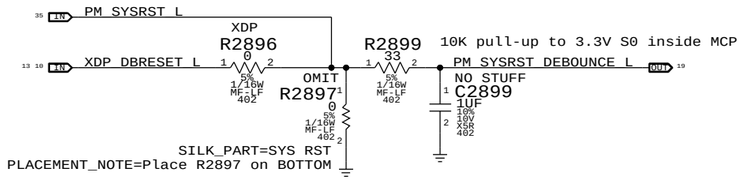




MCP S0 PWRGD & CPU_VLD



System Reset Circuit



DO NOT SYNC WTIH T27. REMOVED PCIE RESET SIGNALS +CAESAR XTAL

SYNC_MASTER=K87_MLB SYNC_DATE=02/26/2010

PAGE TITLE: SB Misc

Apple Inc.

DRAWING NUMBER: 051-8407 SIZE: D

REVISION: A.0.0

BRANCH:

PAGE: 28 OF 109

SHEET: 25 OF 76

Page Notes

Power aliases required by this page:
- =PPLVDDR_S3_MEM_A
- =PPDDRVTT_S0_MEM_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)
NOTE: J3100 is OMITted on this page.
Proper APN(s) required elsewhere.

DDR3 Plane Stitching Caps (Space evenly across plane split)

=PPLVDDR_S3_MEM_A

C2900 10UF 20% 6.3V X5R 603 1 2
C2901 10UF 20% 6.3V X5R 603 1 2
C2910 0.1UF 10% 10V CERM 402 2 1
C2911 0.1UF 10% 10V CERM 402 2 1
C2912 0.1UF 10% 10V CERM 402 2 1
C2913 0.1UF 10% 10V CERM 402 2 1
C2914 0.1UF 10% 10V CERM 402 2 1
C2915 0.1UF 10% 10V CERM 402 2 1
C2916 0.1UF 10% 10V CERM 402 2 1
C2917 0.1UF 10% 10V CERM 402 2 1
C2918 0.1UF 10% 10V CERM 402 2 1
C2919 0.1UF 10% 10V CERM 402 2 1
C2920 0.1UF 10% 10V CERM 402 2 1
C2921 0.1UF 10% 10V CERM 402 2 1
C2922 0.1UF 10% 10V CERM 402 2 1
C2923 0.1UF 10% 10V CERM 402 2 1

=PPDDRVTT_S0_MEM_A

=PPVREF_S3_MEM_VREFDQ_A

C2930 2.2UF 20% 6.3V CERM 402-LF 1 2
C2931 0.1UF 10% 10V CERM 402 1 2

=PPVREF_S3_MEM_VREFCA_A

C2936 0.1UF 10% 10V CERM 402 1 2
C2935 2.2UF 20% 6.3V CERM 402-LF 1 2

=PPSPD_S0_MEM_A

C2940 2.2UF 20% 6.3V CERM 402-LF 1 2
R2940 10K 5% 1/16W MF-LF 402 1 2
R2941 10K 5% 1/16W MF-LF 2402 1 2

SPD Addr: 0xA0(Wr)/0xA1(Rd)

DDR3-SODIMM-DUAL-M97-3 (SYMBOL 2 OF 2)

KEY: CRITICAL OMIT J2900 F-RT-THB

	MEM_A_CKE<0>	73	CKE0	CKE1	74	MEM_A_CKE<1>	
		75	VDD	VDD	76		
NCX		77	NC	A15	78	MEM_A_A<15>	
	MEM_A_BA<2>	79	BA2	A14	80	MEM_A_A<14>	
		81	VDD	VDD	82		
	MEM_A_A<12>	83	A12/BC*	A11	84	MEM_A_A<11>	
	MEM_A_A<9>	85	A9	A7	86	MEM_A_A<7>	
		87	VDD	VDD	88		
	MEM_A_A<8>	89	A8	A6	90	MEM_A_A<6>	
	MEM_A_A<5>	91	A5	A4	92	MEM_A_A<4>	
		93	VDD	VDD	94		
	MEM_A_A<3>	95	A3	A2	96	MEM_A_A<2>	
	MEM_A_A<1>	97	A1	A0	98	MEM_A_A<0>	
		99	VDD	VDD	100		
	MEM_A_CLK_P<0>	101	CK0	CK1	102	MEM_A_CLK_P<1>	
	MEM_A_CLK_N<0>	103	CK0*	CK1*	104	MEM_A_CLK_N<1>	
		105	VDD	VDD	106		
	MEM_A_A<10>	107	A10/AP	BA1	108	MEM_A_BA<1>	
	MEM_A_BA<0>	109	BA0	RAS*	110	MEM_A_RAS_L	
		111	VDD	VDD	112		
	MEM_A_WE_L	113	WE*	S0*	114	MEM_A_CS_L<0>	
	MEM_A_CAS_L	115	CAS*	ODT0	116	MEM_A_ODT<0>	
		117	VDD	VDD	118		
	MEM_A_A<13>	119	A13	ODT1	120	MEM_A_ODT<1>	
	MEM_A_CS_L<1>	121	S1*	NC	122	NC	
		123	VDD	VDD	124		
NCX		125	TEST	VREFCA	126		
		127	VSS	VSS	128		
	=MEM_A_DQ<32>	129	DQ32	DQ36	130	=MEM_A_DQ<36>	
	=MEM_A_DQ<33>	131	DQ33	DQ37	132	=MEM_A_DQ<37>	
		133	VSS	VSS	134		
	=MEM_A_DQS_N<4>	135	DQS4*	DM4	136	=MEM_A_DM<4>	
	=MEM_A_DQS_P<4>	137	DQS4	VSS	138		
		139	VSS	DQ38	140	=MEM_A_DQ<38>	
	=MEM_A_DQ<34>	141	DQ34	DQ39	142	=MEM_A_DQ<39>	
	=MEM_A_DQ<35>	143	DQ35	VSS	144		
		145	VSS	DQ44	146	=MEM_A_DQ<44>	
	=MEM_A_DQ<40>	147	DQ40	DQ45	148	=MEM_A_DQ<45>	
	=MEM_A_DQ<41>	149	DQ41	VSS	150		
		151	VSS	DQS5*	152	=MEM_A_DQS_N<5>	
	=MEM_A_DM<5>	153	DM5	DQS5	154	=MEM_A_DQS_P<5>	
		155	VSS	VSS	156		
	=MEM_A_DQ<42>	157	DQ42	DQ46	158	=MEM_A_DQ<46>	
	=MEM_A_DQ<43>	159	DQ43	DQ47	160	=MEM_A_DQ<47>	
		161	VSS	VSS	162		
	=MEM_A_DQ<48>	163	DQ48	DQ52	164	=MEM_A_DQ<52>	
	=MEM_A_DQ<49>	165	DQ49	DQ53	166	=MEM_A_DQ<53>	
		167	VSS	VSS	168		
	=MEM_A_DQS_N<6>	169	DQS6*	DM6	170	=MEM_A_DM<6>	
	=MEM_A_DQS_P<6>	171	DQS6	VSS	172		
		173	VSS	DQ54	174	=MEM_A_DQ<54>	
	=MEM_A_DQ<50>	175	DQ50	DQ55	176	=MEM_A_DQ<55>	
	=MEM_A_DQ<51>	177	DQ51	VSS	178		
		179	VSS	DQ60	180	=MEM_A_DQ<60>	
	=MEM_A_DQ<56>	181	DQ56	DQ61	182	=MEM_A_DQ<61>	
	=MEM_A_DQ<57>	183	DQ57	VSS	184		
		185	VSS	DQS7*	186	=MEM_A_DQS_N<7>	
	=MEM_A_DM<7>	187	DM7	DQS7	188	=MEM_A_DQS_P<7>	
		189	VSS	VSS	190		
	=MEM_A_DQ<58>	191	DQ58	DQ62	192	=MEM_A_DQ<62>	
	=MEM_A_DQ<59>	193	DQ59	DQ63	194	=MEM_A_DQ<63>	
		195	VSS	VSS	196		
	MEM_A_SA<0>	197	SA0	EVENT*	198	MEM_EVENT_L	OUT
		199	VDDSPD	SDA	200	=I2C_SODIMMA_SDA	BI
	MEM_A_SA<1>	201	SA1	SCL	202	=I2C_SODIMMA_SCL	IN
		203	VTT	VTT	204		

Foxconn: 516-0201
Molex: 516-0213

"Factory" (top) slot

KEY: CRITICAL OMIT J2900 F-RT-THB

DDR3-SODIMM-DUAL-M97-3 (SYMBOL 1 OF 2)

		1	VREFDQ	VSS	2		
	=MEM_A_DQ<0>	3	VSS	DQ4	4	=MEM_A_DQ<4>	
	=MEM_A_DQ<1>	5	DQ0	DQ5	6	=MEM_A_DQ<5>	
		7	DQ1	VSS	8		
	=MEM_A_DM<0>	9	VSS	DQS0*	10	=MEM_A_DQS_N<0>	
		11	DM0	DQS0	12	=MEM_A_DQS_P<0>	
	=MEM_A_DQ<2>	13	VSS	VSS	14		
	=MEM_A_DQ<3>	15	DQ2	DQ6	16	=MEM_A_DQ<6>	
		17	DQ3	DQ7	18	=MEM_A_DQ<7>	
	=MEM_A_DQ<8>	19	VSS	VSS	20		
	=MEM_A_DQ<9>	21	DQ8	DQ12	22	=MEM_A_DQ<12>	
		23	DQ9	DQ13	24	=MEM_A_DQ<13>	
	=MEM_A_DQS_N<1>	25	VSS	VSS	26		
	=MEM_A_DQS_P<1>	27	DQS1*	DM1	28	=MEM_A_DM<1>	
		29	DQS1	RESET*	30	MEM_RESET_L	
	=MEM_A_DQ<10>	31	VSS	VSS	32		
	=MEM_A_DQ<11>	33	DQ10	DQ14	34	=MEM_A_DQ<14>	
		35	DQ11	DQ15	36	=MEM_A_DQ<15>	
	=MEM_A_DQ<16>	37	VSS	VSS	38		
	=MEM_A_DQ<17>	39	DQ16	DQ20	40	=MEM_A_DQ<20>	
		41	DQ17	DQ21	42	=MEM_A_DQ<21>	
	=MEM_A_DQS_N<2>	43	VSS	VSS	44		
	=MEM_A_DQS_P<2>	45	DQS2*	DM2	46	=MEM_A_DM<2>	
		47	DQS2	VSS	48		
	=MEM_A_DQ<18>	49	VSS	DQ22	50	=MEM_A_DQ<22>	
	=MEM_A_DQ<19>	51	DQ18	DQ23	52	=MEM_A_DQ<23>	
		53	DQ19	VSS	54		
	=MEM_A_DQ<24>	55	VSS	DQ28	56	=MEM_A_DQ<28>	
	=MEM_A_DQ<25>	57	DQ24	DQ29	58	=MEM_A_DQ<29>	
		59	DQ25	VSS	60		
	=MEM_A_DM<3>	61	VSS	DQS3*	62	=MEM_A_DQS_N<3>	
		63	DM3	DQS3	64	=MEM_A_DQS_P<3>	
	=MEM_A_DQ<26>	65	VSS	VSS	66		
	=MEM_A_DQ<27>	67	DQ26	DQ30	68	=MEM_A_DQ<30>	
		69	DQ27	DQ31	70	=MEM_A_DQ<31>	
		71	VSS	VSS	72		

Foxconn: 516-0201
Molex: 516-0213

SYNC_MASTER=K87_MLB SYNC_DATE=02/26/2010

PAGE TITLE: DDR3 SO-DIMM Connector A

Apple Inc.

DRAWING NUMBER: 051-8407 SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 29 OF 109
SHEET: 26 OF 76

Page Notes

Power aliases required by this page:
- =PPLVDDR_S3_MEM_B
- =PPDDRVTT_S0_MEM_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)
NOTE: J3100 is OMITted on this page.
Proper APN(s) required elsewhere.

DDR3 Plane Stitching Caps (Space evenly across plane split)

=PPLVDDR_S3_MEM_B

C3100 10UF 6.3V 20% X5R 603
C3101 10UF 6.3V 20% X5R 603
C3110 0.1UF 10V 10% CERM 402
C3111 0.1UF 10V 10% CERM 402
C3112 0.1UF 10V 10% CERM 402
C3113 0.1UF 10V 10% CERM 402
C3114 0.1UF 10V 10% CERM 402
C3115 0.1UF 10V 10% CERM 402
C3116 0.1UF 10V 10% CERM 402
C3117 0.1UF 10V 10% CERM 402
C3118 0.1UF 10V 10% CERM 402
C3119 0.1UF 10V 10% CERM 402
C3120 0.1UF 10V 10% CERM 402
C3121 0.1UF 10V 10% CERM 402
C3122 0.1UF 10V 10% CERM 402
C3123 0.1UF 10V 10% CERM 402

=PPDDRVTT_S0_MEM_B

C3130 2.2UF 6.3V 20% CERM 402-LF
C3131 0.1UF 10V 10% CERM 402
C3135 2.2UF 6.3V 20% CERM 402-LF
C3136 0.1UF 10V 10% CERM 402

PPVREF_S3_MEM_VREFDQ_B
PPVREF_S3_MEM_VREFCA_B

DDR3-SODIMM (2 OF 2) — J3100 F-RT-BGA3

KEY: CRITICAL OMIT J3100 F-RT-BGA3

	MEM_B_CKE<0>	73	CKE0	CKE1	74	MEM_B_CKE<1>	
		75	VDD	VDD	76		
NC		77	NC	A15	78	MEM_B_A<15>	
	MEM_B_BA<2>	79	BA2	A14	80	MEM_B_A<14>	
		81	VDD	VDD	82		
	MEM_B_A<12>	83	A12/BC*	A11	84	MEM_B_A<11>	
	MEM_B_A<9>	85	A9	A7	86	MEM_B_A<7>	
		87	VDD	VDD	88		
	MEM_B_A<8>	89	A8	A6	90	MEM_B_A<6>	
	MEM_B_A<5>	91	A5	A4	92	MEM_B_A<4>	
		93	VDD	VDD	94		
	MEM_B_A<3>	95	A3	A2	96	MEM_B_A<2>	
	MEM_B_A<1>	97	A1	A0	98	MEM_B_A<0>	
		99	VDD	VDD	100		
	MEM_B_CLK_P<0>	101	CK0	CK1	102	MEM_B_CLK_P<1>	
	MEM_B_CLK_N<0>	103	CK0*	CK1*	104	MEM_B_CLK_N<1>	
		105	VDD	VDD	106		
	MEM_B_A<10>	107	A10/AP	BA1	108	MEM_B_BA<1>	
	MEM_B_BA<0>	109	BA0	RAS*	110	MEM_B_RAS_L	
		111	VDD	VDD	112		
	MEM_B_WE_L	113	WE*	S0*	114	MEM_B_CS_L<0>	
	MEM_B_CAS_L	115	CAS*	ODT0	116	MEM_B_ODT<0>	
		117	VDD	VDD	118		
	MEM_B_A<13>	119	A13	ODT1	120	MEM_B_ODT<1>	
	MEM_B_CS_L<1>	121	S1*	NC	122	NC	
		123	VDD	VDD	124		
NC		125	TEST	VREFCA	126	PPVREF_S3_MEM_VREFCA_B	
		127	VSS	VSS	128		
	=MEM_B_DQ<32>	129	DQ32	DQ36	130	=MEM_B_DQ<36>	
	=MEM_B_DQ<33>	131	DQ33	DQ37	132	=MEM_B_DQ<37>	
		133	VSS	VSS	134		
	=MEM_B_DQS_N<4>	135	DQS4*	DM4	136	=MEM_B_DM<4>	
	=MEM_B_DQS_P<4>	137	DQS4	VSS	138		
		139	VSS	DQ38	140	=MEM_B_DQ<38>	
	=MEM_B_DQ<34>	141	DQ34	DQ39	142	=MEM_B_DQ<39>	
	=MEM_B_DQ<35>	143	DQ35	VSS	144		
		145	VSS	DQ44	146	=MEM_B_DQ<44>	
	=MEM_B_DQ<40>	147	DQ40	DQ45	148	=MEM_B_DQ<45>	
	=MEM_B_DQ<41>	149	DQ41	VSS	150		
		151	VSS	DQS5*	152	=MEM_B_DQS_N<5>	
	=MEM_B_DM<5>	153	DM5	DQS5	154	=MEM_B_DQS_P<5>	
		155	VSS	VSS	156		
	=MEM_B_DQ<42>	157	DQ42	DQ46	158	=MEM_B_DQ<46>	
	=MEM_B_DQ<43>	159	DQ43	DQ47	160	=MEM_B_DQ<47>	
		161	VSS	VSS	162		
	=MEM_B_DQ<48>	163	DQ48	DQ52	164	=MEM_B_DQ<52>	
	=MEM_B_DQ<49>	165	DQ49	DQ53	166	=MEM_B_DQ<53>	
		167	VSS	VSS	168		
	=MEM_B_DQS_N<6>	169	DQS6*	DM6	170	=MEM_B_DM<6>	
	=MEM_B_DQS_P<6>	171	DQS6	VSS	172		
		173	VSS	DQ54	174	=MEM_B_DQ<54>	
	=MEM_B_DQ<50>	175	DQ50	DQ55	176	=MEM_B_DQ<55>	
	=MEM_B_DQ<51>	177	DQ51	VSS	178		
		179	VSS	DQ60	180	=MEM_B_DQ<60>	
	=MEM_B_DQ<56>	181	DQ56	DQ61	182	=MEM_B_DQ<61>	
	=MEM_B_DQ<57>	183	DQ57	VSS	184		
		185	VSS	DQS7*	186	=MEM_B_DQS_N<7>	
	=MEM_B_DM<7>	187	DM7	DQS7	188	=MEM_B_DQS_P<7>	
		189	VSS	VSS	190		
	=MEM_B_DQ<58>	191	DQ58	DQ62	192	=MEM_B_DQ<62>	
	=MEM_B_DQ<59>	193	DQ59	DQ63	194	=MEM_B_DQ<63>	
		195	VSS	VSS	196		
	MEM_B_SA<0>	197	SA0	EVENT*	198	MEM_EVENT_L	
		199	VDDSPD	SDA	200	=I2C_SODIMMB_SDA	
	MEM_B_SA<1>	201	SA1	SCL	202	=I2C_SODIMMB_SCL	
		203	VTT	VTT	204		
		205	MTG PIN	MTG PIN	206		
		207	MTG PIN	MTG PIN	208		
		209	MTG PIN	MTG PIN	210		
		211	MTG PIN	MTG PIN	212		

MTG PINS

=PPSPD_S0_MEM_B

R3140 10K 5% 1/16W MF-LF 402
R3141 10K 5% 1/16W MF-LF 402
C3140 2.2UF 6.3V 20% CERM 402-LF

SPD Addr: 0xA2(Wr)/0xA3(Rd)

Foxconn: 516s0706
Molex: 516s0790

"Expansion" (bottom) slot

DDR3-SODIMM (1 OF 2) — CRITICAL OMIT J3100 F-RT-BGA3

		1	VREFDQ	VSS	2		
	=MEM_B_DQ<0>	3	VSS	DQ4	4	=MEM_B_DQ<4>	
	=MEM_B_DQ<1>	5	DQ0	DQ5	6	=MEM_B_DQ<5>	
		7	DQ1	VSS	8		
	=MEM_B_DM<0>	9	VSS	DQS0*	10	=MEM_B_DQS_N<0>	
		11	DM0	DQS0	12	=MEM_B_DQS_P<0>	
	=MEM_B_DQ<2>	13	VSS	VSS	14		
	=MEM_B_DQ<3>	15	DQ2	DQ6	16	=MEM_B_DQ<6>	
		17	DQ3	DQ7	18	=MEM_B_DQ<7>	
	=MEM_B_DQ<8>	19	VSS	VSS	20		
	=MEM_B_DQ<9>	21	DQ8	DQ12	22	=MEM_B_DQ<12>	
		23	DQ9	DQ13	24	=MEM_B_DQ<13>	
	=MEM_B_DQS_N<1>	25	VSS	VSS	26		
	=MEM_B_DQS_P<1>	27	DQS1*	DM1	28	=MEM_B_DM<1>	
		29	DQS1	RESET*	30	MEM_RESET_L	
	=MEM_B_DQ<10>	31	VSS	VSS	32		
	=MEM_B_DQ<11>	33	DQ10	DQ14	34	=MEM_B_DQ<14>	
		35	DQ11	DQ15	36	=MEM_B_DQ<15>	
	=MEM_B_DQ<16>	37	VSS	VSS	38		
	=MEM_B_DQ<17>	39	DQ16	DQ20	40	=MEM_B_DQ<20>	
		41	DQ17	DQ21	42	=MEM_B_DQ<21>	
	=MEM_B_DQS_N<2>	43	VSS	VSS	44		
	=MEM_B_DQS_P<2>	45	DQS2*	DM2	46	=MEM_B_DM<2>	
		47	DQS2	VSS	48		
	=MEM_B_DQ<18>	49	VSS	DQ22	50	=MEM_B_DQ<22>	
	=MEM_B_DQ<19>	51	DQ18	DQ23	52	=MEM_B_DQ<23>	
		53	DQ19	VSS	54		
	=MEM_B_DQ<24>	55	VSS	DQ28	56	=MEM_B_DQ<28>	
	=MEM_B_DQ<25>	57	DQ24	DQ29	58	=MEM_B_DQ<29>	
		59	DQ25	VSS	60		
	=MEM_B_DM<3>	61	VSS	DQS3*	62	=MEM_B_DQS_N<3>	
		63	DM3	DQS3	64	=MEM_B_DQS_P<3>	
	=MEM_B_DQ<26>	65	VSS	VSS	66		
	=MEM_B_DQ<27>	67	DQ26	DQ30	68	=MEM_B_DQ<30>	
		69	DQ27	DQ31	70	=MEM_B_DQ<31>	
		71	VSS	VSS	72		

KEY

Foxconn: 516s0706
Molex: 516s0790

SYNC_MASTER=K87_MLB SYNC_DATE=02/26/2010

PAGE TITLE: DDR3 SO-DIMM Connector B

Apple Inc.

DRAWING NUMBER: 051-8407 SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 31 OF 109
SHEET: 27 OF 76

Host Partition A 0 -> SO-DIMM A 0

MEM_A_DQS_P<0>			=MEM_A_DQS_P<0>	B1	26
MEM_A_DQS_N<0>	MAKE_BASE=TRUE	=	=MEM_A_DQS_N<0>	B1	26
MEM_A_DM<0>	MAKE_BASE=TRUE	=	=MEM_A_DM<0>	OUT	26
MEM_A_DQ<0>			=MEM_A_DQ<0>	B1	26
MEM_A_DQ<1>	MAKE_BASE=TRUE	=	=MEM_A_DQ<1>	B1	26
MEM_A_DQ<2>	MAKE_BASE=TRUE	=	=MEM_A_DQ<3>	B1	26
MEM_A_DQ<3>	MAKE_BASE=TRUE	=	=MEM_A_DQ<2>	B1	26
MEM_A_DQ<4>	MAKE_BASE=TRUE	=	=MEM_A_DQ<4>	B1	26
MEM_A_DQ<5>	MAKE_BASE=TRUE	=	=MEM_A_DQ<5>	B1	26
MEM_A_DQ<6>	MAKE_BASE=TRUE	=	=MEM_A_DQ<6>	B1	26
MEM_A_DQ<7>	MAKE_BASE=TRUE	=	=MEM_A_DQ<7>	B1	26

HOST PARTITION A 1 -> SO-DIMM A 1

MEM_A_DQS_P<1>			=MEM_A_DQS_P<1>	B1	26
MEM_A_DQS_N<1>	MAKE_BASE=TRUE	=	=MEM_A_DQS_N<1>	B1	26
MEM_A_DM<1>	MAKE_BASE=TRUE	=	=MEM_A_DM<1>	OUT	26
MEM_A_DQ<8>			=MEM_A_DQ<12>	B1	26
MEM_A_DQ<9>	MAKE_BASE=TRUE	=	=MEM_A_DQ<8>	B1	26
MEM_A_DQ<10>	MAKE_BASE=TRUE	=	=MEM_A_DQ<15>	B1	26
MEM_A_DQ<11>	MAKE_BASE=TRUE	=	=MEM_A_DQ<10>	B1	26
MEM_A_DQ<12>	MAKE_BASE=TRUE	=	=MEM_A_DQ<13>	B1	26
MEM_A_DQ<13>	MAKE_BASE=TRUE	=	=MEM_A_DQ<9>	B1	26
MEM_A_DQ<14>	MAKE_BASE=TRUE	=	=MEM_A_DQ<11>	B1	26
MEM_A_DQ<15>	MAKE_BASE=TRUE	=	=MEM_A_DQ<14>	B1	26

HOST PARTITION A 2 -> SO-DIMM A 3

MEM_A_DQS_P<2>			=MEM_A_DQS_P<3>	B1	26
MEM_A_DQS_N<2>	MAKE_BASE=TRUE	=	=MEM_A_DQS_N<3>	B1	26
MEM_A_DM<2>	MAKE_BASE=TRUE	=	=MEM_A_DM<3>	OUT	26
MEM_A_DQ<16>			=MEM_A_DQ<24>	B1	26
MEM_A_DQ<17>	MAKE_BASE=TRUE	=	=MEM_A_DQ<30>	B1	26
MEM_A_DQ<18>	MAKE_BASE=TRUE	=	=MEM_A_DQ<26>	B1	26
MEM_A_DQ<19>	MAKE_BASE=TRUE	=	=MEM_A_DQ<27>	B1	26
MEM_A_DQ<20>	MAKE_BASE=TRUE	=	=MEM_A_DQ<29>	B1	26
MEM_A_DQ<21>	MAKE_BASE=TRUE	=	=MEM_A_DQ<28>	B1	26
MEM_A_DQ<22>	MAKE_BASE=TRUE	=	=MEM_A_DQ<25>	B1	26
MEM_A_DQ<23>	MAKE_BASE=TRUE	=	=MEM_A_DQ<31>	B1	26

HOST PARTITION A 3 -> SO-DIMM A 2

MEM_A_DQS_P<3>			=MEM_A_DQS_P<2>	B1	26
MEM_A_DQS_N<3>	MAKE_BASE=TRUE	=	=MEM_A_DQS_N<2>	B1	26
MEM_A_DM<3>	MAKE_BASE=TRUE	=	=MEM_A_DM<2>	OUT	26
MEM_A_DQ<24>			=MEM_A_DQ<17>	B1	26
MEM_A_DQ<25>	MAKE_BASE=TRUE	=	=MEM_A_DQ<20>	B1	26
MEM_A_DQ<26>	MAKE_BASE=TRUE	=	=MEM_A_DQ<23>	B1	26
MEM_A_DQ<27>	MAKE_BASE=TRUE	=	=MEM_A_DQ<18>	B1	26
MEM_A_DQ<28>	MAKE_BASE=TRUE	=	=MEM_A_DQ<22>	B1	26
MEM_A_DQ<29>	MAKE_BASE=TRUE	=	=MEM_A_DQ<21>	B1	26
MEM_A_DQ<30>	MAKE_BASE=TRUE	=	=MEM_A_DQ<16>	B1	26
MEM_A_DQ<31>	MAKE_BASE=TRUE	=	=MEM_A_DQ<19>	B1	26

Host Partition A 4 -> SO-DIMM A 4

MEM_A_DQS_P<4>			=MEM_A_DQS_P<4>	B1	26
MEM_A_DQS_N<4>	MAKE_BASE=TRUE	=	=MEM_A_DQS_N<4>	B1	26
MEM_A_DM<4>	MAKE_BASE=TRUE	=	=MEM_A_DM<4>	OUT	26
MEM_A_DQ<32>			=MEM_A_DQ<33>	B1	26
MEM_A_DQ<33>	MAKE_BASE=TRUE	=	=MEM_A_DQ<32>	B1	26
MEM_A_DQ<34>	MAKE_BASE=TRUE	=	=MEM_A_DQ<34>	B1	26
MEM_A_DQ<35>	MAKE_BASE=TRUE	=	=MEM_A_DQ<35>	B1	26
MEM_A_DQ<36>	MAKE_BASE=TRUE	=	=MEM_A_DQ<36>	B1	26
MEM_A_DQ<37>	MAKE_BASE=TRUE	=	=MEM_A_DQ<37>	B1	26
MEM_A_DQ<38>	MAKE_BASE=TRUE	=	=MEM_A_DQ<38>	B1	26
MEM_A_DQ<39>	MAKE_BASE=TRUE	=	=MEM_A_DQ<39>	B1	26

Host Partition A 5 -> SO-DIMM A 5

MEM_A_DQS_P<5>			=MEM_A_DQS_P<5>	B1	26
MEM_A_DQS_N<5>	MAKE_BASE=TRUE	=	=MEM_A_DQS_N<5>	B1	26
MEM_A_DM<5>	MAKE_BASE=TRUE	=	=MEM_A_DM<5>	OUT	26
MEM_A_DQ<40>			=MEM_A_DQ<45>	B1	26
MEM_A_DQ<41>	MAKE_BASE=TRUE	=	=MEM_A_DQ<41>	B1	26
MEM_A_DQ<42>	MAKE_BASE=TRUE	=	=MEM_A_DQ<43>	B1	26
MEM_A_DQ<43>	MAKE_BASE=TRUE	=	=MEM_A_DQ<47>	B1	26
MEM_A_DQ<44>	MAKE_BASE=TRUE	=	=MEM_A_DQ<40>	B1	26
MEM_A_DQ<45>	MAKE_BASE=TRUE	=	=MEM_A_DQ<42>	B1	26
MEM_A_DQ<46>	MAKE_BASE=TRUE	=	=MEM_A_DQ<46>	B1	26
MEM_A_DQ<47>	MAKE_BASE=TRUE	=	=MEM_A_DQ<44>	B1	26

Host Partition A 6 -> SO-DIMM A 6

MEM_A_DQS_P<6>			=MEM_A_DQS_P<6>	B1	26
MEM_A_DQS_N<6>	MAKE_BASE=TRUE	=	=MEM_A_DQS_N<6>	B1	26
MEM_A_DM<6>	MAKE_BASE=TRUE	=	=MEM_A_DM<6>	OUT	26
MEM_A_DQ<48>			=MEM_A_DQ<52>	B1	26
MEM_A_DQ<49>	MAKE_BASE=TRUE	=	=MEM_A_DQ<55>	B1	26
MEM_A_DQ<50>	MAKE_BASE=TRUE	=	=MEM_A_DQ<54>	B1	26
MEM_A_DQ<51>	MAKE_BASE=TRUE	=	=MEM_A_DQ<49>	B1	26
MEM_A_DQ<52>	MAKE_BASE=TRUE	=	=MEM_A_DQ<48>	B1	26
MEM_A_DQ<53>	MAKE_BASE=TRUE	=	=MEM_A_DQ<53>	B1	26
MEM_A_DQ<54>	MAKE_BASE=TRUE	=	=MEM_A_DQ<51>	B1	26
MEM_A_DQ<55>	MAKE_BASE=TRUE	=	=MEM_A_DQ<50>	B1	26

Host Partition A 7 -> SO-DIMM A 7

MEM_A_DQS_P<7>			=MEM_A_DQS_P<7>	B1	26
MEM_A_DQS_N<7>	MAKE_BASE=TRUE	=	=MEM_A_DQS_N<7>	B1	26
MEM_A_DM<7>	MAKE_BASE=TRUE	=	=MEM_A_DM<7>	OUT	26
MEM_A_DQ<56>			=MEM_A_DQ<61>	B1	26
MEM_A_DQ<57>	MAKE_BASE=TRUE	=	=MEM_A_DQ<60>	B1	26
MEM_A_DQ<58>	MAKE_BASE=TRUE	=	=MEM_A_DQ<58>	B1	26
MEM_A_DQ<59>	MAKE_BASE=TRUE	=	=MEM_A_DQ<59>	B1	26
MEM_A_DQ<60>	MAKE_BASE=TRUE	=	=MEM_A_DQ<57>	B1	26
MEM_A_DQ<61>	MAKE_BASE=TRUE	=	=MEM_A_DQ<56>	B1	26
MEM_A_DQ<62>	MAKE_BASE=TRUE	=	=MEM_A_DQ<62>	B1	26
MEM_A_DQ<63>	MAKE_BASE=TRUE	=	=MEM_A_DQ<63>	B1	26

Host Partition B 0 -> SO-DIMM B 0

MEM_B_DQS_P<0>			=MEM_B_DQS_P<0>	B1	27
MEM_B_DQS_N<0>	MAKE_BASE=TRUE	=	=MEM_B_DQS_N<0>	B1	27
MEM_B_DM<0>	MAKE_BASE=TRUE	=	=MEM_B_DM<0>	OUT	27
MEM_B_DQ<0>			=MEM_B_DQ<0>	B1	27
MEM_B_DQ<1>	MAKE_BASE=TRUE	=	=MEM_B_DQ<1>	B1	27
MEM_B_DQ<2>	MAKE_BASE=TRUE	=	=MEM_B_DQ<2>	B1	27
MEM_B_DQ<3>	MAKE_BASE=TRUE	=	=MEM_B_DQ<3>	B1	27
MEM_B_DQ<4>	MAKE_BASE=TRUE	=	=MEM_B_DQ<4>	B1	27
MEM_B_DQ<5>	MAKE_BASE=TRUE	=	=MEM_B_DQ<5>	B1	27
MEM_B_DQ<6>	MAKE_BASE=TRUE	=	=MEM_B_DQ<6>	B1	27
MEM_B_DQ<7>	MAKE_BASE=TRUE	=	=MEM_B_DQ<7>	B1	27

Host Partition B 1 -> SO-DIMM B 2

MEM_B_DQS_P<1>			=MEM_B_DQS_P<2>	B1	27
MEM_B_DQS_N<1>	MAKE_BASE=TRUE	=	=MEM_B_DQS_N<2>	B1	27
MEM_B_DM<1>	MAKE_BASE=TRUE	=	=MEM_B_DM<2>	OUT	27
MEM_B_DQ<8>			=MEM_B_DQ<17>	B1	27
MEM_B_DQ<9>	MAKE_BASE=TRUE	=	=MEM_B_DQ<16>	B1	27
MEM_B_DQ<10>	MAKE_BASE=TRUE	=	=MEM_B_DQ<19>	B1	27
MEM_B_DQ<11>	MAKE_BASE=TRUE	=	=MEM_B_DQ<23>	B1	27
MEM_B_DQ<12>	MAKE_BASE=TRUE	=	=MEM_B_DQ<21>	B1	27
MEM_B_DQ<13>	MAKE_BASE=TRUE	=	=MEM_B_DQ<20>	B1	27
MEM_B_DQ<14>	MAKE_BASE=TRUE	=	=MEM_B_DQ<22>	B1	27
MEM_B_DQ<15>	MAKE_BASE=TRUE	=	=MEM_B_DQ<18>	B1	27

Host Partition B 2 -> SO-DIMM B 3

MEM_B_DQS_P<2>			=MEM_B_DQS_P<3>	B1	27
MEM_B_DQS_N<2>	MAKE_BASE=TRUE	=	=MEM_B_DQS_N<3>	B1	27
MEM_B_DM<2>	MAKE_BASE=TRUE	=	=MEM_B_DM<3>	OUT	27
MEM_B_DQ<16>			=MEM_B_DQ<29>	B1	27
MEM_B_DQ<17>	MAKE_BASE=TRUE	=	=MEM_B_DQ<25>	B1	27
MEM_B_DQ<18>	MAKE_BASE=TRUE	=	=MEM_B_DQ<26>	B1	27
MEM_B_DQ<19>	MAKE_BASE=TRUE	=	=MEM_B_DQ<30>	B1	27
MEM_B_DQ<20>	MAKE_BASE=TRUE	=	=MEM_B_DQ<28>	B1	27
MEM_B_DQ<21>	MAKE_BASE=TRUE	=	=MEM_B_DQ<24>	B1	27
MEM_B_DQ<22>	MAKE_BASE=TRUE	=	=MEM_B_DQ<27>	B1	27
MEM_B_DQ<23>	MAKE_BASE=TRUE	=	=MEM_B_DQ<31>	B1	27

Host Partition B 3 -> SO-DIMM B 1

MEM_B_DQS_P<3>			=MEM_B_DQS_P<1>	B1	27
MEM_B_DQS_N<3>	MAKE_BASE=TRUE	=	=MEM_B_DQS_N<1>	B1	27
MEM_B_DM<3>	MAKE_BASE=TRUE	=	=MEM_B_DM<1>	OUT	27
MEM_B_DQ<24>			=MEM_B_DQ<9>	B1	27
MEM_B_DQ<25>	MAKE_BASE=TRUE	=	=MEM_B_DQ<13>	B1	27
MEM_B_DQ<26>	MAKE_BASE=TRUE	=	=MEM_B_DQ<14>	B1	27
MEM_B_DQ<27>	MAKE_BASE=TRUE	=	=MEM_B_DQ<15>	B1	27
MEM_B_DQ<28>	MAKE_BASE=TRUE	=	=MEM_B_DQ<8>	B1	27
MEM_B_DQ<29>	MAKE_BASE=TRUE	=	=MEM_B_DQ<12>	B1	27
MEM_B_DQ<30>	MAKE_BASE=TRUE	=	=MEM_B_DQ<11>	B1	27
MEM_B_DQ<31>	MAKE_BASE=TRUE	=	=MEM_B_DQ<10>	B1	27

Host Partition B 4 -> SO-DIMM B 4

MEM_B_DQS_P<4>			=MEM_B_DQS_P<4>	B1	27
MEM_B_DQS_N<4>	MAKE_BASE=TRUE	=	=MEM_B_DQS_N<4>	B1	27
MEM_B_DM<4>	MAKE_BASE=TRUE	=	=MEM_B_DM<4>	OUT	27
MEM_B_DQ<32>			=MEM_B_DQ<32>	B1	27
MEM_B_DQ<33>	MAKE_BASE=TRUE	=	=MEM_B_DQ<36>	B1	27
MEM_B_DQ<34>	MAKE_BASE=TRUE	=	=MEM_B_DQ<34>	B1	27
MEM_B_DQ<35>	MAKE_BASE=TRUE	=	=MEM_B_DQ<35>	B1	27
MEM_B_DQ<36>	MAKE_BASE=TRUE	=	=MEM_B_DQ<37>	B1	27
MEM_B_DQ<37>	MAKE_BASE=TRUE	=	=MEM_B_DQ<33>	B1	27
MEM_B_DQ<38>	MAKE_BASE=TRUE	=	=MEM_B_DQ<38>	B1	27
MEM_B_DQ<39>	MAKE_BASE=TRUE	=	=MEM_B_DQ<39>	B1	27

Host Partition B 5 -> SO-DIMM B 5

MEM_B_DQS_P<5>			=MEM_B_DQS_P<5>	B1	27
MEM_B_DQS_N<5>	MAKE_BASE=TRUE	=	=MEM_B_DQS_N<5>	B1	27
MEM_B_DM<5>	MAKE_BASE=TRUE	=	=MEM_B_DM<5>	OUT	27
MEM_B_DQ<40>			=MEM_B_DQ<41>	B1	27
MEM_B_DQ<41>	MAKE_BASE=TRUE	=	=MEM_B_DQ<40>	B1	27
MEM_B_DQ<42>	MAKE_BASE=TRUE	=	=MEM_B_DQ<43>	B1	27
MEM_B_DQ<43>	MAKE_BASE=TRUE	=	=MEM_B_DQ<42>	B1	27
MEM_B_DQ<44>	MAKE_BASE=TRUE	=	=MEM_B_DQ<44>	B1	27
MEM_B_DQ<45>	MAKE_BASE=TRUE	=	=MEM_B_DQ<45>	B1	27
MEM_B_DQ<46>	MAKE_BASE=TRUE	=	=MEM_B_DQ<47>	B1	27
MEM_B_DQ<47>	MAKE_BASE=TRUE	=	=MEM_B_DQ<46>	B1	27

Host Partition B 6 -> SO-DIMM B 6

MEM_B_DQS_P<6>			=MEM_B_DQS_P<6>	B1	27
MEM_B_DQS_N<6>	MAKE_BASE=TRUE	=	=MEM_B_DQS_N<6>	B1	27
MEM_B_DM<6>	MAKE_BASE=TRUE	=	=MEM_B_DM<6>	OUT	27
MEM_B_DQ<48>			=MEM_B_DQ<52>	B1	27
MEM_B_DQ<49>	MAKE_BASE=TRUE	=	=MEM_B_DQ<49>	B1	27
MEM_B_DQ<50>	MAKE_BASE=TRUE	=	=MEM_B_DQ<55>	B1	27
MEM_B_DQ<51>	MAKE_BASE=TRUE	=	=MEM_B_DQ<51>	B1	27
MEM_B_DQ<52>	MAKE_BASE=TRUE	=	=MEM_B_DQ<50>	B1	27
MEM_B_DQ<53>	MAKE_BASE=TRUE	=	=MEM_B_DQ<54>	B1	27
MEM_B_DQ<54>	MAKE_BASE=TRUE	=	=MEM_B_DQ<53>	B1	27
MEM_B_DQ<55>	MAKE_BASE=TRUE	=	=MEM_B_DQ<48>	B1	27

Host Partition B 7 -> SO-DIMM B 7

MEM_B_DQS_P<7>			=MEM_B_DQS_P<7>	B1	27
MEM_B_DQS_N<7>	MAKE_BASE=TRUE	=	=MEM_B_DQS_N<7>	B1	27
MEM_B_DM<7>	MAKE_BASE=TRUE	=	=MEM_B_DM<7>	OUT	27
MEM_B_DQ<56>			=MEM_B_DQ<56>	B1	27
MEM_B_DQ<57>	MAKE_BASE=TRUE	=	=MEM_B_DQ<57>	B1	27
MEM_B_DQ<58>	MAKE_BASE=TRUE	=	=MEM_B_DQ<62>	B1	27
MEM_B_DQ<59>	MAKE_BASE=TRUE	=	=MEM_B_DQ<59>	B1	27
MEM_B_DQ<60>	MAKE_BASE=TRUE	=	=MEM_B_DQ<60>	B1	27
MEM_B_DQ<61>	MAKE_BASE=TRUE	=	=MEM_B_DQ<61>	B1	27
MEM_B_DQ<62>	MAKE_BASE=TRUE	=	=MEM_B_DQ<63>	B1	27
MEM_B_DQ<63>	MAKE_BASE=TRUE	=	=MEM_B_DQ<58>	B1	27

SYNC_MASTER=K87_MLB SYNC_DATE=02/26/2010

PAGE TITLE

SO-DIMM Pinswaps

Apple Inc.

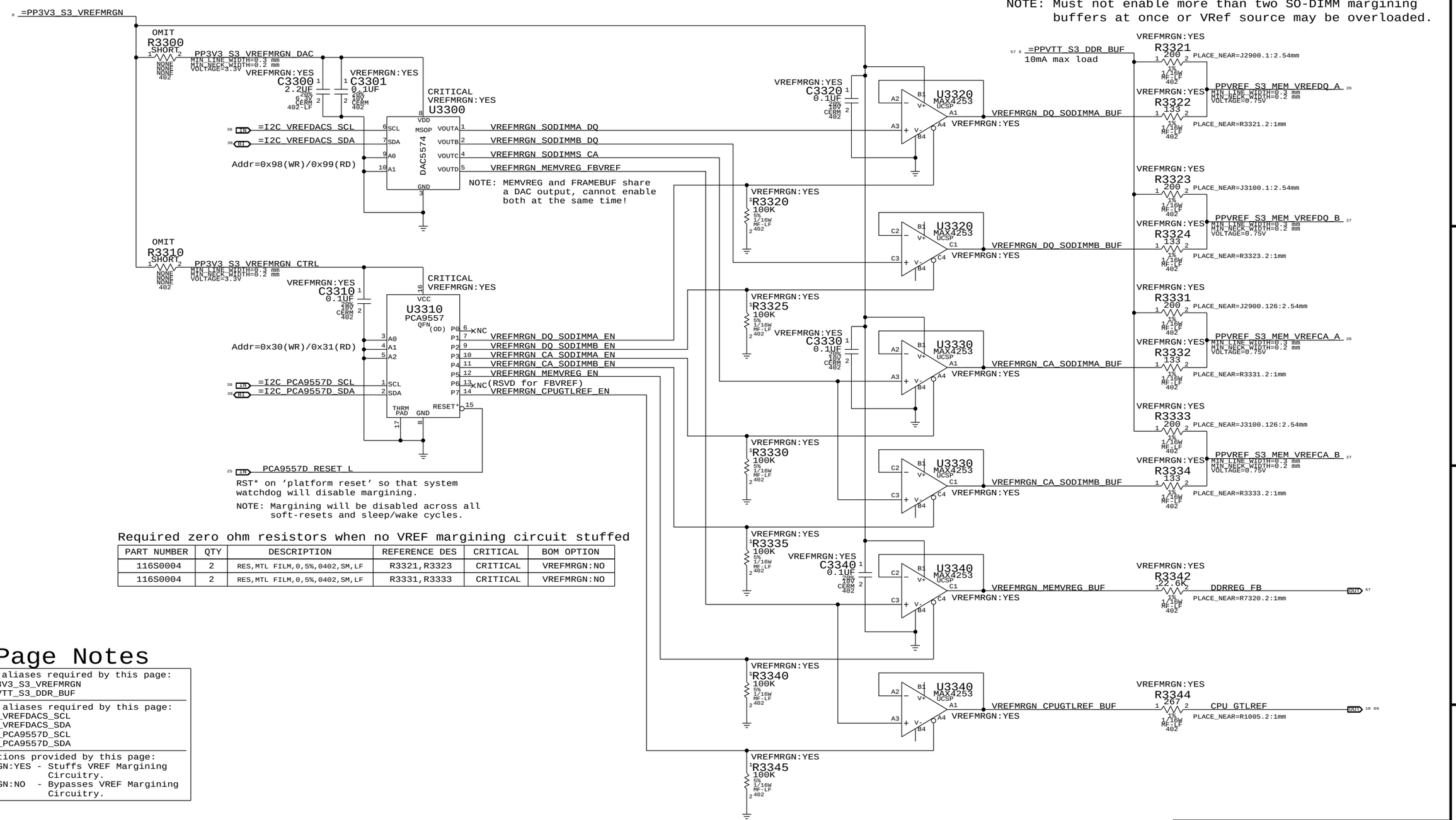
DRAWING NUMBER 051-8407 SIZE D

REVISION A.0.0

BRANCH

PAGE 32 OF 109

SHEET 28 OF 76



Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3321,R3323	CRITICAL	VREFMRGN:NO
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3331,R3333	CRITICAL	VREFMRGN:NO

Page Notes

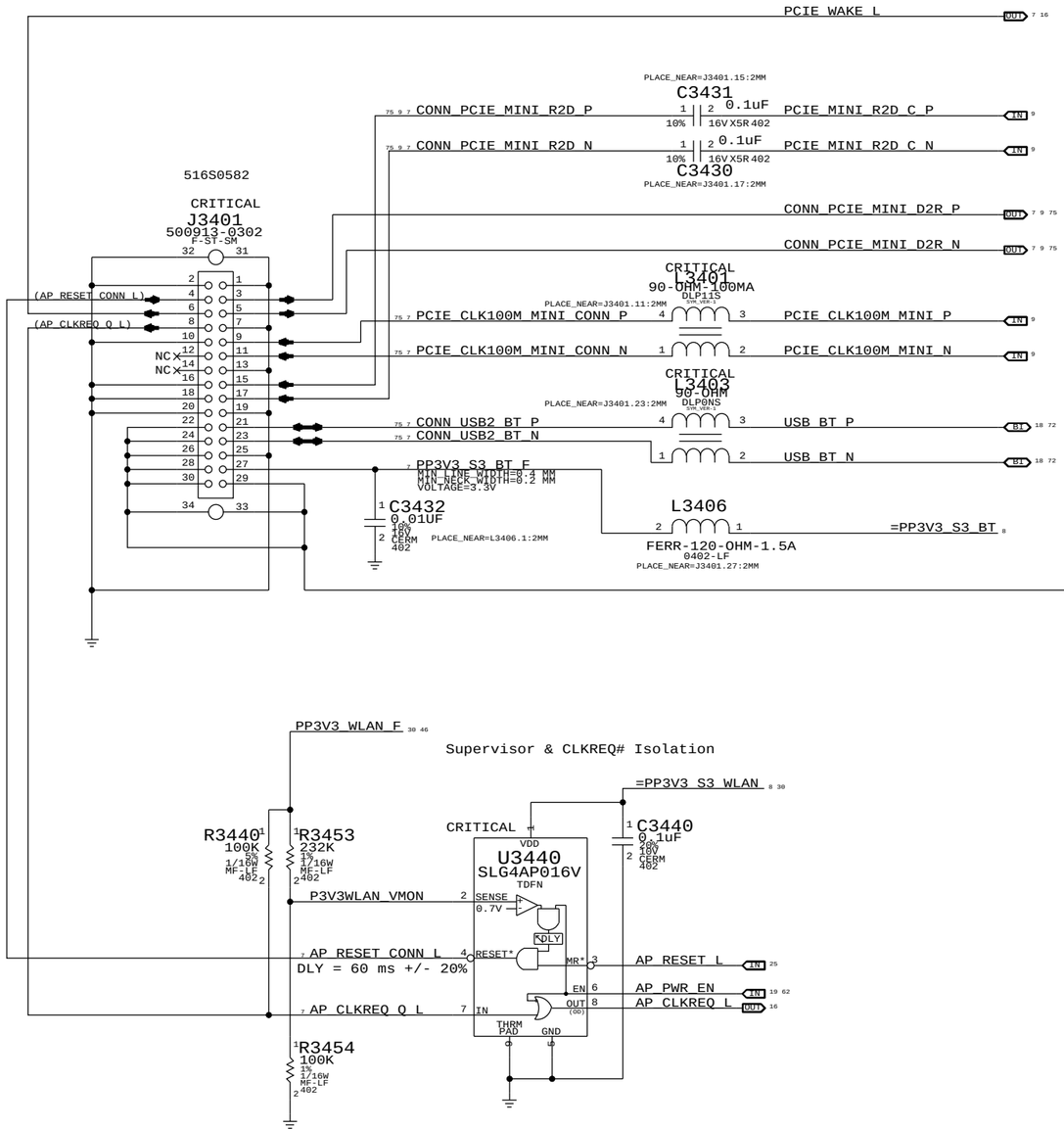
Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN:YES - Stuffs VREF Margining Circuitry.
VREFMRGN:NO - Bypasses VREF Margining Circuitry.

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	CPU GTLREF (FSB)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	7
Nominal value	0.75V (DAC: 0x3A)				1.5V (DAC: 0x3A)	0.7V (DAC: 0x8B)
Margined target:	0.300V - 1.200V (+/- 450mV)				1.998V - 1.002V (+/- 498mV)	0.200V - 1.050V (+/- 500mV)
DAC range:	0.000V - 1.501V (0x00 - 0x74)				0.000V - 1.501V (0x00 - 0x74)	0.000V - 1.191V (0x00 - 0x5C)
VRef current:	+3.4mA - -3.4mA (- = sourced)				+33uA - -33uA (- = sourced)	+750uA - -528uA (- = sourced)
DAC step size:	7.69mV / step @ output				8.59mV / step @ output	9.24mV / step @ output

SYNC_MASTER=K87_MLB SYNC_DATE=02/26/2010
PAGE TITLE
FSB/DDR3 Vref Margining
Apple Inc.
DRAWING NUMBER 051-8407 SIZE D
REVISION A.0.0
BRANCH
PAGE 33 OF 109
SHEET 29 OF 76



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
101S0245	1	RES,0OHM,5%,1/4W,MF-LF,1206	R3452		SENS_R:PROD

DO NOT SYNC WITH K84. CHANGED MINI_RESET_CONN_L CIRCUIT FROM SCHMITT TRIGGER TO SLG PART COPIED FROM K69. R3453 IS DIFFERENT FROM K6

SYNC_MASTER=K87_MLB SYNC_DATE=02/26/2010

PAGE TITLE: X16 WIRELESS CONNECTOR

Apple Inc.

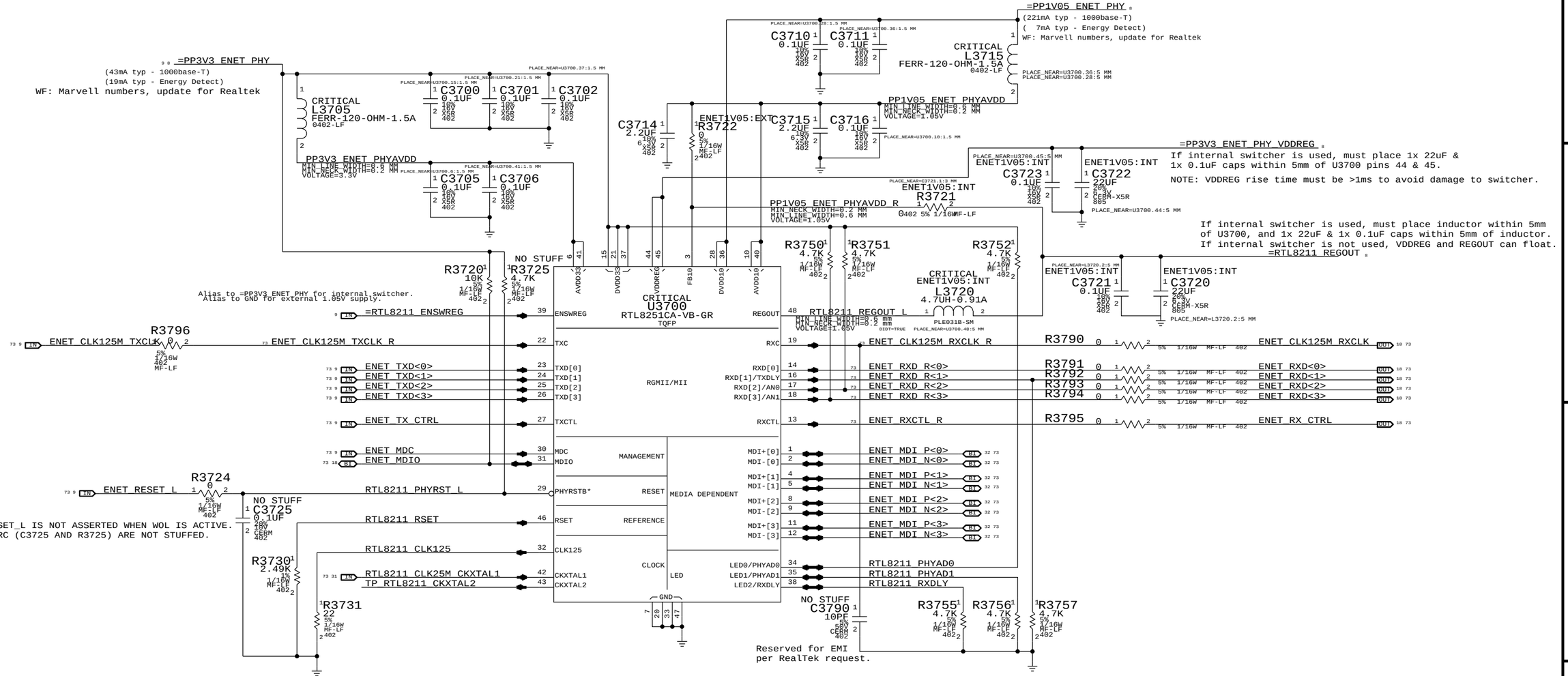
DRAWING NUMBER: 051-8407 SIZE: D

REVISION: A.0.0

BRANCH:

PAGE: 34 OF 109

SHEET: 30 OF 76



RTL8211 25MHz Clock

NOTE: MCP89 CAN PROVIDE 25MHZ CLOCK, BUT CLOCK RUNS WHENEVER RMGT RAILS ARE POWERED.
Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.

Configuration Settings:

PHYAD = 01 (PHY Address 00001)
AN[1:0] = 11 (Full auto-negotiation)
RXDLY = 0 (RXCLK transitions with data)
TXDLY = 0 (No TXCLK Delay)

DO NOT SYNC, EXTERNAL 1.05V REGULATOR OPTION

SYNC_MASTER=K87_MLB SYNC_DATE=02726?2010

PAGE TITLE

Ethernet PHY (RTL8211CL)

Apple Inc.

DRAWING NUMBER 051-8407
SIZE D
REVISION A.0.0
BRANCH
PAGE 37 OF 109
SHEET 31 OF 76

- COPY THIS PAGE FROM K36 CSA.39

ENET_MDI_x<1> pinswapped for layout

PLACE_NEAR=T3900.3:2.54 MM
PLACE_NEAR=T3900.4:2.54 MM
PLACE_NEAR=T3901.4:2.54 MM
PLACE_NEAR=T3901.3:2.54 MM

ENET_CONN_CTAP

C3900 0.1UF 10% 16V X5R 402
C3901 0.1UF 10% 16V X5R 402
C3902 0.1UF 10% 16V X5R 402
C3903 0.1UF 10% 16V X5R 402

CRITICAL
T3901
SM
TX →
TLA-6T213HF
← RX

CRITICAL
T3902
SM
TX →
TLA-6T213HF
← RX

R3903 75 1% 1/16W MF-LF 402
R3902 75 1% 1/16W MF-LF 402
R3901 75 1% 1/16W MF-LF 402
R3900 75 1% 1/16W MF-LF 402

ENET_CENTER_TAP<1>
ENET_CENTER_TAP<3>
ENET_CENTER_TAP<2>
ENET_CENTER_TAP<0>

ENET_MDI_P<1>
ENET_MDI_N<1>
ENET_MDI_P<3>
ENET_MDI_N<3>
ENET_MDI_N<2>
ENET_MDI_P<2>
ENET_MDI_N<0>
ENET_MDI_P<0>

ENET_MDI_TRAN_P<1>
ENET_MDI_TRAN_N<1>
ENET_MDI_TRAN_P<3>
ENET_MDI_TRAN_N<3>
ENET_MDI_TRAN_N<2>
ENET_MDI_TRAN_P<2>
ENET_MDI_TRAN_N<0>
ENET_MDI_TRAN_P<0>

D3900 RCLAMP0524P SLP2510P8
ENET_ESD CRITICAL

D3901 RCLAMP0524P SLP2510P8
ENET_ESD CRITICAL

Transformers should be mirrored on opposite sides of the board

D3900.1: PLACE_NEAR=T3901.6:4 MM
D3900.5: PLACE_NEAR=T3902.2:4 MM

D3901.1: PLACE_NEAR=T3902.6:4 MM
D3901.5: PLACE_NEAR=T3901.2:4 MM

ETHERNET CONNECTOR

CRITICAL
J3900
RJ45-10/100TX-K83
F-R-TH1
ENET_MDI
TRAN_P0
TRAN_N0
TRAN_P1
TRAN_P2
TRAN_N2
TRAN_N1
TRAN_P3
TRAN_N3
SHIELD PINS
514-0704

ENET_BOB_SMITH_CAP
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.25MM

CRITICAL
C3910
1000PF
10%
2KV
CERM
1206

DO NOT SYNC FROM K6, WITH K84’S CONNECTOR

SYNC MASTER=K87_MLB SYNC DATE=02726720100

PAGE TITLE
ETHERNET CONNECTOR

Apple Inc.

DRAWING NUMBER 051-8407
SIZE D
REVISION A.0.0
BRANCH
PAGE 39 OF 109
SHEET 32 OF 76

SIL

518S0519

CRITICAL
J4502
78171-0002
M-RT-SM

R4531
4.7
5% 1/16W
MF-LF
402

L4530
FERR-1000-OHM
0402

L4531
FERR-1000-OHM
0402

C4531
0.001UF
10%
50V
CERM
402

SYS_LED_ANODE
SYS_LED_ANODE_R
SYS_LED_ANODE_UF
SYS_LED_RETURN_UF

ODD Power Control

=PP5V_S3_ODD
=PP3V3_S0_ODD

R4596
100K
5%
1/16W
MF-LF
402

R4597
100K
5%
1/16W
MF-LF
402

Q4596
SSM6N15FEAPE
SOT563

Q4596
SSM6N15FEAPE
SOT563

ODD_PWR_EN
ODD_PWR_EN_L
ODD_PWR_EN_LS5V_L

R4595
100K
5%
1/16W
MF-LF
402

C4595
0.068UF
10%
16V
CERM
402

CRITICAL
Q4590
TPCP8102
23V1K-SM

C4596
0.01UF
10%
16V
CERM
402

ODD_PWR_SS

PP5V_SW_ODD_R
MIN_LINE_WIDTH=0.6mm
MIN_NECK_WIDTH=0.4mm
VOLTAGE=5V

NOTE: 3.3V must be S0 if 5V is S3 or S5 to
ensure the drive is unpowered in S3/S5.

SENS_R:ENG
CRITICAL
R4598
0.002
1%
1/4W
MF
1206

ISNS_ODD_P
ISNS_ODD_N

PP5V_SW_ODD
MIN_LINE_WIDTH=0.6mm
MIN_NECK_WIDTH=0.4mm
VOLTAGE=5V

SATA ODD

=PP3V3_S0_ODD

R4590
33K
5%
1/16W
MF-LF
402

SMC_ODD_DETECT
Indicates disc presence

CRITICAL
J4500
54722-0164
F-ST-SM

516S0616

SATA_ODD_R2D_P
SATA_ODD_R2D_N
SATA_ODD_D2R_C_N
SATA_ODD_D2R_C_P

CRITICAL
FL4520
90-OHM-100MA
DLP11S

SATA_ODD_R2D_UF_P
SATA_ODD_R2D_UF_N

PLACE_NEAR=C4520:3MM
C4521
0.01UF
10%16V CERM 402
SATA_ODD_R2D_C_P

C4520
0.01UF
10%16V CERM 402
SATA_ODD_R2D_C_N

PLACE_NEAR=J4500.6:4MM
PLACE_NEAR=U1400.AJ2:3MM

CRITICAL
FL4525
90-OHM-100MA
DLP11S

SATA_ODD_D2R_UF_N
SATA_ODD_D2R_UF_P

PLACE_NEAR=FL4525.3:3MM
C4526
0.01UF
10%16V CERM 402
SATA_ODD_D2R_N

C4525
0.01UF
10%16V CERM 402
SATA_ODD_D2R_P

PLACE_NEAR=J4500.10:4MM
PLACE_NEAR=C4526:3MM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
101S0245	2	RES,0OHM,5%,1/4W,MF-LF,1206	R4599,R4598		SENS_R:PROD

SATA HDD

SENS_R:ENG
CRITICAL
R4599
0.002
1%
1/4W
MF
1206

=PP5V_S0_HDD

C4502
0.1UF
20%
10V
CERM
402

ISNS_HDD_P
ISNS_HDD_N

PLACE_NEAR=L4500.2:2mm

CRITICAL
L4500
FERR-70-OHM-4A
0603

PP5V_S0_HDD_FLT
PP5V_S0_HDD_R
MIN_LINE_WIDTH=0.6mm
MIN_NECK_WIDTH=0.2mm
VOLTAGE=5V
MIN_LINE_WIDTH=0.6mm
MIN_NECK_WIDTH=0.4mm
VOLTAGE=5V

PLACE_NEAR=J4501.9:3mm

Passive de-emphasis filter
Use 0-ohm resistors and NOSTUFF caps if not using

CRITICAL
J4501
54722-0164
F-ST-SM

516S0616

NCX

SATA_HDD_D2R_C_P
SATA_HDD_D2R_C_N
SATA_HDD_R2D_N
SATA_HDD_R2D_P

CRITICAL
FL4502
90-OHM-100MA
DLP11S

SATA_HDD_D2R_UF_P
SATA_HDD_D2R_UF_N

C4516
0.01UF
10%16V CERM 402
SATA_HDD_D2R_FILT_P

C4515
0.01UF
10%16V CERM 402
SATA_HDD_D2R_FILT_N

PLACE_NEAR=J4501.6:3MM
PLACE_NEAR=J4501.6:3MM
PLACE_NEAR=C4516.1:3MM

C4586
47PF
5%
CERM
50V
402

R4586
27.4
1%
MF-LF
1/16W
402

R4585
27.4
1%
MF-LF
1/16W
402

C4585
47PF
5%
CERM
50V
402

PLACEMENT_NOTE: Place R4585,R4586,C4585,C4586 on the same side.
Resistors should be on inside, with SATA passing straight through.

SATA_HDD_D2R_P
SATA_HDD_D2R_N

CRITICAL
FL4501
90-OHM-100MA
DLP11S

SATA_HDD_R2D_UF_N
SATA_HDD_R2D_UF_P

C4511
0.01UF
10%16V CERM 402
SATA_HDD_R2D_C_N

C4510
0.01UF
10%16V CERM 402
SATA_HDD_R2D_C_P

PLACE_NEAR=J4501.12:3MM
PLACE_NEAR=C4510.1:3MM
PLACE_NEAR=J4501.14:3MM

SYNC_MASTER=K87_MLB SYNC_DATE=02/26/2010

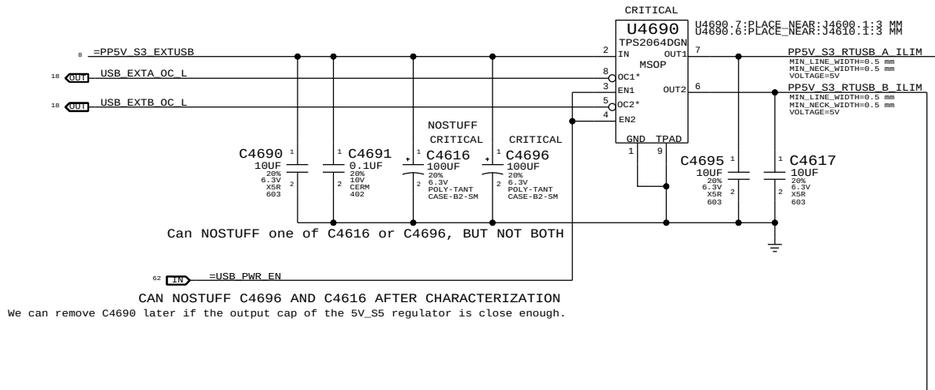
PAGE TITLE
SATA Connectors

Apple Inc.

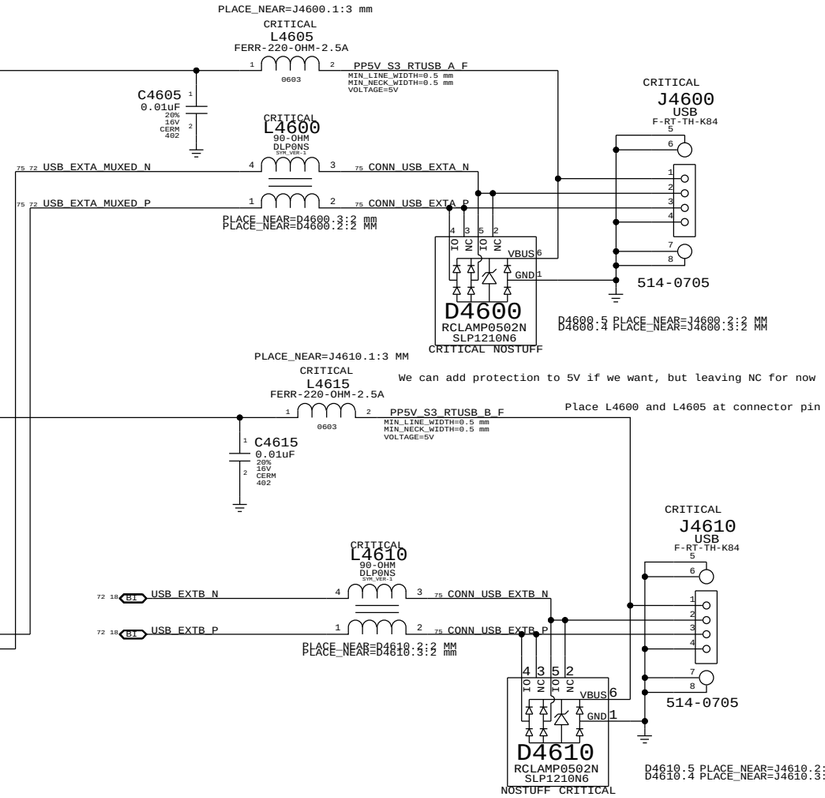
DRAWING NUMBER 051-8407
SIZE D
REVISION A.0.0
BRANCH
PAGE 45 OF 109
SHEET 33 OF 76

POR IS METAL USB CONNECTOR PARTS

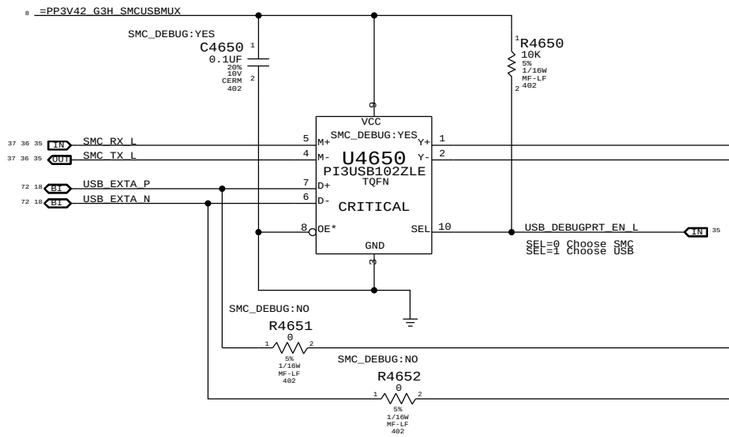
Port Power Switch



USB PORT A (FRONT PORT)



USB/SMC Debug Mux



USB PORT B (BACK PORT)

DO NOT SYNC WITH K84. UPDATED PLACE NEAR NOTES
UPDATED SMC_DEBUG BOMOPTION, STUFFED C4690

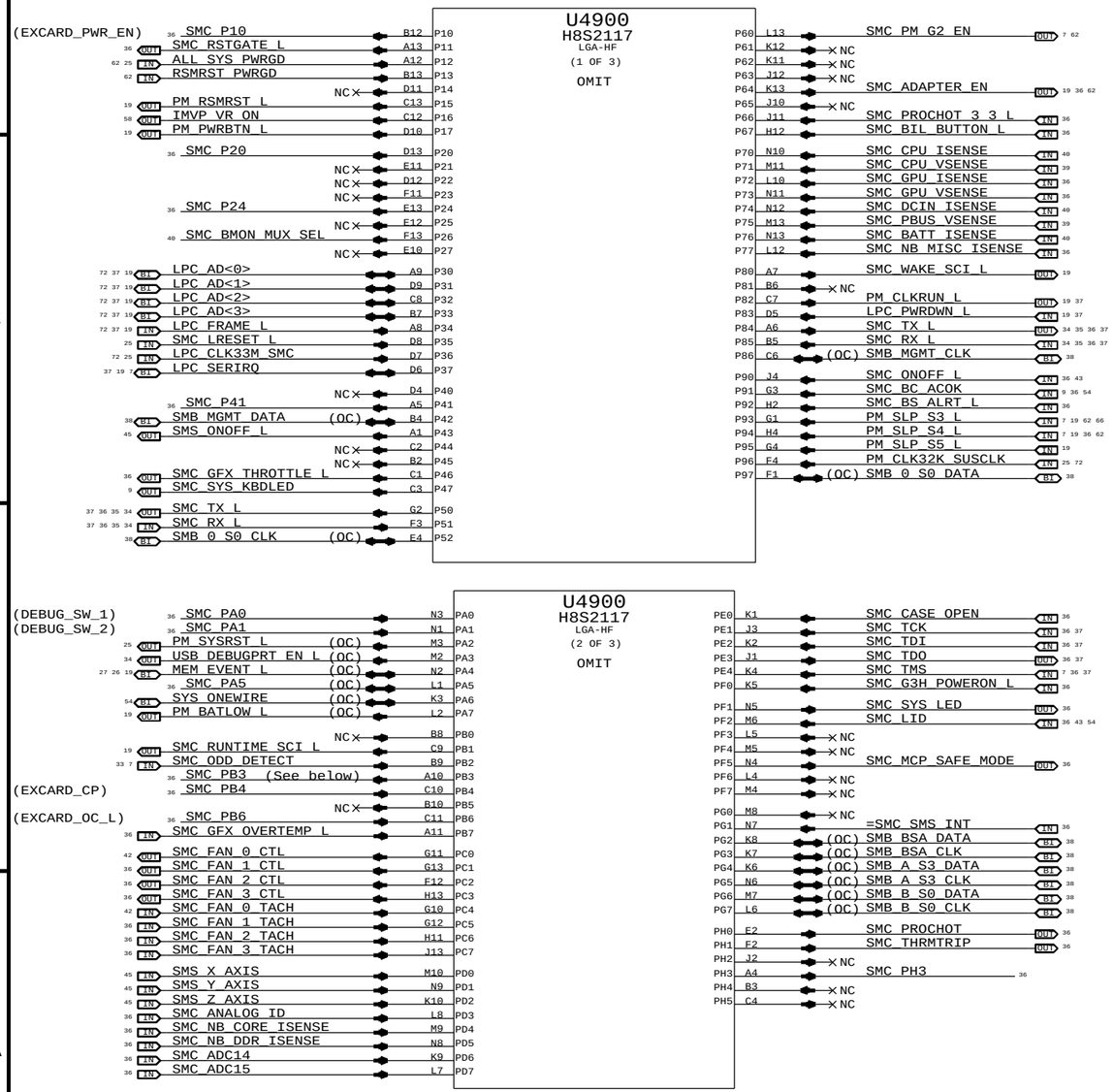
SYNC_MASTER=K87_MLB SYNC_DATE=02/26/2010

PAGE TITLE: External USB Connectors

Apple Inc.

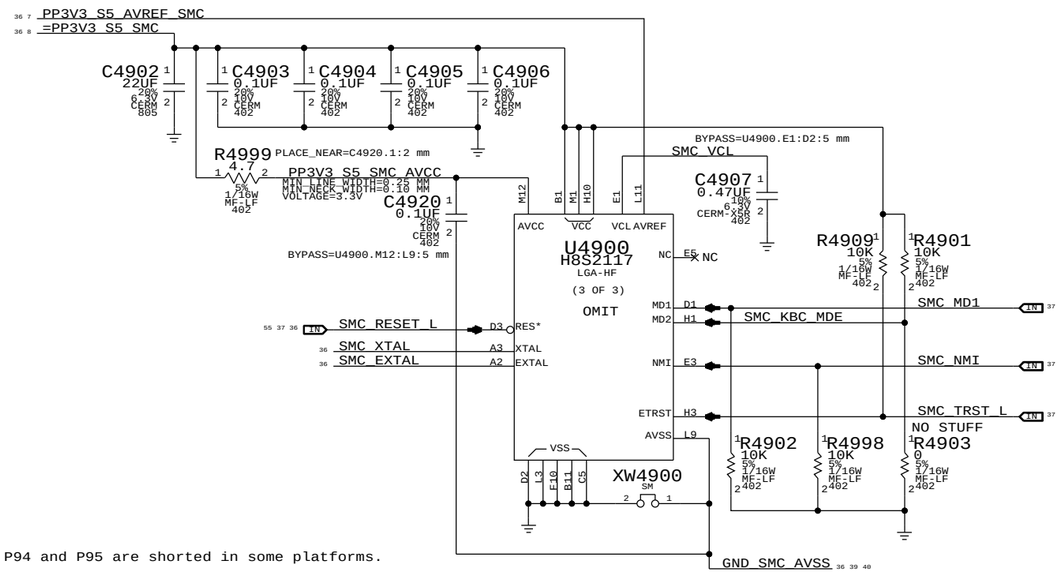
DRAWING NUMBER: 051-8407 SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 46 OF 109
SHEET: 34 OF 76

NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.



SMC_PB3:

SMC_IG_THROTTLE_L for MG systems.
Otherwise, TP/NC okay.



NOTE: P94 and P95 are shorted in some platforms.

NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

H8S2117-R:
(SMC_PECI)
(SMC_PECI_VREF)
(SMC_PECI_VSTP)

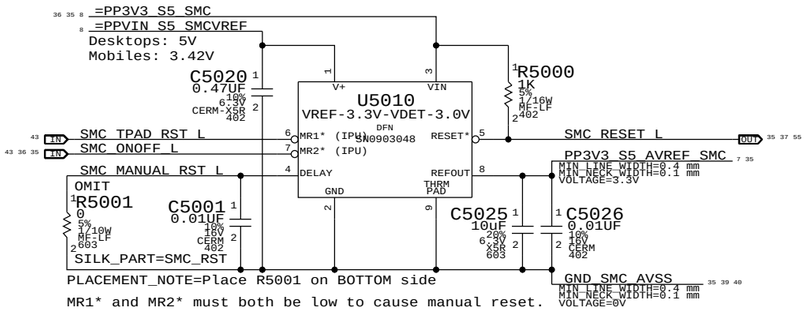
SYNC_MASTER=K87_MLB SYNC_DATE=02/26/2010

PAGE TITLE: SMC

Apple Inc.

DRAWING NUMBER: 051-8407 SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 49 OF 109
SHEET: 35 OF 76

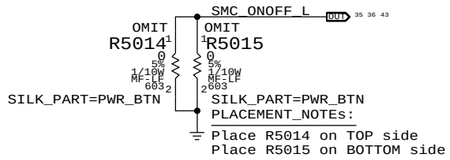
SMC Reset "Button", Supervisor & AVREF Supply



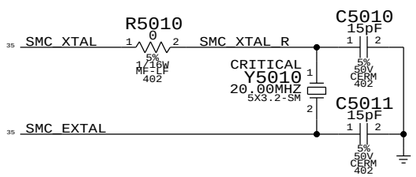
MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.

NOTE: Internal pull-ups are to VIN, not V+.

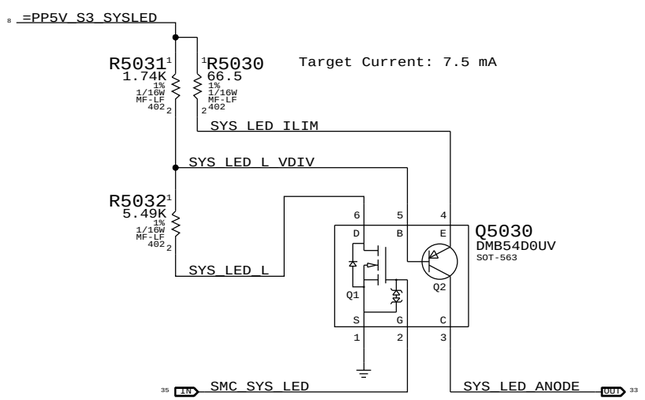
Debug Power "Buttons"



SMC Crystal Circuit



System (Sleep) LED Circuit



R5030,R5031,R5032 CHANGED FOR DIMMER LED

SMC Aliases

SMC_MCP_VSENSE	=	SMC_ADC14
SMC_CPU_FSB_ISENSE	=	SMC_ADC15
SMC_MCP_CORE_ISENSE	=	SMC_NB_CORE_ISENSE
SMC_MCP_DDR_ISENSE	=	SMC_NB_DDR_ISENSE
TP_SMC_CPU_HI_ISENSE	=	SMC_NB_MISC_ISENSE
TP_SMC_GPU_1V8_ISENSE	=	SMC_ANALOG_ID
TP_SMC_GPU_ISENSE	=	SMC_GPU_ISENSE
TP_SMC_GPU_VSENSE	=	SMC_GPU_VSENSE
SMC_GFX_THROTTLE_L	=	SMC_IG_THROTTLE_L
SMS_INT_L	=	=SMC_SMS_INT
MCP_WAKE_REQ_L	=	SMC_G3H_POWERON_L

All: MAKE_BASE=TRUE

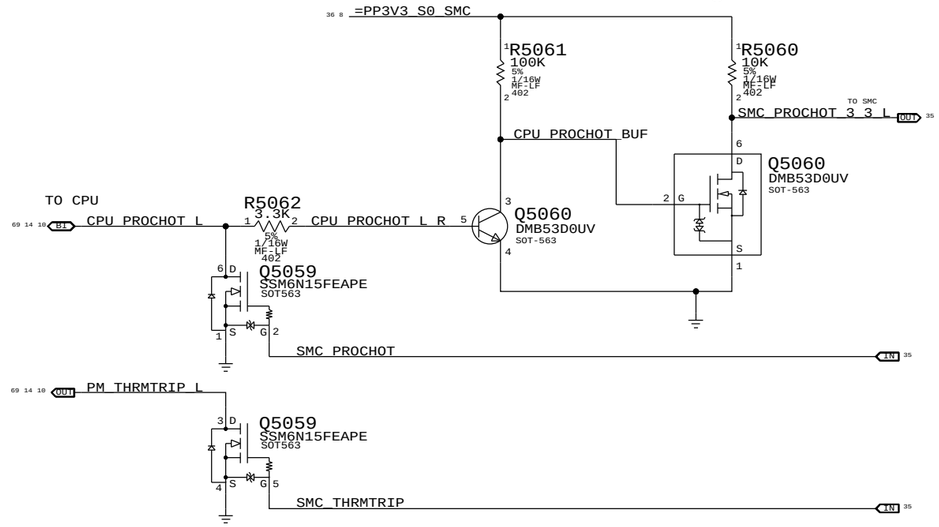
R5096 0 5% 1/16W MF-LF 402
SMC_MCP_SAFE_MODE — MCP_SPKR

Unused Pins

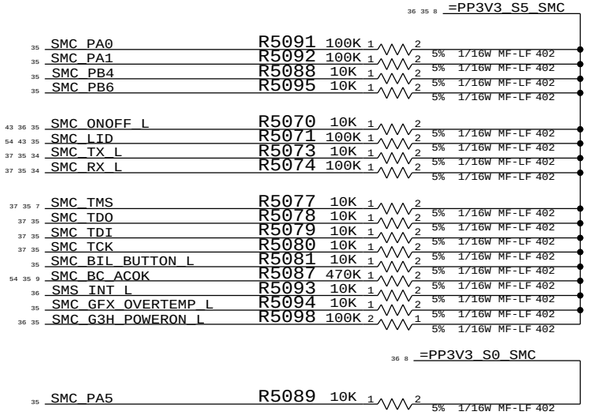
SMC_FAN_1_CTL	=	TP_SMC_FAN_1_CTL
TP_SMC_FAN_1_TACH	=	SMC_FAN_1_TACH
SMC_FAN_2_CTL	=	NC_SMC_FAN_2_CTL
NC_SMC_FAN_2_TACH	=	SMC_FAN_2_TACH
SMC_FAN_3_CTL	=	NC_SMC_FAN_3_CTL
NC_SMC_FAN_3_TACH	=	SMC_FAN_3_TACH
SMC_RSTGATE_L	=	TP_SMC_RSTGATE_L
SMC_P10	=	TP_SMC_P10
SMC_P20	=	TP_SMC_P20
SMC_P24	=	TP_SMC_P24
SMC_P41	=	TP_SMC_P41
SMC_PB3	=	TP_SMC_PB3
SMC_PH3	=	TP_SMC_PH3

MAKE_BASE=TRUE; NO_TEST=TRUE

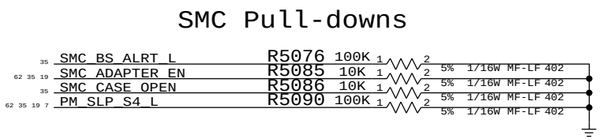
SMC FSB to 3.3V Level Shifting



SMC Pull-ups



SMC Pull-downs



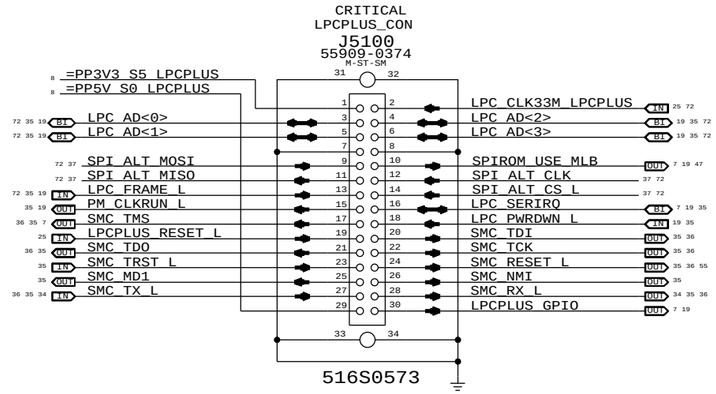
SYNC_MASTER=K87_MLB SYNC_DATE=02/26/2010

PAGE TITLE: SMC Support

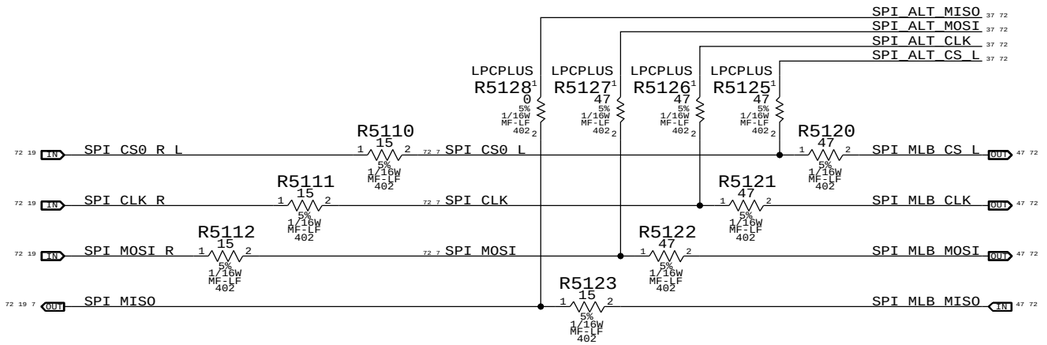
Apple Inc.

DRAWING NUMBER: 051-8407 SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 50 OF 109
SHEET: 36 OF 76

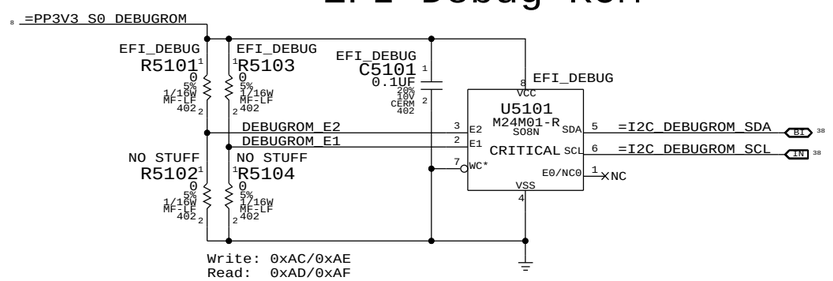
LPC+SPI Connector



SPI Bus Series Termination



EFI Debug ROM



SYNC_MASTER=K87_MLB SYNC_DATE=02/26/2010

PAGE TITLE: LPC+SPI Debug Connector

Apple Inc.

DRAWING NUMBER: 051-8407 SIZE: D

REVISION: A.0.0

BRANCH:

PAGE: 51 OF 109

SHEET: 37 OF 76

MCP89 SMBus "0" Connections

=PP3V3_S0_SMBUS_MCP_0

MCP89
U1400
(MASTER)

SMBUS_MCP_0_CLK (MAKE_BASE=TRUE)
SMBUS_MCP_0_DATA (MAKE_BASE=TRUE)

R5200 1K 5% 1/16W MF-LF 402
R5201 1K 5% 1/16W MF-LF 402

SO-DIMM "A"
J2900
(Write: 0xA0 Read: 0xA1)
=I2C_SODIMMA_SCL
=I2C_SODIMMA_SDA

SO-DIMM "B"
J3100
(Write: 0xA2 Read: 0xA3)
=I2C_SODIMMB_SCL
=I2C_SODIMMB_SDA

Mikey
CD3275: U6880
(Write: 0x72 Read: 0x73)
=I2C_MIKEY_SCL
=I2C_MIKEY_SDA

Debug Devices
(Not stuffed in production)

Vref DACs
DAC5574: U3300
(Write: 0x98 Read: 0x99)
=I2C_VREFDACS_SCL
=I2C_VREFDACS_SDA

Margin Control
PCA9557: U3310
(Write: 0x30 Read: 0x31)
=I2C_PCA9557D_SCL
=I2C_PCA9557D_SDA

EFI Debug Serial
M24M01: U5101
(Write: 0xAC/0xAE
Read: 0xAD/0xAF)
=I2C_DEBUGROM_SCL
=I2C_DEBUGROM_SDA

MCP89 SMBus "1" Connections

=PP3V3_S0_SMBUS_MCP_1

MCP89
U1400
(Write: 0xE0 Read: 0xE1)

SMBUS_MCP_1_CLK (MAKE_BASE=TRUE)
SMBUS_MCP_1_DATA (MAKE_BASE=TRUE)

NO STUFF
R5230 2.0K 5% 1/16W MF-LF 402
NO STUFF
R5231 2.0K 5% 1/16W MF-LF 402

R5235 0 5% 1/16W MF-LF 402
R5236 0 5% 1/16W MF-LF 402

MCP89 SMBus 1 is slave port to access internal thermal sensors

Another slave port is available at 0x10/0x11, probably not used.

SMC "0" SMBus Connections

=PP3V3_S0_SMBUS_SMC_0_S0

SMC
U4900
(MASTER)

SMB_0_S0_CLK
SMB_0_S0_DATA

SMBUS_SMC_0_S0_SCL (MAKE_BASE=TRUE)
SMBUS_SMC_0_S0_SDA (MAKE_BASE=TRUE)

R5250 10K 5% 1/16W MF-LF 402
R5251 10K 5% 1/16W MF-LF 402

Debug Temp
TMP442A: U5535
(WRITE: 0x98 READ: 0x99)
=I2C_MCPTHMSNS_SCL
=I2C_MCPTHMSNS_SDA

SMC "A" SMBus Connections

NOTE: SMC RMT bus remains powered and may be active in S3 state

=PP3V3_S3_SMBUS_SMC_A_S3

SMC
U4900
(MASTER)

SMB_A_S3_CLK
SMB_A_S3_DATA

SMBUS_SMC_A_S3_SCL (MAKE_BASE=TRUE)
SMBUS_SMC_A_S3_SDA (MAKE_BASE=TRUE)

R5270 1K 5% 1/16W MF-LF 402
R5271 1K 5% 1/16W MF-LF 402

Trackpad
J5800
(Write: 0x90 Read: 0x91)
=I2C_TPAD_SCL
=I2C_TPAD_SDA

SMC "B" SMBus Connections

=PP3V3_S0_SMBUS_SMC_B_S0

SMC
U4900
(MASTER)

SMB_B_S0_CLK
SMB_B_S0_DATA

SMBUS_SMC_B_S0_SCL (MAKE_BASE=TRUE)
SMBUS_SMC_B_S0_SDA (MAKE_BASE=TRUE)

R5260 4.7K 5% 1/16W MF-LF 402
R5261 4.7K 5% 1/16W MF-LF 402

Prod Temp
EMC1413: U5515
(Write: 0x98 Read: 0x99)
=I2C_CPUTHMSNS_SCL
=I2C_CPUTHMSNS_SDA

SMC "Battery A" SMBus Connections

=PP3V42_G3H_SMBUS_SMC_BSA

SMC
U4900
(MASTER)

SMB_BSA_CLK
SMB_BSA_DATA

SMBUS_SMC_BSA_SCL (MAKE_BASE=TRUE)
SMBUS_SMC_BSA_SDA (MAKE_BASE=TRUE)

R5280 2.61K 1% 1/16W MF-LF 402
R5281 2.61K 1% 1/16W MF-LF 402

Battery Charger
ISL6259 - U7000
(Write: 0x12 Read: 0x13)
=SMBUS_CHGR_SCL
=SMBUS_CHGR_SDA

BATTERY
J6950
(See Table)
=SMBUS_BATT_SCL
=SMBUS_BATT_SDA

Battery

Battery Manager - (Write: 0x16 Read: 0x17)
Battery LED Driver - (Write: 0x36 Read: 0x37)
Battery Temp - (Write: 0x90 Read: 0x91)

SMC "Management" SMBus Connections

The bus formerly known as "Battery B"

=PP3V3_S3_SMBUS_SMC_MGMT

SMC
U4900
(MASTER)

SMB_MGMT_CLK
SMB_MGMT_DATA

SMBUS_SMC_MGMT_SCL (MAKE_BASE=TRUE)
SMBUS_SMC_MGMT_SDA (MAKE_BASE=TRUE)

R5290 4.7K 5% 1/16W MF-LF 402
R5291 4.7K 5% 1/16W MF-LF 402

Debug ADC
LT2309: U6000
(Write: 0x10 Read: 0x11)
=I2C_SMC_ADCS_SCL
=I2C_SMC_ADCS_SDA

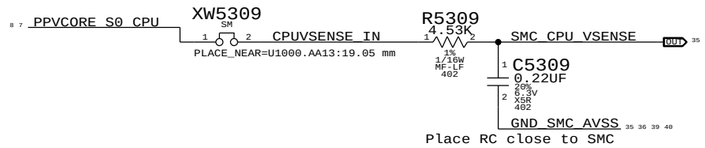
SYNC_MASTER=K87_MLB SYNC_DATE=02/26/2010

PAGE TITLE: K87 SMBus Connections

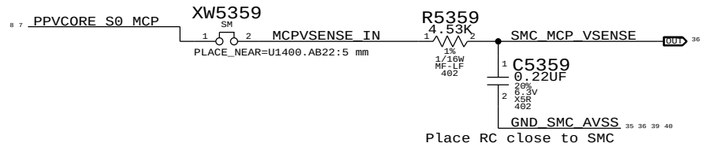
Apple Inc.

DRAWING NUMBER: 051-8407 SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 52 OF 109
SHEET: 38 OF 76

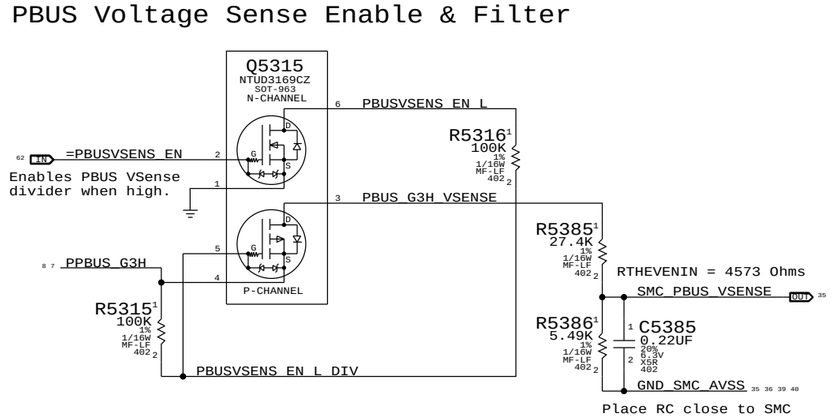
CPU Voltage Sense / Filter



MCP Voltage Sense / Filter



PBUS Voltage Sense Enable & Filter



SYNC_MASTER=K87_MLB SYNC_DATE=02/26/2010

PAGE TITLE: Voltage Sensing

Apple Inc.

DRAWING NUMBER: 051-8407 SIZE: D

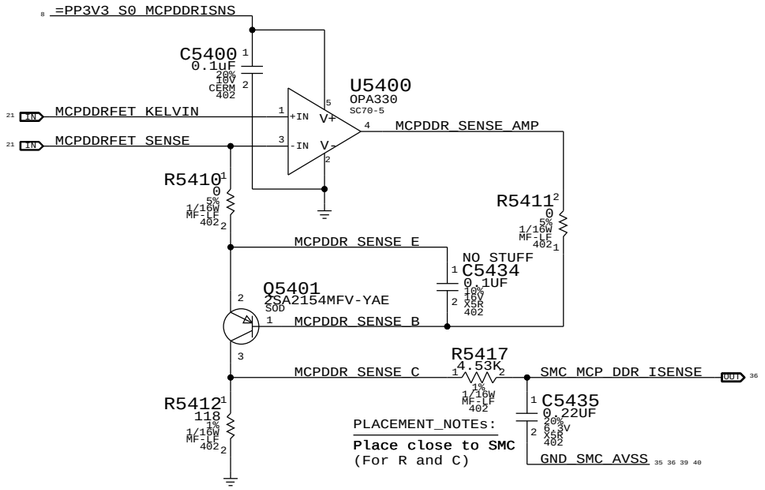
REVISION: A.0.0

BRANCH:

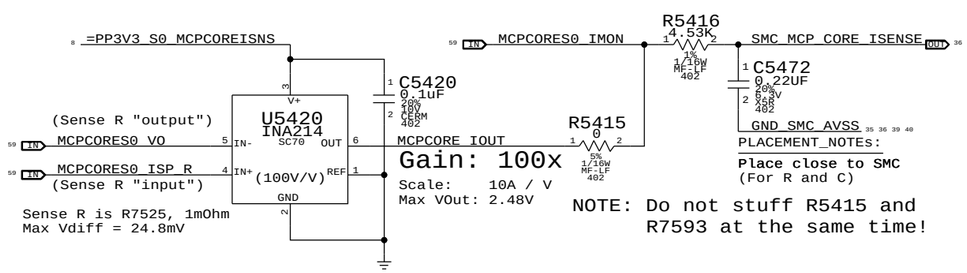
PAGE: 53 OF 109

SHEET: 39 OF 76

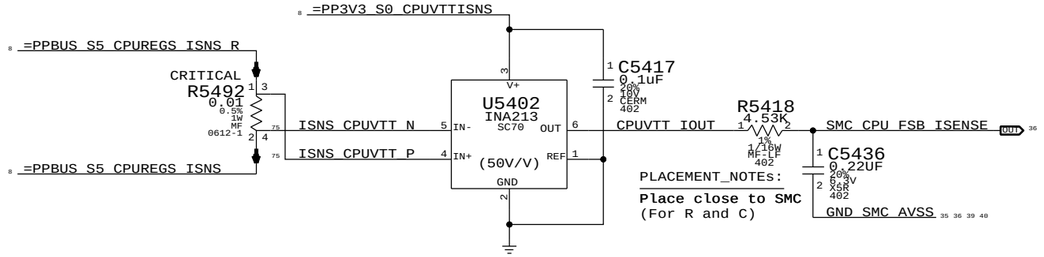
MCP MEM VDD Current Sense / Filter



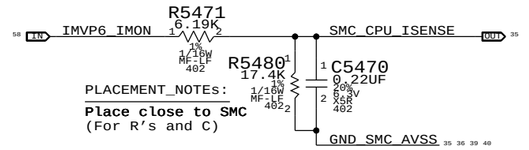
MCP VCore Current Sense Filter



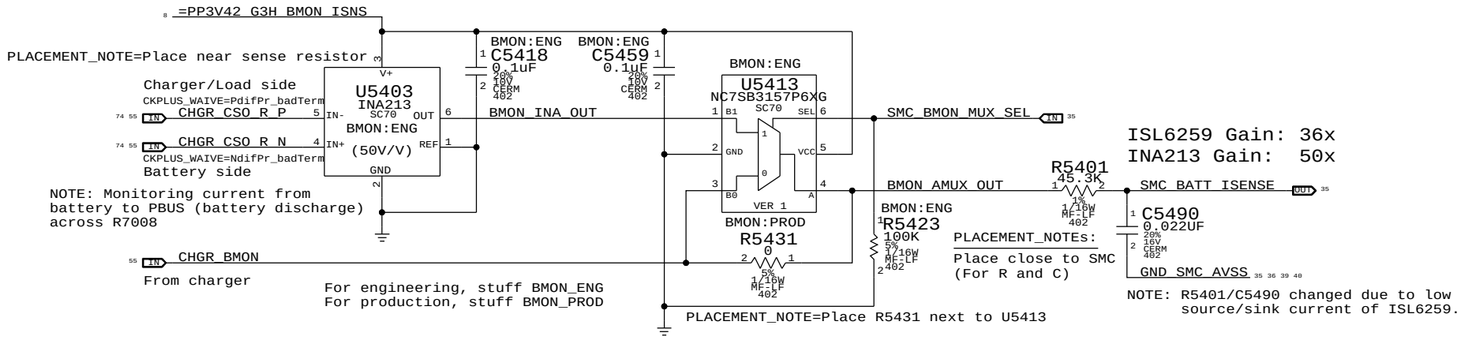
MCP/CPU 1.05V AND CPU VCore High-Side Current Sense / Filter



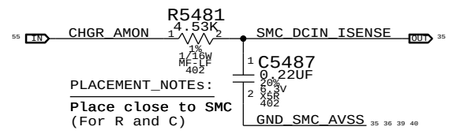
CPU VCore Load Side Current Sense / Filter



Battery (BMON) Current Sense, MUX & Filter



DC-IN (AMON) Current Sense Filter



SYNC_MASTER=K87_MLB SYNC_DATE=02/26/2010

PAGE TITLE: Current Sensing

Apple Inc.

DRAWING NUMBER: 051-8407 SIZE: D

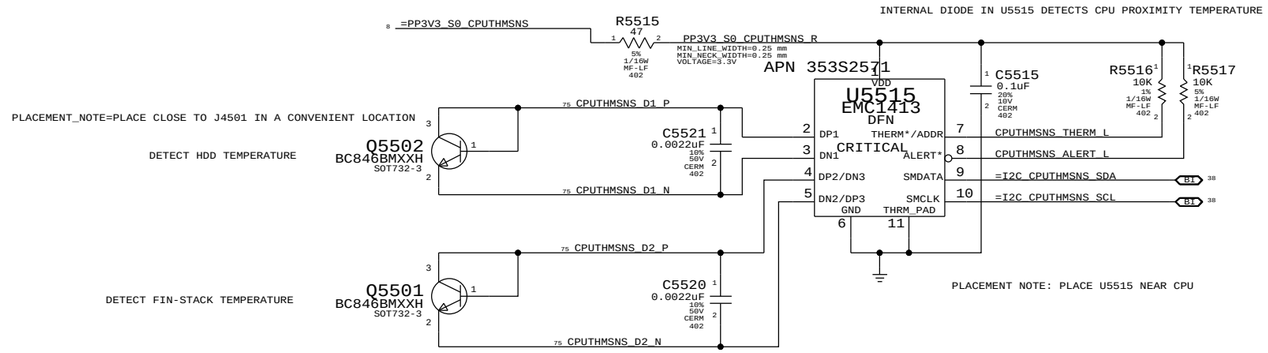
REVISION: A.0.0

BRANCH:

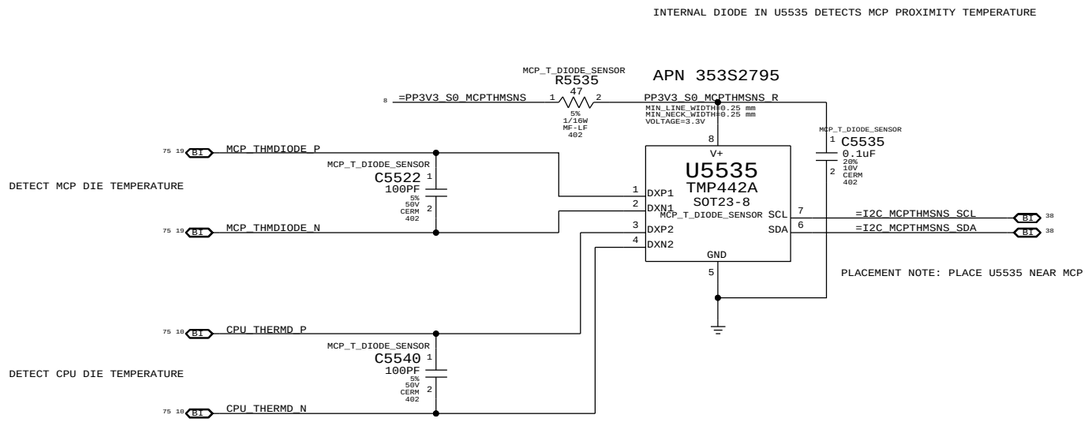
PAGE: 54 OF 109

SHEET: 40 OF 76

CPU PROXIMITY/HDD FLEX AREA/FINSTACK THERMAL SENSOR



MCP DIE/CPU DIE/MCP PROXIMITY THERMAL SENSOR



SYNC MASTER=K87_MLB SYNC DATE=02/26/2010

PAGE TITLE: Thermal Sensors

Apple Inc.

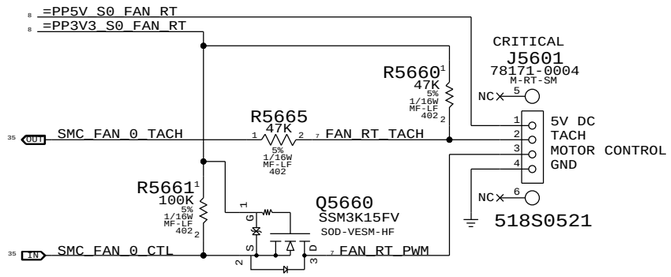
DRAWING NUMBER: 051-8407 SIZE: D

REVISION: A.0.0

BRANCH:

PAGE: 55 OF 109

SHEET: 41 OF 76



SYNC_MASTER=K87_MLB SYNC_DATE=02/26/2010

PAGE TITLE

Fan Connector

Apple Inc.

DRAWING NUMBER 051-8407 SIZE D

REVISION A.0.0

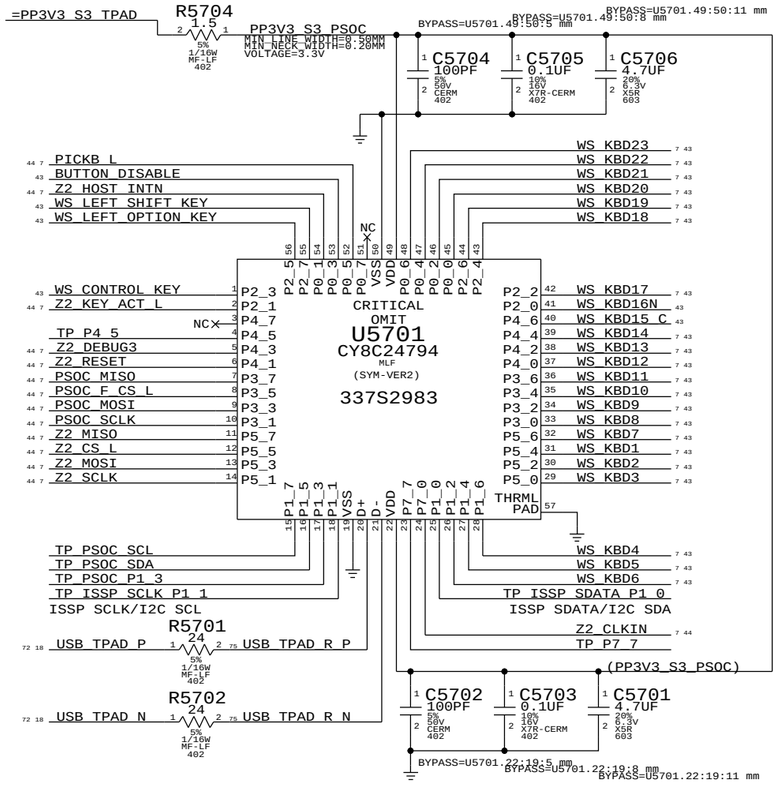
BRANCH

PAGE 56 OF 109

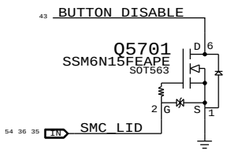
SHEET 42 OF 76

PSOC USB CONTROLLER

- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER



TPAD Buttons Disable

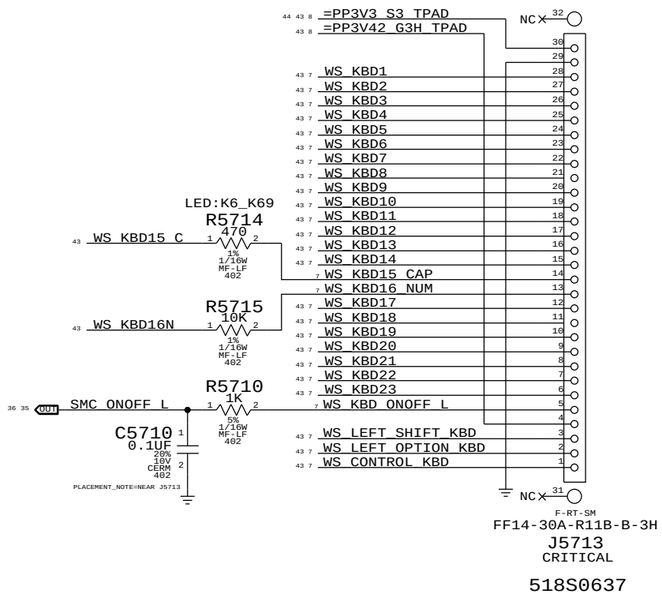


PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V

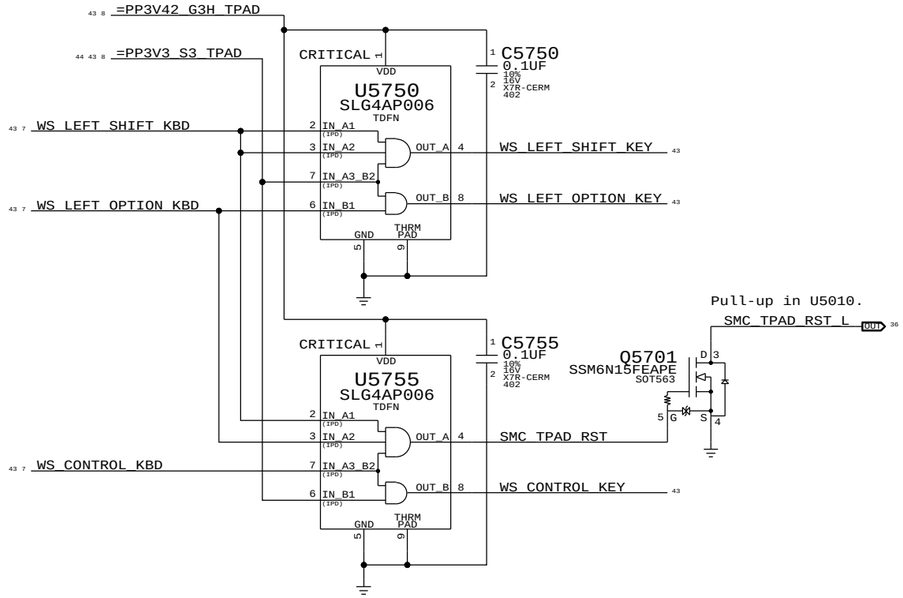
IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
		80UA		0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA (MAX)	10 OHM	0.6 V	36E-3 W
	VOUT	60MA (MAX)	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
		14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

Keyboard Connector



SMC Manual Reset & Isolation

Left shift, option & control keys combined with power button cause SMC RESET# assertion.
Keys ANDed with PSOC power to isolate when PSOC is not powered.



SYNC_MASTER=K87_MLB SYNC_DATE=02/26/2010

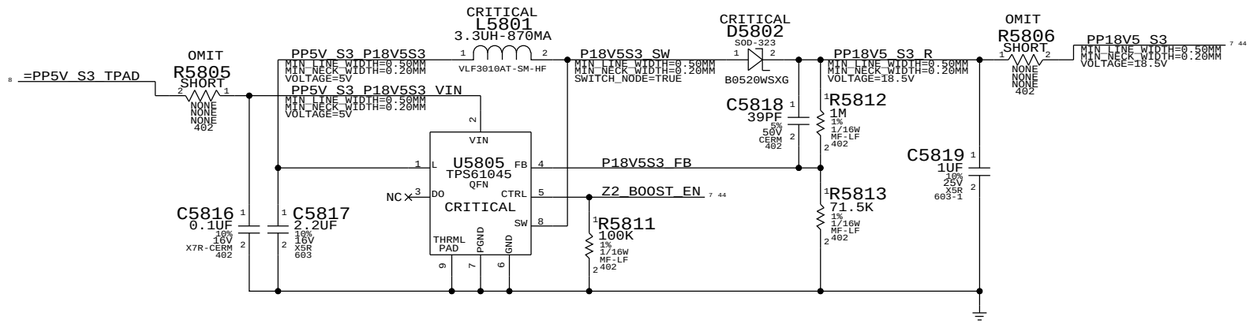
PAGE TITLE: WELLSPRING 1

Apple Inc.

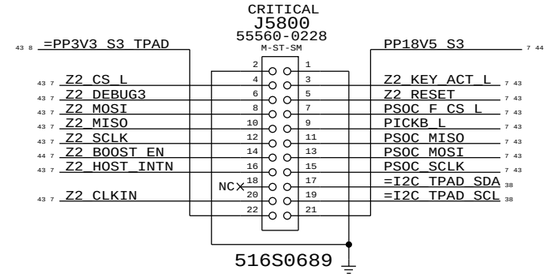
DRAWING NUMBER: 051-8407 SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 57 OF 109
SHEET: 43 OF 76

BOOSTER +18.5VDC FOR SENSORS

BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
- DROOP LINE REGULATION
- RIPPLE TO MEET ERS
- 100-300 KHZ CLEAN SPECTRUM
- STARTUP TIME LESS THAN 2MS
- R5812,R5813,C5818 MODIFIED



IPD Flex Connector



DO NOT SYNC FROM T27. REMOVED KEYBOARD BKLIGHT CIRCUIT

SYNC_MASTER=K87_MLB SYNC_DATE=02/26/2010

PAGE TITLE: WELLSPRING 2

Apple Inc.

DRAWING NUMBER: 051-8407 SIZE: D

REVISION: A.0.0

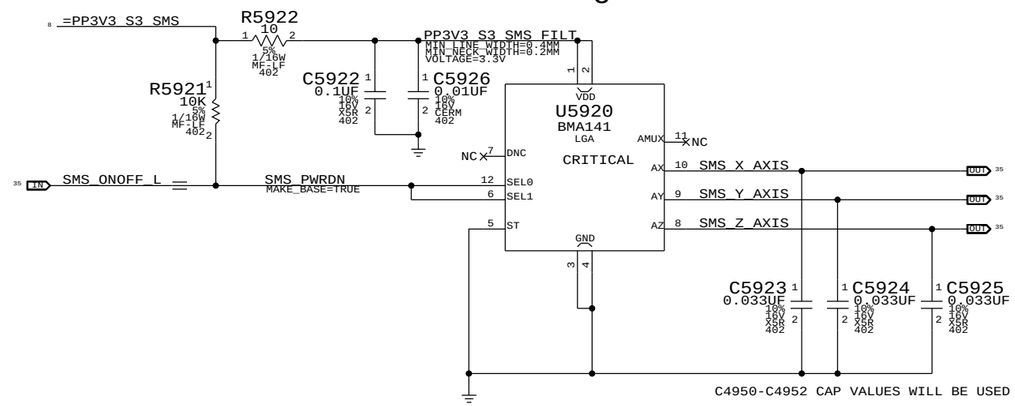
BRANCH:

PAGE: 58 OF 109

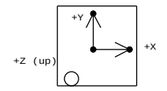
SHEET: 44 OF 76

R5921 PULLS UP SEL PINS TO ENTER STANDBY MODE WHEN PIN IS NOT BEING DRIVEN BY SMC

Analog SMS



Desired orientation when placed on board top-side:



Front of system

Circle indicates pin 1 location when placed in correct orientation

C4950-C4952 CAP VALUES WILL BE USED TO GET CUT-OFF FREQUENCY OF ~146HZ

PLACE_NEARs:

C5923.1:PLACE_NEAR=U4900.M10;2.54MM
C5924.1:PLACE_NEAR=U4900.N9;2.54MM
C5925.1:PLACE_NEAR=U4900.K10;2.54MM

DO NOT SYNC WITH K84. REMOVED NO STUFF ON C5923,C5924,C5925. ADDED PLACE NEARS

SYNC_MASTER=K87_MLB SYNC_DATE=02/26/2010

PAGE TITLE: SMS

Apple Inc.

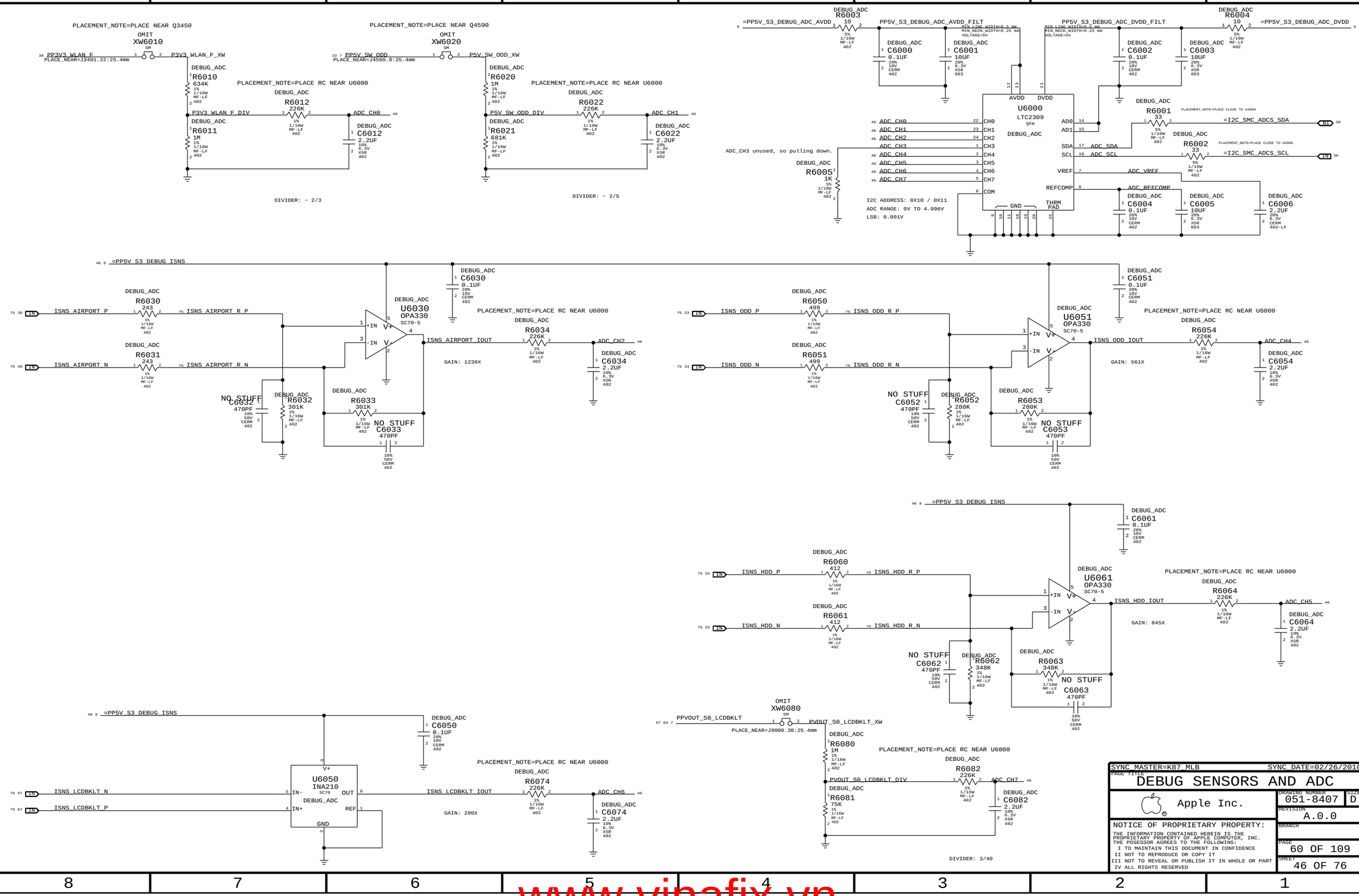
DRAWING NUMBER: 051-8407 SIZE: D

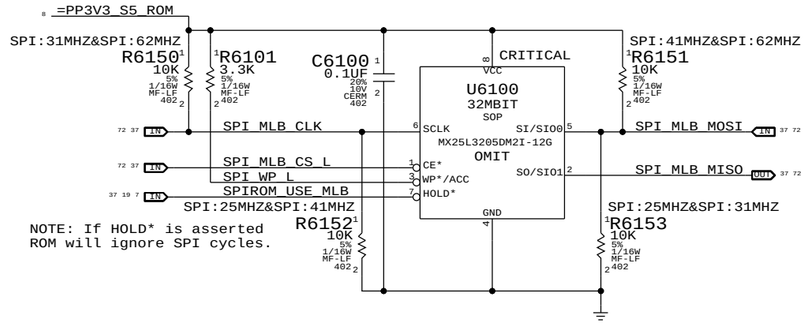
REVISION: A.0.0

BRANCH:

PAGE: 59 OF 109

SHEET: 45 OF 76





MCP89 SPI Frequency Select

Frequency	SPI_MOSI	SPI_CLK
25.0 MHz	0	0
31.2 MHz	0	1
41.7 MHz	1	0
62.5 MHz	1	1

NOTE: 42 & 62 MHz use FAST_READ command.

SYNC_MASTER=K87_MLB SYNC_DATE=02/26/2010

PAGE TITLE: SPI ROM

Apple Inc.

DRAWING NUMBER: 051-8407 SIZE: D

REVISION: A.0.0

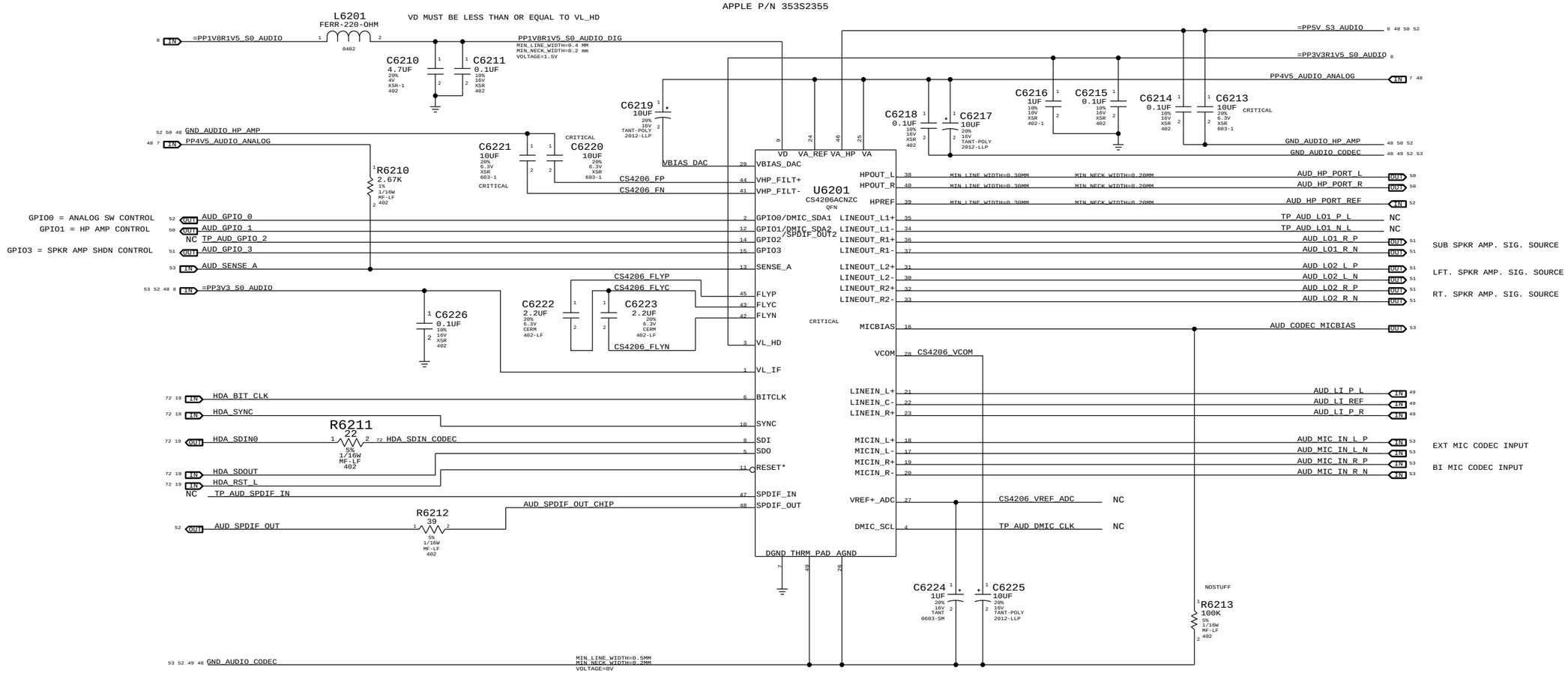
BRANCH:

PAGE: 61 OF 109

SHEET: 47 OF 76

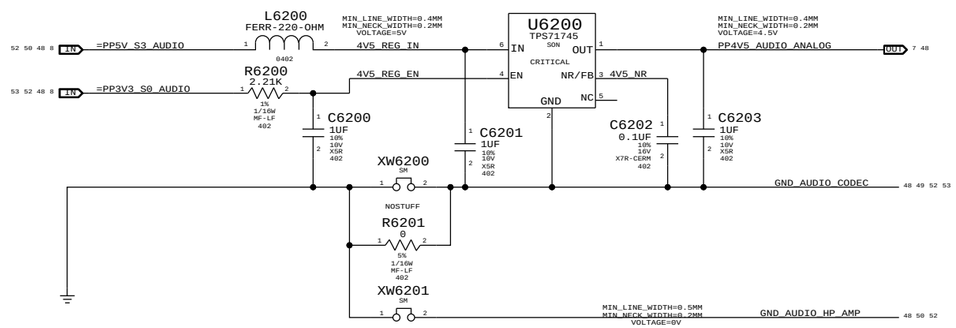
AUDIO CODEC

APPLE P/N 353S2355



4.5V POWER SUPPLY FOR CODEC

APPLE P/N 353S2281



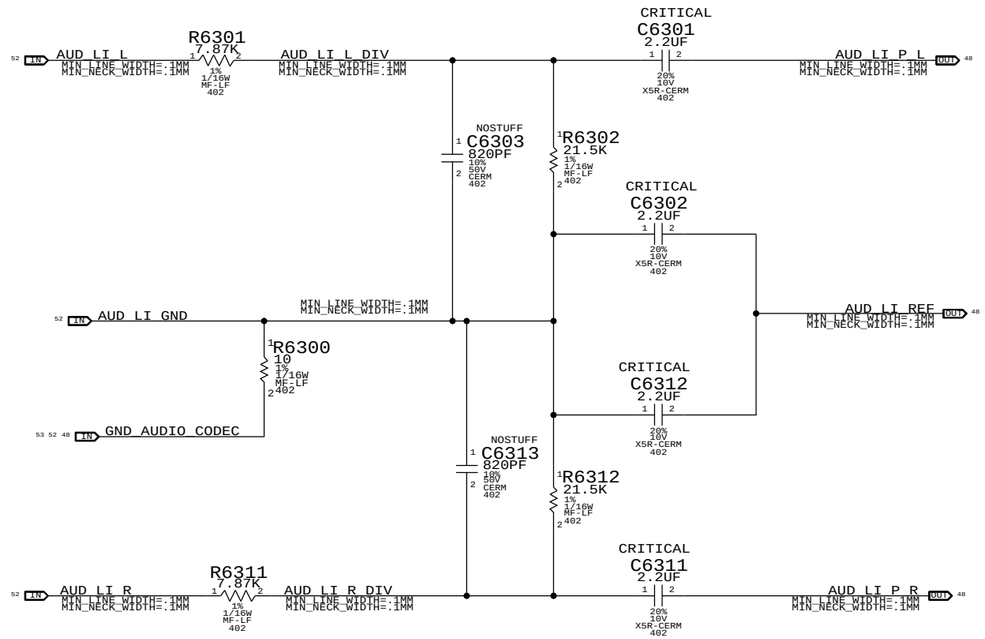
NOTES ON CODEC I/O

DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

SYNC_MASTER=K87_MLB	SYNC_DATE=02/26/2010
PAGE TITLE	AUDIO: CODEC/REGULATOR
Apple Inc.	DRAWING NUMBER 051-8407 SIZE D
	REVISION A.0.0
	BRANCH
	PAGE 62 OF 109
	SHEET 48 OF 76

LINE INPUT VOLTAGE DIVIDER

CODEC RIN = 20K OHMS
NET RIN = 10.36K OHMS (INCLUDING PULL-DOWNS AT ANALOG SWITCH COM PINS)
FC_HP = 3.6 HZ
FC_LP = 43KHZ
VIN = 2VRMS, CODEC VIN = 1.14 VRMS

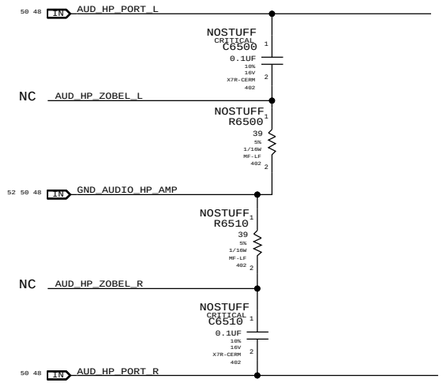


PAGE TITLE
AUDIO: LINE INPUT FILTER

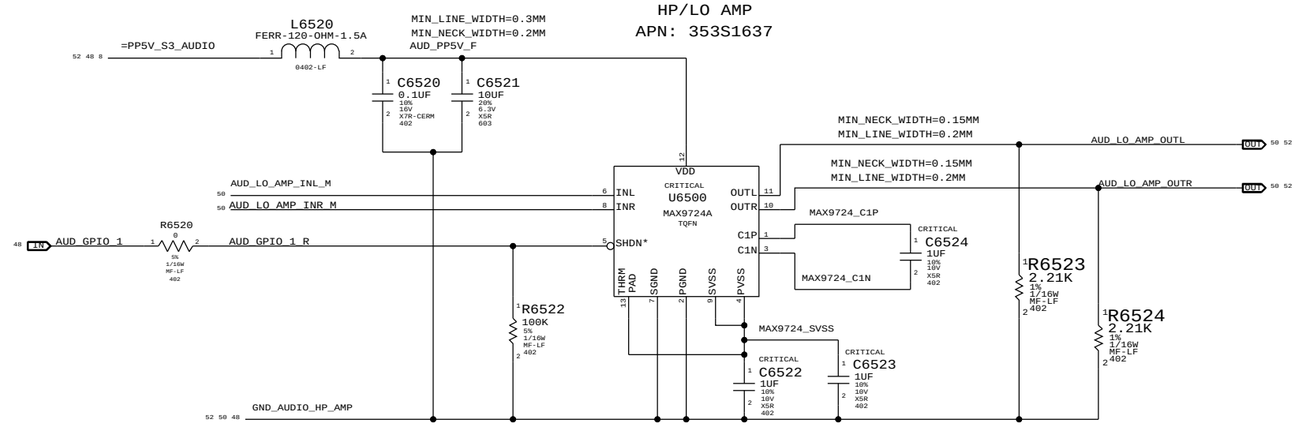
Apple Inc.

DRAWING NUMBER 051-8407 | SIZE D
REVISION A.0.0
BRANCH
PAGE 63 OF 109
SHEET 49 OF 76

CS4206 HP OUTPUT ZOBEL NETWORK

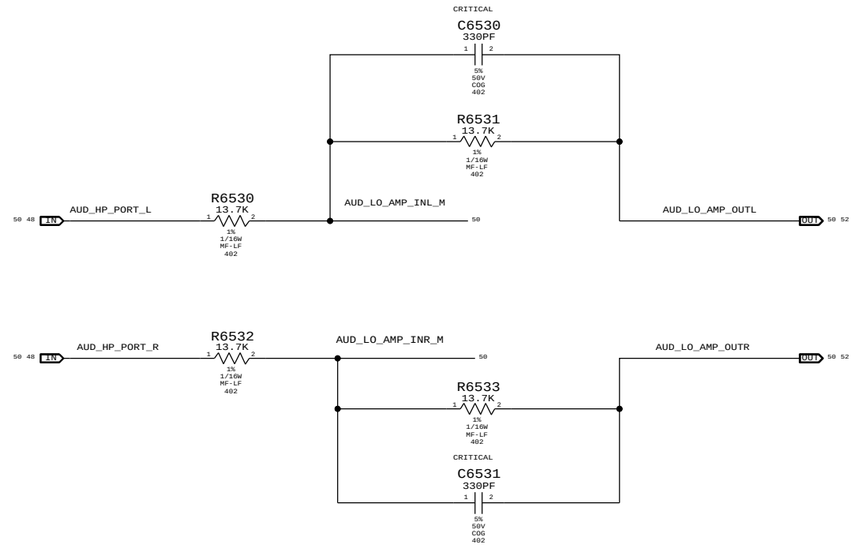


HP/LO AMP
APN: 353S1637



MAX9724 GAIN/FILTER COMPONENTS

AV_PB = -1V/V, FC_LPF = 35.2KHZ



SYNC_MASTER=K87_MLB SYNC_DATE=02/26/2010

PAGE TITLE

AUDIO: HEADPHONE FILTER

Apple Inc.

DRAWING NUMBER 051-8407 SIZE D

REVISION A.0.0

BRANCH

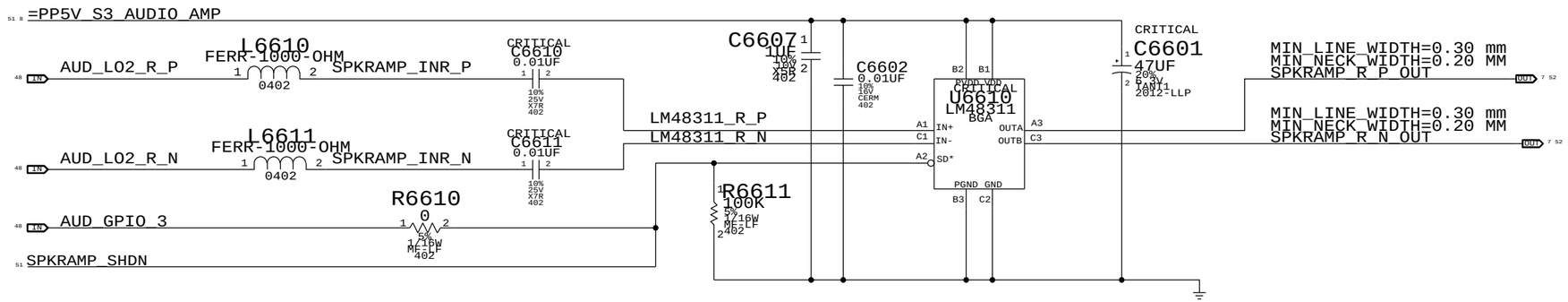
PAGE 65 OF 109

SHEET 50 OF 76

SATELLITE 796Hz < HPF FC < 936Hz
SUB 80 Hz < HPF FC < 94 Hz
GAIN 6DB (2V/V)
SPRK AMP. INPUT REFERRED CLIP POINT = ~-6dBFS

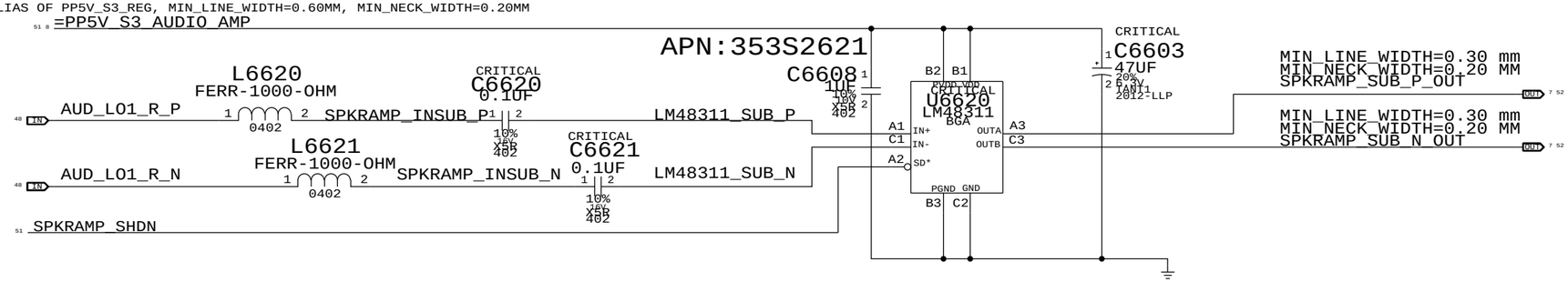
ALIAS OF PP5V_S3_REG, MIN_LINE_WIDTH=0.60MM, MIN_NECK_WIDTH=0.20MM

APN:353S2621



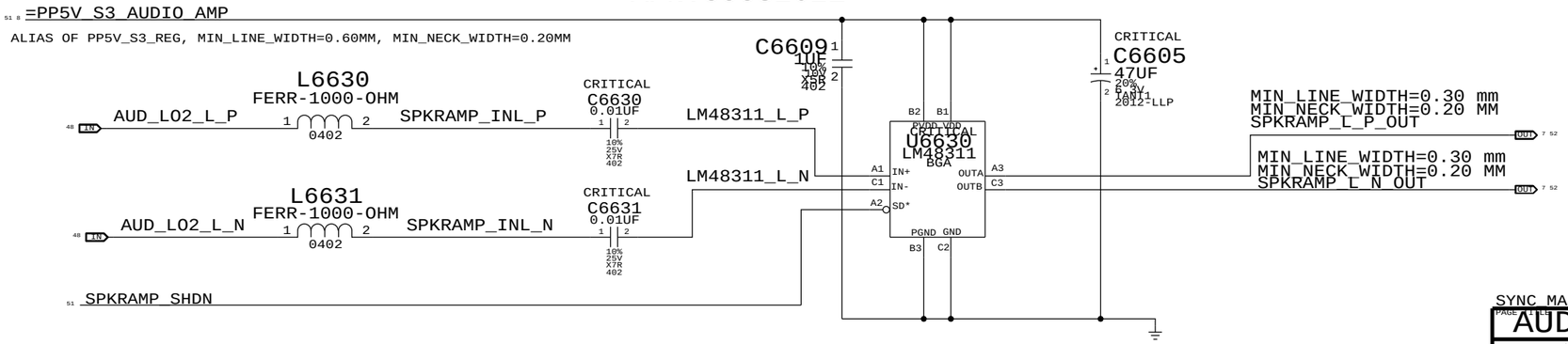
ALIAS OF PP5V_S3_REG, MIN_LINE_WIDTH=0.60MM, MIN_NECK_WIDTH=0.20MM

APN:353S2621



APN:353S2621

ALIAS OF PP5V_S3_REG, MIN_LINE_WIDTH=0.60MM, MIN_NECK_WIDTH=0.20MM



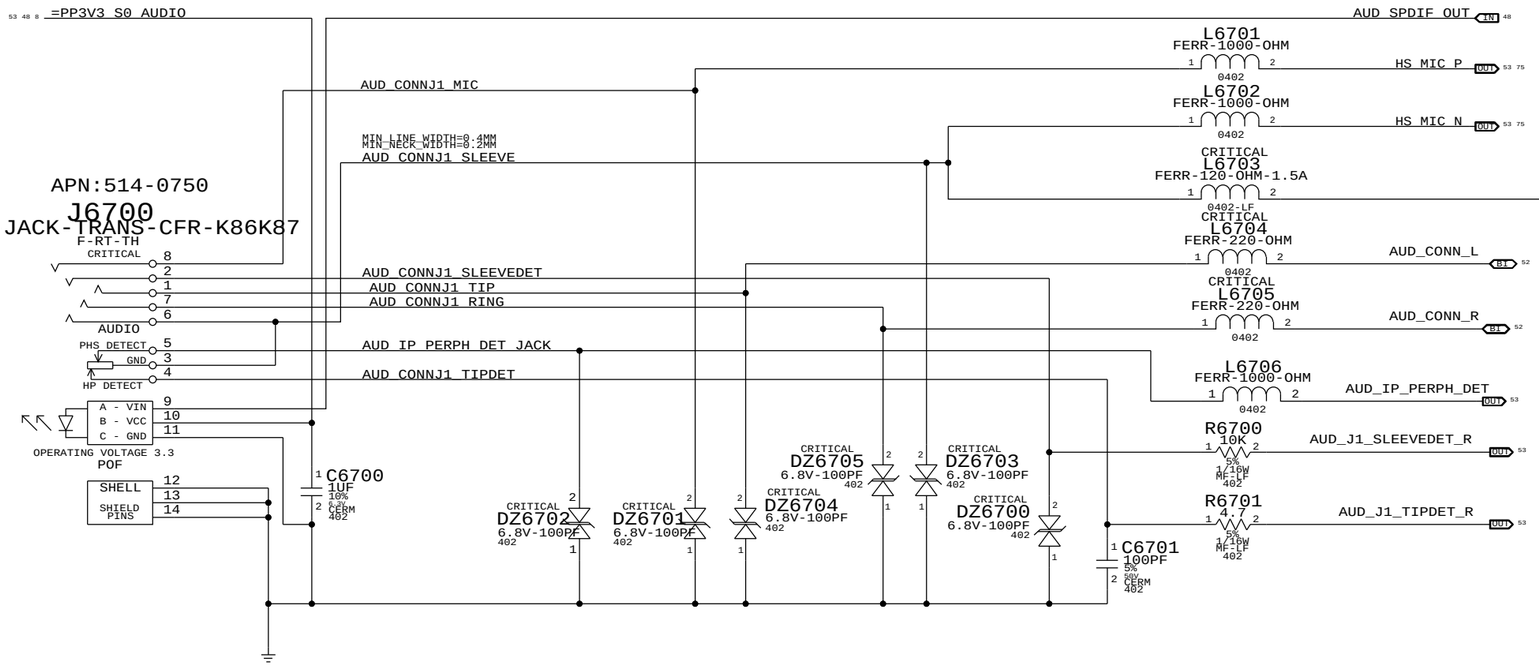
SYNC_MASTER=K87_MLB SYNC_DATE=02/26/2010

PAGE TITLE
AUDIO: SPEAKER AMP

Apple Inc.

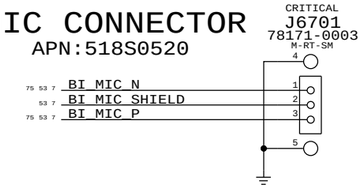
DRAWING NUMBER 051-8407
SIZE D
REVISION A.0.0
BRANCH
PAGE 66 OF 109
SHEET 51 OF 76

AUDIO JACK: LI/LO/HP CONNECTOR, SPDIF TX



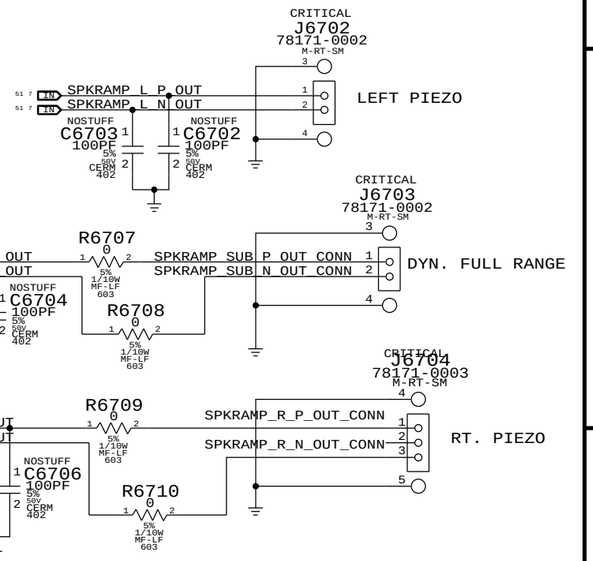
MIC CONNECTOR

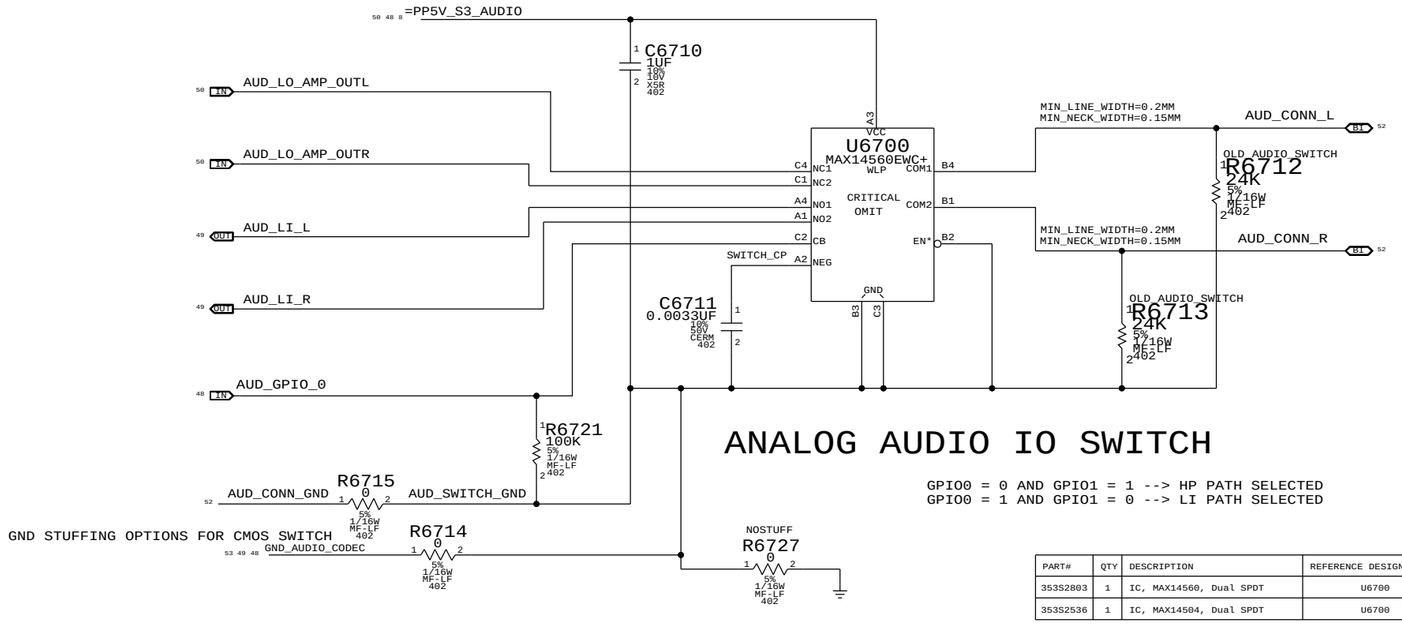
APN:518S0520



SPEAKER CONNECTORS

APN:518S0519





ANALOG AUDIO IO SWITCH

GPIO0 = 0 AND GPIO1 = 1 --> HP PATH SELECTED
GPIO0 = 1 AND GPIO1 = 0 --> LI PATH SELECTED

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S2803	1	IC, MAX14560, Dual SPDT	U6700	CRITICAL	NEW_AUDIO_SWITCH
353S2536	1	IC, MAX14504, Dual SPDT	U6700	CRITICAL	OLD_AUDIO_SWITCH

DO NOT SYNC K84. UPDATED PLACE NEARS

SYNC MASTER=K87 MLB SYNC DATE=02/26/2010

PAGE TITLE: AUDIO: JACK

Apple Inc.

DRAWING NUMBER: 051-8407 | SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 67 OF 109
SHEET: 52 OF 76

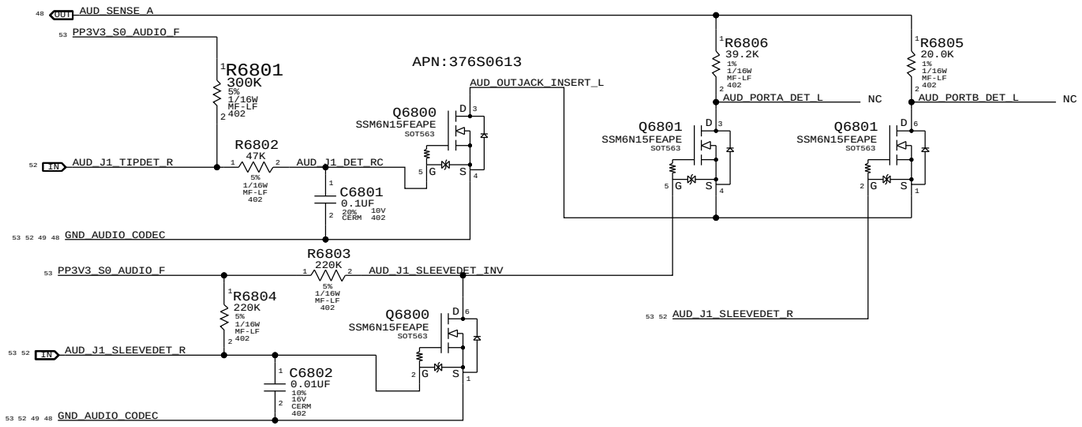
CODEC OUTPUT SIGNAL PATHS

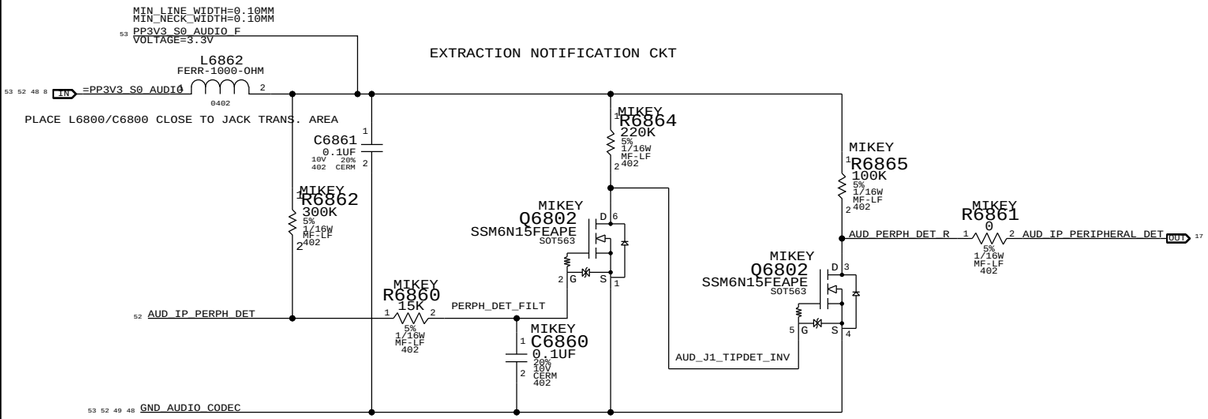
FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X02 (2)	0X02 (2)	0X09 (9,A)	GPIO_0 AND GPIO_1	0X09 (A)
LINE IN	0X05 (5)	0X05 (5)	0X0C (12)	GPIO_0 AND GPIO_1	0X09 (A) AND UI ELEMENT
SATELLITES	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_3	N/A
SUB	0X03 (3)	0X03 (03)	0X0A (10)	GPIO_3	N/A
SPDIF OUT	N/A	0X08 (8)	0X10 (16)	N/A	0X0D (B)

CODEC INPUT SIGNAL PATHS

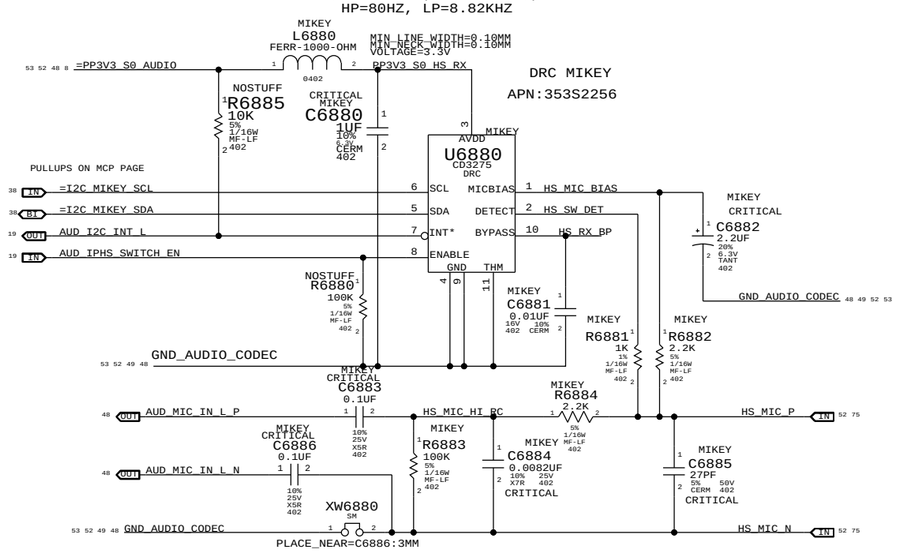
FUNCTION	CONVERTER	PIN COMPLEX	VREF/ENABLE	DET ASSIGNMENT
BUILT-IN MIC	0X06 (6)	0X0D (13,B,RIGHT)	MIC_BIAS (80%)	N/A
HEADSET MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	MCP79 GPIO_38	MCP79 GPIO_17 (PERIPH DETECT) MCP79 GPIO_4 (LOAD DETECT)

PORT A DETECT (HEADPHONES) PORT B DETECT(SPDIF DELEGATE)

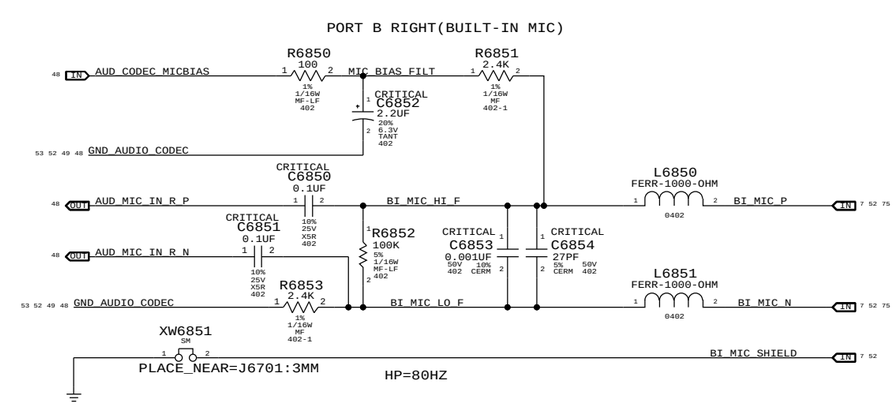




PORT B LEFT(HEADSET MIC)
HP=80HZ, LP=8.82KHZ



PORT B RIGHT(BUILT-IN MIC)



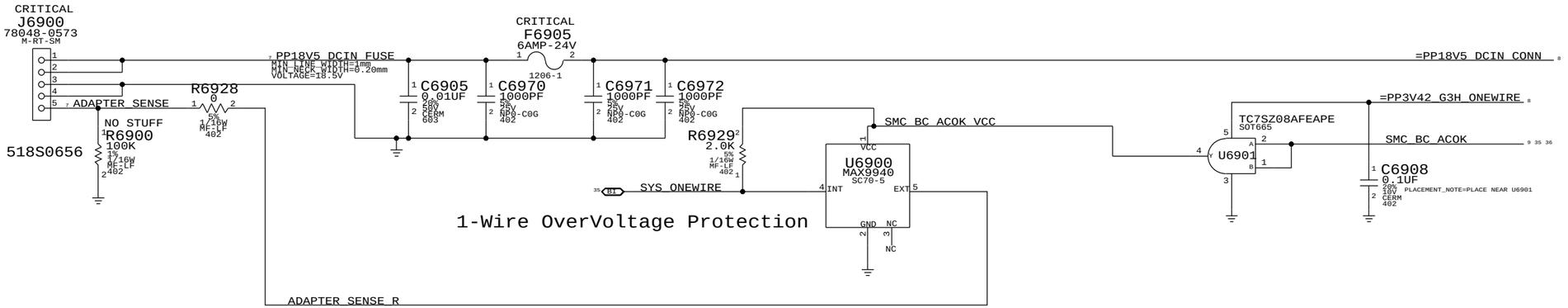
SYNC MASTER=K87 MLB SYNC DATE=02726720106

AUDIO: JACK TRANSLATORS

Apple Inc.

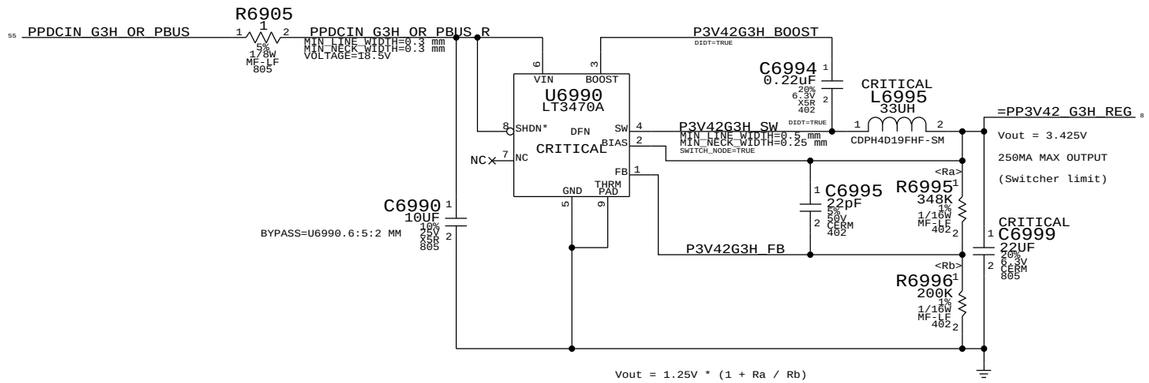
DRAWING NUMBER 051-8407 SIZE D
REVISION A.0.0
BRANCH
PAGE 68 OF 109
SHEET 53 OF 76

MagSafe DC Power Jack



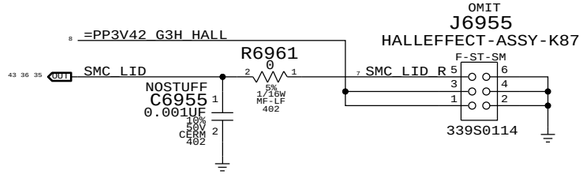
3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator



HALL EFFECT ASSEMBLY

Assembly APN: 339S0114
- BOM: 639-0680
- PCBF: 820-2801
- MCO: 056-3515
- Conn APN:518S0788

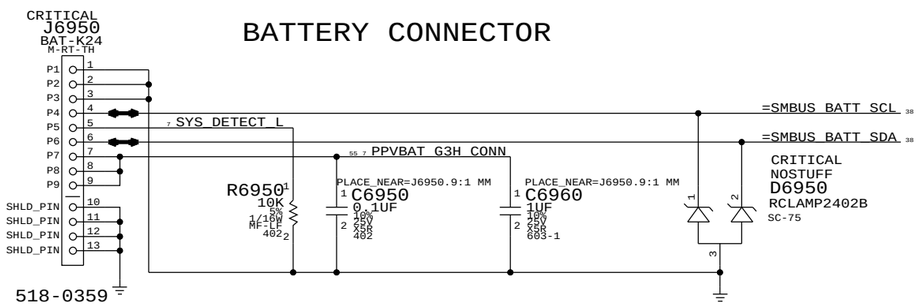


PROTO 0: STUFFING K84 CONNECTOR ONTO MODIFIED K84 PADS
PROTO 1: STUFFING K87 HALL EFFECT ASSEMBLY ONTO K87 PADS

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
607-6831	1	SUB ASSY - HALL EFFECT, K86 K87	J6955	CRITICAL	

PN: 607-6831 for WCPM. PN: 339S0114 for schematic/board layout

BATTERY CONNECTOR



DO NOT SYNC WITH K84. R6900,C6960,SIGNAL NAMES CHANGED. HALL EFFECT CONNECTOR CHANGED.

SYNC_MASTER=K87_MLB SYNC_DATE=02/26/2010

PAGE TITLE: DC-In & Battery Connectors

Apple Inc.

DRAWING NUMBER: 051-8407 SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 69 OF 109
SHEET: 54 OF 76

Reverse-Current Protection

Inrush Limiter

This node is powered through body diodes:
* DCIN through Q7080.
* PBUS through Q7085, Charger TOP FETs and Q7055.

FROM ADAPTER

=PPDCIN_S5_CHGR

Q7080 SI7149DP CRITICAL

PPDCIN_G3H_OR_PBUS
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=18.5V

Q7085 SI7149DP CRITICAL

PPDCIN_G3H_INRUSH
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=18.5V

R7080 100K 5% 1/16W MF-LF 402

C7085 0.1UF 10% 25V X5R 402

R7085 470K 1% 1/16W MF-LF 402

CHGR_SGATE_DIV
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.3 mm

CHGR_AGATE_DIV
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.3 mm

R7081 62K 5% 1/16W MF-LF 402

R7086 332K 1% 1/16W MF-LF 402

CRITICAL
D7005 BAT30CWFILM SOT-323

R7005 20 5% 1/16W MF-LF 402

CHGR_DCIN_D_R

(CHGR_SGATE) MIN_LINE_WIDTH=0.3 mm MIN_NECK_WIDTH=0.3 mm

(CHGR_AGATE) MIN_LINE_WIDTH=0.3 mm MIN_NECK_WIDTH=0.3 mm

(CHGR_DCIN)

ACIN pin threshold is 3.2V, +/- 50mV

Divider sets ACIN threshold at 13.55V

Input impedance of ~40K meets sparkitecture requirements

30mA max load

PP5V1_CHGR_VDD
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.1 mm
VOLTAGE=5.1V

R7001 4.7 5% 1/16W MF-LF 402

PP5V1_CHGR_VDDP
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5.1V

C7001 1UF 10% 10V X5R 402

=PP3V42_G3H_CHGR

R7010 30.1K 1% 1/16W MF-LF 402

C7002 1UF 10% 10V X5R 402

GND_CHGR_AGND

NO STUFF R7002 100K 5% 1/16W MF-LF 402

R7000 0 5% 1/16W MF-LF 402

R7012 1K 1% 1/16W MF-LF 402

SMC_RESET_L

CHGR_RST_L

U7000 ISL6259 TQFN

APN 353S2929

12	VHST	DCIN	2
13	SMB_RST_N	SGATE	26
11	SCL	AGATE	1
10	SDA	CSIP	28
4	VFRQ	CSIN	27
6	CELL	BOOT	25
3	ACIN	UGATE	24
5	ICOMP	PHASE	23
7	VCOMP	LGATE	21
8	VNEG	BGATE	16
18	CSOP	20V/V AMON	9
17	CSON	36V/V BMON	15
29	(AGND) THRM_PAD	(0.8) ACOK	14
22	PGND		

CHGR_DCIN
CHGR_SGATE
CHGR_AGATE
CHGR_CSI_P
CHGR_CSI_N
CHGR_BOOT
CHGR_UGATE
CHGR_PHASE
CHGR_LGATE
CHGR_BGATE
=SMBUS_CHGR_SCL
=SMBUS_CHGR_SDA
CHGR_VFRQ
CHGR_CELL
CHGR_ACIN
CHGR_ICOMP
CHGR_VCOMP
CHGR_VNEG
CHGR_CSO_P
CHGR_CSO_N
CHGR_AMON
CHGR_BMON
=CHGR_ACOK

C7020 0.047UF 10% 10V CERM 402

R7021 10 5% 1/16W MF-LF 402

R7022 10 5% 1/16W MF-LF 402

C7022 0.1UF 10% 25V X5R 402

C7021 0.1UF 10% 25V X5R 402

CRITICAL
R7020 0.02 0.5% 1W MF 0612-1

CHGR_CSI_R_P

CHGR_CSI_R_N

PPDCIN_G3H_CHGR
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=18.5V

CRITICAL C7030 22UF 20% 25V POLY-TANT CASE-D2-SM

CRITICAL C7031 22UF 20% 25V POLY-TANT CASE-D2-SM

C7035 1UF 10% 25V X5R 603-1

C7036 1UF 10% 25V X5R 603-1

C7037 0.001UF 10% 50V X7R 402

PLACE_NEAR=Q7030.5:1.5MM

C7025 0.22UF 10% 10V CERM 402

CRITICAL
Q7030 RJK0332DPB-01 LFPAK-SM

Max Current = 8A

f = 400 kHz

CRITICAL
L7030 4.7UH-9.5A IHLP4040DZ-SM

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
SWITCH_NODE=TRUE
DIDT=TRUE

CRITICAL
F7040 8AMP-24V 1206

TO SYSTEM

=PPBUS_G3H

NO STUFF R7039 180 5% 1/10W MF-LF 603

PPVBAT_G3H_CHGR_REG
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=12.6V

CRITICAL C7040 39UF-0.027OHM 20% 16V POLY B1A-SM

C7045 0.001UF 10% 50V X7R 402

PLACE_NEAR=L7030.2:2MM

CRITICAL
Q7035 RJK0305DPB LFPAK-HF

CHGR_PHASE_RC

NO STUFF C7039 470PF 10% 50V CERM 402

R7050 0.01 0.5% 1W MF 0612-1

PPVBAT_G3H_CHGR_R
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=12.6V

CRITICAL
Q7055 SI7137DP SO-8

TO/FROM BATTERY

PPVBAT_G3H_CONN
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=12.6V

R7051 2.2 5% 1/10W MF-LF 402

R7052 0 5% 1/10W MF-LF 402

CHGR_CSO_R_P

CHGR_CSO_R_N

(PPVBAT_G3H_CHGR_R)

(CHGR_BGATE)

NO STUFF R7013 1K 1% 1/16W MF-LF 402

R7015 56.2K 1% 1/16W MF-LF 402

R7011 9.31K 1% 1/16W MF-LF 402

CHGR_VCOMP_R

C7050 1UF 10% 16V X5R 402

C7015 0.001UF 10% 50V CERM 402

R7016 3.01K 1% 1/16W MF-LF 402

CHGR_VNEG_R

C7016 470PF 10% 50V CERM 402

XW7000 SM

PLACE_NEAR=U7000.29:1mm
PLACE_NEAR=U7000.22:1mm

(GND)

(CHGR_CSO_P)

(CHGR_CSO_N)

(PPVBAT_G3H_CHGR_R)

C7042 0.068UF 10% 10V CERM 402

C7011 0.01UF 10% 16V CERM 402

C7000 1UF 10% 10V X5R 402-1

C7005 0.22UF 20% 25V X5R 603

C7026 0.001UF 10% 50V CERM 402

GND_CHGR_AGND
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0V

* R7051 HAS 2.2OHM TO COMPENSATE UNBALANCED VOLTAGE DUE TO DIFFERENT CURRENT ON _P AND _N. (FROM INTERSIL)

K6 NOTES : L7030 CHANGED BACK TO K24 IND DUE TO LAYOUT
K87 NOTES : R7050 APN 1075007S

SYNC_MASTER=K87_MLB SYNC_DATE=02/26/2010

PAGE TITLE: PBus Supply & Battery Charger

Apple Inc.

DRAWING NUMBER: 051-8407 SIZE: D

REVISION: A.0.0

BRANCH:

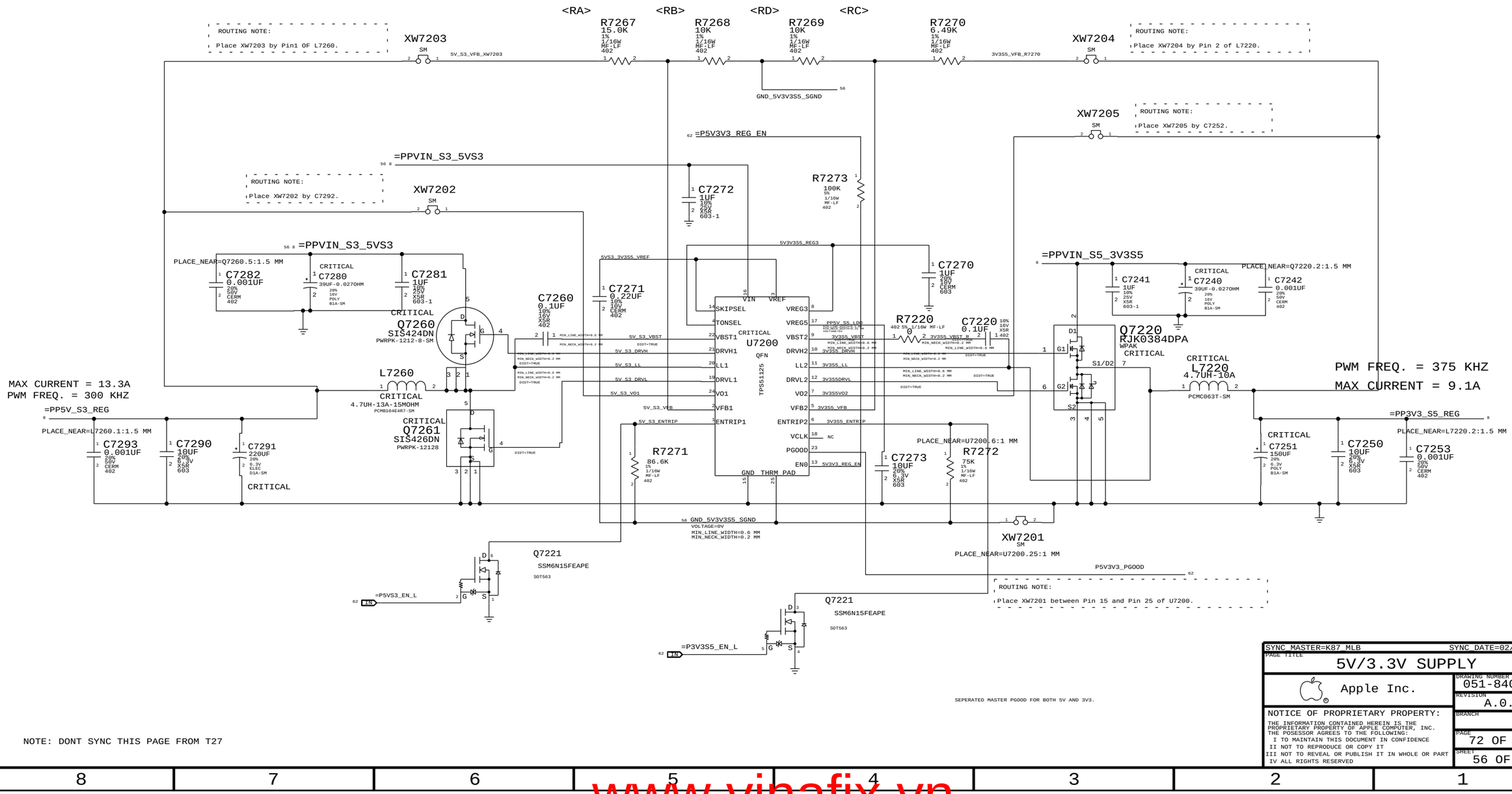
PAGE: 70 OF 109

SHEET: 55 OF 76

5V_S3/3.3V_S5 POWER SUPPLY

VOUT = (2 * RA / RB) + 2

VOUT = (2 * RC / RD) + 2



NOTE: DONT SYNC THIS PAGE FROM T27

SYNC MASTER=K87_MLB SYNC DATE=02/26/2010

PAGE TITLE

5V/3.3V SUPPLY

Apple Inc.

DRAWING NUMBER 051-8407 SIZE D

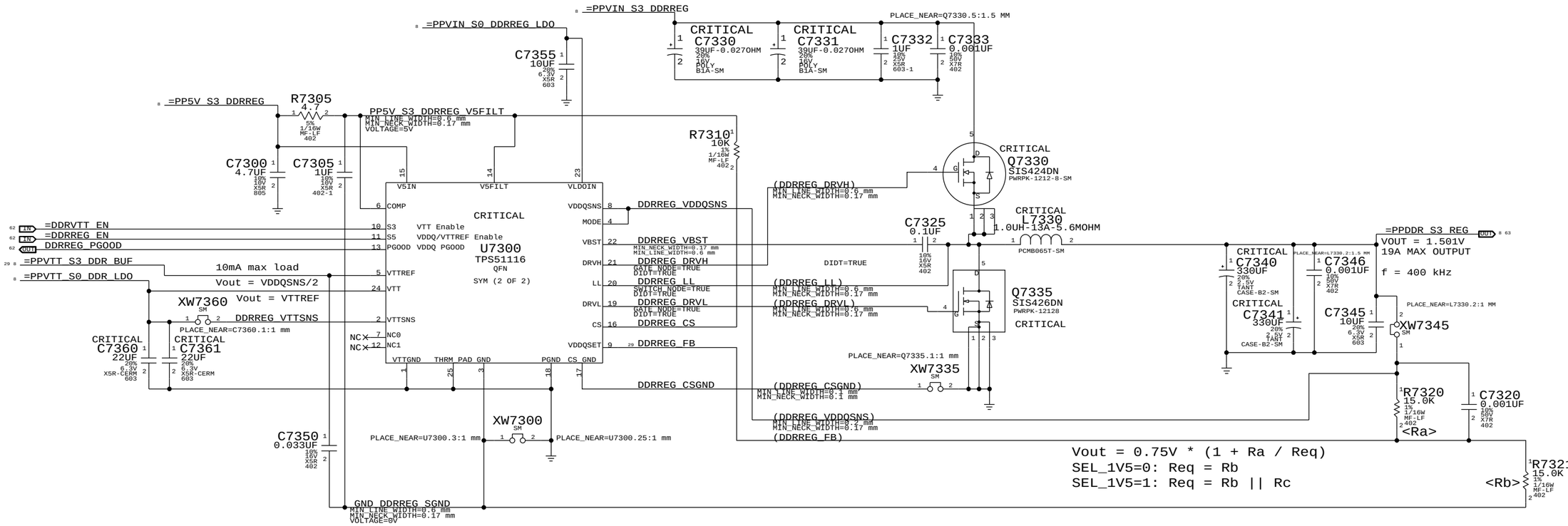
REVISION A.0.0

BRANCH

PAGE 72 OF 109

SHEET 56 OF 76

1.5V/0.75 DDR3 POWER SUPPLY



NOTE: DONT SYNC THIS PAGE FROM T27. C7330 AND C7331 IS CHANGED TO OSCON CAPS
NOTE: DONT SYNC THIS PAGE FROM K6 REMOVED R7380

SYNC_MASTER=K87_MLB SYNC_DATE=02/26/2010

PAGE TITLE: 1.5V/0.75V DDR3 SUPPLY

Apple Inc.

DRAWING NUMBER: 051-8407 SIZE: D

REVISION: A.0.0

BRANCH:

PAGE: 73 OF 109

SHEET: 57 OF 76

IMVP6 CPU VCORE REGULATOR

DPRSLPVR	DPRSTP*	PSI*	OPERATION MODE
0	1	1	2-PHASE CCM
0	1	0	1-PHASE CCM
1	0	1	1-PHASE DCM
1	0	0	1-PHASE DCM

	2PHASE	1PHASE
PWM Freq.	300 kHz	300 kHz
Max Current	44 A	17.6 A
Load Line	-2.107 mV/A	-4 mV/A

IMVP6:1PHASE BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0307	1	RES,MTL FILM,1/16W,8.25K,1,0402,SMD,LF	R7417		IMVP6:1PHASE
114S0336	1	RES,MTL FILM,1/16W, 16.9K, 1,0402,SM,LF	R7416		IMVP6:1PHASE
132S0080	1	CAP,CER, .22UF,20,6.3V,X5R,0402	C7428		IMVP6:1PHASE
114S0236	1	RES,MTL FILM,1/16W,1.58K,1,0402,SMD,LF	R7409		IMVP6:1PHASE
114S0160	1	RES,MTL FILM,1/16W,255 OHM,1,0402,SMD,LF	R7411		IMVP6:1PHASE
132S4720	1	CAP CER 470PF,+/-10%,50V,0402,SMD	C7406		IMVP6:1PHASE
114S0410	1	RES,MTL FILM,1/16W,97.6K,1,0402,SMD,LF	R7414		IMVP6:1PHASE
132S0045	1	CAP,CER,1000PF,50V,10%,X7R,0402,SMD	C7414		IMVP6:1PHASE
131S1027	1	CAP,CER,100PF,5%,50V,CC0402	C7413		IMVP6:1PHASE
132S0099	1	CAP,X5R,0.1UF,10%,16V,0402	C7434		IMVP6:1PHASE

R1100/R1101 **ON THE CPU PAGE** PROTECT THE IMVP6 IF THE CPU IS NOT INSTALLED

NOTE 1: C7432,C7433 = 27.4 OHM FOR VALIDATING CPU ONLY.

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_OCSET	0.25 MM	0.20 MM
IMVP6_VSUM	0.25 MM	0.20 MM
GND_IMVP6_SGND	0.50 MM	0.20 MM
IMVP6_VO	0.25 MM	0.20 MM
IMVP6_DROOP	0.25 MM	0.20 MM
IMVP6_DFB	0.25 MM	0.20 MM
IMVP6_SOFT	0.25 MM	0.20 MM
IMVP6_RBIAS	0.25 MM	0.20 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_VDIFF	0.25 MM	0.20 MM
IMVP6_FB2	0.25 MM	0.20 MM
IMVP6_FB	0.25 MM	0.20 MM
IMVP6_COMP	0.25 MM	0.20 MM
IMVP6_VW	0.25 MM	0.25 MM
IMVP6_VSEN_P	0.25 MM	0.25 MM
IMVP6_VSEN_N	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE1	1.5 MM	0.25 MM
IMVP6_BOOT1	0.25 MM	0.25 MM
IMVP6_UGATE1	1.5 MM	0.25 MM
IMVP6_LGATE1	1.5 MM	0.25 MM
IMVP6_ISEN1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE2	1.5 MM	0.25 MM
IMVP6_BOOT2	0.25 MM	0.25 MM
IMVP6_UGATE2	0.25 MM	0.25 MM
IMVP6_LGATE2	0.25 MM	0.25 MM
IMVP6_ISEN2	0.25 MM	0.25 MM

SYNC_MASTER=K87_MLB SYNC_DATE=02/26/2010

PAGE TITLE: IMVP6 CPU VCore Regulator

Apple Inc.

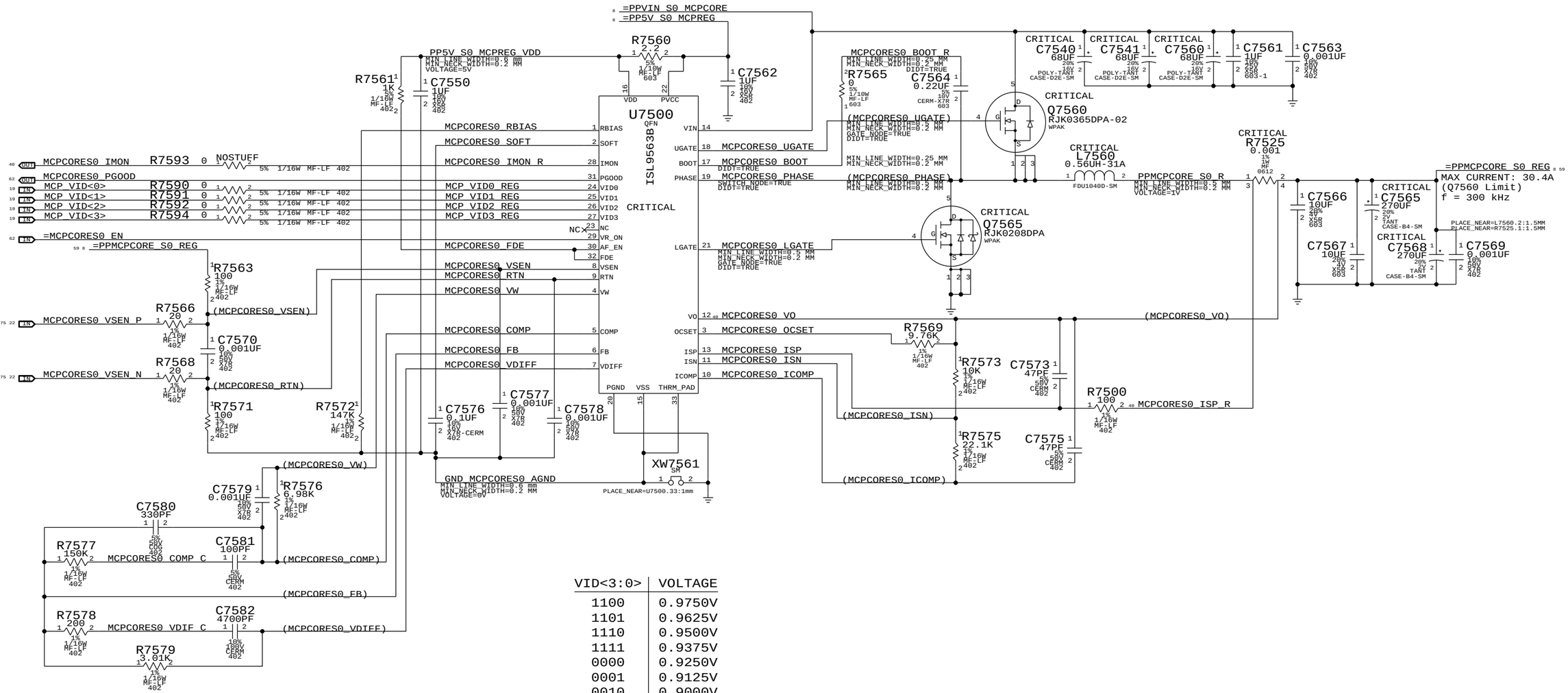
DRAWING NUMBER: 051-8407 SIZE: D

REVISION: A.0.0

BRANCH:

PAGE: 74 OF 109

SHEET: 58 OF 76



VID<3:0>	VOLTAGE
1100	0.9750V
1101	0.9625V
1110	0.9500V
1111	0.9375V
0000	0.9250V
0001	0.9125V
0010	0.9000V
0011	0.8875V
0100	0.8750V
0101	0.8625V
0110	0.8500V
0111	0.8375V
1000	0.8250V
1001	0.8125V
1010	0.8000V
1011	0.7875V

K6 NOTES : XOR AND INVERTER IS REMOVED, CANNOT SYNC THIS PAGE FROM T27

SYNC_MASTER=K87_MLB SYNC_DATE=02/26/2010

PAGE TITLE: MCP VCore Regulator

Apple Inc.

DRAWING NUMBER: 051-8407 SIZE: D

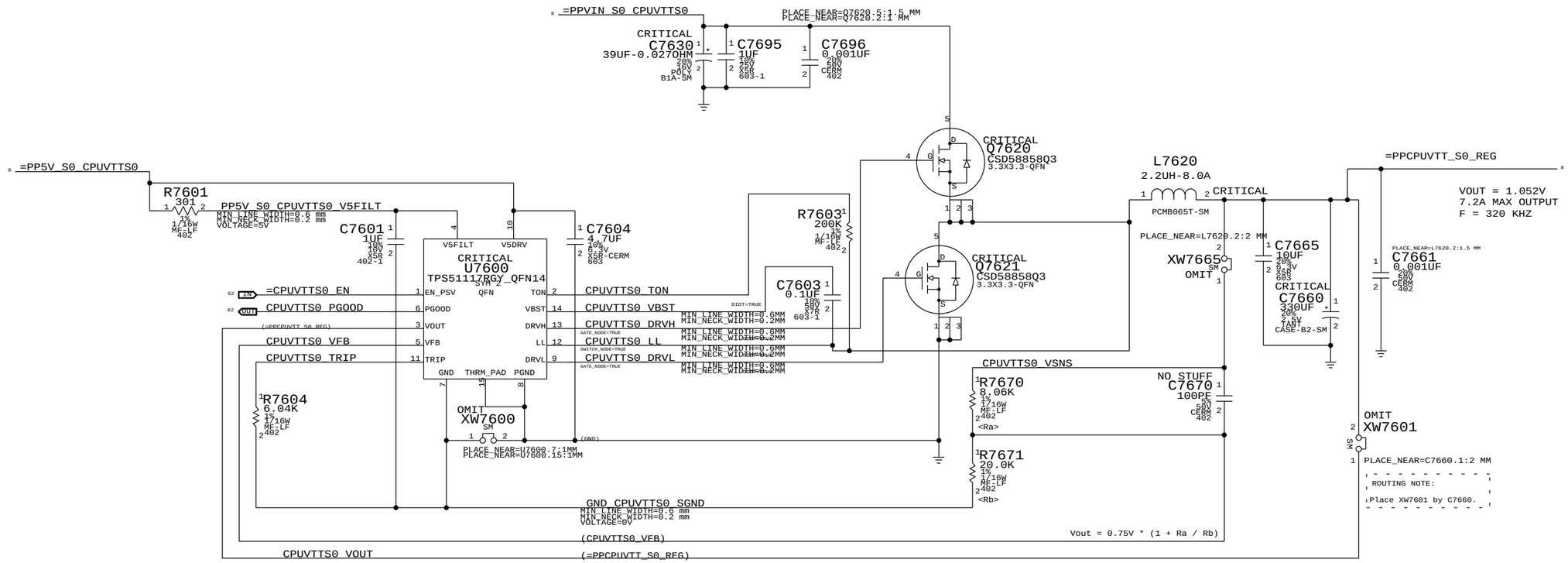
REVISION: A.0.0

BRANCH:

PAGE: 75 OF 109

SHEET: 59 OF 76

CPUVTT POWER SUPPLY



SYNC_MASTER=K87_MLB SYNC_DATE=02/26/2010

PAGE TITLE
CPU VTT(1.05V) SUPPLY

Apple Inc.

DRAWING NUMBER 051-8407 SIZE D

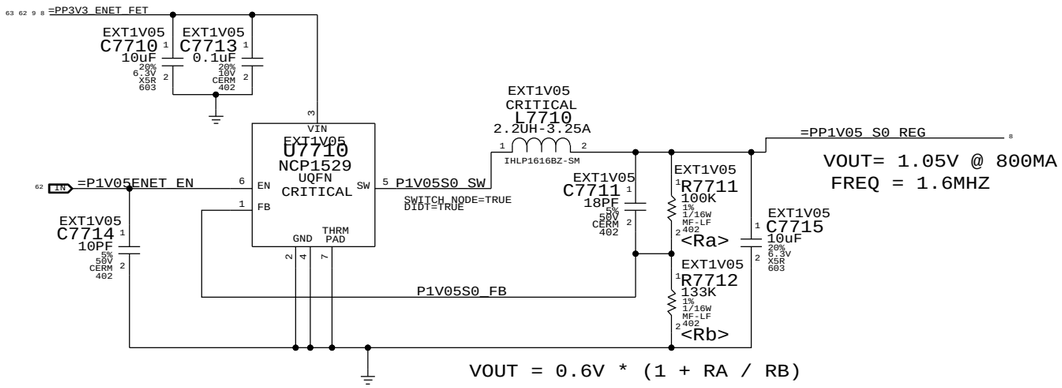
REVISION A.0.0

BRANCH

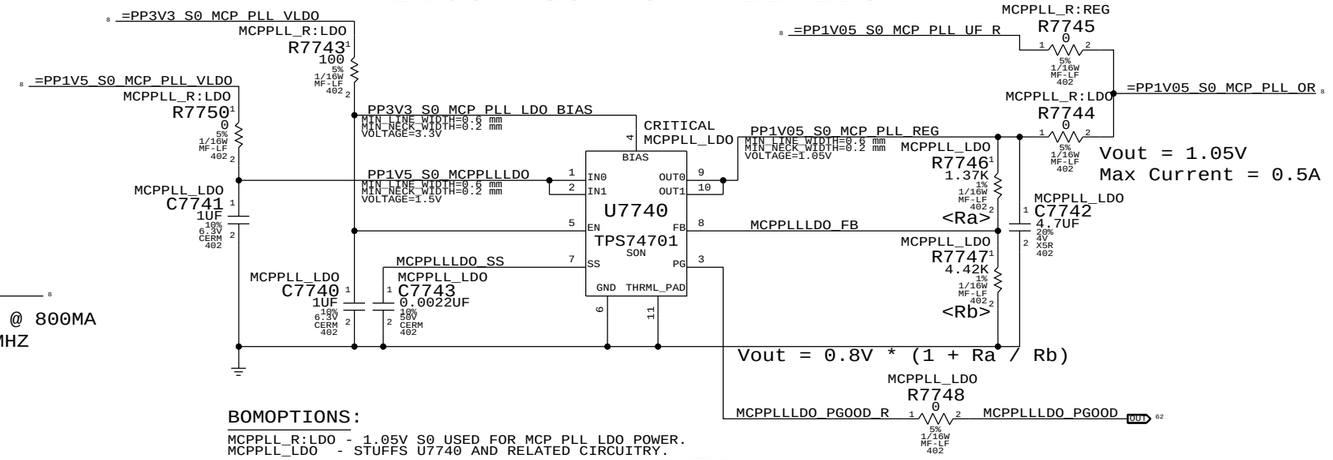
PAGE 76 OF 109

SHEET 60 OF 76

1.05V ENET Switcher



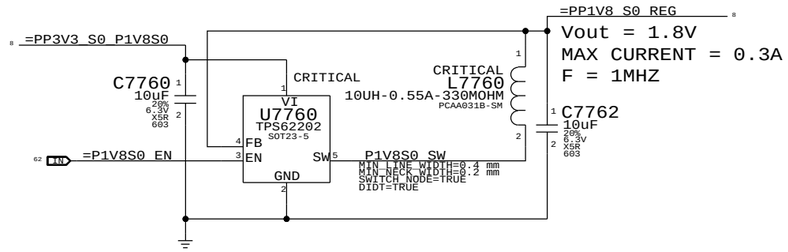
1.05V S0 MCP PLL LDO



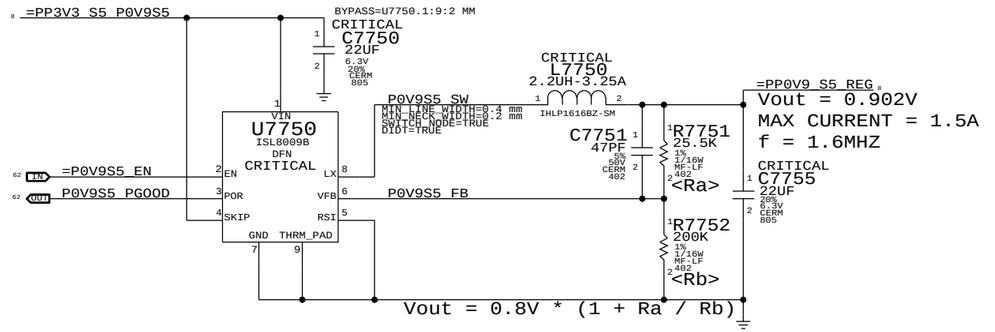
BOMOPTIONS:

MCPPLL_R:LDO - 1.05V S0 USED FOR MCP PLL LDO POWER.
MCPPLL_LDO - STUFFS U7740 AND RELATED CIRCUITRY.
TO USE U7740, MCPPLL_R:LDO AND MCPPLL_LDO MUST BE ACTIVE.
TO USE 1.05V S0, MCPPLL_R:REG MUST BE ACTIVE, MCPPLL_LDO CAN BE ACTIVE, MCPPLL_R:LDO MUST BE INACTIVE.

1.8V S0 Switcher



MCP 0.9V S5 (AUXC) Switcher



K6 NOTES : C7710 AND C7750 HAS BYPASS PROPERTY, SHOULD BE ADDED INCASE THIS PAGE IS SYNC'ED FROM T27

SYNC_MASTER=K87_MLB SYNC_DATE=02/26/2010

PAGE TITLE: Misc Power Supplies

Apple Inc.

DRAWING NUMBER: 051-8407 SIZE: D

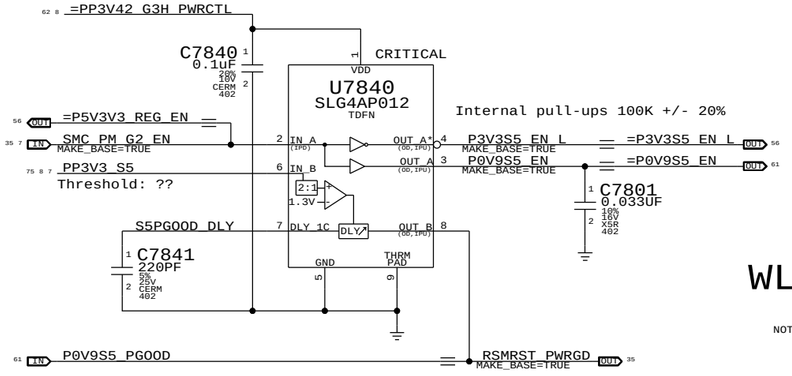
REVISION: A.0.0

BRANCH:

PAGE: 77 OF 109

SHEET: 61 OF 76

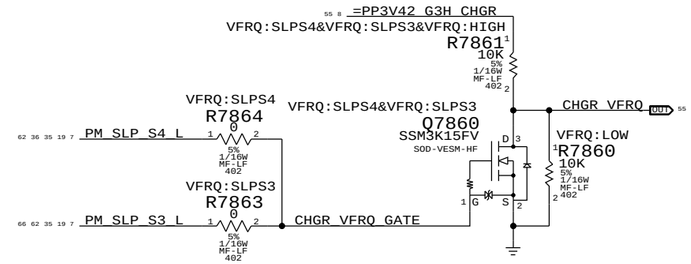
S5 Rail Enables & PGOOD



Power Control Signals

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

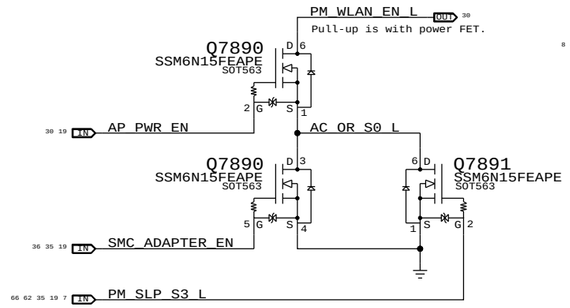
ISL6259 Frequency Select



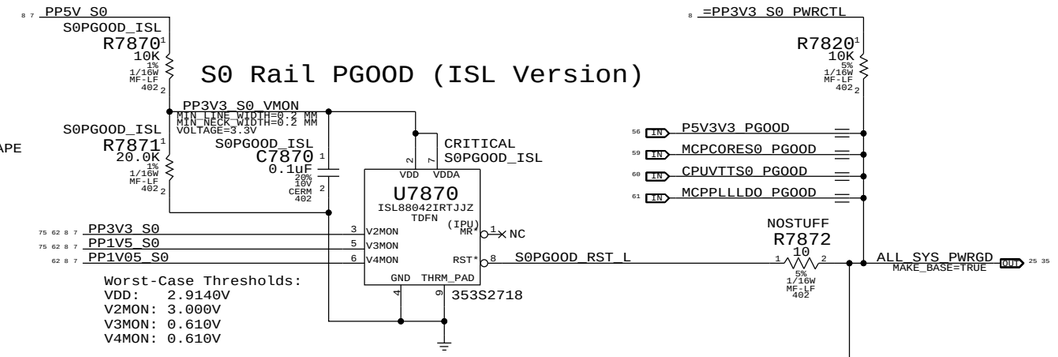
WLAN Enable Generation

"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))

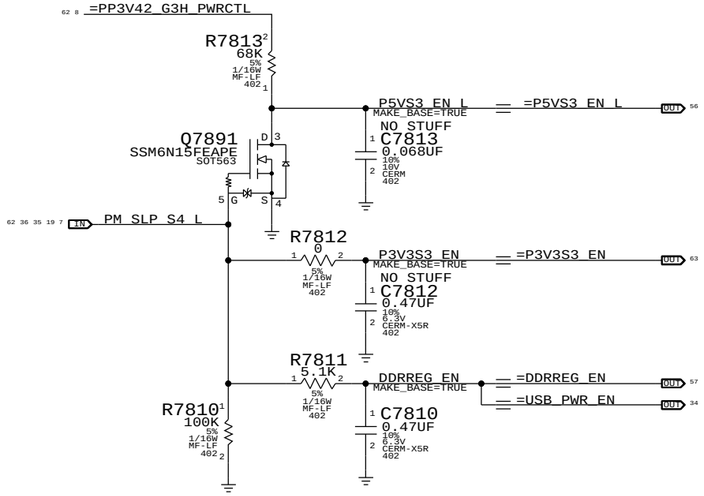
NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.



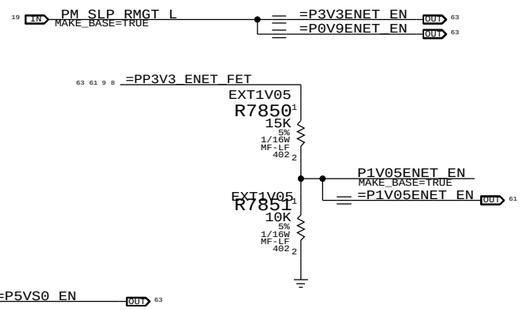
S0 Rail PGOOD Circuitry



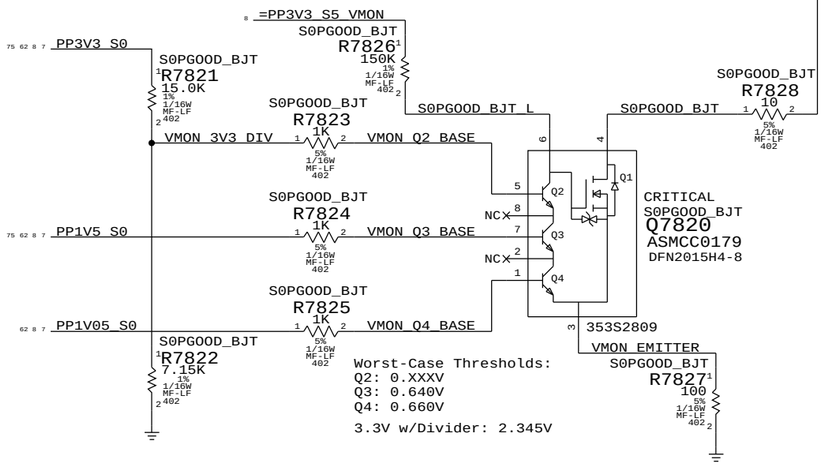
S3 Rail Enables



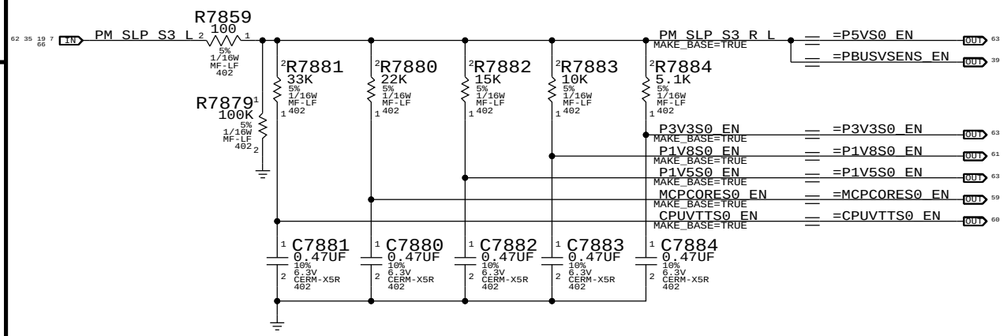
ENET Rail Enables



S0 Rail PGOOD (BJT Version)



S0 Rail Enables



VTT Rail Enable

VTT rail must ramp up in about the same time as MEMVDD rail (Q2300).

DO NOT SYNC T27, ENET RAILS CHANGED

Unused PGOOD signal

SYNC_MASTER=K87_MLB SYNC_DATE=02/26/2010

PAGE TITLE: Power Sequencing

Apple Inc.

DRAWING NUMBER: 051-8407 SIZE: D

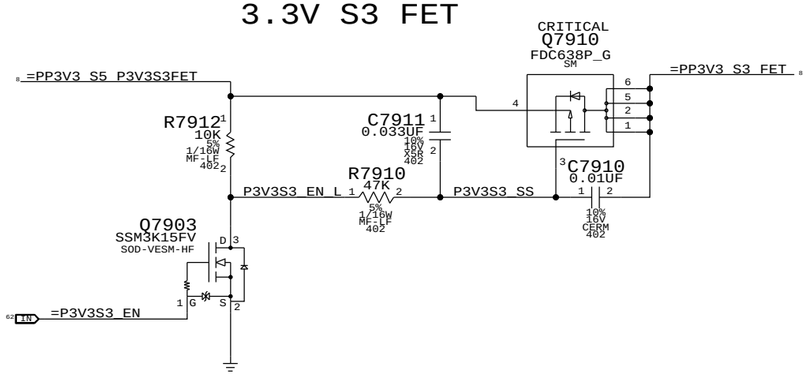
REVISION: A.0.0

BRANCH:

PAGE: 78 OF 109

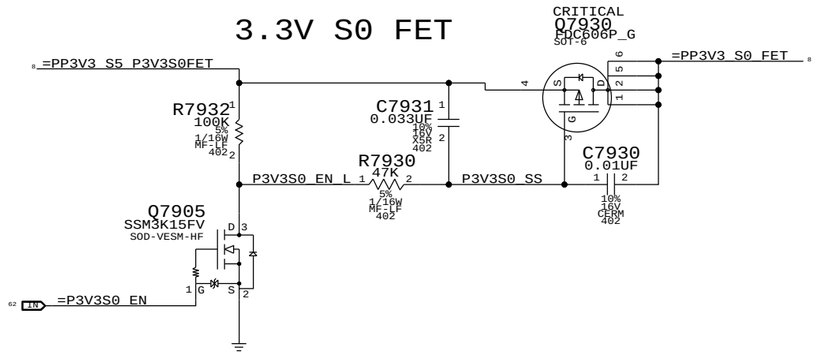
SHEET: 62 OF 76

3.3V S3 FET



3.3V S3 FET	
MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	48 mOhm @4.5V
LOADING	0.811 A (EDP)

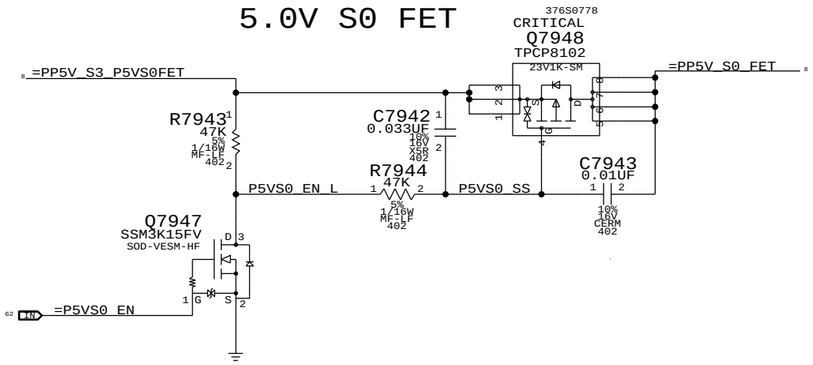
3.3V S0 FET



3.3V S0 FET	
MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 MOHM @4.5V
LOADING	1.240 A (EDP)

(Used to be 5.0V LT S0 FET)

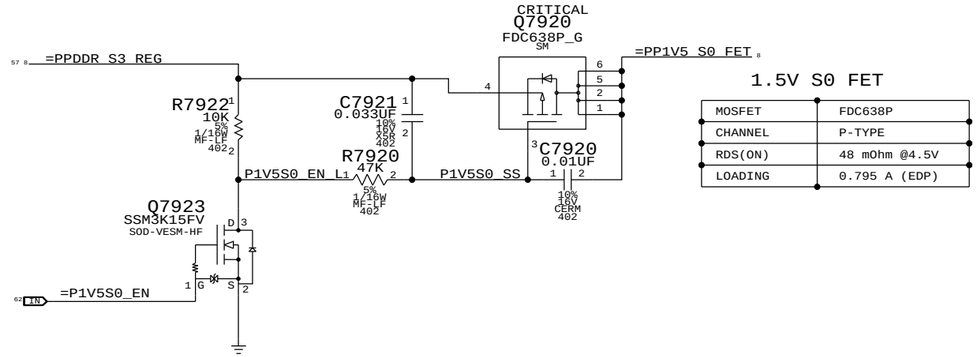
5.0V S0 FET



5.0V LT S0 FET	
MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	13.5 MOHM @4.5V
LOADING	1.569 A (EDP)

DO NOT SYNC FROM K84. ADDED ENET CIRCUITS, REMOVED 1V05 ENET CIRCUIT

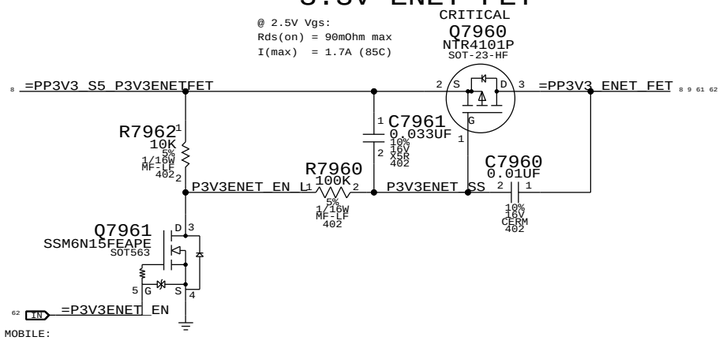
1.5V S0 FET



1.5V S0 FET	
MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	48 mOhm @4.5V
LOADING	0.795 A (EDP)

3.3V ENET FET

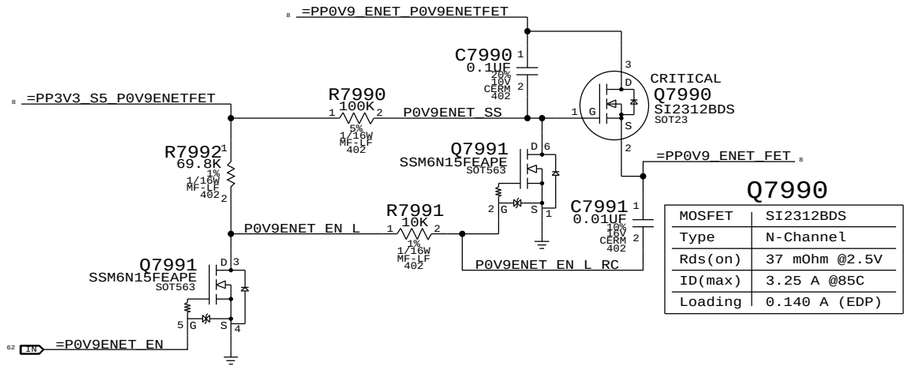
@ 2.5V Vgs:
Rds(on) = 90mOhm max
I(max) = 1.7A (85C)



MOBILE:

Recommend aliasing PM_SLP_RMGT_L and =P3V3ENET_EN. Nets separated on ARB for alternate power options.

0.9V ENET FET



Q7990	
MOSFET	SI2312BDS
Type	N-Channel
Rds(on)	37 mOhm @2.5V
ID(max)	3.25 A @85C
Loading	0.140 A (EDP)

SYNC_MASTER=K87_MLB SYNC_DATE=02/26/2010

PAGE TITLE: POWER FETS

Apple Inc.

DRAWING NUMBER: 051-8407 SIZE: D

REVISION: A.0.0

BRANCH:

PAGE: 79 OF 109

SHEET: 63 OF 76

CHECK IF LVDS_IG_PANEL_PWR GLITCHES ON POWER UP

9 LVDS_IG_PANEL_PWR
R9014 1K 5% 1/16W MF-LF 402
APN 353S2805
CRITICAL U9000 FPF1009 MFET-2X2-8IN
8 =PP3V3_S0_LCD_PANEL
C9009 0.1UF 10% 16V X5R 402
C9011 0.1UF 10% 16V X5R 402
C9012 10UF 20% 6.3V X5R 603
PP3V3_SW_LCD_PANEL
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.30 MM
MIN_NECK_WIDTH=0.20 MM
L9004 FERR-120-OHM-1.5A 0402-LF
C9015 0.001UF 10% 50V X7R 402
C9010 0.001UF 10% 50V X7R 402
PLACE_NEAR=J9000.32:1MM
PLACE_NEAR=L9004.1:1MM
MIN_NECK_WIDTH=0.20 MM
MIN_LINE_WIDTH=0.30 MM
VOLTAGE=3.3V
7 PP3V3_SW_LCD_PANEL_F

CRITICAL L9008 120-OHM-0.3A-EMI 0402-LF
7 PP3V3_S0_LCD_DDC_F
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V
8 =PP3V3_S0_LCD_DDC
(LVDS DDC POWER)
R9008 100K 5% 1/16W MF-LF 402
R9009 100K 5% 1/16W MF-LF 402
9 7 LVDS_IG_DDC_CLK
9 7 LVDS_IG_DDC_DATA

CRITICAL L9080 90-OHM-200MA AMC2012-SN
71 9 LVDS_IG_A_CLK_N
71 9 LVDS_IG_A_CLK_P
75 7 LVDS_IG_A_CLK_F_N
75 7 LVDS_IG_A_CLK_F_P
71 9 7 LVDS_IG_A_DATA_N<0>
71 9 7 LVDS_IG_A_DATA_P<0>
71 9 7 LVDS_IG_A_DATA_N<1>
71 9 7 LVDS_IG_A_DATA_P<1>
71 9 7 LVDS_IG_A_DATA_N<2>
71 9 7 LVDS_IG_A_DATA_P<2>

67 46 7 PPVOUT_S0_LCDBKLT
C9017 1000PF 5% 50V C0G-CERM 603
PLACE_NEAR=J9000.19:1MM
67 7 LED_RETURN_6
67 7 LED_RETURN_5
67 7 LED_RETURN_4
67 7 LED_RETURN_3
67 7 LED_RETURN_2
67 7 LED_RETURN_1

L9050 FERR-120-OHM-1.5A 0402-LF
8 =PP5V_S3_CAMERA
C9016 0.1UF 10% 25V CERM 402
PLACE_NEAR=L9050.2:1MM
7 PP5V_S3_CAMERA_F
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V

CRITICAL J9000 20474-030E-11 F-RT-SM
NC
NC
LVDS I/F
LED BKLT I/F
CAMERA I/F

LCD CONNECTOR

LVDS CONNECTOR:518S0650

FOUR GROUNDING VIAS SHOULD BE DISTRIBUTED ALONG THE GROUND SHAPE THAT BOUND THE CONNECTOR BODY

CAMERA

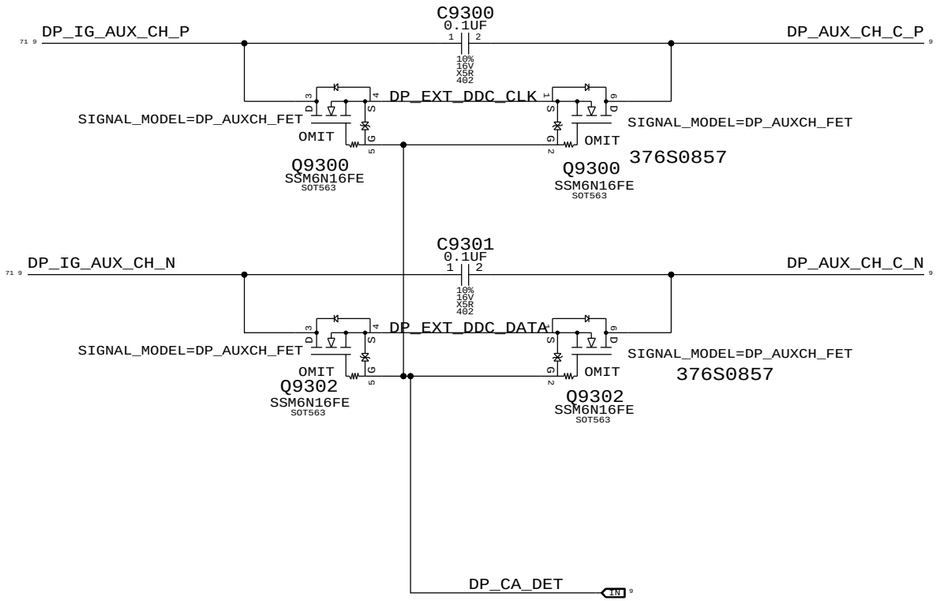
CRITICAL L9060 90-OHM DLP0NS
72 18 OUT USB_CAMERA_P
72 18 OUT USB_CAMERA_N
75 7 USB_CAMERA_CONN_P
75 7 USB_CAMERA_CONN_N
PLACEMENT_NOTE=PLACE CLOSE TO J9000.

SYNC_MASTER=K87_MLB SYNC_DATE=02/26/2010

PAGE TITLE: LVDS CONNECTOR

Apple Inc.

DRAWING NUMBER: 051-8407
SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 90 OF 109
SHEET: 64 OF 76



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
376S0859	2	XSTR,FT,N-CH,DUAL,SOT-563	Q9300,Q9302	CRITICAL	

SYNC_MASTER=K87_MLB SYNC_DATE=02/26/2010

PAGE TITLE
DISPLAYPORT SUPPORT

Apple Inc.

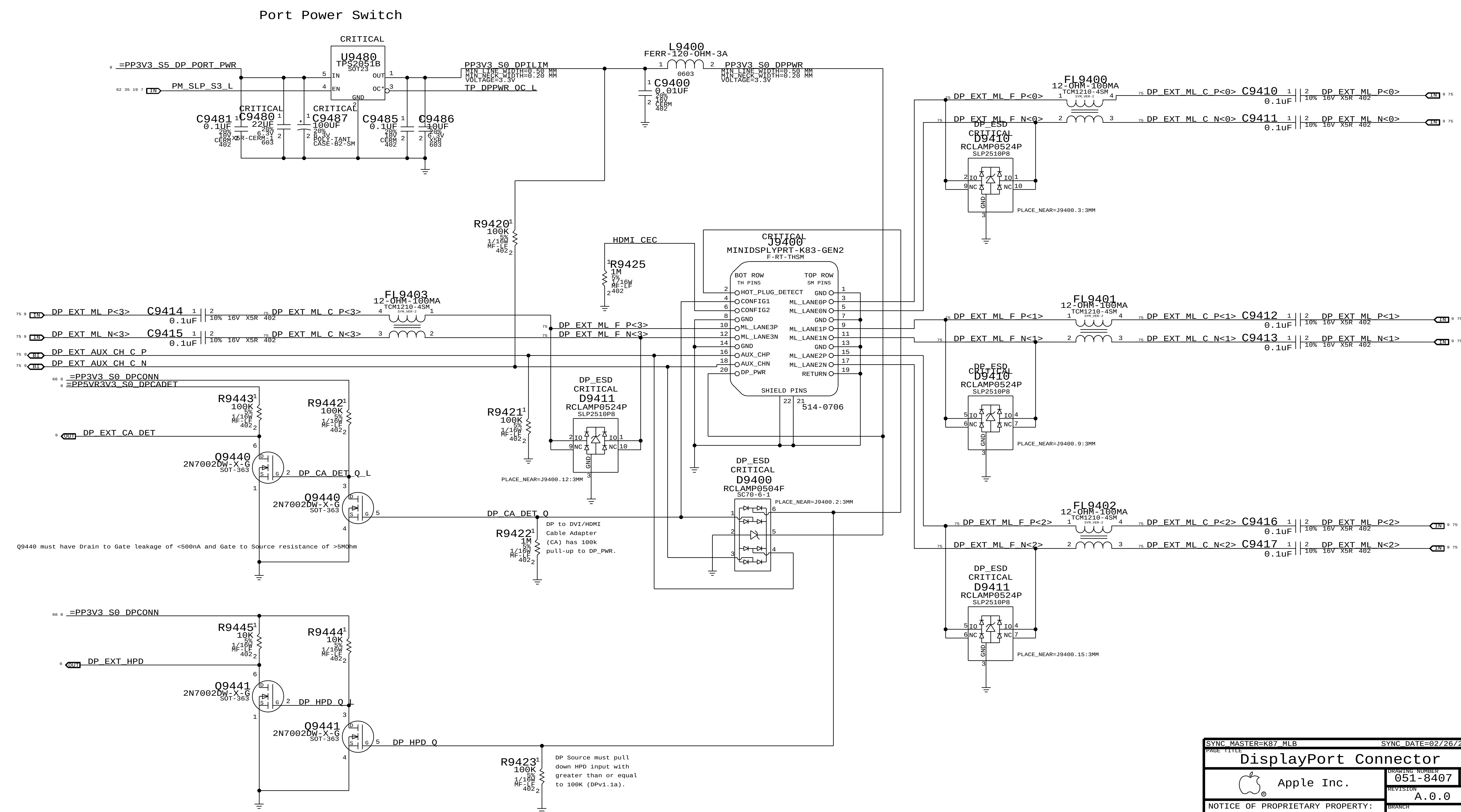
DRAWING NUMBER 051-8407 SIZE D

REVISION A.0.0

BRANCH

PAGE 93 OF 109

SHEET 65 OF 76


Port Power Switch
CRITICAL
U9480
TPS2051B
SOT23
=PP3V3_S5_DP_PORT_PWR
PM_SLP_S3_L
PP3V3_S0_DPILIM
MIN_LINE_WIDTH=0.50 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V
TP_DPPWR_OC_L
L9400
FERR-120-OHM-3A
0603
PP3V3_S0_DPPWR
C9400
0.01UF
C9481
0.1UF
C9480
22UF
C9487
100UF
POLY-TANT
CASE-B2-SM
C9485
0.1UF
C9486
10UF
FL9400
12-OHM-100MA
TCM1210-4SM
DP_EXT_ML_F_P<0>
DP_EXT_ML_F_N<0>
DP_EXT_ML_C_P<0>
DP_EXT_ML_C_N<0>
C9410
C9411
DP_EXT_ML_P<0>
DP_EXT_ML_N<0>
DP_ESD
CRITICAL
D9410
RCLAMP0524P
SLP2510P8
PLACE_NEAR=J9400.3:3MM
R9420
100K
HDMI_CEC
R9425
1M
CRITICAL
J9400
MINIDSPLYPRT-K83-GEN2
F-RT-THSM
BOT ROW
TH PINS
TOP ROW
SM PINS
HOT_PLUG_DETECT
CONFIG1
CONFIG2
GND
ML_LANE3P
ML_LANE3N
AUX_CHP
AUX_CHN
DP_PWR
ML_LANE0P
ML_LANE0N
ML_LANE1P
ML_LANE1N
ML_LANE2P
ML_LANE2N
RETURN
SHIELD PINS
514-0706
DP_EXT_ML_P<3>
DP_EXT_ML_N<3>
C9414
C9415
DP_EXT_ML_C_P<3>
DP_EXT_ML_C_N<3>
FL9403
DP_EXT_ML_F_P<3>
DP_EXT_ML_F_N<3>
DP_EXT_AUX_CH_C_P
DP_EXT_AUX_CH_C_N
=PP3V3_S0_DPCONN
=PP5VR3V3_S0_DPCADET
R9443
100K
R9442
100K
DP_EXT_CA_DET
Q9440
2N7002DW-X-G
SOT-363
DP_CA_DET_Q_L
DP_CA_DET_Q
R9421
100K
D9411
PLACE_NEAR=J9400.12:3MM
DP_ESD
CRITICAL
D9400
RCLAMP0504F
SC70-6-1
PLACE_NEAR=J9400.2:3MM
R9422
1M
DP to DVI/HDMI
Cable Adapter
(CA) has 100k
pull-up to DP_PWR.
Q9440 must have Drain to Gate leakage of <500nA and Gate to Source resistance of >5MOhm
FL9401
DP_EXT_ML_F_P<1>
DP_EXT_ML_F_N<1>
DP_EXT_ML_C_P<1>
DP_EXT_ML_C_N<1>
C9412
C9413
DP_EXT_ML_P<1>
DP_EXT_ML_N<1>
PLACE_NEAR=J9400.9:3MM
FL9402
DP_EXT_ML_F_P<2>
DP_EXT_ML_F_N<2>
DP_EXT_ML_C_P<2>
DP_EXT_ML_C_N<2>
C9416
C9417
DP_EXT_ML_P<2>
DP_EXT_ML_N<2>
PLACE_NEAR=J9400.15:3MM
R9445
10K
R9444
10K
DP_EXT_HPD
Q9441
2N7002DW-X-G
SOT-363
DP_HPD_Q_L
DP_HPD_Q
R9423
100K
DP Source must pull
down HPD input with
greater than or equal
to 100K (DPv1.1a).

DO NOT SYNC. K6 PAGE WITH K84 CONNECTOR

SYNC_MASTER=K87_MLB SYNC_DATE=02/26/2010

PAGE TITLE

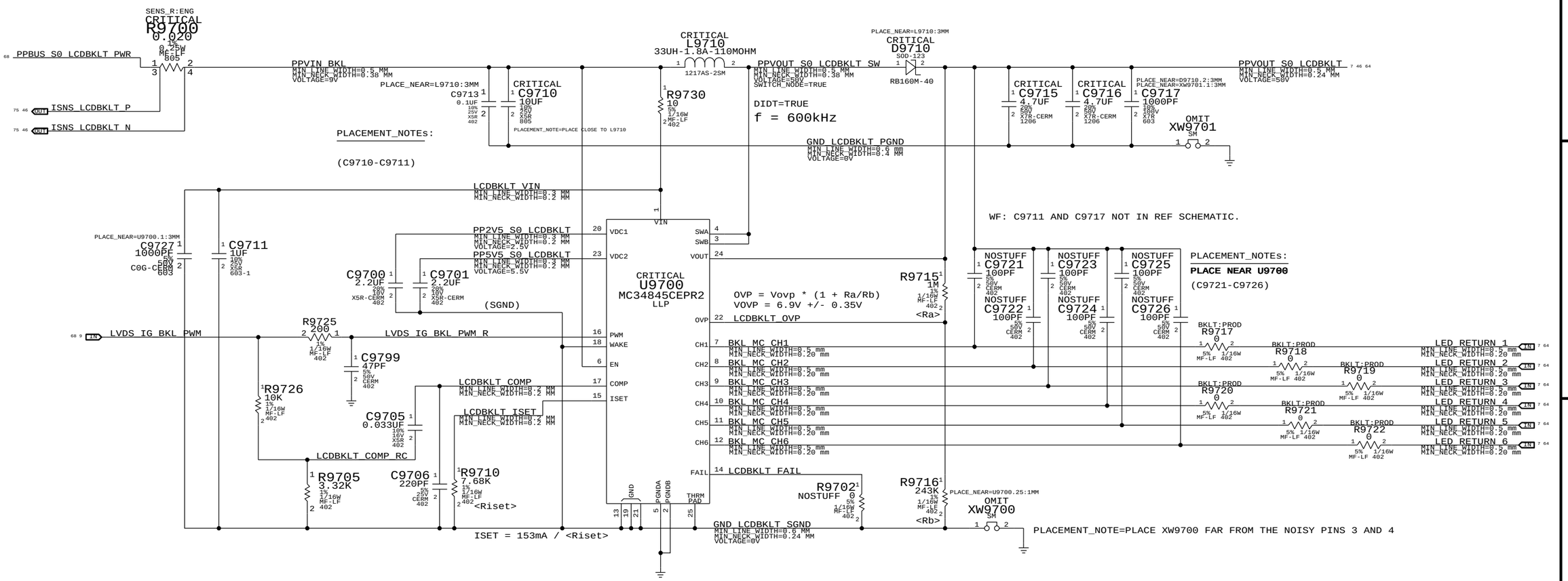
DisplayPort Connector

Apple Inc.

DRAWING NUMBER 051-8407 SIZE D

REVISION A.0.0

BRANCH



13.3 Inch, K84 Panel (9 LEDs per string)

TARGET: ISET = 20mA, OVP = 35V
ACTUAL: ISET = 19.9mA, OVP = 35.2V

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9717,R9718,R9719		BKLT:ENG
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9720,R9721,R9722		BKLT:ENG
101S0075	1	RES,MF,0 OHM,5%,1/8W,SMD,LF,0805	R9700		SENS_R:PROD

10.2 ohm resistors for current measurement on LED strings.

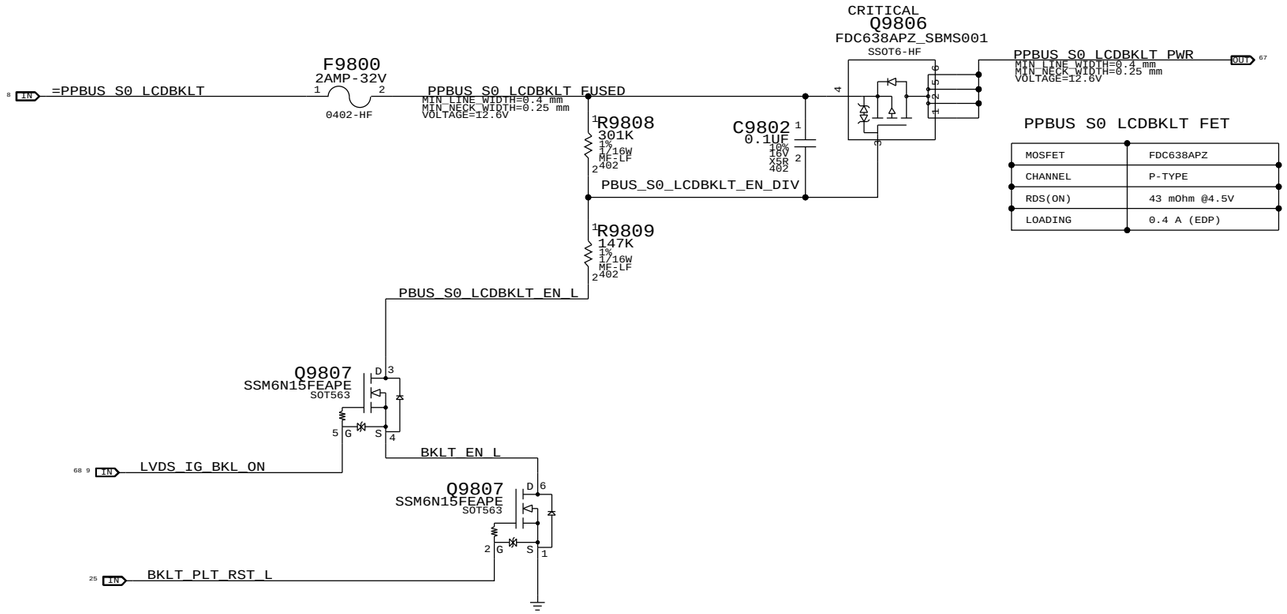
DO NOT SYNC FROM K84. L9710 CHANGED TO K6/K69

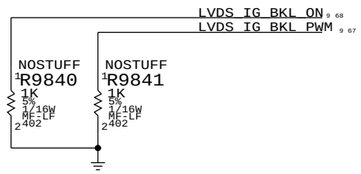
SYNC MASTER=K87_MLB SYNC DATE=02/26/2010

PAGE TITLE
LCD Backlight Driver (MC34845)

Apple Inc.

DRAWING NUMBER 051-8407 SIZE D
REVISION A.0.0
BRANCH
PAGE 97 OF 109
SHEET 67 OF 76





MCP79 HAD INTERNAL 10K PULL-UP FOR THESE SIGNALS
MCP89 DRIVES THEM LOW

SYNC_MASTER=K87_MLB SYNC_DATE=02/26/2010

PAGE TITLE: LCD Backlight Support

Apple Inc.

DRAWING NUMBER: 051-8407 SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 98 OF 109
SHEET: 68 OF 76

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2x_DIELECTRIC	?
FSB_DSTB	*	=3x_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?
FSB_ADSTB	*	=2x_DIELECTRIC	?
FSB_1X	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_DSTB	TOP,BOTTOM	=5x_DIELECTRIC	?
FSB_ADDR	TOP,BOTTOM	=3x_DIELECTRIC	?
FSB_ADSTB	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_1X	TOP,BOTTOM	=3x_DIELECTRIC	?

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.
Signals within each 4x group should be matched within 5 ps of strobe.
DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 135 ps.
Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.

FSB 2X signals / groups shown in signal table on right.
Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 270 ps.
Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

FSB 1X signals shown in signal table on right.

Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.1
SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?

SR DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.1
SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	8 MIL	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.1.4

FSB Clock Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5

CPU / FSB Net Properties

	NET_TYPE		
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB_D_L<15..0> 7 10 14
FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB_DINV_L<0> 7 10 14
FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<0> 7 10 14
FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<0> 7 10 14
FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB_D_L<31..16> 7 10 14
FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB_DINV_L<1> 7 10 14
FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<1> 7 10 14
FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<1> 7 10 14
FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB_D_L<47..32> 7 10 14
FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB_DINV_L<2> 7 10 14
FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<2> 7 10 14
FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<2> 7 10 14
FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB_D_L<63..48> 7 10 14
FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB_DINV_L<3> 7 10 14
FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<3> 7 10 14
FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<3> 7 10 14
FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB_A_L<16..3> 7 10 14
FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB_REQ_L<4..0> 7 10 14
FSB_ADSTB0	FSB_50S	FSB_ADSTB	FSB_ADSTB_L<0> 7 10 14
FSB_ADDR_GROUP1	FSB_50S	FSB_ADDR	FSB_A_L<35..17> 7 10 14
FSB_ADSTB1	FSB_50S	FSB_ADSTB	FSB_ADSTB_L<1> 7 10 14
FSB_1X	FSB_50S	FSB_1X	FSB_ADS_L 7 10 14
FSB_BREQ0_L	FSB_50S	FSB_1X	FSB_BREQ0_L 10 14
FSB_1X	FSB_50S	FSB_1X	FSB_BNR_L 10 14
FSB_1X	FSB_50S	FSB_1X	FSB_BPRI_L 10 14
FSB_1X	FSB_50S	FSB_1X	FSB_DBSY_L 10 14
FSB_1X	FSB_50S	FSB_1X	FSB_DEFER_L 10 14
FSB_1X	FSB_50S	FSB_1X	FSB_DRDY_L 10 14
FSB_1X	FSB_50S	FSB_1X	FSB_HIT_L 7 10 14
FSB_1X	FSB_50S	FSB_1X	FSB_HITM_L 7 10 14
FSB_1X	FSB_50S	FSB_1X	FSB_LOCK_L 7 10 14
FSB_CPURST_L	FSB_50S	FSB_1X	FSB_CPURST_L 10 13 14
FSB_1X	FSB_50S	FSB_1X	FSB_RS_L<2..0> 10 14
FSB_1X	FSB_50S	FSB_1X	FSB_TRDY_L 10 14
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_A20M_L 10 14
CPU_BSEL	CPU_50S	CPU_AGTL	CPU_BSEL<2..0> 9 10
CPU_FERR_L	CPU_50S	CPU_8MIL	CPU_FERR_L 10 14
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_IGNNE_L 10 14
CPU_INIT_L	CPU_50S	CPU_AGTL	CPU_INIT_L 10 14
CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU_INTR 10 14
CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU_NMI 10 14
CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L 10 14 36
CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD 10 13 14
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_SMI_L 10 14
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_STPCLK_L 10 14
PM_THRMTRIP_L	CPU_50S	CPU_8MIL	PM_THRMTRIP_L 10 14 36
FSB_CPUSLP_L	CPU_50S	CPU_AGTL	FSB_CPUSLP_L 10 14
CPU_FROM_SB	CPU_50S	CPU_AGTL	CPU_DPSLP_L 10 14
CPU_DPRSTP_L	CPU_50S	CPU_AGTL	CPU_DPRSTP_L 10 14 58
CPU_ASYNC	CPU_50S	CPU_AGTL	FSB_DPWR_L 10 14
FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P 10 14
FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N 10 14
FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_P 13 14
FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_N 13 14
FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_P 14
FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_N 14
CPU_IERR_L	CPU_50S		CPU_IERR_L 10
PM_DPRSLPVR	CPU_50S	CPU_AGTL	PM_DPRSLPVR 14 58
(See above)	CPU_50S	CPU_AGTL	IMVP_DPRSLPVR 58
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_VDD 14
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_GND 14
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_VCC 14
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_GND 14
CPU_GTLREF	CPU_50S	CPU_GTLREF	CPU_GTLREF 10 29
CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<3> 10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<2> 10
CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<1> 10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<0> 10
XDP_TDI	CPU_50S	CPU_ITP	XDP_TDI 10 13
XDP_TDO	CPU_50S	CPU_ITP	XDP_TDO 10 13
XDP_TMS	CPU_50S	CPU_ITP	XDP_TMS 10 13
XDP_TCK	CPU_50S	CPU_ITP	XDP_TCK 10 13
XDP_TRST_L	CPU_50S	CPU_ITP	XDP_TRST_L 10 13
XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<4..0> 10 13
XDP_BPM_L5	CPU_50S	CPU_ITP	XDP_BPM_L<5> 10 13
(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP_CPURST_L 13
	CPU_50S	CPU_8MIL	CPU_VID<6..0> 11 58
	CPU_50S	CPU_8MIL	IMVP6_VID<6..0>
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P 11 58
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N 11 58
(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P 58
(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N 58

FSB 4X Signal Groups

FSB 2X Signals

FSB 1X Signals

SYNC_MASTER=K87_MLB SYNC_DATE=02/26/2010

PAGE TITLE: CPU/FSB Constraints

Apple Inc.

DRAWING NUMBER: 051-8407 SIZE: D

REVISION: A.0.0

BRANCH:

PAGE: 100 OF 109

SHEET: 69 OF 76

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	
MEM_CLK2MEM	*	=4:1_SPACING	?	NV DG says 3x inner, 4x outer
MEM_CTRL2CTRL	*	=2:1_SPACING	?	NV DG says 2x inner, 4x outer
MEM_CTRL2MEM	*	=2.5:1_SPACING	?	NV DG says 2x inner, 4x outer
MEM_CMD2CMD	*	=1.5:1_SPACING	?	NV DG says 2x inner, 4x outer
MEM_CMD2MEM	*	=3:1_SPACING	?	NV DG says 2x inner, 4x outer
MEM_DATA2DATA	*	=1.5:1_SPACING	?	NV DG says 2x inner, 4x outer
MEM_DATA2MEM	*	=3:1_SPACING	?	NV DG says 2x inner, 4x outer
MEM_DQS2MEM	*	=3:1_SPACING	?	NV DG says 4x inner, 5x outer
MEM_2OTHER	*	25 MIL	?	

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

DDR3:
DQ signals should be matched within 5 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, inter-pair matching shoulw be within 360 ps
No DQS to clock matching requirement.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.
CMD/CTRL signals should be matched within 150 ps.
All memory signals maximum length is 1.030 ps.

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.2.3
SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	=2x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.2.2

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_A_CLK	MEM_70D	MEM_CLK	MEM_A_CLK_P<5..0>	15 26
MEM_A_CLK	MEM_70D	MEM_CLK	MEM_A_CLK_N<5..0>	15 26
MEM_A_CKE	MEM_40S	MEM_CTRL	MEM_A_CKE<3..0>	15 21 26
MEM_A_CNTL	MEM_40S	MEM_CTRL	MEM_A_CS_L<3..0>	15 26
MEM_A_CNTL	MEM_40S	MEM_CTRL	MEM_A_ODT<3..0>	15 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_A<15..0>	15 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_BA<2..0>	15 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_RAS_L	15 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_CAS_L	15 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_WE_L	15 26
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_A_DQ<7..0>	15 28
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_A_DQ<15..8>	15 28
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_A_DQ<23..16>	15 28
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_A_DQ<31..24>	15 28
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_A_DQ<39..32>	15 28
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_A_DQ<47..40>	15 28
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_A_DQ<55..48>	15 28
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_A_DQ<63..56>	15 28
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_A_DM<0>	15 28
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_A_DM<1>	15 28
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_A_DM<2>	15 28
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_A_DM<3>	15 28
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_A_DM<4>	15 28
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_A_DM<5>	15 28
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_A_DM<6>	15 28
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_A_DM<7>	15 28
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM_A_DQS_P<0>	15 28
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM_A_DQS_N<0>	15 28
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM_A_DQS_P<1>	15 28
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM_A_DQS_N<1>	15 28
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM_A_DQS_P<2>	15 28
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM_A_DQS_N<2>	15 28
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM_A_DQS_P<3>	15 28
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM_A_DQS_N<3>	15 28
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM_A_DQS_P<4>	15 28
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM_A_DQS_N<4>	15 28
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM_A_DQS_P<5>	15 28
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM_A_DQS_N<5>	15 28
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM_A_DQS_P<6>	15 28
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM_A_DQS_N<6>	15 28
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM_A_DQS_P<7>	15 28
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM_A_DQS_N<7>	15 28
MEM_B_CLK	MEM_70D	MEM_CLK	MEM_B_CLK_P<5..0>	15 27
MEM_B_CLK	MEM_70D	MEM_CLK	MEM_B_CLK_N<5..0>	15 27
MEM_B_CKE	MEM_40S	MEM_CTRL	MEM_B_CKE<3..0>	15 21 27
MEM_B_CNTL	MEM_40S	MEM_CTRL	MEM_B_CS_L<3..0>	15 27
MEM_B_CNTL	MEM_40S	MEM_CTRL	MEM_B_ODT<3..0>	15 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_A<15..0>	15 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_BA<2..0>	15 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_RAS_L	15 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_CAS_L	15 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_WE_L	15 27
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_B_DQ<7..0>	15 28
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_B_DQ<15..8>	15 28
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_B_DQ<23..16>	15 28
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_B_DQ<31..24>	15 28
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_B_DQ<39..32>	15 28
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_B_DQ<47..40>	15 28
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_B_DQ<55..48>	15 28
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_B_DQ<63..56>	15 28
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_B_DM<0>	15 28
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_B_DM<1>	15 28
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_B_DM<2>	15 28
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_B_DM<3>	15 28
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_B_DM<4>	15 28
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_B_DM<5>	15 28
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_B_DM<6>	15 28
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_B_DM<7>	15 28
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM_B_DQS_P<0>	15 28
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM_B_DQS_N<0>	15 28
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM_B_DQS_P<1>	15 28
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM_B_DQS_N<1>	15 28
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM_B_DQS_P<2>	15 28
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM_B_DQS_N<2>	15 28
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM_B_DQS_P<3>	15 28
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM_B_DQS_N<3>	15 28
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM_B_DQS_P<4>	15 28
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM_B_DQS_N<4>	15 28
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM_B_DQS_P<5>	15 28
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM_B_DQS_N<5>	15 28
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM_B_DQS_P<6>	15 28
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM_B_DQS_N<6>	15 28
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM_B_DQS_P<7>	15 28
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM_B_DQS_N<7>	15 28
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_VDD	15
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_GND	15

SYNC_MASTER=K87_MLB SYNC_DATE=02/26/2010

PAGE TITLE: Memory Constraints

Apple Inc.

DRAWING NUMBER: 051-8407 SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 101 OF 109
SHEET: 70 OF 76

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?
MCP_PEX_COMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.3

NEED PCIe Gen1/Gen2 notes!

Analog Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CRT	*	20 MIL	?
CRT_2CRT	*	15 MIL	?
CRT_2CLK	*	50 MIL	?
CRT_2SWITCHER	*	250 MIL	?
CRT_SYNC	*	=4x_DIELECTRIC	?
MCP_DAC_COMP	*	=2x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRT	CRT	*	CRT_2CRT

CRT signal single-ended impedence varies by location:
- 37.5-ohm from MCP to first termination resistor.
- 50-ohm from first to second termination resistor.
- 75-ohm from output of three-pole filter to connector (if possible).

R/G/B signals should be matched as close as possible and < 10 inches.
SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.4.1.

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_DV_COMP	*	Y	20 MIL	20 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be matched within 100 mils.
NOTE: NV DG recommends 90 ohm differential for LVDS, but cable/display assume 100 ohm.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 100 ps.
DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max trace length: LVDS 10 inches, DP 8.5 inches.
SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.4.2

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=3x_DIELECTRIC	?
SATA_TERMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=4x_DIELECTRIC	?

SATA intra-pair matching should be 1 ps.
Max trace length: 12 inches for SATA Gen1/Gen2, TBD for SATA Gen3.
SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.6

MCP89 Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	PCIE_90D	PCIE	PEG_R2D_P<15..0>	
	PCIE_90D	PCIE	PEG_R2D_N<15..0>	
PEG_R2D	PCIE_90D	PCIE	PEG_R2D_C_P<15..0>	
	PCIE_90D	PCIE	PEG_R2D_C_N<15..0>	
PEG_D2R	PCIE_90D	PCIE	PEG_D2R_P<15..0>	
	PCIE_90D	PCIE	PEG_D2R_N<15..0>	
	PCIE_90D	PCIE	PEG_D2R_C_P<15..0>	
	PCIE_90D	PCIE	PEG_D2R_C_N<15..0>	
	PCIE_90D	PCIE	PCIE_AP_R2D_P	9
	PCIE_90D	PCIE	PCIE_AP_R2D_N	9
PCIE_AP_R2D	PCIE_90D	PCIE	PCIE_AP_R2D_C_P	9 16
	PCIE_90D	PCIE	PCIE_AP_R2D_C_N	9 16
PCIE_AP_D2R	PCIE_90D	PCIE	PCIE_AP_D2R_P	9 16
	PCIE_90D	PCIE	PCIE_AP_D2R_N	9 16
	PCIE_90D	PCIE	PCIE_ENET_R2D_P	
	PCIE_90D	PCIE	PCIE_ENET_R2D_N	
PCIE_ENET_R2D	PCIE_90D	PCIE	PCIE_ENET_R2D_C_P	9 16
	PCIE_90D	PCIE	PCIE_ENET_R2D_C_N	9 16
PCIE_ENET_D2R	PCIE_90D	PCIE	PCIE_ENET_D2R_P	9 16
	PCIE_90D	PCIE	PCIE_ENET_D2R_N	9 16
	PCIE_90D	PCIE	PCIE_ENET_D2R_C_P	
	PCIE_90D	PCIE	PCIE_ENET_D2R_C_N	
	PCIE_90D	PCIE	PCIE_FW_R2D_P	
	PCIE_90D	PCIE	PCIE_FW_R2D_N	
PCIE_FW_R2D	PCIE_90D	PCIE	PCIE_FW_R2D_C_P	9 16
	PCIE_90D	PCIE	PCIE_FW_R2D_C_N	9 16
PCIE_FW_D2R	PCIE_90D	PCIE	PCIE_FW_D2R_P	9 16
	PCIE_90D	PCIE	PCIE_FW_D2R_N	9 16
	PCIE_90D	PCIE	PCIE_FW_D2R_C_P	
	PCIE_90D	PCIE	PCIE_FW_D2R_C_N	
MCP_PE0_REFCLK	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_P	9 16
	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_N	9 16
MCP_PE1_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_AP_P	9 16
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_AP_N	9 16
MCP_PE2_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET_P	9 16
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET_N	9 16
MCP_PE3_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_P	9 16
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_N	9 16
MCP_PEX_CLK_COMP		MCP_PEX_COMP	MCP_PEX0_TERMP	16
CRT_RED	CRT_50S	CRT	CRT_IG_R_C_PR	
CRT_GREEN	CRT_50S	CRT	CRT_IG_G_Y_Y	
CRT_BLUE	CRT_50S	CRT	CRT_IG_B_COMP_PB	
CRT_SYNC	CRT_50S	CRT_SYNC	CRT_IG_HSYNC	
CRT_SYNC	CRT_50S	CRT_SYNC	CRT_IG_VSYNC	
MCP_DAC_RSET		MCP_DAC_COMP	MCP_TV_DAC_RSET	
MCP_DAC_VREF		MCP_DAC_COMP	MCP_TV_DAC_VREF	
TMDS_IG_TXC	DP_90D	DISPLAYPORT	TMDS_IG_TXC_P	
TMDS_IG_TXC	DP_90D	DISPLAYPORT	TMDS_IG_TXC_N	
TMDS_IG_TXD	DP_90D	DISPLAYPORT	TMDS_IG_TXD_P<5..0>	
TMDS_IG_TXD	DP_90D	DISPLAYPORT	TMDS_IG_TXD_N<5..0>	
DP_EXT_ML	DP_90D	DISPLAYPORT	DP_IG_ML_P<3..0>	9
DP_EXT_ML	DP_90D	DISPLAYPORT	DP_IG_ML_N<3..0>	9
DP_EXT_AUX_CH	DP_90D	DISPLAYPORT	DP_IG_AUX_CH_P	9 65
DP_EXT_AUX_CH	DP_90D	DISPLAYPORT	DP_IG_AUX_CH_N	9 65
MCP_TMDS0_RSET	MCP_DV_COMP		MCP_TMDS0_RSET	17 24
MCP_TMDS0_VPROBE			MCP_TMDS0_VPROBE	17 24
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_P	9 64
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_N	9 64
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_P<2..0>	7 9 64
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_N<2..0>	7 9 64
LVDS_IG_A_DATA3	LVDS_100D	LVDS	LVDS_IG_A_DATA_P<3>	
LVDS_IG_A_DATA3	LVDS_100D	LVDS	LVDS_IG_A_DATA_N<3>	
LVDS_IG_B_CLK	LVDS_100D	LVDS	LVDS_IG_B_CLK_P	
LVDS_IG_B_CLK	LVDS_100D	LVDS	LVDS_IG_B_CLK_N	
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS_IG_B_DATA_P<2..0>	
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS_IG_B_DATA_N<2..0>	
LVDS_IG_B_DATA3	LVDS_100D	LVDS	LVDS_IG_B_DATA_P<3>	
LVDS_IG_B_DATA3	LVDS_100D	LVDS	LVDS_IG_B_DATA_N<3>	
MCP_IFPAB_RSET	MCP_DV_COMP		MCP_IFPAB_RSET	17 24
MCP_IFPAB_VPROBE			MCP_IFPAB_VPROBE	17 24
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_C_P	18 33
	SATA_90D	SATA	SATA_HDD_R2D_C_N	18 33
	SATA_90D	SATA	SATA_HDD_R2D_P	7 33
	SATA_90D	SATA	SATA_HDD_R2D_N	7 33
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_P	18 33
	SATA_90D	SATA	SATA_HDD_D2R_N	18 33
	SATA_90D	SATA	SATA_HDD_D2R_C_P	7 33
	SATA_90D	SATA	SATA_HDD_D2R_C_N	7 33
SATA_ODD_R2D	SATA_90D	SATA	SATA_ODD_R2D_C_P	18 33
	SATA_90D	SATA	SATA_ODD_R2D_C_N	18 33
	SATA_90D	SATA	SATA_ODD_R2D_P	7 33
	SATA_90D	SATA	SATA_ODD_R2D_N	7 33
SATA_ODD_D2R	SATA_90D	SATA	SATA_ODD_D2R_P	18 33
	SATA_90D	SATA	SATA_ODD_D2R_N	18 33
	SATA_90D	SATA	SATA_ODD_D2R_C_P	7 33
	SATA_90D	SATA	SATA_ODD_D2R_C_N	7 33
MCP_SATA_TERMP		SATA_TERMP	MCP_SATA_TERMP	18

SYNC_MASTER=K87_MLB SYNC_DATE=02/26/2010

PAGE TITLE: MCP Constraints 1

Apple Inc.

DRAWING NUMBER: 051-8407 SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 102 OF 109
SHEET: 71 OF 76

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	=1.5x_DIELECTRIC	?
CLK_LPC	*	=2x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.7

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.8

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.9

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?
MCP_HDA_COMP	*	8 MIL	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.10

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=1.5x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.11

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	=1.5x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.12

MCP89 Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
LPC_AD	LPC_55S	LPC	LPC AD<3..0> 19 35 37
LPC_FRAME_L	LPC_55S	LPC	LPC FRAME L 19 35 37
LPC_RESET_L	LPC_55S	LPC	LPC RESET L 19 25
MCP_LPC_CLK0	CLK_LPC_55S	CLK_LPC	LPC CLK33M SMC R 19 25
	CLK_LPC_55S	CLK_LPC	LPC CLK33M SMC 25 35
	CLK_LPC_55S	CLK_LPC	LPC CLK33M LPCPLUS 25 37
USB_EXTA	USB_90D	USB	USB EXTA P 18 34
	USB_90D	USB	USB EXTA N 18 34
	USB_90D	USB	USB EXTA MUXED P 34 75
	USB_90D	USB	USB EXTA MUXED N 34 75
USB_MINI	USB_90D	USB	USB MINI P 9 18
	USB_90D	USB	USB MINI N 9 18
USB_EXTD	USB_90D	USB	USB EXTD P 9 18
	USB_90D	USB	USB EXTD N 9 18
USB_CAMERA	USB_90D	USB	USB CAMERA P 18 64
	USB_90D	USB	USB CAMERA N 18 64
USB_BT	USB_90D	USB	USB BT P 18 30
	USB_90D	USB	USB BT N 18 30
USB_TPAD	USB_90D	USB	USB TPAD P 18 43
	USB_90D	USB	USB TPAD N 18 43
USB_IR	USB_90D	USB	USB IR P 9 18
	USB_90D	USB	USB IR N 9 18
USB_EXTB	USB_90D	USB	USB EXTB P 18 34
	USB_90D	USB	USB EXTB N 18 34
USB_T57	USB_90D	USB	USB T57 P 9 18
	USB_90D	USB	USB T57 N 9 18
USB_EXTC	USB_90D	USB	USB EXTC P 9 18
	USB_90D	USB	USB EXTC N 9 18
USB_SDCARD	USB_90D	USB	USB SDCARD P 9 18
	USB_90D	USB	USB SDCARD N 9 18
USB_WM	USB_90D	USB	USB WM P 9 18
	USB_90D	USB	USB WM N 9 18
MCP_USB_RBIAS	MCP_USB_RBIAS		MCP USB RBIAS GND 18
SMBUS_MCP_0_CLK	SMB_55S	SMB	SMBUS MCP 0 CLK 13 19 38
SMBUS_MCP_0_DATA	SMB_55S	SMB	SMBUS MCP 0 DATA 13 19 38
(SMBUS_SMC_MGMT_SCL)	SMB_55S	SMB	SMBUS MCP 1 CLK 19 38
(SMBUS_SMC_MGMT_SDA)	SMB_55S	SMB	SMBUS MCP 1 DATA 19 38
HDA_BIT_CLK	HDA_55S	HDA	HDA BIT CLK 19 48
	HDA_55S	HDA	HDA BIT CLK R 19
HDA_SYNC	HDA_55S	HDA	HDA SYNC 19 48
	HDA_55S	HDA	HDA SYNC R 19
HDA_RST_L	HDA_55S	HDA	HDA RST R L 19
	HDA_55S	HDA	HDA RST L 19 48
HDA_SDIN0	HDA_55S	HDA	HDA SDIN0 19 48
	HDA_55S	HDA	HDA SDIN CODEC 48
HDA_SDOUT	HDA_55S	HDA	HDA SDOUT 19 48
	HDA_55S	HDA	HDA SDOUT R 19
MCP_HDA_PULLDN_COMP		MCP_HDA_COMP	MCP HDA PULLDN COMP 19
MCP_SUS_CLK	CLK_SLOW_55S	CLK_SLOW	PM CLK32K SUSCLK R 19 25
	CLK_SLOW_55S	CLK_SLOW	PM CLK32K SUSCLK 25 35
SPI_CLK	SPI_55S	SPI	SPI CLK R 19 37
	SPI_55S	SPI	SPI CLK 7 37
SPI_MOSI	SPI_55S	SPI	SPI MOSI R 19 37
	SPI_55S	SPI	SPI MOSI 7 37
SPI_MISO	SPI_55S	SPI	SPI MISO 7 19 37
SPI_CS0	SPI_55S	SPI	SPI CS0 R L 19 37
	SPI_55S	SPI	SPI CS0 L 7 37
	SPI_55S	SPI	SPI MLB CLK 37 47
	SPI_55S	SPI	SPI MLB MOSI 37 47
	SPI_55S	SPI	SPI MLB MISO 37 47
	SPI_55S	SPI	SPI MLB CS L 37 47
	SPI_55S	SPI	SPI ALT CLK 37
	SPI_55S	SPI	SPI ALT MOSI 37
	SPI_55S	SPI	SPI ALT MISO 37
	SPI_55S	SPI	SPI ALT CS L 37

SYNC_MASTER=K87_MLB SYNC_DATE=02/26/2010

PAGE TITLE: MCP Constraints 2

Apple Inc.

DRAWING NUMBER: 051-8407 SIZE: D

REVISION: A.0.0

BRANCH:

PAGE: 103 OF 109

SHEET: 72 OF 76

MCP RGMII (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MII_COMP	*	=STANDARD	7.5 MIL	7.5 MIL	=STANDARD	=STANDARD	=STANDARD
ENET_MII_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	12 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4

88E1116R (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_MDI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_VDD	18
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_GND	18
MCP_CLK25M_BUF0	ENET_MII_55S	MCP_BUF0_CLK	MCP_CLK25M_BUF0_R	9 31
	ENET_MII_55S	MCP_BUF0_CLK	RTL8211_CLK25M_CKXTAL1	31
ENET_INTR_L	ENET_MII_55S	ENET_MII	ENET_INTR_L	
ENET_MDIO	ENET_MII_55S	ENET_MII	ENET_MDIO	18 31
ENET_MDC	ENET_MII_55S	ENET_MII	ENET_MDC	9 31
ENET_PWRDWN_L	ENET_MII_55S	ENET_MII	ENET_PWRDWN_L	
	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK_R	31
ENET_RXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK	18 31
	ENET_MII_55S	ENET_MII	ENET_RXD_R<3..0>	31
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RXD<0>	18 31
ENET_RXD_STRAP	ENET_MII_55S	ENET_MII	ENET_RXD<3..1>	18 31
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RX_CTRL	18 31
	ENET_MII_55S	ENET_MII	ENET_RXCTL_R	31
	ENET_MII_55S	ENET_MII	ENET_CLK125M_TXCLK_R	31
ENET_TXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_TXCLK	9 31
ENET_TXD0	ENET_MII_55S	ENET_MII	ENET_TXD<0>	9 31
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TXD<3..1>	9 31
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TX_CTRL	9 31
	ENET_MII_55S	ENET_MII	ENET_RESET_L	9 31
ENET_MDI	ENET_MDI_100D	ENET_MDI	ENET_MDI_P<3..0>	31 32
	ENET_MDI_100D	ENET_MDI	ENET_MDI_N<3..0>	31 32
	ENET_MDI_100D	ENET_MDI	ENET_MDI_TRAN_P<3..0>	32
	ENET_MDI_100D	ENET_MDI	ENET_MDI_TRAN_N<3..0>	32

SYNC_MASTER=K87_MLB SYNC_DATE=02/26/2010

PAGE TITLE: Ethernet Constraints

Apple Inc.

DRAWING NUMBER: 051-8407 SIZE: D

REVISION: A.0.0

BRANCH:

PAGE: 104 OF 109

SHEET: 73 OF 76

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
SMBUS_SMC_A_S3_SCL	SMB_55S	SMB	SMBUS_SMC_A_S3_SCL 7 38
SMBUS_SMC_A_S3_SDA	SMB_55S	SMB	SMBUS_SMC_A_S3_SDA 7 38
SMBUS_SMC_B_S0_SCL	SMB_55S	SMB	SMBUS_SMC_B_S0_SCL 38
SMBUS_SMC_B_S0_SDA	SMB_55S	SMB	SMBUS_SMC_B_S0_SDA 38
SMBUS_SMC_0_S0_SCL	SMB_55S	SMB	SMBUS_SMC_0_S0_SCL 38
SMBUS_SMC_0_S0_SDA	SMB_55S	SMB	SMBUS_SMC_0_S0_SDA 38
SMBUS_SMC_BSA_SCL	SMB_55S	SMB	SMBUS_SMC_BSA_SCL 7 38
SMBUS_SMC_BSA_SDA	SMB_55S	SMB	SMBUS_SMC_BSA_SDA 7 38
SMBUS_SMC_MGMT_SCL	SMB_55S	SMB	SMBUS_SMC_MGMT_SCL 38
SMBUS_SMC_MGMT_SDA	SMB_55S	SMB	SMBUS_SMC_MGMT_SDA 38

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P 55
	1TO1_DIFFPAIR		CHGR_CSI_N 55
	1TO1_DIFFPAIR		CHGR_CSI_R_P 55
	1TO1_DIFFPAIR		CHGR_CSI_R_N 55
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P 55
	1TO1_DIFFPAIR		CHGR_CSO_N 55
	1TO1_DIFFPAIR		CHGR_CSO_R_P 40 55
	1TO1_DIFFPAIR		CHGR_CSO_R_N 40 55

SYNC_MASTER=K87_MLB SYNC_DATE=02/26/2010

PAGE TITLE: SMC Constraints

Apple Inc.

DRAWING NUMBER: 051-8407 SIZE: D

REVISION: A.0.0

BRANCH:

PAGE: 106 OF 109

SHEET: 74 OF 76

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
MEM_POWER	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_POWER	*	PWR_P2MM
MEM_CMD	MEM_POWER	*	PWR_P2MM
MEM_CTRL	MEM_POWER	*	PWR_P2MM
MEM_DATA	MEM_POWER	*	PWR_P2MM
MEM_DQS	MEM_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_FSB	GND	*	GND_P2MM
CPU_COMP	GND	*	GND_P2MM
CPU_GTLREF	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM

MCP Fanout Constraint Relaxations

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*			0.09 MM	5.8 MM		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP	TOP			0.1 MM	500 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MCP_MEM_COMP	TOP			0.1 MM	500 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MCP_MII_COMP	TOP			0.1 MM	500 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MCP_USB_RBIAS	TOP			0.1 MM	500 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP	*			0.25 MM	250 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE

Misc Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
(PCIE_AP)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_AP_CONN_P
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_AP_CONN_N
(USB_EXTA)	USB_90D	USB	USB_EXTA_MUXED_P 34 72
(USB_EXTA)	USB_90D	USB	USB_EXTA_MUXED_N 34 72
(USB_EXTA)	USB_90D	USB	USB_LT1_P
(USB_EXTA)	USB_90D	USB	USB_LT1_N
(USB_TPAD)	USB_90D	USB	USB_TPAD_R_P 43
(USB_TPAD)	USB_90D	USB	USB_TPAD_R_N 43
(USB_CAMERA)	USB_90D	USB	USB_CAMERA_CONN_P 7 64
(USB_CAMERA)	USB_90D	USB	USB_CAMERA_CONN_N 7 64
	USB_90D	USB	USB_LT2_P
	USB_90D	USB	USB_LT2_N
	ENET_MDI_100D	ENETCONN	ENETCONN_P<3..0>
	ENET_MDI_100D	ENETCONN	ENETCONN_N<3..0>
	SATA_90D	SATA	SATA_ODD_R2D_UF_P 33
	SATA_90D	SATA	SATA_ODD_R2D_UF_N 33
	SATA_90D	SATA	SATA_ODD_D2R_UF_P 33
	SATA_90D	SATA	SATA_ODD_D2R_UF_N 33
	SATA_90D	SATA	SATA_HDD_D2R_FILT_P 33
	SATA_90D	SATA	SATA_HDD_D2R_FILT_N 33
	SATA_90D	SATA	SATA_HDD_D2R_UF_P 33
	SATA_90D	SATA	SATA_HDD_D2R_UF_N 33
	SATA_90D	SATA	SATA_HDD_R2D_UF_P 33
	SATA_90D	SATA	SATA_HDD_R2D_UF_N 33
	SATA_90D	SATA	SATA_HDD_D2R_RDRV_IN_P
	SATA_90D	SATA	SATA_HDD_D2R_RDRV_IN_N
	SATA_90D	SATA	SATA_HDD_R2D_RDRV_IN_P
	SATA_90D	SATA	SATA_HDD_R2D_RDRV_IN_N
	SATA_90D	SATA	SATA_HDD_D2R_RDRV_OUT_P
	SATA_90D	SATA	SATA_HDD_D2R_RDRV_OUT_N
	SATA_90D	SATA	SATA_HDD_R2D_RDRV_OUT_P
	SATA_90D	SATA	SATA_HDD_R2D_RDRV_OUT_N
	SATA_90D	SATA	SATA_HDD_D2R_NORDRV_P
	SATA_90D	SATA	SATA_HDD_D2R_NORDRV_N
	SATA_90D	SATA	SATA_HDD_R2D_NORDRV_P
	SATA_90D	SATA	SATA_HDD_R2D_NORDRV_N
PCIE_AP_D2R	PCIE_90D	PCIE	CONN_PCIE_MINI_D2R_P 7 9 30
	PCIE_90D	PCIE	CONN_PCIE_MINI_D2R_N 7 9 30
PCIE_AP_R2D	PCIE_90D	PCIE	CONN_PCIE_MINI_R2D_P 7 9 30
	PCIE_90D	PCIE	CONN_PCIE_MINI_R2D_N 7 9 30
USB_BT	USB_90D	USB	CONN_USB2_BT_P 7 30
	USB_90D	USB	CONN_USB2_BT_N 7 30
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_F_P 7 64
	LVDS_100D	LVDS	LVDS_IG_A_CLK_F_N 7 64
MCP_PE1_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CONN_P 7 30
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CONN_N 7 30
(129) USB_EXTA	USB_90D	USB	CONN_USB_EXTA_P 34
(129)	USB_90D	USB	CONN_USB_EXTA_N 34
(129) USB_EXTB	USB_90D	USB	CONN_USB_EXTB_P 34
(129)	USB_90D	USB	CONN_USB_EXTB_N 34

GRAPHICS NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
(DP_EXT_ML)	DP_90D	DISPLAYPORT	DP_EXT_ML_P<3..0> 9 66
	DP_90D	DISPLAYPORT	DP_EXT_ML_N<3..0> 9 66
	DP_90D	DISPLAYPORT	DP_EXT_ML_C_P<3..0> 66
	DP_90D	DISPLAYPORT	DP_EXT_ML_C_N<3..0> 66
	DP_90D	DISPLAYPORT	DP_EXT_ML_F_P<3..0> 66
	DP_90D	DISPLAYPORT	DP_EXT_ML_F_N<3..0> 66
(DP_EXT_AUX_CH)	DP_90D	DISPLAYPORT	DP_EXT_AUX_CH_C_P 9 66
	DP_90D	DISPLAYPORT	DP_EXT_AUX_CH_C_N 9 66
	DP_90D	DISPLAYPORT	DP_EXT_DDC_DATA 65
	DP_90D	DISPLAYPORT	DP_EXT_DDC_CLK 65

Power Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
CPUTHMSNS_D2	THERM_1TO1_55S	THERM	CPUTHMSNS_D1_P 41
	THERM_1TO1_55S	THERM	CPUTHMSNS_D1_N 41
(1498) CPUTHMSNS_D2	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_P 41
(1497)	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_N 41
CPU_THERMD	THERM_1TO1_55S	THERM	CPU_THERMD_P 10 41
	THERM_1TO1_55S	THERM	CPU_THERMD_N 10 41
MCPTHMSNS_D2	THERM_1TO1_55S	THERM	MCPTHMSNS_D2_P
	THERM_1TO1_55S	THERM	MCPTHMSNS_D2_N
MCP_THMDIODE	THERM_1TO1_55S	THERM	MCP_THMDIODE_P 19 41
	THERM_1TO1_55S	THERM	MCP_THMDIODE_N 19 41
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_P
	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_N
	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_R_P
	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_R_N
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_P 30 46
	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_N 30 46
	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_R_P 46
	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_R_N 46
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HDD_P 33 46
	SENSE_1TO1_55S	SENSE	ISNS_HDD_N 33 46
	SENSE_1TO1_55S	SENSE	ISNS_HDD_R_P 46
	SENSE_1TO1_55S	SENSE	ISNS_HDD_R_N 46
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_P 46 67
	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_N 46 67
	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_R_P
	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_R_N
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_ODD_P 33 46
	SENSE_1TO1_55S	SENSE	ISNS_ODD_N 33 46
	SENSE_1TO1_55S	SENSE	ISNS_ODD_R_P 46
	SENSE_1TO1_55S	SENSE	ISNS_ODD_R_N 46
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_CPUVTT_P 40
	SENSE_1TO1_55S	SENSE	ISNS_CPUVTT_N 40
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	MCPCORES0_VSEN_P 22 59
	SENSE_1TO1_55S	SENSE	MCPCORES0_VSEN_N 22 59
PWR		MEM_POWER	PP1V5R1V35_S3 7 8
		SB_POWER	PP3V3_S5 7 8 62
		SB_POWER	PP3V3_S0 7 8 62
		SB_POWER	PP1V5_S0 7 8 62
		GND	GND

Audio Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
	DIFFPAIR	AUDIO	AUD_SPKRAMP_LIN_P
	DIFFPAIR	AUDIO	AUD_SPKRAMP_LIN_N
	DIFFPAIR	AUDIO	AUD_SPKRAMP_SUBIN_P
	DIFFPAIR	AUDIO	AUD_SPKRAMP_SUBIN_N
	DIFFPAIR	AUDIO	AUD_SPKRAMP_RIN_P
	DIFFPAIR	AUDIO	AUD_SPKRAMP_RIN_N
	DIFFPAIR	AUDIO	SSM2315L_P
	DIFFPAIR	AUDIO	SSM2315L_N
	DIFFPAIR	AUDIO	SSM2315S_P
	DIFFPAIR	AUDIO	SSM2315S_N
	DIFFPAIR	AUDIO	SSM2315R_P
	DIFFPAIR	AUDIO	SSM2315R_N
SPK_OUT	DIFFPAIR	AUDIO	SPKRCONN_L_OUT_P
	DIFFPAIR	AUDIO	SPKRCONN_L_OUT_N
SPK_OUT	DIFFPAIR	AUDIO	SPKRCONN_S_OUT_P
	DIFFPAIR	AUDIO	SPKRCONN_S_OUT_N
SPK_OUT	DIFFPAIR	AUDIO	SPKRCONN_R_OUT_P
	DIFFPAIR	AUDIO	SPKRCONN_R_OUT_N
	DIFFPAIR	AUDIO	BI_MIC_P 7 52 53
	DIFFPAIR	AUDIO	BI_MIC_N 7 52 53
	DIFFPAIR	AUDIO	HS_MIC_P 52 53
	DIFFPAIR	AUDIO	HS_MIC_N 52 53

SYNC_MASTER=K87_MLB SYNC_DATE=02/26/2010

PAGE TITLE: K87 SPECIFIC CONSTRAINTS

Apple Inc.

DRAWING NUMBER: 051-8407 SIZE: D

REVISION: A.0.0

BRANCH:

PAGE: 108 OF 109

SHEET: 75 OF 76

K87 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA_P1MM	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	0.100MM	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.115 MM	0.115 MM			
50_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.100 MM			
40_OHM_SE	*	Y	0.126 MM	0.100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.310 MM			
27P4_OHM_SE	*	Y	0.222 MM	0.222 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.151 MM	0.100 MM	=STANDARD	0.224 MM	0.224 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.185 MM	0.100 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.095 MM	0.095 MM		0.234 MM	0.234 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.112 MM	0.112 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.075 MM	0.075 MM		0.244 MM	0.244 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.091 MM	0.091 MM		0.230 MM	0.230 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.08 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P3MM	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5X_DIELECTRIC	TOP,BOTTOM	0.105 MM	?
2X_DIELECTRIC	TOP,BOTTOM	0.140 MM	?
3X_DIELECTRIC	TOP,BOTTOM	0.210 MM	?
4X_DIELECTRIC	TOP,BOTTOM	0.280 MM	?
5X_DIELECTRIC	TOP,BOTTOM	0.350 MM	?
1.5X_DIELECTRIC	*	0.095 MM	?
2X_DIELECTRIC	*	0.126 MM	?
3X_DIELECTRIC	*	0.189 MM	?
4X_DIELECTRIC	*	0.252 MM	?
5X_DIELECTRIC	*	0.315 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA_P1MM	BGA_P1MM
MEM_CLK	*	BGA_P1MM	BGA_P2MM
CLK_FSB	*	BGA_P1MM	BGA_P2MM
CLK_LPC	*	BGA_P1MM	BGA_P2MM
CLK_PCIE	*	BGA_P1MM	BGA_P2MM
CLK_SLOW	*	BGA_P1MM	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA_P1MM	BGA_P3MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_405	BGA_P1MM	STANDARD

SYNC_MASTER=K87_MLB SYNC_DATE=12/03/2009

PAGE TITLE: K87 RULE DEFINITIONS

Apple Inc.

DRAWING NUMBER: 051-8407 SIZE: D

REVISION: A.0.0

BRANCH:

PAGE: 109 OF 109

SHEET: 76 OF 76