1. ALL RESISTANCE VALUES ARE IN OHMS; 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSALS & OSCILLATOR VALUES ARE IN HERTZ.
### BOM Groups

#### Always-present

- **Module Parts**
  - 353S2811
  - 138S0603
  - 152S0796, 152S0685 (ALL)
  - 152S0693, 152S0778 (ALL)

#### Development BOM

- **Programmable Parts**
  - 514-0718 (IS CLOUD GREY 4/LB3 PLASTIC W/PDNI PLATING VERSION OF 514-0694 PART FOR AUDIO CONNECTOR)
  - 514-0706 (IS CLOUD GREY 4/LB3 PLASTIC W/PDNI PLATING VERSION OF 514-0691 PART FOR MINI DP CONNECTOR)
  - 514-0705 (IS CLOUD GREY 4/LB3 PLASTIC W/PDNI PLATING VERSION OF 514-0689 PART FOR USB CONNECTORS)
  - 514-0704 (IS CLOUD GREY 4/LB3 PLASTIC W/PDNI PLATING VERSION OF 514-0692 PART FOR RJ45 CONNECTOR)

- **NEW IMPROVED INTERSIL PART AS ALTERNATE**
  - 353S2718

#### Project phase-dependent

- **K86_K87_DEBUG**
  - PROD: VREFMRGN: NO, BMON: PROD, SENS_R: PROD
  - ENG: VREFMRGN: YES, BMON: ENG, SENS_R: ENG

- **K86_K87_COMMON**
  - 639-1059: MOLEX_DDR_CONN, EE: DCV3PCBA, MLB, MOLEX, K86
  - 639-0708: FOX_DDR_CONN, EE: E3TPCBA, MLB, FOXCONN, K86

- **SUBASSY, IC, BOOT ROM, K86/K87**
  - SUBASSY, IC, SMC, K86
  - SUBASSY, IC, SMC, K87

- **POGO PIN**
  - TALL, NOISE-IMPROVED, SILVER, K87
  - ZS0900, ZS0901, ZS0902, ZS0903

- **516-0213**
  - MOLEX_DDR_CONN1 CRITICAL J2900

- **335S0610**
  - IC, FLASH, SPI, 32MBIT, 3.3V, 86MHZ, 8-SOP

- **SCREW1, SCREW2, SCREW3, SCREW4**

- **452-1708**

- **516S0790**
  - CONN, 204P, SODIMM, SOCKET, DDR3, RAM, BGA

- **337S3866**

- **337S3792**
  - U1000 CRITICAL CPU: 1.2GHZ

- **085-1154**
  - CRITICAL 1

#### Part Number

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>ALTERNATE FOR</th>
<th>PART NUMBER</th>
<th>ALTERNATE FOR</th>
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<tbody>
<tr>
<td>8 7 5 4 2 1</td>
<td>1341S2677</td>
<td>U5701</td>
<td>WELLSPRING: PROG</td>
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<td>U5701</td>
<td>CRITICAL WELLSPRING: BLANK</td>
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<td>U6100</td>
<td>BOOTROM: PROG</td>
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<td>CRITICAL BOOTROM: BLANK</td>
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<td>U4900</td>
<td>SMC: PROG_K86</td>
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<td>U4900</td>
<td>SMC: PROG_K87</td>
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<td>IC, SMC, HS8/2117, 9X9MM, TLP, HF</td>
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<td>3870-1938</td>
<td>CRITICAL</td>
<td>5870-1939</td>
<td>CRITICAL</td>
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<td>3870-1940</td>
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<td>1337S3876</td>
<td>U1400 CRITICAL</td>
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<td>1337S3680</td>
<td>IC, WELLSPRING CONTROLLER, K87</td>
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<td>3870-1938</td>
<td>CRITICAL</td>
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<td>5870-1939</td>
<td>CRITICAL</td>
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<td></td>
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<td>3870-1940</td>
<td>CRITICAL</td>
<td></td>
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</tr>
<tr>
<td></td>
<td></td>
<td>1337S3876</td>
<td>U1400 CRITICAL</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### K86/K87 BOARD STACK-UP

#### TOP SIGNAL
- 2 GROUND
- 3 SIGNAL (High Speed)
- 4 SIGNAL (High Speed)
- 5 GROUND
- 6 POWER
- 7 POWER
- 8 GROUND
- 9 SIGNAL (High Speed)
- 10 SIGNAL (High Speed)
- 11 GROUND

#### BOTTOM SIGNAL

---

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**Page Information:**

- **Page Title:**
- **Sync Master:** K87_MLB
- **Branch:**
- **Drawing Number:**
- **Size:**
- **Printed Page:** 4 of 109
- **Ready to Print:**
- **Branch:**
- **Printed Page:** 4 of 76

---

**Back Cover:**

- **Search & Tools:**
- **Find in This Document:**
- **Copy to Clipboard:**
- **Add Note:**
- **Add Bookmark:**

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**Apple Inc.:**

A.O.S

851-8407 D

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**Drawn by:**

- **Date:**

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- **Date:**

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- **Date:**

---

**Page Terminology:**

- **FRAME:**
- **PALETTE:**
- **GUIDES:**
- **OUTER LINE:**
- **INNER LINE:**
- **TEXT:**
- **ANIMATED:**
- **WORKALONG:**
- **ANGLED:**
- **ANCHOR:**
- **TEXT:**
- **ANIMATED:**
- **WORKALONG:**
- **ANGLED:**
- **ANCHOR:**

---

**Note:**

- **Description:**
- **Reference:**
- **Design:**
- **Options:**
- **Criticality:**
- **Component:**
- **Assembly:**
- **Handling:**
- **Material:**
- **Specification:**
- **Designator:**
- **Description:**
- **Package:**
- **Vendor:**
- **Application:**
- **Function:**
- **Assembly:**
- **Handling:**
- **Material:**
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- **Package:**
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- **Material:**
- **Specification:**
- **Designator:**
- **Description:**
- **Package:**
- **Vendor:**
- **Application:**
- **Function:**
- **Assembly:**
- **Handling:**
- **Material:**
- **Specification:**
- **Designator:**
### Revision History

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<th>DATE</th>
<th>SIZE</th>
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<tbody>
<tr>
<td>051-8407</td>
<td>9/12/2010</td>
<td>5 OF 109</td>
</tr>
</tbody>
</table>

**NOTE:** All page numbers are .cns, .txt PDF. See page 1 for .cns -> PDF mapping.

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**2010-01-13:** 2.2.0

- 2010-01-13: 2.1.0
- 2010-01-06: 1.11.0
- 2009-12-22: 1.10.0
- 2009-12-16: 1.8.0
- 2009-12-09: 1.5.0
- 2009-12-08: 1.3.0
- 2009-12-04: 1.1.0
- 2009-12-03: Proto 0 release 1.0.0

---

* *** Started syncing with K6

**Per [rdar://problem/7544629](http://rdar://problem/7544629)** K86/K87: Update MCP83 description on csa 4

- Switching from Engineering to Production BOM should only require changing PROJECT_PHASE:DEV to PROJECT_PHASE:PROD
- Changed BOM group structure to match that in the radar (see PDF attached to radar)

**csa 4:**

- Per [rdar://problem/7549122](http://rdar://problem/7549122) K86/K87: Switch to new BOM group structure

**csa 74, csa 79:**

- R7416 added to BOM table, 16.9K, (APN 114S0336)

**csa 74:**


**csa 51:**

- (Per [rdar://problem/7540522](http://rdar://problem/7540522) K86/K87: Production Debug Components)
- Changed all instances of K87_DEVEL_xxxx to K87_DEVEL:xxxx
- Changed all instances of K87_DEBUG_xxxx to K87_DEBUG:xxxx

**Unchanged:**

- BKLT:ENG        ==>     BKLT:PROD
- BMON:ENG        ==>     BMON:PROD
- VREFMRGN:YES    ==>     VREFMRGN:NO

- Diff from the two changes above:
  - Changed K87_COMMON to call out K87_DEBUG_PVT instead of K87_DEBUG_ENG

**csa 4:**

- Cosmetic: changed text sizes and alignment
- Per [rdar://problem/7540383](http://rdar://problem/7540383) K86: Update CPU part number to 337S3792

**Changed R4585, R4586 to 114S0065 (27.4 ohm, 1%)**

**Deleted BOM table that stuffsdel the bypass option**

**Changed U7000 from 353S2392 to 353S2929**

**csa 23:**

- *** BROKE SYNC WITH T27

**LPC_SERIRQ**

**LPCPLUS_GPIO**

- Changed BOMOPTION for R7872 from S0PGOOD_ISL to NOSTUFF

- Conn APN:518S0788"

- MCO:     056-3515
- BOM:     639-0680

- Added text note with part numbers for components of the assembly

**csa 69:**

- Per [rdar://problem/7494087](http://rdar://problem/7494087) K87: remove OMIT from J6955 and delete BOM table

**Changed BOOTROM:PROG to call out 341T0251 (SUBASSY, IC, BOOT ROM, K86/K87)**

**Per [rdar://problem/7495072](http://rdar://problem/7495072) K87: Call out LED:K86_K87 BOMOPTION in the K87_MISC BOM group**

**Added BOM table entry for MCP83M (337S3876)**

**Alternates table on csa 4 already has 152S0778 as alternate to 152S0693**

**Changed R3440 color to green, deleted WF text note about needing PU**

**Updated DLY text note for U3440 to match T27**

**Changed R3454 to 100k, 1% (114S0411) to match T27 and K69**

**csa 34:**

- Changed U3440 from AP002 part to AP016 (343S0511) per [radar:7459498](http://radar:7459498) BOM: APN updates for FPF1009 and SAK parts

- Added R5714 (114S0125) to table with BOMOPTION LED:K86_K87

---

**csa 108:*** Made the following changes to follow T27 on the following unsynced pages:

- **T27:** Added CKPLUS_WAIVE properties to dismiss false errors (pg. 54).
- **C5490 changed from CAP_402-0.022UF,10%,16V,CERM-X5R to CAP_402-0.022UF,20%,16V,CERM**

**csa 29,31:*** Began syncing from T27 per [radar:7424246](http://radar:7424246) BOM: K87 needs omit on J3100 and J2900 from T27

---

**csa 20:**

- **T27:** Added CKPLUS_WAIVE properties to dismiss false errors (pg. 20). [radar:7368529] TASK: Waive false CheckPlus errors

**csa 18:**

- **T27:** Swapped USB_EXTB and USB_EXTD for NVRN-612340 (pg. 18). [radar:7416825] Ensure USB_EXTB is on ports 8-11 (NVRN-612340)

**csa 108:**

- Added NET_PHYSICAL property to SATA_HDD_D2R_FILT_P and _N

**csa 90:**

- Deleted net properties for =PP5V_S3_CAMERA

**csa 8:**

- Deleted net properties for the following nets:

**Added BOM table to stuff 0-ohms until we get go-ahead for filter**

- Added C4585, C4586 (10pF, 5%, 131S0029) and NOSTUFFed

**STILL NEED TO UPDATE VALUE OF C7428!**

- **C7413 = 100pF   5%  (131S1027)**
- **C7406 = 470pF   10% (132S4720)**
- **R7417 = 7.68k   1%  (114S0304)**

- **R7417, C7428, R7409, R7411, C7406, R7414, C7414, C7413**

**Added IMVP6:2PHASE to the following components:**

**Implemented different stuffing options for 1-phase vs 2-phase:**

- **C7434 from 0.12uF => 0.022uF, 10% (132S0102)**
- **R7417 from 5.36k => 6.34k, 1% (114S0296)**

---

**36**

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**www.vinafix.vn**
### CPU VCore HF and Bulk Decoupling

**Sync Date**: 12/09/2009  
**Sync Master**: K83_MLB

**CPU Decoupling**

**Decoupling**: Place inside socket cavity on secondary side.

<table>
<thead>
<tr>
<th>Decoupling Type</th>
<th>Value</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC (CPU AVdd)</td>
<td>1x 0.1µF, 2x 0.01µF</td>
<td>(20%) 6.3V</td>
</tr>
<tr>
<td>VCCP (CPU I/O)</td>
<td>1x 0.1µF, 2x 0.01µF</td>
<td>(20%) 6.3V</td>
</tr>
</tbody>
</table>

---

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---

**Drawings Number Size**: 051-8407  
**Page**: 12 of 109  
**Dimensions**: 1224.0 x 792.0
Mini-XDP Connector

NOTE: This is not the standard XDP pinout.
Use with custom adapter flex to support CPU, MCP debugging.

MCP89-SPECIFIC PINOUT

Direction of XDP module

Note: XDP_DBRESET_L must be pulled-up to 3.3V.

Sync Master=K87_MLB
Sync Date=12/09/2009

PE1 ports are Gen1-only. 2 RCs: x1, x1

PE0 ports are Gen2-capable. 4 RCs: 4x, x2, x1, x1

If PE0[4:5] and PE1[0:1] are not used, +VIO_PE_AVDD0 and +VIO_PE_DVDD0 can be GND

If PEI[3:0] are not used, +VIO_PE_AVDD1 and +VIO_PE_DVDD1 can be GND

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DDC Mode Pull-downs

Note: If all DDC signals are unused, no pull-downs are necessary. If used, pull-downs are required.

GPIO Pull-Ups

Note: If unused, pull-downs are required.
Connect RGMII_VREF to 10K pull-down.

+3.3V_PLL_MAC_DUAL must remain connected to 3.3V RMGT rail.

Connect RGMII_RXCLK to 10K pull-down.

RGMII_COMP_GND
RGMII_COMP_VDD
RGMII_RXCTL
RGMII_RXD1

USB8_N
USB5_P

USB8-11 support nV
USB_OC0*/GPIO_25
USB_OC2*/GPIO_27_MGPIO_0
USB_OC3*/GPIO_28_MGPIO_1

USB_EXTB_N
USB_BT_P
USB_TPAD_N
USB_TPAD_P
USB_CAMERA_P
USB_WM_N
USB_WM_P
USB_EXTD_N
USB_EXTC_OC_L
USB_EXTB_OC_L
USB_EXTA_OC_L
OC2# Also for EXTE

Bluetooth

www.vinafix.vn

Platform-Specific Connections


Output limited to +VDD_HDA.

NOTE: MCP89 does not support FWH, only FWH. So Apple designs will
not use LPC for BrownOut override.

Frequency

HDA_SYNC
24 MHz
24.31818 MHz
1
1

BIOS Boot Select

I/F LPC_FRAME
LPC 0
S PI 1

NOTE: MCP89 does not support FWH, only FWH. So Apple designs will
not use LPC for BrownOut override.

LPC Clock Run*/GPIO_42
LPC_RESET*/GPIO_45

Frequency

SPI_CLK
25.0 MHz
0
0

SPI_CLK
31.2 MHz
0
1

SPI_CLK
62.5 MHz
1
1

NOTE: 42 & 62 MHz use FAST_BOOT commands.


NOTE: "SM" rails are dynamically switched in the SM state as needed, controlled by MCP89 GPIOs.

Instead connect regulator sense point regulators.

www.vinafix.vn
Q2300 helps reduce input rail droop during Q2305 turn-on.

Approx. Ramp Time (EN to 1.35V, uS): 7.91 + 0.0678 * R1 (Kohms)

NOTE: nVidia recommends Infineon BSC030N03MS for Q2300.

Gated Rail Savings: 120mW

DIMM CKE Clamps

CKE must be held low to keep memory in self-refresh. Clamps enable before MCP89 MEMVDD rail switched off. Clamps release after MCP89 MEMVDD is up and CKEs are driven by MCP89. Clamps also discharge VTT rail via termination resistor on each CKE signal on DIMM. Q2355/Q2356 chosen for low output capacitance.

NO STUBS on CKE signals!
C2400 helps reduce input rail drop during GFX5 transition:
\[ \text{Approx. Ramp Time (EN to 1V, \mu s)} = 43.9 + 0.6943 \times C1(\text{pF}) \]

Max Ramp-Up Time: 1500 \mu s (ENABLE to 90%)

- Min Ramp-Up Time: 100 \mu s (10% to 90%)
- FET Ron \leq 2.5 \text{mOhms}
- Gated Rail Savings: 860mW

Loading
\[ \text{Rds(on)} \]

<table>
<thead>
<tr>
<th>SM</th>
<th>Part</th>
<th>Loading</th>
<th>Rds(on)</th>
</tr>
</thead>
<tbody>
<tr>
<td>XW2400</td>
<td>SI4838BDY</td>
<td>SO-8</td>
<td>3.2 mOhm @2.5V</td>
</tr>
<tr>
<td>XW2401</td>
<td>PLACE_NEAR=C2400.2:1 mm</td>
<td>SM</td>
<td>59 75</td>
</tr>
<tr>
<td>XW2402</td>
<td>PLACE_NEAR=C2400.1:1 mm</td>
<td>SM</td>
<td>59 75</td>
</tr>
</tbody>
</table>

NOTE: nVidia recommends Infineon BSC020N03MS for Q2400.

C2405 helps reduce input rail droop during Q2400 turn-on.

C2405 helps reduce input rail droop during Q2400 transition:
\[ \text{Approx. Ramp Time (EN to 1V, \mu s)} = 43.9 + 0.6943 \times C1(\text{pF}) \]

Max Ramp-Up Time: 1500 \mu s (ENABLE to 90%)

- Min Ramp-Up Time: 100 \mu s (10% to 90%)
- FET Ron \leq 2.5 \text{mOhms}
- Gated Rail Savings: 860mW

Loading
\[ \text{Rds(on)} \]

<table>
<thead>
<tr>
<th>SM</th>
<th>Part</th>
<th>Loading</th>
<th>Rds(on)</th>
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</thead>
<tbody>
<tr>
<td>XW2400</td>
<td>SI4838BDY</td>
<td>TDFN</td>
<td>402</td>
</tr>
<tr>
<td>XW2401</td>
<td>PLACE_NEAR=C2400.2:1 mm</td>
<td>SM</td>
<td>59 75</td>
</tr>
<tr>
<td>XW2402</td>
<td>PLACE_NEAR=C2400.1:1 mm</td>
<td>SM</td>
<td>59 75</td>
</tr>
</tbody>
</table>

NOTE: nVidia recommends Infineon BSC020N03MS for Q2400.

Gated Rail Savings: 860mW
### Page Notes

<table>
<thead>
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<tbody>
<tr>
<td>+33V/3.3V_VREFDACS</td>
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<tr>
<td>I2C_PCA9557D_SDA</td>
</tr>
<tr>
<td>I2C_PCA9557D_SCL</td>
</tr>
<tr>
<td>I2C_VREFDACS_SDA</td>
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</tbody>
</table>

**NOTE:** Soft resets and sleep/wake cycles.

---

### Required zero ohm resistors when no VREF margining circuit stuffed

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>REFERENCE DES</th>
<th>CRITICAL</th>
<th>NOTE</th>
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</thead>
<tbody>
<tr>
<td>R3332, R3334</td>
<td>2</td>
<td>22.6K1%</td>
<td>CRITICAL</td>
<td>PLACE_NEAR=R3321.2:1mm</td>
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<tr>
<td>R3333</td>
<td>1</td>
<td>200MF-LF</td>
<td>CRITICAL</td>
<td>PLACE_NEAR=J2900.126:2.54mm</td>
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<tr>
<td>R3340</td>
<td>1</td>
<td>133MF-LF</td>
<td>CRITICAL</td>
<td>PLACE_NEAR=R3333.2:1mm</td>
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<tr>
<td>R3342, R3344</td>
<td>2</td>
<td>133MF-LF</td>
<td>CRITICAL</td>
<td>PLACE_NEAR=R3333.2:1mm</td>
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### DAC Channel

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<thead>
<tr>
<th>MEM A VREF DQ</th>
<th>MEM B VREF DQ</th>
<th>MEM A VREF CA</th>
<th>MEM B VREF CA</th>
<th>MEM VREG</th>
<th>CPU GTLRREF (FSB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>B</td>
<td>C</td>
<td>D</td>
<td>E</td>
<td>F</td>
</tr>
<tr>
<td>1.0V (DAC: 0x3A)</td>
<td>0.7V (DAC: 0x88)</td>
<td>1.99V = 1.002V (+/- 498mV)</td>
<td>1.998V = 1.002V (+/- 498mV)</td>
<td>0.000V = 0.050V (+/- 50mV)</td>
<td>0.000V = 0.050V (+/- 50mV)</td>
</tr>
<tr>
<td>0.300V = 1.200V (+/- 450mV)</td>
<td>0.300V = 1.200V (+/- 450mV)</td>
<td>0.000V = 0.050V (+/- 50mV)</td>
<td>0.000V = 0.050V (+/- 50mV)</td>
<td>0.000V = 0.050V (+/- 50mV)</td>
<td>0.000V = 0.050V (+/- 50mV)</td>
</tr>
<tr>
<td>+3.4mA (+/- sourced)</td>
<td>+3.4mA (+/- sourced)</td>
<td>+33.4mA (+/- sourced)</td>
<td>+33.4mA (+/- sourced)</td>
<td>+750uA (+/- sourced)</td>
<td>+750uA (+/- sourced)</td>
</tr>
<tr>
<td>8.59mV / step @ output</td>
<td>9.24mV / step @ output</td>
<td>0.300V - 1.200V (+/- 450mV)</td>
<td>0.75V (DAC: 0x3A)</td>
<td>0.000V - 1.501V (0x00 - 0x74)</td>
<td>1.5V (DAC: 0x3A)</td>
</tr>
</tbody>
</table>

---

### Signal aliases required by this page:

<table>
<thead>
<tr>
<th>Signal Alias</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>PPVTT_S3_DDR_BUF</td>
<td>DDR Reg FB</td>
</tr>
<tr>
<td>PP3V3_S3_VREFMRGN</td>
<td>PPCNT_FSB_VREF_CA</td>
</tr>
</tbody>
</table>

---

### Margined target:

- Margined target: 0.300V = 1.200V (+/- 450mV)
- DAC range: 0.000V = 1.501V (0x00 = 0x74)
- DAC step size: 8.59mV / step @ output
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---

**Ethernet PHY (RTL8211CL)**

**Configuration Settings:**
- **RSTC**: 0 (Reset Configuration)
- **RESW**: 0 (Reset all)
- **RESE**: 0 (Reset all)
- **RECV**: 0 (No connect)
- **MDI**: 0 (No connect)
- **MDI+**: 0 (No connect)
- **MDI-**: 0 (No connect)
- **MDI0**: 0 (No connect)
- **MDI1**: 0 (No connect)
- **MDI2**: 0 (No connect)
- **MDI3**: 0 (No connect)
- **MDI4**: 0 (No connect)
- **MDI5**: 0 (No connect)
- **MDI6**: 0 (No connect)
- **MDI7**: 0 (No connect)
- **MDI8**: 0 (No connect)
- **MDI9**: 0 (No connect)
- **MDI10**: 0 (No connect)
- **MDI11**: 0 (No connect)
- **MDI12**: 0 (No connect)
- **MDI13**: 0 (No connect)
- **MDI14**: 0 (No connect)
- **MDI15**: 0 (No connect)
- **MDI16**: 0 (No connect)
- **MDI17**: 0 (No connect)
- **MDI18**: 0 (No connect)
- **MDI19**: 0 (No connect)
- **MDI20**: 0 (No connect)
- **MDI21**: 0 (No connect)
- **MDI22**: 0 (No connect)
- **MDI23**: 0 (No connect)
- **MDI24**: 0 (No connect)
- **MDI25**: 0 (No connect)
- **MDI26**: 0 (No connect)
- **MDI27**: 0 (No connect)
- **MDI28**: 0 (No connect)
- **MDI29**: 0 (No connect)
- **MDI30**: 0 (No connect)
- **MDI31**: 0 (No connect)
- **MDI32**: 0 (No connect)
- **MDI33**: 0 (No connect)
- **MDI34**: 0 (No connect)
- **MDI35**: 0 (No connect)
- **MDI36**: 0 (No connect)
- **MDI37**: 0 (No connect)
- **MDI38**: 0 (No connect)
- **MDI39**: 0 (No connect)
- **MDI40**: 0 (No connect)
- **MDI41**: 0 (No connect)
- **MDI42**: 0 (No connect)
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- **MDI64**: 0 (No connect)
- **MDI65**: 0 (No connect)
- **MDI66**: 0 (No connect)
- **MDI67**: 0 (No connect)
- **MDI68**: 0 (No connect)
- **MDI69**: 0 (No connect)
- **MDI70**: 0 (No connect)
- **MDI71**: 0 (No connect)
- **MDI72**: 0 (No connect)
- **MDI73**: 0 (No connect)
- **MDI74**: 0 (No connect)
- **MDI75**: 0 (No connect)
- **MDI76**: 0 (No connect)
- **MDI77**: 0 (No connect)
- **MDI78**: 0 (No connect)
- **MDI79**: 0 (No connect)
- **MDI80**: 0 (No connect)
- **MDI81**: 0 (No connect)
- **MDI82**: 0 (No connect)
- **MDI83**: 0 (No connect)
- **MDI84**: 0 (No connect)
- **MDI85**: 0 (No connect)
- **MDI86**: 0 (No connect)
- **MDI87**: 0 (No connect)
- **MDI88**: 0 (No connect)
- **MDI89**: 0 (No connect)
- **MDI90**: 0 (No connect)
- **MDI91**: 0 (No connect)
- **MDI92**: 0 (No connect)
- **MDI93**: 0 (No connect)
- **MDI94**: 0 (No connect)
- **MDI95**: 0 (No connect)
- **MDI96**: 0 (No connect)
- **MDI97**: 0 (No connect)
- **MDI98**: 0 (No connect)
- **MDI99**: 0 (No connect)
- **MDI100**: 0 (No connect)
- **MDI101**: 0 (No connect)
- **MDI102**: 0 (No connect)
- **MDI103**: 0 (No connect)
- **MDI104**: 0 (No connect)
NOTE: 3.3V must be S0 if 5V is S3 or S5 to ensure the drive is unpowered in S3/S5.

Use 0-ohm resistors and M0SUF caps if not using Passive de-emphasis filter.

Ensure the drive is unpowered in S3/S5.
PORT IS METAL USB CONNECTOR PARTS

Port Power Switch

USB/SMC Debug Mux

USB PORT A (FRONT PORT)

USB PORT B (BACK PORT)

External USB Connectors

Apple Inc. 851-8407-2

www.vinafix.vn
NOTE: Internal pull-ups are to VIN, not V+.

Used on mobiles to support SMC reset via keyboard.
MR1* and MR2* must both be low to cause manual reset. Use on mobiles to support SMC reset via keyboard.
NOTE: Internal pull-ups are to VIN, not V+.

Debug Power "Buttons"

SMC Crystal Circuit

System (Sleep) LED Circuit

SMC Pull-ups

SMC Pull-downs

SMC Support
MCP89 SMBus "0" Connections

Vref DACs
DAC5574: U3310
(Write: 0x72 Read: 0x73)

Mikey
CD3275: U6880
(Wires: GND/0, 5V/1)

Debug Devices
(SMBus Slave)

Margin Control
(U4900)

EFI Debug Serial
(Battery Charger)

MCP89 SMBus "1" Connections

SMB "0" SMBus Connections

Debug Temp
TPMEMA: U2533
(Write: 0x2D Read: 0x2B)

Trackpad
J5800
(Wire: 12V/4)

SMB "1" SMBus Connections

Prod Temp
SMIF123: U5521
(Write: 0x00 Read: 0x01)

SMB "A" SMBus Connections

SMB "Battery A" SMBus Connections

Battery Charger
(ISL6259 - U7000)

Battery
LT2309: U6000
(Write: 0x19)

SMB "Management" SMBus Connections

SMC "Battery A" SMBus Connections

SMC Trackpad
J5800
(Wire: 12V/4)

SMC "B" SMBus Connections

Debug ADC
(ISL6259 - U7000)

Battery Manager
(Write: 0x16)

Battery Temp
(ISL6259 - U7000)

The bus formerly known as "Battery B"
CPU PROXIMITY/HDD FLEX AREA/FINSTACK THERMAL SENSOR

DETECT HDD TEMPERATURE

DETECT FIN-STACK TEMPERATURE

MCP DIE/CPU DIE/MCP PROXIMITY THERMAL SENSOR

DETECT MCP DIE TEMPERATURE

DETECT CPU DIE TEMPERATURE
TPAD Buttons Disable

Place these components close to JP400.

This assumes there's a PP3V3_S3_PAD pull up on MLB.

The TPAD BUTTONS WILL BE DISABLED WHEN THE LED IS CLOSED.

The TPAD BUTTONS WILL BE DISABLED WHEN THE LED IS CLOSED.

Keys ANDed with PSOC power to isolate when PSOC is not powered.

SMC Manual Reset & Isolation

Left shift, option & control keys combined with power button cause SMC RESET assertion.

Keys ANDed with PSOC power to isolate when PSOC is not powered.
BOOSTER +18.5VDC FOR SENSORS

BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
- DROP LINE REGULATION
- RIPPLE TO MEET ESP
- STARTUP TIME LESS THAN 2MS
- R5812, R5813, C5818 MODIFIED

IPD Flex Connector

DO NOT SYNC FROM T27. REMOVED KEYBOARD BACKLIGHT CIRCUIT

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BRANCH

REVISION

DRAWING NUMBER SIZE

APPLE INC.
DO NOT SYNC WITH K84. REMOVED NO STUFF ON C5923, C5924, C5925. ADDED PLACE NEARS
LINE INPUT VOLTAGE DIVIDER

CODEC RIN = 70K OHMS
NET RIN = 15.26K OHMS (INCLUDING PULL-DOWNS AT ANALOG SWITCH COM PINS)
PC_25 = 3.6 Hz
PC_26 = 430KHz
VIN = 2V RMS, CODEC VIN = 1.14 VRMS

FC_LP = 43KHz
NET RIN = 10.36K OHMS (INCLUDING PULL-DOWNS AT ANALOG SWITCH COM PINS)

FC_HP = 3.6 Hz

CODEC RIN = 20K OHMS

LINE INPUT VOLTAGE DIVIDER

Vin = 2VRMS, CODEC VIN = 1.14 VRMS

FC_LP = 43KHz

NET RIN = 10.36K OHMS (INCLUDING PULL-DOWNS AT ANALOG SWITCH COM PINS)

FC_HP = 3.6 Hz

CODEC RIN = 20K OHMS

LINE INPUT VOLTAGE DIVIDER

Vin = 2VRMS, CODEC VIN = 1.14 VRMS

FC_LP = 43KHz

NET RIN = 10.36K OHMS (INCLUDING PULL-DOWNS AT ANALOG SWITCH COM PINS)

FC_HP = 3.6 Hz

CODEC RIN = 20K OHMS

LINE INPUT VOLTAGE DIVIDER

Vin = 2VRMS, CODEC VIN = 1.14 VRMS

FC_LP = 43KHz

NET RIN = 10.36K OHMS (INCLUDING PULL-DOWNS AT ANALOG SWITCH COM PINS)

FC_HP = 3.6 Hz

CODEC RIN = 20K OHMS

LINE INPUT VOLTAGE DIVIDER

Vin = 2VRMS, CODEC VIN = 1.14 VRMS

FC_LP = 43KHz

NET RIN = 10.36K OHMS (INCLUDING PULL-DOWNS AT ANALOG SWITCH COM PINS)

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CODEC RIN = 20K OHMS

LINE INPUT VOLTAGE DIVIDER

Vin = 2VRMS, CODEC VIN = 1.14 VRMS

FC_LP = 43KHz

NET RIN = 10.36K OHMS (INCLUDING PULL-DOWNS AT ANALOG SWITCH COM PINS)

FC_HP = 3.6 Hz

CODEC RIN = 20K OHMS
SATELLITE  796Hz < HPF FC < 936Hz
SUB     80 Hz < HPF FC < 94 Hz
GAIN    6DB (2V/V)

SPRK AMP. INPUT REFERRED CLIP POINT = ~6dBFS

ALIAS OF PP5V_S3_REG, MIN_LINE_WIDTH=0.30 mm, MIN_NECK_WIDTH=0.20 mm
-PP5V_S3_AUDIO_AMP

APN:353S2621

C6607

C6601

R6610

C6611

L6631

L6630

L6621

L6620

C6603

C6601

C6603

C6601

C6603

C6603

C6603

SYNC_DATE=02/26/2010
SYNC_MASTER=K87_MLB
AUDI0: SPEAKER AMP

AUD_GPIO_3

SPKRAMP_SHDN

SPKRAMP_SHDN

SPKRAMP_INSUB_P

SPKRAMP_INSUB_N

SPKRAMP_SUB_P_OUT

SPKRAMP_SUB_N_OUT

SPKRAMP_L_P_OUT

SPKRAMP_L_N_OUT

SPKRAMP_R_P_OUT

SPKRAMP_R_N_OUT

SPKRAMP_INL_P

SPKRAMP_INL_N

SPKRAMP_INR_P

SPKRAMP_INR_N

SPKRAMP_R_N

SPKRAMP_R_P

SPKRAMP_L_N

SPKRAMP_L_P
**Reverse-Current Protection**

- VIN threshold is 5.2V, +/- 10%
- R7051 has 2.2ohm to compensate unbalanced voltage due to different current
  - CHGR_CSI_R_P and (CHGR_CSI_R_N)
  - CHGR_CSI_R_P

**Inrush Limiter**

- R7010 divider sets ACIN threshold at 13.55V
- 40K input impedance meets sparkitecture requirements

**CriticalSpecifications**

- GND
- CHGR_BOOT
- CHGR_UGATE
- CHGR_PHASE
- CHGR_CSI_R
- CHGR_PHASE_RC
- CHGR_DCIN
- CHGR_BGATE
- CHGR_AMON
- CHGR_VNEG
- CHGR_ICOMP
- CHGR_CELL
- CHGR_ACIN
- CHGR_CSO_P
- CHGR_CSO_N
- CHGR_CSO_R_P
- CHGR_CSO_R_N
- CHGR_VNEG_R

**Notes:**

- R7050 APN 107S0075
- Bi-directional power interface for 1S

**Circuit Diagram**

- R7010 divider sets ACIN threshold at 13.55V
- 40K input impedance meets sparkitecture requirements
- GND
- CHGR_BOOT
- CHGR_UGATE
- CHGR_PHASE
- CHGR_CSI_R
- CHGR_PHASE_RC
- CHGR_DCIN
- CHGR_BGATE
- CHGR_AMON
- CHGR_VNEG
- CHGR_ICOMP
- CHGR_CELL
- CHGR_ACIN
- CHGR_CSO_P
- CHGR_CSO_N
- CHGR_CSO_R_P
- CHGR_CSO_R_N
- CHGR_VNEG_R

**Notes:**

- R7050 APN 107S0075
- Bi-directional power interface for 1S
MCP VCore Regulator

Apple Inc.
DO NOT SYNC FROM K84. ADDED ENET CIRCUITS, REMOVED 1V05 ENET CIRCUIT
FOUR GROUND VIAS SHOULD BE DISTRIBUTED ALONG THE GROUND SHAPE THAT BOUND THE CONNECTOR BODY.
<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>REFERENCE DES</th>
<th>CRITICAL</th>
<th>REV OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>C9300</td>
<td>1</td>
<td>SIGNAL_MODEL=DP_AUXCH_FET</td>
<td>SSOT563 SSM6N16FE</td>
<td>OMIT</td>
<td></td>
</tr>
</tbody>
</table>
13.3 Inch, K84 Panel (9 LEDs per string)

TARGET: ISET = 20mA, OVP = 35V

DO NOT SYNC FROM K84. L9710 CHANGED TO K6/K69

---

10.2 ohm resistors for current measurement on LED strings.
### FSB (Front-Side Bus) Constraints

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>FSB_CLK_CPU</td>
<td>100_OHM_DIFF</td>
<td>+</td>
<td>10 mil</td>
<td>100 mil</td>
</tr>
<tr>
<td>FSB_CPURST_L</td>
<td>100_OHM_DIFF</td>
<td>+</td>
<td>10 mil</td>
<td>100 mil</td>
</tr>
<tr>
<td>FSB_DSTB</td>
<td>27.4_OHM_SE</td>
<td>+</td>
<td>10 mil</td>
<td>100 mil</td>
</tr>
<tr>
<td>FSB_1X</td>
<td>27.4_OHM_SE</td>
<td>+</td>
<td>10 mil</td>
<td>100 mil</td>
</tr>
<tr>
<td>FSB_DATA</td>
<td>27.4_OHM_SE</td>
<td>+</td>
<td>10 mil</td>
<td>100 mil</td>
</tr>
</tbody>
</table>

### CPU / FSB Net Properties

<table>
<thead>
<tr>
<th>Net Property</th>
<th>Description</th>
<th>Min. Gap</th>
<th>Min. Dielectric Spacing</th>
</tr>
</thead>
<tbody>
<tr>
<td>FSB_CLK</td>
<td>4x_DIELECTRIC</td>
<td>10 mil</td>
<td>30 mil</td>
</tr>
<tr>
<td>FSB_DSTB</td>
<td>2x_DIELECTRIC</td>
<td>10 mil</td>
<td>30 mil</td>
</tr>
<tr>
<td>FSB_DATA</td>
<td>2x_DIELECTRIC</td>
<td>10 mil</td>
<td>30 mil</td>
</tr>
</tbody>
</table>

### MCP FSB COMP Signal Constraints

<table>
<thead>
<tr>
<th>Net Property</th>
<th>Description</th>
<th>Min. Gap</th>
<th>Min. Dielectric Spacing</th>
</tr>
</thead>
<tbody>
<tr>
<td>MCP_CPU_COMP_VCC</td>
<td>100_OHM_DIFF</td>
<td>10 mil</td>
<td>100 mil</td>
</tr>
<tr>
<td>MCP_50S</td>
<td>100_OHM_DIFF</td>
<td>10 mil</td>
<td>100 mil</td>
</tr>
</tbody>
</table>

### CPU Signal Constraints

<table>
<thead>
<tr>
<th>Net Property</th>
<th>Description</th>
<th>Min. Gap</th>
<th>Min. Dielectric Spacing</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU_DPRSTP_L</td>
<td>3x_DIELECTRIC</td>
<td>10 mil</td>
<td>30 mil</td>
</tr>
<tr>
<td>CPU_DPSLP_L</td>
<td>3x_DIELECTRIC</td>
<td>10 mil</td>
<td>30 mil</td>
</tr>
<tr>
<td>CPU_SMI_L</td>
<td>3x_DIELECTRIC</td>
<td>10 mil</td>
<td>30 mil</td>
</tr>
<tr>
<td>CPU_ASYNC</td>
<td>3x_DIELECTRIC</td>
<td>10 mil</td>
<td>30 mil</td>
</tr>
<tr>
<td>CPU_A20M_L</td>
<td>3x_DIELECTRIC</td>
<td>10 mil</td>
<td>30 mil</td>
</tr>
<tr>
<td>CPU_FERR_L</td>
<td>3x_DIELECTRIC</td>
<td>10 mil</td>
<td>30 mil</td>
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</tbody>
</table>

### CPU Overvoltage Protection

<table>
<thead>
<tr>
<th>Net Property</th>
<th>Description</th>
<th>Min. Gap</th>
<th>Min. Dielectric Spacing</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU_VCCSENSE</td>
<td>STANDARD</td>
<td>10 mil</td>
<td>100 mil</td>
</tr>
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</table>

### Physical Rule Set

<table>
<thead>
<tr>
<th>Layer</th>
<th>Minimum Neck Width</th>
<th>Maximum Neck Length</th>
</tr>
</thead>
<tbody>
<tr>
<td>TOP</td>
<td>1:1_DIFFPAIR</td>
<td>2:1_SPACING</td>
</tr>
<tr>
<td>BOTTOM</td>
<td>1:1_DIFFPAIR</td>
<td>2:1_SPACING</td>
</tr>
</tbody>
</table>

### Source References

- **Source 1**: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5
- **Source 2**: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4
- **Source 3**: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

---

**Note**: The above content has been extracted from the page and formatted to maintain readability and coherence. The original page contains detailed tables and diagrams that are not transcribed here due to the limitations of the text representation. For a comprehensive understanding, refer to the original document.
Max trace length: 12 inches for SATA Gen1/Gen2, TBD for SATA Gen3.

SATA intra-pair matching should be 1 ps.

Max trace length: LVDS 10 inches, DP 8.5 inches.

DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.

DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 100 ps.

NOTE: NV DG recommends 90 ohm differential for LVDS, but cable/display assume 100 ohm.

50-ohm from first to second termination resistor.

37.5-ohm from MCP to first termination resistor.

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.4.1.

- = 100_OHM_DIFF

* = 3x_DIELECTRIC

= STANDARD

= 90_OHM_DIFF

= 50_OHM_SEC
<table>
<thead>
<tr>
<th>Interface</th>
<th>Constraints</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPI</td>
<td>SIO Signal Constraints, SPI Interface Constraints</td>
</tr>
<tr>
<td>HD Audio</td>
<td>SMBus Interface Constraints, USB 2.0 Interface Constraints</td>
</tr>
<tr>
<td>SMBus</td>
<td>USB 2.0 Interface Constraints</td>
</tr>
<tr>
<td>LPC Bus</td>
<td></td>
</tr>
</tbody>
</table>

**Notes:**
- **SMBUS_SMC_MGMT_SDA**
- **MCP_HDA_PULLDN_COMP**
- **HDA_RST_L**
- **HDA_BIT_CLK**
- **SMBUS_MCP_0_CLK**
- **USB_WM_P**
- **USB_EXTC_P**
- **USB_T57**
- **USB_IR**
- **USB_90D**
- **USB_TPAD_P**
- **USB_MINI**
- **LPC_FRAME_L**
- **LPC_RESET_L**
- **SPI_CS0_R_L**
- **SPI_55S**
- **SPI_MISO**
- **SPI_MOSI**
- **SPI_55S**
- **SPI_CLK**
- **HDA_55S**
- **SMB_55S**
- **USB_90D**
- **USB_55S**
- **CLK_LPC_55S**
- **LPC_55S**
### SMC SMBus Net Properties

<table>
<thead>
<tr>
<th>ELECTRICAL_CONSTRAINT_SET</th>
<th>MINIMUM</th>
<th>MAXIMUM</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>1.25 V</td>
<td>1.35 V</td>
</tr>
<tr>
<td>GND</td>
<td>0.0 V</td>
<td>0.0 V</td>
</tr>
</tbody>
</table>

### SMBus Charger Net Properties

<table>
<thead>
<tr>
<th>ELECTRICAL_CONSTRAINT_SET</th>
<th>MINIMUM</th>
<th>MAXIMUM</th>
</tr>
</thead>
<tbody>
<tr>
<td>CHGR_CSI_P</td>
<td>1.25 V</td>
<td>1.35 V</td>
</tr>
<tr>
<td>CHGR_CSI_N</td>
<td>1.25 V</td>
<td>1.35 V</td>
</tr>
<tr>
<td>CHGR_CSI_R_P</td>
<td>1.25 V</td>
<td>1.35 V</td>
</tr>
<tr>
<td>CHGR_CSI_R_N</td>
<td>1.25 V</td>
<td>1.35 V</td>
</tr>
<tr>
<td>CHGR_CSO_P</td>
<td>1.25 V</td>
<td>1.35 V</td>
</tr>
<tr>
<td>CHGR_CSO_N</td>
<td>1.25 V</td>
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### K87 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

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<th>Table Name</th>
<th>Layer</th>
<th>Min. Neck Width</th>
<th>Max. Neck Length</th>
<th>DiffPair PRIMARY</th>
<th>DiffPair NECK GAP</th>
<th>Physical Rule Set</th>
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#### BOARD LAYERS

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<tr>
<th>Layer Name</th>
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<th>Allow Route</th>
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<tbody>
<tr>
<td>TOP, BOTTOM</td>
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<td>0.091 MM</td>
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#### BOARD UNITS

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