SCHEM, BLACK_PEARL, MLB, K92

pre-evt 11/22/10 rev3.11.3

ALIASES RESOLVED
### Bar Code Labels / EEEE #’s

<table>
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<tr>
<th>PART NUMBER</th>
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<th>DESCRIPTION</th>
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<th>CRITICAL</th>
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### K92 Module Parts

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### K92 Programmed Parts—All Builds

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### Alternate Parts

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### EPC

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### Ethernet

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### PSoC

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---

The document contains detailed parts lists and descriptions for various components, including ICs, memory modules, and labels. Each part number is accompanied by a description of the component, its reference design, and whether it is critical or not. The BOM Configuration section includes a table with part numbers, descriptions, and references, indicating the type of documentation required for each part.
Intel is investigating processor driven VREF_DQ generation.
VAXG DECOUPLING

Intel recommendation: 2x 720uF 10mΩ, 2a 720uF 10mΩ (MOSFET), 6a 10uF 0603, 2a 10uF 0805 (MOSFET), 4a 1uF 0402, 2a 1uF 0402 (MOSFET), 2a 15uF 0603 (MOSFET)

Apple implementation: 2x 720uF 10mΩ, 2a 720uF 10mΩ (MOSFET), 4a 1uF 0402, 2a 1uF 0402 (MOSFET), 4a 10uF 0402, 2a 10uF 0402 (MOSFET), 4a 15uF 0603 (MOSFET)

PLACEMENT NOTE (C1700-C1708):

- Apple implementation: 2x 470uF 4mΩ, 1x 470uF 4mΩ (NOSTUFF), 6x 22uF 0603, 2x 22uF 0603 (NOSTUFF), 6x 10uF 0402, 2x 10uF 0402 (NOSTUFF)

- Intel recommendation: 2x 470uF 4mΩ, 2x 470uF 4mΩ (NOSTUFF), 6x 22uF 0805, 2x 22uF 0805 (NOSTUFF), 6x 10uF 0603, 2x 10uF 0603 (NOSTUFF), 9x 1uF 0402, 9x 1uF 0402 (NOSTUFF)

CPU VCCS VCCS

Apple implementation: in 300µF, 6a 15uF 0603, 6a 15uF 0603

Intel recommendation: in 10mΩ, 1% 10Ω, 6a 15uF 0603

PLACEMENT NOTE (C1714-C1742):

- Apple implementation: 2x 470uF 4mΩ, 1x 470uF 4mΩ (NOSTUFF), 6x 22uF 0603, 2x 22uF 0603 (NOSTUFF), 6x 10uF 0402, 2x 10uF 0402 (NOSTUFF)

- Intel recommendation: 2x 470uF 4mΩ, 2x 470uF 4mΩ (NOSTUFF), 6x 22uF 0805, 2x 22uF 0805 (NOSTUFF), 6x 10uF 0603, 2x 10uF 0603 (NOSTUFF), 9x 1uF 0402, 9x 1uF 0402 (NOSTUFF)
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

**NOTE:** In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert.

**IMPORTANT:** CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

<table>
<thead>
<tr>
<th>Step</th>
<th>ISOLATE_CPU_MEM_L</th>
<th>PLT_RESET_L</th>
<th>PM_SLP_S3_L</th>
<th>PM_SLP_S4_L</th>
<th>CPU_MEM_RESET_L</th>
<th>MEM_RESET_L</th>
<th>MEMVTT_EN</th>
<th>P1V5CPU_EN</th>
</tr>
</thead>
<tbody>
<tr>
<td>MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L</td>
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<tr>
<td>MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L</td>
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</tr>
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</table>

WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.

ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.

As isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

**1V5 S0 "PGOOD" for CPU**

**MEMVTT Clamp**

Ensures CKE signals are held low in S3

**CPU Memory S3 Support**

*Apple Inc.*

---

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---

**Drawings and Specifications:**

CPU Memory S3 Support

*Apple Inc.*

---

**Page Title:**

SYNC_MASTER=K17_MLB SYNCDATE=04/26/2010

---

**Revision:**

Andrew Levis

---

**Sheet:**

Apple Inc.
DAC step size: 7.69mV / step @ output

VRef current: +61μA - -61μA (- = sourced)

1.5V (DAC: 0x3A)

1.442V (+/ - 180mV)

1.056V - 1.267V (DAC: 0x8B)

8.59mV / step @ output

1.51mV / step @ output

NOTE: Must not enable more than two SO-DIMM margining buffers at once or VRef source may be overloaded.

NOTE: Must not enable more than two SO-DIMM margining buffers at once or VRef source may be overloaded.

PPVTT_DDR_BUF

PP3V3_S3_VREFMRGN

VREFMRGN_CTRL

VREFMRGN_DAC

MIN_NECK_WIDTH=0.2 mm

MIN_LINE_WIDTH=0.3 mm

Page Notes

DAC Channel:

PCA9557D Pin:

Nominal value

Margined target:

DAC range:

DAC step size:

DIGITAL IO

LOGIC LEVELS

POWER SUPPLIES

SIGNAL GROUND

SHEETS

REV

DRAWING NUMBER

REV

SHEET

ORDERING INFORMATION

Product

Part Number

Description

Supply Voltage

Maximum Operating Frequency

Operating Temperature Range

Packaging

Article

Total Page Count

Document Name

Abstract

Introduction

Specifications

Electrical Characteristics

Functional Description

Interfacing

Applications

Test Equipment

Test Conditions

Test Results

Test Circuit

Appendices

References

Appendix A

Appendix B

Appendix C

Appendix D

Revision History

Legal Notice

www.vinafix.vn
Transformers should be mirrored on opposite sides of the board.

Place one of 0.1uf cap close to each centertap pin of transformer.

---

**Diagram Notes:**

- **Page Notes:**
  - Page notes required by this page:
  - Page notes required by this page:
  - Non-essential notes provided by this page:

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- **Sheet and Drawing Information:**
  - Branch: 36
  - Revision: 96
  - Drawing Number: 345678
  - Sheet: 2 1

- **BOM Options Provided by This Page:**
  - Place one of 0.1uf cap close to each centertap pin of transformer.

- **Power Aliases Required by This Page:**
  - Transformer should be mirrored on opposite sides of the board.

- **Signal Aliases Required by This Page:**
  - (NONE)

- **Placement Instructions:**
  - Transformers should be mirrored on opposite sides of the board.
  - 0.1uf cap close to each centertap pin of transformer.

---

**Legend:**

- **Ethernet Connector:**
  - ENET_MDI_P<0>
  - ENET_MDI_N<0>
  - ENET_MDI_P<1>
  - ENET_MDI_N<1>
  - ENET_MDI_P<2>
  - ENET_MDI_N<2>
  - ENET_MDI_P<3>
  - ENET_MDI_N<3>
  - ENETCONN_CTAP2
  - ENETCONN_P<0>
  - ENETCONN_N<0>
  - ENETCONN_P<1>
  - ENETCONN_N<1>
  - ENETCONN_P<2>
  - ENETCONN_N<2>
  - ENETCONN_CTAP1
  - ENETCONN_P<3>
  - ENETCONN_CTAP0
  - ENET_CONN_CTAP
  - CRITICAL

---

**References:**

- [www.vinafix.vn](http://www.vinafix.vn)
FireWire Port Power Switch

- FW_PME_L
- PP1V0_FW_FWPHY (PHY 1.0V)
- PP1V05_FW_P1V0FWFET (1.0V FET Input)
- PP1V05_S0_FWPWRCTL (5KPD Bias Rail)
- PP3V3_FW_FET (3.3V FET Output)
- PPBUS_S5_FWPWRSW (FW VP FET Input)

Power aliases required by this page:

Page Notes

IN 39 45 68 70 73 102 104
PP1V05_S0 FW_PWR_EN

R4275 1
1K

402

Q4275 CRITICAL SOT-563 DMB53D0UV

BC847CDXV6TXG

Current source only active when FW_PWR_EN is low.
Host can detect as load on TPBIAS signal.

All FireWire devices require 5K pull-down on TPB pair.

FireWire Port 5K Pull-Down Detect

All Firewire devices require 5K pull-down on TPB pair.
Host can detect as load on TPBIAS signal.
Current source only active when FW_PWR_EN is low.

FireWire PHY WAKE# Support

When PHY is powered, FW_PHY_DET_L acts as legacy PME# signal.

Dual-purpose output:
1) SW pull-down detect when FW_PHY_DET is low.
2) PHY_WAKE# (FW/#) when PHY is powered.
Pull-up is provided on another page.

3.3V FW Switch

U4201 & U4202

1.0V Switch

R4260 1
1/16W

R4261

1/16W

402

402

MF-LF

MF-LF

FDC638P_G

CRITICAL Q4260

Pull-up provided on another page.

2) FW643 WAKE# (PME#) when PHY is powered.
1) 5K Pull-down Detect when FW_PWR_EN is low.

Dual-purpose output:
1) SW pull-down detect when FW_PHY_DET is low.
2) PHY_WAKE# (FW/#) when PHY is powered.
Pull-up is provided on another page.

FireWire Port & PHY Power

Apple Inc.

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SYNC_MASTER=K91_MLB SYNC_DATE=10/20/2010

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www.vinafix.vn
FW643 TPCPS Leakage Protection

FW643 has internal leakage path from TPCPS pin to VCC93. FET blocks current to TPCPS until VCC93 is powered.

Unused FireWire Ports

Disable per LSI instructions
(All unused port signals TP/NC)

FireWire PHY Config Straps

Configures PHY for:
- Port "1" Bilingual (1394B)
- Port TP/NC (1394A)

Termination

Place close to FireWire PHY

Cable Power

Input Power Note: Trace PP3V3_FW_FWPHY must handle up to 5A

"Snapback" & "Late VC" Protection

U4330 TPCPS394

PORT 1

SIGNALS

SYNC_DATE=07/22/2010

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PAGE TITLE

SYNC_MASTER=K91_MLB

PAGE Notes

Power alias required by this page:
- FW_PHY_DS2
- FW_PHY_DS1
- FW_PHY_DS0

Signal aliases required by this page:
- PP3V3_FW_FWPHY

BOM options provided by this page:
- FW_PHY_DS1
- FW_PHY_DS2
- FW_PHY_DS0

NOTE: This page is expected to contain references to signal aliases and notes that are not visible in this format.
USB Port Power Switch

Left USB Port A

Current limit per port (R4600): 2.18A min / 2.63A max

USB/SMC Debug Mux

Left USB Port B

External USB Connectors

Apple Inc.

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USB Port Power Switch

Current limit (R4700): 2.19A min / 2.76A max
Keyboard Backlight Driver & Detection

To detect keyboard backlight, DMC will tristate and read SMC_SYS_KBDLED:
- IF LOW, keyboard backlight present
- IF HIGH, keyboard backlight not present
- R5853 always stuffed, R5854 only grounded when KB BL flex connected.

BOOSTER +18.5VDC FOR SENSORS

BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
- DROP LINE REGULATION
- SIMPLE TO MOUNT AND WIRE
- EMI - BUS APPROX. 10X SENSITIVITY
- START UP TIME LESS THAN 1MS
- R5812, R5813, C5818 MODIFIED
- STARTUP TIME LESS THAN 2MS
- 100-300KHZ CLEAN SPECTRUM
- RIPPLE TO MEET ERS
- DROOP LINE REGULATION
- POWER CONSUMPTION

BOOSTER DESIGN CONSIDERATION:
- BOOSTER +18.5VDC FOR SENSORS
- VOLTAGE = 5V MIN
- NECK_WIDTH = 0.20MM
- MIN_LINE_WIDTH = 0.50MM

- IPD Flex Connector
- Keyboard Backlight Connector
Digital Accelerometer

Apple Inc.

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SYNC_DATE=06/02/2010
SYNC_MASTER=K92_DINESH

Desired orientation when placed on board bottom-side (view thru top):

Front of system

Circle indicates pin 1 location when placed in correct orientation.

SMS_ADDR_SELECT=1 Addr: 0x32(Wr)/0x33(Rd)
SMS_ADDR_SELECT=0 Addr: 0x30(Wr)/0x31(Rd)

NOTE: SDA and SCL have internal pull-ups to VDD_IO.
CPU VCCIO (1.05V S0) Regulator

OCP = R7641 x 8.5uA / R7640
OCP = 25.6A
Vout = 0.5V * (1 + Ra / Rb)

Vout = 1.05V
f = 300 kHz
LCD (LVDS) INTERFACE

- Panel has 2K pull-ups
- 100K pull-ups are for no-panel case (development)
- Place close to the connector

**Components:**
- DLP11S 90-OHM-100MA
- CRITICAL
- L9000
- DLP11S 90-OHM-100MA
- CRITICAL
- L9010
- L9011
- CRITICAL
- F-RT-SM 20474-040E-11

**Connectors:**
- LVDS Display Connector
- PP3V3_SW_LCD
- VOLTAGE=3.3V
- MIN_NECK_WIDTH=0.25 mm
- MIN_LINE_WIDTH=0.5 mm

**Other Details:**
- LVDS DDC_CLK
- LVDS_CONN_A_DATA_N<0>
- LVDS_CONN_A_DATA_P<0>
- LVDS_CONN_B_CLK_F_P
- LVDS_CONN_B_CLK_N
- LVDS_CONN_B_CLK_P
- LVDS_CONN_B_DATA_N<0>
- LVDS_CONN_A_DATA_P<2>
- LVDS_CONN_A_DATA_N<2>
- LVDS_CONN_A_DATA_N<1>
- LVDS_CONN_B_DATA_P<1>
- LVDS_CONN_B_DATA_P<0>
- LVDS_CONN_A_CLK_F_P
- LVDS_CONN_A_CLK_F_N
- LVDS_CONN_A_DATA_P<1>
- PPVOUT_S0_LCDBKLT

**Miscellaneous:**
- 100VX7R 603
- MIN_LINE_WIDTH=0.5 mm
- VOLTAGE=3.3V
- MIN_NECK_WIDTH=0.2 mm
GPU Rail Sequencing

unused PGOOD signal

CPUIMVP_AXG_PGOOD

PP3V3_S0

MAKE_BASE=TRUE

TP_P1V5S3RS0_RAMP_DONE

TP_DDRREG_PGOOD

MAKE_BASE=TRUE

GPUVCORE_EN

P1V8GPU_EN

MAKE_BASE=TRUE

P1V0GPU_EN

MAKE_BASE=TRUE

P3V3GPU_EN

MAKE_BASE=TRUE

P1V5FB1V8GPU_R_EN

MAKE_BASE=TRUE

PM_PCH_PWROK

PP3V3_S5

PM_ALL_GPU_PGOOD

PM_ALL_GPU_PGOOD

PM_ALL_GPU_PGOOD

PM_ALL_GPU_PGOOD

CPUIMVP_PGOOD

PM_PCH_SYS_PWROK

ALL_SYS_PWRGD

6 7 12 23 25 26 28 32 35 36 39 40 41 46

48 49 50 51 52 54 57 61 62 72 73 80 83

84 85 88 89 91 100 102

6 7 17 19 20 22 23 24 25 29 46 48 56 71

72 73 83 86 100 102 104

17 91

www.vinafix.vn
Some signals require 27.4-ohm single-ended impedance. Most CPU signals with impedance requirements are 50-ohm single-ended.
Memory Bus Constraints

- Memory Data to Memory Data
  - spacing: 50 Ohm SE
  - spacing: 72 Ohm DIFF
- Memory Control to Memory Control
  - spacing: 50 Ohm SE
  - spacing: 72 Ohm DIFF
- Memory Ctrl to Memory Data
  - spacing: 85 Ohm DIFF
- Memory Command to Memory Control
  - spacing: 50 Ohm SE

Memory Net Properties

- Memory Data to Memory Data
  - spacing: 50 Ohm SE
  - spacing: 72 Ohm DIFF
- Memory Control to Memory Control
  - spacing: 50 Ohm SE
  - spacing: 72 Ohm DIFF
- Memory Command to Memory Control
  - spacing: 85 Ohm DIFF

Memory Bus Spacing Group Assignments

- DDR3: Signals should be matched within 0.50mm of associated DQS pair.
- DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.
- DQS to clock matching should be within [CLK-0.127mm] and [CLK+0.127mm].
- CLK inter-pair matching should be within 0.127mm, inter-pair matching should be within 0.508mm.
- DQS to MEM_DATA, MEM_CTRL, or MEM_CMD should be matched within [MEM_CLK-0.127mm] to [MEM_CLK+0.127mm] of the pair.
- DQS to MEM_DATA should be matched within [MEM_CLK-0.127mm] to [MEM_CLK+25.4mm] of the pair.

Source: Calpella 3F Platform SG, Rev 1.5 (#D072066), Section 2.5
### Digital Video Signal Constraints

<table>
<thead>
<tr>
<th>Source</th>
<th>Constraints</th>
<th>Min Width</th>
<th>Max Width</th>
<th>Min Length</th>
<th>Max Length</th>
<th>Gap Width</th>
<th>Gap Height</th>
</tr>
</thead>
</table>

### SATA Interface Constraints

<table>
<thead>
<tr>
<th>Source</th>
<th>Constraints</th>
<th>Min Width</th>
<th>Max Width</th>
<th>Min Length</th>
<th>Max Length</th>
<th>Gap Width</th>
<th>Gap Height</th>
</tr>
</thead>
</table>

### USB 2.0 Interface Constraints

<table>
<thead>
<tr>
<th>Source</th>
<th>Constraints</th>
<th>Min Width</th>
<th>Max Width</th>
<th>Min Length</th>
<th>Max Length</th>
<th>Gap Width</th>
<th>Gap Height</th>
</tr>
</thead>
</table>

### PCH Net Properties

<table>
<thead>
<tr>
<th>Source</th>
<th>Constraints</th>
<th>Min Width</th>
<th>Max Width</th>
<th>Min Length</th>
<th>Max Length</th>
<th>Gap Width</th>
<th>Gap Height</th>
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</thead>
</table>

### PCH Constraints 1

Source: HR Platform Design Guide, Tables 191, 193
### SMBus Interface Constraints

<table>
<thead>
<tr>
<th>Constraint</th>
<th>Constraint Type</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>LPC_RESET_L</td>
<td>LPC_50S</td>
<td>1</td>
</tr>
<tr>
<td>LPC_FRAME_L</td>
<td>LPC_50S</td>
<td>1</td>
</tr>
<tr>
<td>LPC_AD</td>
<td>LPC_50S</td>
<td>1</td>
</tr>
</tbody>
</table>

### LPC Bus Constraints

<table>
<thead>
<tr>
<th>Constraint</th>
<th>Constraint Type</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>LPC_RESET_L</td>
<td>LPC_50S</td>
<td>1</td>
</tr>
<tr>
<td>LPC_FRAME_L</td>
<td>LPC_50S</td>
<td>1</td>
</tr>
<tr>
<td>LPC_AD</td>
<td>LPC_50S</td>
<td>1</td>
</tr>
</tbody>
</table>

### HD Audio Interface Constraints

<table>
<thead>
<tr>
<th>Constraint</th>
<th>Constraint Type</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>HDA_EXPRISON</td>
<td>HDA</td>
<td>1</td>
</tr>
<tr>
<td>HDA_SDOUT</td>
<td>HDA</td>
<td>1</td>
</tr>
<tr>
<td>HDA_RST_L</td>
<td>HDA</td>
<td>1</td>
</tr>
<tr>
<td>HDA_SYNC</td>
<td>HDA</td>
<td>1</td>
</tr>
<tr>
<td>HDA_BIT_CLK</td>
<td>HDA</td>
<td>1</td>
</tr>
</tbody>
</table>

### SPI Interface Constraints

<table>
<thead>
<tr>
<th>Constraint</th>
<th>Constraint Type</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPI_MISO</td>
<td>SPI_55S</td>
<td>1</td>
</tr>
<tr>
<td>SPI_MOSI</td>
<td>SPI_55S</td>
<td>1</td>
</tr>
<tr>
<td>SPI_CLK</td>
<td>SPI_55S</td>
<td>1</td>
</tr>
</tbody>
</table>

### PCH Net Properties

<table>
<thead>
<tr>
<th>Net</th>
<th>Property</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>SMBUS_PCH_0_CLK</td>
<td>SMB_50S</td>
<td>1</td>
</tr>
<tr>
<td>LPC_RESET_L</td>
<td>LPC_50S</td>
<td>1</td>
</tr>
<tr>
<td>LPC_FRAME_L</td>
<td>LPC_50S</td>
<td>1</td>
</tr>
<tr>
<td>LPC_AD</td>
<td>LPC_50S</td>
<td>1</td>
</tr>
<tr>
<td>PCH_CLK14P3M_REFCLK</td>
<td>PCH_CLK96M_DOT_N</td>
<td>1</td>
</tr>
<tr>
<td>PCH_CLK33M_PCIIN</td>
<td>PCH_CLK33M_SMC_R</td>
<td>1</td>
</tr>
<tr>
<td>PCIE_CLK100M_T29_P</td>
<td>PCIE_CLK100M_PCH_P</td>
<td>1</td>
</tr>
<tr>
<td>PCIE_CLK100M_ENET_P</td>
<td>PCIE_CLK100M_ENET_P</td>
<td>1</td>
</tr>
<tr>
<td>PCIE_CLK100M_FW_P</td>
<td>PCIE_CLK100M_FW_P</td>
<td>1</td>
</tr>
<tr>
<td>PCIE_ENET_R2D_N</td>
<td>PCIE_ENET_D2R_N</td>
<td>1</td>
</tr>
</tbody>
</table>
CAESAR II (Ethernet) Constraints

Ethernet Net Properties

Ethernet/FW Constraints

FireWire Interface Constraints

FireWire Net Properties

Port 0 and 2 Not Used

SOURCE: Broadcom 5764-DS04-RDS Page 38

FireWire Net Properties

Port 0 and 2 Not Used

SOURCE: Broadcom 5764-DS04-RDS Page 38
## DisplayPort Signal Constraints

**NOTE:** DisplayPort Physical/Spacing Constraints provided by Chipset or ODP page.

### T29 I2C Signal Constraints

<table>
<thead>
<tr>
<th>Layer</th>
<th>Min Width</th>
<th>Max Width</th>
<th>Diff Primary</th>
<th>Diff Neck</th>
<th>Neck Gap</th>
</tr>
</thead>
<tbody>
<tr>
<td>I2C</td>
<td>100 μm</td>
<td>200 μm</td>
<td>100 μm</td>
<td>200 μm</td>
<td>100 μm</td>
</tr>
</tbody>
</table>

### T29 DP Connector Signal Constraints

<table>
<thead>
<tr>
<th>Layer</th>
<th>Min Width</th>
<th>Max Width</th>
<th>Diff Primary</th>
<th>Diff Neck</th>
<th>Neck Gap</th>
</tr>
</thead>
<tbody>
<tr>
<td>DP</td>
<td>50 μm</td>
<td>100 μm</td>
<td>50 μm</td>
<td>100 μm</td>
<td>50 μm</td>
</tr>
</tbody>
</table>

---

**SOURCE:** Bill Cornelius’ T29 Routing Notes

---

### T29 IC Net Properties

<table>
<thead>
<tr>
<th>Electrical Constraint</th>
<th>Min Width</th>
<th>Max Width</th>
<th>Diff Primary</th>
<th>Diff Neck</th>
<th>Neck Gap</th>
</tr>
</thead>
<tbody>
<tr>
<td>I2C</td>
<td>100 μm</td>
<td>200 μm</td>
<td>100 μm</td>
<td>200 μm</td>
<td>100 μm</td>
</tr>
</tbody>
</table>

**only used on hosts supporting T29 video-in**

---

**SOURCE:** Bill Cornelius’ T29 Routing Notes

---

## T29/DP Net Properties

<table>
<thead>
<tr>
<th>Electrical Constraint</th>
<th>Position</th>
<th>Min Width</th>
<th>Max Width</th>
<th>Diff Primary</th>
<th>Diff Neck</th>
<th>Neck Gap</th>
</tr>
</thead>
<tbody>
<tr>
<td>DP</td>
<td>I2C</td>
<td>100 μm</td>
<td>200 μm</td>
<td>100 μm</td>
<td>200 μm</td>
<td>100 μm</td>
</tr>
</tbody>
</table>

**only used on dual-port hosts.**

---

**SOURCE:** Bill Cornelius’ T29 Routing Notes

---

## T29 Constraints

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**SYNC_DATE=10/20/2010**

**SYNC_MASTER=T29_REF**

---

**DRAWING NUMBER SIZE**

- 97 OF 105
- 97 OF 105
### GDDR5 Frame Buffer Signal Constraints

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Signal Type</th>
<th>Signal Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>GDDR5_45R5</td>
<td>LVDS</td>
<td>85_OHM_DIFF</td>
</tr>
<tr>
<td>GDDR5_EDC</td>
<td>LVDS</td>
<td>85_OHM_DIFF</td>
</tr>
<tr>
<td>DP_85D</td>
<td>LVDS</td>
<td>85_OHM_DIFF</td>
</tr>
</tbody>
</table>

* LVDSCONN

#### Digital Video Signal Constraints

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Signal Type</th>
<th>Signal Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>GDDR5_FB_A</td>
<td>LVDS</td>
<td>85_OHM_DIFF</td>
</tr>
<tr>
<td>GDDR5_FB_B</td>
<td>LVDS</td>
<td>85_OHM_DIFF</td>
</tr>
</tbody>
</table>

#### GDDR5 FB A Net Properties

<table>
<thead>
<tr>
<th>Net Name</th>
<th>Net Type</th>
<th>Propagation Delays</th>
</tr>
</thead>
<tbody>
<tr>
<td>FB_A0_EDC3</td>
<td>LVDS</td>
<td>GDDR5_EDC, GDDR5_45R5</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
<td>...</td>
</tr>
</tbody>
</table>

#### GDDR5 FB B Net Properties

<table>
<thead>
<tr>
<th>Net Name</th>
<th>Net Type</th>
<th>Propagation Delays</th>
</tr>
</thead>
<tbody>
<tr>
<td>FB_B0_EDC2</td>
<td>LVDS</td>
<td>GDDR5_EDC, GDDR5_45R5</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
<td>...</td>
</tr>
</tbody>
</table>
### Memory Constraint Relaxations

Allow 0.127 mm width for 0.127 mm lines for AGP fanout.

<table>
<thead>
<tr>
<th>Project Specific Constraints</th>
<th>Memory Constraint Relaxations</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>A</td>
</tr>
<tr>
<td></td>
<td>B</td>
</tr>
<tr>
<td>Alternate different layout</td>
<td>through AGP fanout area (in the diff)</td>
</tr>
<tr>
<td></td>
<td>C</td>
</tr>
<tr>
<td></td>
<td>D</td>
</tr>
</tbody>
</table>

### Graphics, SATA Constraint Relaxations

Alternate different layout through SATA fanout area (in the diff)

<table>
<thead>
<tr>
<th>Project Specific Constraints</th>
<th>Graphics, SATA Constraint Relaxations</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>A</td>
</tr>
<tr>
<td></td>
<td>B</td>
</tr>
<tr>
<td></td>
<td>C</td>
</tr>
<tr>
<td></td>
<td>D</td>
</tr>
</tbody>
</table>

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<table>
<thead>
<tr>
<th>Section</th>
<th>Description</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>PCB Rule Definitions</td>
<td></td>
</tr>
<tr>
<td>B</td>
<td>Table_Physical_Rule_High</td>
<td></td>
</tr>
<tr>
<td>C</td>
<td>Table_Physical_Rule_Head</td>
<td></td>
</tr>
<tr>
<td>D</td>
<td>Table_Physical_Rule_Item</td>
<td></td>
</tr>
</tbody>
</table>

**NOTE:** Based on K92 mm stackup.
Page Title

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