2. All capacitance values are in microfarads.

1. All resistance values are in ohms, 0.1 watt +/- 5%.
### Phantom BOM #'s

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>REFERENCE DES</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>341S1813</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>341S1814</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Module Parts**

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>REFERENCE DES</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1_DEBUG</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M1_DEBUG</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**"LeMenu Stage #1" Parts**

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>REFERENCE DES</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>341S1812</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>341S1813</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**"LeMenu Stage #2" Parts**

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>REFERENCE DES</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>341S1813</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>341S1814</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**"LeMenu Stage #3" Parts**

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>REFERENCE DES</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>341S1813</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>341S1814</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Chassis connection to be made at the mounting hole northwest of the DVI connector

Chassis connection to be made at the mounting hole southwest of the USB connector

Chassis connection to be made at the mounting hole east of the LVDS connector
www.vinafix.vn
CPU 2 OF 2-PWR/GND

NOTICE OF PROPRIETARY PROPERTY

The possession and/or disclosure of this document, and the information contained therein, is the proprietary property of Apple Computer, Inc. The possession of this document, and the information contained therein, is the proprietary property of Apple Computer, Inc. The notice of proprietary property shall not be removed or altered by any person or organization.

This diagram contains confidential and proprietary information and is intended for use by authorized personnel only. Unauthorized disclosure or reproduction is strictly prohibited.

STUB. TO TP_VSSSENSE WITH NO LAYOUT NOTE: CONNECT R0803 (3 OF 4)

CPU

BGA

VCCP_14

VCCP_11

VCCP_6

VCCP_5

VCCP_9

VCCP_8

VCCP_4

VCCP_3

VCCP_2

VCCP_1

VCCP_0

VCCSENSE_P

VCCSENSE_N

CPU_VID<6>

CPU_VID<5>

CPU_VID<4>

CPU_VID<3>

CPU_VID<2>

CPU_VID<1>

=PP1V5_S0_CPU

100

402

MF-LF

1/16W

OUT

OUT

OUT

OUT

ZO=27.4 OHM DIFFERENTIAL TRACE ROUTING.

IF NO USE, NEED PULL-UP OR

VCCA=1.5 ONLY

RESISTORS TERMINATE THE 55 OHM

BETWEEN VCCSENSE AND VSSSENSE AT THE

TO CONNECT A DIFFERENTIAL PROBE

PROVIDE A TEST POINT (WITH NO STUB)

www.vinafix.vn

81
CPU VCORE HF AND BULK DECOUPLING

- 4x 470μF, 20x 22μF 0805

VCCA (CPU AVdd) Decoupling

- 1x 10μF, 1x 0.01μF

VCCP (CPU I/O) Decoupling

- 4x 470μF, 6x 22μF 0805

NOTE: This cap is shared between CPU and NB.

CPU VCORE VID Connections

- Resistors to allow for override of CPU VID
- Will probably be removed before production

CPU_VID<6>
CPU_VID<5>
CPU_VID<4>
CPU_VID<3>
CPU_VID<2>
CPU_VID<1>
CPU_VID<0>

SYNC_MASTER=(MASTER)
SYNC_DATE=(MASTER)
CPU ZONE THERMAL SENSOR

- PLACE U1001 NEAR THE U1200
- ADD GND GUARD TRACE
- ROUTE CPU_THERMD_P AND CPU_THERMD_N ON SAME LAYER.
- 10 MIL TRACE
- 10 MIL SPACING
- PLACEHOLDER ADT7461A
- CPU_THERMD_N (TO CPU INTERNAL THERMAL DIODE)
CPU ITP700FLEX DEBUG SUPPORT

ITP TCK SIGNAL LAYOUT NOTE: ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX CONNECTOR'S FBO PIN.

NOTE: ITP IS USING TAP I/F, HC IN 945GM CHIPSET SYSTEM, AND WITH SYSTEM RESET LOGIC.
<table>
<thead>
<tr>
<th>Output</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CRT_IREF</td>
<td>CRT_DDC_CLK</td>
</tr>
<tr>
<td>CRT_RED_L</td>
<td>CRT_RED</td>
</tr>
<tr>
<td>CRT_GREEN</td>
<td>CRT_BLUE_L</td>
</tr>
<tr>
<td>CRT_BLUE</td>
<td>CRT_GREEN*</td>
</tr>
<tr>
<td>TV_IRTNC</td>
<td>TV_IRTNB</td>
</tr>
<tr>
<td>TV_IRTNA</td>
<td>TV_IFREF</td>
</tr>
<tr>
<td>TV_DACC_OUT</td>
<td>LB_DATA2</td>
</tr>
<tr>
<td>LVDS_B_DATA_P&lt;2&gt;</td>
<td>LVDS_B_DATA_P&lt;1&gt;</td>
</tr>
<tr>
<td>LVDS_B_DATA_P&lt;0&gt;</td>
<td>LVDS_A_DATA_P&lt;1&gt;</td>
</tr>
<tr>
<td>LVDS_A_CLK_N</td>
<td>LVDS_VREFL</td>
</tr>
<tr>
<td>LVDS_VREFH</td>
<td>LVDS_VDDEN</td>
</tr>
<tr>
<td>LVDS_CLKCTLB</td>
<td>LVDS_CLKCTLA</td>
</tr>
<tr>
<td>LVDS_BKLTEN</td>
<td>LVDS_BKLTCTL</td>
</tr>
</tbody>
</table>

**VDD Disable**

For some PCI signals NC if VDD is not implemented. Tie VCC_TVOUT and VCC_AVS to GND. If AVO is used VCC_AVS and VCC_TVOUT are powered with proper decoupling. Otherwise, tie VCC_TVOUT to GND also.

**CRT Disable**

VCCA_TVBG to 1.5V power rail. Tie VSSA_TVBG to GND.

**TV-Out Disable**

Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and DACx_OUT, IRTNx, and IREF to 1.5V power rail.

**Composite: DACA only**

VCCD_LVDS must remain powered with proper decoupling.
Layout Note:
Place near pin BA15

0.47uF CERM-X5R

Speed
660MHz 1 Channel 2 Channel
530MHz 1500mA 2400mA
400MHz 1300mA 2400mA

1.8V Max Current

IMPACTING PART PERFORMANCE.

www.vinafix.vn
The reference voltage must be provided.

I2C_SODIMMA_SDA

Signal aliases required by this page:

- PP1V8_S3_MEM

Power aliases required by this page:

- MEM_VREF
- C2800 0.1uF
- C2846 20%
- 22.4 10V
- C2818 0.1uF
- C2813 0.1uF
- C2812 0.1uF
- 22.4 10V
- 0.1uF

=I2C_SODIMMA_SCL

"Upper" (surface-mount) slot

DDR2 Bypass Caps

(For return current)

C2808 10UF
C2809 10UF
C2810 10UF
C2811 10UF
C2812 10UF
C2813 10UF
C2814 10UF
C2815 10UF
C2816 10UF
C2817 10UF
C2818 10UF
C2819 10UF
C2820 10UF
C2821 10UF

DDR2 SO-DIMM Connector A

APPLE COMPUTER INC.

NOTICE OF PROPRIETARY PROPERTY

NOT TO REPRODUCE OR COPY IT

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

AGREES TO THE FOLLOWING

REV. 07001

II NOT TO REPRODUCE OR COPY IT
One cap for each side of every RPAK, one cap for every two discrete resistors

Ensure CS_L and ODT resistors are close to SO-DIMM connector
Memory Vtt Supply

- =PP5V_S0_MEMVTT
- =PP1V8_S0_MEMVTT
- =PP0V9_S0_MEMVTT_LDO

Okay to turn off 5V and leave 1.8V powered in S3.

If power inputs are not S0, MEMVTT_EN can be used to disable MEMVTT in sleep.

Component Details:

- **R3100**: 1K, 5%, 1/16W, MF-LF, 402
- **C3100**: 1uF, CERM, 10%, 6.3V
- **C3101**: 10uF, X5R, 603
- **C3102**: 6.3V, 10uF, X5R, 603
- **C3103**: 0.1uF, X5R, 16V, 10%
- **C3104**: 2.2uF, CERM, 10%, 6.3V
- **C3105**: 150UF, 20%, POLY, SMC-LF, 6.3V

**Notes:**
- DDR2 Vtt Regulator
- SYNC_MASTER=(MASTER)
- SYNC_DATE=(MASTER)
- MIN_LINE_WIDTH=0.2 mm
- MIN_NECK_WIDTH=0.2 mm
- VOLTAGE=1.8V
- CMOS

WWW.VINAFIX.VN
NOTICE OF PROPRIETARY PROPERTY

I AGREE TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
III NOT TO REPRODUCE OR COPY IT

PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY
Port Power Switch

- FWPWR_PWRON
- FWPWR_ACIN
- FWPWR_EN
- FWPWR_RUN

FireWire Port Current Sense

- PPBUS_S0_FW_PORTPWRSW
- PPBUS_S5_FWPWRSW
- PPBUS_S5_FW_FET
- PPBUS_S5_FW_FET_D
- PPBUS_S5_FW_FET_D_R
- PPBUS_S5_FW_FET_D_L

FireWire Port Power

- SMC_ADAPTER_EN
- FW_PWRSW

- MIN_NECK_WIDTH=0.2 mm
- MIN_LINE_WIDTH=0.2 mm
- VOLTAGE=12.6V

- MIN_NECK_WIDTH=0.25 mm
- MIN_LINE_WIDTH=0.5 mm
- VOLTAGE=12.6V
FireWire Design Guide (FWDG 0.6, 5/14/03)

**BOM options provided by this page:**
- Properly terminate unused signals.
- Use appropriate connectors and/or to FireWire TPA/TPB pairs to their necessary aliases to map the signal.
- Place close to FireWire PHY.

**NOTE:** This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

**Signal aliases required by this page:**
- =GND_CHASSIS_FW_PORT1
- =PP3V3_S5_FWLATEVG

**Power aliases required by this page:**
- =PPFW_PORT1
- =PPFW_PORT1_VP
- =PPFW_PORT1_VP
- =VCC_FW_PORT1

**Late-VG Protection Power**

**FW Power Class Strap**

**Cable Power**
Port Power Switch

Right USB Port

Place L5200, L5205 and L5206 across moat

External USB Connector

---

NOTICE OF PROPRIETARY PROPERTY

I agree to the following:

I agree to maintain the Document in Confidence
I agree not to reveal or publish in whole or part
I agree not to reproduce or copy it

property of Apple Computer, Inc. the posessor

I agree that the Information contained herein is the proprietary

---

www.vinafix.vn
PCI-E x1 Port "A" = Ethernet (Yukon)
PCI-E x1 Port "B" = PCI-E Mini Card
PCI-E x1 Port "C" = ExpressCard
PCI-E x1 Port "D" = Unused
PCI-E x1 Port "E" = Unused
PCI-E x1 Port "F" = Unused
R6303 SHOULD BE PLACED LESS THAN 100 MILS FROM FLASH ROM

R6307 AND R6306 SHOULD BE PLACED LESS THAN 100 MILS FORM ICH7M

R6309 IS NOT NEEDED WHEN SHARING SPI FLASH WITH ICH7M AND TERCOM(LAN CHIP)
Left ALS "Connector"

Keyboard LED Driver

Right ALS Circuit

ALS Support
PAGE NOTES

INPUT
-3V3V, 3.3V power for SMS (STATE ALIVE IN SLEEP)
SMS_ONOFF_L - CONNECT TO SMC TO BE ABLE TO PUT SMS INTO LOW-POWER MODE

OUTPUT
SMS_ACC_X_AXIS - ACCELEROMETER OUTPUT TO SMC

PAGE HISTORY
5/19/2005 - FIRST REVISION OF PAGE
7/26/2005 - REMOVED BOM TABLE AND UPDATED SYMBOL TO KXM52-2050
7/26/2005 - CONNECTED PD PIN TO SMC'S SMS_ONOFF_L

SMS_ACC_SELFTEST - SHOULD BE PULLED HIGH WHEN NOT USED
SMS_ONOFF_L - CONNECT TO SMC TO BE ABLE TO PUT SMS INTO LOW-POWER MODE
SMS_X_AXIS - 3.3V POWER FOR SMS (STAYS ALIVE IN SLEEP)
SMS_X_AXIS - SMS X AXIS
SMS_Y_AXIS - SMS Y AXIS
SMS_Z_AXIS - SMS Z AXIS

Desired Orientation
(Placed on board topside)
Package Top

NOTICE OF PROPRIETARY PROPERTY
I AGREE TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
III NOT TO REPRODUCE OR COPY IT

PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR

REV.
APPLE COMPUTER INC.
2.5V S3 Regulator

- Connect RUNSS off-page to control.
  If unconnected, powers up with PVIN.

1.2V S3 Regulator

- Connect SHDNRT off-page to control.

Vout = 0.8V * (1 + Ra / (Rb + Rc))
3.425V "G3Hot" Supply

Supply needs to guarantee 3.3V delivered to SMC VRref generator

\[ V_{\text{out}} = 3.425 \text{V} \]

200mA max output (Switcher limit)

\[ V_{\text{out}} = 1.25V \times (1 + \frac{R_a}{R_b}) \]

Vout = 3.425

www.vinafix.vn
Left I/O Power Connector

Battery Connector (Digital Signals)

---

NOTICE OF PROPRIETARY PROPERTY

I AGREE TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
I NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
I NOT TO REPRODUCE OR COPY IT

PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR

The information contained herein is the proprietary

PBus-In & Battery Connectors

SYNC_DATE=(MASTER)
SYNC_MASTER=(MASTER)

APPLE COMPUTER INC.
63 81
051-6941 07001

SMC_BS_ALRT_L = SMBUS_BATT_SCL
SMC_BS_ALRT_H = SMBUS_BATT_SDA
GND_BATT = PPBUS_G3H_LIO_CONN

---

www.vinafix.vn
**GDDR3 Frame Buffer A**

The device on this page is GDDR3 Frame Buffer A, which is used in various Apple products. It is a memory interface chip designed to communicate with the GPU and other components in the system.

### Notice of Proprietary Property

The device is protected by a Notice of Proprietary Property, indicating that it contains intellectual property rights.

### Device Description

The diagram illustrates the connections and signals involved in the operation of the GDDR3 Frame Buffer A. It shows various pins, signals, and their interconnections, which are crucial for the proper functioning of the device.

### Software Considerations

The diagram highlights the importance of software in managing the configuration and operation of the device. Bits within byte-lane need to be swapped as indicated in the diagram, and software must know how these bits are mapped for proper support within the GPU device.

### Specifications

- **Pad Values:**
  - **I/O:** Various pins marked as I/O
  - **CS:** Chip Select
  - **RAS:** Row Address Strobe
  - **CAS:** Column Address Strobe
  - **CLK:** Clock Signal
  - **DQ:** Data Output
  - **M11**
  - **M10**
  - **M1**
  - **D1**
  - **B12**
  - **B11**
  - **A1**
  - **A2**
  - **A3**
  - **A4**
  - **A5**
  - **A6**
  - **A7**
  - **A8/A9**

### Power Supply

- **Power Supply:**
  - **U8900.J1**
  - **R8946**
  - **R8948**
  - **C8920**
  - **C8922**
  - **C8924**

### Additional Notes

- **OMIT:** Some signals are omitted for clarity.
- **FBGA:** The device is packaged in FBGA (Fine Pitch Ball Grid Array) technology, which is capable of high-density pin connections.
- **CRITICAL:** Critical signals are marked with a critical symbol.

---

**www.vinafix.vn**

---
Secure Signal List

- Nets must be buried with no exposed via between parts listed in `SECURE_NET` property. No test points allowed between the secure devices. Test points are allowed in the non-secure areas. Optional `NO_TEST=TRUE`, so test points are allowed on those nets.

- `SMC <-> CPU JTAG Level-Shifting` ALL OF THOSE PARTS WILL BE COVERED IN EPOXY

- Place these parts on one side and as close together as possible, and keep enough room from other parts to leave room for epoxy covering. Nets that are local to this circuit do not need test points as they will not be accessible.

- Nets must be buried with no exposed vias between parts.

- `Physical Security`

- `SYNC_DATE=(MASTER)`

- `SYNC_MASTER=(MASTER)`

- `NO_TEST=TRUE, no test points are allowed on those nets.`

- `NEED TO TURN PCI_GNT3_L INTO A NC NET!`

- `R9955 & R9956 values are TBD`

- `IMVP_VR_ON = 0.52V`

- `VOLTAGE = 0.52V`

- `NO_TEST=TRUE`
**DD2 Memory Bus Constraints**

Most CPU signals with impedance requirements are 55-ohm single-ended.

- **Recommended spacing:** Within data bus, with 2:1 spacing to the DSTB.
- **Recommended routing:** Each strobe/signal group routed on the same layer.
- **NOTE:** Design Guide recommends FSB spacing to other signals, assumed 3:1.

All FSB signals with impedance requirements are 55-ohm single-ended.
- **Recommended spacing:** Within data bus, with 2:1 spacing to the DSTB.
- **Recommended routing:** Each strobe/signal group routed on the same layer.
- **NOTE:** Design Guide does not indicate FSB spacing to other signals, assumed 3:1.

---

**Disk Interface Constraints**

- **NOTE:** DLL pair spacing is 2:1 within DLL pair, with 3:1 spacing to the DMA.
- **Recommended routing:** DLL pair routing is 2:1 within DLL pair, with 3:1 spacing to the DMA.
- **NOTE:** Design Guide recommends 25 mils, >50 mils preferred.

---

**PCI-Express / DMI Bus Constraints**

- **NOTE:** DLL pair spacing is 2:1 within DLL pair, with 3:1 spacing to the DMA.
- **Recommended routing:** DLL pair routing is 2:1 within DLL pair, with 3:1 spacing to the DMA.
- **NOTE:** Design Guide recommends 25 mils, >50 mils preferred.

---

**USB 2.0 Interface Constraints**

**NOTE:** DLL pair spacing is 2:1 within DLL pair, with 3:1 spacing to the DMA.
- **Recommended routing:** DLL pair routing is 2:1 within DLL pair, with 3:1 spacing to the DMA.
- **NOTE:** Design Guide recommends 25 mils, >50 mils preferred.

---

**Internal Interface Constraints**

**NOTE:** DLL pair spacing is 2:1 within DLL pair, with 3:1 spacing to the DMA.
- **Recommended routing:** DLL pair routing is 2:1 within DLL pair, with 3:1 spacing to the DMA.
- **NOTE:** Design Guide recommends 25 mils, >50 mils preferred.

---

**Clock Signal Constraints**

**NOTE:** DLL pair spacing is 2:1 within DLL pair, with 3:1 spacing to the DMA.
- **Recommended routing:** DLL pair routing is 2:1 within DLL pair, with 3:1 spacing to the DMA.
- **NOTE:** Design Guide recommends 25 mils, >50 mils preferred.

---

**Napa Platform Constraints**

The contents of this page are subject to change and may not reflect the current design guidelines. If you have any questions, please contact Apple Computer Inc. for the most up-to-date information.
**Video Signal Constraints**

**NOTE:** Layout Guide does not specify LVDS/TMDS spacing to other traces other than "do not run close"

- Ground shields recommended around VGA signals.
- VGA signals should be kept at least 15 mils from other traces.
- VGA should be routed as close to 75-ohms single-ended impedence as possible.
- Ground shields can be used around each pair if spacing cannot be met.
- LVDS and TMDS pairs should be kept at least 25 mils apart.

---

**GDDR3 (Frame Buffer) Memory Bus Constraints**

**FB_35S_TO_55S**

**NET_SPACING_TYPE1**

**PHYSICAL_RULE_SET**

**SPACING_RULE_SET**

**PHYSICAL_RULE_SET**

---

**PCI Bus Constraints**

**High-Speed I/O Interface Constraints**

---

More System Constraints

---
## M1 Board-Specific Spacing & Physical Constraints

### Table 1: Physical Rule Set

<table>
<thead>
<tr>
<th>Layer</th>
<th>Name</th>
<th>Layer</th>
<th>Name</th>
<th>Width</th>
<th>Height</th>
<th>Override</th>
</tr>
</thead>
<tbody>
<tr>
<td>TOP</td>
<td>BGA_P2MM</td>
<td>BOTTOM</td>
<td>BGA_P2MM</td>
<td>0.070</td>
<td>0.070</td>
<td>STD</td>
</tr>
<tr>
<td>TOP</td>
<td>BGA_P1MM</td>
<td>BOTTOM</td>
<td>BGA_P1MM</td>
<td>0.070</td>
<td>0.070</td>
<td>STD</td>
</tr>
<tr>
<td>TOP</td>
<td>BGA_P3MM</td>
<td>BOTTOM</td>
<td>BGA_P3MM</td>
<td>0.070</td>
<td>0.070</td>
<td>STD</td>
</tr>
<tr>
<td>TOP</td>
<td>BGA_P2GT</td>
<td>BOTTOM</td>
<td>BGA_P2GT</td>
<td>0.070</td>
<td>0.070</td>
<td>STD</td>
</tr>
<tr>
<td>TOP</td>
<td>BGA_P3GT</td>
<td>BOTTOM</td>
<td>BGA_P3GT</td>
<td>0.070</td>
<td>0.070</td>
<td>STD</td>
</tr>
<tr>
<td>TOP</td>
<td>BGA_P1GT</td>
<td>BOTTOM</td>
<td>BGA_P1GT</td>
<td>0.070</td>
<td>0.070</td>
<td>STD</td>
</tr>
</tbody>
</table>

### Table 2: Minimum Neck Width

<table>
<thead>
<tr>
<th>Layer</th>
<th>Name</th>
<th>Width</th>
<th>Override</th>
</tr>
</thead>
<tbody>
<tr>
<td>TOP</td>
<td>BGA_P1MM</td>
<td>0.101</td>
<td>STD</td>
</tr>
<tr>
<td>TOP</td>
<td>BGA_P1GT</td>
<td>0.101</td>
<td>STD</td>
</tr>
<tr>
<td>TOP</td>
<td>BGA_P2MM</td>
<td>0.076</td>
<td>STD</td>
</tr>
<tr>
<td>TOP</td>
<td>BGA_P2GT</td>
<td>0.076</td>
<td>STD</td>
</tr>
</tbody>
</table>

### Table 3: Minimum Neck Length

<table>
<thead>
<tr>
<th>Layer</th>
<th>Name</th>
<th>Length</th>
<th>Override</th>
</tr>
</thead>
<tbody>
<tr>
<td>TOP</td>
<td>BGA_P1MM</td>
<td>0.102</td>
<td>STD</td>
</tr>
<tr>
<td>TOP</td>
<td>BGA_P1GT</td>
<td>0.102</td>
<td>STD</td>
</tr>
<tr>
<td>TOP</td>
<td>BGA_P2MM</td>
<td>0.076</td>
<td>STD</td>
</tr>
<tr>
<td>TOP</td>
<td>BGA_P2GT</td>
<td>0.076</td>
<td>STD</td>
</tr>
</tbody>
</table>

### Table 4: Diffpair Primary Gap

<table>
<thead>
<tr>
<th>Layer</th>
<th>Name</th>
<th>Gap</th>
<th>Override</th>
</tr>
</thead>
<tbody>
<tr>
<td>TOP</td>
<td>BGA_P1MM</td>
<td>0.330</td>
<td>STD</td>
</tr>
<tr>
<td>TOP</td>
<td>BGA_P1GT</td>
<td>0.220</td>
<td>STD</td>
</tr>
<tr>
<td>TOP</td>
<td>BGA_P2MM</td>
<td>0.125</td>
<td>STD</td>
</tr>
<tr>
<td>TOP</td>
<td>BGA_P2GT</td>
<td>0.125</td>
<td>STD</td>
</tr>
</tbody>
</table>

### Table 5: Diffpair Neck Gap

<table>
<thead>
<tr>
<th>Layer</th>
<th>Name</th>
<th>Gap</th>
<th>Override</th>
</tr>
</thead>
<tbody>
<tr>
<td>TOP</td>
<td>BGA_P1MM</td>
<td>0.125</td>
<td>STD</td>
</tr>
<tr>
<td>TOP</td>
<td>BGA_P1GT</td>
<td>0.125</td>
<td>STD</td>
</tr>
</tbody>
</table>

### Table 6: Minimum Line Width

<table>
<thead>
<tr>
<th>Layer</th>
<th>Name</th>
<th>Width</th>
<th>Override</th>
</tr>
</thead>
<tbody>
<tr>
<td>TOP</td>
<td>BGA_P2GT</td>
<td>0.076</td>
<td>STD</td>
</tr>
<tr>
<td>TOP</td>
<td>BGA_P2GT</td>
<td>0.335</td>
<td>STD</td>
</tr>
</tbody>
</table>

### Table 7: Minimum Neck Width

<table>
<thead>
<tr>
<th>Layer</th>
<th>Name</th>
<th>Width</th>
<th>Override</th>
</tr>
</thead>
<tbody>
<tr>
<td>TOP</td>
<td>BGA_P1GT</td>
<td>0.080</td>
<td>STD</td>
</tr>
<tr>
<td>TOP</td>
<td>BGA_P1GT</td>
<td>0.165</td>
<td>STD</td>
</tr>
</tbody>
</table>

### Table 8: Maximum Neck Length

<table>
<thead>
<tr>
<th>Layer</th>
<th>Name</th>
<th>Length</th>
<th>Override</th>
</tr>
</thead>
<tbody>
<tr>
<td>TOP</td>
<td>BGA_P1GT</td>
<td>0.124</td>
<td>STD</td>
</tr>
<tr>
<td>TOP</td>
<td>BGA_P1GT</td>
<td>0.090</td>
<td>STD</td>
</tr>
</tbody>
</table>

### Table 9: Diffpair Primary Gap

<table>
<thead>
<tr>
<th>Layer</th>
<th>Name</th>
<th>Gap</th>
<th>Override</th>
</tr>
</thead>
<tbody>
<tr>
<td>TOP</td>
<td>BGA_P1GT</td>
<td>0.335</td>
<td>STD</td>
</tr>
<tr>
<td>TOP</td>
<td>BGA_P1GT</td>
<td>0.165</td>
<td>STD</td>
</tr>
</tbody>
</table>

### Table 10: Diffpair Neck Gap

<table>
<thead>
<tr>
<th>Layer</th>
<th>Name</th>
<th>Gap</th>
<th>Override</th>
</tr>
</thead>
<tbody>
<tr>
<td>TOP</td>
<td>BGA_P1GT</td>
<td>0.125</td>
<td>STD</td>
</tr>
<tr>
<td>TOP</td>
<td>BGA_P1GT</td>
<td>0.125</td>
<td>STD</td>
</tr>
</tbody>
</table>

---

*III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART*

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY NOTICE OF PROPRIETARY PROPERTY.

APPLE COMPUTER INC.

D  
051-6994 -07001  
www.vinafix.vn
ELECTRICAL_CONSTRAINT_SET

CPU_27P4S
CPU_27P4S
CPU_27P4S
CPU_55S
CLK_FSB_100D
CLK_FSB_100D
CPU_55S
CPU_55S
CPU_55S
CPU_55S
CPU_55S
CPU_55S
CPU_55S
CPU_55S
CPU_55S
FSB_55S
FSB_55S
FSB_55S
FSB_55S
FSB_55S
FSB_55S
FSB_55S
FSB_55S

PHYSICAL

NET_TYPE

CPU_VCCSENSE
CPU_VCCSENSE
CPU_VCCSENSE
CPU_VCCSENSE
CPU_2TO1
CPU_2TO1
CPU_ITP
CPU_ITP
CPU_COMP
CPU_COMP
CPU_COMP
CPU_COMP
CPU_GTLREF
CPU_2TO1
CPU_2TO1
FSB_ADSTB
FSB_ADDR
FSB_DSTB
FSB_DATA
FSB_COMMON
FSB_COMMON
FSB_COMMON
FSB_COMMON
FSB_COMMON
FSB_COMMON
FSB_COMMON
FSB_COMMON

IMVP6_VSEN_N
IMVP6_VSEN_P
CPU_VCCSENSE_N
CPU_VCCSENSE_P
CPU_VID<6..0>
CPU_VID<6..0>
CPU_XDP_CLK_N
CPU_XDP_CLK_P
XDP_BPM_L<5..0>
CPU_COMP<1>
IMVP_DPRSLPVR
PM_DPRSLPVR
CPU_THERMTRIP_L
CPU_STPCLK_L
CPU_SMI_L
CPU_IGNNE_L
CPU_DPSLP_L
CPU_A20M_L
FSB_FERR_L
FSB_IERR_L
FSB_ADSTB_L<3..0>
FSB_REQ_L<4..0>
FSB_A_L<31..3>
FSB_DSTBN_L<3..0>
FSB_DSTBP_L<3..0>
FSB_DINV_L<3..0>
FSB_D_L<63..0>
FSB_CPURST_L
FSB_TRDY_L
FSB_RS_L<2..0>
FSB_LOCK_L
FSB_HITM_L
FSB_DBSY_L
FSB_BREQ0_L
FSB_BPRI_L
FSB_BNR_L
FSB_ADS_L

APPENDIX B

M1 Net Properties

SIZE
D
NONE

DRAWING NUMBER
SHT
051-6941

REV.
D
07001

NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
NOT TO REPRODUCE OR COPY IT

NOTICE OF PROPRIETARY PROPERTY
I AGREE TO THE FOLLOWING

www.vinafix.vn