Mullet

M1 MLB

DVT Build - 12/02/2005

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Schematic / PCB #'

Part Number

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROMICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

(apple.com)
### BOM OPTION Groups

<table>
<thead>
<tr>
<th>BOM NUMBER</th>
<th>RUN NAME</th>
<th>RUN OPTIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>625-0211</td>
<td>PCBA, MULLET, SST</td>
<td></td>
</tr>
<tr>
<td>625-0212</td>
<td>PCBA, MULLET, ST</td>
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</table>

### BOM Configuration

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>REFERENCE DES</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>338S0270</td>
<td>1</td>
<td>U3600, STC</td>
<td>[EEE:TPV]</td>
<td>CRITICAL</td>
<td>M1, BST, EEE204</td>
</tr>
<tr>
<td>338S0271</td>
<td>1</td>
<td>U3601, STC</td>
<td>[EEE:TPV]</td>
<td>CRITICAL</td>
<td>M1, BST, EEE205</td>
</tr>
<tr>
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<td>1</td>
<td>U3602, STC</td>
<td>[EEE:TPV]</td>
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<td>M1, BST, EEE206</td>
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<tr>
<td>338S0273</td>
<td>1</td>
<td>U3603, STC</td>
<td>[EEE:TPV]</td>
<td>CRITICAL</td>
<td>M1, BST, EEE207</td>
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</tbody>
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### Phantom BOM #’s

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>REFERENCE DES</th>
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<th>BOM OPTION</th>
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<tr>
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<td>254000, M1</td>
<td>BST, EEE208</td>
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<td>M1, BST, EEE209</td>
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<tr>
<td>625-0214</td>
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<td>EEE204</td>
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<td>625-0215</td>
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<td>M1, BST</td>
<td>EEE204</td>
<td>CRITICAL</td>
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</table>

### Bar Code Label / EEE #’s

<table>
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<th>PART NUMBER</th>
<th>QTY</th>
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<th>REFERENCE DES</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
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<tbody>
<tr>
<td>338S0274</td>
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<tr>
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<td>U3601, STC</td>
<td>[EEE:TPV]</td>
<td>CRITICAL</td>
<td>M1, BST, EEE205</td>
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<tr>
<td>338S0276</td>
<td>1</td>
<td>U3602, STC</td>
<td>[EEE:TPV]</td>
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<td>M1, BST, EEE206</td>
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<tr>
<td>338S0277</td>
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<td>M1, BST, EEE207</td>
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### Module Parts

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
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<th>REFERENCE DES</th>
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<td>U3603, STC</td>
<td>[EEE:TPV]</td>
<td>CRITICAL</td>
<td>M1, BST, EEE207</td>
</tr>
</tbody>
</table>

### The above stages and build settings are per 8/25 strategy statement.

The number of parts managed as Le Menu decreases as a project progresses.

The above stages and build settings are per 8/25 strategy statement.
Power Supply NO_TESTS

CPU FSB NO_TESTS

Misc EXPOSED_VIA Nets

Functional Test Points

Fan Connectors

Battery Digital Connector

LPC+ Debug Connector

Left I/O Data Connector

Left I/O Power Connector

Functional / ICT Test
Chassis connection to be made at the mounting hole northeast of the LVDS connector

Chassis connection to be made at the mounting hole southwest of the USB connector

Chassis connection to be made at the mounting hole northwest of the DVI connector

HOLE-VIA-P5RP25

NO_TEST=TRUE
MAKE_BASE=TRUE

NO_TEST=TRUE
MAKE_BASE=TRUE

NO_TEST=TRUE
MAKE_BASE=TRUE

NO_TEST=TRUE
MAKE_BASE=TRUE

NO_TEST=TRUE
MAKE_BASE=TRUE

NO_TEST=TRUE
MAKE_BASE=TRUE

NO_TEST=TRUE
MAKE_BASE=TRUE

NO_TEST=TRUE
MAKE_BASE=TRUE

HOLE-VIA-P5RP25

HOLE-VIA-P5RP25

HOLE-VIA-P5RP25

Ethernet Power Management Support

NOTE:  some options "USB_L NC P0" and "USB_L NC DISABLE" are mutually-exclusive.

USB Port 'A' (Debug Port) = Right USB 2.0 Port

USB Port 'B' = Trackpad (Geyser)

USB Port "C" = Left USB 2.0 Port

USB Port "D" = Camera

USB Port "E" = ExpressCard

USB Port "F" = IR Receiver

USB Port "G" = Bluetooth (MIJP)

USB Port "H" = Reserved (PCI-Z Mini Card)

Trace deleted to make room for other diffpairs over RAM connector.
CPU VCORE VID Connections

Resistors to allow for override of CPU VID

CPU_VID<4>  CPU_VID<3>  CPU_VID<2>  CPU_VID<1>  CPU_VID<0>

Will probably be removed before production.
ITP TCK SIGNAL LAYOUT NOTE: ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU's TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX CONNECTOR'S FBO PIN.
In VOUT Disable, do not use DC-Out signals. If VOUT is not implemented, tie VCC_VOUT and VCC_A208 to GND. If SDVO is used, VCC_VOUT must remain powered with proper decoupling. Otherwise, tie VCC_VOUT to GND also.

TV-Out Disable

- Tie VCC_VOUT, VSSA_VOUT, VCC_A208, and VSSA_A208 to 1.5V power rail.
- Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail.

TV-Out Signal Usage:

- Composite: DACA only
- Component: DACA, DACB & DACC

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NCTF balls are Not Critical To Function

These connections can break without impacting part performance.

C1615
Place near pin BA21

Layout Note:
Place near pin BA21

C1619
Place in cavity

Layout Note:
Place in cavity
NOTE: ENHANCE INTERNAL 1.3V SUSPEND REG

INTERNAL 20K PD
INTERNAL 20K PD ENABLED WHEN OUT

ACZ_SDATAOUT
ACZ_SYNC

R2196

TP_SB_XOR_U7
TP_SB_XOR_T5
TP_SB_XOR_V4
TP_SB_XOR_W1

NOTE: LDRQ<0-1># HAVE INTERNAL 20K PU

NOTE: RISING-EDGE TRIGGERED AT CPU

NOTE: CPU THERMTRIP R

NOTE: SUSTUFF

LAYOUT NOTE: PLACE R2101 & R2194 WHERE ACCESSIBLE

INTERNAL 20K PD

NOTE: ALL IDE PINS HAVE INTERNAL 33-OHM SERIES R'S
Platform Reset Connections

Unbuffered

Buffered

Initial resistor values are based on CRB, but may change after characterization.

Platform Reset Connections

Unbuffered

Buffered

Initial resistor values are based on CRB, but may change after characterization.

Platform Reset Connections

Unbuffered

Buffered

Initial resistor values are based on CRB, but may change after characterization.
ICH7-M SMBus Connections

- SMB_DATA
- SMB_CLK

ExpressCard Slot

(Write: 0x92 Read: 0x93)

M35 - TMP105

Left I/O SMBus Connections:

(Write: 0x72 Read: 0x73)

U2 - Keyboard Controller

(Write: 0x70 Read: 0x71)

U1 - Trackpad Controller

(Write: 0x70 Read: 0x71)

Trackpad I2C Connections:

U1 - Trackpad Controller

(Write: 0x92 Read: 0x93)

U2 - Keyboard Controller

(Write: 0x92 Read: 0x93)

Left I/O Board

(Write: 0xA4 Read: 0xA5)

(Write: 0xA0 Read: 0xA1)

SO-DIMM "A"

(Write: 0xD2 Read: 0xD3)

SO-DIMM "B"

Left I/O Board

(Write: 0xA4 Read: 0xA5)

(Write: 0xA0 Read: 0xA1)

SMC "Battery A" SMBus Connections

SMC "Battery B" SMBus Connections

SMC "0" SMBus Connections

SMC "A" SMBus Connections

SMC "B" SMBus Connections

Clock Chip

CP28045-0 D230

(Master)

(SDA)

(SCL)

(D0)

(CLK)

Clock Chip

CP28045-0 D230

(Master)

(SDA)

(SCL)

(D0)

(CLK)

Clock Chip

CP28045-0 D230

(Master)

(SDA)

(SCL)

(D0)

(CLK)

Clock Chip

CP28045-0 D230

(Master)

(SDA)

(SCL)

(D0)

(CLK)

Clock Chip

CP28045-0 D230

(Master)

(SDA)

(SCL)

(D0)

(CLK)

Clock Chip

CP28045-0 D230

(Master)

(SDA)

(SCL)

(D0)

(CLK)
One cap for each side of every RPAK, one cap for every two discrete resistors

Ensure CS_L and ODT resistors are close to SO-DIMM connector.
Page Notes

Power aliases required by this page:
- PP5V_S0_MEMVTT
- PP0V9_S0_MEMVTT_LDO

Signal aliases required by this page:
NONE.

BOM options provided by this page:
NONE.

Page Notes

Okay to turn off 5V and leave 1.8V powered in S3.

DDR2 Vtt Regulator

If power inputs are not S0, MEMVTT_EN can be used to
okay to turn off 5V and
leave 1.8V powered in S3.

Memory Vtt Supply

051-6941

www.vinafix.vn
NOSTUFF R3450, R3451, R3453 FOR MANUAL CPU FREQUENCY

Clock Termination

Apple Computer Inc.

www.vinafix.vn
Yukon Power Control

Allows powering Yukon down during battery sleep to save power

- ENETPWR_S3 BOMOPTION is active:

- ENETPWR_S3AC BOMOPTION is active:

<table>
<thead>
<tr>
<th>State</th>
<th>PM_SLP_S4_L</th>
<th>PM_SLP_S3BATT</th>
<th>PM_SLP_S3BATT_L</th>
<th>P2V5S3_EN_L</th>
<th>P1V2S3_RUNSS</th>
</tr>
</thead>
<tbody>
<tr>
<td>S0 Batt</td>
<td>0V</td>
<td>3.3V</td>
<td>0V (3.3V ON)</td>
<td>3.3V</td>
<td>0V (2.5V ON)</td>
</tr>
<tr>
<td>S3 Batt</td>
<td>PBUS</td>
<td>3.3V</td>
<td>PBUS (3.3V OFF)</td>
<td>0V</td>
<td>3.3V (2.5V OFF)</td>
</tr>
<tr>
<td>S5 Batt</td>
<td>PBUS</td>
<td>0V</td>
<td>PBUS (3.3V OFF)</td>
<td>0V</td>
<td>Hi-Z (2.5V OFF)</td>
</tr>
<tr>
<td>G3H Batt</td>
<td>PBUS</td>
<td>0V</td>
<td>PBUS (3.3V OFF)</td>
<td>0V</td>
<td>Hi-Z (2.5V OFF)</td>
</tr>
</tbody>
</table>

- Yukon Power Control

5% 1/16W MF-LF
402 470K
1 2
R4302

2N7002DW-X-F SOT-363

4

Q4304

100K 1/16W 5%
402 2
1
R4301

0

Q4300

MF-LF
1/16W 5%
402 1
2
R4300

Q4305

SYNC_DATE=(MASTER)
SYNC_MASTER=(MASTER)

Yukon Power Control

051-6941
43
44
43
**Page Notes**

Power aliases required by this page:
- -PP3V3_S0_FWISENS (system supply for bus power)
- -PPBUS_S5_FWPWRSW

Signal aliases required by this page:
- -FWPWR_PWRON (see related text note below)

BOM options provided by this page:
(NONE)

Power aliases required by this page:
- -PP3V3_S0_FWPORTPWRSW

Signal aliases required by this page:
- -FWPWR_IOUT

---

**Port Power Switch**

**FireWire Port Current Sense**

- **Port Power Switch**
  - CRITICAL
  - FIREWIRE SWTCH SW
  - FIREWIRE SWTCH SW
  - FIREWIRE SWTCH SW
  - FIREWIRE SWTCH SW

- **FireWire Port Current Sense**
  - CRITICAL
  - FIREWIRE SWTCH SW
  - FIREWIRE SWTCH SW
  - FIREWIRE SWTCH SW
  - FIREWIRE SWTCH SW

---

**FireWire Port Power**

- **SYNC_DATE=(MASTER)**
- **SYNC_MASTER=(MASTER)**

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- -PPBUS_S5_FWPWRSW

**Signal aliases required by this page:**
- -FWPWR_PWRON (see related text note below)

- **FireWire Port Power**
  - CRITICAL
  - FIREWIRE SWTCH SW
  - FIREWIRE SWTCH SW
  - FIREWIRE SWTCH SW
  - FIREWIRE SWTCH SW

---

**Port Power Switch**

**FireWire Port Current Sense**

- **Port Power Switch**
  - CRITICAL
  - FIREWIRE SWTCH SW
  - FIREWIRE SWTCH SW
  - FIREWIRE SWTCH SW
  - FIREWIRE SWTCH SW

- **FireWire Port Current Sense**
  - CRITICAL
  - FIREWIRE SWTCH SW
  - FIREWIRE SWTCH SW
  - FIREWIRE SWTCH SW
  - FIREWIRE SWTCH SW

---

**FireWire Port Power**

- **SYNC_DATE=(MASTER)**
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www.vinafix.vn
R6309 is not needed when sharing SPI flash with ICH7M and TEKOA (LAN chip).

R6307 and R6306 should be placed less than 100 mils from ICH7M.

R6303 should be placed less than 100 mils from flash ROM.
Power Control Signals

3.425V "G3Hot" Supply
Supplies need to guarantee 3.4V delivered to PPC that generator

1.5V / 1.05V PWRGD Circuit
Reports when 1.5V S0 and 1.05V S0 are in regulation

Other S0 Rails PWRGD Circuit
Reports when 5V S0, 2.7V S0, 2.5V S0, 1.2V S0 and 0.9V S0 are in regulation
Place series R's and common-mode filtering close to GPU, common mode chokes near connector.

VGA SYNC BUFFERS

DVI INTERFACE

DVI DDC CURRENT LIMIT

3V LEVEL SHIFTERS

External Display Connector

Apple Computer Inc.
Left ALS Connector

Bluetooth (M13P) & SATA HDD Flex Connector

NOTE: Club cross DDR2 signals and pick up significant noise, Common-mode chokes are to remove this noise from DATA signals.
LVDS Interface Pull-downs

NOTE: These parts are to counter an invalid state caused by the LVDS interface pull-downs. The voltage is present on LVDS interface pins even when they should be 0V. Resulting pump-up in LCD panel can cause startup issues. Pull-down resistors reduce the pump-up in the panel, though some voltage will still be seen on LVDS signals when they should be 0V.
2005/09/26 - 4274915 - Added 2.2µF caps on 10030N-90 chip. - PMMine_L.
2005/09/26 - 4294710 - Aligned part nos to parts identified in 50 populated.
2005/09/26 - 4294715 - Added polysilicon Nanoe converter for 203 fPC connector.

2005/09/26 - 4274915 - Added 2.2µF caps on 10030N-90 chip. - PMMine_L.
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