3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.

Mullet

Pansy Build - 08/10/2005

FireWire Ports

Internal USB Connections

External USB Connector

Left I/O Board Connector

PCI-E Connections

SDM Support

LPCF Debug Connector

Thermal Sensors

Current & Voltage Sensing

SPI BootROM

ALS Support

Fan Connectors

SMB

IMPF CPU VCore Regulator

5V / 1.5V Power Supply

1.5V & 1.8V Regulators

1.8V Supply

1.9V / 1.05V Power Supplies

1.9V DIMM Supply

Power Aliases

PBus-In & Battery Connectors

S3/S0 POSTs & Power Control

ATI M56 PCI-E

CPU (H55) Core Supplies

ATI M56 Core Power

ATI M56 Frame Buffer I/F

GPU Straps

GDDR3 Frame Buffer A

GDDR3 Frame Buffer B

ATI M56 GPIO/DVO/Misc

ATI M56 Video Interfaces

Internal Display Connectors

External Display Connector

M1 Net Properties

NB Power 1

NB Power 2

NB Grounds

NB (GH) Decoupling

NB Config Straps

NB Misc

M1 SMBus Connections

DDR2 2D-DIMM Connector A

DDR2 2D-DIMM Connector B

Memory Active Termination

Memory Vtt Supply

DDR2 VRAM

CLOCK

Clock Termination

Mobile Clocking

PATA Connector

ETHERNET CONTROLLERS

Ethernet Connector

FireWire Controller

FireWire Port Power

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**Phantom BOM #’s**

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>REFERENCE DESIGNATOR(S)</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>333S0350</td>
<td>1</td>
<td>IC, SGRAM, GDDR3, 8MX32, 700MHZ, 136 FBGA</td>
<td>VRAM_128</td>
<td>CRITICAL</td>
<td></td>
</tr>
</tbody>
</table>

**Module Parts**

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>REFERENCE DESIGNATOR(S)</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>333S0354</td>
<td>4</td>
<td>IC, SGRAM, GDDR3, 8MX32, 700MHZ, 136 FBGA</td>
<td>VRAM_256</td>
<td>CRITICAL</td>
<td></td>
</tr>
</tbody>
</table>

**Alternate Parts**

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>DESCRIPTION</th>
<th>REFERENCE DESIGNATOR(S)</th>
<th>BOM OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>333S0354</td>
<td>IC, SGRAM, GDDR3, 8MX32, 700MHZ, 136 FBGA</td>
<td>VRAM_256, GPU_MEM_256M</td>
<td>VRAM_128, GPU_MEM_128M</td>
</tr>
</tbody>
</table>
Chassis connection to be made at the mounting hole northeast of the DVI connector.

Chassis connection to be made at the mounting hole northwest of the USB connector.

Chassis connection to be made at the mounting hole east of the USB connector.

Chassis connection to be made at the mounting hole southwest of the USB connector.

HOLE-VIA-P5RP25
VCCA (CPU AVdd) Decoupling

- 1x 10uF, 1x 0.01uF

VCCP (CPU I/O) Decoupling

- 1x 470uF, 6x 0.1uF 0402

NOTE: This cap is shared between CPU and NB.

Need to make sure we can do dual-footprint for 128S0068 & 128S0074!!!
CPU ZONE THERMAL SENSOR

PLACE U1001 NEAR THE MCH

CPU MISC1-TEMP SENSOR

SYNC_MASTER=M42  
SYNC_DATE=08/04/2005

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**CPU ITP700FLEX DEBUG SUPPORT**

- **PP1V05 50 CPU**
- **PP1V3 65 SB PM**
- **PP1V3 65 SB PM**
- **XDP TDO**
- **XDP TDI**
- **CPU XDP_CLK_P**
- **CPU XDP_CLK_N**
- **XDP TCK**
- **XDP TMS**
- **XDP TRST_L**
- **XDP TDO**
- **XDP BPM_L<5>**
- **XDP BPM_L<4>**
- **XDP BPM_L<2>**
- **XDP BPM_L<3>**
- **XDP BPM_L<1>**
- **XDP BPM_L<0>**
- **ITP_BPM_L<5>**
- **ITP_BPM_L<4>**
- **ITP_BPM_L<2>**
- **ITP_BPM_L<3>**
- **ITP_BPM_L<1>**
- **ITP_BPM_L<0>**
- **ITP TDO**
- **ITP TDI**
- **ITP TCK**
- **ITP TMS**
- **ITP TRST_L**
- **ITP TDO**
- **ITP BPM_L<5>**
- **ITP BPM_L<4>**
- **ITP BPM_L<2>**
- **ITP BPM_L<3>**
- **ITP BPM_L<1>**
- **ITP BPM_L<0>**
- **ITP TDO**
- **ITP TDI**
- **CPU XDP_CLK_P**
- **CPU XDP_CLK_N**
- **XDP TCK**
- **XDP TMS**
- **CPU XDP_CLK_P**
- **CPU_XDP_CLK_N**

**ITP TCK SIGNAL LAYOUT NOTE:**
- Route the TCK signal from ITP700FLEX Connector's TCK pin to CPU's TCK pin and then fork back from CPU TCK pin and route back to ITP700FLEX Connector's FBO pin.

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**Revision:**
- The revision date is 07/26/2005.
NCTF balls are Not Critical To Function
These connections can break without impacting part performance.

- **U1250**
  - 945GM
  - NB Power 1

**NB Power 1**

**SCALE**

**SIZE**

**SYNC_DATE** (MASTER)
ICH7-M SMBus Connections

[Diagram of ICH7-M SMBus Connections]

SMC "0" SMBus Connections

[Diagram of SMC "0" SMBus Connections]

SMC "A" SMBus Connections

[Diagram of SMC "A" SMBus Connections]

SMC "Battery A" SMBus Connections

[Diagram of SMC "Battery A" SMBus Connections]

SMC "Battery B" SMBus Connections

[Diagram of SMC "Battery B" SMBus Connections]

SMC "Clock Chip"

[Diagram of Clock Chip]

SMC "CPU Temp"

[Diagram of CPU Temp]

SMC "GPU Temp"

[Diagram of GPU Temp]

SMC "Left ALS - TSL2561"

[Diagram of Left ALS - TSL2561]

SMC "Top-Case"

[Diagram of Top-Case]
One cap for each side of every RPAK, one cap for every two discrete resistors.
disable MEMVTT in sleep.
MEMVTT_EN can be used to leave 1.8V powered in S3.
Okay to turn off 5V and
If power inputs are not S0, MEMVTT_EN can be used to.
TPM Crystal Circuit

SMC G3Hot Oscillator

Mobile Clocking

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SMC G3Hot Oscillator

TPM Crystal Circuit

Is this the best part to use?

SM-2 32.768K Y3720 1/16W 5%

R3721 1/16W 5%

R3720 10M

U3750 10V CERM 402 20%

C3751 0.1uF

L3750 4.7uF 20% CERM

C3750 6.3V

R3750 50V 5%

C3720 50V 5%

C3721 12pF

VOLTAGE=3.425V PP3V42_G3H_SMC_CLK_MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.2 mm

SMC_CLK32K_SUSCLK SMC_SUS_CLK SMC_CLK32K_SUSCLK_R

VPP=3V42 SMC_CLK

SYNC_DATE=(MASTER) SYNC_MASTER=(MASTER)

051-6941 103

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Page Notes

- **NOTE:** FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB pairs.

- This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

- BOM options provided by this page:
  - * =GND_CHASSIS_FW_PORT1
  - * =PP3V3_FW

- Power aliases required by this page:
  - =PP3V3_S5_FWLATEVG

- Signal aliases required by this page:
  - - =GND_CHASSIS_FW_PORT1
  - - =PP3V3_FW

- Electrical Constraints provided by this page:
  - ELECTRICAL_CONSTRAINT_SET

- SPACING

- TERMINATION

- PAGE

- PHYSICAL

- R4690

- SHT

- SCALE

- SYNC_DATE = (MASTER)

- DRAWING NUMBER

- DRAWING

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- II NOT TO REPRODUCE OR COPY IT

- III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

- NO TEST = YES

- MAKE_BASE = TRUE

- NO STUFF

- NO STUFF FOR THE MOMENT.
Top-Case Connector
(Pinout is almost fixed)

Camera Connector

Bluetooth (ML3P) & SATA HDD Flex Connector

Post-proto, replace with 180346 (C0830-000RT-SN)

Place these 2 caps close to SouthBridge

Place these 2 caps close to motherbridge

Internal USB Connections
Place L5200, L5205 and L5206 across moat.
**SMC Reset Button / Brownout Detect**

**SMC Crystal Circuit**

**Debug Power Button**

Silk: "PWR BTN"

**SMC AVREF Supply**

**SMC PWRGD Circuit**

System (Sleep) LED Circuit

SMC Support

---

NOTE: R5965 acts as 10K pull-up for PGOOD signal

ISL6269 undervoltage threshold 81-87% (2.67 - 2.87V)

=PP3V42_G3H_SMC_PWRGD

VOLTAGE=0V

MIN_NECK_WIDTH=0.2 mm

VOLTAGE=3.3V

MIN_NECK_WIDTH=0.2 mm

C5967 0.01uF

CERM

5%

SYNC_MASTER=(MASTER)

SYNC_DATE=(MASTER)

---

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---

MAKE_BASE=TRUE

---

SMC Support

---

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C6309 and C6310 are not needed when sharing SPI flash with ICH7M and TEKO (LAN chip).
R6307 and R6306 should be placed less than 100 mils from ICH7M.
R6303 should be placed less than 100 mils from flash ROM.
SMS
SYNC_MASTER=M42
SYNC_DATE=07/26/2005

Desired Orientation
(Placed on board topside)
Package Top

SMS_Y_AXIS
SMS_Z_AXIS
SMS_X_AXIS
SMS_ONOFF_L
SMS_ACC_SELTEST - SHOULD BE PULLED HIGH WHEN NOT USED
SMS_ACC_SELFTEST - SHOULD BE PULLED HIGH WHEN NOT USED
SMS_ACC_SELFTEST - ACCELEROMETER OUTPUT TO SCU
SMS_ONOFF_L - CONNECT TO SMC TO BE ABLE TO PUT SMS INTO LOW-POWER MODE

VOLTAGE=3.3V
MIN_NECK_WIDTH=0.2 MM
MIN_LINE_WIDTH=0.2 MM

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Connect to power pin to control outputs.
If unconnected, powers up with VIN.

Vout = 0.8V * (1 + Ra / Rb)
NOTE: Be aware of pull-up on this signal.
If unconnected, powers up with PVIN.

2.5V S3 Regulator

Vout = 0.8V * (1 + Ra / (Rb + Rc))

1.2V S3 Regulator

Vout = 0.8V * (1 + Ra / Rb)
Vout = 1.199V ± 1.2 A
Vout = 0.6V * (1 + Ra / Rb)
3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator

Vout = 1.25V * (1 + Ra / Rb)
Note: Place all jumpers on top-side of MLB
Connect to designated pin, then GND

within byte-lane, but software must know how these bits are mapped for GPU to support GDDR3 vendor/device identification scheme.
TMDS Filtering

Place series R's close to GPU, other parts near connector.

DVI DDC CURRENT LIMIT

DVI INTERFACE

VGA SYNC BUFFERS

Isolation required for DVI power switch

3V LEVEL SHIFTERS

External Display Connector

ELECTRICAL_CONSTRAINT_SET

MIN_LINE_WIDTH=0.38 mm

MIN_NECK_WIDTH=0.25 mm

VOLTAGE=5V

ANALOG FILTERING

PLACE CLOSE TO CONNECTOR

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