1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

Mullet

M1 MLB

Pansy Build - 08/10/2005

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
03		394758	ENGINEERING RELEASED	08/10/05	

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-6941	1	SCHEM,MULLET,M1	SCH		
820-1881	1	PCBF,MULLET,M1	PCB		
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:TSQ]	CRITICAL	

DRAWING
TITLE=MULLET
ABBREV=DRAWING
LAST_MODIFIED=Wed Aug 10 08:42:29 2005

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE

SIZE D

Apple Computer Inc.

TITLE
SCHEM,MULLET,M1

DRAWING NUMBER 051-6941 REV. 03

SHT 1 OF 103

8 7 6 5 4 3 2 1

D C B A

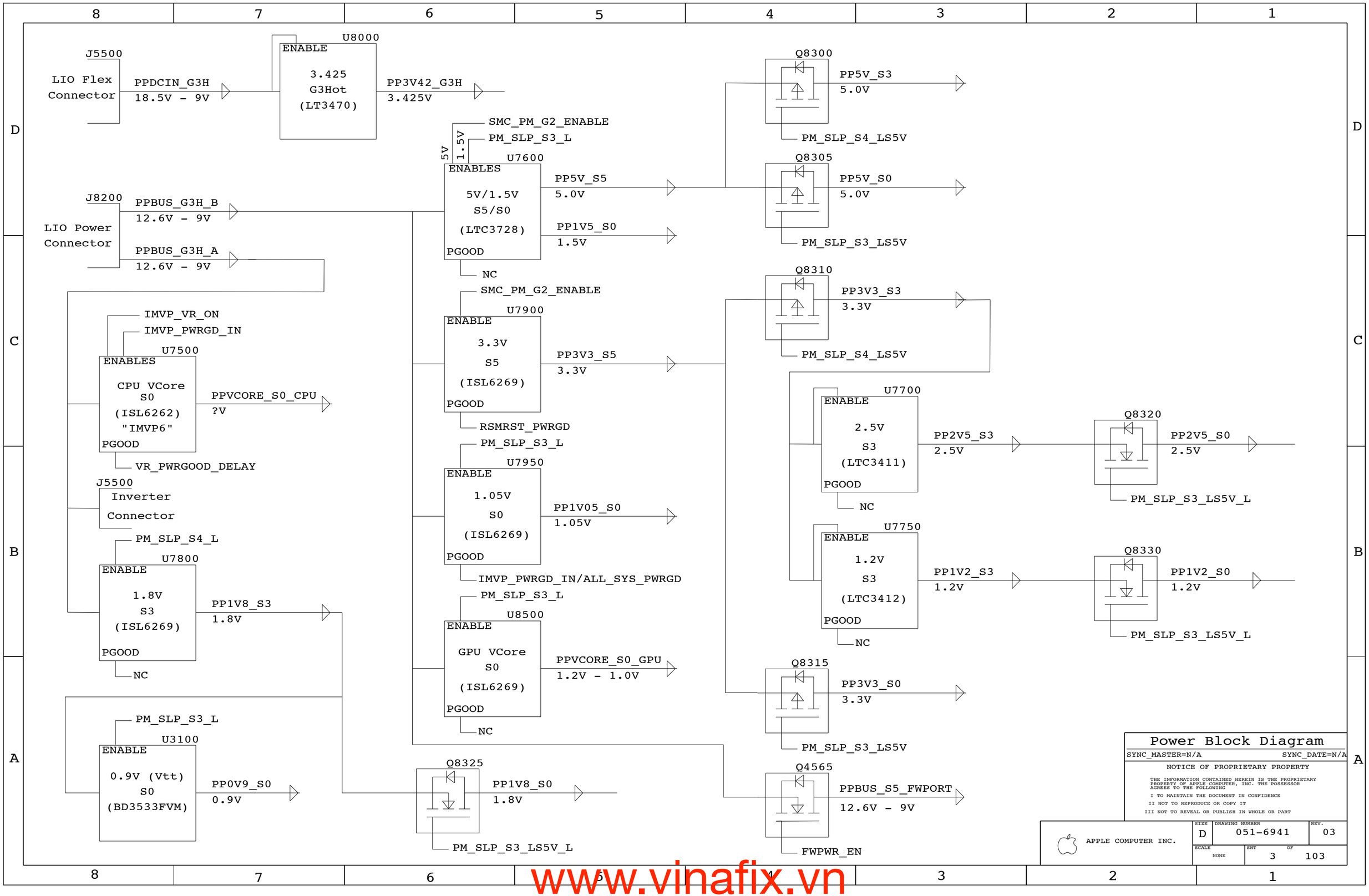
System Block Diagram

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	2	103



Power Block Diagram

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	3	103

BOM NUMBER	BOM NAME	BOM OPTIONS
630-7207	PCBA,MULLET_128,M1	075-0137,075-0139,075-0140
630-7254	PCBA,MULLET_256,M1	075-0138,075-0139,075-0140
075-0137	128,MULLET,M1	VRAM_128
075-0138	256,MULLET,M1	VRAM_256,GPU_MEM_256M
075-0139	PROJ_PTS,MULLET,M1	ALTERNATE,COMMON,M1_COMMON1,M1_COMMON2,M1_DEBUG
075-0140	LEMENU_PTS,MULLET,M1	LEMENU

BOM GROUP	BOM OPTIONS
M1_COMMON1	CAMERA_S3,CPUCORE_2PIN,GPU_BB_CTL,GPUTHM_A_GPU,INVERTER_BUF,KBDLED_HAS,LCD_CTL_GPU
M1_COMMON2	MEMVREF_S3,MEMVTT_EN_PU,PLTRST_GATE_STUFF,PROTO_ONLY,USB_C_OC_PU,USB_D_OC_PU
M1_DEBUG	DEVELOPMENT,ITP,LPCPLUS

Phantom BOM #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
075-0137	1	128,MULLET,M1	BOM1		075-0137
075-0138	1	256,MULLET,M1	BOM2		075-0138
075-0139	1	PROJ PTS,MULLET,M1	BOM3		075-0139
075-0140	1	LeMENU PTS,MULLET,M1	BOM4		075-0140

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0354	4	IC,SGRAM,GDDR3,8MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_128
333S0350	4	IC,SGRAM,GDDR3,16MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_256
341S1797	1	IC,EEPROM,SERIAL IIC,8KBIT,SO8	U4102	CRITICAL	LEMENU

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	REFERENCE DESIGNATOR(S)	DESCRIPTION	BOM OPTION
998-1175	128S0074	C0935,C0950,C0952,C0953,C0954,C1900	470uF,2.5V,7mOhm	

BOM Configuration

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	4	103

Functional Test Points

Power Supply NO_TESTs

NO_TEST

TRUE	IMVP6_RBIAS	56
TRUE	IMVP6_COMP	56
TRUE	P5VS5_RUNSS	57 64
TRUE	P1V5S0_RUNSS	57 64
TRUE	P2V5S3_MODE	58
TRUE	P2V5S3_SHDNRT	58 64
TRUE	P1V2S3_RT	58
TRUE	P1V2S3_RUNSS	58 64
TRUE	P1V8S3_COMP	59
TRUE	P1V8S3_FSET	59
TRUE	P3V3S5_COMP	60
TRUE	P3V3S5_FSET	60
TRUE	P1V05S0_COMP	60
TRUE	P1V05S0_FSET	60
TRUE	P3V42G3H_FB	61
TRUE	GPUVCORE_COMP	66
TRUE	GPUVCORE_FSET	66
TRUE	GPUBBP_ADJ	66

CPU FSB NO_TESTs

NO_TEST

TRUE	FSB_A_L<31..3>	7 12 76
TRUE	FSB_ADS_L	7 12 76
TRUE	FSB_ADSTB_L<1..0>	7 12 76
TRUE	FSB_BNR_L	7 12 76
TRUE	FSB_BREQ0_L	7 12 76
TRUE	FSB_D_L<63..0>	7 12 76
TRUE	FSB_DBSY_L	7 12 76
TRUE	FSB_DINV_L<3..0>	7 12 76
TRUE	FSB_DRDY_L	7 12 76
TRUE	FSB_DSTBN_L<3..0>	7 12 76
TRUE	FSB_DSTBP_L<3..0>	7 12 76
TRUE	FSB_HIT_L	7 12 76
TRUE	FSB_HITM_L	7 12 76
TRUE	FSB_LOCK_L	7 12 76
TRUE	FSB_REQ_L<4..0>	7 12 76

FUNC_TEST property removed since these test points are not on the proper side for Functional Test points.

Fan Connectors

FUNC_TEST

	=PP5V_S0_FAN_LT	53 62
	FAN_LT_PWM	53
	FAN_LT_TACH	53
	FAN_RT_PWM	53
	FAN_RT_TACH	53

LPC+ Debug Connector

FUNC_TEST

TRUE	=PP3V3_S5_LPCPLUS	48 62
TRUE	=PP5V_S0_LPCPLUS	48 62
TRUE	LPC_AD<0>	21 46 48 55
TRUE	LPC_AD<1>	21 46 48 55
TRUE	LPC_FRAME_L	21 46 48 55
TRUE	PM_CLKRUN_L	23 39 46 48 55
TRUE	BOOT_LPC_SPI_L	22 47 48
TRUE	SMC_TMS	46 47 48
TRUE	DEBUG_RST_L	26 48
TRUE	SMC_TRST_L	46 48
TRUE	SMC_TDO	46 47 48
TRUE	SMC_MD1	46 48
TRUE	SMC_TX_L	46 47 48
TRUE	FWH_INIT_L	21 47 48
TRUE	PCI_CLK_PORT80_LPC	34 48
TRUE	LPC_AD<2>	21 46 48 55
TRUE	LPC_AD<3>	21 46 48 55
TRUE	INT_SERIRQ	23 46 48 55
TRUE	PM_SUS_STAT_L	23 46 48 55
TRUE	SMC_TDI	46 47 48
TRUE	SMC_TCK	46 47 48
TRUE	SMC_RST_L	46 47 48
TRUE	SMC_NMI	46 48
TRUE	SMC_RX_L	46 47 48
TRUE	SV_SET_UP	23 48

Other Func Test Points

FUNC_TEST

TRUE	=PP1V05_S0_REG	50 60 62

Battery Digital Connector

FUNC_TEST

TRUE	SMC_BS_ALRT_L	46 47 63
TRUE	=SMBUS_BATT_SCL	27 63
TRUE	=SMBUS_BATT_SDA	27 63
TRUE	GND_BATT	63

Left I/O Data Connector

FUNC_TEST

TRUE	=PP1V5_S0_LIO	44 62
TRUE	=PPDCIN_G3H_LIO	44 62
TRUE	=PP5V_S3_LIO	44 62
TRUE	=PP3V42_G3H_LIO	44 62
TRUE	PP5V_S0_AUDIO_PWR	44
TRUE	PP5V_S0_AUDIO	44
TRUE	GND_AUDIO_PWR	44
TRUE	GND_AUDIO	44
TRUE	ACZ_SDATAIN<0>	21 44 76
TRUE	ACZ_SDATAOUT	21 44 76
TRUE	ACZ_BITCLK	21 44 76
TRUE	ACZ_RST_L	21 44 76
TRUE	EXCARD_OC_L	6 44 47
TRUE	LTUSB_OC_L	6 44
TRUE	LIO_BATT_ISENSE	44 50
TRUE	SMC_SYS_ISET	44 46
TRUE	SMC_BATT_ISET	44 46
TRUE	SMC_BATT_CHG_EN	44 46 47
TRUE	SMC_BC_ACOK	44 46 47
TRUE	SMC_PS_ON	40 44 46 47
TRUE	LIO_P3V3S0_EN_L	44 64
TRUE	LIO_DCIN_ISENSE	44 50
TRUE	LIO_P3V3S3_EN	44 64
TRUE	SMC_BATT_TRICKLE_EN_L	44 46 47
TRUE	SYS_ONEWIRE	44 46 47
TRUE	MINI_CLKREQ_L	34 44
TRUE	SMC_EXCARD_CP	44 46 47
TRUE	EXCARD_CLKREQ_L	34 44
TRUE	SMC_EXCARD_PWR_EN	44 46
TRUE	LIO_PLT_RESET_L	26 44
TRUE	ACZ_SYNC	21 44 76
TRUE	=USB2_LT_N	6 44
TRUE	=USB2_LT_P	6 44
TRUE	=USB2_EXCARD_N	6 44
TRUE	=USB2_EXCARD_P	6 44
TRUE	=PCIE_EXCARD_R2D_N	44 45
TRUE	=PCIE_EXCARD_R2D_P	44 45
TRUE	=PCIE_EXCARD_D2R_N	44 45
TRUE	=PCIE_EXCARD_D2R_P	44 45
TRUE	PCIE_CLK100M_EXCARD_P	34 44
TRUE	PCIE_CLK100M_EXCARD_N	34 44
TRUE	=USB2_MINI_N	6 44
TRUE	=USB2_MINI_P	6 44
TRUE	=PCIE_MINI_R2D_N	44 45
TRUE	=PCIE_MINI_R2D_P	44 45
TRUE	=PCIE_MINI_D2R_N	44 45
TRUE	=PCIE_MINI_D2R_P	44 45
TRUE	PCIE_CLK100M_MINI_P	34 44
TRUE	PCIE_CLK100M_MINI_N	34 44
TRUE	=SMBUS_LIO_SMC_SCL	27 44
TRUE	=SMBUS_LIO_SMC_SDA	27 44
TRUE	=SMBUS_LIO_SB_SCL	27 44
TRUE	=SMBUS_LIO_SB_SDA	27 44
TRUE	PCIE_WAKE_L	23 37 44

Left I/O Power Connector

FUNC_TEST

TRUE	=PPBUSA_G3H_LIO_CONN	62 63
TRUE	=PPBUSB_G3H_LIO_CONN	62 63
TRUE	GND	

Request for at least 10 GND test points

Functional / ICT Test

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	5	103

NC_CPU_A32_L — TP_CPU_A32_L (7)
MAKE_BASE=TRUE, NO_TEST=TRUE

NC_CPU_A33_L — TP_CPU_A33_L (7)
MAKE_BASE=TRUE, NO_TEST=TRUE

NC_CPU_A34_L — TP_CPU_A34_L (7)
MAKE_BASE=TRUE, NO_TEST=TRUE

NC_CPU_A35_L — TP_CPU_A35_L (7)
MAKE_BASE=TRUE, NO_TEST=TRUE

NC_CPU_A36_L — TP_CPU_A36_L (7)
MAKE_BASE=TRUE, NO_TEST=TRUE

NC_CPU_A37_L — TP_CPU_A37_L (7)
MAKE_BASE=TRUE, NO_TEST=TRUE

NC_CPU_A38_L — TP_CPU_A38_L (7)
MAKE_BASE=TRUE, NO_TEST=TRUE

NC_CPU_A39_L — TP_CPU_A39_L (7)
MAKE_BASE=TRUE, NO_TEST=TRUE

NC_CPU_APM0_L — TP_CPU_APM0_L (7)
MAKE_BASE=TRUE, NO_TEST=TRUE

NC_CPU_APM1_L — TP_CPU_APM1_L (7)
MAKE_BASE=TRUE, NO_TEST=TRUE

NC_CPU_EXTBREF — TP_CPU_EXTBREF (7)
MAKE_BASE=TRUE, NO_TEST=TRUE

NC_CPU_HFPLL — TP_CPU_HFPLL (7)
MAKE_BASE=TRUE, NO_TEST=TRUE

NC_CPU_SPARE0 — TP_CPU_SPARE0 (7)
MAKE_BASE=TRUE, NO_TEST=TRUE

NC_CPU_SPARE1 — TP_CPU_SPARE1 (7)
MAKE_BASE=TRUE, NO_TEST=TRUE

NC_CPU_SPARE2 — TP_CPU_SPARE2 (7)
MAKE_BASE=TRUE, NO_TEST=TRUE

NC_CPU_SPARE4 — TP_CPU_SPARE4 (7)
MAKE_BASE=TRUE, NO_TEST=TRUE

NC_MEM_A_A<15..14> — MEM_A_A<15..14> (28)
MAKE_BASE=TRUE, NO_TEST=TRUE

NC_MEM_B_A<15..14> — MEM_B_A<15..14> (29)
MAKE_BASE=TRUE, NO_TEST=TRUE

TP_NB_CFG<4..3> — NB_CFG<4..3> (14)
MAKE_BASE=TRUE

TP_NB_CFG<6> — NB_CFG<6> (14)
MAKE_BASE=TRUE

TP_NB_CFG<8> — NB_CFG<8> (14)
MAKE_BASE=TRUE

TP_NB_CFG<11..10> — NB_CFG<11..10> (14)
MAKE_BASE=TRUE

TP_NB_CFG<15..14> — NB_CFG<15..14> (14)
MAKE_BASE=TRUE

TP_NB_CFG<17> — NB_CFG<17> (14)
MAKE_BASE=TRUE

NOTE: NB_CFG<13..12> require test access

TP_NB_CFG<13..12> — NB_CFG<13..12> (14)
MAKE_BASE=TRUE

TP_SB_SUS_CLK — SUS_CLK_SB (23)
MAKE_BASE=TRUE

NC_ENET_CTRL12 — ENET_CTRL12 (37)
MAKE_BASE=TRUE, NO_TEST=TRUE

NC_ENET_CTRL25 — ENET_CTRL25 (37)
MAKE_BASE=TRUE, NO_TEST=TRUE

NC_FWPWR_PWRON — =FWPWR_PWRON (40)
MAKE_BASE=TRUE, NO_TEST=TRUE

FW_PC0 (39)

USB Port "A" (Debug Port) = Right USB 2.0 Port

=USB2_RT_P — USB2_RT_P — USB_A_P (43, 22)
MAKE_BASE=TRUE

=USB2_RT_N — USB2_RT_N — USB_A_N (43, 22)
MAKE_BASE=TRUE

=RTUSB_OC_L — RTUSB_OC_L — USB_A_OC_L (43, 22)
MAKE_BASE=TRUE

USB Port "B" = PCI-E Mini Card

=USB2_MINI_P — USB2_MINI_P — USB_B_P (44, 22)
MAKE_BASE=TRUE

=USB2_MINI_N — USB2_MINI_N — USB_B_N (44, 22)
MAKE_BASE=TRUE

UNUSED_USB_B_OC_L — USB_B_OC_L (22)
MAKE_BASE=TRUE

USB Port "C" = Left USB 2.0 Port

=USB2_LT_P — USB2_LT_P — USB_C_P (44, 22)
MAKE_BASE=TRUE

=USB2_LT_N — USB2_LT_N — USB_C_N (44, 22)
MAKE_BASE=TRUE

LTUSB_OC_L — USB_C_OC_L (44, 22)
MAKE_BASE=TRUE

USB Port "D" = Camera

=USB2_CAMERA_P — USB2_CAMERA_P — USB_D_P (42, 22)
MAKE_BASE=TRUE

=USB2_CAMERA_N — USB2_CAMERA_N — USB_D_N (42, 22)
MAKE_BASE=TRUE

UNUSED_USB_D_OC_L — USB_D_OC_L (22)
MAKE_BASE=TRUE

USB Port "E" = ExpressCard

=USB2_EXCARD_P — USB2_EXCARD_P — USB_E_P (44, 22)
MAKE_BASE=TRUE

=USB2_EXCARD_N — USB2_EXCARD_N — USB_E_N (44, 22)
MAKE_BASE=TRUE

EXCARD_OC_L — USB_E_OC_L (47, 44, 22)
MAKE_BASE=TRUE

USB Port "F" = Unused

TP_USBP_F — USB_F_P (22)
MAKE_BASE=TRUE

TP_USBN_F — USB_F_N (22)
MAKE_BASE=TRUE

USB Port "G" = Bluetooth (M13P)

=USB_BT_P — USB_BT_P — USB_G_P (42, 22)
MAKE_BASE=TRUE

=USB_BT_N — USB_BT_N — USB_G_N (42, 22)
MAKE_BASE=TRUE

USB Port "H" = Trackpad (Geyser)

=USB_TRACKPAD_P — USB_TRACKPAD_P — USB_H_P (42, 22)
MAKE_BASE=TRUE

=USB_TRACKPAD_N — USB_TRACKPAD_N — USB_H_N (42, 22)
MAKE_BASE=TRUE

Chassis connection to be made at the mounting hole northwest of the DVI connector

ZT0600
HOLE-VIA-P5RP25
1
GND_CHASSIS_DVI_TOP
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
MAKE_BASE=TRUE

=GND_CHASSIS_DVI2 (75)
=GND_CHASSIS_DVI3 (75)

Chassis connection to be made at the mounting hole southwest of the USB connector

ZT0601
HOLE-VIA-P5RP25
1
GND_CHASSIS_DVI_BOT
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
MAKE_BASE=TRUE

=GND_CHASSIS_DVI1 (75)
=GND_CHASSIS_DVI4 (75)
=GND_CHASSIS_ENET (38)
=GND_CHASSIS_FW_EMI (41)
=GND_CHASSIS_FW_PORT1 (41)
=GND_CHASSIS_RTUSB (43)

Chassis connection to be made at the mounting hole east of the LVDS connector

ZT0602
HOLE-VIA-P5RP25
1
GND_CHASSIS_LVDS
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
MAKE_BASE=TRUE

=GND_CHASSIS_LCD1 (74)
=GND_CHASSIS_LCD2 (74)
=GND_CHASSIS_LCD3 (74)
=GND_CHASSIS_LCD4 (74)

SH0600
OG-503040
SHLD-SM-LF
1
2
3
GND_CHASSIS_INVERTER
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
MAKE_BASE=TRUE

=GND_CHASSIS_INVERTER (74)

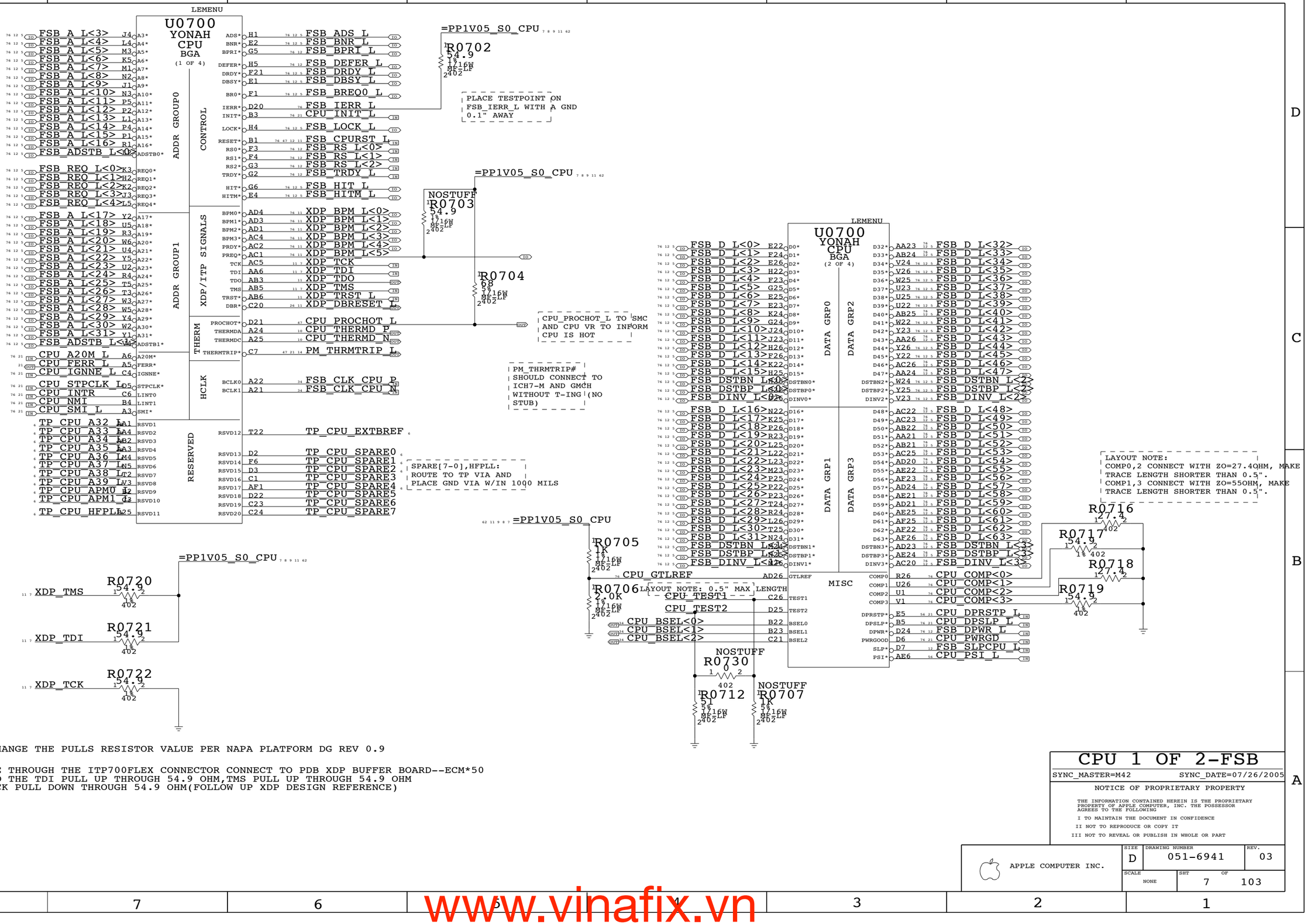
Signal Aliases

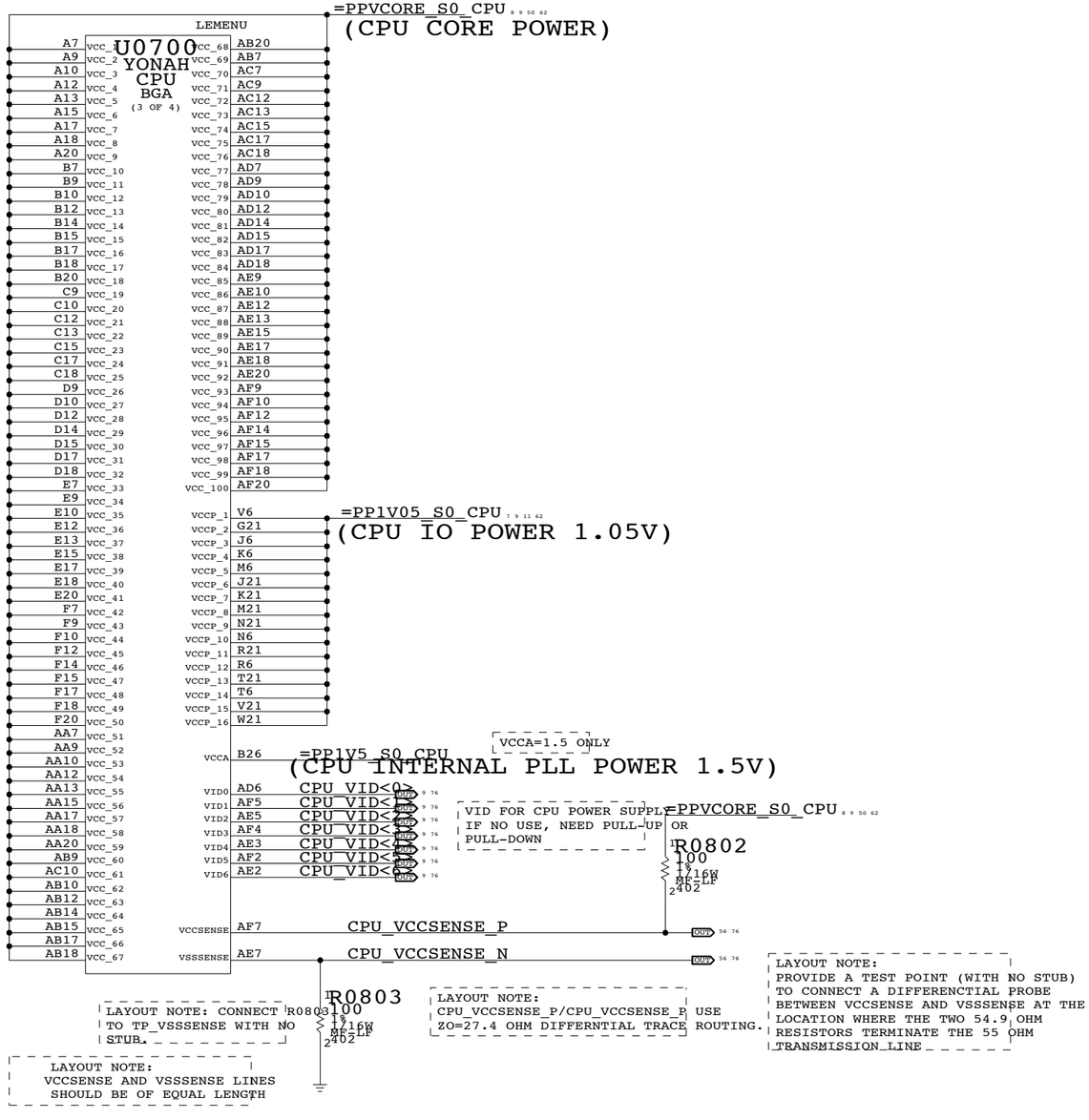
SYNC_MASTER=N/A SYNC_DATE=N/A

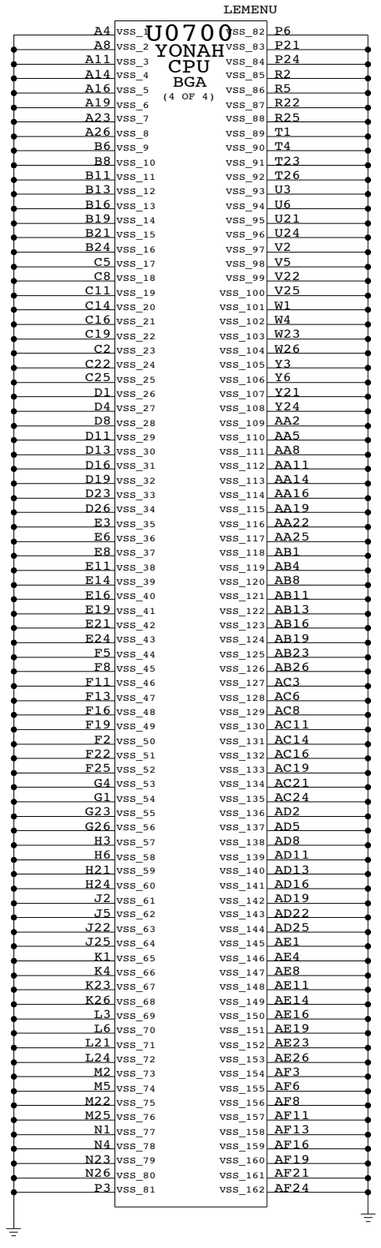
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	6	103







CPU 2 OF 2-PWR/GND

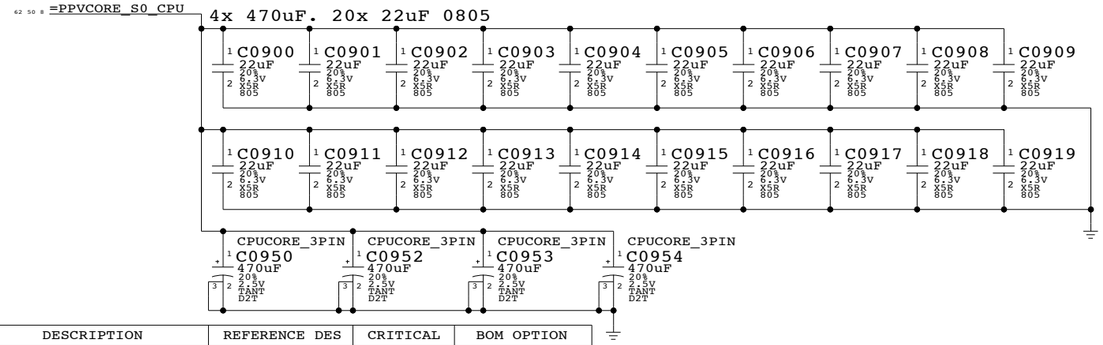
SYNC_MASTER=M42 SYNC_DATE=07/26/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	8	103

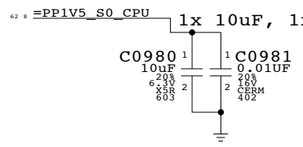
CPU VCORE HF AND BULK DECOUPLING



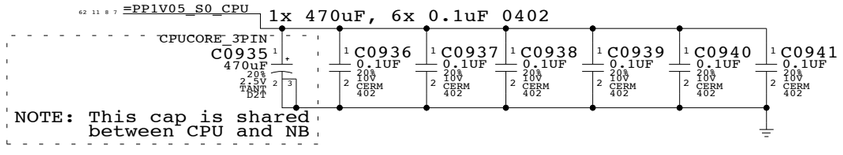
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
128S0074	4	CAP,TANT,POLY,470UF,20%,2.5V,7MOHM,D2E	C0950,C0952,C0953,C0954	CRITICAL	CPUCORE_2PIN

Need to make sure we can do dual-footprint for 128S0068 & 128S0074!!!

VCCA (CPU AVdd) Decoupling



VCCP (CPU I/O) Decoupling

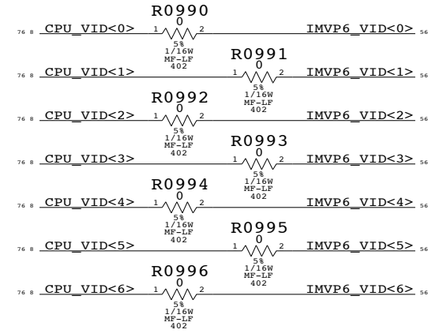


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
128S0074	1	CAP,TANT,POLY,470UF,20%,2.5V,7MOHM,D2E	C0935	CRITICAL	CPUCORE_2PIN

Need to make sure we can do dual-footprint for 128S0068 & 128S0074!!!

CPU VCORE VID Connections

Resistors to allow for override of CPU VID
Will probably be removed before production



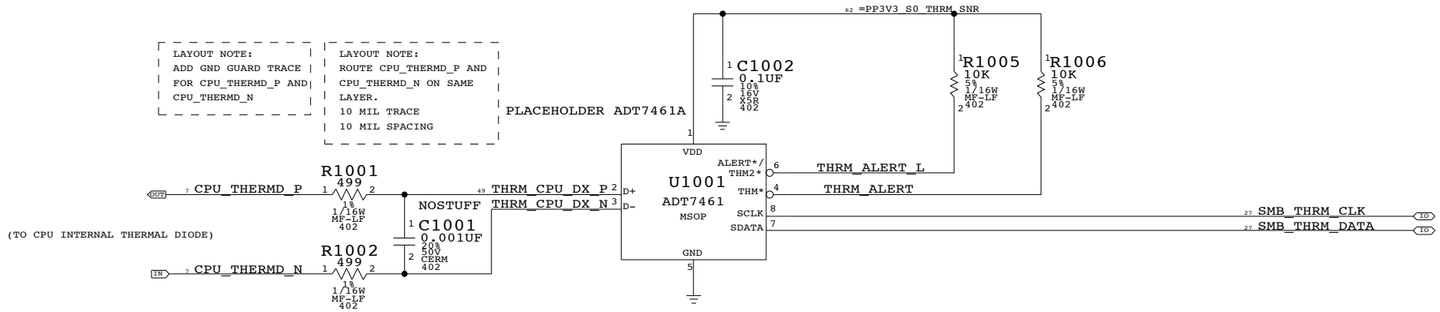
CPU Decoupling & VID

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03
SCALE: NONE	SHT 9 OF 103	

CPU ZONE THERMAL SENSOR



PLACE U1001 NEAR THE MCH

CPU MISC1-TEMP SENSOR

SYNC_MASTER=M42 SYNC_DATE=08/04/2005

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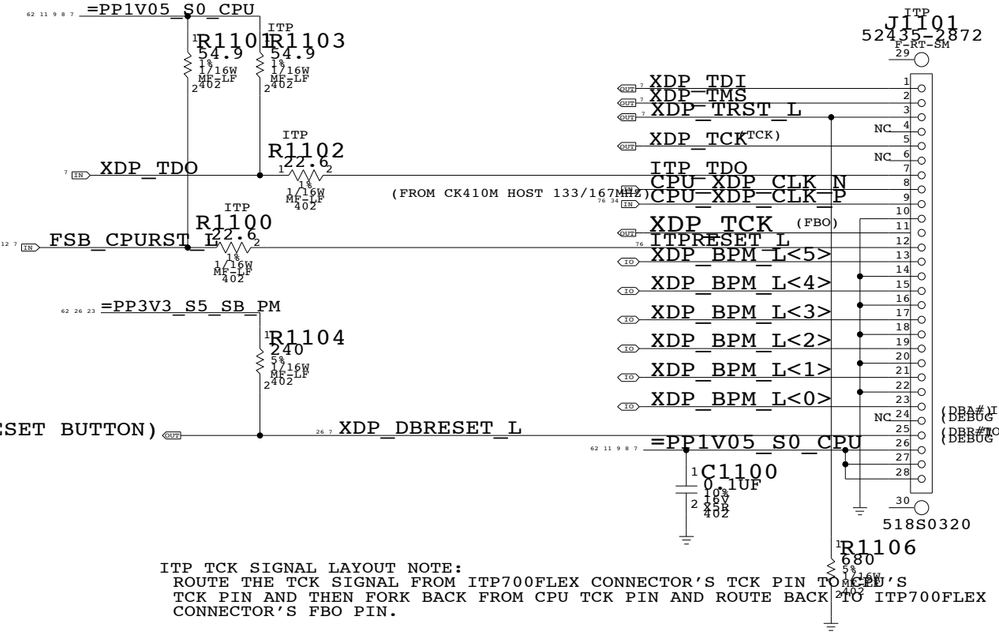
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	10	103

CPU ITP700FLEX DEBUG SUPPORT

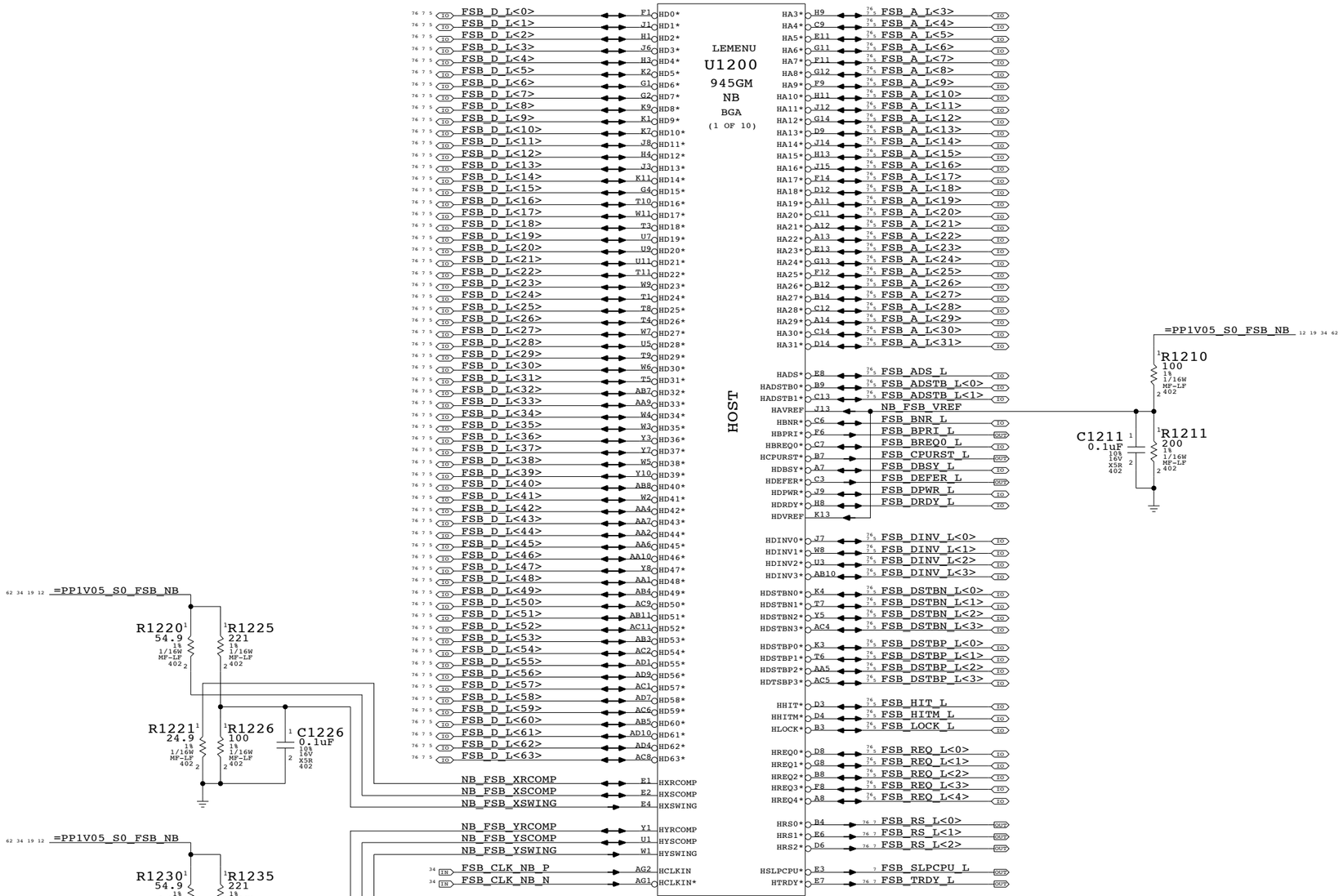


ITP TCK SIGNAL LAYOUT NOTE:
ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX CONNECTOR'S FBO PIN.

CPU ITP700FLEX DEBUG

SYNC_MASTER=M52 SYNC_DATE=07/26/2005

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6941	03
	SCALE: NONE	SHT 11 OF 103	



NB CPU Interface

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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LVDS Disable

Can leave all signals NC if LVDS is not implemented
Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
VCCD_LVDS must remain powered with proper decoupling.
Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

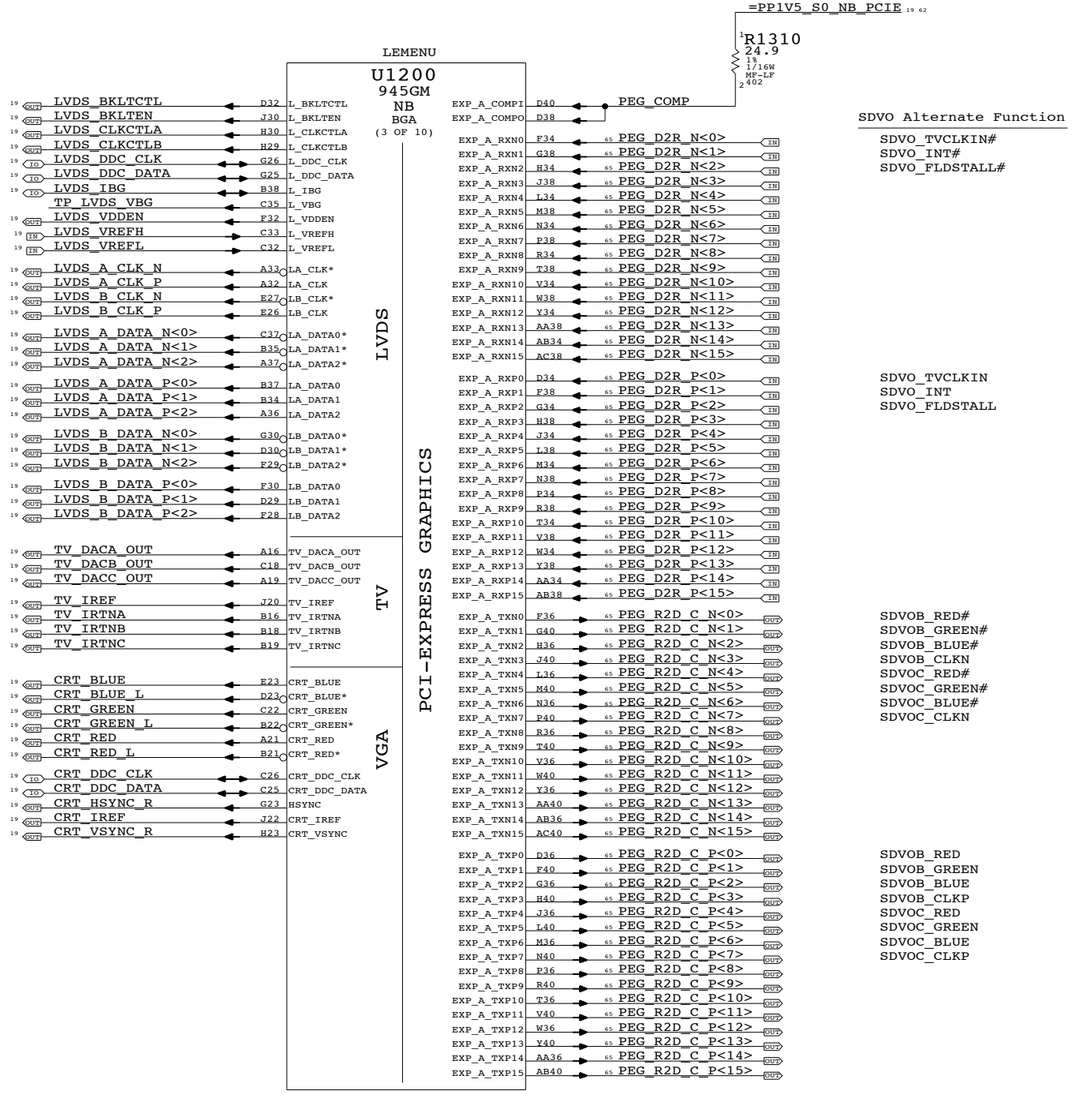
Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable

Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail.
Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and
VCCA_TVBG to 1.5V power rail. Tie VSSA_TVBG to GND.

CRT Disable

Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.



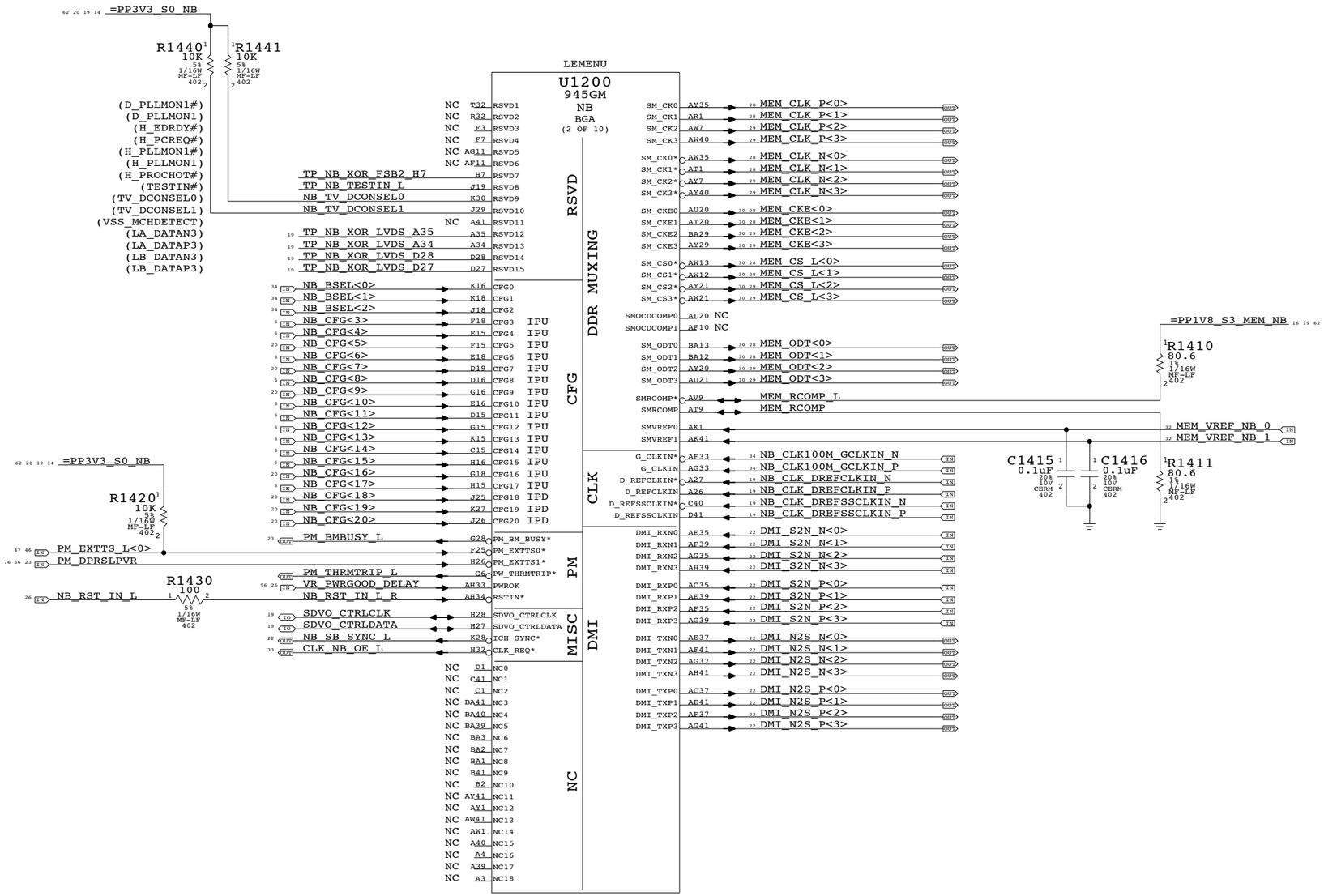
NB PEG / Video Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	13	103



NB Misc Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SIZE	DRAWING NUMBER	REV.
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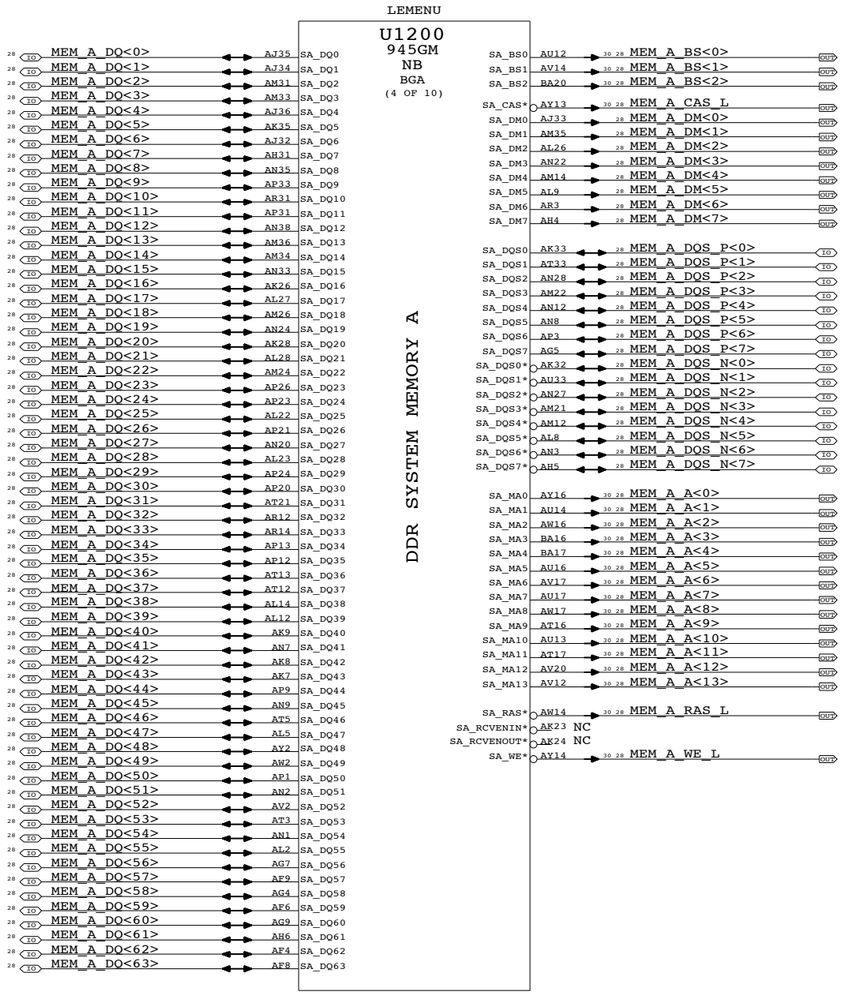
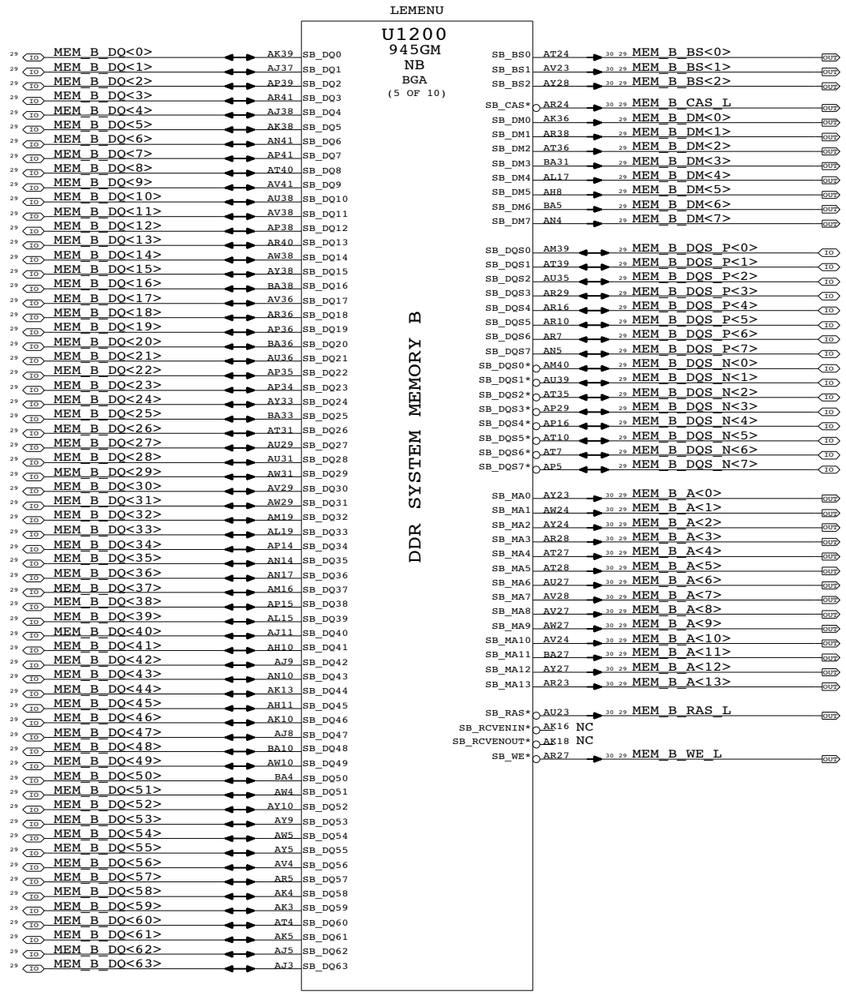
SCALE: NONE SHT 14 OF 103





NB DDR2 Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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D	051-6941	03
SCALE: NONE	SHT 15 OF 103	

NCTF balls are Not Critical To Function

These connections can break without impacting part performance.

=PPVCORE_S0_NB 16 19 62

1.05V or 1.5V

1.05V, Internal Graphics: 3500mA Max
1.05V, External Graphics: 1500mA Max
1.5V, Internal Graphics: 5500mA Max

U1200 945GM NB BGA (6 OF 10) LEMENU VCC

1.8V Max Current

Speed	1 Channel	2 Channel
400MTs	1300mA	2400mA
533MTs	1500mA	2800mA
667MTs	1700mA	3200mA

NB_VCCSM_LF4
NB_VCCSM_LF5

C1614 1 2 0.47uF 20% 6.3V CERM-X5R 402

C1613 1 2 0.47uF 20% 6.3V CERM-X5R 402

C1615 1 2 0.47uF 20% 6.3V CERM-X5R 402 62 19 14 =PP1V8_S3_MEM_NB

Layout Note: Place near pin BA23

C1620 1 2 10uF 20% 6.3V X5R 603

C1621 1 2 10uF 20% 6.3V X5R 603

Layout Note: Place in cavity

C1610 1 2 0.47uF 20% 6.3V CERM-X5R 402

Layout Note: Place near pin BA15

NB_VCCSM_LF2
NB_VCCSM_LF1

C1612 1 2 0.47uF 20% 6.3V CERM-X5R 402

C1611 1 2 0.47uF 20% 6.3V CERM-X5R 402

62 19 16 =PPVCORE_S0_NB

U1200 945GM NB BGA (7 OF 10) LEMENU NCTF

VCC_NCTF0 AD27
VCC_NCTF1 AC27
VCC_NCTF2 AB27
VCC_NCTF3 AA27
VCC_NCTF4 Y27
VCC_NCTF5 W27
VCC_NCTF6 V27
VCC_NCTF7 U27
VCC_NCTF8 T27
VCC_NCTF9 R27
VCC_NCTF10 AD26
VCC_NCTF11 AC26
VCC_NCTF12 AB26
VCC_NCTF13 AA26
VCC_NCTF14 Y26
VCC_NCTF15 W26
VCC_NCTF16 V26
VCC_NCTF17 U26
VCC_NCTF18 T26
VCC_NCTF19 R26
VCC_NCTF20 AD25
VCC_NCTF21 AC25
VCC_NCTF22 AB25
VCC_NCTF23 AA25
VCC_NCTF24 Y25
VCC_NCTF25 W25
VCC_NCTF26 V25
VCC_NCTF27 U25
VCC_NCTF28 T25
VCC_NCTF29 R25
VCC_NCTF30 AD24
VCC_NCTF31 AC24
VCC_NCTF32 AB24
VCC_NCTF33 AA24
VCC_NCTF34 Y24
VCC_NCTF35 W24
VCC_NCTF36 V24
VCC_NCTF37 U24
VCC_NCTF38 T24
VCC_NCTF39 R24
VCC_NCTF40 AD23
VCC_NCTF41 Y23
VCC_NCTF42 U23
VCC_NCTF43 T23
VCC_NCTF44 R23
VCC_NCTF45 AD22
VCC_NCTF46 V22
VCC_NCTF47 U22
VCC_NCTF48 T22
VCC_NCTF49 R22
VCC_NCTF50 AD21
VCC_NCTF51 V21
VCC_NCTF52 U21
VCC_NCTF53 T21
VCC_NCTF54 R21
VCC_NCTF55 AD20
VCC_NCTF56 V20
VCC_NCTF57 U20
VCC_NCTF58 T20
VCC_NCTF59 R20
VCC_NCTF60 AD19
VCC_NCTF61 V19
VCC_NCTF62 U19
VCC_NCTF63 T19
VCC_NCTF64 AD18
VCC_NCTF65 AC18
VCC_NCTF66 AB18
VCC_NCTF67 AA18
VCC_NCTF68 Y18
VCC_NCTF69 W18
VCC_NCTF70 V18
VCC_NCTF71 U18
VCC_NCTF72 T18

VSS_NCTF0 AE27
VSS_NCTF1 AE26
VSS_NCTF2 AE25
VSS_NCTF3 AE24
VSS_NCTF4 AE23
VSS_NCTF5 AE22
VSS_NCTF6 AE21
VSS_NCTF7 AE20
VSS_NCTF8 AE19
VSS_NCTF9 AE18
VSS_NCTF10 AC17
VSS_NCTF11 Y17
VSS_NCTF12 U17

=PP1V5_S0_NB_VCCAUX 17 19 62

VCCAUX_NCTF0 AG27
VCCAUX_NCTF1 AF27
VCCAUX_NCTF2 AG26
VCCAUX_NCTF3 AF26
VCCAUX_NCTF4 AG25
VCCAUX_NCTF5 AF25
VCCAUX_NCTF6 AG24
VCCAUX_NCTF7 AF24
VCCAUX_NCTF8 AG23
VCCAUX_NCTF9 AF23
VCCAUX_NCTF10 AG22
VCCAUX_NCTF11 AF22
VCCAUX_NCTF12 AG21
VCCAUX_NCTF13 AF21
VCCAUX_NCTF14 AG20
VCCAUX_NCTF15 AF20
VCCAUX_NCTF16 AG19
VCCAUX_NCTF17 AF19
VCCAUX_NCTF18 R19
VCCAUX_NCTF19 AG18
VCCAUX_NCTF20 AF18
VCCAUX_NCTF21 R18
VCCAUX_NCTF22 AG17
VCCAUX_NCTF23 AF17
VCCAUX_NCTF24 AE17
VCCAUX_NCTF25 AD17
VCCAUX_NCTF26 AB17
VCCAUX_NCTF27 AA17
VCCAUX_NCTF28 W17
VCCAUX_NCTF29 V17
VCCAUX_NCTF30 T17
VCCAUX_NCTF31 R17
VCCAUX_NCTF32 AG16
VCCAUX_NCTF33 AF16
VCCAUX_NCTF34 AE16
VCCAUX_NCTF35 AD16
VCCAUX_NCTF36 AC16
VCCAUX_NCTF37 AB16
VCCAUX_NCTF38 AA16
VCCAUX_NCTF39 Y16
VCCAUX_NCTF40 W16
VCCAUX_NCTF41 V16
VCCAUX_NCTF42 U16
VCCAUX_NCTF43 T16
VCCAUX_NCTF44 R16
VCCAUX_NCTF45 AG15
VCCAUX_NCTF46 AF15
VCCAUX_NCTF47 AE15
VCCAUX_NCTF48 AD15
VCCAUX_NCTF49 AC15
VCCAUX_NCTF50 AB15
VCCAUX_NCTF51 AA15
VCCAUX_NCTF52 Y15
VCCAUX_NCTF53 W15
VCCAUX_NCTF54 V15
VCCAUX_NCTF55 U15
VCCAUX_NCTF56 T15
VCCAUX_NCTF57 R15

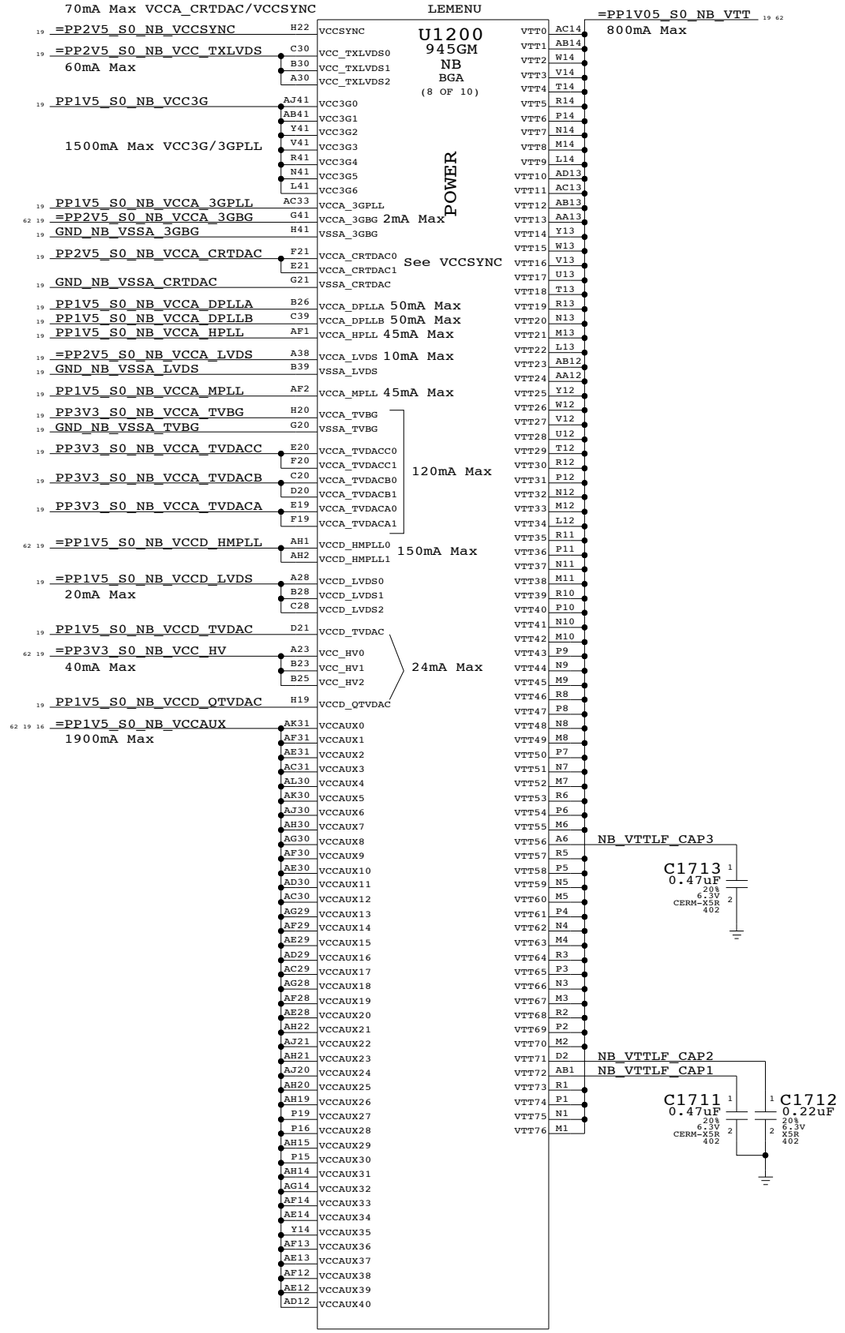
NB Power 1

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	16	103



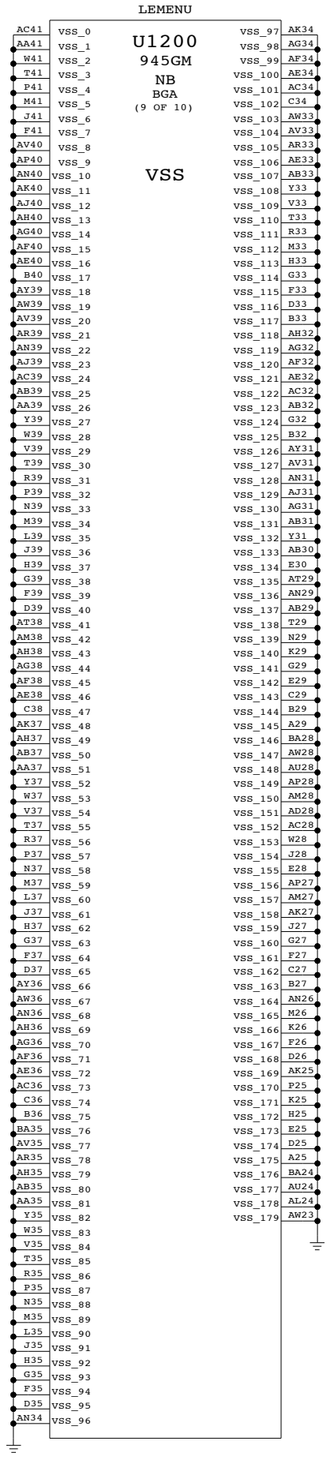
NB Power 2

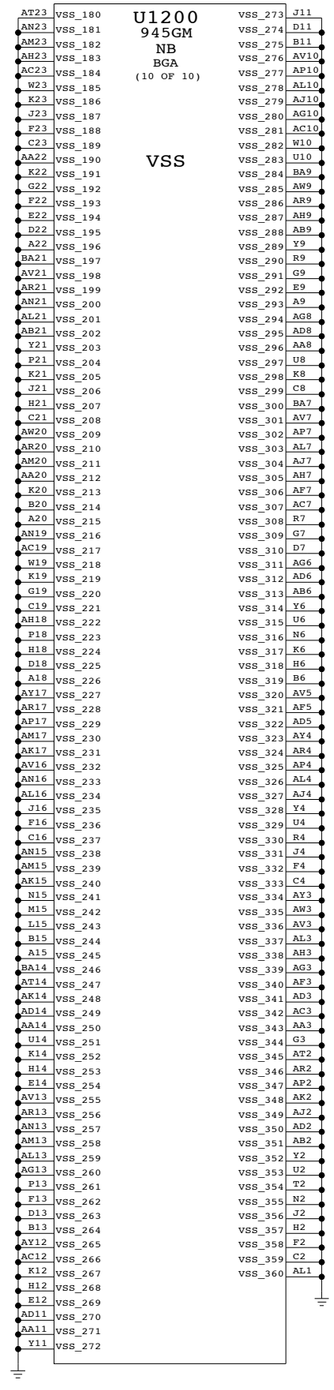
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	17	103





NB Grounds

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SCALE	SHT	OF
NONE	18	103

Power Interface

These are the power signals that leave the NB "block"

Rail Totals:

2310mA Max?	IN	=PPVCORE_S0_NB	16 19 62	1500mA Max
	IN	=PP1V05_S0_FSB_NB	12 34 62	10mA Max?
	IN	=PP1V05_S0_NB_VTT	17 19 62	800mA Max
	IN	=PP1V05_S0_NB_CRT	19 62	?mA Max
3674mA Max	IN	=PP1V5_S0_NB	62	?mA Max
	IN	=PP1V5_S0_NB_3G	19 62	1500mA Max
	IN	=PP1V5_S0_NB_3GPLL	19 62	
	IN	=PP1V5_S0_NB_PCIE	13 62	?mA Max
	IN	=PP1V5_S0_NB_PLL	19 62	100mA Max
	IN	=PP1V5_S0_NB_TVDAC	19 62	24mA Max
	IN	=PP1V5_S0_NB_VCCD_HMPLL	17 62	150mA Max
	IN	=PP1V5_S0_NB_VCCAUX	16 17 19 62	1900mA Max
3200mA Max	IN	=PP1V8_S3_MEM_NB	14 16 62	3200mA Max
	IN	=PP2V5_S0_NB_VCCSYNC	17 19	70mA Max
132mA Max	IN	=PP2V5_S0_NB_VCC_TXLVDS	17 19	60mA Max
	IN	=PP2V5_S0_NB_VCCA_3GBG	17 19 62	2mA Max
	IN	=PP3V3_S0_NB	14 20 62	?mA Max
40mA Max?	IN	=PP3V3_S0_NB_VCC_HV	17 19 62	40mA Max

62 19 =PP1V05_S0_NB_CRT
- CRT_RED — 13
- CRT_GREEN — 13
- CRT_BLUE — 13
- CRT_RED_L — 13
- CRT_GREEN_L — 13
- CRT_BLUE_L — 13
- CRT_IREF — 13
- CRT_HSYNC_R — 13
- CRT_VSYNC_R — 13

TP_CRT_DDC_CLK (MAKE_BASE=TRUE) — CRT_DDC_CLK — 13
TP_CRT_DDC_DATA (MAKE_BASE=TRUE) — CRT_DDC_DATA — 13

62 19 =PP1V5_S0_NB_TVDAC
- TV_DACA_OUT — 13
- TV_DACB_OUT — 13
- TV_DACC_OUT — 13
- TV_IREF — 13
- TV_IRTNA — 13
- TV_IRTNB — 13
- TV_IRTNC — 13

TP_LVDS_BKLTCTL (MAKE_BASE=TRUE) — LVDS_BKLTCTL — 13
TP_LVDS_BKLTEN (MAKE_BASE=TRUE) — LVDS_BKLTEN — 13
TP_LVDS_CLKCTLA (MAKE_BASE=TRUE) — LVDS_CLKCTLA — 13
TP_LVDS_CLKCTLB (MAKE_BASE=TRUE) — LVDS_CLKCTLB — 13
TP_LVDS_DDC_CLK (MAKE_BASE=TRUE) — LVDS_DDC_CLK — 13
TP_LVDS_DDC_DATA (MAKE_BASE=TRUE) — LVDS_DDC_DATA — 13
NC_LVDS_IBG (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_IBG — 13
TP_LVDS_VDDEN (MAKE_BASE=TRUE) — LVDS_VDDEN — 13
NC_LVDS_VREFH (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_VREFH — 13
TP_LVDS_VREFL (MAKE_BASE=TRUE) — LVDS_VREFL — 13
NC_LVDS_A_CLKP (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_A_CLK_P — 13
NC_LVDS_A_CLKN (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_A_CLK_N — 13
NC_LVDS_A_DATAP<2..0> (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_A_DATA_P<2..0> — 13
NC_LVDS_A_DATAN<2..0> (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_A_DATA_N<2..0> — 13
NC_LVDS_B_CLKP (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_B_CLK_P — 13
NC_LVDS_B_CLKN (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_B_CLK_N — 13
NC_LVDS_B_DATAP<2..0> (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_B_DATA_P<2..0> — 13
NC_LVDS_B_DATAN<2..0> (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_B_DATA_N<2..0> — 13
NC_NB_XOR_LVDS_A34 (MAKE_BASE=TRUE NO_TEST=TRUE) — TP_NB_XOR_LVDS_A34 — 14
NC_NB_XOR_LVDS_A35 (MAKE_BASE=TRUE NO_TEST=TRUE) — TP_NB_XOR_LVDS_A35 — 14
NC_NB_XOR_LVDS_D27 (MAKE_BASE=TRUE NO_TEST=TRUE) — TP_NB_XOR_LVDS_D27 — 14
NC_NB_XOR_LVDS_D28 (MAKE_BASE=TRUE NO_TEST=TRUE) — TP_NB_XOR_LVDS_D28 — 14
TP_SDVO_CTRLCLK (MAKE_BASE=TRUE) — SDVO_CTRLCLK — 14
TP_SDVO_CTRLDATA (MAKE_BASE=TRUE) — SDVO_CTRLDATA — 14

(MCH LVDS DATA/CLK TX 2.5V PWR)
=PP2V5_S0_NB_VCC_TXLVDS — 17 19
(MCH LVDS DIGITAL 1.5V PWR)
=PP1V5_S0_NB_VCCD_LVDS — 17
(MCH LVDS ANALOG 2.5V PWR)
=PP2V5_S0_NB_VCCA_LVDS — 17

NC_GND_NB_VSSA_LVDS (MAKE_BASE=TRUE NO_TEST=TRUE) — GND_NB_VSSA_LVDS — 17

62 19 16 =PPVCORE_S0_NB
- (MCH CRTDAC ANALOG 2.5V PWR)
- PP2V5_S0_NB_VCCA_CRTDAC — 17
- GND_NB_VSSA_CRTDAC — 17
- (MCH H/V SYNC 2.5V PWR)
- =PP2V5_S0_NB_VCCSYNC — 17 19

62 19 =PP1V5_S0_NB_TVDAC
- (MCH TV OUT CHANNEL A 3.3V PWR)
- PP3V3_S0_NB_VCCA_TVDACA — 17
- (MCH TV OUT CHANNEL B 3.3V PWR)
- PP3V3_S0_NB_VCCA_TVDACB — 17
- (MCH TV OUT CHANNEL C 3.3V PWR)
- PP3V3_S0_NB_VCCA_TVDACC — 17
- (MCH TV DAC BAND GAP 3.3V PWR)
- PP3V3_S0_NB_VCCA_TVBG — 17
- GND_NB_VSSA_TVBG — 17

(MCH DISPLAY A PLL 1.5V PWR)
TP_NB_VCCA_DPLLA (MAKE_BASE=TRUE) — PP1V5_S0_NB_VCCA_DPLLA — 17
(MCH DISPLAY B PLL 1.5V PWR)
TP_NB_VCCA_DPLLB (MAKE_BASE=TRUE) — PP1V5_S0_NB_VCCA_DPLLB — 17

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
128S0074	1	CAP,TANT,POLY,470UF,20%,2.5V,7MOHM,D2E	C1900	CRITICAL	CPUCORE_2PIN

Need to make sure we can do dual-footprint for 128S0068 & 128S0074!!!

62 19 16 =PPVCORE_S0_NB, 1500mA Max — GMCH CORE PWR 1.05V BYPASS

CPUCORE_3PIN
- C1900 470UF 20% 2.5V TANT D2E
- C1902 10uF 20% 6.3V X5R 603
- C1903 10uF 20% 6.3V X5R 603
- C1904 1uF 10% 6.3V CERM 402
- C1905 0.22uF 20% 25V X5R 402
- C1906 0.22uF 20% 25V X5R 402
- C1907 0.22uF 20% 25V X5R 402

62 19 17 =PP1V05_S0_NB_VTT, 800mA Max — MCH VTT BYPASS (MCH FSB 1.05V PWR)

(SHARE C0940 470UF)
- C1965 4.7uF 20% 6.3V CERM 603
- C1966 2.2uF 20% 6.3V CERM1 603

Layout Note: Place in cavity

- C1967 0.22uF 20% 6.3V X5R 402

Layout Note: Place on the edge

62 19 17 =PP3V3_S0_NB_VCC_HV, 40mA Max — MCH VCC_HV BYPASS (MCH HV BUFFER 3.3V PWR)
- C1914 10uF 20% 6.3V X5R 603
- C1915 0.1uF 20% 10V CERM 402

MCH VCCA_3GBG BYPASS (MCH PCIE/DMI BAND GAP 2.5V PWR)

62 19 17 =PP2V5_S0_NB_VCCA_3GBG, 2mA Max
- C1916 0.1uF 20% 10V CERM 402

GMCH VCCAUX FILTER (MCH DDR DLL&IO, FSB HSIO&IO PWR 1.5V)

62 19 17 16 =PP1V5_S0_NB_VCCAUX, 1900mA Max
- C1918 0.1uF 20% 10V CERM 402

NB_CLK_DREFCLKIN_P — 14
NB_CLK_DREFCLKIN_N — 14
NB_CLK_DREFSSCLKIN_P — 14
NB_CLK_DREFSSCLKIN_N — 14

62 19 =PP1V5_S0_NB_TVDAC, 24mA Max
- C1921 22000pF-1000mA 16V NPM18 — GMCH VCCD_TVDAC FILTER (MCH TVDAC DEDICATED PWR 1.5V) — PP1V5_S0_NB_VCCD_TVDAC — 17 (MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=1.5V) — 24mA Max TVDAC/QTVDAC
- C1920 0.1uF 20% 10V CERM 402

Layout Note: These 4 caps should be within 6.35 mm of NB edge

- L1922 180-OHM-1.5A 0603 — PP1V5_S0_NB_QTVDAC (MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=1.5V)
- C1923 22000pF-1000mA 16V NPM18 — GMCH VCCD_QTVDAC FILTER (MCH TVDAC DIGITAL QUIET 1.5V PWR) — PP1V5_S0_NB_VCCD_QTVDAC — 17 (MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=1.5V)
- C1922 0.1uF 20% 10V CERM 402

1500mA Max — 62 19 =PP1V5_S0_NB_3G
- L1970 91nH 2010
- C1970 220UF 20% 2.5V POLY SMB2

Layout Note: Place L and C close to MCH

- C1971 10uF 20% 6.3V X5R 603
- C1972 10uF 20% 6.3V X5R 603

Layout Note: 10uF caps should be close to MCH on opposite side.

GMCH VCC3G FILTER (PCI-E/DMI ANALOG 1.5V PWR)
PP1V5_S0_NB_VCC3G — 17 (MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.4 mm VOLTAGE=1.5V)

1500mA Max

62 19 =PP1V5_S0_NB_3GPLL, 1.0UH-220MA-0.12-OHM
- L1975 0805 — PP1V5_S0_NB_3GPLL_F (MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.4 mm VOLTAGE=1.5V)
- R1975 0.51 1% 1/16W MF-LF 402
- C1975 10uF 20% 6.3V X5R 603
- C1976 0.1uF 20% 10V CERM 402

GMCH VCCA_3GPLL FILTER (3GIO PLL 1.5V PWR)
PP1V5_S0_NB_VCCA_3GPLL — 17 (MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.4 mm VOLTAGE=1.5V)

Layout Note: 3GPLL 10uF cap should be placed in cavity

GND_NB_VSSA_3GBG — 17

Layout Note: Route to caps, then GND

62 19 =PP1V5_S0_NB_PLL, 100mA Max
- L1934 FERR-120-OHM-0.2A 0603 — GMCH VCCA_HPLL FILTER (HOST PLL 1.5V PWR) — PP1V5_S0_NB_VCCA_HPLL — 17 (MIN_LINE_WIDTH=0.38 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=1.5V) — 45mA Max
- C1934 22uF 20% 6.3V X5R 805
- C1935 0.1uF 20% 10V CERM 402
- L1936 FERR-120-OHM-0.2A 0603 — GMCH VCCA_MPLL FILTER (MCH MEMORY PLL 1.5V PWR) — PP1V5_S0_NB_VCCA_MPLL — 17 (MIN_LINE_WIDTH=0.38 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=1.5V) — 45mA Max
- C1936 22uF 20% 6.3V X5R 805
- C1937 0.1uF 20% 10V CERM 402

NB (GM) Decoupling

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03
SCALE: NONE	SHT 19 OF 103	

NB_CFG<3>	RESERVED

NB_CFG<4>	RESERVED

14 NB_CFG<5>
Internal pull-up

NB_CFG<5> DMI x2 Select	High = DMIx4 Low = DMIx2

NBCFG_DMI_X2
R2075
2.2K
5%
1/16W
MF-LF
402

PROBABLY NOT NEEDED

NB_CFG<6>	RESERVED

14 NB_CFG<7>
Internal pull-up

NB_CFG<7> CPU Strap	High = Mobile CPU Low = RESERVED

NO STUFF
R2077
2.2K
5%
1/16W
MF-LF
402

NB_CFG<8>	RESERVED

14 NB_CFG<9>
Internal pull-up

NB_CFG<9> PCIE Graphics Lane Reversal	High = Normal Low = Reversed

NBCFG_PEG_REVERSE
R2079
2.2K
5%
1/16W
MF-LF
402

NB_CFG<10>	RESERVED

NB_CFG<11>	RESERVED

Internal pull-ups

NB_CFG<13:12>	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal Operation

NB_CFG<14>	RESERVED

NB_CFG<15>	RESERVED

14 NB_CFG<16>
Internal pull-up

NB_CFG<16> FSB Dynamic ODT	High = Enabled Low = Disabled

NBCFG_DYN_ODT_DISABLE
R2085
2.2K
5%
1/16W
MF-LF
402

NB_CFG<17>	RESERVED

=PP3V3_S0_NB 14 19 20 62
NBCFG_VCC_1V5
R2058
2.2K
5%
1/16W
MF-LF
402

NB_CFG<18> VCC Select	High = 1.5V Low = 1.05V

14 NB_CFG<18>
Internal pull-down

=PP3V3_S0_NB 14 19 20 62
NBCFG_DMI_REVERSE
R2059
2.2K
5%
1/16W
MF-LF
402

NB_CFG<19> DMI Lane Reversal	High = Reversed Low = Normal

14 NB_CFG<19>
Internal pull-down

945 External Design Spec says reserved

=PP3V3_S0_NB 14 19 20 62
NBCFG_SDVO_AND_PCIE
R2060
2.2K
5%
1/16W
MF-LF
402

NB_CFG<20> PCIe Backward Interop. Mode	High = Both active Low = Only SDVO or PCIe x1

14 NB_CFG<20>
Internal pull-down

PROBABLY NOT NEEDED

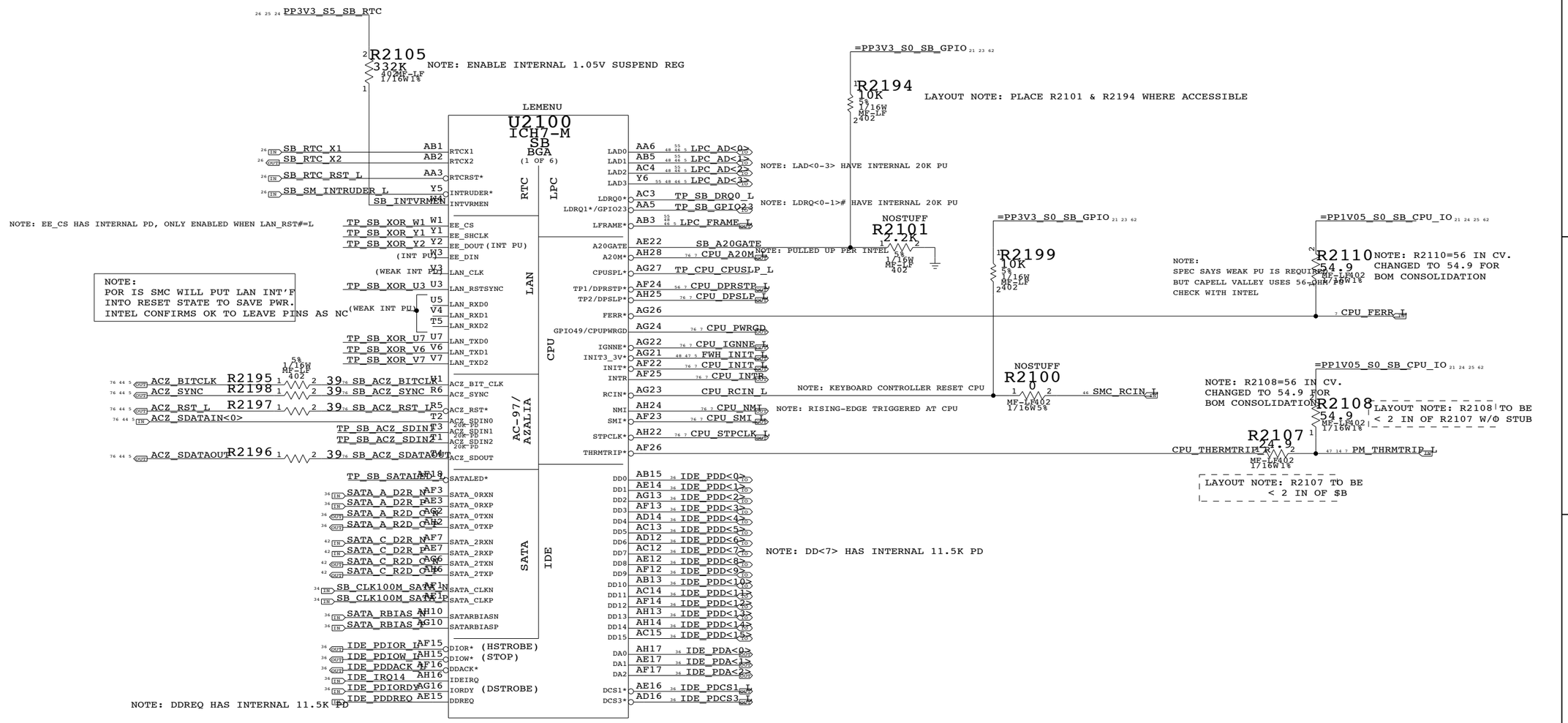
NB Config Straps

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	20	103

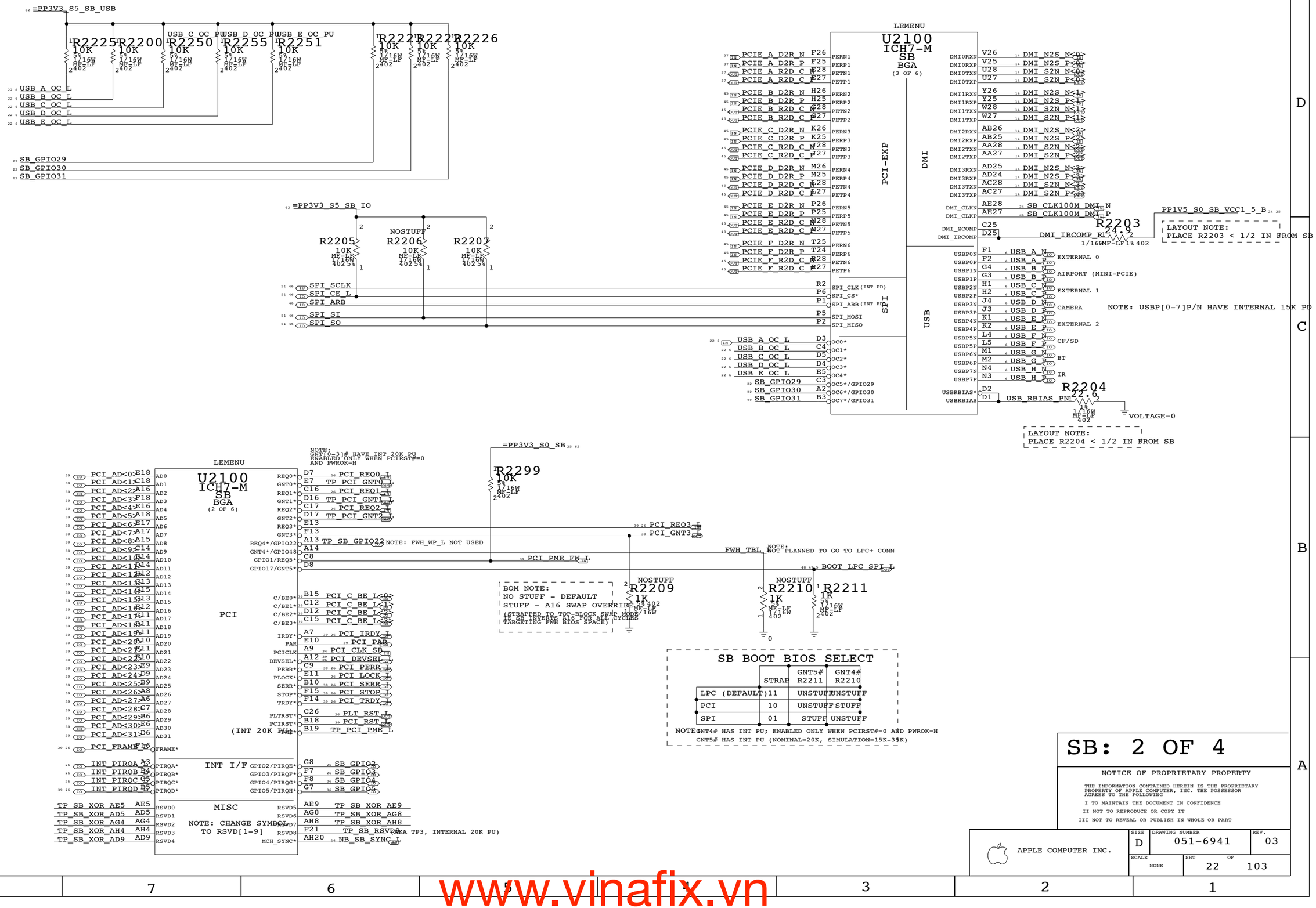


	AC '07	INTEL HIGH DEFINITION AUDIO
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN	INTERNAL 20K PD ONLY ENABLED IN S3COLD
ACZ_RST#	- LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	NONE
ACZ_SDIN[0-2]	INTERNAL 20K PD	INTERNAL 20K PD
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
ACZ_SYNC		INTERNAL 20K PD

SB: 1 OF 4

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03
SCALE: NONE	SHT: 21 OF: 103	



NOTE FOR R2323 (DEF=NOSTUFF)
STRAPPING 8 PWROK_RISING:
SB WILL DISABLE TCO TIMER
SO AVOID UNWANTED SYSTEM REBOOT FEATURE

=PP3V3_S0_SB_GPIO 21 23 62

=PP3V3_S5_SB 23 25 62

62 25 23 =PP3V3_S5_SB

R2318 10K 1/16W 402 2MF-LF 5%
R2395 8.2K 1/16W 402 2MF-LF 5%
R2396 10K 1/16W 402 2MF-LF 5%
R2397 8.2K 1/16W 402 2MF-LF 5%
R2327 10K 1/16W 402 2MF-LF 5%
R2326 10K 1/16W 402 2MF-LF 5%
R2323 1K 1/16W 402 2MF-LF 5%
NOSTUFF
NO_REBOOT_MODE

RP2300 10K 5% 1/16W 8M-LF

R2398 1K 1/16W 402 2MF-LF 5%
R2320 10K 1/16W 402 2MF-LF 5%
R2317 10K 1/16W 402 2MF-LF 5%
R2316 10K 1/16W 402 2MF-LF 5%

LEMENU
U2100
ICH7-M SB
BGA
(4 OF 6)

SMB_CLK 27 TO — C22 SMBCLK
SMB_DATA 27 TO — B22 SMBDATA
SMB_LINK_ALERT_L — A26 SMLINKALERT*
SMLINK<0> — B25 SMLINK0
SMLINK<1> — A25 SMLINK1
NOT USED
PM_RI_L — A28 RI*
SB_SPKR — A19 SPKR (INT WEAK PD)
PM_SUS_STAT_L 55 48 46 5 OUT — A27 SUS_STAT*
PM_SYSRST_L 46 26 IN — A22 SYS_RST*
PM_BMBUSY_L 14 IN — AB18 GPIO0/BM_BUSY*
SMB_ALERT_L — B23 GPIO11/SMBALERT*
NOTE: RESERVED FOR FUTURE
PM_STPPCI_L 33 OUT — AC20 GPIO18/STPPCI*
PM_STPCPU_L 34 OUT — AF21 GPIO20/STPCPU*
SB_GPIO26 IN — A21 GPIO26
BIOS_REC 23 — B21 GPIO27
FWH_MFG_MODE 23 — E23 GPIO28
PM_CLKRUN_L 55 48 46 39 5 TO — AG18 GPIO32/CLKRUN*
RESERVED FOR MOBILE
AZALIA DOCKING INTF
TP_AZ_DOCK_EN1 — AG19 GPIO33/AZ_DOCK_EN*
TP_AZ_DOCK_RST1_L — AG22 GPIO34/AZ_DOCK_RST*
PCIE_WAKE_L 44 37 5 IN — F20 WAKE*
INT_SERIRQ 55 48 46 5 TO — AH21 SERIRQ
PM_THRM_L 46 IN — AF20 THRM*
VR_PWRGD_CK410 26 IN — AD22 VRMPWRGD
TP_SB_GPIO6 TO — AC21 GPIO6
SB_RUNTIME_SCI_L — AC18 GPIO7
SB_EXTSMI_L — E21 GPIO8

SMB

SATA GPIO
GPIO21/SATA0GP — AF19 SB_GPIO21 100 1 2 R2302
GPIO19/SATA1GP — AH18 SB_GPIO19 100 1 2 R2303
GPIO36/SATA2GP — AH19
GPIO37/SATA3GP — AE19 SB_GPIO37 100 1 2 R2305
36 SATA_C_DET_L IN

CLKS
CLK14 — AC1 34 SB_CLK14P3M_TIMER IN
CLK48 — B2 34 SB_CLK48M_USBCTLR IN
SUSCLK — C20 6 SUS_CLK_SB OUT

SYS GPIO
PWR MNGT
SLP_S3* — B24 64 46 PM_SLP_S3_L OUT
SLP_S4* — D23 64 46 PM_SLP_S4_L OUT
SLP_S5* — F22 46 PM_SLP_S5_L OUT
PWROK — AA4 26 PM_SB_PWROK IN
GPIO16/DPRSLPVR — AC22 76 56 14 PM_DPRSLPVR OUT
TP0/BATLOW* — C21 NOTE: DPRSLPVR HAS INT 20K PD, ENABLED AT BOOT/RESET FOR STRAPPING FCN
(INT 20K PU) PWRBTN* — C23 46 PM_PWRBTN_L IN
LAN_RST* — C19 46 PM_LAN_ENABLE IN NOTE: SMC WILL DRIVE 0-1-0 TO KEEP LAN INT'F IN RESET STATE TO SAVE PWR
RSMRST* — Y4

GPIO

GPIO9 — E20 47 46 SMS_INT_L IN
GPIO10 — A20 46 SMC_SB_NMI IN
DEF=GPI GPIO12 — F19 23 PATA_PWR_EN_L OUT
GPIO13 — E19
DEF=GPI GPIO14 — R4 36 23 IDE_RESET_L OUT
GPIO15 — E22 SV_SET_UP 5 23 48
GPIO24 — R3 CRB_SV_DET 23
GPIO25 — D20 TP_SB_GPIO25_DO_NOT_USE
OD GPIO35 — AD21 33 SB_CLK100M_SATA_OE_L OUT
GPIO38 — AD20 TP_SB_GPIO38 NC
DEF=GPI GPIO39 — AE20 23 SATA_C_PWR_EN_L OUT

=PP3V3_S5_SB_PM 11 26 62

R2319 10K 1/16W 402 2MF-LF 5%
R2343 8.2K 1/16W 402 2MF-LF 5%

46 PM_BATLOW_L IN
46 PM_RSMRST_L IN
R2399 100K 5% 1/16W 402 2MF-LF
46 SMC_WAKE_SCI_L IN

NOTE FOR GPIO25:
- HAS INTERNAL 20K PU, ENABLED DURING RSMRST# AND DISABLED WITHIN 100MS AFTER RSMRST# DEASSERTS
- CAN NOT BE LOW FOR 35US AFTER RSMRST# ON BOOT (DMI AC COUPLING MODE STRAP)

NOSTUFF
R2300 0 1/16W 402 2MF-LF 5%
R2301 0 1/16W 402 2MF-LF 5%
46 SMC_RUNTIME_SCI_L IN
46 SMC_EXTSMI_L IN

62 23 21 =PP3V3_S0_SB_GPIO

R2306 NOSTUFF 10K 1/16W 402 2MF-LF 5%
R2308 10K 1/16W 402 2MF-LF 5%
SV_SET_UP 1 23 48
CRB_SV_DET 23

NOTE:
SV_SET_UP IS LINDACARD DETECT
HI = PRESENT
LO = NOT PRESENT

LAYOUT NOTE:
PLACE R2306-14 WHERE PHYSICALLY ACCESSIBLE

R2307 10K 1/16W 402 2MF-LF 5%
R2309 NOSTUFF 0 1/16W 402 2MF-LF 5%

62 25 23 =PP3V3_S5_SB

R2313 10K 1/16W 402 2MF-LF 5%
R2310 10K 1/16W 402 2MF-LF 5%
FWH_MFG_MODE 23
BIOS_REC 23

R2314 NOSTUFF 0 1/16W 402 2MF-LF 5%
R2311 NOSTUFF 10K 1/16W 402 2MF-LF 5%

=PP3V3_S0_SB_GPIO 21 23 62

R2390 10K 5% 1/16W 402 2MF-LF
R2389 10K 5% 1/16W 402 2MF-LF
R2388 10K 5% 1/16W 402 2MF-LF

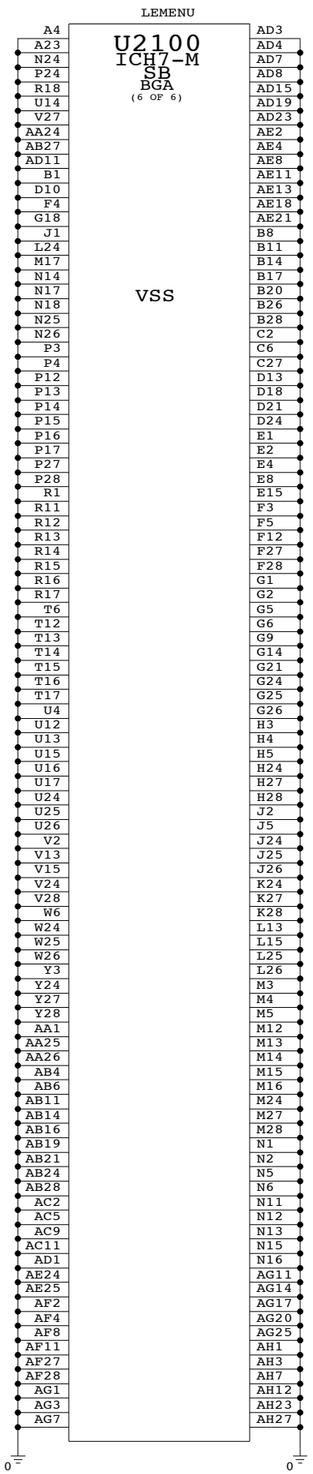
23 PATA_PWR_EN_L
36 23 IDE_RESET_L
23 SATA_C_PWR_EN_L

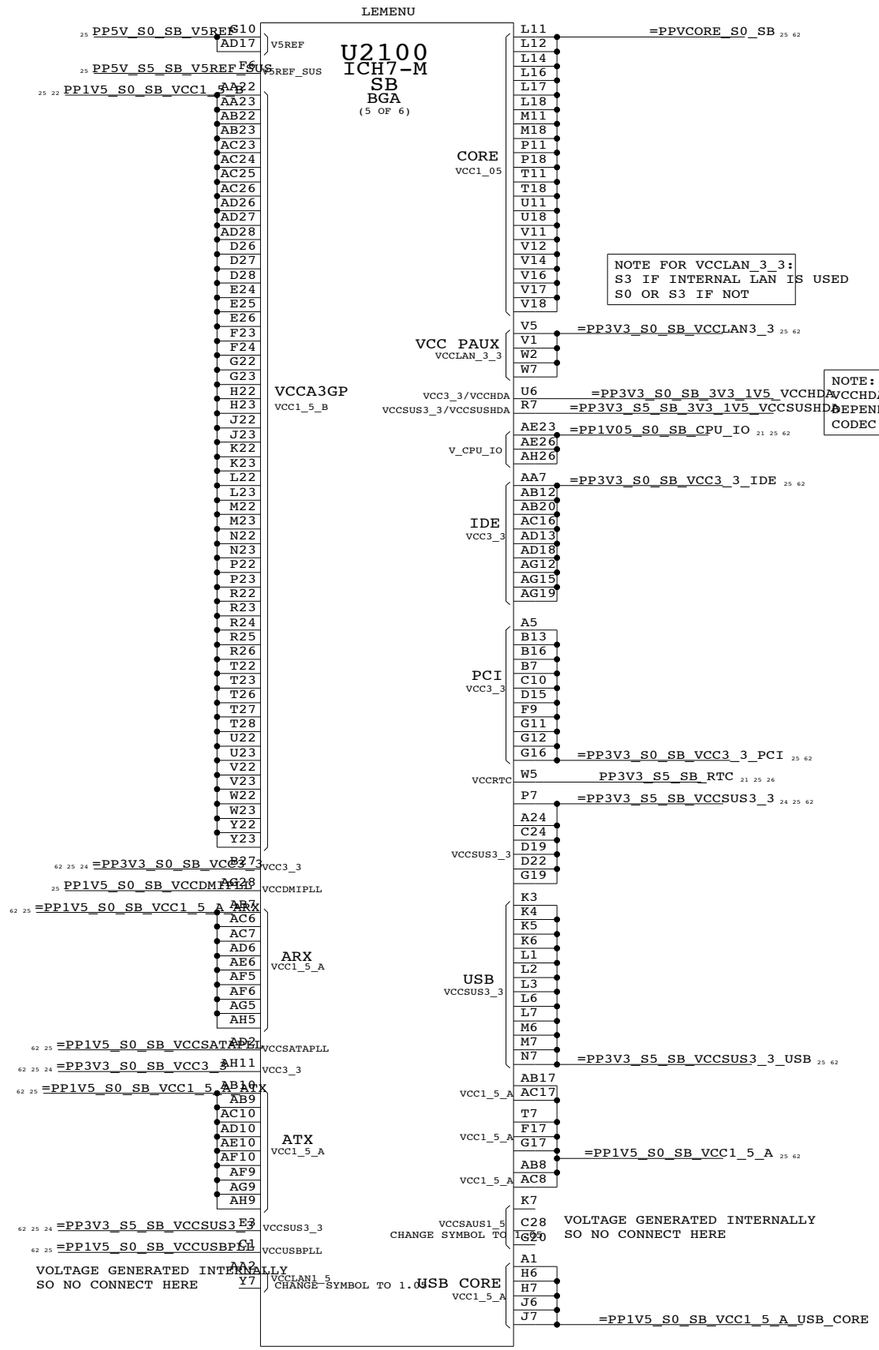
SB: 3 OF 4

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	23	103



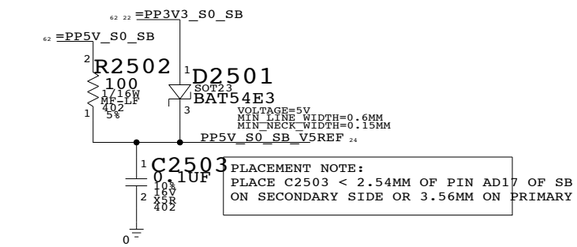


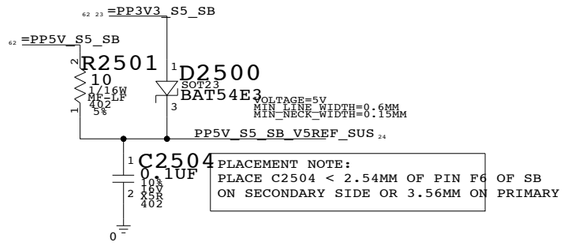
SB: 4 OF 4

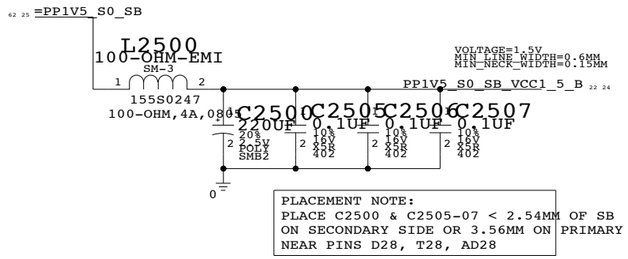
APPLE COMPUTER INC.

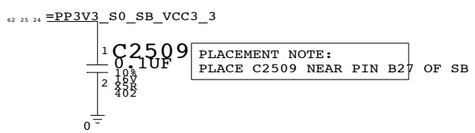
SIZE	DRAWING NUMBER	REV.
D	051-6941	03

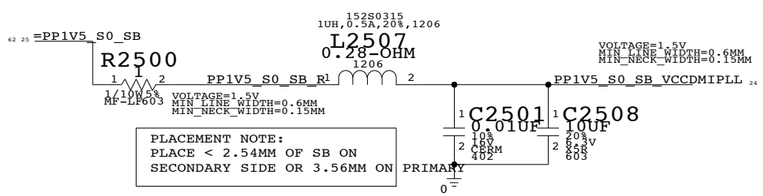
SCALE	SHT	OF
NONE	24	103

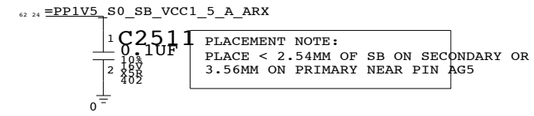


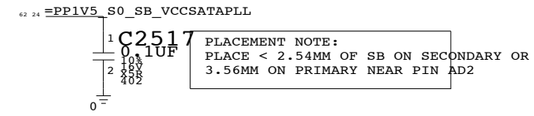


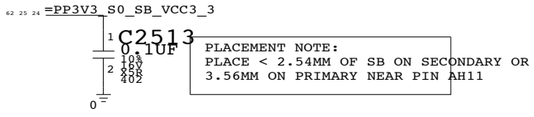


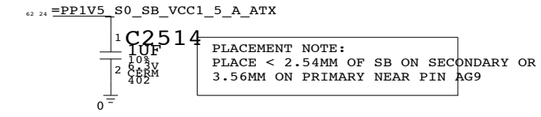


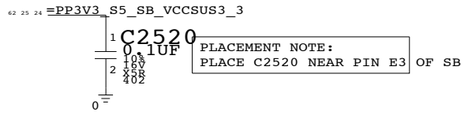


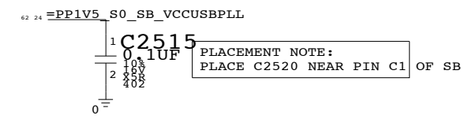


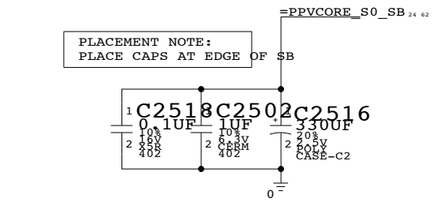


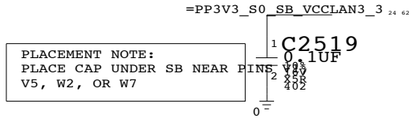


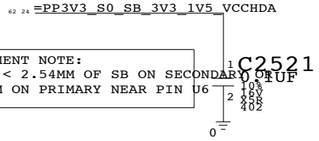


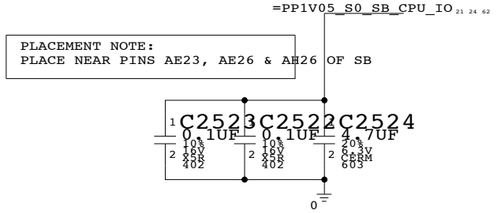


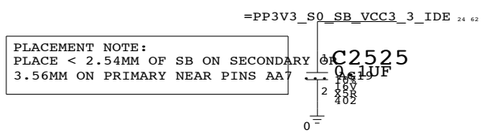


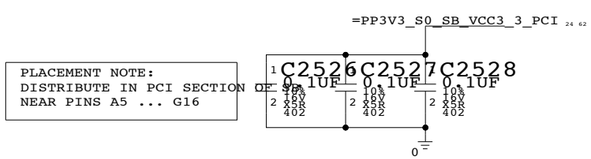


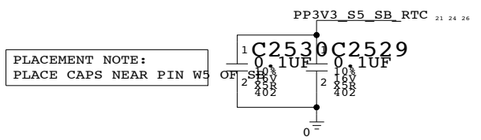


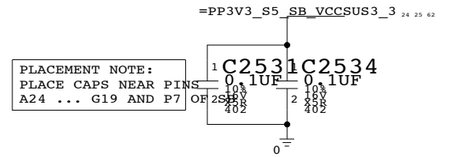


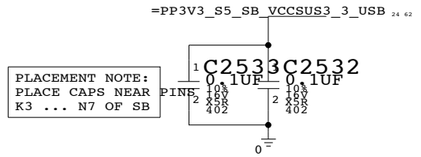


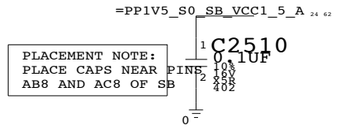


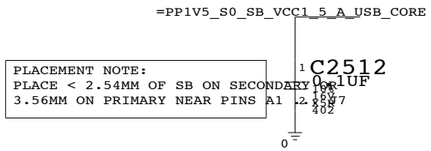










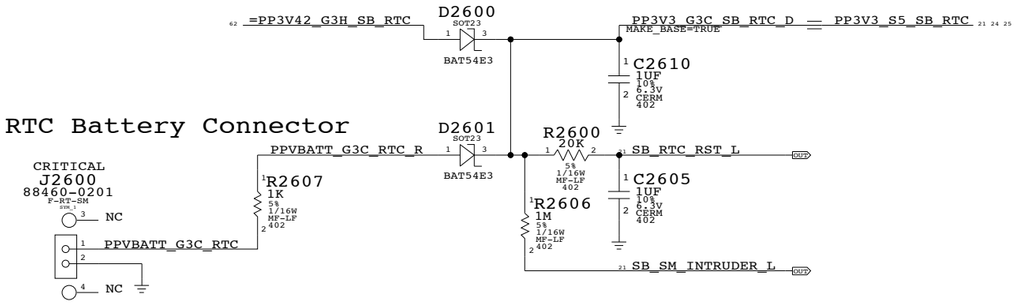


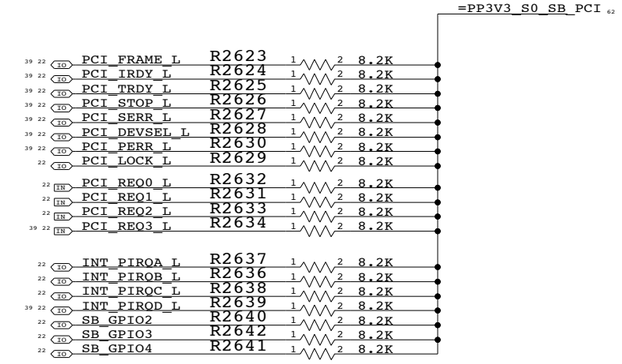
SB: 4 OF 4

APPLE COMPUTER INC.

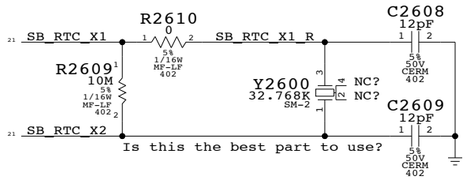
SIZE	DRAWING NUMBER	REV.
D	051-6941	03

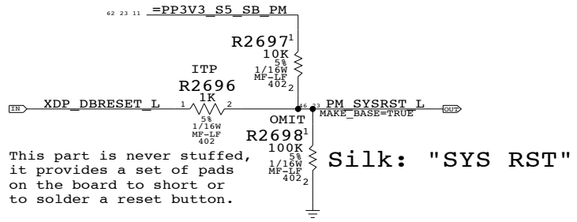
SCALE	SHT	OF
NONE	25	103





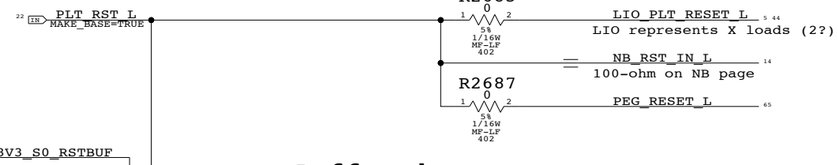
SB RTC Crystal Circuit



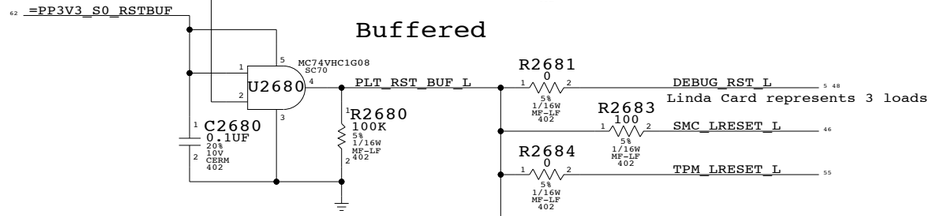


Platform Reset Connections

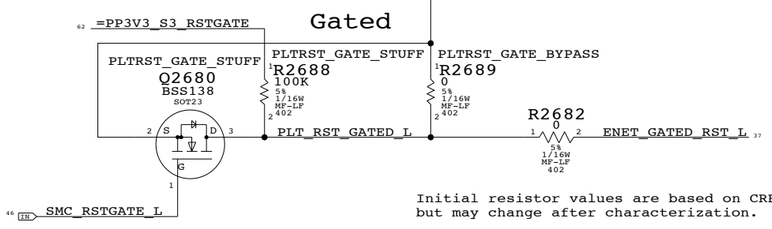
Unbuffered



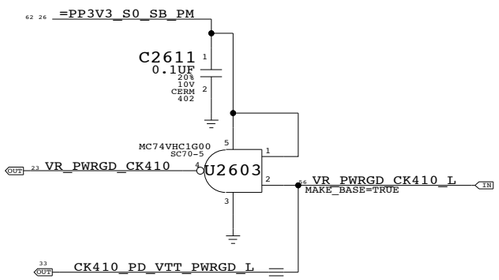
Buffered



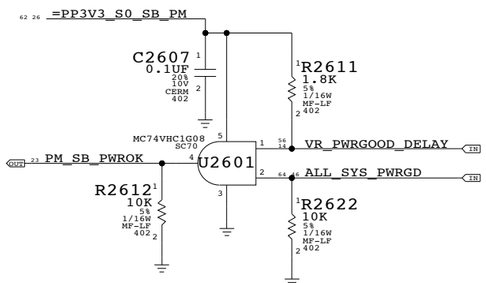
Gated



Initial resistor values are based on CRB,
but may change after characterization.



1G00 used as small & cheap inverter



SB Misc

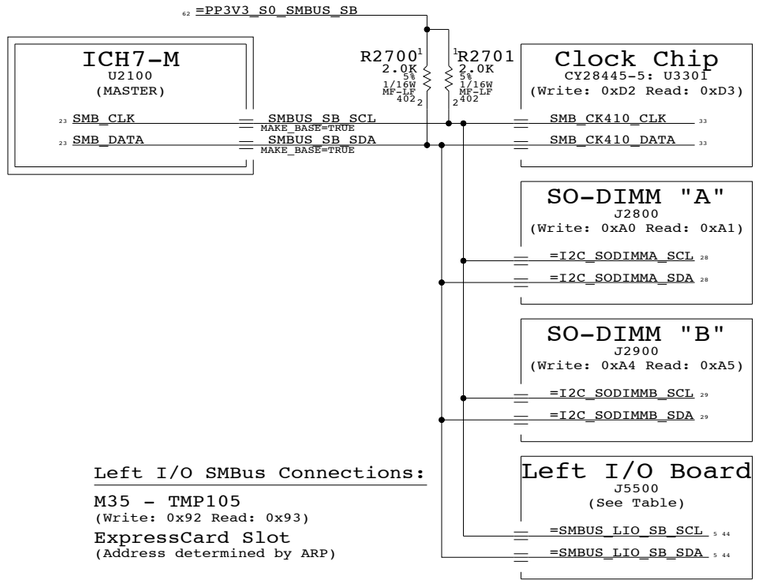
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

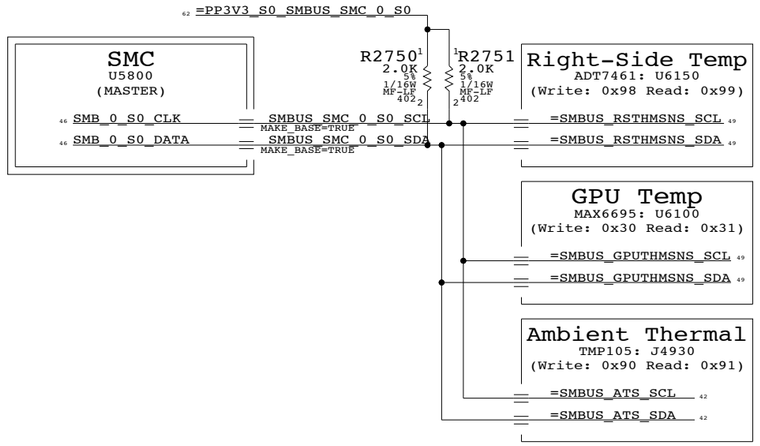
SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	26	103

ICH7-M SMBus Connections

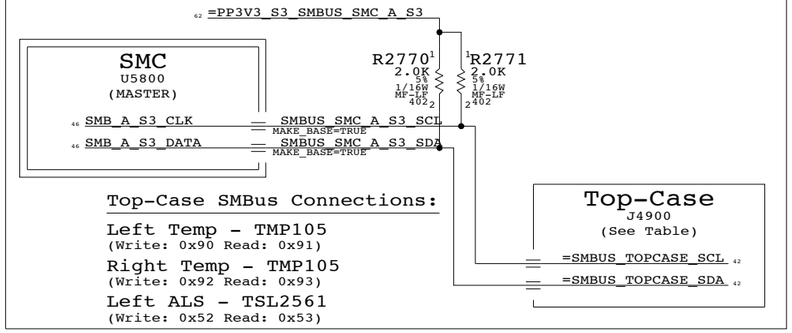


SMC "0" SMBus Connections

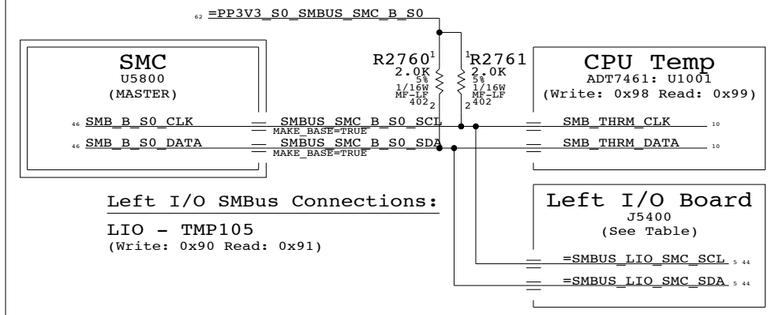


SMC "A" SMBus Connections

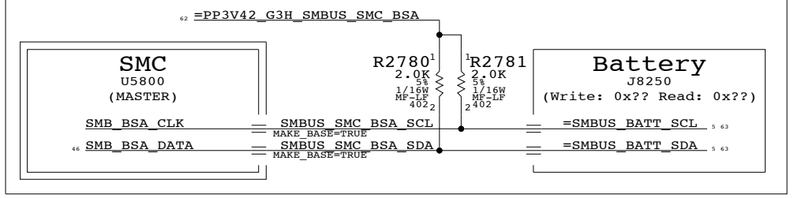
NOTE: SMC RMT bus remains powered and may be active in S3 state



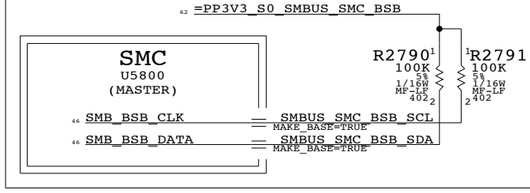
SMC "B" SMBus Connections



SMC "Battery A" SMBus Connections



SMC "Battery B" SMBus Connections



M1 SMBus Connections

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	27	103

Page Notes

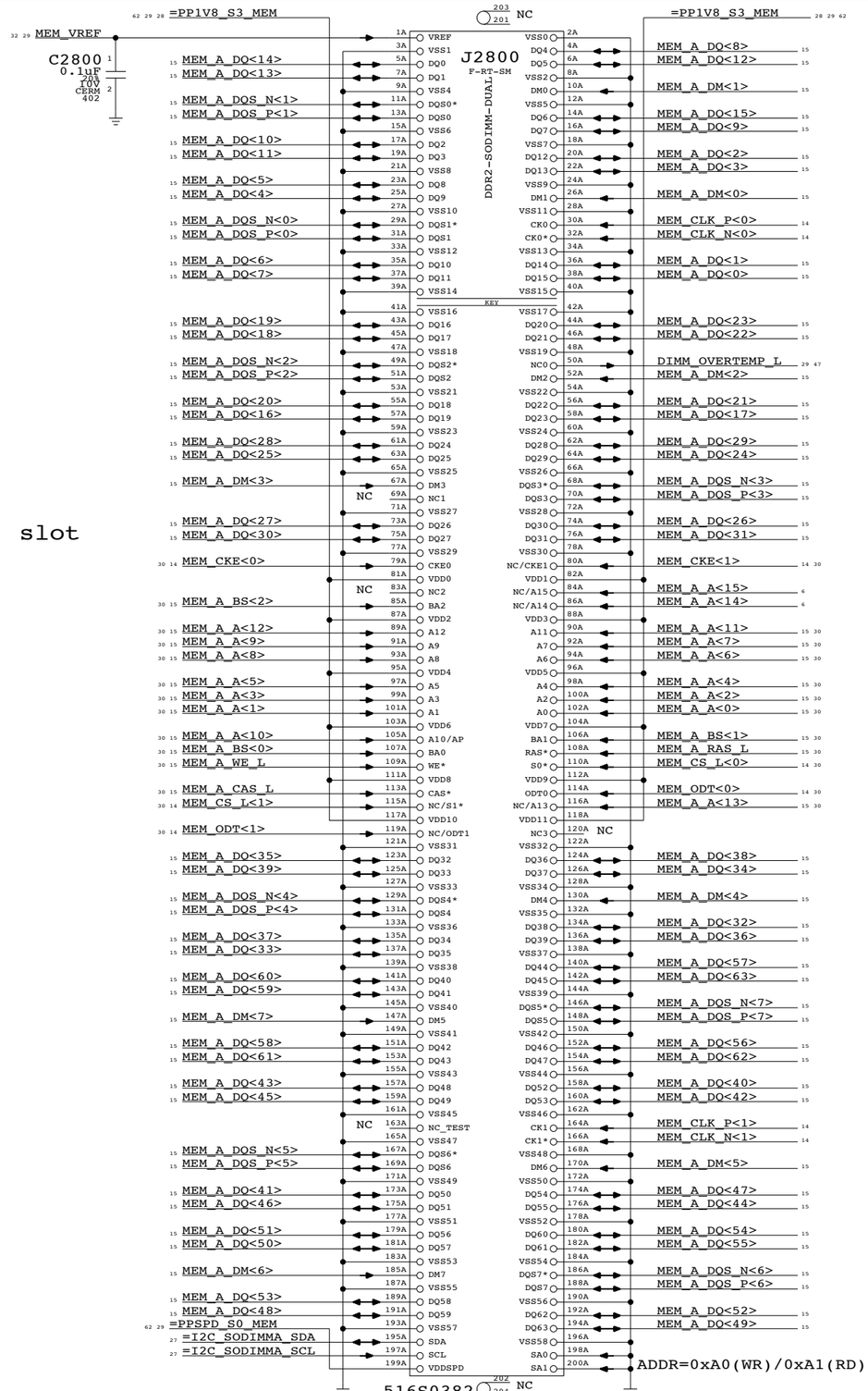
Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

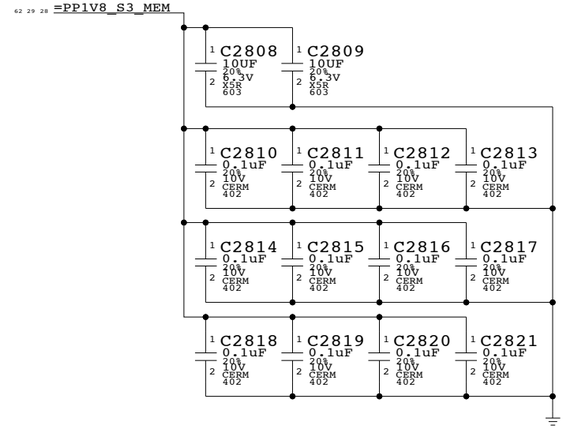
NOTE: This page does not supply VREF. The reference voltage must be provided by another page.

"Upper" (surface-mount) slot



DDR2 Bypass Caps

(For return current)



DDR2 SO-DIMM Connector A

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	28	103

Page Notes

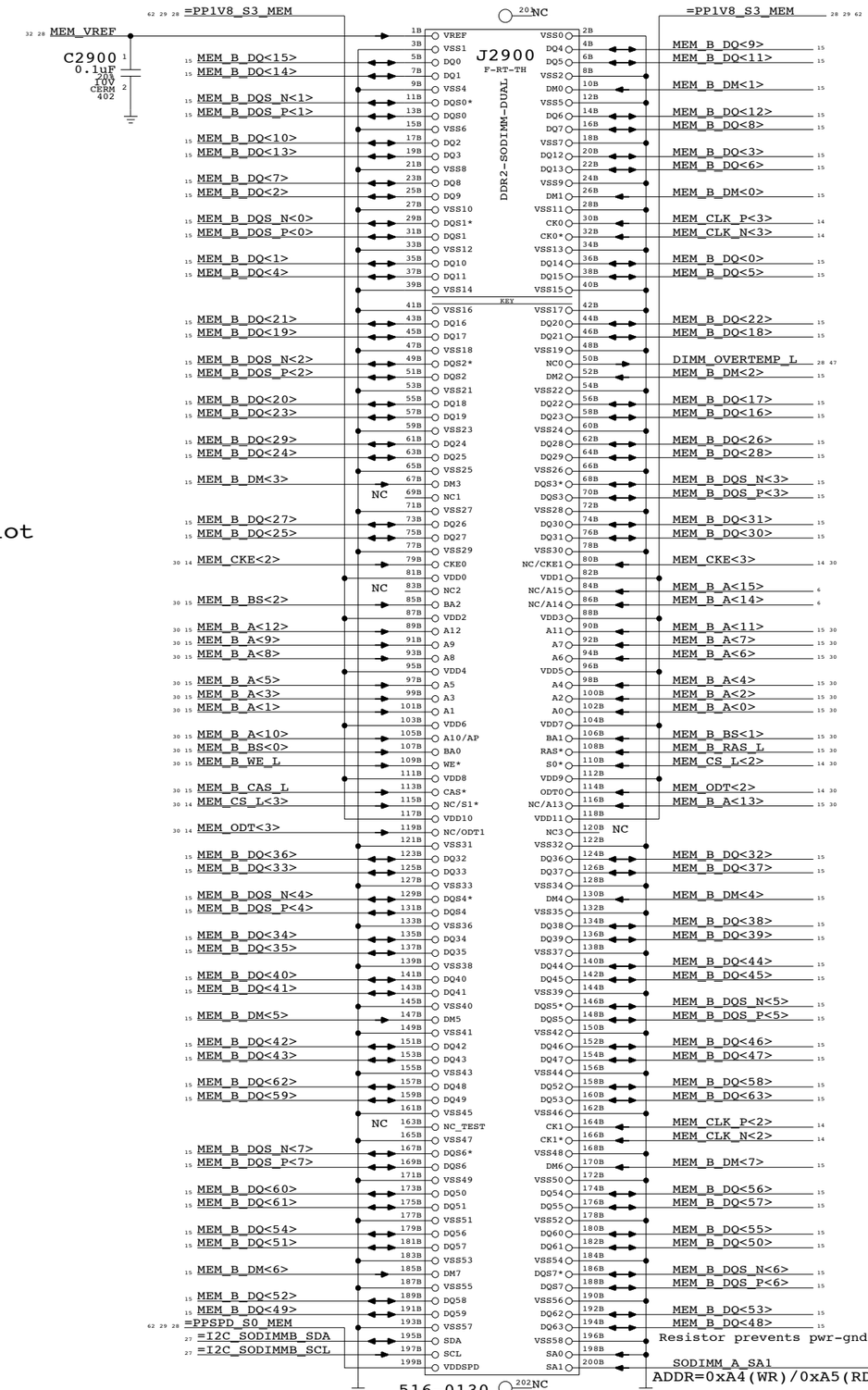
Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

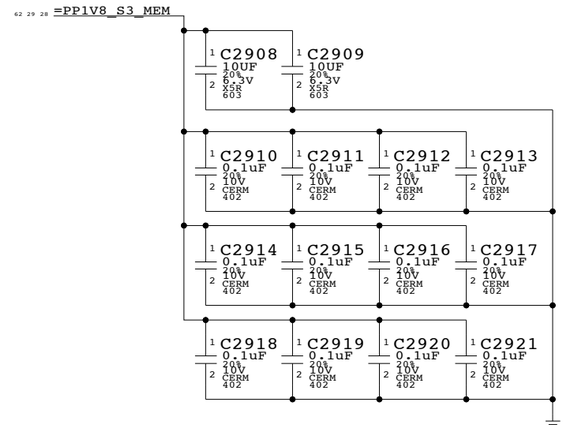
NOTE: This page does not supply VREF. The reference voltage must be provided by another page.

"Lower" (thru-hole) slot



DDR2 Bypass Caps

(For return current)



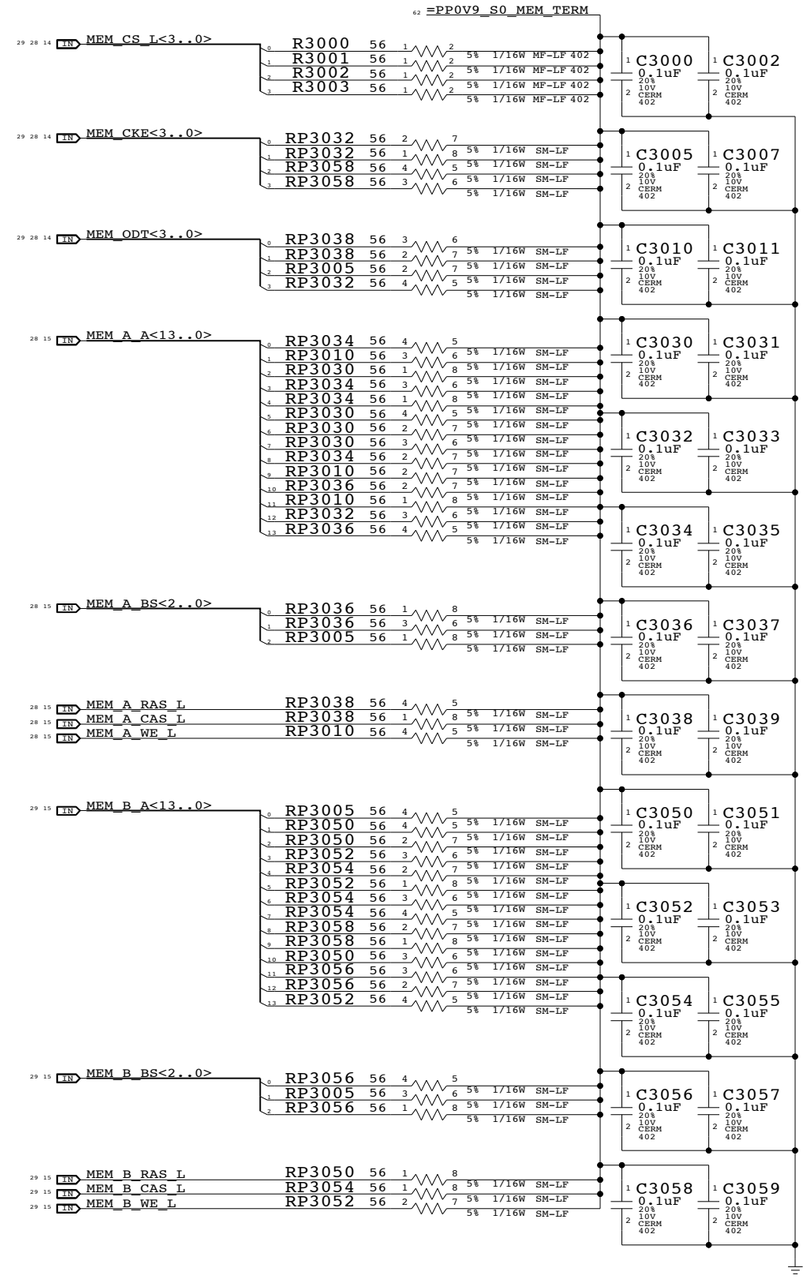
DDR2 SO-DIMM Connector B

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03
SCALE: NONE	SHT 29 OF 103	

One cap for each side of every RPAK, one cap for every two discrete resistors



Memory Active Termination

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	30	103

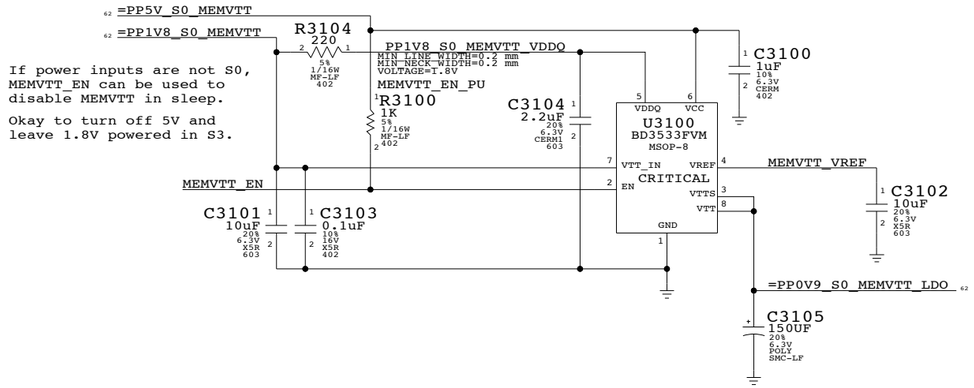
Page Notes

Power aliases required by this page:
- =PP5V_S0_MEMVTT
- =PP1V8_S0_MEMVTT
- =PP0V9_S0_MEMVTT_LDO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

DDR2 Vtt Regulator



If power inputs are not S0, MEMVTT_EN can be used to disable MEMVTT in sleep.

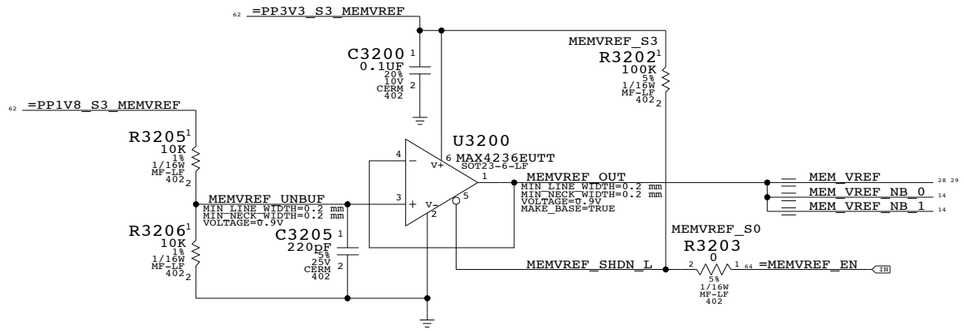
Okay to turn off 5V and leave 1.8V powered in S3.

Memory Vtt Supply

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03
SCALE: NONE	SHT 31 OF 103	



DDR2 VRef

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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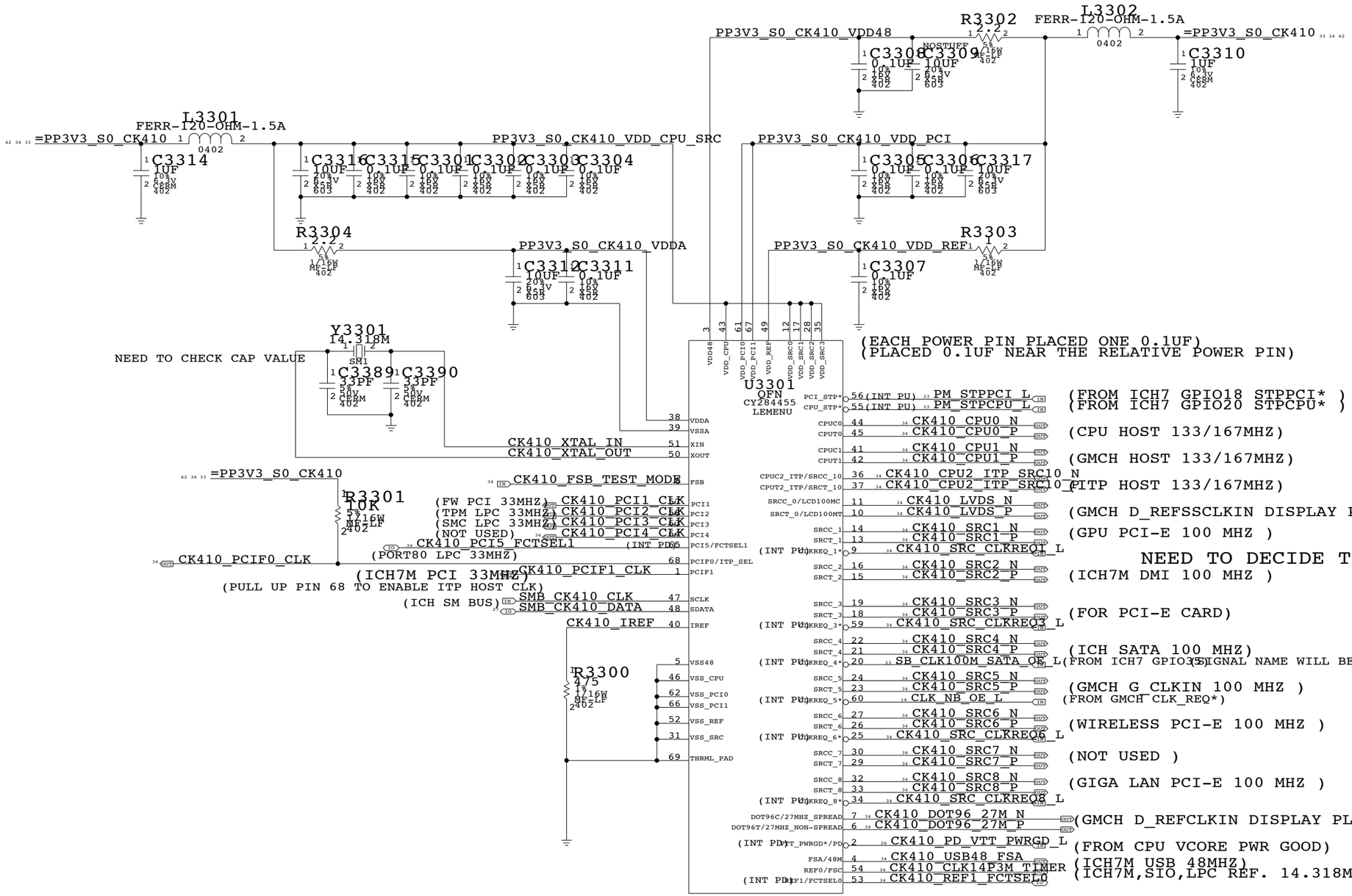
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	32	103



FCTSEL1	FCTSEL0	PIN 6	PIN 7	PIN 10	PIN 11	
0	0	DOT96T	DOT96C	100MT_SST	100MC_SST	* FOR INT. GRAPHIC SYSTEM
0	1	DOT96T	DOT96C	SRCT0	SRCC0	
1	0	27M_NON-SPREAD	27M_SPREAD	SRCT0	SRCC0	* FOR EXT. GRAPHIC SYSTEM
1	1	OFF LOW	TBD	SRCT0	SRCC0	

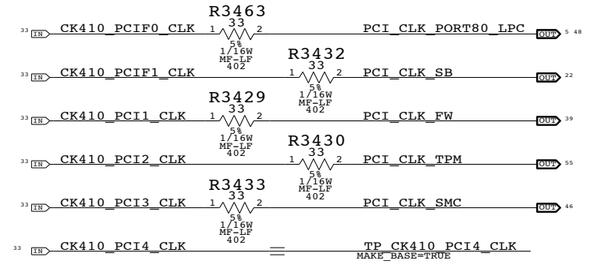
CLOCKS

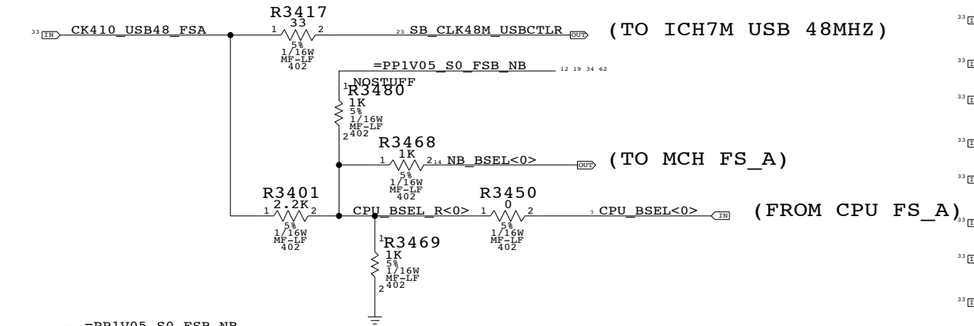
SYNC_MASTER=M62 SYNC_DATE=08/04/2005

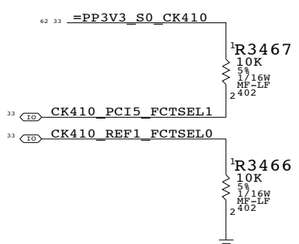
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	33	103



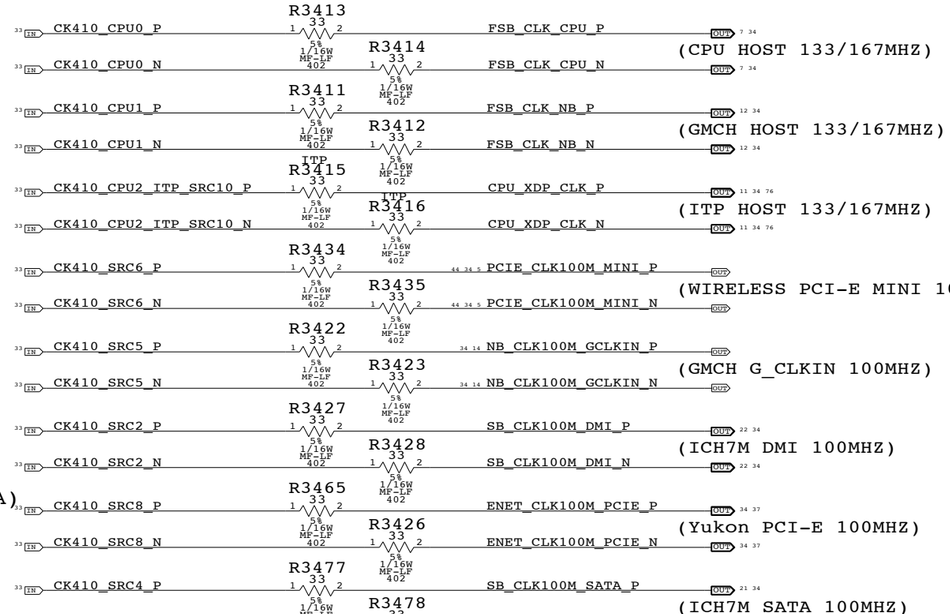


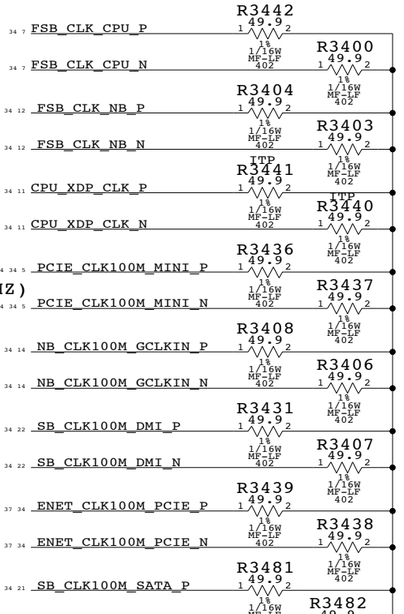


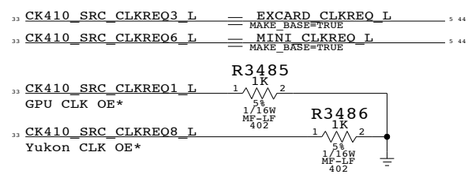
NOSTUFF R3450,R3451,R3453 FOR MANUAL CPU FREQUENCY

FS_C	FS_B	FS_A	CPU
0	0	0	266M
# 0	0	1	133M
# 0	1	0	166M
0	1	1	200M
1	0	0	100M
1	0	1	333M
1	1	0	400M
1	1	1	RESERVED

NAPA PLATFORM ONLY SUPPORT 133M/166M CPU SPEED







Clock Termination

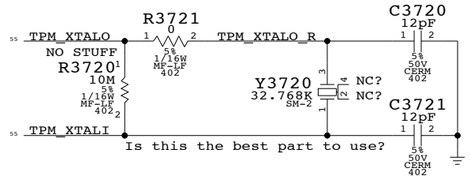
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

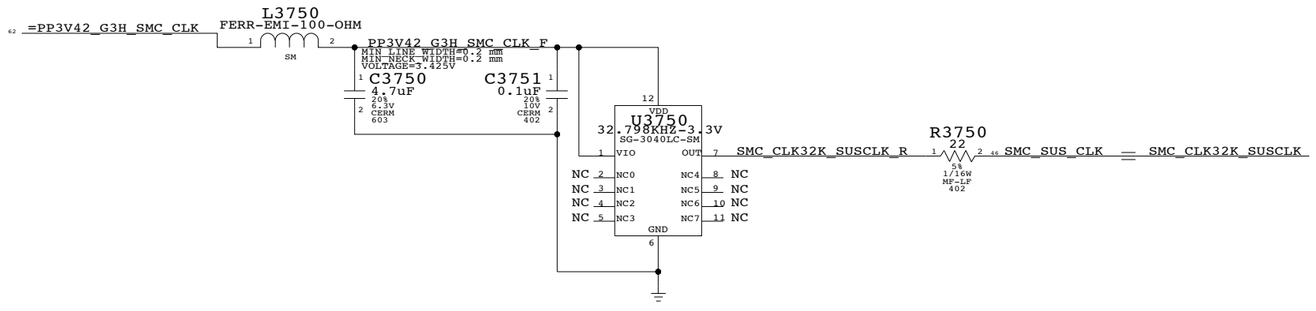
SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	34	103

TPM Crystal Circuit



SMC G3Hot Oscillator



Mobile Clocking

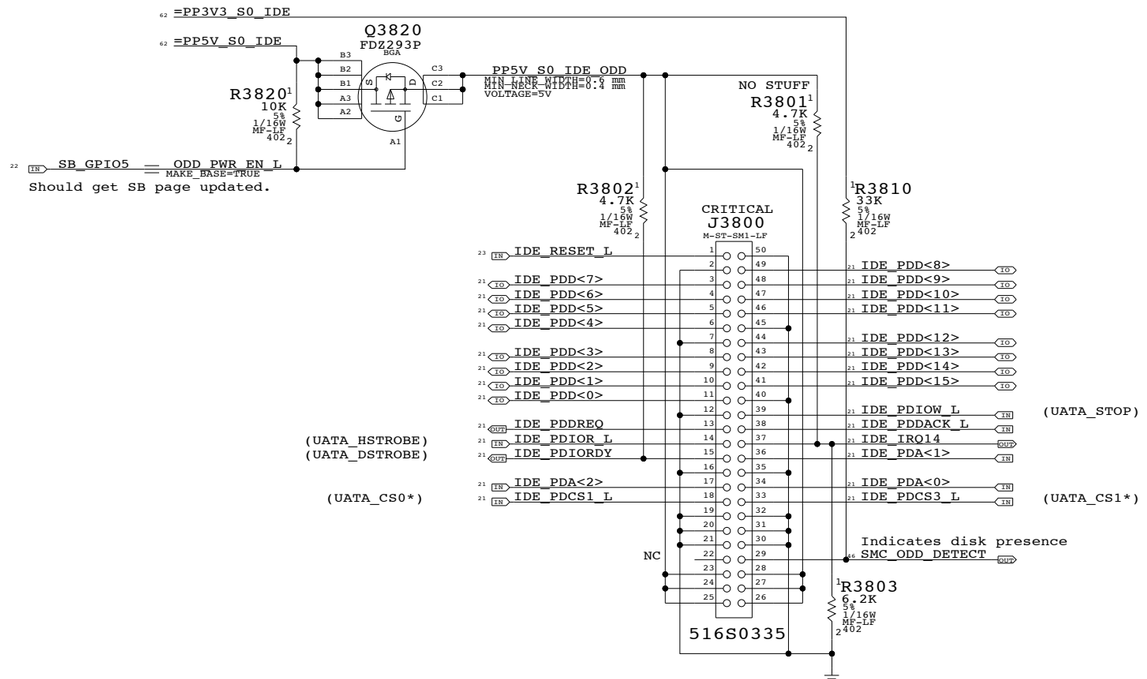
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

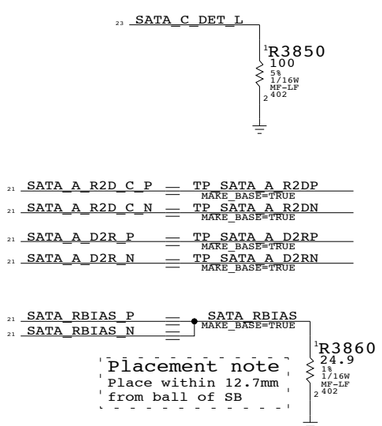
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	37	103

IDE (ODD) Connector





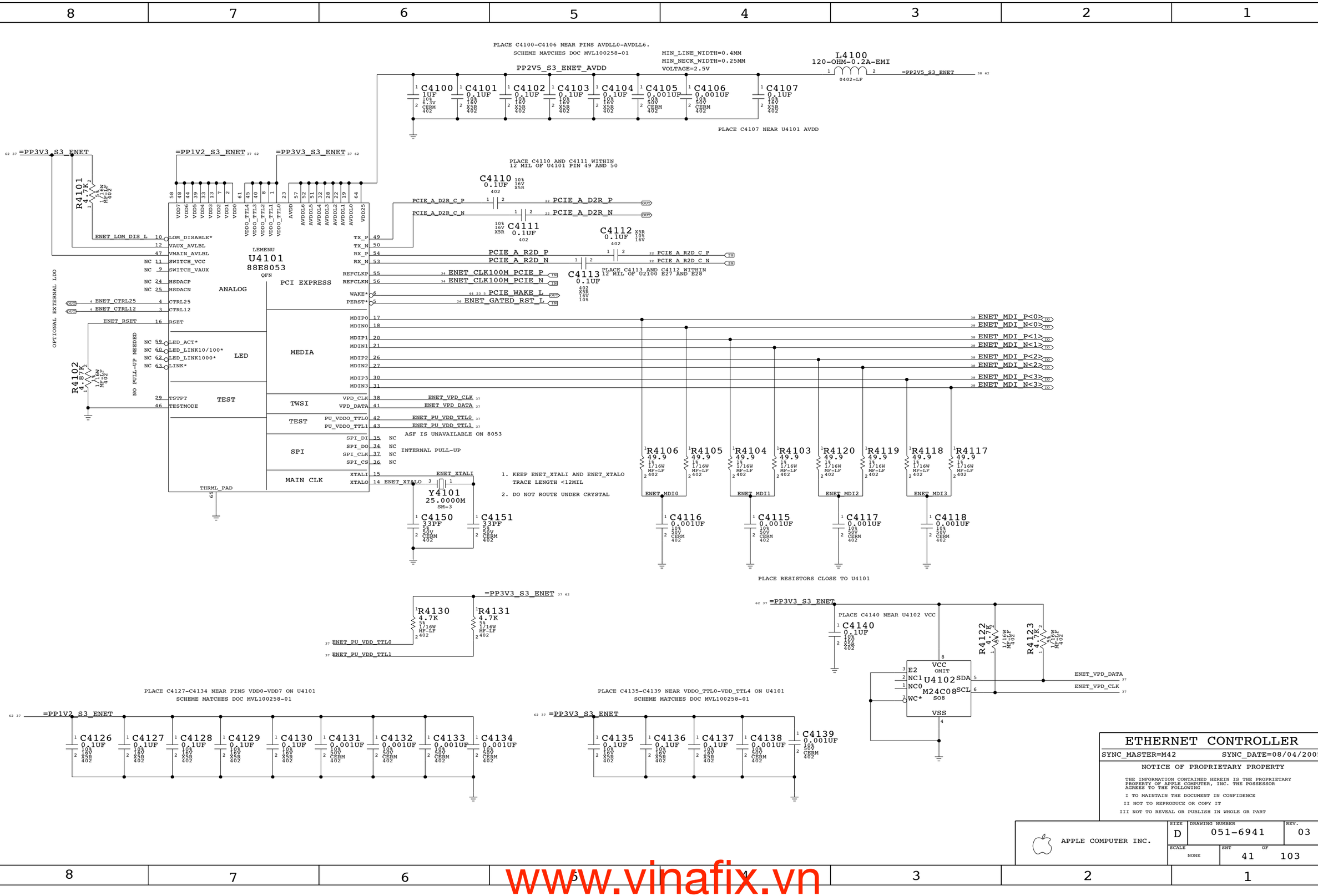
PATA Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	38	103



ETHERNET CONTROLLER

SYNC_MASTER=M42 SYNC_DATE=08/04/2005

NOTICE OF PROPRIETARY PROPERTY

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	41	103

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	
PROVIDED BY ETHERNET PHY	ENETCONN	ENET_100D	ENETCONN_P<0>
	ENETCONN	ENET_100D	ENETCONN_N<0>
	ENETCONN	ENET_100D	ENETCONN_P<1>
	ENETCONN	ENET_100D	ENETCONN_N<1>
	ENETCONN	ENET_100D	ENETCONN_P<2>
	ENETCONN	ENET_100D	ENETCONN_N<2>
	ENETCONN	ENET_100D	ENETCONN_P<3>
	ENETCONN	ENET_100D	ENETCONN_N<3>

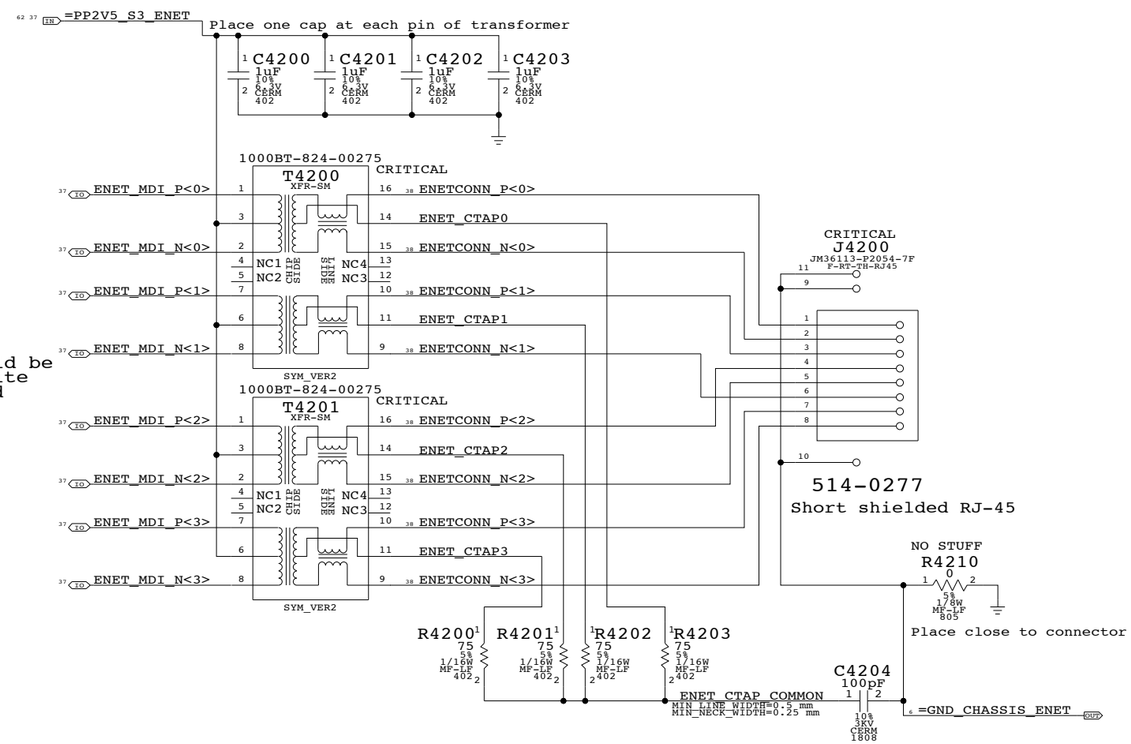
Page Notes

Power aliases required by this page:
- =PP2V5_ENET
- =GND_CHASSIS_ENET

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Transformers should be mirrored on opposite sides of the board



Ethernet Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03
SCALE: NONE	SHT 42 OF 103	

PAGE NOTES

INPUT
=PP3V3_S0_FW - 3.3V POWER FOR FIREWIRE (MOBILE: OFF DURING SLEEP)
=PP3V3_S0_PCI - 3.3V POWER FOR PCI FIREWIRE (MOBILE: OFF DURING SLEEP)
PCI_GNT3_L - PCI GRANT FROM SB
PCI_CLK_FW - NEED TO REFERENCE TO ALIAS PAGE
PCI_RST_L - PCI RESET FROM SB
FW_PC0 - FIREWIRE POWER CLASS IDENTIFIER

INPUT/OUTPUT
PCI_AD<0..31>,PCI_C_BE_L<0..3>,PCI_FRAME_L,PCI_IRDY_L,PCI_TRDY_L,
PCI_DEVSEL_L, PCI_STOP_L, PCI_PAR, PCI_PERR_L, PCI_SERR_L
FW_A_TPA_P/N, FW_A_TPB_P/N, FW_A_TPBIAS - PORT 0 FIREWIRE DIFF PAIRS
FW_B_TPA_P/N, FW_B_TPB_P/N, FW_B_TPBIAS - PORT 1 FIREWIRE DIFF PAIRS
FW_C_TPA_P/N, FW_C_TPB_P/N, FW_C_TPBIAS - PORT 2 FIREWIRE DIFF PAIRS

OUTPUT
PCI_REQ3_L - PCI REQUEST TO SB
PM_CLKRUN_L - CLOCK-RUN PCI PROTOCOL
INT_PIRQD_L - INTERRUPT TO SB
PCI_PME_FW_L - DEDICATED PME FOR FIREWIRE (SB GPIO1)

PAGE HISTORY

5/19/2005 - FIRST REVISION OF PAGE
6/20/2005 - BGA VERSION OF FW323-06 ADDED
6/21/2005 - CHANGED INT* TO INT_PIRQD_L (PER ARCHITECTURAL DEFINITION)
6/21/2005 - CHANGED PCI_ID TO AD19 (PER ARCHITECTURAL DEFINITION)
6/21/2005 - CHANGED REQ/GNT TO REQ3/GNT3 (PER ARCHITECTURAL DEFINITION)
6/22/2005 - ADDED 51UK PULL-DOWN ON RST* AND REMOVED CONNECTION TO PLT_RST_L
6/22/2005 - CHANGED CLK_PME_R1FE_PAIR NAMES TO BE RE-USE COMPLIANT
6/22/2005 - REMOVED CONSTRAINT SETS AS THEY WILL BE MANAGED ON BOARD SIDE
6/22/2005 - REMOVED C4421 - REDUNDANT
6/22/2005 - BRING OUT PCI CONNECTION TO BE CONNECTED ON PORT PAGE
7/26/2005 - CONNECTED PIN E10 TO GND

MOBILE TURNS OFF CONTROLLER POWER DURING SLEEP

=PP3V3_S0_FW

C4424 10UF 20% 6.3V X5R 603
C4418 0.1UF 20% 10V X5R 402
C4422 0.1UF 20% 10V CERM 402
C4426 0.1UF 20% 10V CERM 402
C4428 0.1UF 20% 10V CERM 402
C4430 0.1UF 20% 10V CERM 402
C4432 0.1UF 20% 10V CERM 402

L4400 600-OHM-300MA 0402

PP3V3_S0_FW_AVDD

C4416 10UF 20% 6.3V X5R 603
C4417 0.1UF 20% 10V X5R 402
C4429 0.1UF 20% 10V X5R 402
C4425 0.1UF 20% 10V X5R 402

=PP3V3_S0_PCI

CONNECT TO VDD FOR 3.3V OPERATION

R4431 22 5% 1/16W MF-LF 402

THIS IS FROM ICH-7M

U4400
FW32306
BGA
LEMENU

PCI_AD<0>	F10	PCI_AD0
PCI_AD<1>	G10	PCI_AD1
PCI_AD<2>	H10	PCI_AD2
PCI_AD<3>	H12	PCI_AD3
PCI_AD<4>	J13	PCI_AD4
PCI_AD<5>	J12	PCI_AD5
PCI_AD<6>	K13	PCI_AD6
PCI_AD<7>	K10	PCI_AD7
PCI_AD<8>	L12	PCI_AD8
PCI_AD<9>	M13	PCI_AD9
PCI_AD<10>	L11	PCI_AD10
PCI_AD<11>	M12	PCI_AD11
PCI_AD<12>	M11	PCI_AD12
PCI_AD<13>	N12	PCI_AD13
PCI_AD<14>	M10	PCI_AD14
PCI_AD<15>	N11	PCI_AD15
PCI_AD<16>	M4	PCI_AD16
PCI_AD<17>	N5	PCI_AD17
PCI_AD<18>	N4	PCI_AD18
PCI_AD<19>	M3	PCI_AD19
PCI_AD<20>	M2	PCI_AD20
PCI_AD<21>	N3	PCI_AD21
PCI_AD<22>	K4	PCI_AD22
PCI_AD<23>	M1	PCI_AD23
PCI_AD<24>	K2	PCI_AD24
PCI_AD<25>	J4	PCI_AD25
PCI_AD<26>	K1	PCI_AD26
PCI_AD<27>	J2	PCI_AD27
PCI_AD<28>	J1	PCI_AD28
PCI_AD<29>	H2	PCI_AD29
PCI_AD<30>	H4	PCI_AD30
PCI_AD<31>	H1	PCI_AD31
PCI_C_BE_L<0>	K12	PCI_CBE0*
PCI_C_BE_L<1>	M9	PCI_CBE1*
PCI_C_BE_L<2>	L3	PCI_CBE2*
PCI_C_BE_L<3>	L1	PCI_CBE3*
PCI_PAR	N10	PCI_PAR
PCI_FRAME_L	N6	PCI_FRAME*
PCI_IRDY_L	M6	PCI_IRDY*
PCI_TRDY_L	N7	PCI_TRDY*
PCI_DEVSEL_L	N8	PCI_DEVSEL*
PCI_STOP_L	M7	PCI_STOP*
FW_PCI_IDSEL	L2	PCI_IDSEL
PCI_REQ3_L	E2	PCI_REQ*
PCI_GNT3_L	E1	PCI_GNT*
PCI_PERR_L	M8	PCI_PERR*
PCI_SERR_L	N9	PCI_SERR*
PCI_CLK_FW	G2	PCI_CLK
PM_CLKRUN_L	D1	CLKRUN*
PCI_RST_L	F1	PCI_RST*
INT_PIRQD_L	D2	PCI_INTA*
PCI_PME_FW_L	F2	PCI_PME*

VDD0	G4	
VDD1	N1	
VDD2	N2	
VDD3	K5	
VDD4	K6	
VDD5	K7	
VDD6	L13	
VDD7	H13	
VDD9	A2	
VDDA0	D10	
VDDA1	A13	
VDDA2	B13	
VDDA3	A7	
VDDA4	A8	
VDDA5	D6	
PCI_VIOS	F10	

VSS0	A1	
VSS1	B2	
VSS2	C3	
VSS3	D4	
VSS4	E4	
VSS5	E5	
VSS6	F4	
VSS7	F6	
VSS8	F7	
VSS9	F8	
VSS10	G1	
VSS11	G6	
VSS12	G7	
VSS13	G8	
VSS14	H6	
VSS15	H7	
VSS16	H8	
VSS17	J5	
VSS18	J9	
VSS19	J10	
VSS20	K8	
VSS21	K9	
VSS22	N13	
VSSA0	E13	
VSSA1	E9	
VSSA2	D9	
VSSA3	D7	
VSSA4	D5	

197S0030 3.2MMX2.5MM

Y4403 SM-2 24.576MHZ

R4400 390 5% 1/16W MF-LF 402

C4411 22PF 5% 50V CERM 402
C4412 22PF 5% 50V CERM 402

NEED TO CHECK CRYSTAL LOAD CAPACITANCE

XI	A5	FW_XI
XO	B5	FW_XO
RESET*	B4	FW_PWRON_RST_L
R1	A6	FW_R1
R0	B7	FW_R0
TPBIAS0	B8	FW_A_TPBIAS
TPA0_P	A9	FW_A_TPA_P
TPA0_N	B9	FW_A_TPA_N
TPB0_P	B10	FW_A_TPB_P
TPB0_N	A10	FW_A_TPB_N
TPBIAS1	D8	FW_B_TPBIAS
TPA1_P	A11	FW_B_TPA_P
TPA1_N	B11	FW_B_TPA_N
TPB1_P	B12	FW_B_TPB_P
TPB1_N	A12	FW_B_TPB_N
TPBIAS2	C13	FW_C_TPBIAS
TPA2_P	C11	FW_C_TPA_P
TPA2_N	C12	FW_C_TPA_N
TPB2_P	D13	FW_C_TPB_P
TPB2_N	D12	FW_C_TPB_N

SPEC RECOMMENDS 2.49K

R4452 2.49K 1% 1/16W MF-LF 402

C4420 0.1UF 10% 10V X5R 402

R4420 510K 5% 1/16W MF-LF 402

MODE_420	M5	MODE FOR EXTERNAL LINK
MODE_A	B6	
PC0	E12	FW_PC0
PC1	F13	
PC2	F12	
CONTENDER	G12	LOW = NOT BUS MANAGER
CARDBUSN	B1	LOW = PCI OPERATION
MPCI_ACTN_323	E10	

DUAL PORT DEVICES ARE POWER CLASS 4 (‘100’)
SINGLE PORT DEVICES ARE POWER CLASS 0 (‘000’)

MANUFACTURING TEST PINS

TEST0	C2	
TEST1	C1	
PTEST	A4	
SE	A3	
SM	B3	

FIREWIRE CONTROLLER

SYNC_MASTER=MSZ SYNC_DATE=07/26/2005

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6941 | REV. 03

SCALE NONE | SHT 44 OF 103

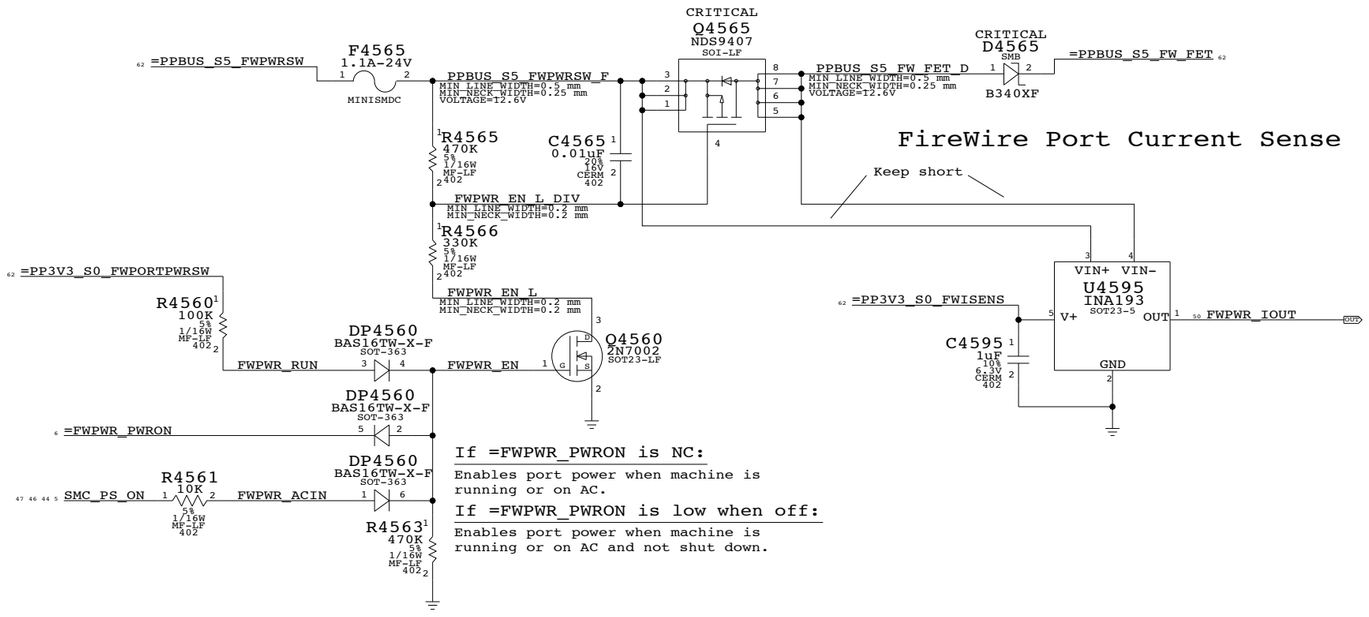
Page Notes

Power aliases required by this page:
- =PPBUS_S0_FWPWRSW (system supply for bus power)
- =PP3V3_S0_FWPORTPWRSW

Signal aliases required by this page:
- =FWPWR_PWRON (see related text note below)

BOM options provided by this page:
(NONE)

Port Power Switch



FireWire Port Power

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	45	103

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	
PROVIDED BY PHY PAGE	FW	FW_110D	FW_PORT1_TPA_FL_P 41
	FW	FW_110D	FW_PORT1_TPA_FL_N 41
	FW	FW_110D	FW_PORT1_TPB_FL_P 41
	FW	FW_110D	FW_PORT1_TPB_FL_N 41

Page Notes

Power aliases required by this page:
- =PPFW_PORT1
- =PP3V3_FW
- =GND_CHASSIS_FW_PORT1

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

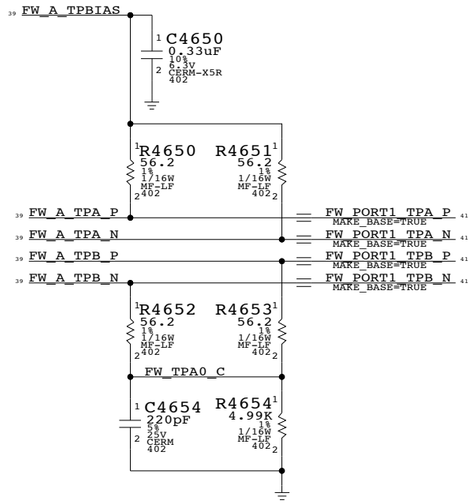
BOM options provided by this page:
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

Termination

Place close to FireWire PHY



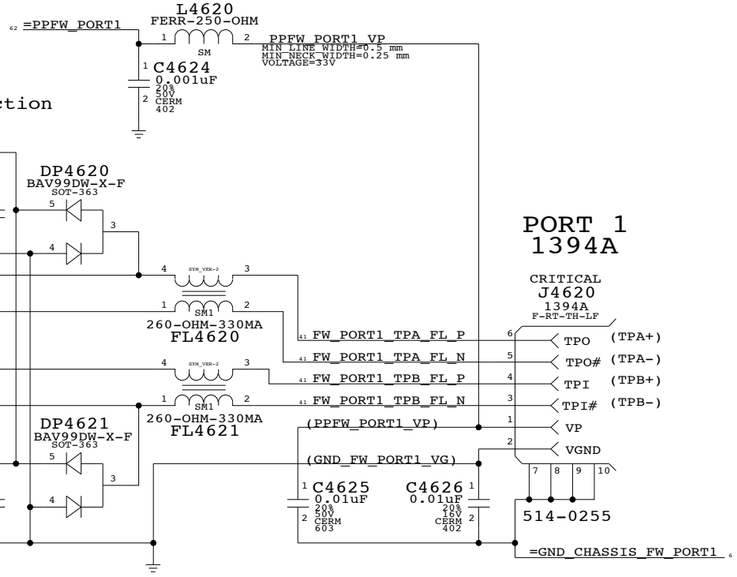
2nd TPA/TPB pair unused

39 FW_B_TPBIAS = NC_FW_B_TPBIAS (MAKE_BASE=TRUE, NO_TEST=YES)
39 FW_B_TPA_P = NC_FW_B_TPAP (MAKE_BASE=TRUE, NO_TEST=YES)
39 FW_B_TPA_N = NC_FW_B_TPAN (MAKE_BASE=TRUE, NO_TEST=YES)
39 FW_B_TPB_P = NC_FW_B_TPBP (MAKE_BASE=TRUE, NO_TEST=YES)
39 FW_B_TPB_N = NC_FW_B_TPBN (MAKE_BASE=TRUE, NO_TEST=YES)

3rd TPA/TPB pair unused

39 FW_C_TPBIAS = NC_FW_C_TPBIAS (MAKE_BASE=TRUE, NO_TEST=YES)
39 FW_C_TPA_P = NC_FW_C_TPAP (MAKE_BASE=TRUE, NO_TEST=YES)
39 FW_C_TPA_N = NC_FW_C_TPAN (MAKE_BASE=TRUE, NO_TEST=YES)
39 FW_C_TPB_P = NC_FW_C_TPBP (MAKE_BASE=TRUE, NO_TEST=YES)
39 FW_C_TPB_N = NC_FW_C_TPBN (MAKE_BASE=TRUE, NO_TEST=YES)

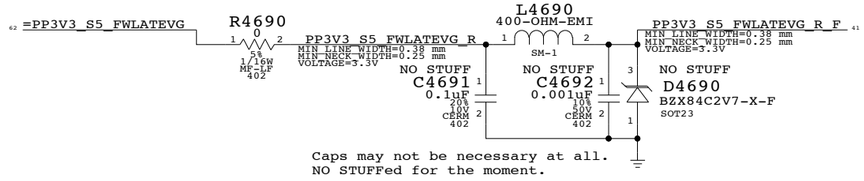
Cable Power



"Snapback" & "Late VG" Protection

R4699 0 5% 1/16W MF-LF 402 =GND_CHASSIS_FW_EMI 6

Late-VG Protection Power



Caps may not be necessary at all.
NO STUFFed for the moment.

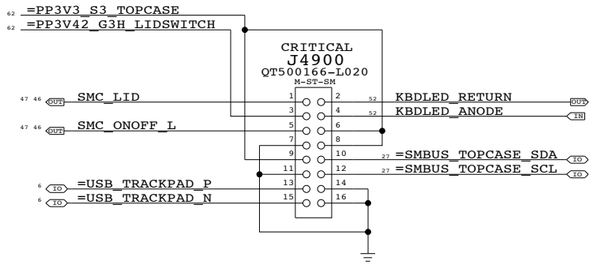
FireWire Ports

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

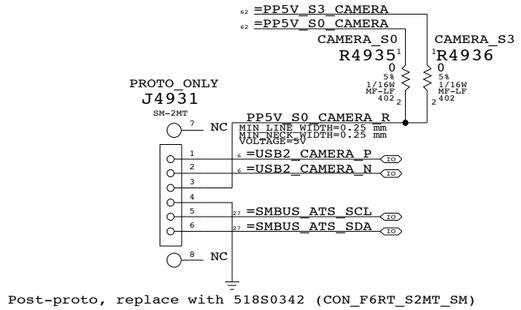
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6941	03
	SCALE NONE	SHT 46 OF 103	

Top-Case Connector

(Pinout is almost fixed)

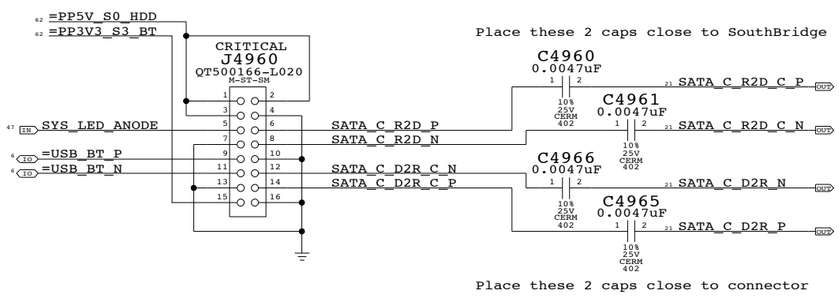


Camera Connector



Post-proto, replace with 518S0342 (CON_F6RT_S2MT_SM)

Bluetooth (M13P) & SATA HDD Flex Connector



Internal USB Connections

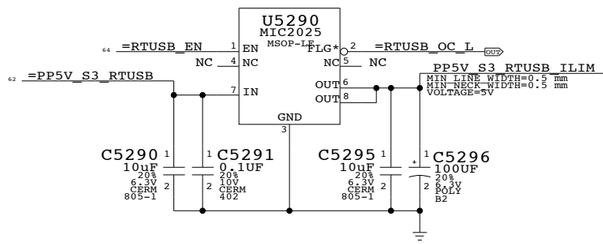
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

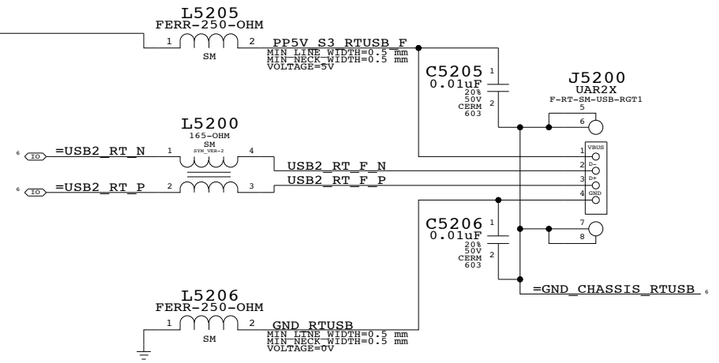
SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	49	103

Port Power Switch



Right USB Port



Place L5200, L5205 and L5206 across moat

External USB Connector

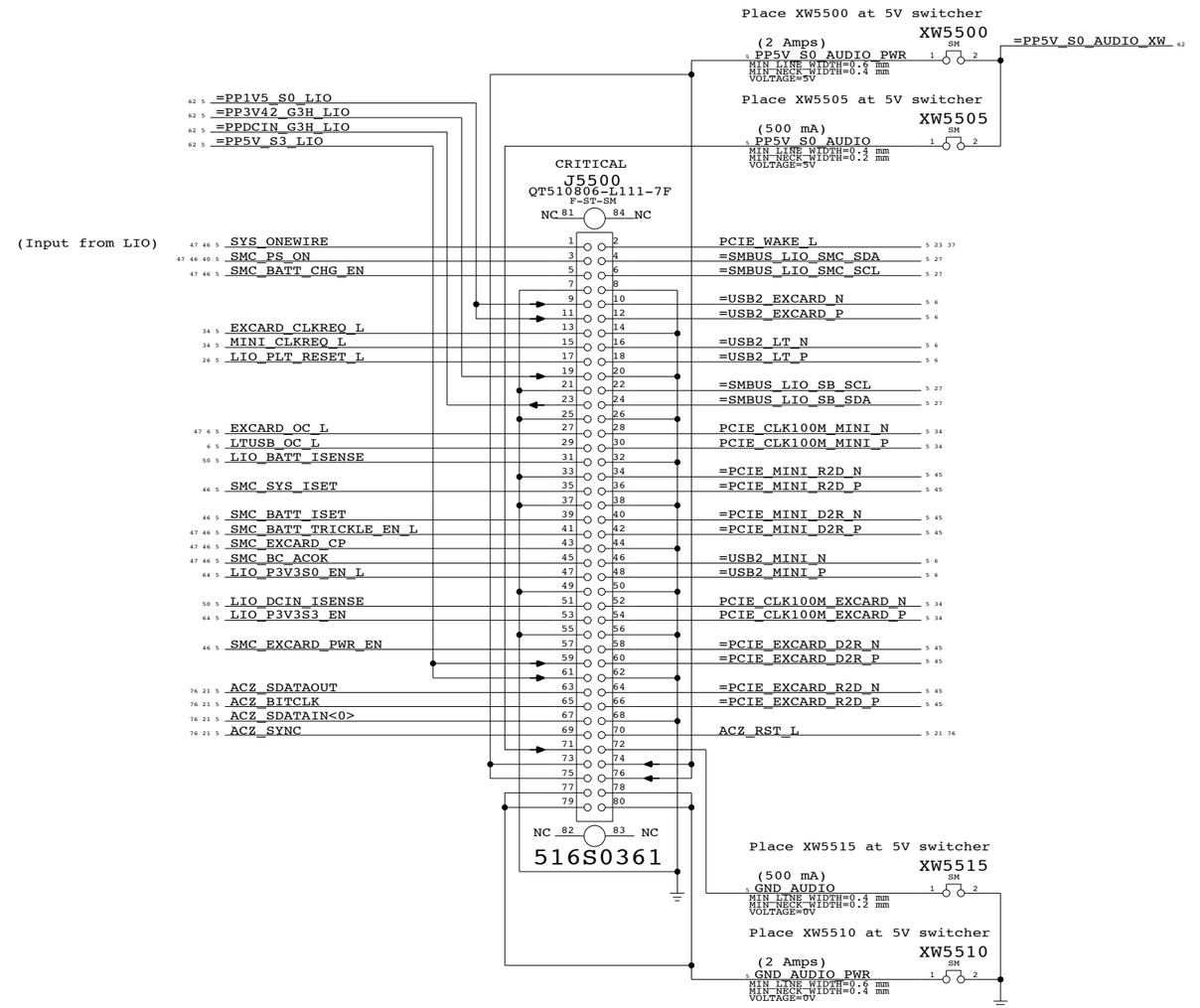
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	52	103

Left I/O Board Connector



Left I/O Board Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

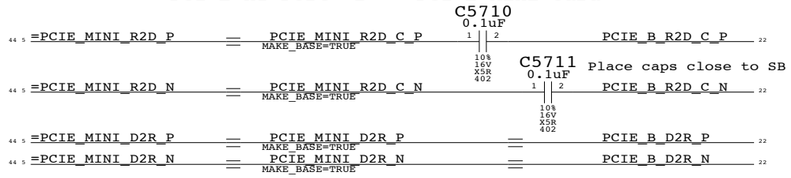
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

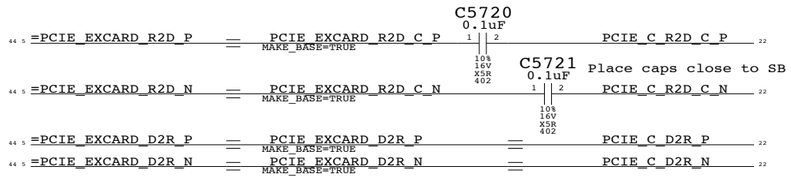
SCALE	SHT	OF
NONE	55	103

PCI-E x1 Port "A" = Ethernet (Yukon)

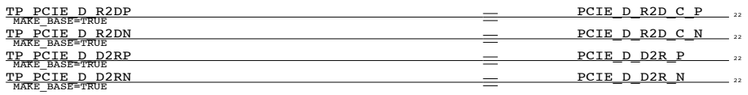
PCI-E x1 Port "B" = PCI-E Mini Card



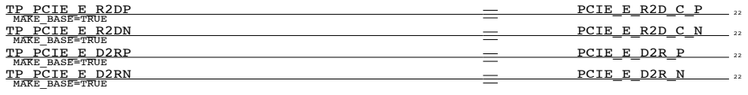
PCI-E x1 Port "C" = ExpressCard



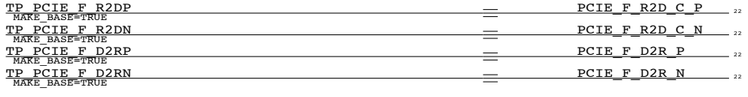
PCI-E x1 Port "D" = Unused



PCI-E x1 Port "E" = Unused



PCI-E x1 Port "F" = Unused



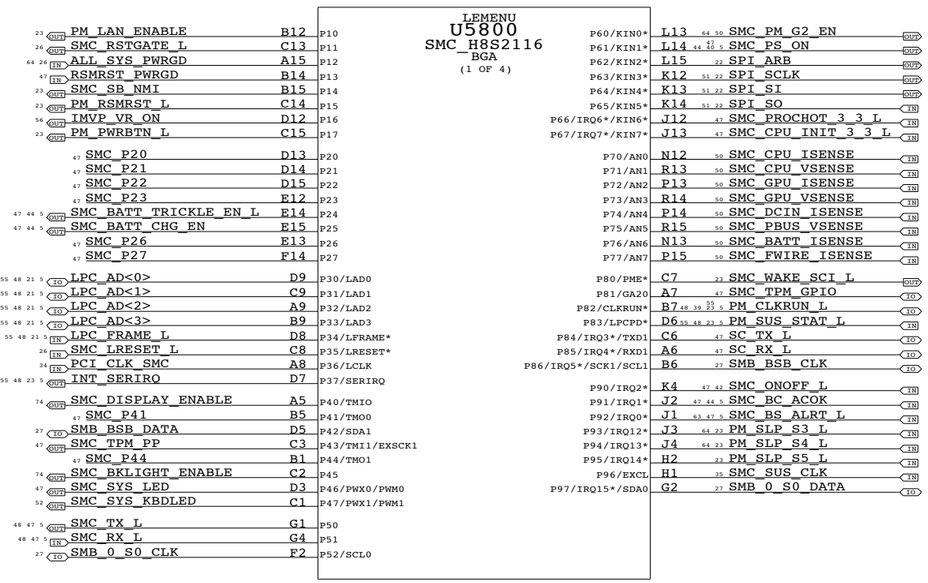
PCI-E Connections

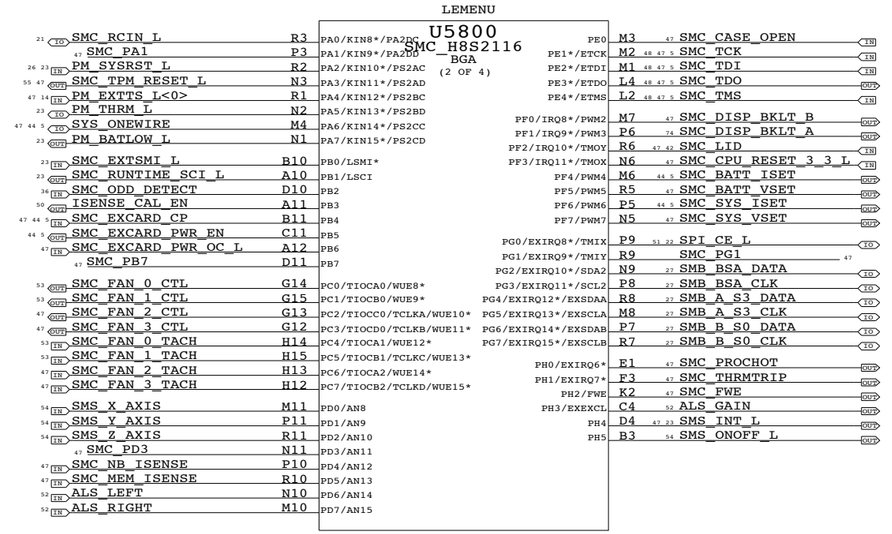
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

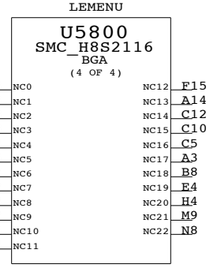
APPLE COMPUTER INC.

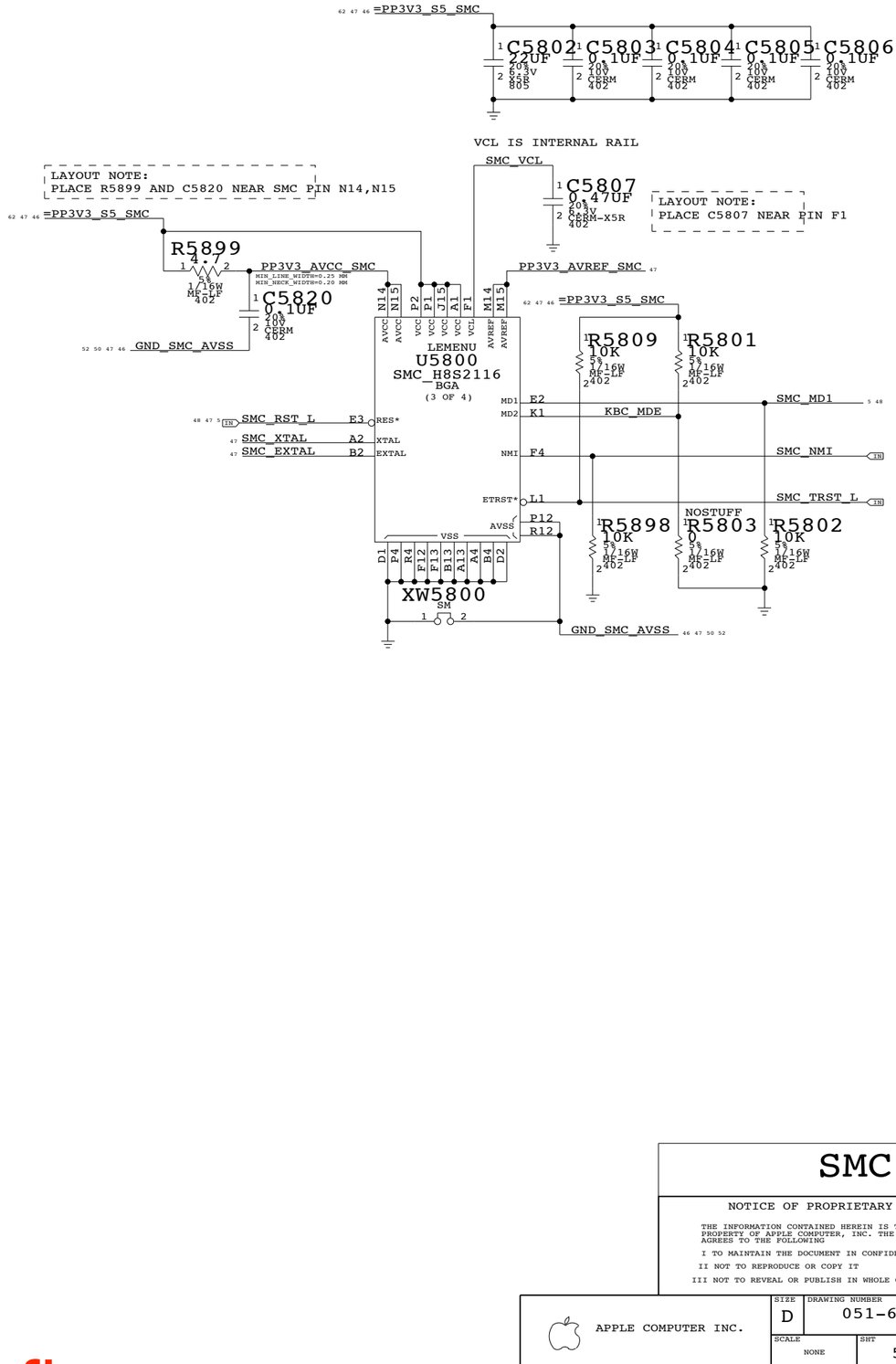
SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	57	103









SMC

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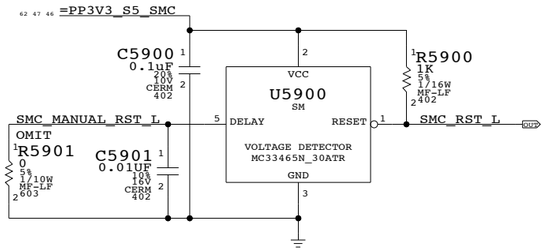
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

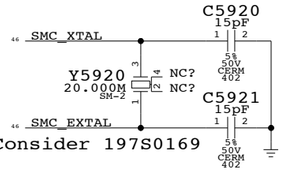
SCALE	SHT	OF
NONE	58	103

SMC Reset Button / Brownout Detect



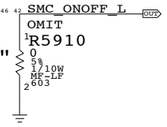
Silk: "SMC RST"

SMC Crystal Circuit



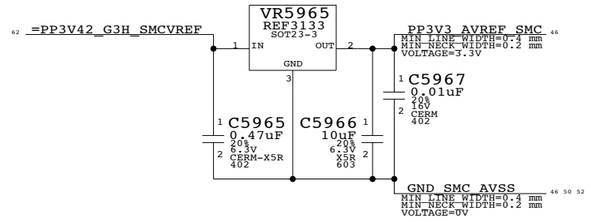
Post-Proto: Consider 197S0169

Debug Power Button

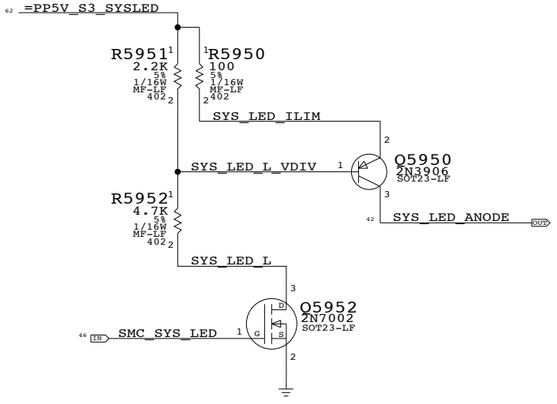


Silk: "PWR BTN"

SMC AVREF Supply

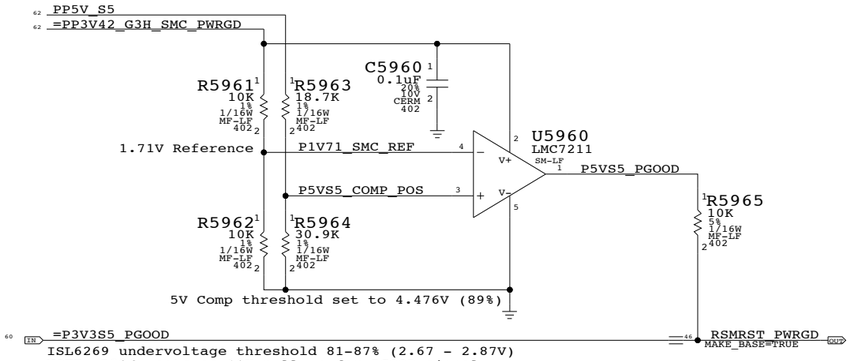


System (Sleep) LED Circuit



SMC PWRGD Circuit

Reports when 5V S5 and 3.3V S5 are in regulation



ISL6269 undervoltage threshold 81-87% (2.67 - 2.87V)
NOTE: R5965 acts as 10K pull-up for PGOOD signal

SMC_CPU_INIT_3_3_L — FWH_INIT_L

SMC_NB_ISENSE — SMC_P1V05S0_ISENSE

SMC_MEM_ISENSE — SMC_P1V8S3_ISENSE

SMC_PA1 — BOOT_LPC_SPI_L

PM_EXTTS_L<0> — DIMM_OVERTEMP_L

MAKE_BASE=TRUE

SMC_BATT_VSET — TP_SMC_BATT_VSET

SMC_SYS_VSET — TP_SMC_SYS_VSET

SMC_DISP_BKLT_B — TP_SMC_DISP_BKLT_B

SMC_FAN_2_CTL — TP_SMC_FAN_2_CTL

SMC_FAN_2_TACH — TP_SMC_FAN_2_TACH

SMC_FAN_3_CTL — TP_SMC_FAN_3_CTL

SMC_FAN_3_TACH — TP_SMC_FAN_3_TACH

SMC_P20 — TP_SMC_P20

SMC_P21 — TP_SMC_P21

SMC_P22 — TP_SMC_P22

SMC_P23 — TP_SMC_P23

SMC_P26 — TP_SMC_P26

SMC_P27 — TP_SMC_P27

SMC_P41 — TP_SMC_P41

SMC_P44 — TP_SMC_P44

SMC_PB7 — TP_SMC_PB7

SMC_PD3 — TP_SMC_PD3

SMC_PG1 — TP_SMC_PG1

MAKE_BASE=TRUE

SMC_TPM_GPIO — R5990 0 — TPM_GPIO1

SMC_TPM_GPIO1

SMC_TPM_GPIO2 — R5991 0 — TPM_GPIO2

SMC_TPM_PP — R5995 0 — TPM_PP

SC_RX_L — R5992 0 — SMC_RX_L

DEVELOPMENT

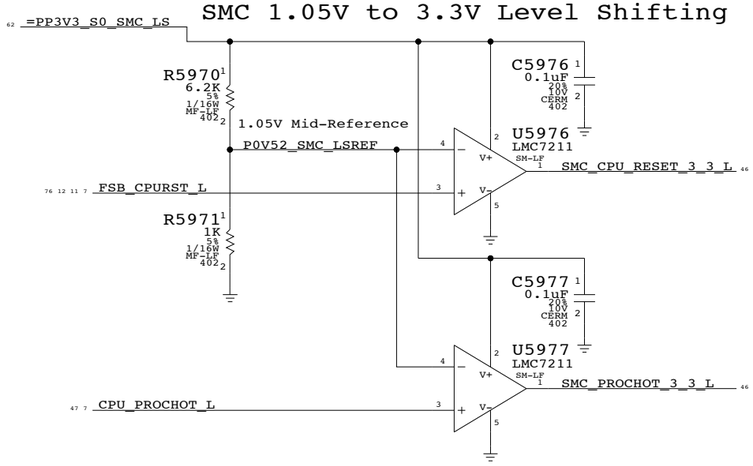
SC_TX_L — R5993 0 — SMC_TX_L

DEVELOPMENT

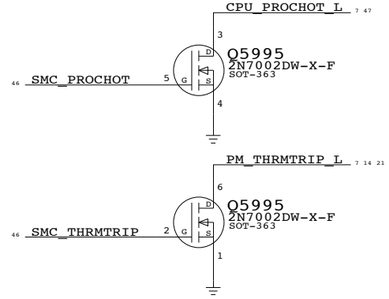
SMC_EXCARD_PWR_OC_L — R5994 0 — EXCARD_OC_L

5% 1/16W MF-LF 402

SMC 1.05V to 3.3V Level Shifting



SMC 3.3V to 1.05V Level Shifting



=PP3V3_S5_SMC
=PP3V3_S3_TPM
=PP3V3_S3_SMS

SMS_INT_L	R5829	10K	5%	1/16W MF-LF 402
SMC_TPM_RESET_L	R5827	10K	5%	1/16W MF-LF 402
SMC_ONOFF_L	R5808	10K	5%	1/16W MF-LF 402
SMC_LID	R5814	100K	5%	1/16W MF-LF 402
SMC_FWE	R5815	10K	5%	1/16W MF-LF 402
SMC_TX_L	R5817	10K	5%	1/16W MF-LF 402
SMC_RX_L	R5818	100K	5%	1/16W MF-LF 402
SYS_ONEWIRE	R5819	2.0K	5%	1/16W MF-LF 402
SMC_BS_ALRT_L	R5821	100K	5%	1/16W MF-LF 402
SMC_TMS	R5822	10K	5%	1/16W MF-LF 402
SMC_TDO	R5823	10K	5%	1/16W MF-LF 402
SMC_TDI	R5824	10K	5%	1/16W MF-LF 402
SMC_TCK	R5825	10K	5%	1/16W MF-LF 402
SMC_BATT_TRICKLE_EN_L	R5810	10K	5%	1/16W MF-LF 402
SMC_BATT_CHG_EN	R5811	10K	5%	1/16W MF-LF 402
SMC_PS_ON	R5812	10K	5%	1/16W MF-LF 402
SMC_CASE_OPEN	R5813	10K	5%	1/16W MF-LF 402
SMC_BC_ACOK	R5826	470K	5%	1/16W MF-LF 402
SMC_EXCARD_CP	R5828	10K	5%	1/16W MF-LF 402

SMC Support

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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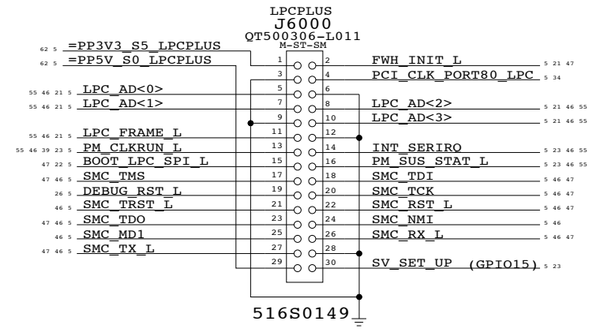
	D	051-6941	03
	SCALE: NONE	SHT 59 OF 103	



LPC+ Debug Connector

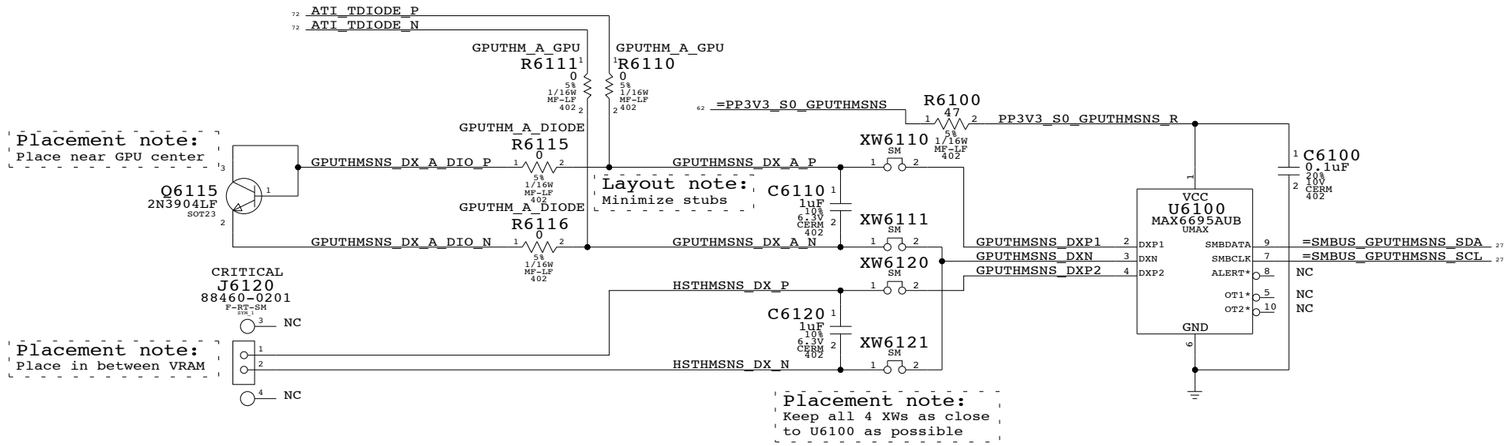
SYNC_MASTER=M42 SYNC_DATE=07/20/2005

APPLE COMPUTER INC.

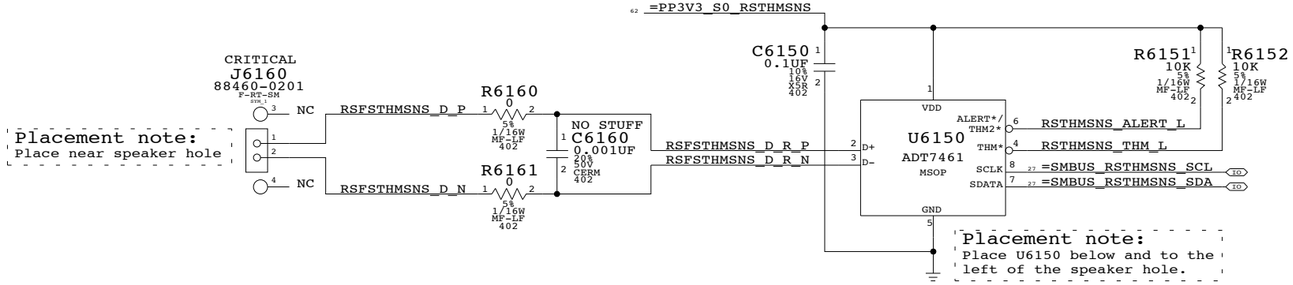
SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	60	103

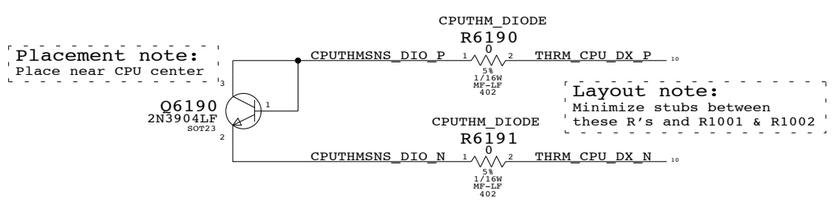
GPU / Heat Pipe Thermal Sensor



Right-Side/Fin Stack Thermal Sensor



CPU Back-Up Thermal Diode



R1001 / R1002 are not currently BOMOPTIONed. Can not programatically unstuff those parts to stuff these.

Thermal Sensors

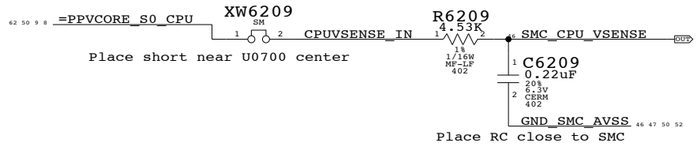
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

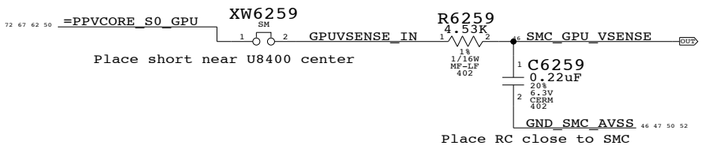
SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	61	103

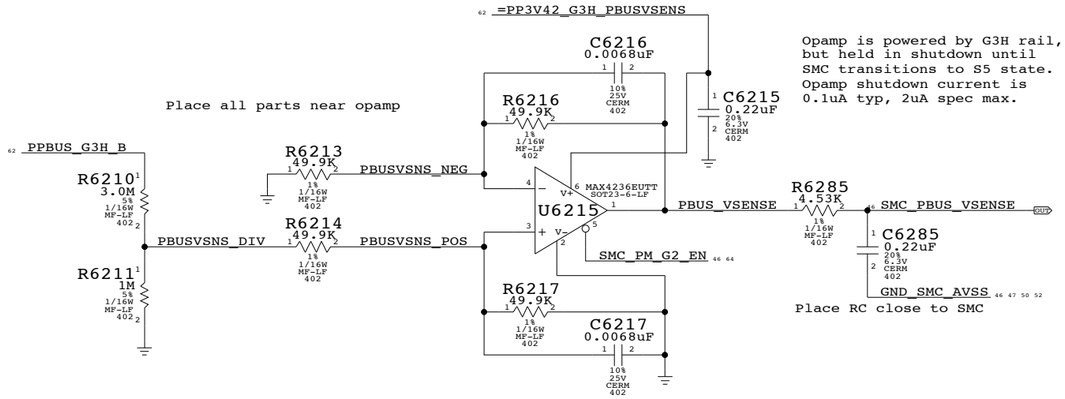
CPU Voltage Sense / Filter



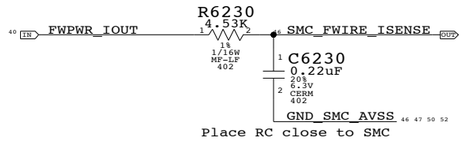
GPU Voltage Sense / Filter



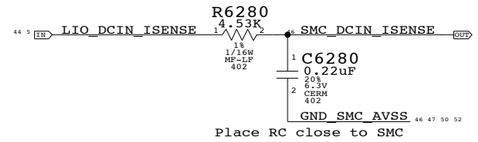
PBUS Voltage Sense Buffer & Filter



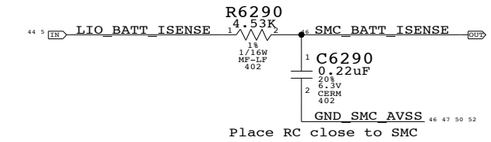
FireWire Current Sense Filter



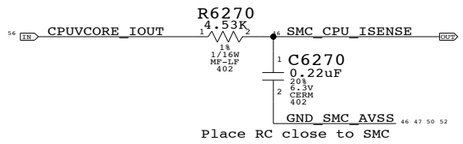
DCIN Current Sense Filter



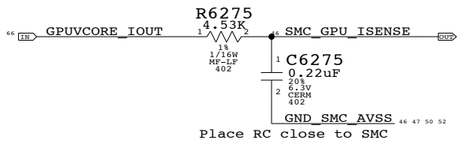
Battery Current Sense Filter



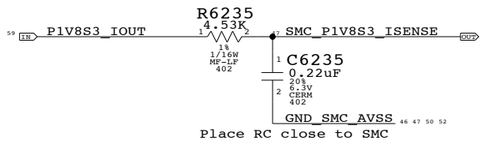
CPU Current Sense Filter



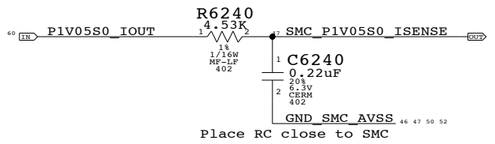
GPU Current Sense Filter



1.8V S3 (Memory) Current Sense Filter

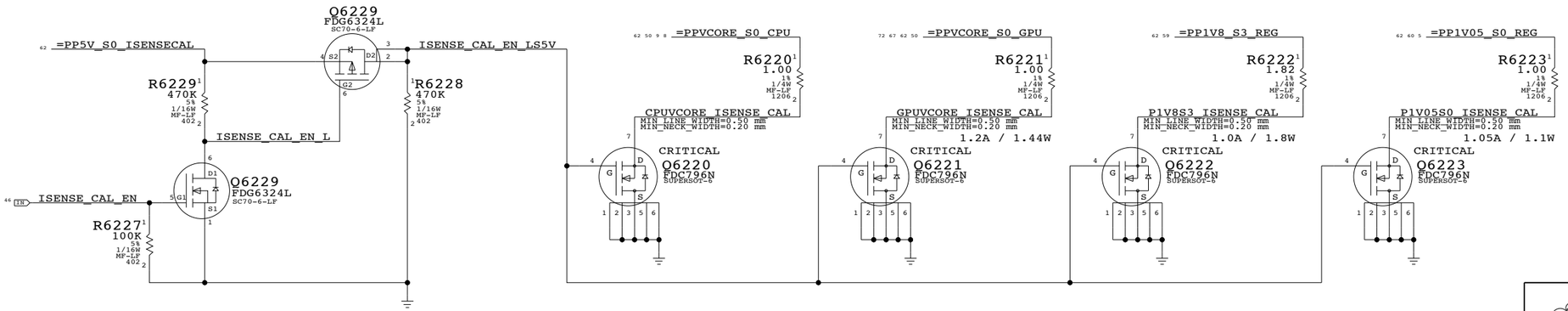


1.05V S0 (NB) Current Sense Filter



Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits



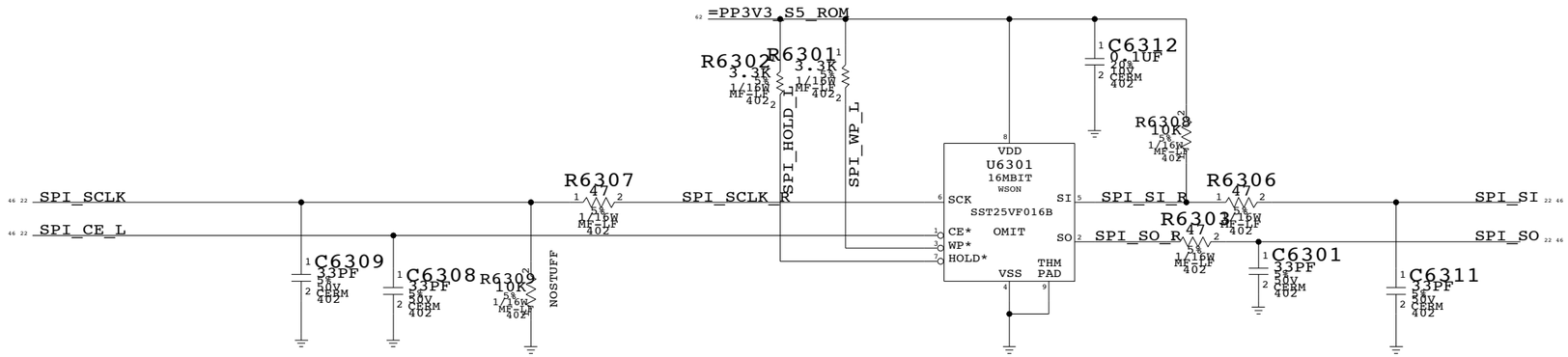
Current & Voltage Sensing

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03
SCALE: NONE	SHT 62 OF 103	

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S0384	1	IC,16MBIT -PIN SPI SERIAL FLASH,SOIC8	U6301		LEMENU



R6309 IS NOT NEEDED WHEN SHARING SPI FLASH WITH ICH7M AND TEKOA(LAN CHIP)

R6307 AND R6306 SHOULD BE PLACED LESS THAN 100 MILS FORM ICH7M

R6303 SHOULD BE PLACED LESS THAN 100 MILS FORM FLASH ROM

SPI BOOTROM

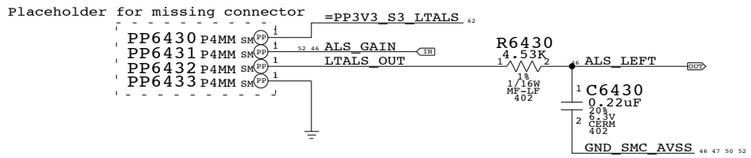
SYNC_MASTER=M87 SYNC_DATE=07/26/2005

APPLE COMPUTER INC.

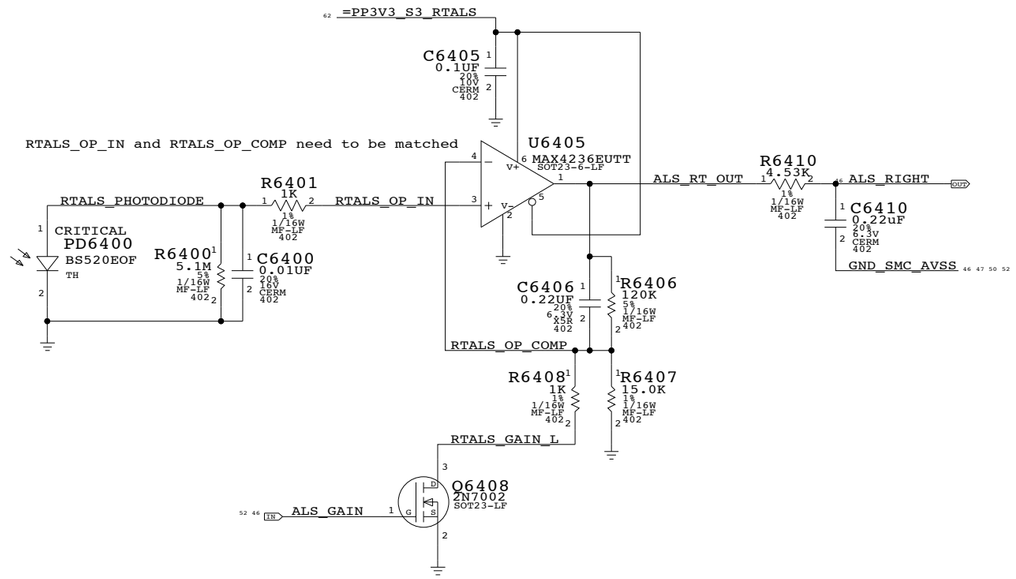
SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	63	103

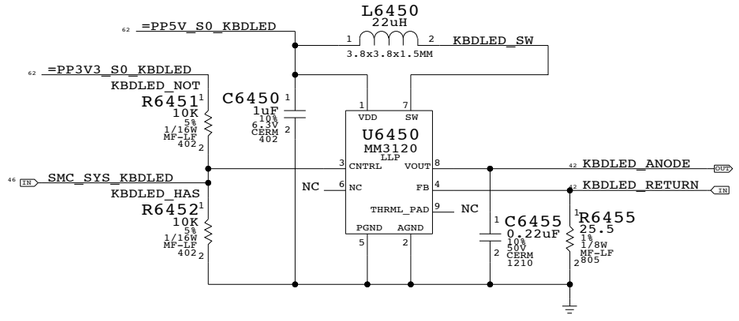
Left ALS "Connector"



Right ALS Circuit



Keyboard LED Driver



ALS Support

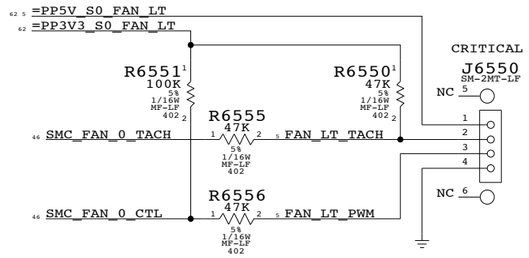
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

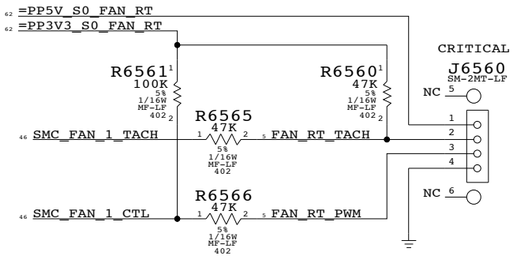
SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	64	103

Left Fan



Right Fan



Fan Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	65	103

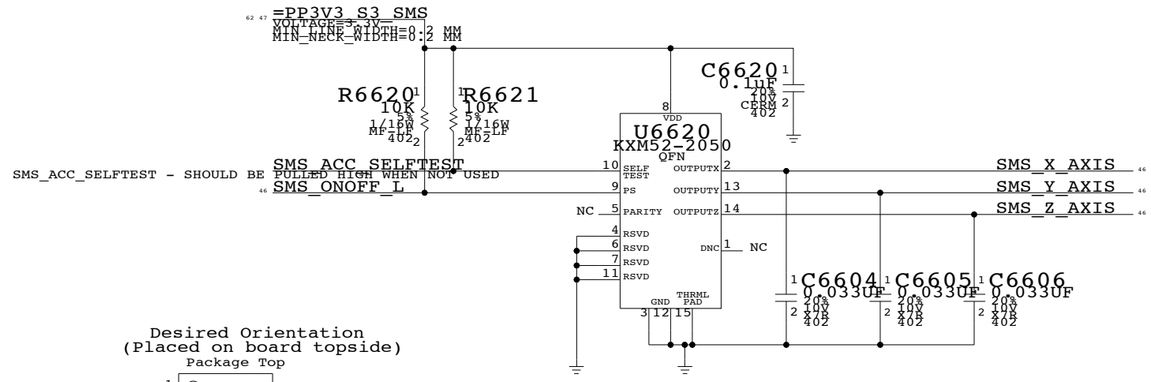
PAGE NOTES

INPUT
=PP3V3_S3_SMS - 3.3V POWER FOR SMS (STAYS ALIVE IN SLEEP)
SMS_ONOFF_L - CONNECT TO SMC TO BE ABLE TO PUT SMS INTO LOW-POWER MODE

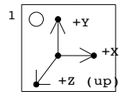
OUTPUT
SMS_ACC_*_AXIS - ACCELEROMETER OUTPUT TO SCU

PAGE HISTORY

5/19/2005 - FIRST REVISION OF PAGE
7/26/2005 - REMOVED BOM TABLE AND UPDATED SYMBOL TO KXM52-2050
7/26/2005 - CONNECTED PD PIN TO SMC'S SMS_ONOFF_L



Desired Orientation
(Placed on board topside)

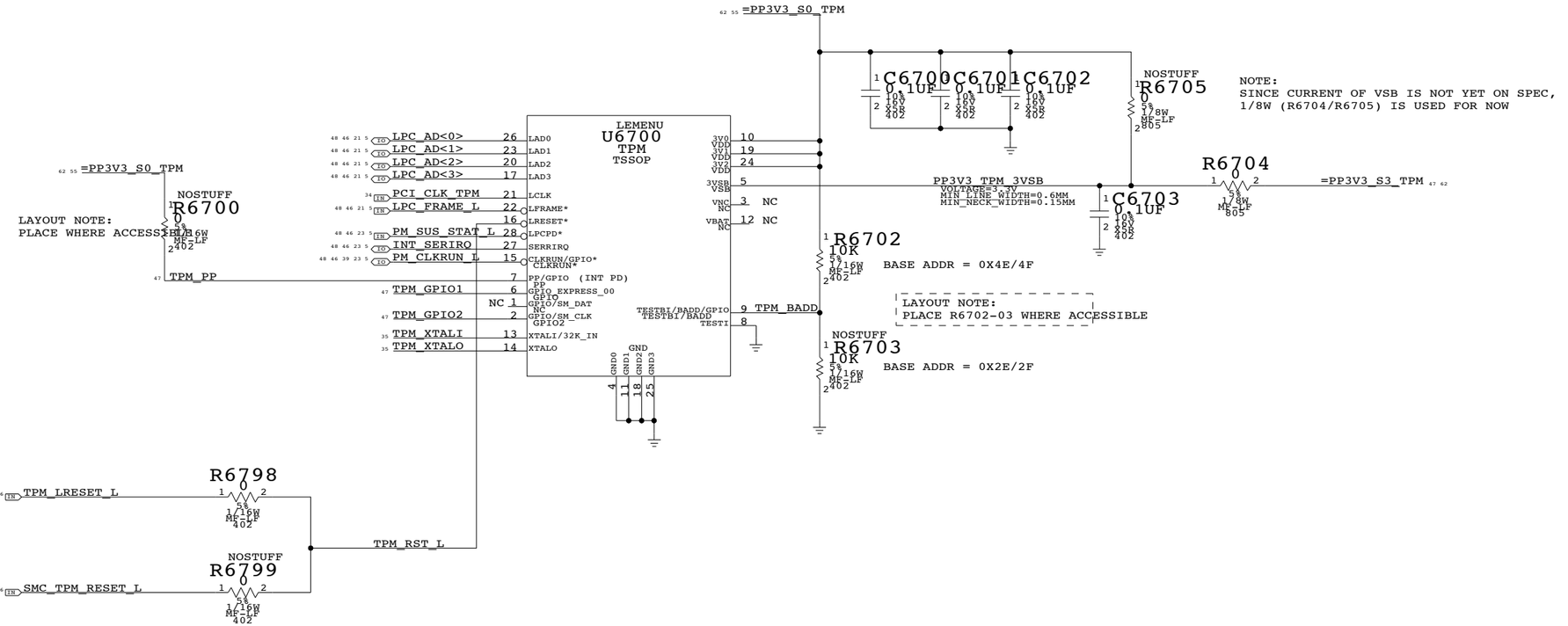


SMS
SYNC_MASTER=MSY SYNC_DATE=07/26/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	66	103



TPM

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03
SCALE: NONE	SHT 67 OF 103	

DPRSLPVR	DPRSTP*	PSI*	Operation	Mode
0	1	1	2-Phase	CCM
0	1	0	1-Phase	CCM
1	0	1	1-Phase	DCM
1	1	0	1-Phase	DCM

CPU VCore Current Sense

Placement Note:
Keep R7599 and R7596 close to inductor

IMVP6 CPU VCore Regulator

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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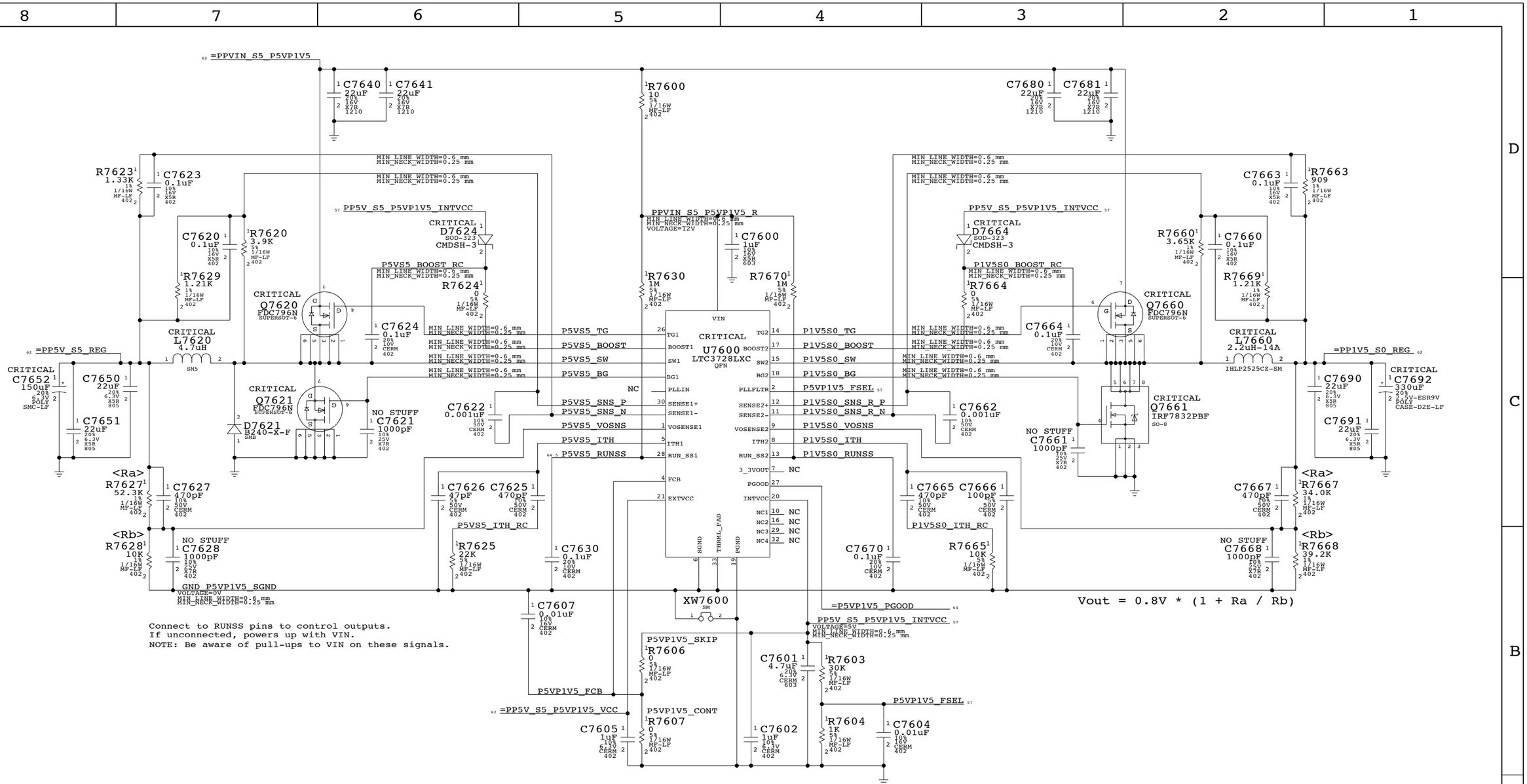
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03
SCALE: NONE	SHT 75 OF 103	



5V / 1.5V Power Supply

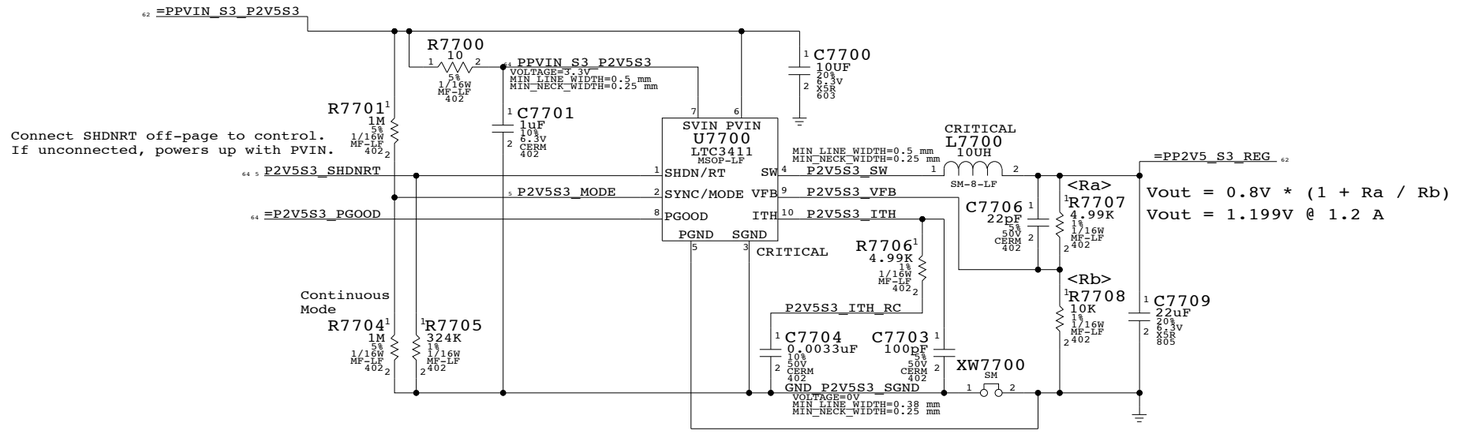
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

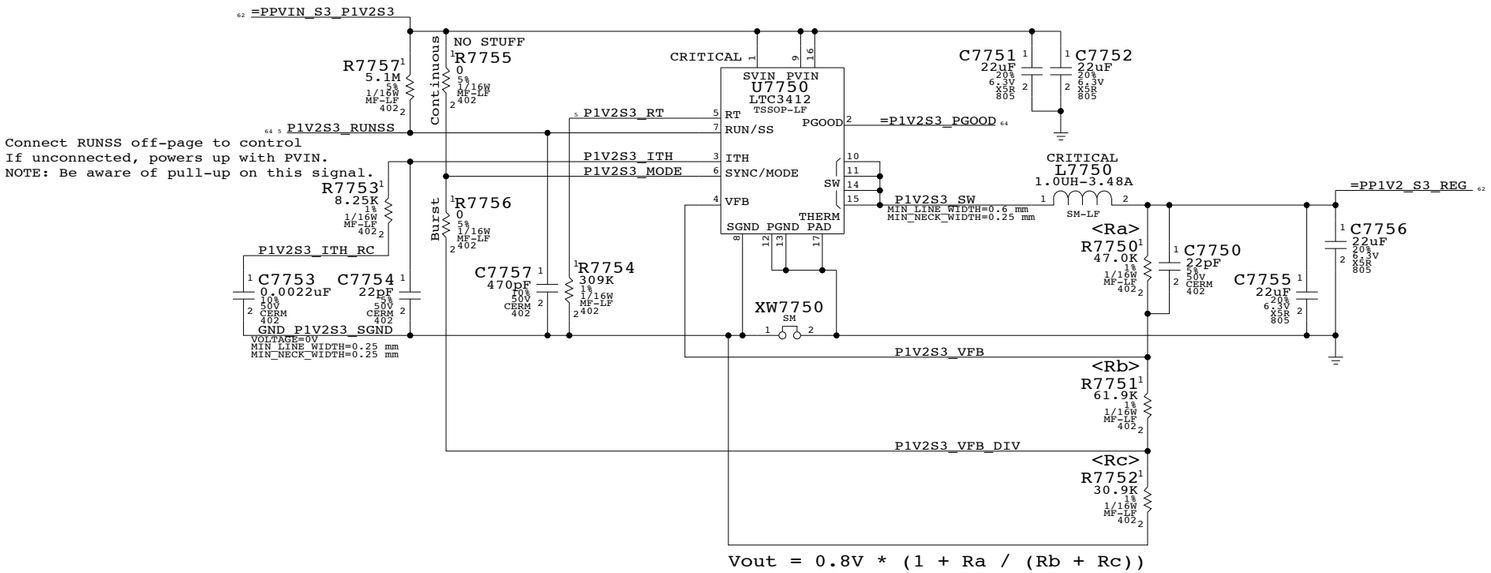
SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	76	103

2.5V S3 Regulator



1.2V S3 Regulator



2.5V & 1.2V Regulators

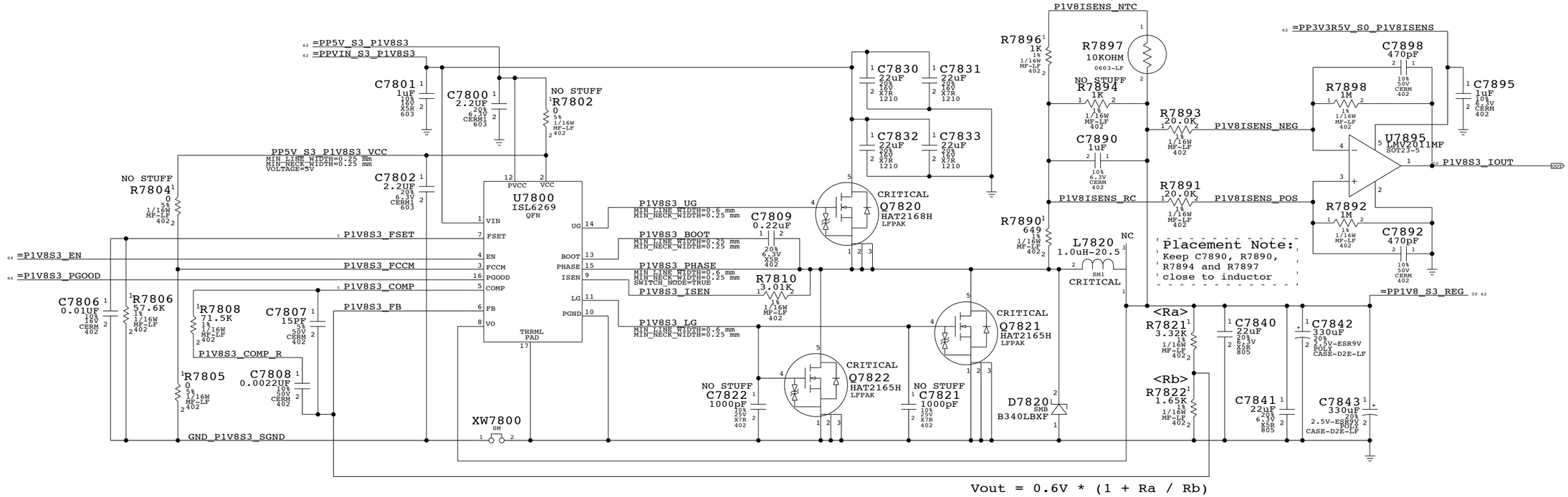
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	77	103

1.8V S3 Current Sense



Vout = 0.6V * (1 + Ra / Rb)

1.8V Supply

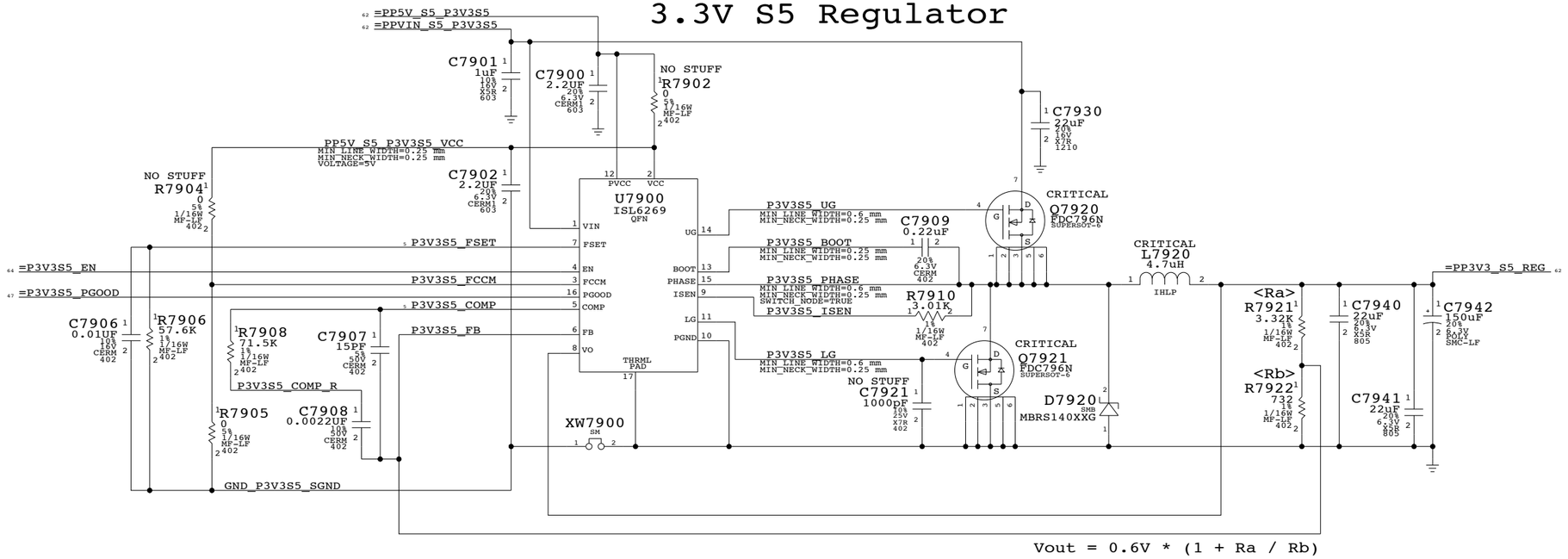
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

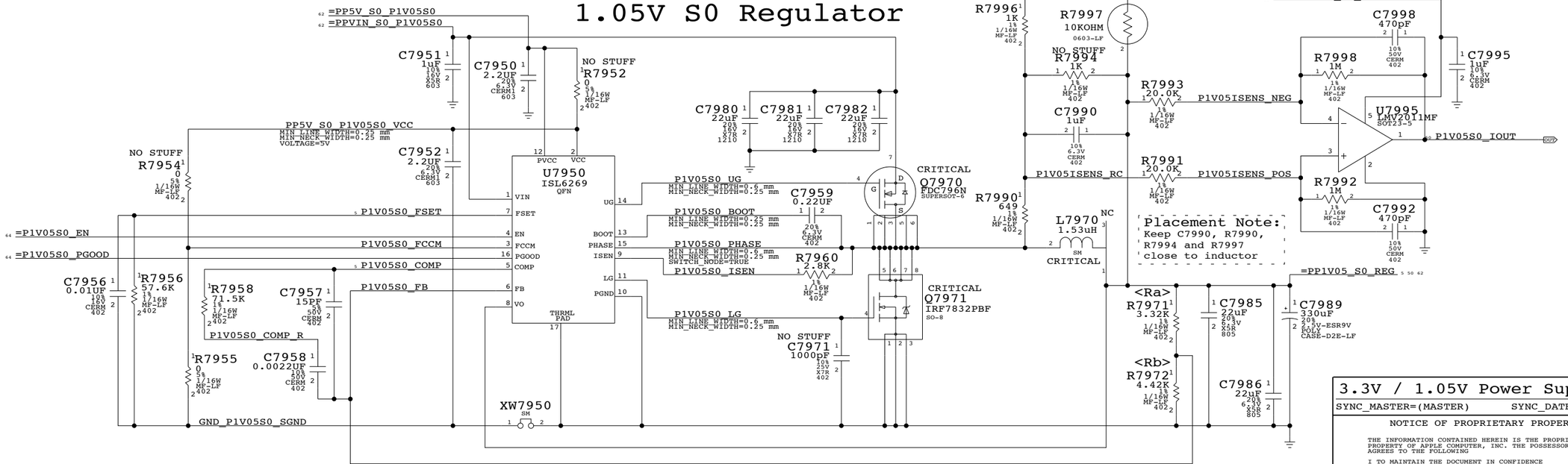
SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	78	103

3.3V S5 Regulator



1.05V S0 Regulator



1.05V Current Sense

3.3V / 1.05V Power Supplies

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

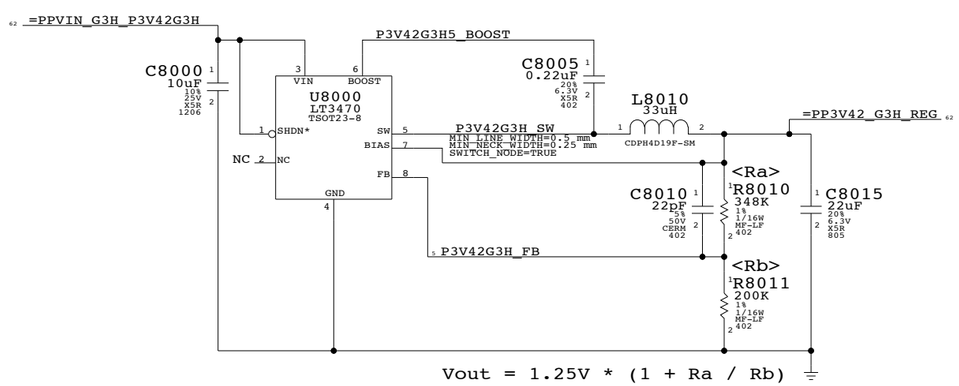
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	79	103

3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator



Vout = 1.25V * (1 + Ra / Rb)

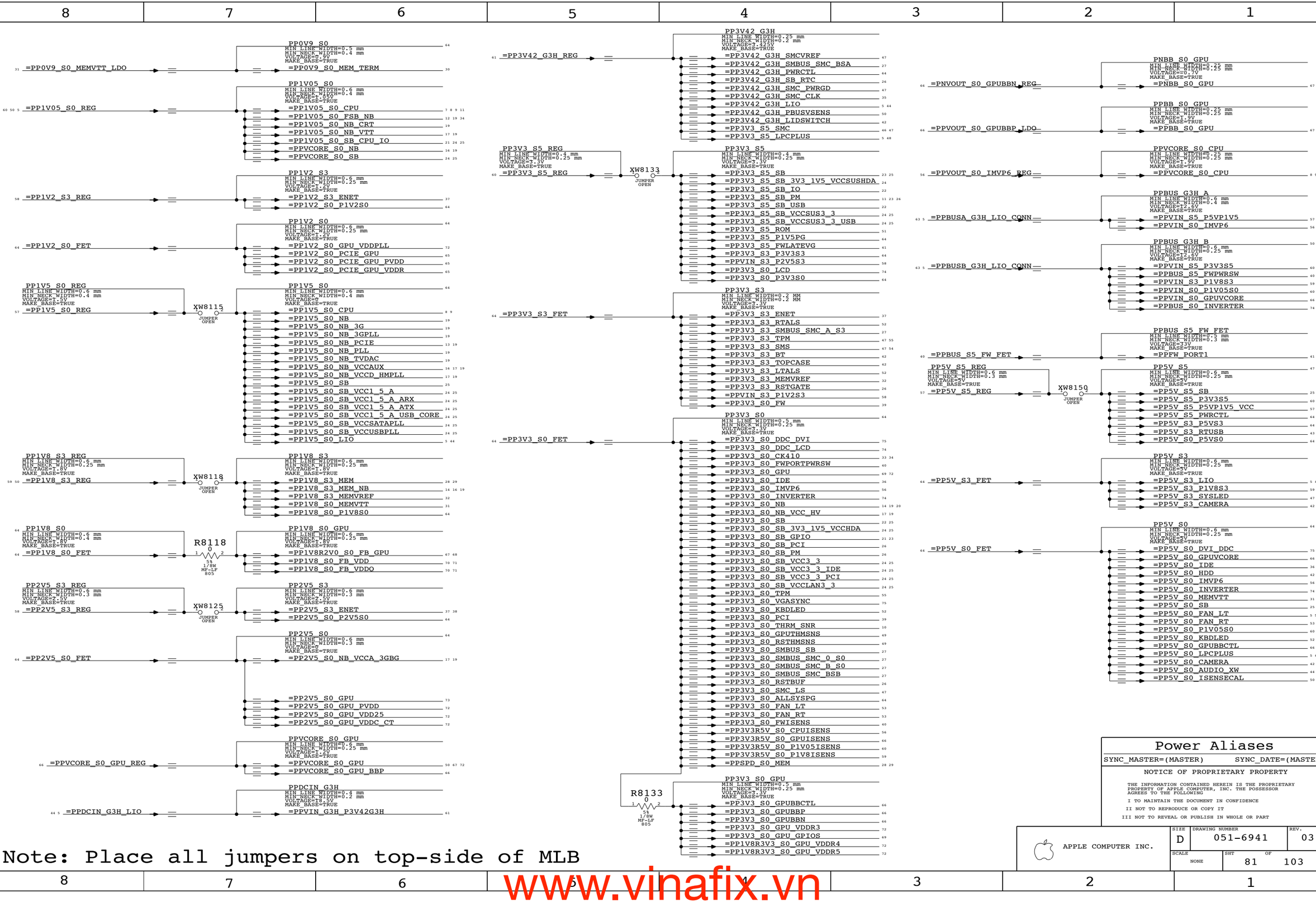
3.3V G3Hot Supply

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

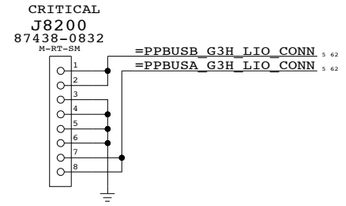
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

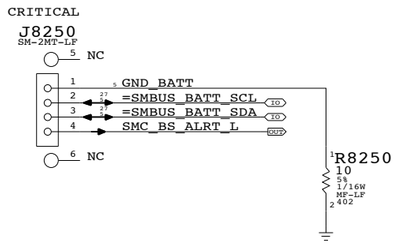
SCALE	SHT	OF
NONE	80	103



Left I/O Power Connector



Battery Connector (Digital Signals)



PBus-In & Battery Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE: NONE

SHT 82 OF 103

Unused PGOOD Signals

57 =P5VP1V5_PGOOD — TP_P5V_P1V5_PGOOD (MAKE_BASE=TRUE)
58 =P2V5S3_PGOOD — TP_P2V5S3_PGOOD (MAKE_BASE=TRUE)
59 =P1V8S3_PGOOD — TP_P1V8S3_PGOOD (MAKE_BASE=TRUE)
58 =P1V2S3_PGOOD — TP_P1V2S3_PGOOD (MAKE_BASE=TRUE)

These rails are monitored by LTC2908

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

5V S3 FET

Q8300 FDC638P SM-LF
62 =PP5V_S3_P5VS3 → Q8300 pin 4; Q8300 pin 3 → =PP5V_S3_FET 62
64 =P5VS3_EN_L → R8300 0 5% 1/16W MF-LF 402 → P5VS3_EN_L_RC
C8300 0.0022uF 10% 50V CERM 402 (Q8300 pin 3 to pin 1)

5V S0 FET

Q8305 FDC638P SM-LF
62 =PP5V_S0_P5VS0 → Q8305 pin 4; Q8305 pin 3 → =PP5V_S0_FET 62
64 =P5VS0_EN_L → R8305 0 5% 1/16W MF-LF 402 → P5VS0_EN_L_RC
C8305 0.0022uF 10% 50V CERM 402 (Q8305 pin 3 to pin 1)
C8306 22uF 20% 6.3V X5R 805 (=PP5V_S0_FET to GND)
C8307 22uF 20% 6.3V X5R 805 (=PP5V_S0_FET to GND)

2.5V S0 FET

62 =PP2V5_S0_P2V5S0 → Q8320 ST3446DV TSOP-LF pin 1; Q8320 pin 3 → =PP2V5_S0_FET 62
C8320 0.0022uF 10% 50V CERM 402 (Q8320 pin 1 to pin 2)
64 =P2V5S0_EN → R8320 0 5% 1/16W MF-LF 402 → P2V5S0_EN_RC

3.3V S3 FET

Q8310 FDC638P SM-LF
62 =PP3V3_S3_P3V3S3 → Q8310 pin 4; Q8310 pin 3 → =PP3V3_S3_FET 62
64 =P3V3S3_EN_L → R8310 0 5% 1/16W MF-LF 402 → P3V3S3_EN_L_RC
C8310 0.0022uF 10% 50V CERM 402 (Q8310 pin 3 to pin 1)

3.3V S0 FET

Q8315 FDC638P SM-LF
62 =PP3V3_S0_P3V3S0 → Q8315 pin 4; Q8315 pin 3 → =PP3V3_S0_FET 62
64 =P3V3S0_EN_L → R8315 0 5% 1/16W MF-LF 402 → P3V3S0_EN_L_RC
C8315 0.0022uF 10% 50V CERM 402 (Q8315 pin 3 to pin 1)

1.8V S0 FET

62 =PP1V8_S0_P1V8S0 → Q8325 FDC796N SUPERSOT-6 pin 7; Q8325 pin 5 → =PP1V8_S0_FET 62
C8325 0.0022uF 10% 50V CERM 402 (Q8325 pin 7 to pin 4)
64 =P1V8S0_EN → R8325 0 5% 1/16W MF-LF 402 → P1V8S0_EN_RC
C8326 22uF 20% 6.3V X5R 805 (=PP1V8_S0_FET to GND)
C8327 22uF 20% 6.3V X5R 805 (=PP1V8_S0_FET to GND)

Power Control Signals

64 62 =PP5V_S5_PWRCTL
R8350 10K 5% 1/16W MF-LF 402
R8351 10K 5% 1/16W MF-LF 402
PM_SLP_S3_LS5V_L (MAKE_BASE=TRUE) → =P2V5S0_EN 64, =P1V8S0_EN 64, =P1V2S0_EN 64
Q8350 2N7002DW-X-F SOT-363
PM_SLP_S3_LS5V (MAKE_BASE=TRUE) → =P5VS0_EN_L 64, =P3V3S0_EN_L 64, LIO_P3V3S0_EN_L 5 44, P1V5S0_RUNSS 5 57
1.5V Enable has pull-up to PBUS
Q8357 2N7002DW-X-F SOT-363
46 23 PM_SLP_S3_L
R8356 100K 5% 1/16W MF-LF 402
Q8350 2N7002DW-X-F SOT-363
(PM_SLP_S3_L) (MAKE_BASE=TRUE) → =P1V05S0_EN 60, =GPUVCORE_EN 66, =MEMVREF_EN 32

64 62 =PP5V_S5_PWRCTL
R8355 10K 5% 1/16W MF-LF 402
PM_SLP_S4_LS5V (MAKE_BASE=TRUE) → =P5VS3_EN_L 64, =P3V3S3_EN_L 64, P1V2S3_RUNSS 5 58
1.2V Enable has pull-up to 3.3V
46 23 PM_SLP_S4_L
Q8355 2N7002DW-X-F SOT-363
Q8355 2N7002DW-X-F SOT-363
R8357 100K 5% 1/16W MF-LF 402
(PM_SLP_S4_L) (MAKE_BASE=TRUE) → =P1V8S3_EN 59, =RTUSB_EN 43, LIO_P3V3S3_EN 5 44
58 PPVIN_S3_P2V5S3
Q8358 TP0610 SOT23-3
P2V5S3_SHDNRT 5 58
2.5V SHDN/RT pin has dual purpose and pull-down at regulator.

62 =PP3V42_G3H_PWRCTL
50 46 SMC_PM_G2_EN
R8358 100K 5% 1/16W MF-LF 402
(SMC_PM_G2_EN) (MAKE_BASE=TRUE) → =P3V3S5_EN 60
R8359 470K 5% 1/16W MF-LF 402
P5VS5_RUNSS 5 57
5V Enable has pull-up to PBUS
SMC_PM_G2_EN_L
Q8359 2N7002DW-X-F SOT-363
Q8359 2N7002DW-X-F SOT-363

1.5V / 1.05V PWRGD Circuit

Reports when 1.5V S0 and 1.05V S0 are in regulation

62 =PP3V3_S5_P1V5PG
62 PP1V5_S0
R8361 27.4K 1% 1/16W MF-LF 402
R8363 4.99K 1% 1/16W MF-LF 402
C8360 0.1uF 20% 10V CERM 402
0.89V Reference
R8362 10K 1% 1/16W MF-LF 402
R8364 10K 1% 1/16W MF-LF 402
U8360 LMC7211 SM-LF
P1V0_P1V5PG_REF
P1V5S0_COMP_POS
P1V5S0_PGOOD
R8365 10K 5% 1/16W MF-LF 402
1.5V Comp threshold set to 1.32V (88%)
58 IMVP_PWRGD_IN
60 =P1V05S0_PGOOD
P1V5P1V05S0_PGOOD (MAKE_BASE=TRUE)
ISL6269 undervoltage threshold 81-87% (0.85 - 0.91V)
NOTE: R8365 acts as 10K pull-up for PGOOD signal

Other S0 Rails PWRGD Circuit

Reports when 5V S0, 3.3V S0, 2.5V S0, 1.8V S0, 1.2V S0 and 0.9V S0 are in regulation

62 PP5V_S0
62 PP3V3_S0
62 PP2V5_S0
62 PP1V8_S0
62 PP1V2_S0
62 PP0V9_S0
C8370 0.1uF 20% 10V CERM 402
C8371 0.1uF 20% 10V CERM 402
R8374 68.1K 1% 1/16W MF-LF 402
R8372 124K 1% 1/16W MF-LF 402
U8370 LTC2908 ULP
V1 V2 V3 V4 CRITICAL VADJ1 VADJ2 RST* THRML PAD GND
S0PGOOD_1V2_DIV
S0PGOOD_0V9_DIV
S0PGOOD_PWROK
R8376 549K 1% 1/16W MF-LF 402
R8375 100K 1% 1/16W MF-LF 402
R8373 100K 1% 1/16W MF-LF 402
LTC2908 threshold is 95% (4.75V, 3.135V, 2.375V, 1.71V, 1.14V, 0.86V)
LTC2908 sources 6uA at 5.0V
R8375 serves as pull-down
and 3.3V level-shifter.

1.2V S0 FET

62 =PP1V2_S0_P1V2S0 → Q8330 ST3446DV TSOP-LF pin 1; Q8330 pin 3 → =PP1V2_S0_FET 62
C8330 0.0022uF 10% 50V CERM 402 (Q8330 pin 1 to pin 2)
64 =P1V2S0_EN → R8330 0 5% 1/16W MF-LF 402 → P1V2S0_EN_RC

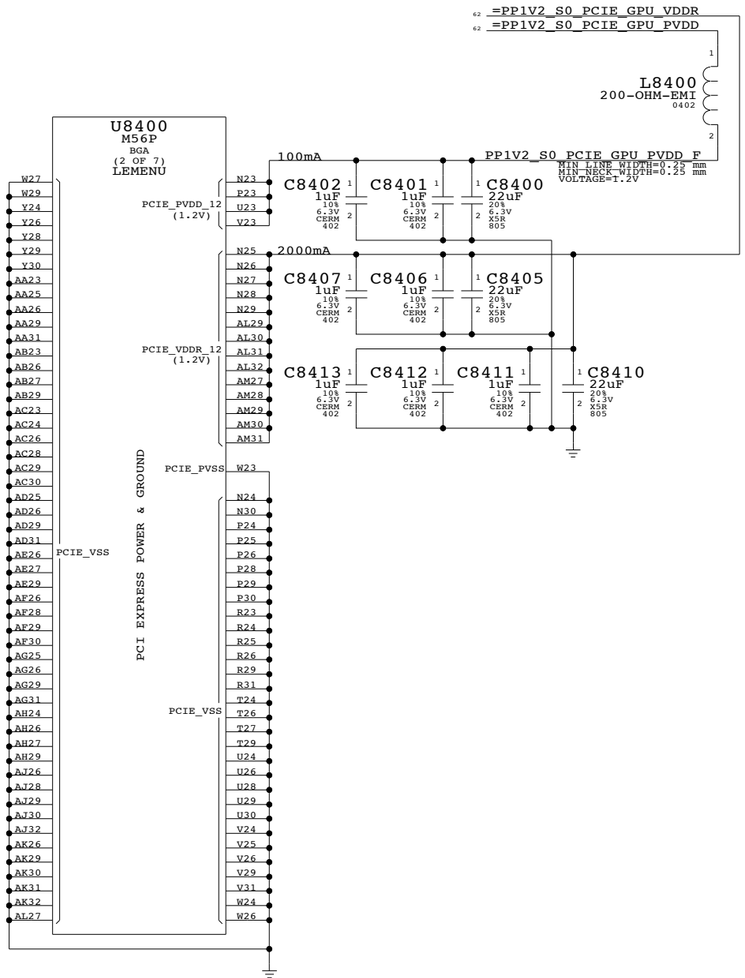
=PP3V3_S0_ALLSYSPG 62
U8380 MC74VHC1G08 SC70 → ALL_SYS_PWRGD OUT
C8380 0.1UF 20% 10V CERM 402

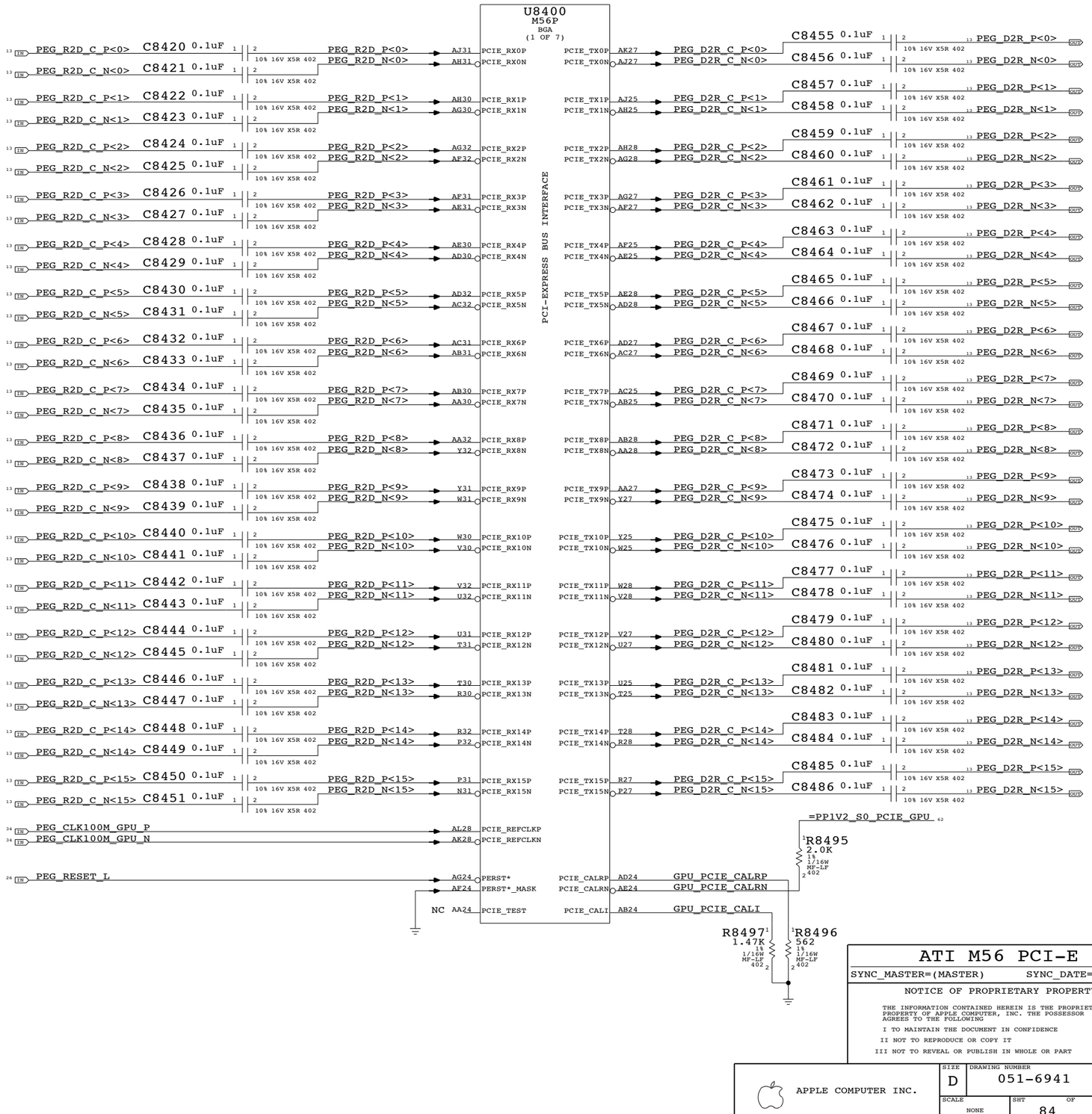
S3/S0 FETs & Power Control

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03
SCALE: NONE	SHT 83 OF 103	





ATI M56 PCI-E

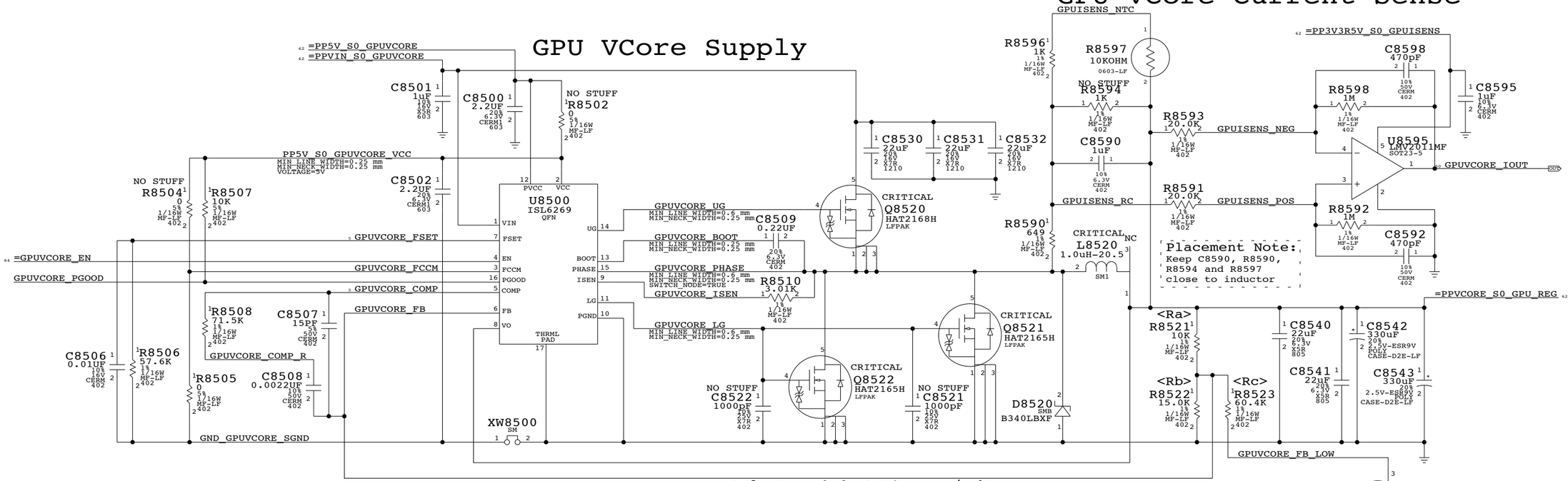
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	84	103

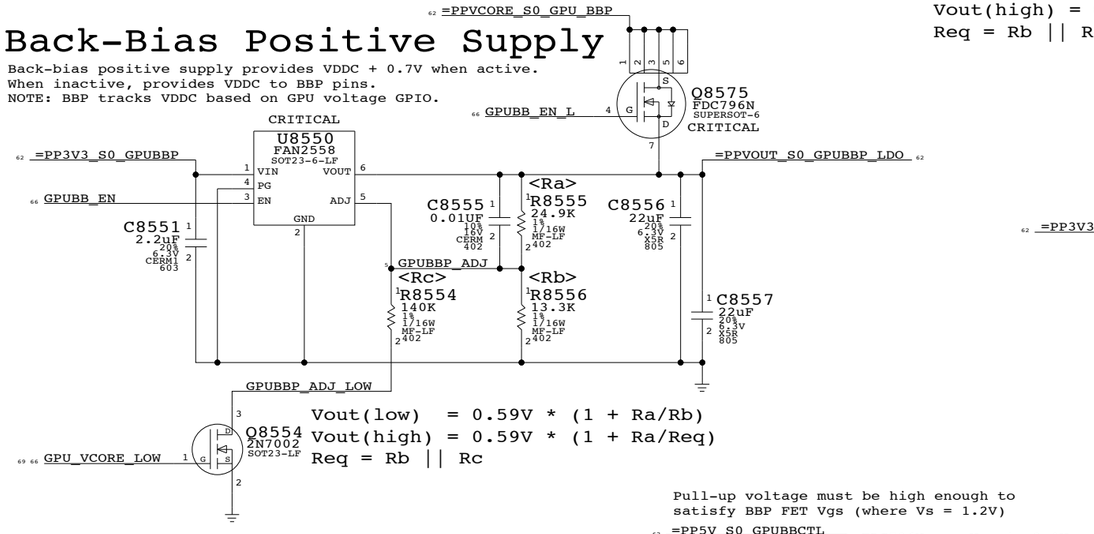
GPU VCore Supply



Vout(low) = 0.6V * (1 + Ra / Rb)
Vout(high) = 0.6V * (1 + Ra / Req)
Req = Rb || Rc

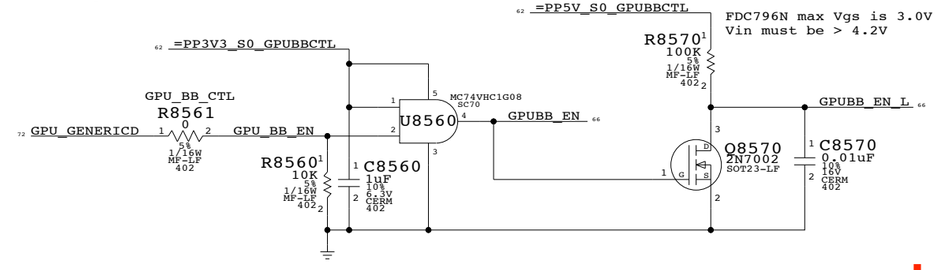
Back-Bias Positive Supply

Back-bias positive supply provides VDDC + 0.7V when active.
When inactive, provides VDDC to BBP pins.
NOTE: BBP tracks VDDC based on GPU voltage GPIO.



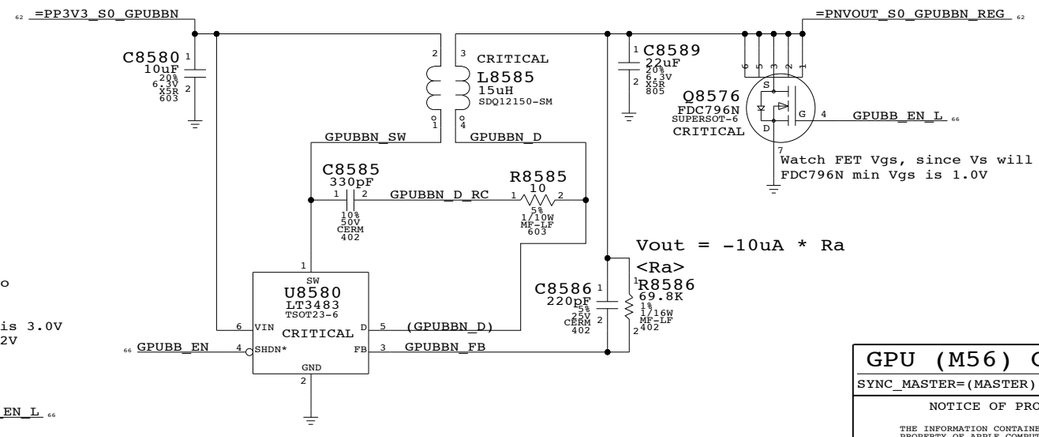
Vout(low) = 0.59V * (1 + Ra/Rb)
Vout(high) = 0.59V * (1 + Ra/Req)
Req = Rb || Rc

Pull-up voltage must be high enough to satisfy BBP FET Vgs (where Vs = 1.2V)



Back-Bias Negative Supply

Back-bias negative supply provides VSS - 0.7V when active.
When inactive, provides VSS to BBN pins.



Vout = -10uA * Ra

GPU (M56) Core Supplies	
SYNC_MASTER=(MASTER)	SYNC_DATE=(MASTER)

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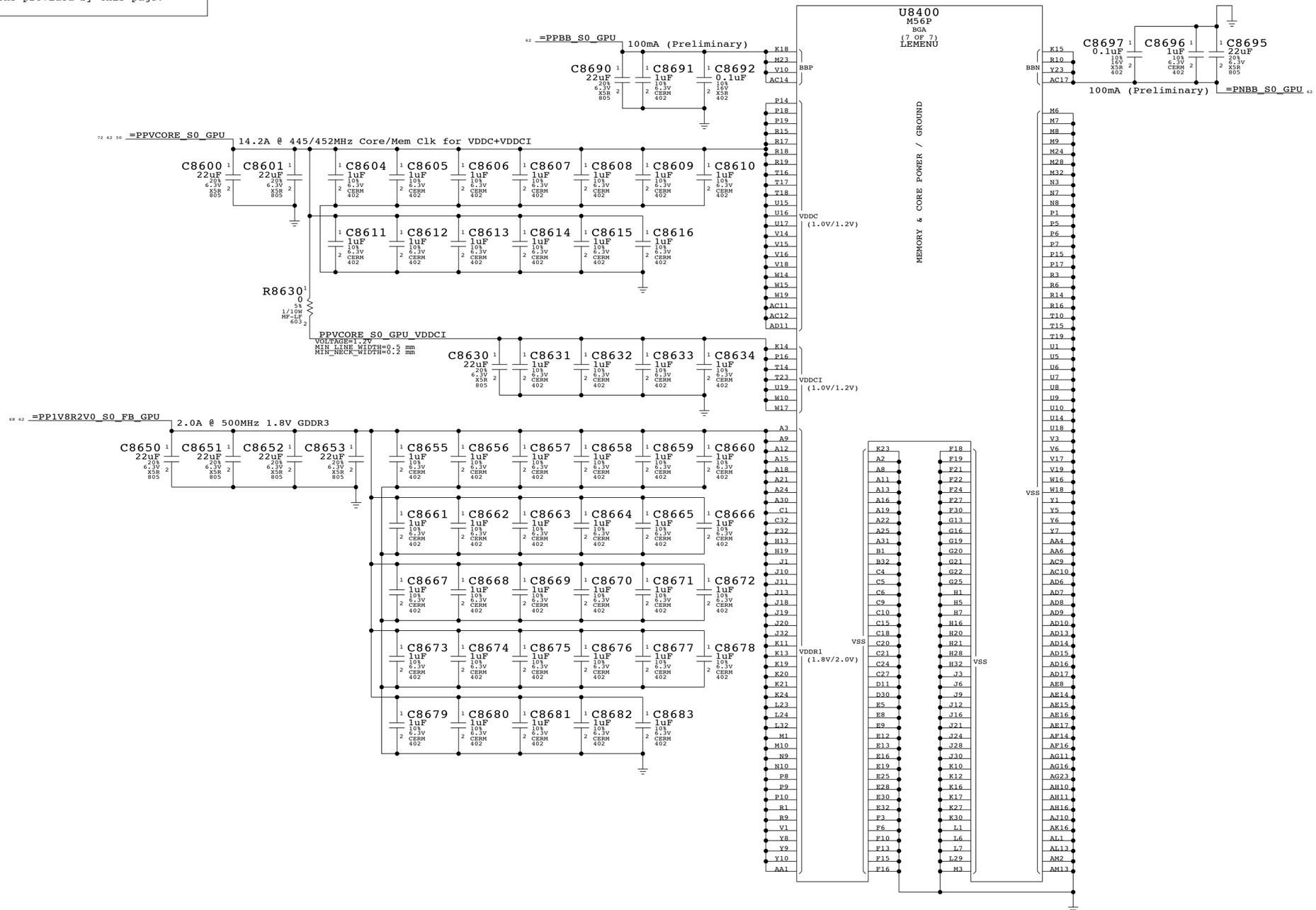
SIZE	DRAWING NUMBER	REV.
D	051-6941	03
SCALE: NONE	SHT 85 OF 103	

Page Notes

Power aliases required by this page:
- =PP1V5_GPU_VDD15
- =PP1VR1V3_GPU_VCORE

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



ATI M56 Core Power

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

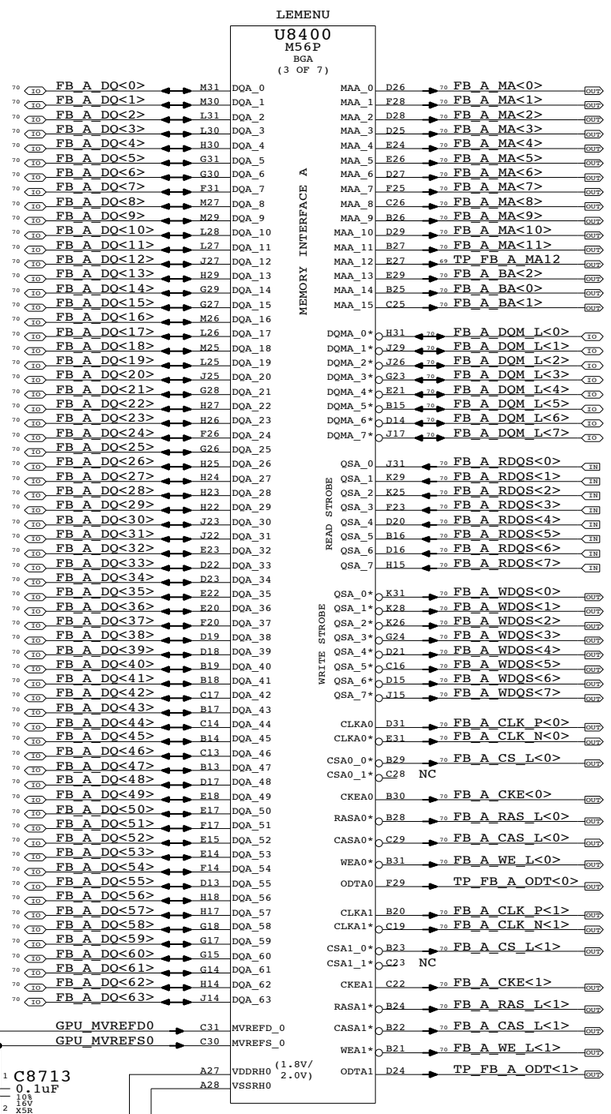
SCALE	SHT	OF
NONE	86	103

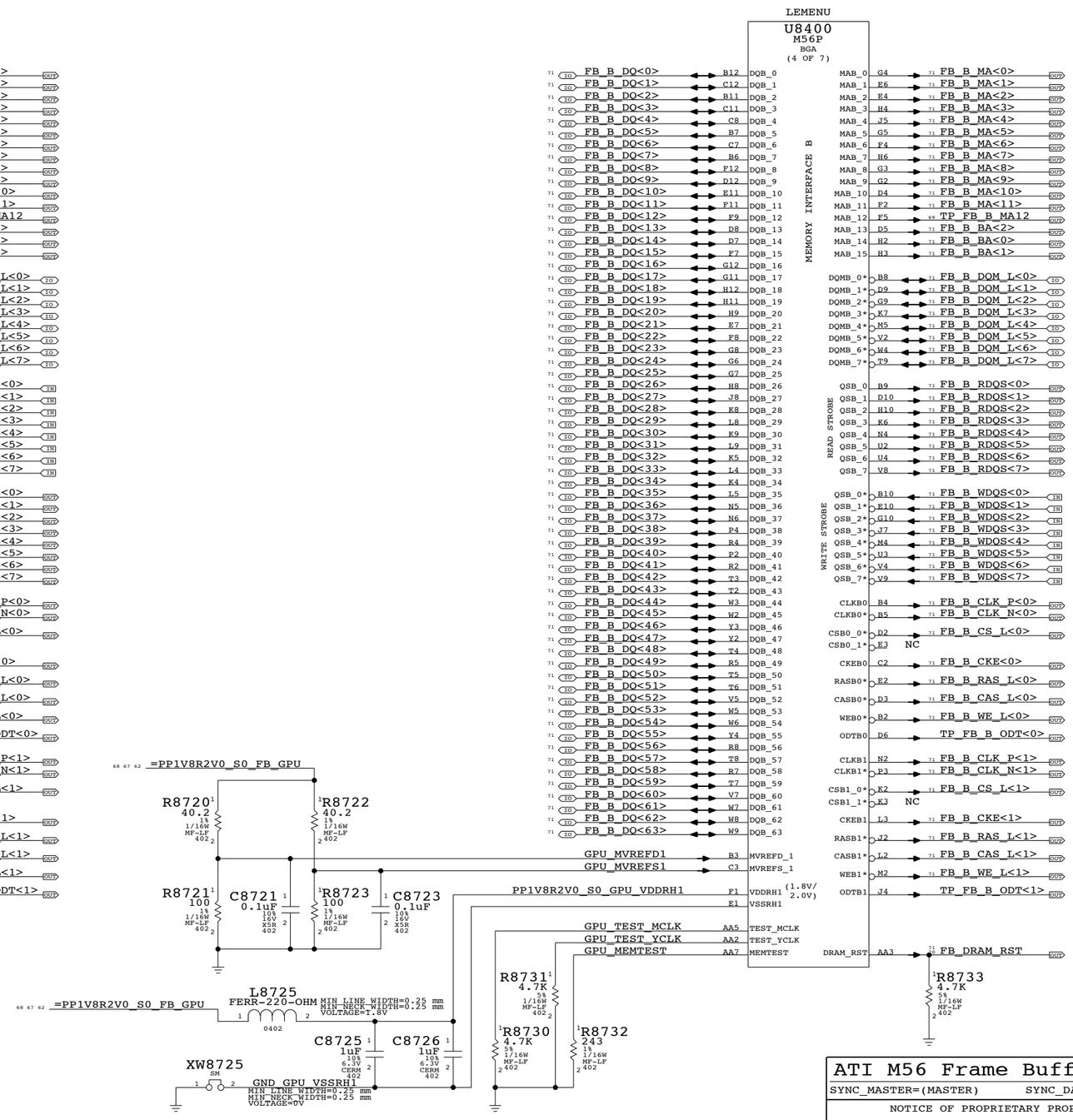
Page Notes

Power aliases required by this page:
- =PP1V8R2V0_S0_FB_GPU

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)





ATI M56 Frame Buffer I/F

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	87	103

	Serial ROM	TestBus	Misc	Straps	
GPU_GPIO_0	IPD	TESTIN[0]		TX_PWRS_ENb	
GPU_GPIO_1	IPD	TESTIN[1]		TX_DEEMPH_EN	
GPU_GPIO_2	VDD_VCL	TESTIN[2]		Reserved	
GPU_GPIO_3		TESTIN[3]		Reserved	
GPU_GPIO_4	IPD	TESTIN[4]		DEBUG_ACCESS	
GPU_GPIO_5		TESTIN[5]		Reserved	
GPU_GPIO_6		TESTIN[6]		Reserved	
GPU_GPIO_7	ENA_BL	TESTIN[7]			GPU_BLON (MAKE_BASE=TRUE)
GPU_GPIO_8	ROMSO	TESTWR		Reserved	
GPU_GPIO_9	IPD ROMSI			ROMIDCFG[3]	
GPU_GPIO_10	ROMSCK	TESTOUT[8]			TP_GPU_GPIO_10 (MAKE_BASE=TRUE)
GPU_GPIO_11	IPD	TESTOUT[9]		ROMIDCFG[0]	Required for debug access
GPU_GPIO_12	IPD	TESTOUT[10]		ROMIDCFG[1]	Required for debug access
GPU_GPIO_13	IPD	TESTOUT[11]		ROMIDCFG[2]	Required for debug access
GPU_GPIO_14		TESTIN[8]			NC_GPU_GPIO_14 (MAKE_BASE=TRUE, NO_TEST=TRUE)
GPU_GPIO_15		TESTIN[9]	PWRCNTL		GPU_VCORE_LOW (MAKE_BASE=TRUE)
GPU_GPIO_16			SS_IN		GPU_CLK27MSS_IN (MAKE_BASE=TRUE)
GPU_GPIO_17			Thm Mon Int		NC_GPU_GPIO_17 (MAKE_BASE=TRUE, NO_TEST=TRUE)

GPU_GPIO_18 — NC_GPU_GPIO_18 (MAKE_BASE=TRUE, NO_TEST=TRUE)
GPU_GPIO_19 — NC_GPU_GPIO_19 (MAKE_BASE=TRUE, NO_TEST=TRUE)
GPU_GPIO_20 — NC_GPU_GPIO_20 (MAKE_BASE=TRUE, NO_TEST=TRUE)
GPU_GPIO_21 — NC_GPU_GPIO_21 (MAKE_BASE=TRUE, NO_TEST=TRUE)
GPU_GPIO_22 — NC_GPU_GPIO_22 (MAKE_BASE=TRUE, NO_TEST=TRUE)
GPU_GPIO_23 — NC_GPU_GPIO_23 (MAKE_BASE=TRUE, NO_TEST=TRUE)
GPU_GPIO_24 — NC_GPU_GPIO_24 (MAKE_BASE=TRUE, NO_TEST=TRUE)
GPU_GPIO_25 — NC_GPU_GPIO_25 (MAKE_BASE=TRUE, NO_TEST=TRUE)
GPU_GPIO_26 — NC_GPU_GPIO_26 (MAKE_BASE=TRUE, NO_TEST=TRUE)
GPU_GPIO_27 — NC_GPU_GPIO_27 (MAKE_BASE=TRUE, NO_TEST=TRUE)
GPU_GPIO_28 — NC_GPU_GPIO_28 (MAKE_BASE=TRUE, NO_TEST=TRUE)
GPU_GPIO_29 — NC_GPU_GPIO_29 (MAKE_BASE=TRUE, NO_TEST=TRUE)
GPU_GPIO_30 — NC_GPU_GPIO_30 (MAKE_BASE=TRUE, NO_TEST=TRUE)
GPU_GPIO_31 — NC_GPU_GPIO_31 (MAKE_BASE=TRUE, NO_TEST=TRUE)
GPU_GPIO_32 — NC_GPU_GPIO_32 (MAKE_BASE=TRUE, NO_TEST=TRUE)
GPU_GPIO_33 — NC_GPU_GPIO_33 (MAKE_BASE=TRUE, NO_TEST=TRUE)
GPU_GPIO_34 — NC_GPU_GPIO_34 (MAKE_BASE=TRUE, NO_TEST=TRUE)

=PP3V3_S0_GPU_GPIOS

ROMCFGID[3..0]
0000 = 128MB
0010 = 256MB
0100 = 64MB
0110 = Reserved

R8800 10K 5% 1/16W MF-LF 402
R8801 10K 5% 1/16W MF-LF 402
R8802 NO STUFF 10K 5% 1/16W MF-LF 402
R8803 NO STUFF 10K 5% 1/16W MF-LF 402
R8804 NO STUFF 10K 5% 1/16W MF-LF 402
R8805 NO STUFF 10K 5% 1/16W MF-LF 402
R8806 NO STUFF 10K 5% 1/16W MF-LF 402
R8808 NO STUFF 10K 5% 1/16W MF-LF 402
R8809 NO STUFF 10K 5% 1/16W MF-LF 402
R8811 NO STUFF 10K 5% 1/16W MF-LF 402
R8812 GPU_MEM_256M 10K 5% 1/16W MF-LF 402
R8813 GPU_MEM_64M 10K 5% 1/16W MF-LF 402

Renamed signals

GPU_CLK27M (MAKE_BASE=TRUE) — GPU_XTALIN

Unused signals

NC_GPU_XTALOUT (MAKE_BASE=TRUE, NO_TEST=TRUE) — GPU_XTALOUT
NC_ATI_ROMCS_L (MAKE_BASE=TRUE, NO_TEST=TRUE) — TP_ATI_ROMCS_L
NC_FB_A_MA12 (MAKE_BASE=TRUE, NO_TEST=TRUE) — TP_FB_A_MA12
NC_FB_B_MA12 (MAKE_BASE=TRUE, NO_TEST=TRUE) — TP_FB_B_MA12
NC_GPU_GENERICA (MAKE_BASE=TRUE, NO_TEST=TRUE) — GPU_GENERICA
NC_GPU_GENERICB (MAKE_BASE=TRUE, NO_TEST=TRUE) — GPU_GENERICB
NC_GPU_GENERICC (MAKE_BASE=TRUE, NO_TEST=TRUE) — GPU_GENERICC
NC_GPU_VGA_R (MAKE_BASE=TRUE, NO_TEST=TRUE) — GPU_VGA_R
NC_GPU_VGA_G (MAKE_BASE=TRUE, NO_TEST=TRUE) — GPU_VGA_G
NC_GPU_VGA_B (MAKE_BASE=TRUE, NO_TEST=TRUE) — GPU_VGA_B
NC_GPU_VGA_HSYNC (MAKE_BASE=TRUE, NO_TEST=TRUE) — GPU_VGA_HSYNC
NC_GPU_VGA_VSYNC (MAKE_BASE=TRUE, NO_TEST=TRUE) — GPU_VGA_VSYNC
NC_GPU_R2 (MAKE_BASE=TRUE, NO_TEST=TRUE) — GPU_R2
NC_GPU_G2 (MAKE_BASE=TRUE, NO_TEST=TRUE) — GPU_G2
NC_GPU_B2 (MAKE_BASE=TRUE, NO_TEST=TRUE) — GPU_B2
NC_LVDS_U_DATAP<3> (MAKE_BASE=TRUE, NO_TEST=TRUE) — LVDS_U_DATA_P<3>
NC_LVDS_U_DATAN<3> (MAKE_BASE=TRUE, NO_TEST=TRUE) — LVDS_U_DATA_N<3>
NC_LVDS_L_DATAP<3> (MAKE_BASE=TRUE, NO_TEST=TRUE) — LVDS_L_DATA_P<3>
NC_LVDS_L_DATAN<3> (MAKE_BASE=TRUE, NO_TEST=TRUE) — LVDS_L_DATA_N<3>
NC_ATI_DVPCLK (MAKE_BASE=TRUE, NO_TEST=TRUE) — ATI_DVPCLK
NC_ATI_DVPCNTL<2..0> (MAKE_BASE=TRUE, NO_TEST=TRUE) — ATI_DVPCNTL<2..0>
NC_ATI_DVPDATA<15..0> (MAKE_BASE=TRUE, NO_TEST=TRUE) — ATI_DVPDATA<15..0>

Required for debug access

TP_ATI_DVPDATA<23..16> (MAKE_BASE=TRUE) — ATI_DVPDATA<23..16>

Also required: GPIO10 - GPIO13

=PP3V3_S0_GPU

R9390 4.7K 5% 1/16W MF-LF 402
R9391 4.7K 5% 1/16W MF-LF 402

GPU_DDC_B_CLK
GPU_DDC_B_DATA

GPU Straps

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SIZE	DRAWING NUMBER	REV.
D	051-6941	03

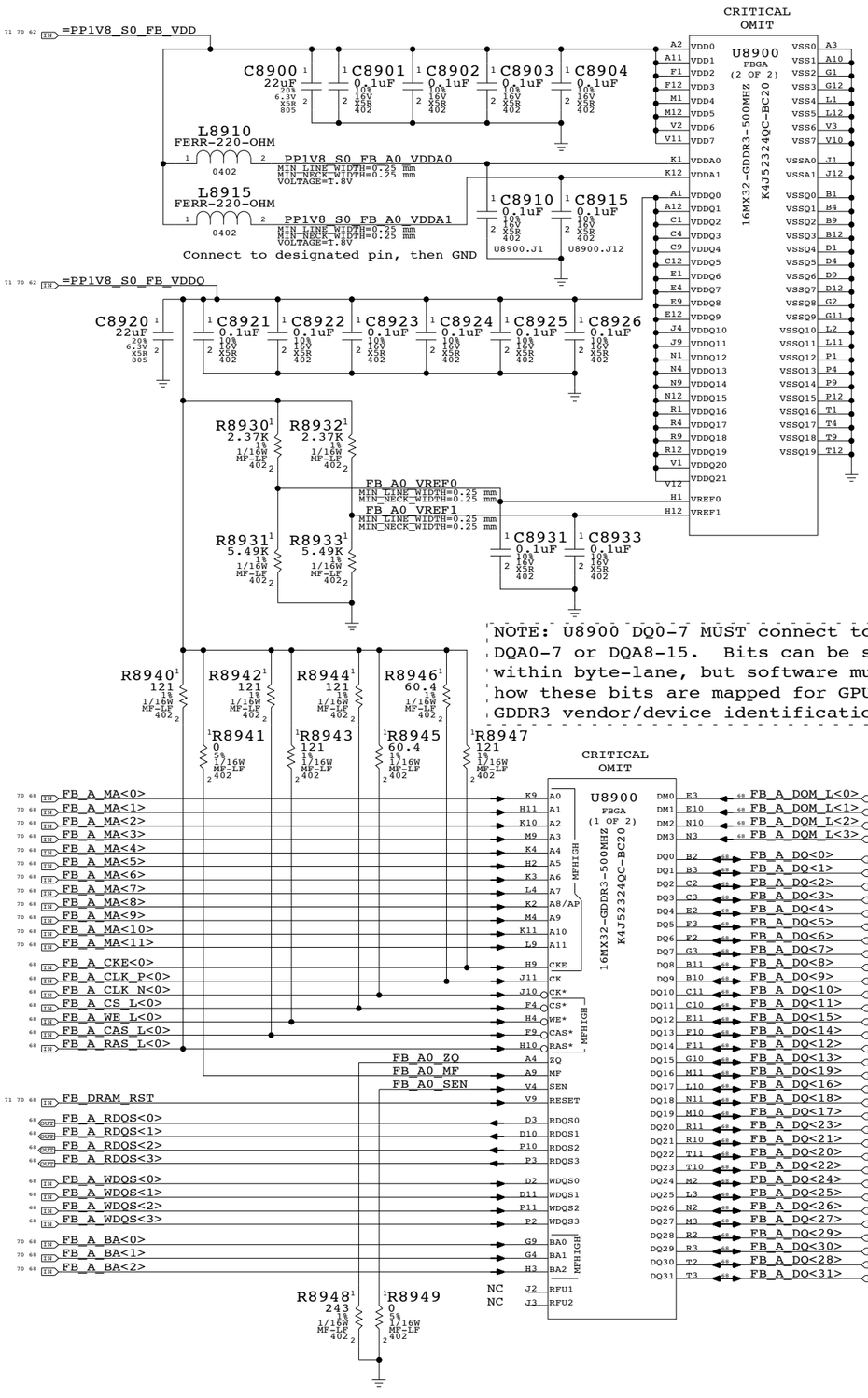
SCALE	SHT	OF
NONE	88	103

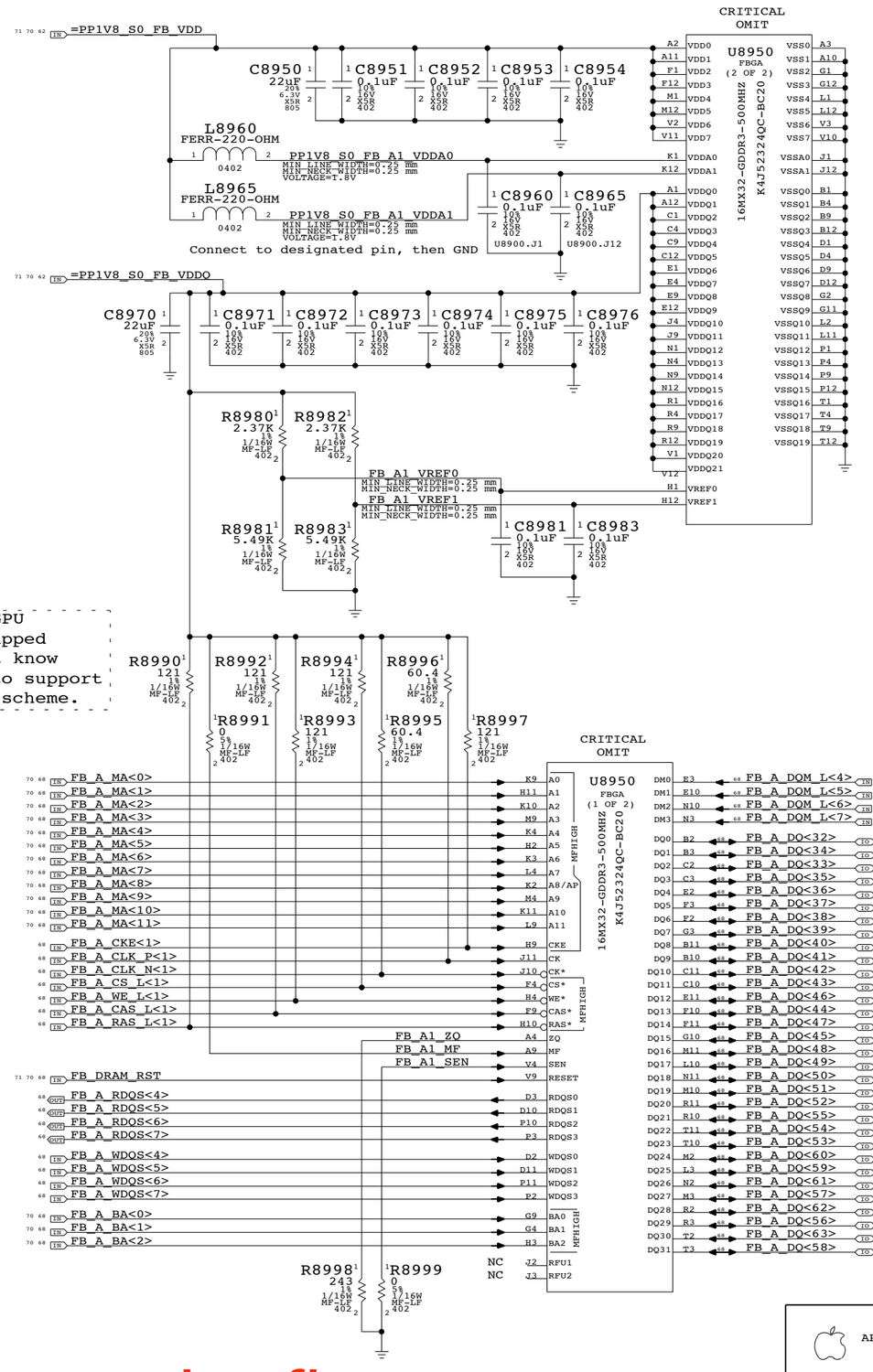
Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)





GDDR3 Frame Buffer A

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

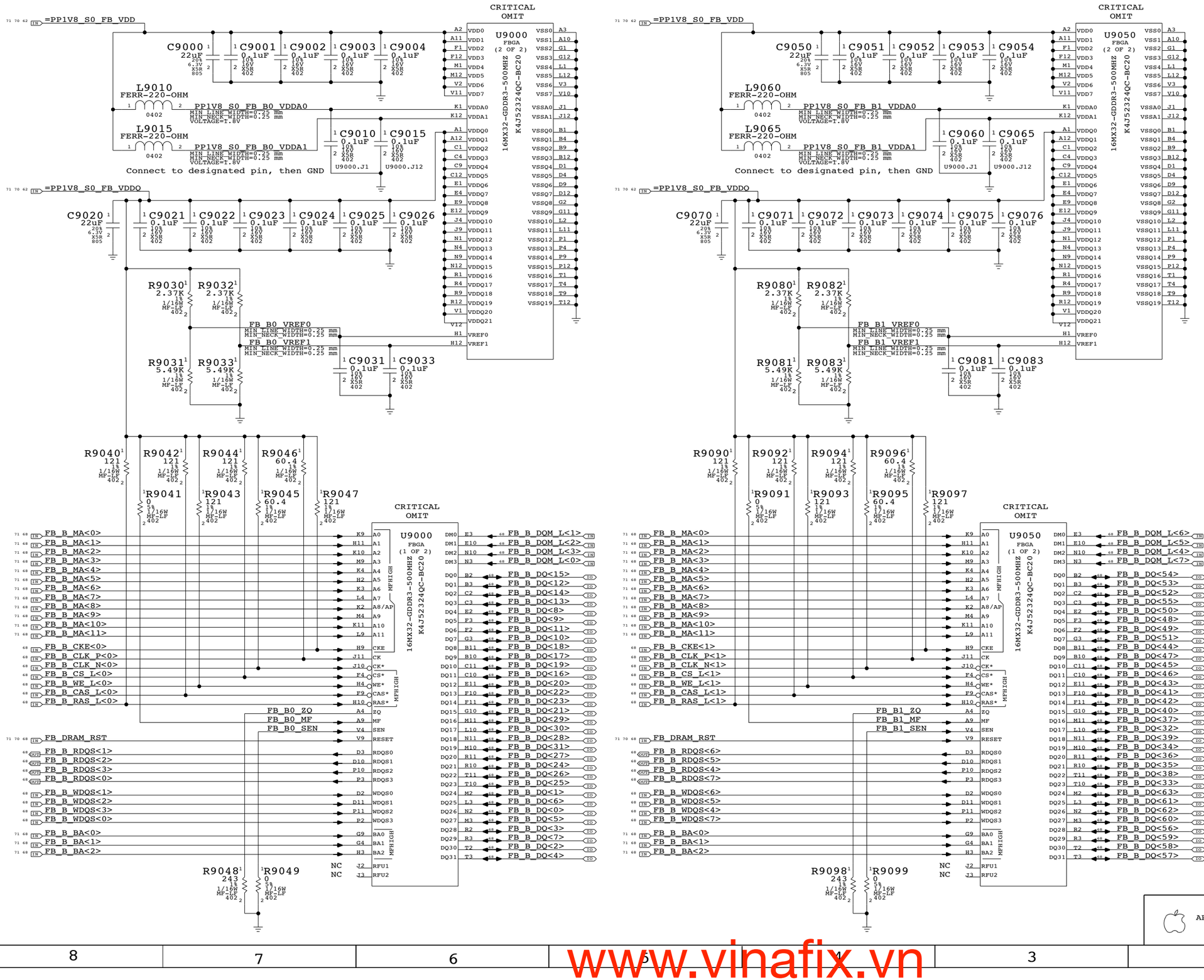
SCALE	SHT	OF
NONE	89	103

Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



GDDR3 Frame Buffer B

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

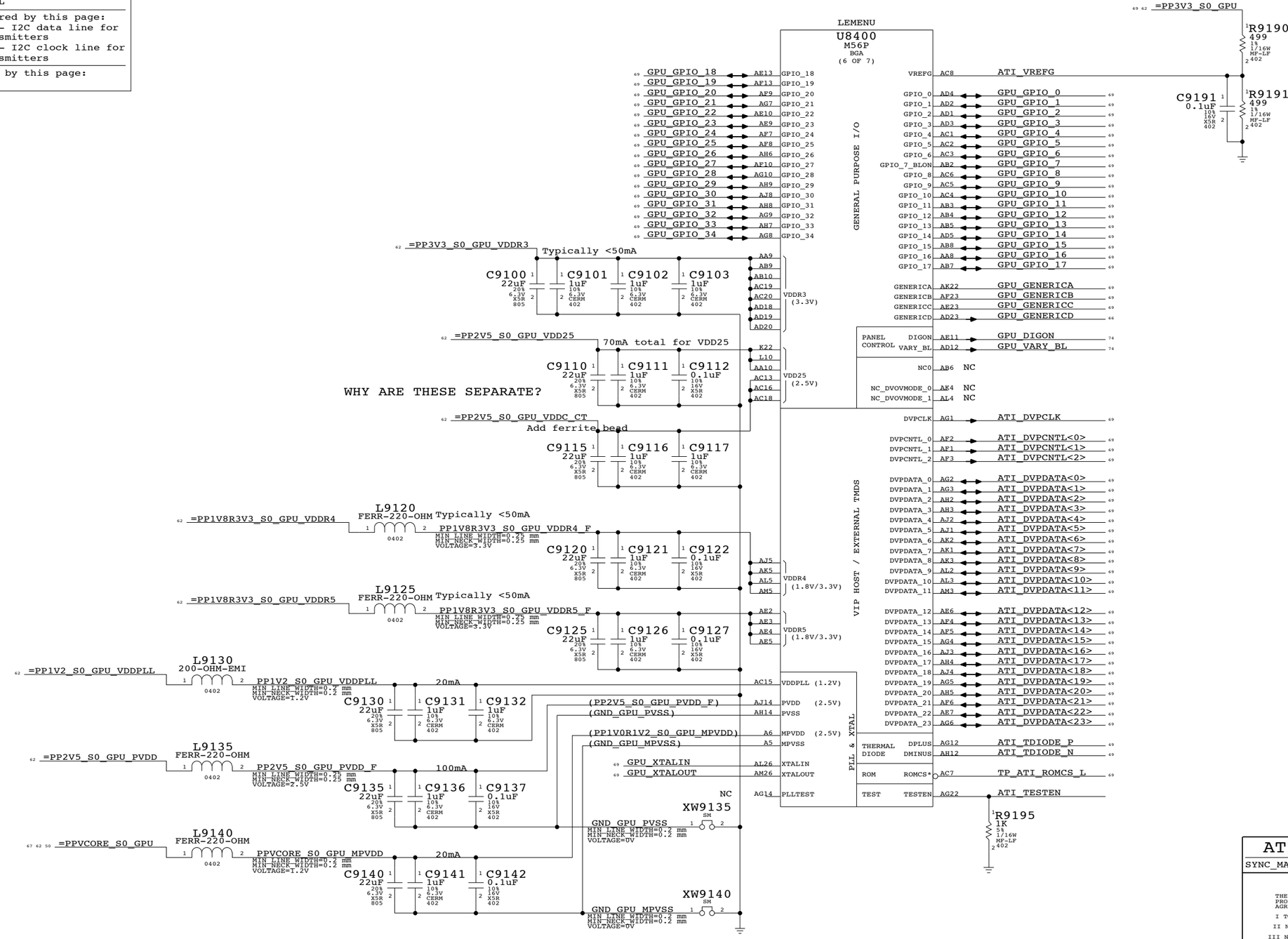
SIZE	DRAWING NUMBER	REV.
D	051-6941	03
SCALE	SHT	OF
NONE	90	103

Page Notes

Power aliases required by this page:
- =PP3V3_GPU_GPIOS
- =PP2V5_PVDD
- =PP1V8_GPU_LVDS_PLL

Signal aliases required by this page:
- =I2C_GPU_TMDS_SDA - I2C data line for external TMDS transmitters
- =I2C_GPU_TMDS_SCL - I2C clock line for external TMDS transmitters

BOM options provided by this page:
(NONE)



ATI M56 GPIO/DVO/Misc

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

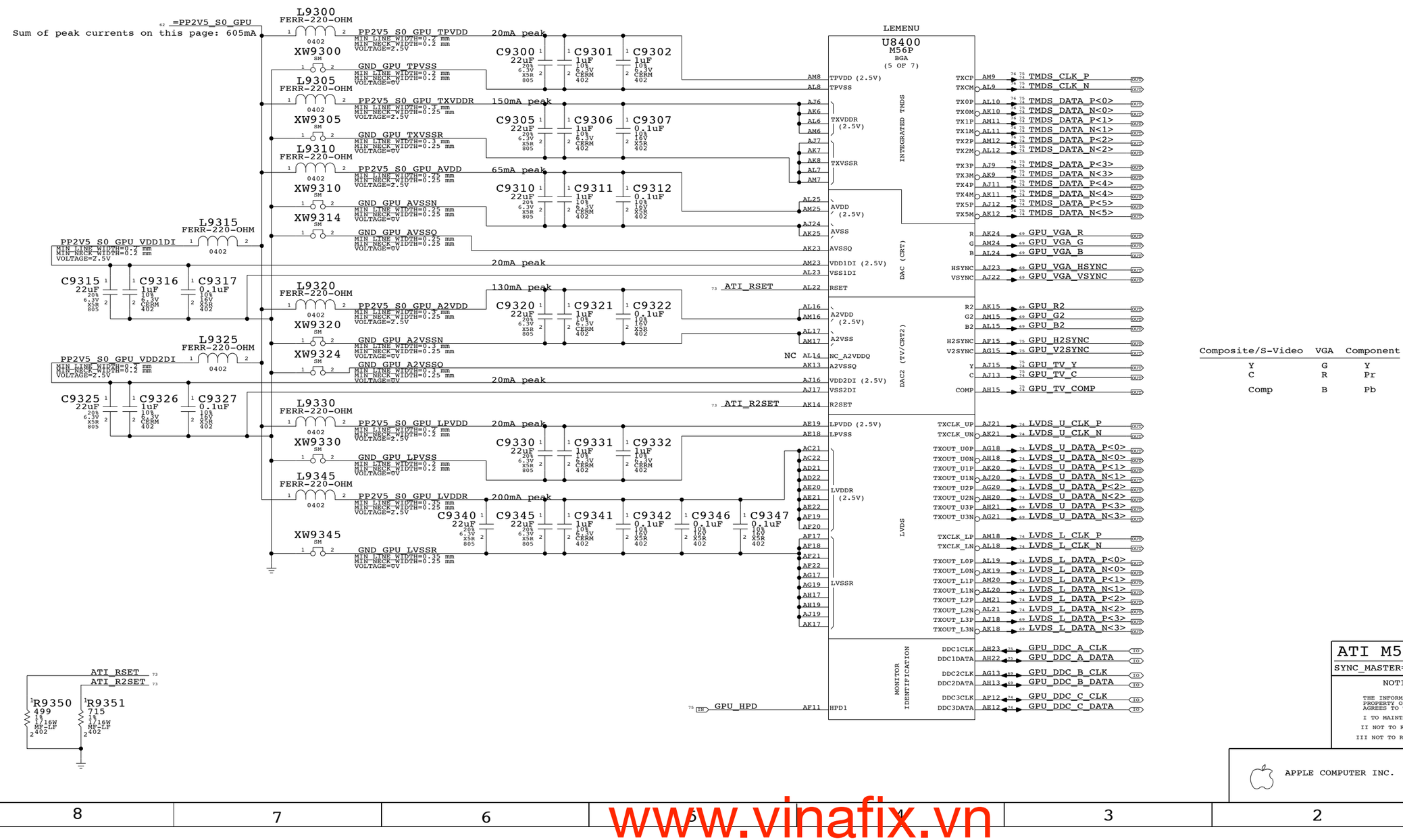
SIZE	DRAWING NUMBER	REV.
D	051-6941	03
SCALE: NONE	SHT 91 OF 103	

Page Notes

Power aliases required by this page:
- =PP2V5_S0_GPU
- =PP1V8R2V5_S0_GPU_LVDDR

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



Composite/S-Video	VGA	Component
Y	G	Y
C	R	Pr
Comp	B	Pb

ATI M56 Video Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03
SCALE: NONE	SHT 93 OF 103	

LCD (LVDS) INTERFACE

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	
	VGA	VGA	GPU_TV_Y
	VGA	VGA	GPU_TV_C
	VGA	VGA	GPU_TV_COMP
	LVDS	LVDS	LVDS_U_CLK_P
	LVDS	LVDS	LVDS_U_CLK_N
	LVDS	LVDS	LVDS_U_DATA_P<2..0>
	LVDS	LVDS	LVDS_U_DATA_N<2..0>
	LVDS	LVDS	LVDS_L_CLK_P
	LVDS	LVDS	LVDS_L_CLK_N
	LVDS	LVDS	LVDS_L_DATA_P<2..0>
	LVDS	LVDS	LVDS_L_DATA_N<2..0>
	TMDS	TMDS	TMDS_CLK_P
	TMDS	TMDS	TMDS_CLK_N
	TMDS	TMDS	TMDS_DATA_P<5..3>
	TMDS	TMDS	TMDS_DATA_N<5..3>
	TMDS	TMDS	TMDS_DATA_P<2..0>
	TMDS	TMDS	TMDS_DATA_N<2..0>

62 =PP3V3_S0_LCD

R9400 100K 5% 1/16W MF-LF 402

C9400 0.0022uF 10% 50V CERM 402

R9401 100K 5% 1/16W MF-LF 402

LCD_PWREN_L_RC

LCD_PWREN_L

Q9400 SI3443DV TSOP-LF

PP3V3_LCD_SW
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V

I9400 FERR-250-OHM SM

C9401 0.001uF 20% 50V CERM 402

6 =GND_CHASSIS_LCD2

LCD_CTL_SMC
R9494 0 5% 1/16W MF-LF 402

46 SMC_DISPLAY_ENABLE

GPU_OR_SMC_DISP_EN

Q9401 2N7002 SOT23-LF

LCD_CTL_GPU
R9495 0 5% 1/16W MF-LF 402

72 GPU_DIGON

62 =PP3V3_S0_DDC_LCD

100K pull-ups are for no-panel case (development)
Panel has 2K pull-ups

R9410 100K 5% 1/16W MF-LF 402

R9411 100K 5% 1/16W MF-LF 402

73 GPU_DDC_C_CLK

73 GPU_DDC_C_DATA

C9410 0.001uF 20% 50V CERM 402

6 =GND_CHASSIS_LCD3

6 =GND_CHASSIS_LCD1

C9420 0.001uF 20% 50V CERM 402

CRITICAL
J9400 MSC-RB30-5-FA F-RT-SM

PP3V3_LCD_CONN
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V

NC

74 73 LVDS_L_DATA_N<0>
74 73 LVDS_L_DATA_P<0>
74 73 LVDS_L_DATA_N<1>
74 73 LVDS_L_DATA_P<1>
74 73 LVDS_L_DATA_N<2>
74 73 LVDS_L_DATA_P<2>
74 73 LVDS_L_CLK_N
74 73 LVDS_L_CLK_P
74 73 LVDS_U_DATA_N<0>
74 73 LVDS_U_DATA_P<0>
74 73 LVDS_U_DATA_N<1>
74 73 LVDS_U_DATA_P<1>
74 73 LVDS_U_DATA_N<2>
74 73 LVDS_U_DATA_P<2>
74 73 LVDS_U_CLK_N
74 73 LVDS_U_CLK_P

C9421 0.001uF 20% 50V CERM 402

6 =GND_CHASSIS_LCD4

INVERTER INTERFACE

62 =PPBUS_S0_INVERTER

L9450 FERR-1K-OHM-EMI SM

PPBUS_S0_INVERTER
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=T2.8V

C9450 0.001uF 20% 50V CERM 402

62 =PP5V_S0_INVERTER

Q9450 FDG6324L SC70-6-LF

R9450 100K 5% 1/16W MF-LF 402

FP_PWR_EN_L

PP5V_INVERTER_SW_F
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V

L9452 400-OHM-EMI SM-1

C9451 10UF 20% 6.3V X5R 603

CRITICAL
J9450 SM-2MT-LF

NC

PP5V_INVERTER_SW
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V

C9452 0.001uF 20% 50V CERM 402

INVERTER_PWM

GND_INVERTER
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V

L9454 400-OHM-EMI SM-1

C9454 0.001uF 20% 50V CERM 402

C9455 0.001uF 20% 50V CERM 402

L9455 FERR-250-OHM SM

6 =GND_CHASSIS_INVERTER

INVERTER EXPECTS ACTIVE HIGH PWM SIGNAL

LCD_CTL_SMC
R9490 0 5% 1/16W MF-LF 402

46 SMC_BKLIGHT_ENABLE

LCD_CTL_GPU
R9491 0 5% 1/16W MF-LF 402

69 GPU_BLON

GPU_OR_SMC_BL_EN

Q9450 FDG6324L SC70-6-LF

R9489 10K 5% 1/16W MF-LF 402

62 =PP3V3_S0_INVERTER

INVERTER_BUF

U9453 MC74VHC1G08 SC70

LCD_CTL_SMC
R9492 0 5% 1/16W MF-LF 402

46 SMC_DISP_BKLT_A

GPU_OR_SMC_BL_PWM

INVERTER_PWM_F

INVERTER_BUF
C9453 0.1uF 20% 10V CERM 402

LCD_CTL_GPU
R9493 0 5% 1/16W MF-LF 402

72 GPU_VARY_BL

INVERTER_UNBUF
R9496 0 5% 1/16W MF-LF 402

Internal Display Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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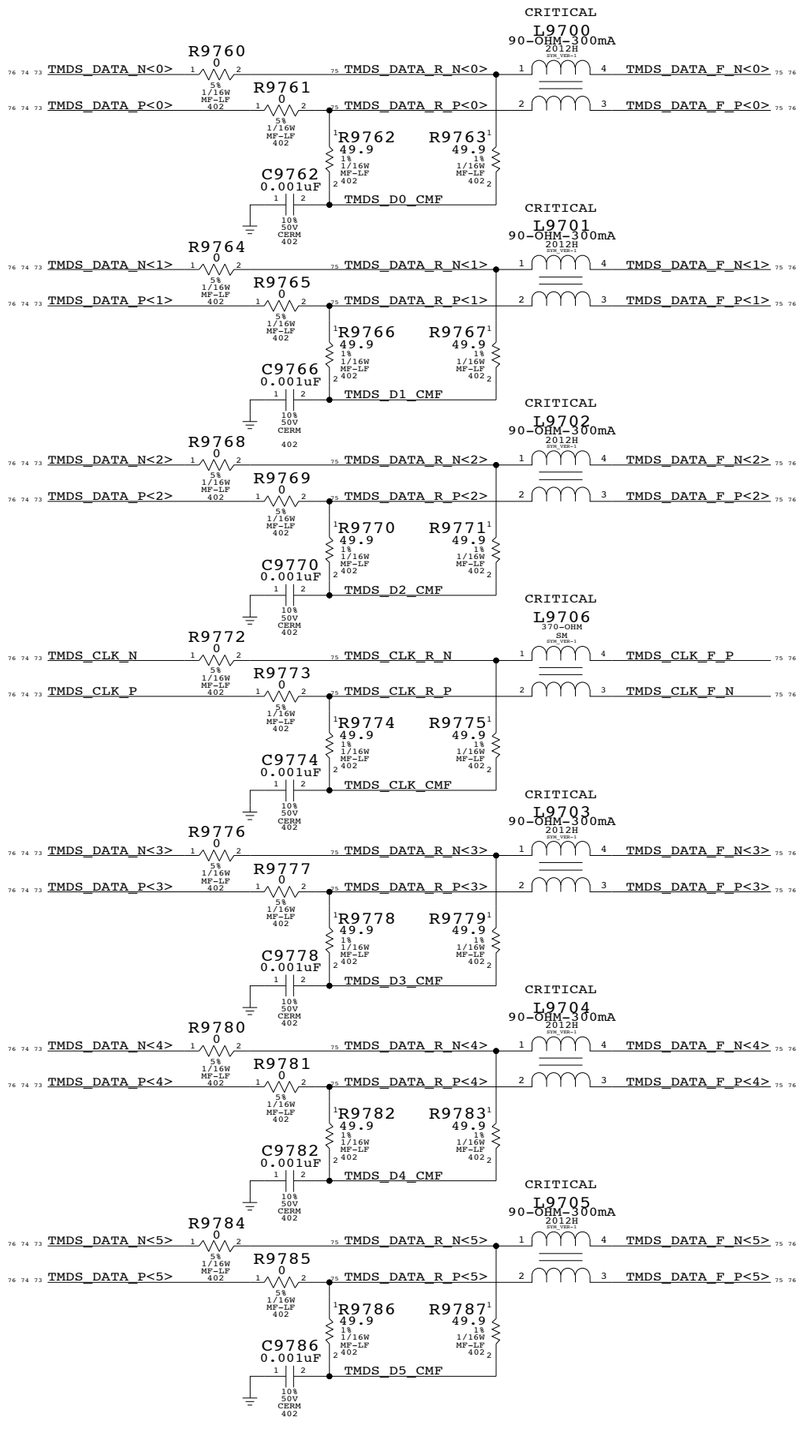
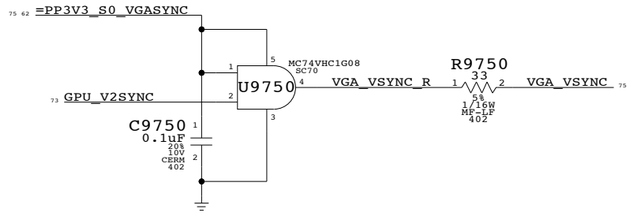
TMDS Filtering

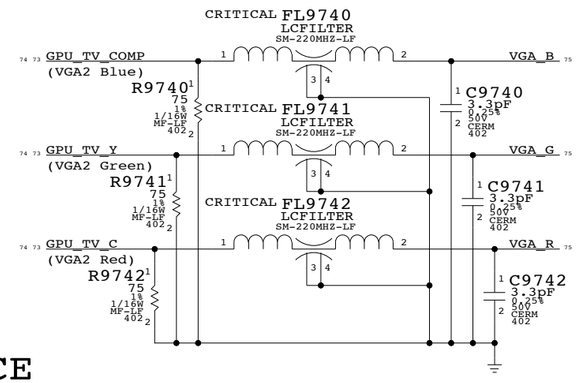
Place series R's close to GPU, other parts near connector.



VGA SYNC BUFFERS

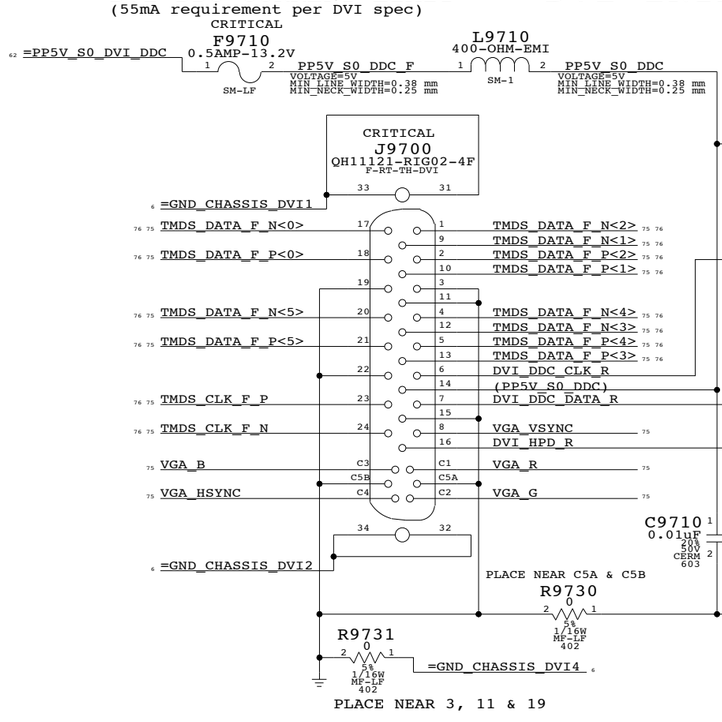


ANALOG FILTERING
PLACE CLOSE TO CONNECTOR

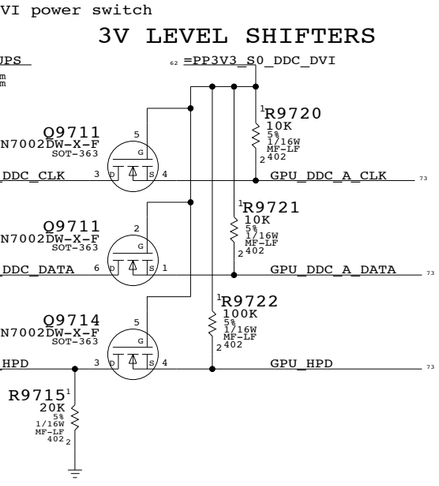


DVI INTERFACE

DVI DDC CURRENT LIMIT
(55mA requirement per DVI spec)



3V LEVEL SHIFTERS



NET_TYPE		
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL
	TMDS	TMDS_CLK_R_P
	TMDS	TMDS_CLK_R_N
	TMDS	TMDS_DATA_R_P<5..0>
	TMDS	TMDS_DATA_R_N<5..0>
	TMDSCONN	TMDS_CLK_F_P
	TMDSCONN	TMDS_CLK_F_N
	TMDSCONN	TMDS_DATA_F_P<5..0>
	TMDSCONN	TMDS_DATA_F_N<5..0>

External Display Connector

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ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
	FSB_55S	FSB_COMMON	FSB_ADS_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_BNR_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_BPRI_L	7 12
	FSB_55S	FSB_COMMON	FSB_BREQ0_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_DBSY_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_DEFER_L	7 12
	FSB_55S	FSB_COMMON	FSB_DPWR_L	7 12
	FSB_55S	FSB_COMMON	FSB_DRDY_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_HIT_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_HITM_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_LOCK_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_RS_L<2..0>	7 12
	FSB_55S	FSB_COMMON	FSB_TRDY_L	7 12
	FSB_55S	FSB_COMMON	FSB_CPURST_L	7 11 12 47
	FSB_55S	FSB_DATA	FSB_D_L<63..0>	5 7 12
	FSB_55S	FSB_DATA	FSB_DINV_L<3..0>	5 7 12
	FSB_55S	FSB_DSTB	FSB_DSTBP_L<3..0>	5 7 12
	FSB_55S	FSB_DSTB	FSB_DSTBN_L<3..0>	5 7 12
	FSB_55S	FSB_ADDR	FSB_A_L<31..3>	5 7 12
	FSB_55S	FSB_ADDR	FSB_REQ_L<4..0>	5 7 12
	FSB_55S	FSB_ADSTB	FSB_ADSTB_L<3..0>	5 7 12
	CPU_55S		FSB_IERR_L	7
	CPU_55S		FSB_FERR_L	
	CPU_55S		CPU_PWRGD	7 21
	CPU_55S		CPU_INTR	7 21
	CPU_55S		CPU_NMI	7 21
	CPU_55S		CPU_A20M_L	7 21
	CPU_55S		CPU_DPSLP_L	7 21
	CPU_55S		CPU_IGNNE_L	7 21
	CPU_55S		CPU_INIT_L	7 21
	CPU_55S		CPU_SMI_L	7 21
	CPU_55S		CPU_STPCLK_L	7 21
	CPU_55S	CPU_2TO1	CPU_THERMTRIP_L	
	CPU_55S	CPU_2TO1	PM_DPRSLPVR	14 23 56
	CPU_55S	CPU_2TO1	IMVP_DPRSLPVR	56
	CPU_55S	CPU_GTLREF	CPU_GTLREF	7
	CPU_55S	CPU_COMP	CPU_COMP<3>	7
	CPU_27P4S	CPU_COMP	CPU_COMP<2>	7
	CPU_55S	CPU_COMP	CPU_COMP<1>	7
	CPU_27P4S	CPU_COMP	CPU_COMP<0>	7
	CPU_55S	CPU_ITP	XDP_BPM_L<5..0>	7 11
	CLK_FSB_100D	CPU_ITP	CPU_XDP_CLK_P	11 34
	CLK_FSB_100D	CPU_ITP	CPU_XDP_CLK_N	11 34
	CPU_55S	CPU_ITP	ITPRESET_L	11
	CPU_55S	CPU_2TO1	CPU_VID<6..0>	8 9 76
	CPU_55S	CPU_2TO1	CPU_VID<6..0>	8 9 76
	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	8 56
	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	8 56
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	56
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	56

	MEM_CLK	MEM_70D
	MEM_CTRL	MEM_45S
	MEM_CMD	MEM_55S
	MEM_DATA	MEM_55S
	MEM_DQS	MEM_85D
	FB_CLK	FB_75D
	FB_ADCTRL	FB_35S_TO_55S
	FB_ADCTRL	FB_55S
	FB_DATA	FB_40S
	LVDS	LVDS_100D
	TMDS	TMDS_100D
	VGA	VGA_75S
	PCIE	PCIE_100D
	DMI	DMI_100D
	SATA	SATA_100D
	IDE	IDE_55S
	USB2	USB2_90D
	ENET	ENET_100D
	FW	FW_110D
	SMB	SMB_55S
	SPI	SPI_55S
	CLK_FSB	CLK_FSB_100D
	CLK_PCIE	CLK_PCIE_100D
	CLK_MED	CLK_MED_55S
	CLK_SLOW	CLK_SLOW_55S

	AUDIO_55S	AUDIO	SB_ACZ_BITCLK	21
	AUDIO_55S	AUDIO	ACZ_BITCLK	5 21 44
	AUDIO_55S	AUDIO	SB_ACZ_SYNC	21
	AUDIO_55S	AUDIO	ACZ_SYNC	5 21 44
	AUDIO_55S	AUDIO	SB_ACZ_RST_L	21
	AUDIO_55S	AUDIO	ACZ_RST_L	5 21 44
	AUDIO_55S	AUDIO	ACZ_SDATAIN<0>	5 21 44
	AUDIO_55S	AUDIO	SB_ACZ_SDATAOUT	21
	AUDIO_55S	AUDIO	ACZ_SDATAOUT	5 21 44

	TMDS	TMDS	TMDS_CLK_P	73 74 75
	TMDS	TMDS	TMDS_CLK_N	73 74 75
	TMDS	TMDS	TMDS_DATA_P<5..3>	73 74 75
	TMDS	TMDS	TMDS_DATA_N<5..3>	73 74 75
D0	TMDS	TMDS	TMDS_DATA_P<2..0>	73 74 75
D1	TMDS	TMDS	TMDS_DATA_N<2..0>	73 74 75
	TMDSCONN	TMDSCONN	TMDS_CLK_F_P	75
	TMDSCONN	TMDSCONN	TMDS_CLK_F_N	75
	TMDSCONN	TMDSCONN	TMDS_DATA_F_P<5..3>	75
	TMDSCONN	TMDSCONN	TMDS_DATA_F_N<5..3>	75
D2	TMDSCONN	TMDSCONN	TMDS_DATA_F_P<2..0>	75
D3	TMDSCONN	TMDSCONN	TMDS_DATA_F_N<2..0>	75

M1 Net Properties

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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