1. All resistance values are in ohms, 0.1 watt +/- 5%.
2. All capacitance values are in microfarads.
3. All crystals & oscillator values are in hertz.

<table>
<thead>
<tr>
<th>PDF CSA CONTENTS</th>
<th>CONTENTS</th>
<th>SYNC MASTER</th>
<th>DATE</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. All crystals &amp; oscillator values are in hertz.</td>
<td>2. All capacitance values are in microfarads.</td>
<td>3. All resistance values are in ohms, 0.1 watt +/- 5%.</td>
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### PROCESSORS

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<th>BOM OPTION</th>
<th>REF DES</th>
<th>COMMENTS</th>
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### ALTERNATES

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<tbody>
<tr>
<td></td>
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<td></td>
</tr>
</tbody>
</table>
NO TEST XW NETS

EE IDENTIFIED NO TEST NETS

FUNC TEST NETS
NOTES FROM TOM FUSSELMAN
PLACE TWO TEST POINTS ON TOP SIDE
FOR PPV3, ALL AND GND
PLACE WITHIN 1 INCH OF EACH OTHER
USE FAT TRACKS

TOP SIDE ONLY

FUNC TEST 1 OF 2

APPLE COMPUTER INC.

051-6790 E 6 154

www.vinhafix.vn
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Apple Computer Inc.

Scale
None

CPU heatsink mounting holes

Serial debug

Diag LED

PLL lock LED

Cpu heatsink mounting holes

Signal Alias

www.vinafix.vn
NOTE:
SET OUTPUT=2.5V
VIN=5VDC VREF=1.24VDC
VO=VREF*(R1581+R1582)+1=5.505VDC
POWER BUDGET CURRENT OF TOTAL RAILS 0.2A PEAK
0.1A CONTINUOUS

PEAK CURRENT 0.1A

PP2V5_RUN FET SWITCH

PP5V_ALL

PP2V5_PWRON FET SWITCH

NOSTUFF OPTION TO DELAY 2.5V PWRON TO COME UP WITH 3.3V PWRON
To keep Vesta from being held in reset when system is off

RESET ASSERT REQUIREMENT IS 20MS TO 100MS

POWER ALIASES REQUIRED BY THIS PAGE:

VOLTAGE=1.2V
MIN_NECK_WIDTH=0.25 MM
MIN_LINE_WIDTH=0.50 MM
MAKE_BASE=TRUE

SIGNAL ALIASES REQUIRED BY THIS PAGE:

SYNC_DATE=06/20/2005
SYNC_MASTER=FINO-DC

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5. TO NOTIFY APPROPRIATE PERSONNEL OF THEIR OBLIGATIONS

APPLE COMPUTER INC.

REV. E051-6790

APPLE COMPUTER INC.
For PCI_AD<63..32>

DIGITAL  - 1.2V - 950 mA (1175 mW)

Shasta max (est 06/30/03) current:

I/O 2.5  - 2.5V -  20 mA (  60 mW)
ANALOG12 - 1.2V - 600 mA ( 760 mW)
Total:                    3015 mW
I/O 3.3  - 3.3V - 220 mA ( 770 mW)
VDDPs    - 2.5V - 100 mA ( 250 mW)
N/C ALIASES

N/C RAINIER CLOCKS

N/C CPUB CLOCKS

N/C QUASAR CLOCKS

CLOCK CONSTRAINTS

NOTE:
ALL OTHER CLOCK CONSTRAINTS ON THEIR RESPECTIVE BUS PAGES
SMU ALIASES

ALIASES ARE ONLY RELEVANT WHEN THE ZIFS DIFFER FROM Q3.

CURRENT ONLY IF Q3 DIFFERS FROM Q4.

NOTE SMU ALIASES

M23/M33 USES FAN_RPM0 (P7.3), FAN_RPM1 (P7.5), FAN_RPM2 (P7.7) ONLY.
Q63 USES SMU_SER_SEL FOR SPDIF-SMU-DEBUG. NOT M23/M33 FEATURE.
M23/M33 USES TACH0 (P2.2), TACH1 (P2.3), TACH2 (P2.4) ONLY.
SELECT BETWEEN CPU OR NB TMS AND TDO FROM/TO SMU
M23/M33 DOESN'T HAVE FAN TACHS P2.5, P2.6, P2.7.
CONSIDER DOOR_AJAR FOR M23/M33 DIMM ACCESS DOOR?
CPU_VID_LE1 FOR Q82. NOT M23/M33 FEATURE.
CPU_VID_LE0 FOR Q82. NOT M23/M33 FEATURE.
M23/M33 DOESN'T USE P1.4. NC ON PG 7.
M23/M33 DOESN'T USE. P1.0 NC ON PG 7.
M23/M33 DOESN'T HAVE THIS FAN.
M23/M33 DOESN'T HAVE THOSE FANS.
Q63 NC'S THESE AS IT USES A SAT.
M23/M33 HAS NO SLOTS.
FROM CPU PROCESSOR TEMP SENSE (TDiode Excitation Circuit and Opamp)

PROCESSOR VCORE VOLTAGE SENSE

2.5V PRECISION VOLTAGE REFERENCE SOURCE

PROCESSOR VCORE CURRENT SENSE

DIFFERENTIAL PAIR = CORE_ISNS

DIFFERENTIAL PAIR = KPGND2_FMAX

DIFFERENTIAL PAIR = KP2_FMAX

DIFFERENTIAL PAIR = FMAXT_M

DIFFERENTIAL PAIR = P_FMAXT

DIFFERENTIAL PAIR = KP_V<1>

DIFFERENTIAL PAIR = KP_V<2>

DEVELOPMENT COUNT

DEVELOPMENT

TH-VERT-LF

L5570

U5570

CRITICAL

MC-LF

1W

1%

AVDDVC_NOISE 0.25 MM

GND_SMU_AVSS

TO SMU ADC SAMPLING

TO ASSIST DIODECAL

TDIODE CIRCUIT ALWAYS POWERED

VOLTAGE = 12V

PP12V_CPU_R_L

PP3V3_RUN_CPU

PP3V3_PWRON_CPU = PP3V3_ALL_CPU

MC-LF

1W

1%

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www.vinafix.vn
Q63: SEE P.28 FOR MORE DECOUPLING CAPS FOR THESE PINS.
**KODIAK PCI-E PHYSICAL CONSTRAINT TABLE**

<table>
<thead>
<tr>
<th>COL_NAME</th>
<th>ELECTRICAL_CONSTRAINT_SET</th>
<th>DIFFERENTIAL_PAIR</th>
<th>NET_PHYSICAL_TYPE</th>
<th>NET_DIRECTION_TYPE</th>
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**KODIAK PCI-E POWER PHYSICAL CONSTRAINT TABLE**

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</table>

**KODIAK PCI-E CONST**

Apple Computer Inc.

051-6790

12345678

E051-6790
NOTE: This USB2 implementation supports AD27 (Slot "G") - USB2 (0x1033/0x0035)

PCI Devices implemented on this page:

BOM options provided by this page:

Signal aliases required by this page:

Power aliases required by this page:

Page Notes

fails_Signal Alias: AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7 AD8 AD9 AD10 AD11 AD12 AD13 AD14 AD15 AD16 AD17 AD18 AD19 AD20 AD21 AD22 AD23 AD24 AD25 AD26 AD27 AD28 AD29 AD30 AD31

fails_Power Alias: PP_VIOPCIUSB2_C2

ALL NETS TO FUNCTIONAL TEST PAGE

PP_VIOPCIUSB2_C2
<table>
<thead>
<tr>
<th>Signal aliases required by this page:</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power aliases required by this page:</td>
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</tbody>
</table>

**Page Notes**

- **Page Notes**
  - Textual notes or comments may be present here.
  - Diagram annotations or symbols may be included.

**UATA_NETSPA**
- **UATA_RESET_L**
- **UATA_DMACK_L_R**
- **UATA_CS0_L_R**
- **UATA_DA_R<2..0>**
- **UATA_DD_R<6..0>**
- **UATA_INTRQ**
- **UATA_DMARQ**
- **UATA_DA<2..0>**
- **UATA_CS1_L**
- **UATA_DD<6..0>**
- **UATA_DD<15..8>**

**SATA_RXD_N2_CSATA**
- **SATA_RXD2_CSATA**
- **SATA_RXD_N1_CSATA**
- **SATA_RXD1_CSATA**

**PP_1V2PWRONDISKSB_CC**
- **SM**
- **6**

**Additional Notes**

- **Secondary Length**: 12.70mm
- **Primary Max Sep**: 0.23mm inner, 0.25mm outer
- **Length Tolerance**: 1.27mm
- **Signal aliases required by this page**
- **Power aliases required by this page**

**AC coupling required for any SATA pair used**

- **Recommend 0.1uF cap placed close to Shasta.**

**Scale**

- **Shasta Disk**
- **DRAWING NUMBER**
- **SCALE**

**APPLE COMPUTER INC.**

**Page:** 2

**Date:** 051-6790 E

**Sheet:** A

**Revision:** 127 154

---

**DIOR- :HDMARDY- :HSTROBE > SPARE 1/16W**

**MMF-LF**
- **10K**

**RPC703**
- **RPC702**
- **RPC701**

**SM-LF**
- **1/16W**

**ASSY**

- **MC-LF**
- **33**
- **5%**

**SCALE**

- **D**
- **OFSHT**

**Other notices or details may be included here.**

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**Additional diagrams or sections may be present.**

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---

**A**

**B**

**C**

**D**

**E**

---

**www.vinafix.vn**
4-11-05: BOARD FILE HAS PHYSICAL/SPACING NAME ASSIGNMENT ALREADY FOR SATA DIFF PAIRS (CAP TO SHASTA),
BUT NOT FOR THE SATA CAP TO CONNECTOR ROUTES, WHICH THE ABOVE ARE ADDED FOR THIS PURPOSE.
UATA TRACE IMPEDANCE ROUTE TO 50 OHMS

4-8-05
NOTED FOR SHADDED PAGE 127
FOR M23/M33 CREATE A NICE SHAPE
FOR FFV2, SATA_VOLT AND THEN NECK DOWN
TO THE DEFAULT VALUE WHEN NEEDED.
THE WIDTH/NECK PROPERTIES ON PAGE 127
ARE SET BY Q63 FOR SCHEMATIC SHARING.

LC500 CHANGED TO 15512240 (660 OHM, 0.2 OHM DCR, 1A)
PREVIOUS ONE WAS 15500011 (660 OHM, 0.6 OHM DCR, 0.2A)
PARK TONIN AMERICA PN: 520122401.

4-11-05
FFV2, ALL REG. IS SET TO BE 1.22V TO 1.23V
AS NOTED ON THE 1.2 REG PAGE 13. THIS WILL
HELP MITIGATE THE LOSS ACROSS THE Q1306 FET
Q1332V1.

4-10-05
UPDATE AC COUPLING CAPS FOR SATA JC900.
ADDED DECOUPLING CAPS FOR JC901 PP5V_PATA NET.

4-12-05:
ADDED DECOUPLING CAPS FOR JC901 PP5V_PATA NET.
HELP MITIGATE THE LOSS ACROSS THE Q1306 FET
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PARK TONIN AMERICA PN: 520122401.
EXTRA CONSTRAINTS TO SUPPLEMENT THE MISSING NET PHYSICAL FROM EARLIER PAGE

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<td>0.1UF</td>
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<td>CD606</td>
<td>4.7UF</td>
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<tr>
<td>CD605</td>
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</tr>
<tr>
<td>CD600</td>
<td>4.7UF</td>
<td>2</td>
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PLUG THESE PARTS NEAR VESTA

SPARE GND VIAS FOR LAYER TRAVERSALS DURING ROUTING

ENET TERMINATION

ETHERNET CONNECTOR

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APPEND COMPUTER INC.

DRAWING NUMBER 136 154

SCALE SIZE

051-6790 E

DATE 06/20/2005

DIODES

GREEN-3.6MCD

LED8701_P

LED8700_P

REV. C

D

ETHERNET CONNECTOR

PRELIMINARY

www.vinafix.vn
IT IS 2.2V INSTEAD OF 2.7V BECAUSE THE SNAPBACK ESD DIODES HAVE A .5V DROP

MIN_LINE_WIDTH=0.38 mm
MIN_LINE_WIDTH=0.8MM
MIN_NECK_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25MM
VOLTAGE=1.86V
VOLTAGE=24V
VOLTAGE=0V
VOLTAGE=24V
VOLTAGE=3.3V
VOLTAGE=6.3V
VOLTAGE=1.5AMP-33V
VOLTAGE=0.75AMP-13.2V
VOLTAGE=20% 603-1 0.01uF

“Snapback” & “Late VG” Protection

“Snapback” & “Late VG” Protection

CON, 1394A 7 DEGREES 20_INCH_LCD 514-0251 JE000 CRITICAL 1
CRITICAL BOM OPTION

NO_TEST=YES
NO_TEST=YES
NO_TEST=YES

TERMINATION

ESD Rail

Termination
Place close to Firewire PHY

Spare GND VIAS FOR LAYER TRAVERSALS DURING ROUTING

Termination
Place close to Firewire PHY

Termination
Place close to Firewire PHY

SPARE GND VIAS FOR LAYER TRAVERSALS DURING ROUTING