1. All resistance values are in ohms; 0.1 watt or less.
2. All capacitance values are in microfarads.
3. All crystals & oscillator values are in hertz.
### Table Items

<table>
<thead>
<tr>
<th>Component</th>
<th>Description</th>
<th>Note</th>
<th>Quantity</th>
<th>Reference Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>C6505</td>
<td>CHOKE, COMMON MODE</td>
<td>120UF, 16V, 20%</td>
<td>1</td>
<td>124-0338, 124-0333</td>
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<tr>
<td>C7953, C7954</td>
<td>FOR SUPPLY</td>
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<tr>
<td>C6251</td>
<td>FACTORY SHORTAGE</td>
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### Preliminary Notes

- **Table Items**
- **CRITICAL BOM OPTION**
- **NOTICE OF PROPRIETARY PROPERTY**
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**Diagram**

1. **COMMON**
2. **ALTERNATE PARTS**
3. **MECHANICAL PARTS**
4. **OPS REQUESTED QUAL PARTS**

---

**Credits**

- **APPLE COMPUTER INC.**
- **D 051-7199 A**
- **www.vinafix.vn**
CPU ITP700FLEX DEBUG SUPPORT

ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU's TCK PIN AND THEN FUSE BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX CONNECTOR'S PROG PIN.
B

A

rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.

CRT Disable

TV-Out Disable

connect to GND through 75-ohm resistors.

Unused DAC outputs must remain powered, but can omit

Component: DACA, DACB & DACC

Composite: DACA only

Otherwise, tie VCCD_LVDS to GND also.

VCCD_LVDS must remain powered with proper decoupling.

LVDS Disable

Preliminary
These connections can break without affecting part performance.

OMIT

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www.vinafix.vn
DDR2 Vtt Regulator

Memory Vtt Supply

- =PP5V_S0_MEMVTT
- =PP1V8_S0_MEMVTT
- =PP0V9_S0_MEMVTT_LDO

MEMVTT_EN can be used to disable MEMVTT in sleep.

If power inputs are not S0, MEMVTT_VREF can be used instead of MEMVTT_EN.

BOM options provided by this page:

- C3101: 10UF 20% 6.3V
- U3100: MSOP-8 BD3533FVM
- R3100: 1K 1/16W MF-LF
- C3105: 150UF 2.2UF 10% CERM1
- C3102: 10UF 20% 6.3V
- R3101: 221 1% 1/16W MF-LF
- C3109: 0.1UF 10V CERM
- C3110: 1uF 10% 6.3V
- C3100: 1uF 10% 6.3V

www.vinafix.vn
NOTE: USE THESE PULL-DOWNS IF NOT CONNECTED TO GPIO's

667MHZ (133MHZ CPU CLK)

FSB FREQUENCY SELECT:

1/16W MF-LF 402

R3462
R3458
R3455
R3453

5%

R3461
R3452
R3452
R3452

1K

R3457
R3463
R3459
R3454
R3457
R3452
R3452
R3452

1/16W MF-LF

402

1/16W MF-LF

5%

402MF-LF 1/16W 5%
Termination
Place close to FireWire PWR

3rd TPA/TPB pair unused
-PW C TER+ - TP PW - C TP+ 5.4
-PW C TER+ - TP PW - C TP+ 5.4
-PW C TER+ - TP PW - C TP+ 5.4
-PW C TER+ - TP PW - C TP+ 5.4

ESD Rail

"Snapback" & "Late VC" Protection

Related Notes:
- Current through the bias resistors should be 5mA for a voltage drop to 2.2V instead of 2.7V because the snapback rail drops only 0.5V drop.
- The bias resistor should be 50V, 1% tolerance.

Additional Notes:
- TP_FW_C_TPB_N = TP_FW_C_TPB_P = MAKE_BASE = TRUE
- R4651 = 56.2 Ohm, 1/16W, 1% tolerance
- C4612 = 0.01uF, X7R, 50V, 20%
- C4616 = 0.01uF, X7R, 50V, 20%
- DP4610, DP4611, DP4620, DP4621 = 0.01uF, X7R, 50V, 5%
- C4620, C4621, C4622, C4623 = 0.001uF, 50V, 10%
- R4652, R4653, R4654, R4662 = 4.99K Ohm, 5%
- C4613 = 0.001uF, X7R, 50V, 20%

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R6306-07 SHOULD BE PLACED LESS THAN 2.54MM FROM U6301
R6303 SHOULD BE PLACED LESS THAN 2.54MM FROM U6301
4.5V POWER SUPPLY FOR CODEC AND LINE IN AMP
APN: 353S1233