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- 1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
- 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
- 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

IMAC 5,2 -- REV A

7/25/06

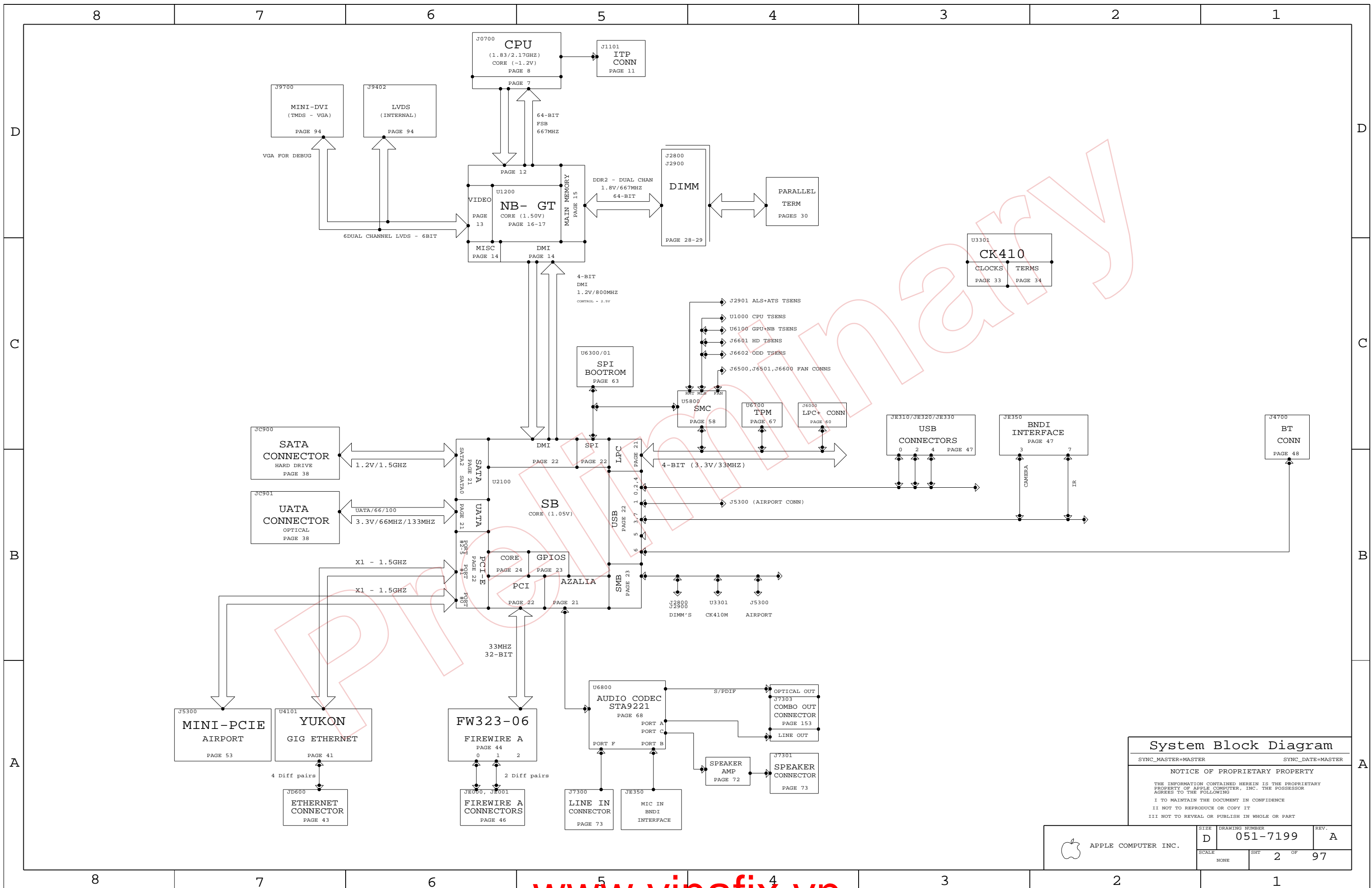
REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD	ENG APPD
A		451207	PRODUCTION RELEASED		
				DATE	DATE
				07/26/06	06/22/04

PDF	CSA	CONTENTS	SYNC	MASTER	DATE
2	2	System Block Diagram	MASTER	MASTER	
3	3	Power Block Diagram	MASTER	MASTER	
4	4	Table Items	MASTER	MASTER	
5	5	FUNC TEST 1 OF 2	MASTER	MASTER	
6	6	Power Conn / Alias	MASTER	MASTER	
7	7	CPU 1 OF 2-FSB	MASTER	MASTER	
8	8	CPU 2 OF 2-PWR/GND	MASTER	MASTER	
9	9	CPU DECAPS & VID<>	MASTER	MASTER	
10	10	CPU TEMP SENSOR	MASTER	MASTER	
11	11	CPU ITP700FLEX DEBUG	M38	01/05/2006	
12	12	NB CPU Interface	M1	01/05/2006	
13	13	NB PEG / Video Interfaces	M1	01/05/2006	
14	14	NB Misc Interfaces	MASTER	MASTER	
15	15	NB DDR2 Interfaces	M1	01/05/2006	
16	16	NB Power 1	MASTER	MASTER	
17	17	NB Power 2	M40	01/05/2006	
18	18	NB Grounds	M1	01/05/2006	
19	19	NB (GM) Decoupling	(MASTER)	(MASTER)	
20	20	NB Config Straps	M1	01/05/2006	
21	21	SB: 1 OF 4	M38	01/05/2006	
22	22	SB: 2 OF 4	MASTER	MASTER	
23	23	SB: 3 OF 4	MASTER	MASTER	
24	24	SB: 4 OF 4	M38	01/05/2006	
25	25	SB: DECOUPLING	MASTER	MASTER	
26	26	SB: MISC	MASTER	MASTER	
27	27	SB: SMB HUB AND ALIAS	MASTER	MASTER	
28	28	DDR2 SO-DIMM Connector	AMASTER	MASTER	
29	29	DDR2 SO-DIMM Connector	BMASTER	MASTER	
30	30	Memory Active Termination	MASTER	MASTER	
31	31	Memory Vtt Supply	MASTER	MASTER	
32	33	CLOCKS	MASTER	MASTER	
33	34	CLOCKS: TERMINATIONS	MASTER	MASTER	
34	38	Disk Connectors	MASTER	MASTER	
35	41	ETHERNET CONTROLLER	MASTER	MASTER	
36	42	ETHERNET MISC	MASTER	MASTER	
37	43	ETHERNET CONNECTOR	MASTER	MASTER	

PDF	CSA	CONTENTS	SYNC	MASTER	DATE
38	44	FW: FW323-06	MASTER	MASTER	
39	45	FW: DECAPS	MASTER	MASTER	
40	46	FIREWIRE CONNECTORS	MASTER	MASTER	
41	47	USB Device Interfaces	MASTER	MASTER	
42	53	AIRPORT CONN	MASTER	MASTER	
43	54	PCIE PORT ALIASES	MASTER	MASTER	
44	58	SMC	M1	01/05/2006	
45	59	SMC & TPM SUPPORT	(MASTER)	(MASTER)	
46	60	LPC+ CONN	M38	12/09/2005	
47	61	NB THERMAL	MASTER	MASTER	
48	63	SPI BOOTROM	M38	01/05/2006	
49	65	Fan 0, 1 & System Temp	MASTER	MASTER	
50	66	Fan 2 & HD Temp	MASTER	MASTER	
51	67	TPM	M38	01/05/2006	
52	68	AUDIO: CODEC	AUDIO	05/12/2006	
53	72	AUDIO: SPEAKER AMP	AUDIO	05/12/2006	
54	73	AUDIO: CONNECTORS	AUDIO	05/12/2006	
55	74	AUDIO: POWER SUPPLIES	AUDIO	05/12/2006	
56	75	IMVP6 CPU VCore Regulator	MASTER	MASTER	
57	76	CPU & SYSTEM SENSE CIRCUM	(MASTER)	(MASTER)	
58	77	PWR GOOD	(MASTER)	(MASTER)	
59	78	3V DC/DC 2.5V	(MASTER)	(MASTER)	
60	79	1.8V & 1.2V VREG	MASTER	MASTER	
61	80	1.5V_S0 & 1.05V_S0 VREG	MASTER	MASTER	
62	82	5V DC/DC	MASTER	MASTER	
63	83	S0 AND S3 FETS	MASTER	MASTER	
64	94	Internal Display Conns	MASTER	MASTER	
65	95	EXTERNAL TMDS	MASTER	MASTER	
66	96	TMDS/Inverter/ExtVGA	MASTER	MASTER	
67	97	External Display Conns	MASTER	MASTER	



DIMENSIONS ARE IN MILLIMETERS		METRIC		Apple Computer Inc.	
XX :	_____	DRAPTER	/	DESIGN CK	/
X.XX :	_____	ENG APPD	/	MFG APPD	/
X.XXX :	_____	QA APPD	/	DESIGNER	/
ANGLES :	_____	RELEASE	/	SCALE	NONE
DO NOT SCALE DRAWING		MATERIAL/FINISH NOTED AS APPLICABLE		SIZE	D
 THIRD ANGLE PROJECTION		DRAWING NUMBER		051-7199	REV. A
				SHT 1 OF 97	




System Block Diagram

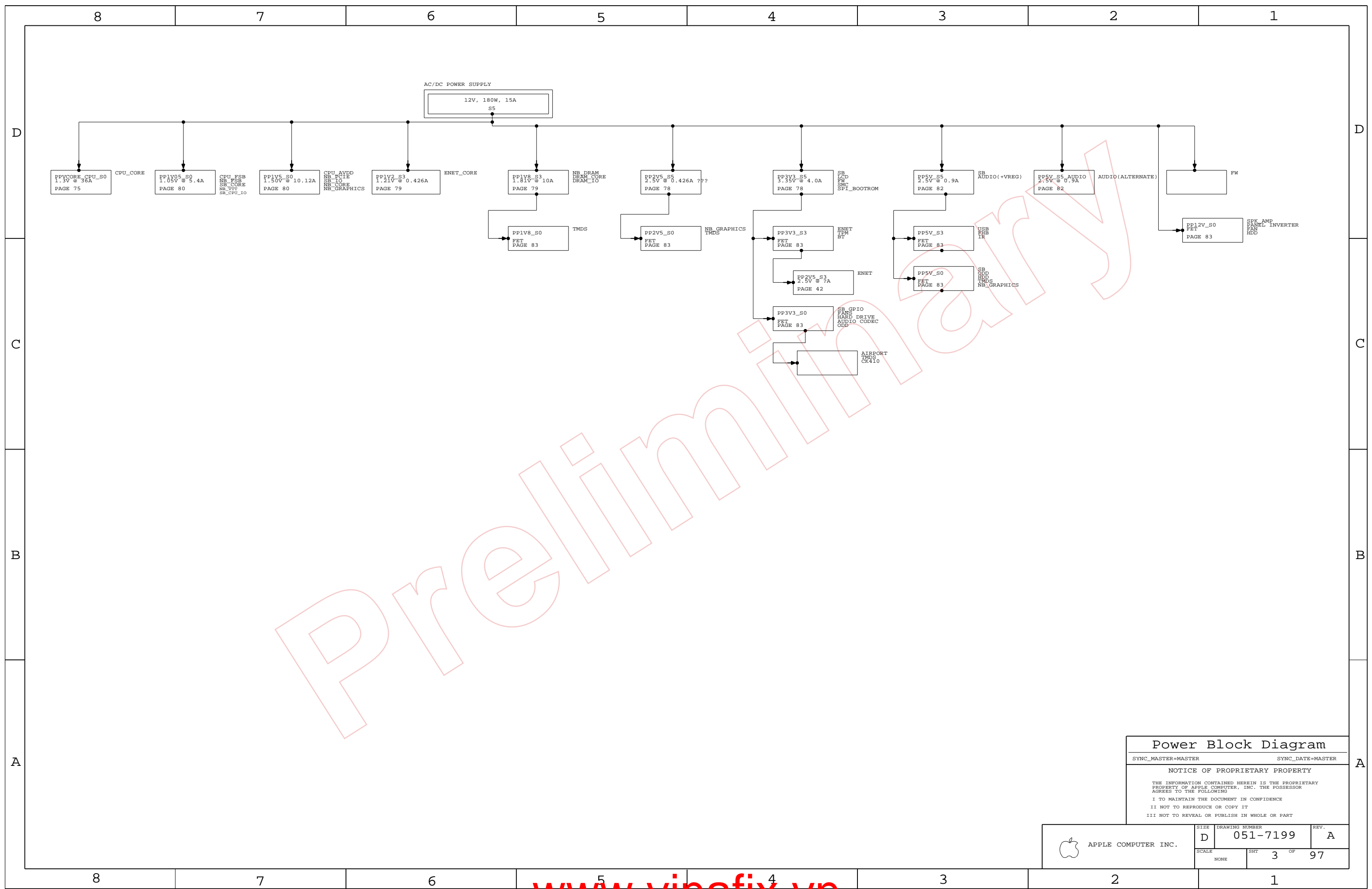
SYNC_MASTER=MASTER SYNC_DATE=MASTER

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	D	051-7199	A
SCALE	SHT	OF	REV.
NONE	2	97	



Power Block Diagram

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7199	REV. A
	SCALE NONE	SHEET 3 OF 97	

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COMMON

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
511S0025	1	IC,CPU-SKT,479BGA	J0700	CRITICAL	
338S0298	1	IC,945GT,NORTHBRIDGE	U1200	CRITICAL	
343S0385	1	IC,SB,652BGA	U2100	CRITICAL	
742-0048	1	BAT,COIN,3V,220MAH,CR2032	BT2600	CRITICAL	
359S0101	1	IC,CY28445-5,CLK GEN,68PIN QFN	U3301	CRITICAL	
338S0270	1	IC,88E8053,GIGABIT ENET XCVR,64P QFN,MD	U4101	CRITICAL	
(335S0382) 341S1797	1	IC,ENET LAN ROM	U4102	CRITICAL	
338S0279	1	IC,FW32306,1394A LINK,TQFP	U4400	CRITICAL	
338S0274 341T0022	1	IC,SMC,M50	U5800	CRITICAL	
341S1789	1	IC,TPM,TSSOP,28P	U6700	CRITICAL	TPM
353S1461	1	IC,CPU VREG,IMVP,TWO PHASE	U7500	CRITICAL	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-7199	1	PCB,SCHM,MLB,M50	SCH1		
820-1960	1	PCB,FAB,MLB,M50	MLB1		
(335S0384) 341T0042	1	EFI ROM,M50A	U6301	CRITICAL	
337S3386	1	M50 MEROM CPU	CPU	CRITICAL	MEROM

341S1859 IC EFI BOOTROM DEV M50
 337S3242 M38 CPU(C0)
 337S3280 M50 1.83G LOW SPEED CPU (D0)
 USE BOM OPTION MEROM FOR MEROM PROCESSOR

OPS REQUESTED QUAL PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
155S0295	1	CHOKE,COMMON_MODE,1650HM,4PIN	L9703	CRITICAL	
124-0359	3	PCAP,120UF,16V,20%,ELEC	C6505,C6504,C6602	CRITICAL	

ALTERNATE PARTS

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
126S0091	126S0092		C625	FACTORY SHORTAGE
353S1278	353S1381		U5940	SMC VREF
378S0141	378S0140		LX2601,LX2602,LX2603	
353S1465	353S1461		U7500	CPU VREG, OLD DIE, SCREENED PART
124-0338	124-0333		C7953,C7954	FOR SUPPLY

MECHANICAL PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
603-9187	1	SUBASSY, M50 NB HEATSINK	HS2	CRITICAL	
603-9186	1	SUBASSY, M50 CPU HEATSINK	HS1	CRITICAL	
725-0668	1	MYLAR WASHER	WASH1	CRITICAL	
725-0720	1	MYLAR BLACK LED CVR, M50	CVR1	CRITICAL	
825-6447	1	BARCODE LABEL, M50A	[EEE:WJ9]	CRITICAL	MEROM

Pre-Announcement

Table Items

SYNC_MASTER=MASTER SYNC_DATE=MASTER

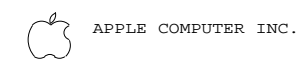
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SCALE	SHT	OF
NONE	4	97

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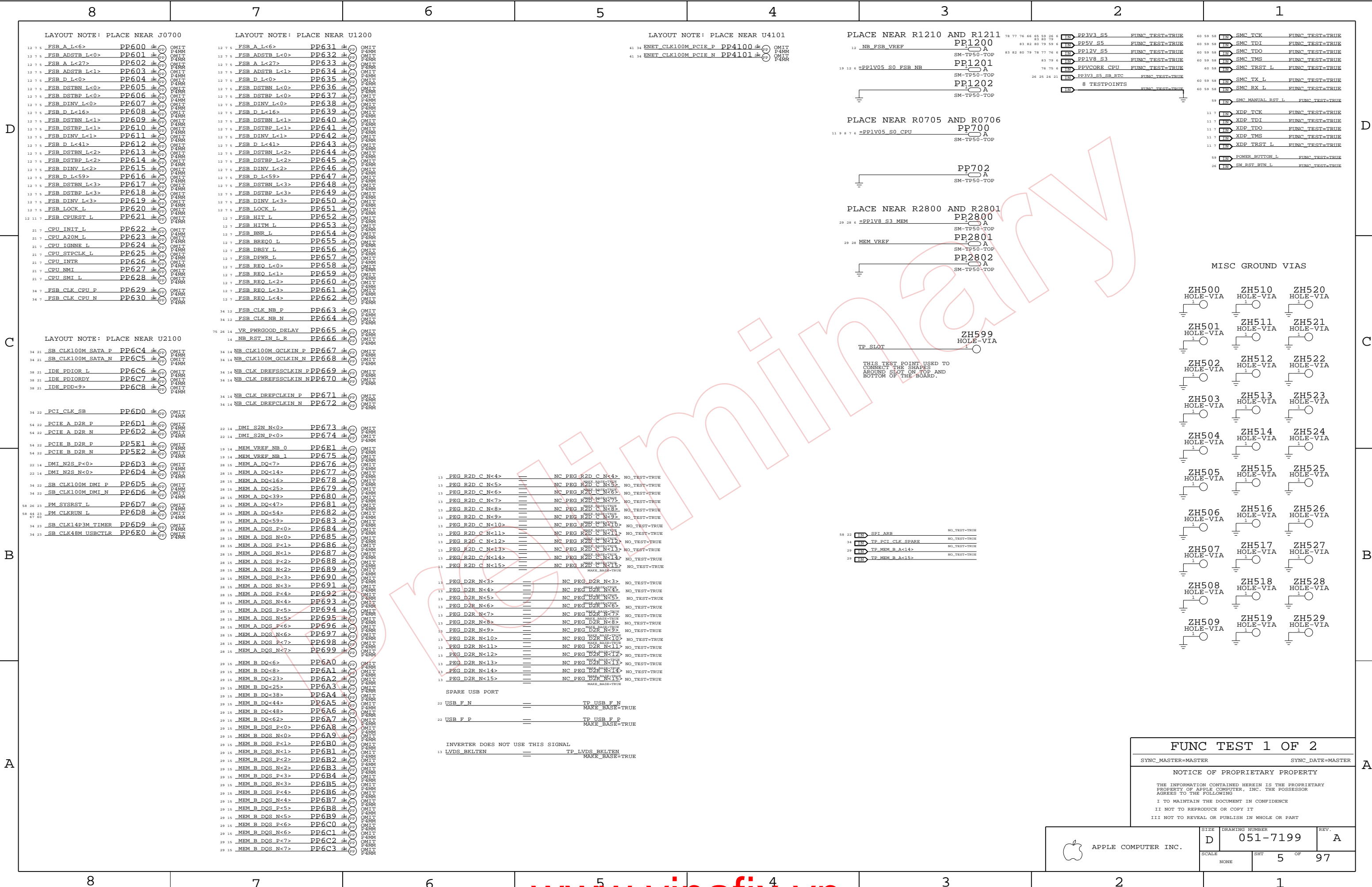
5

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LAYOUT NOTE: PLACE NEAR J0700

LAYOUT NOTE: PLACE NEAR U1200

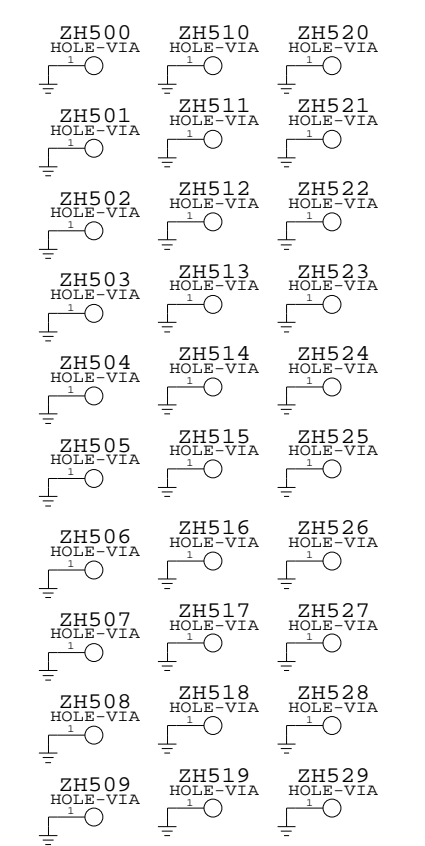
LAYOUT NOTE: PLACE NEAR U4101

PLACE NEAR R1210 AND R1211

PLACE NEAR R0705 AND R0706

PLACE NEAR R2800 AND R2801

MISC GROUND VIAS



THIS TEST POINT USED TO CONNECT THE SHAPES AROUND SLOT ON TOP AND BOTTOM OF THE BOARD.

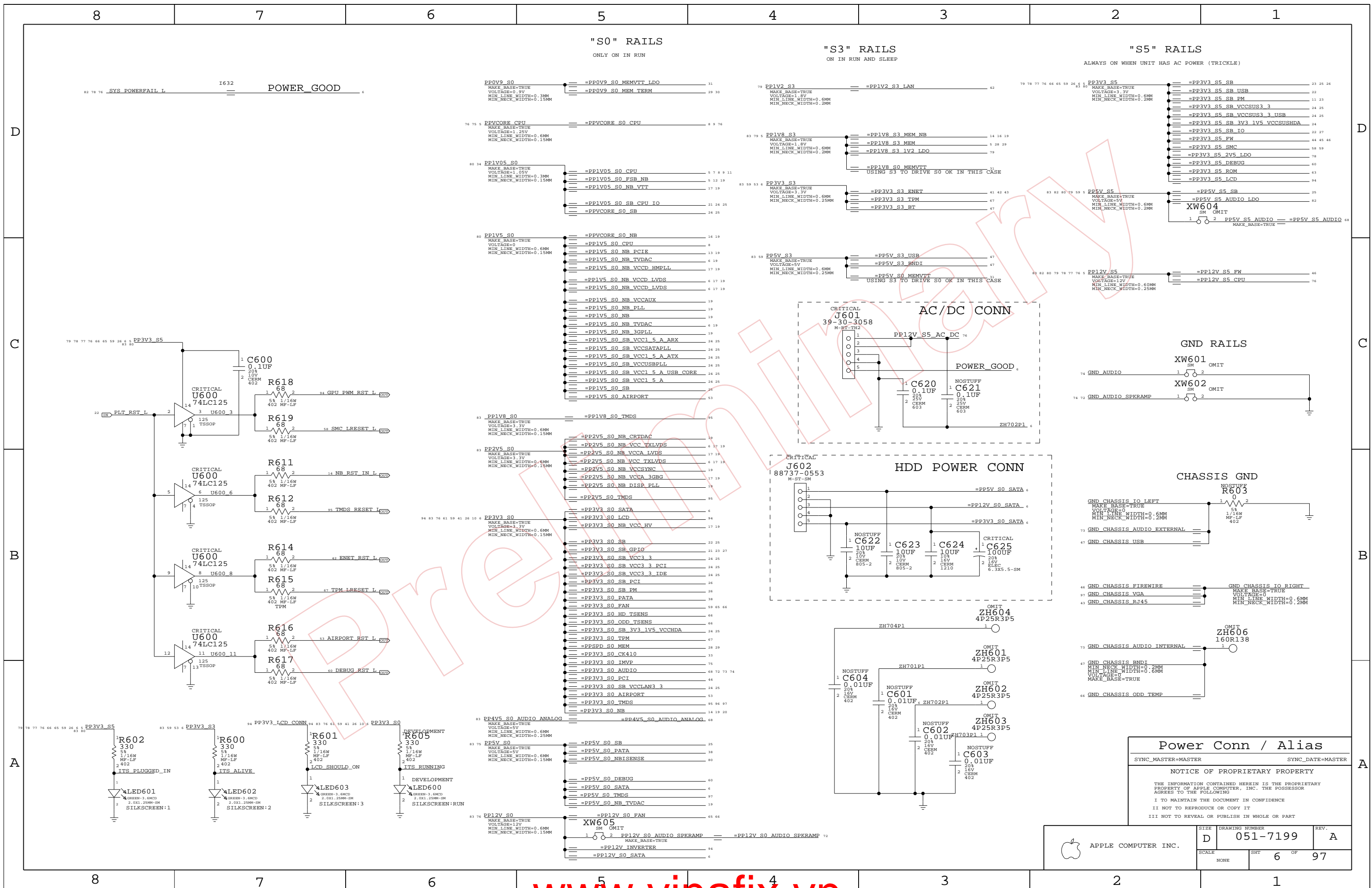
- 52 TP SPI_ARB NO_TEST=TRUE
34 TP PCI_CLK_SPARE NO_TEST=TRUE
28 TP MEM_B_A<14> NO_TEST=TRUE
28 TP MEM_B_A<15> NO_TEST=TRUE

- 33 PEG_R2D_C N<4> NC PEG_R2D_C N<4> NO_TEST=TRUE
33 PEG_R2D_C N<5> NC PEG_R2D_C N<5> NO_TEST=TRUE
33 PEG_R2D_C N<6> NC PEG_R2D_C N<6> NO_TEST=TRUE
33 PEG_R2D_C N<7> NC PEG_R2D_C N<7> NO_TEST=TRUE
33 PEG_R2D_C N<8> NC PEG_R2D_C N<8> NO_TEST=TRUE
33 PEG_R2D_C N<9> NC PEG_R2D_C N<9> NO_TEST=TRUE
33 PEG_R2D_C N<10> NC PEG_R2D_C N<10> NO_TEST=TRUE
33 PEG_R2D_C N<11> NC PEG_R2D_C N<11> NO_TEST=TRUE
33 PEG_R2D_C N<12> NC PEG_R2D_C N<12> NO_TEST=TRUE
33 PEG_R2D_C N<13> NC PEG_R2D_C N<13> NO_TEST=TRUE
33 PEG_R2D_C N<14> NC PEG_R2D_C N<14> NO_TEST=TRUE
33 PEG_R2D_C N<15> NC PEG_R2D_C N<15> NO_TEST=TRUE
33 PEG_D2R N<3> NC PEG_D2R N<3> NO_TEST=TRUE
33 PEG_D2R N<4> NC PEG_D2R N<4> NO_TEST=TRUE
33 PEG_D2R N<5> NC PEG_D2R N<5> NO_TEST=TRUE
33 PEG_D2R N<6> NC PEG_D2R N<6> NO_TEST=TRUE
33 PEG_D2R N<7> NC PEG_D2R N<7> NO_TEST=TRUE
33 PEG_D2R N<8> NC PEG_D2R N<8> NO_TEST=TRUE
33 PEG_D2R N<9> NC PEG_D2R N<9> NO_TEST=TRUE
33 PEG_D2R N<10> NC PEG_D2R N<10> NO_TEST=TRUE
33 PEG_D2R N<11> NC PEG_D2R N<11> NO_TEST=TRUE
33 PEG_D2R N<12> NC PEG_D2R N<12> NO_TEST=TRUE
33 PEG_D2R N<13> NC PEG_D2R N<13> NO_TEST=TRUE
33 PEG_D2R N<14> NC PEG_D2R N<14> NO_TEST=TRUE
33 PEG_D2R N<15> NC PEG_D2R N<15> NO_TEST=TRUE

- 22 USB_F_N TP USB_F_N MAKE_BASE=TRUE
22 USB_F_P TP USB_F_P MAKE_BASE=TRUE
33 LVDS_BKLTEN TP LVDS_BKLTEN MAKE_BASE=TRUE

FUNC TEST 1 OF 2
SYNC_MASTER=MASTER SYNC_DATE=MASTER
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Table with columns: SIZE (D), DRAWING NUMBER (051-7199), REV. (A), SCALE (NONE), SHEET (5 OF 97).



"S0" RAILS

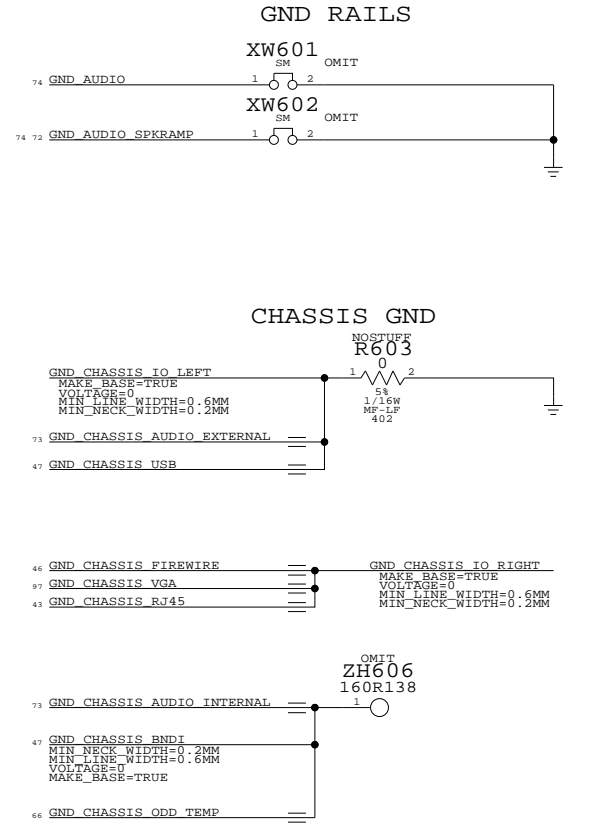
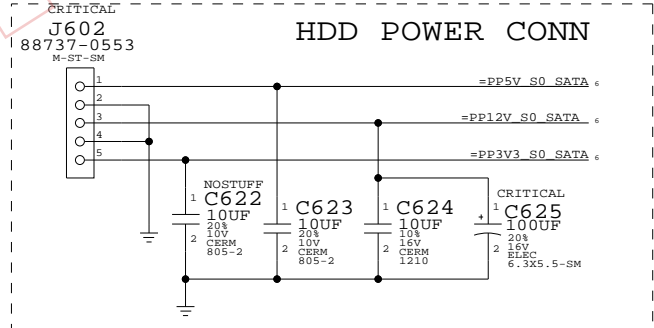
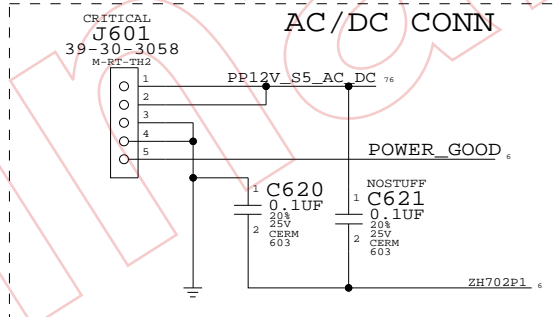
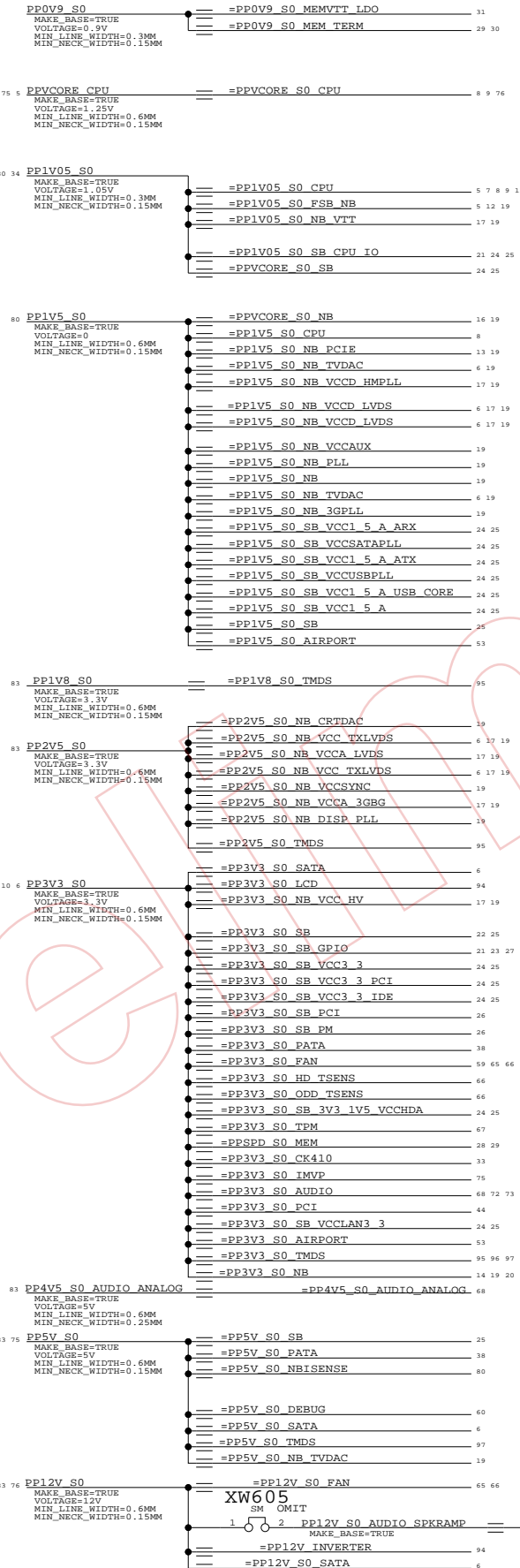
ONLY ON IN RUN

"S3" RAILS

ON IN RUN AND SLEEP

"S5" RAILS

ALWAYS ON WHEN UNIT HAS AC POWER (TRICKLE)



Power Conn / Alias

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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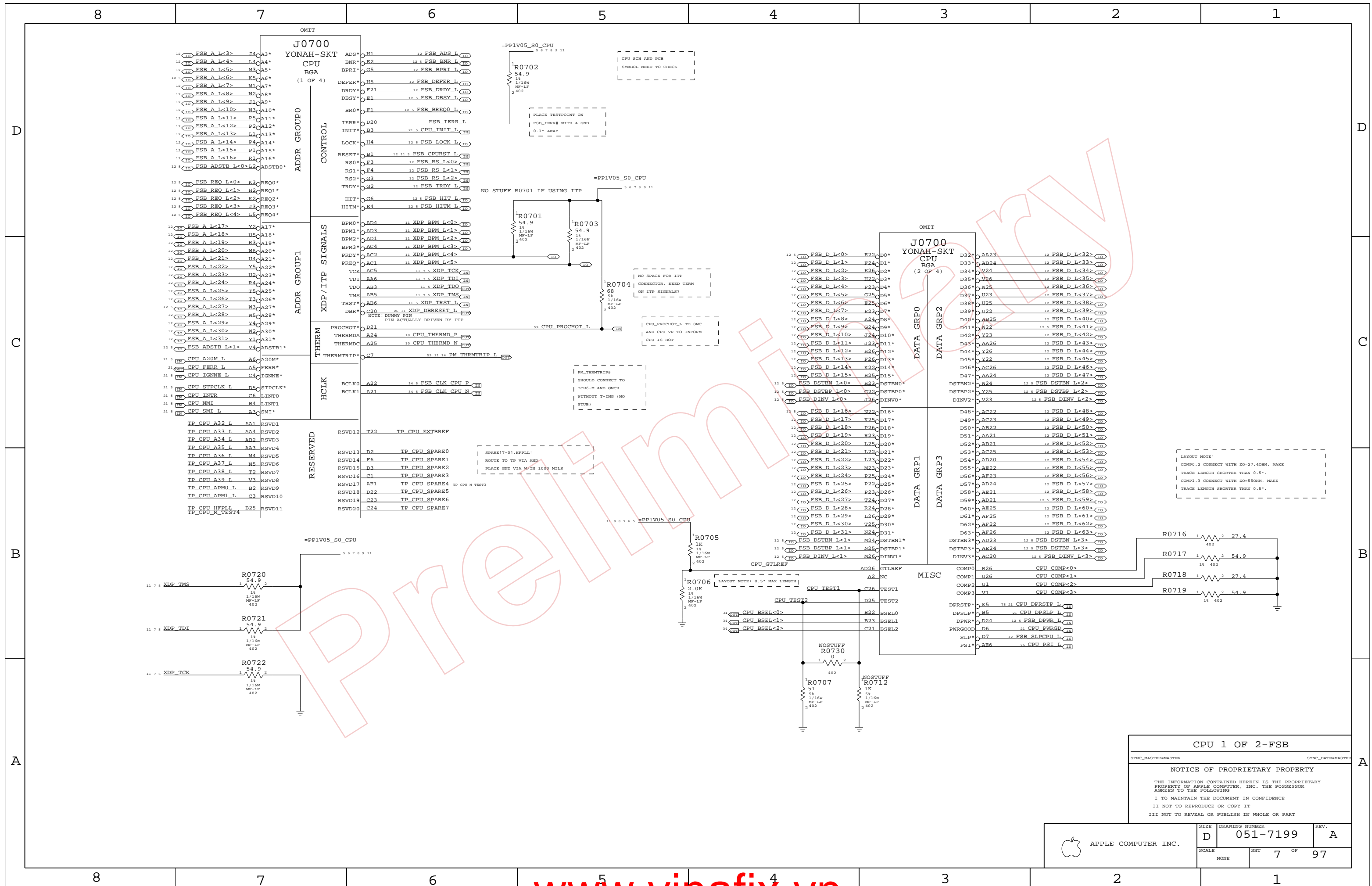
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SCALE	SHT	OF	
NONE	6	97	



CPU 1 OF 2-FSB

SYNC_MASTER-MASTER SYNC_DATE-MASTER

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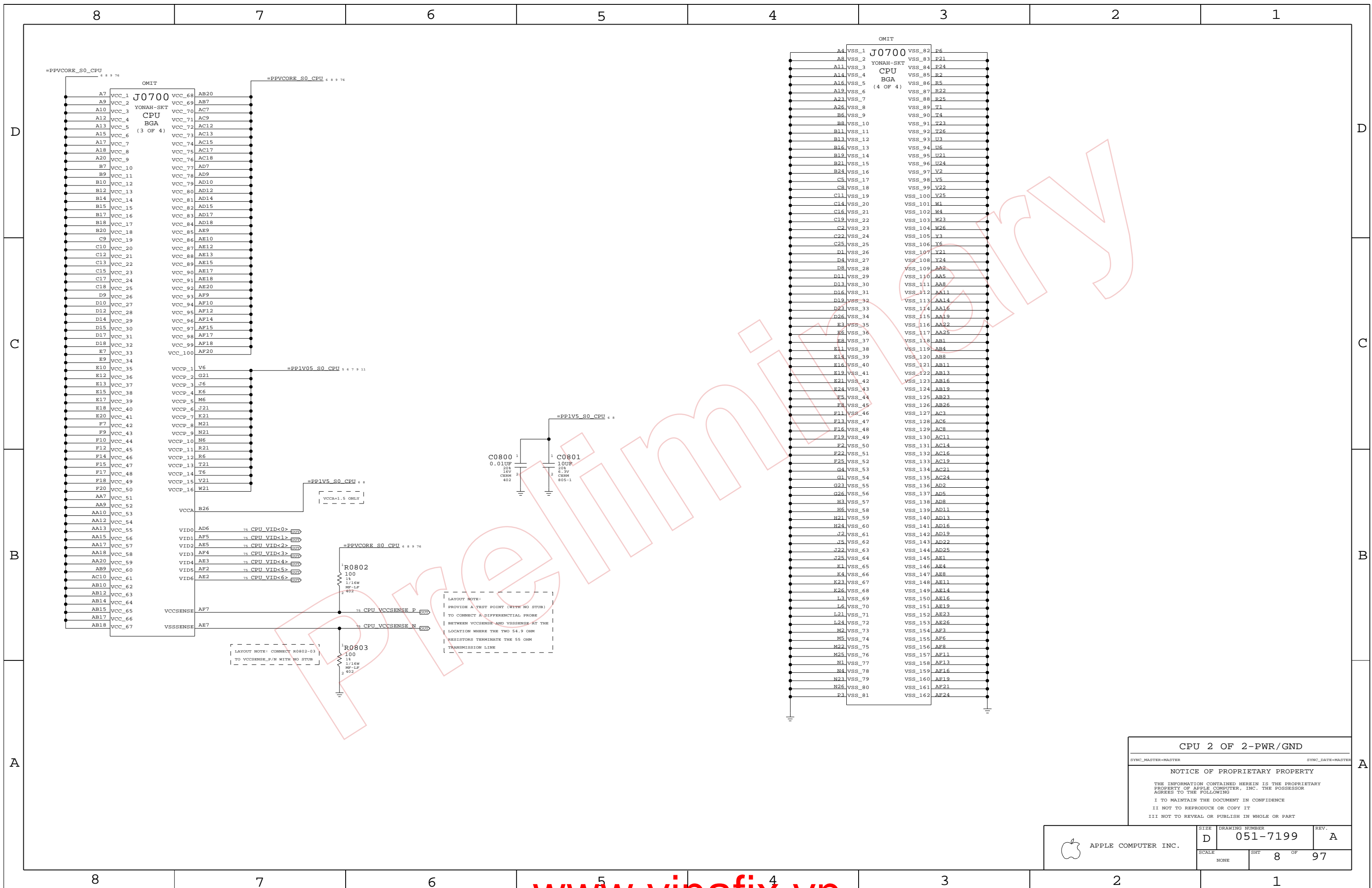
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NONE			



CPU 2 OF 2-PWR/GND

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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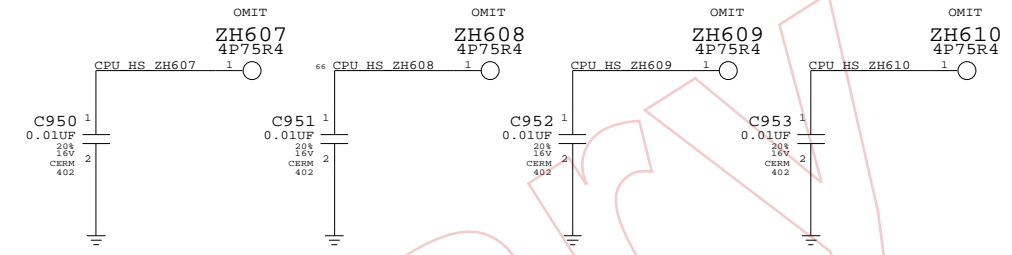
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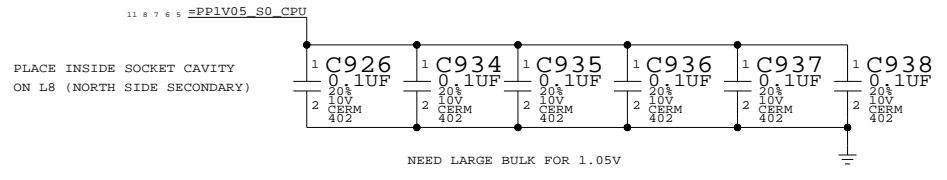
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	A
SCALE	SHT	OF	REV.
NONE	8	97	

CPU HEATSINK MOUNTING HOLES

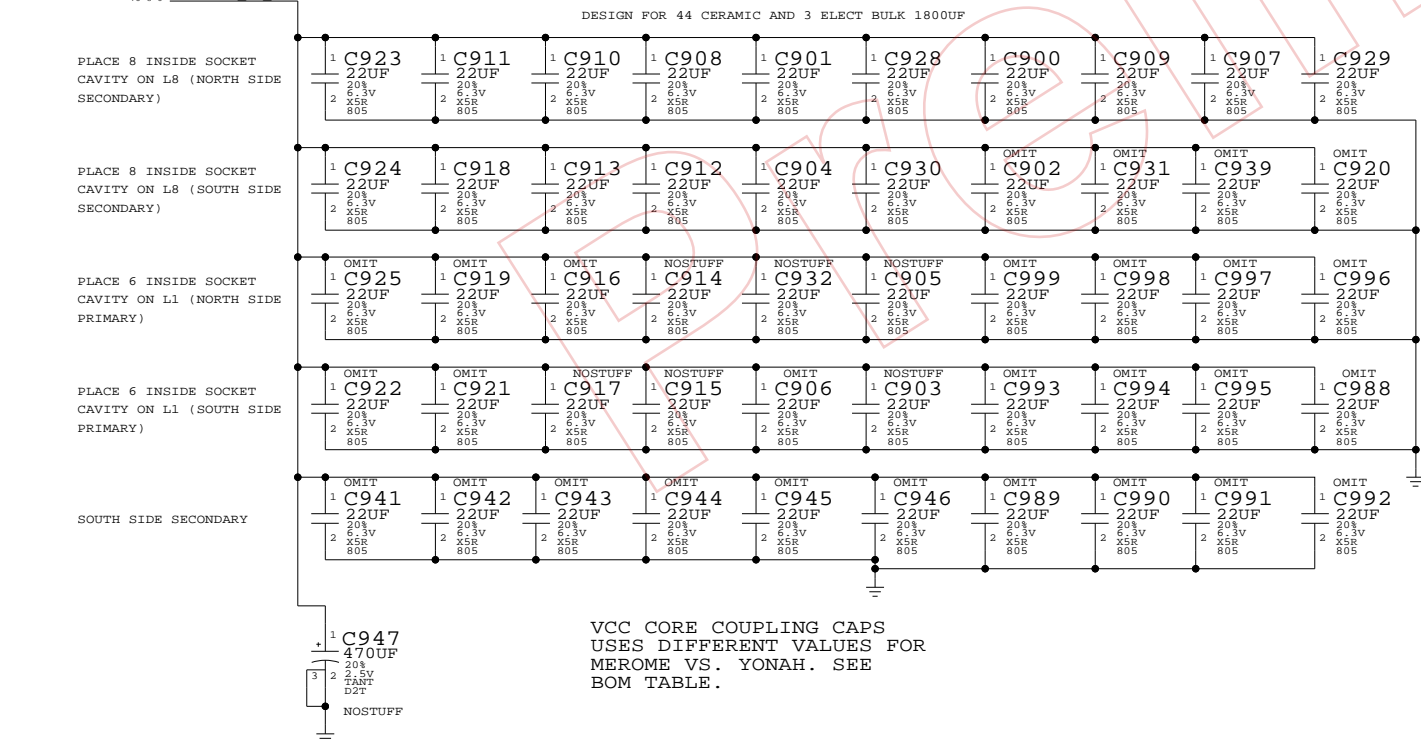


WE HAD A 330UF ELEC CAP HERE FOR 1.05V RAIL - CHECK WE CAN REMOVE

VCCP CORE DECOUPLING



VCC CORE DECOUPLING



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
138S0552	28	CAP, 22UF, 6.3V, 20k, X5R, 0805	C922, C925, C906, C939, C919, C993, C942, C991, C995		MEROME C990, C989, C988, C920, C997, C992, C994, C996, C921, C999, C943, C998, C944, C945, C946, C941, C916, C931, C902
138S0558	28	CAP, 10UF, 6.3V, 20k, X5R, 0805	C922, C925, C906, C939, C919, C993, C942, C991, C995		YONAH C990, C989, C988, C920, C997, C992, C994, C996, C921, C999, C943, C998, C944, C945, C946, C941, C916, C931, C902

CPU DECAPS & VID<>

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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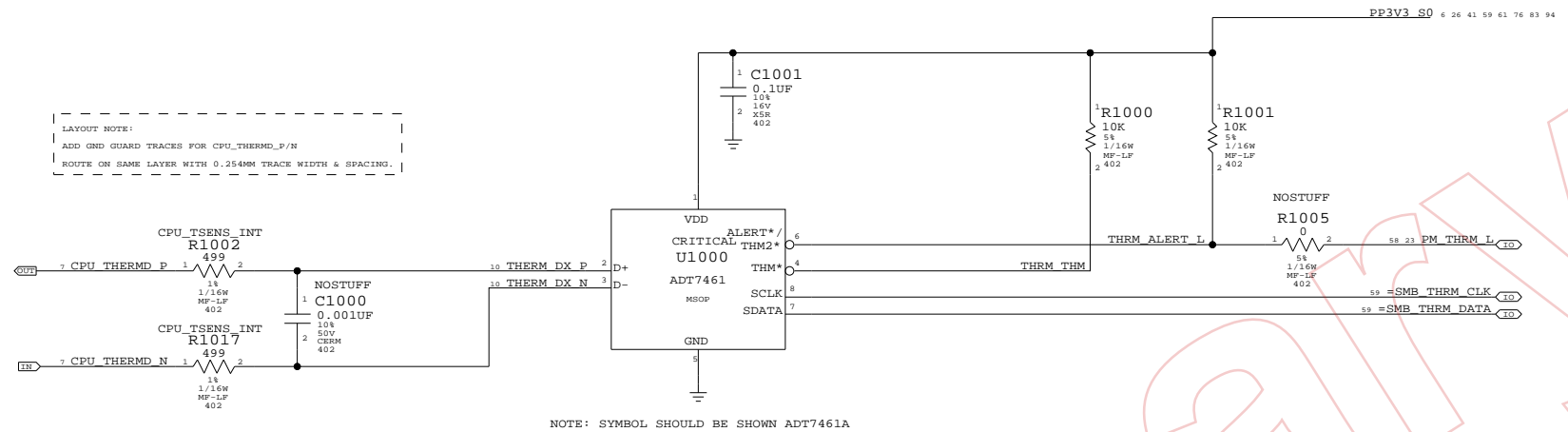
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	A
SCALE	SHT	OF	REV.
NONE	9	97	

CPU THERMAL SENSOR

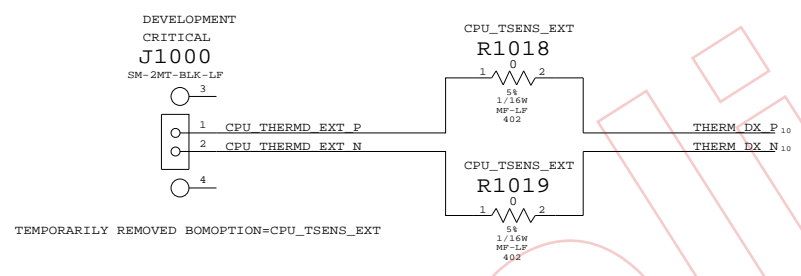
NOTE:
IF CPU T DIODE TO BE READ IN OFF STATE,
THEN THIS SHOULD BE S5

LAYOUT NOTE:
ADD GND GUARD TRACKS FOR CPU_THERMD_P/N
ROUTE ON SAME LAYER WITH 0.254MM TRACE WIDTH & SPACING.



NOTE: SYMBOL SHOULD BE SHOWN ADT7461A

LAYOUT NOTE:
PLACE R1002 AND R1018 SUCH THAT THEY SHARE ONE PAD
PLACE R1017 AND R1019 SUCH THAT THEY SHARE ONE PAD



CPU TEMP SENSOR

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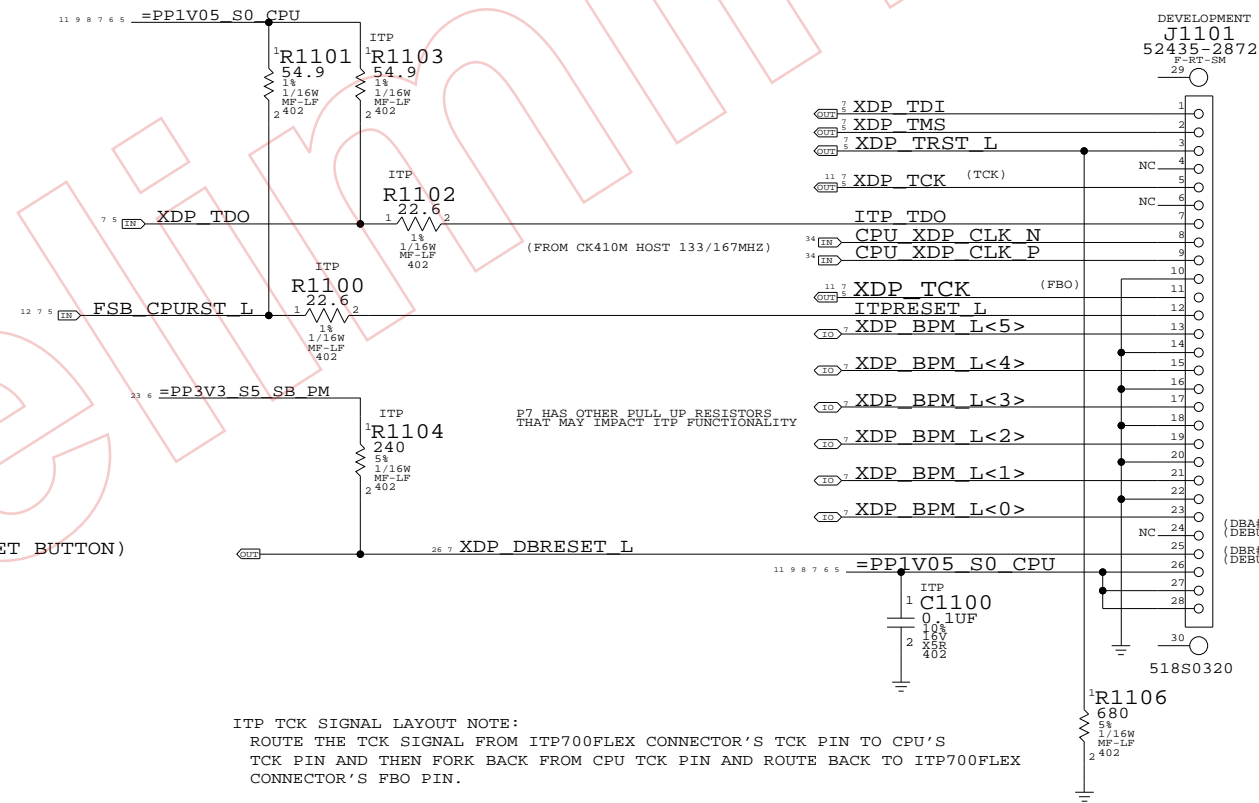
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	D	051-7199	A
SCALE	SHT	10 OF 97	
NONE			

CPU ITP700FLEX DEBUG SUPPORT



DEVELOPMENT
J1101
52435-2872
P-ST-SM
29

(DBA#) INDICATE THAT ITP IS USING TAP I/F, NC IN 945GM CHIPSET SYSTEM.
(DEBUG PORT ACTIVE)
(DBR#) TO ICH7M SYS_RST*, AND WITH SYSTEM RESET LOGIC
(DEBUG PORT RESET)

ITP TCK SIGNAL LAYOUT NOTE:
ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S
TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX
CONNECTOR'S FBO PIN.

(AND WITH RESET BUTTON)

P7 HAS OTHER PULL UP RESISTORS
THAT MAY IMPACT ITP FUNCTIONALITY

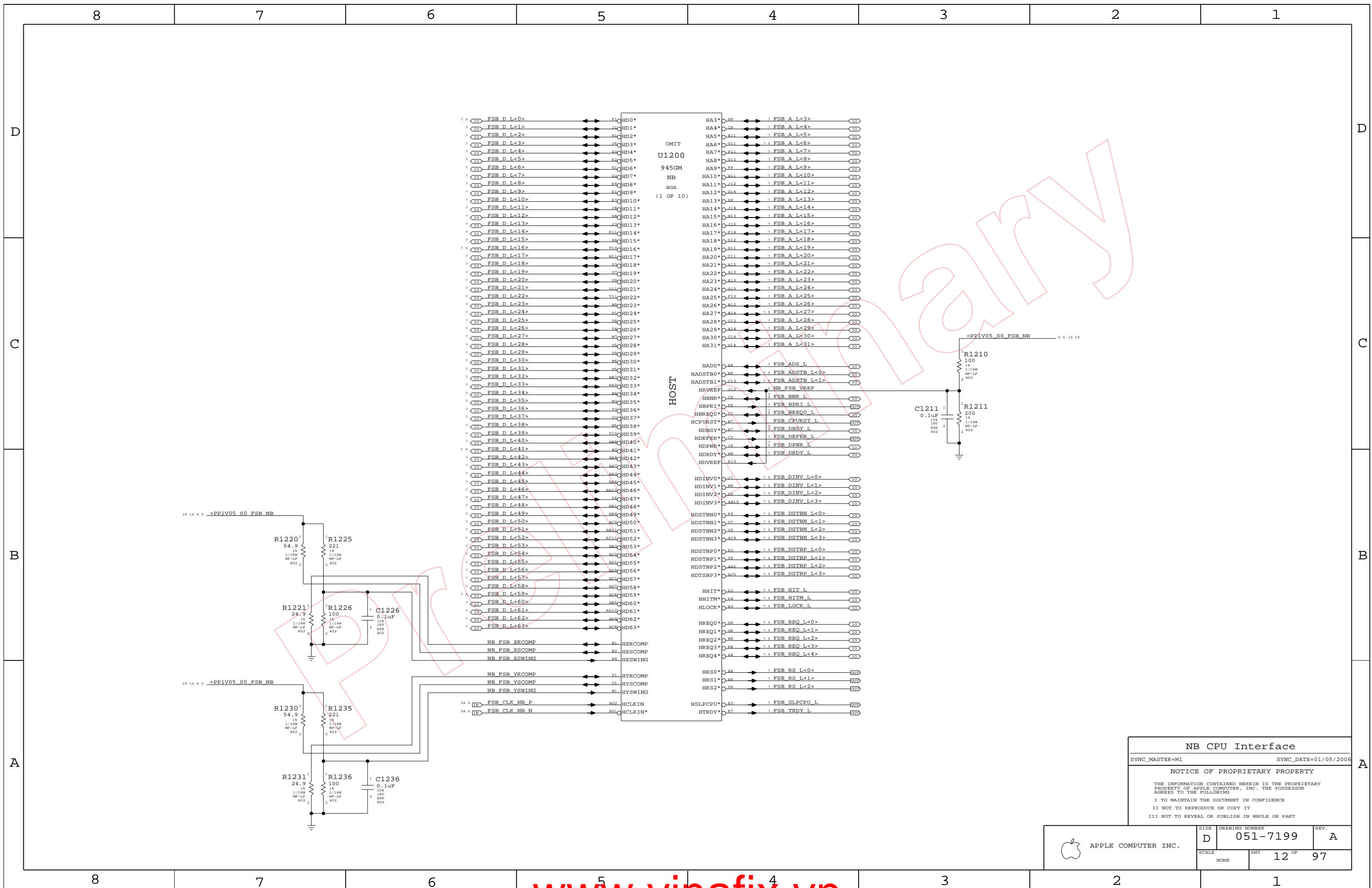
CPU ITP700FLEX DEBUG
 SYNC_MASTER=M38 SYNC_DATE=01/05/2006

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	D	051-7199	A
SCALE	SHT	11 OF	97
NONE			



NB CPU Interface

SYNC_MASTER=M1 SYNC_DATE=01/05/2006

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	SCALE NONE	SHEET 12 OF 97	

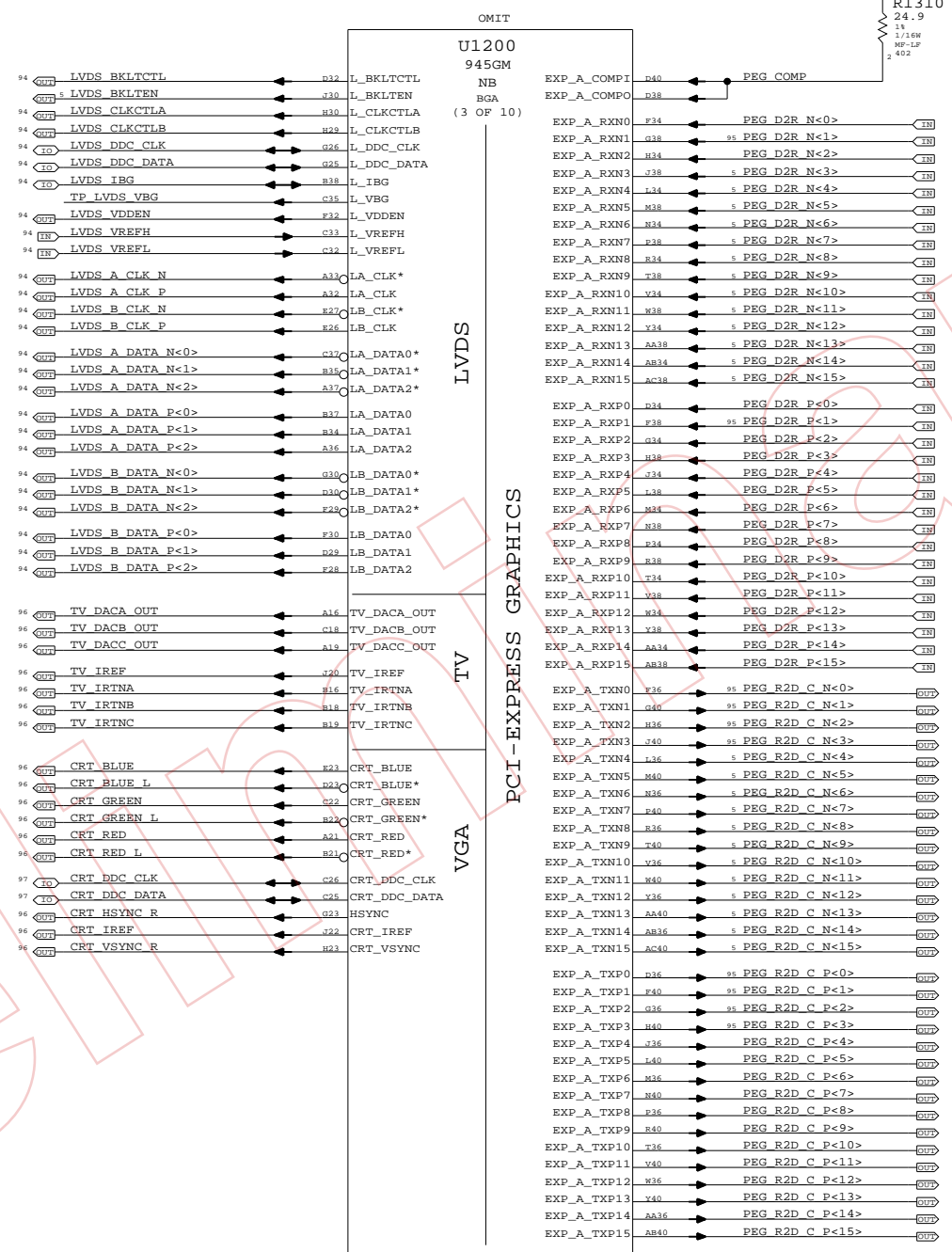
LVDS Disable
 Can leave all signals NC if LVDS is not implemented
 Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
 VCCD_LVDS must remain powered with proper decoupling.
 Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:
 Composite: DACA only
 S-Video: DACB & DACC only
 Component: DACA, DACB & DACC

Unused DAC outputs must remain powered, but can omit
 filtering components. Unused DAC outputs should
 connect to GND through 75-ohm resistors.

TV-Out Disable
 Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail.
 Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and
 VCCA_TVVBG to 1.5V power rail. Tie VSSA_TVVBG to GND.

CRT Disable
 Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie
 HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core
 rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.



SDVO Alternate Function
 SDVO_TVCLKIN#
 SDVO_INT#
 SDVO_FLDSTALL#

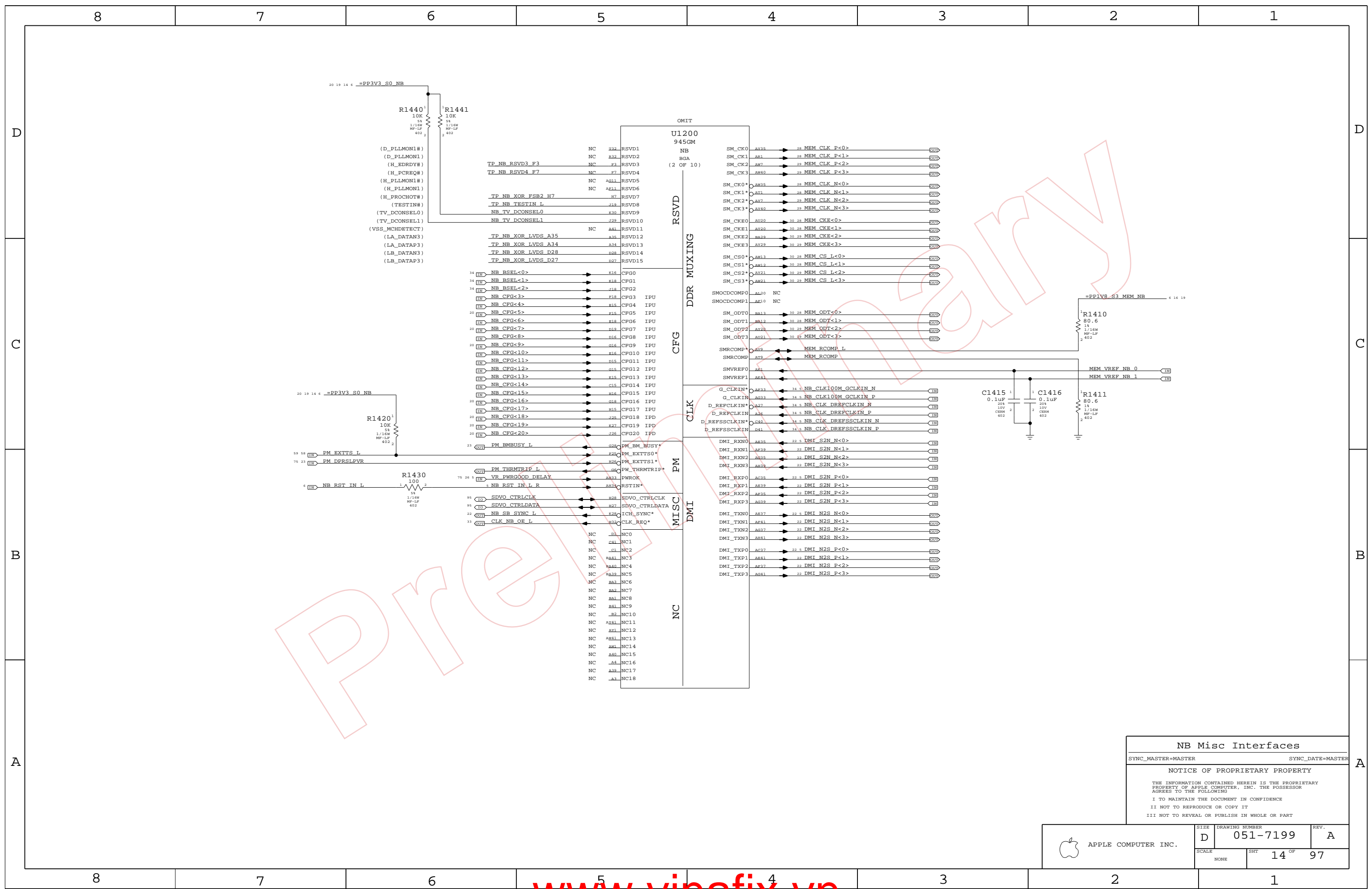
SDVO_TVCLKIN
 SDVO_INT
 SDVO_FLDSTALL

SDVOB_RED#
 SDVOB_GREEN#
 SDVOB_BLUE#
 SDVOB_CLKN
 SDVOC_RED#
 SDVOC_GREEN#
 SDVOC_BLUE#
 SDVOC_CLKN

SDVOB_RED
 SDVOB_GREEN
 SDVOB_BLUE
 SDVOB_CLKP
 SDVOC_RED
 SDVOC_GREEN
 SDVOC_BLUE
 SDVOC_CLKP

NB PEG / Video Interfaces
 SYNC_MASTER=M1 SYNC_DATE=01/05/2006
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	D	051-7199	A
SCALE	SHT	13 OF 97	
NONE			



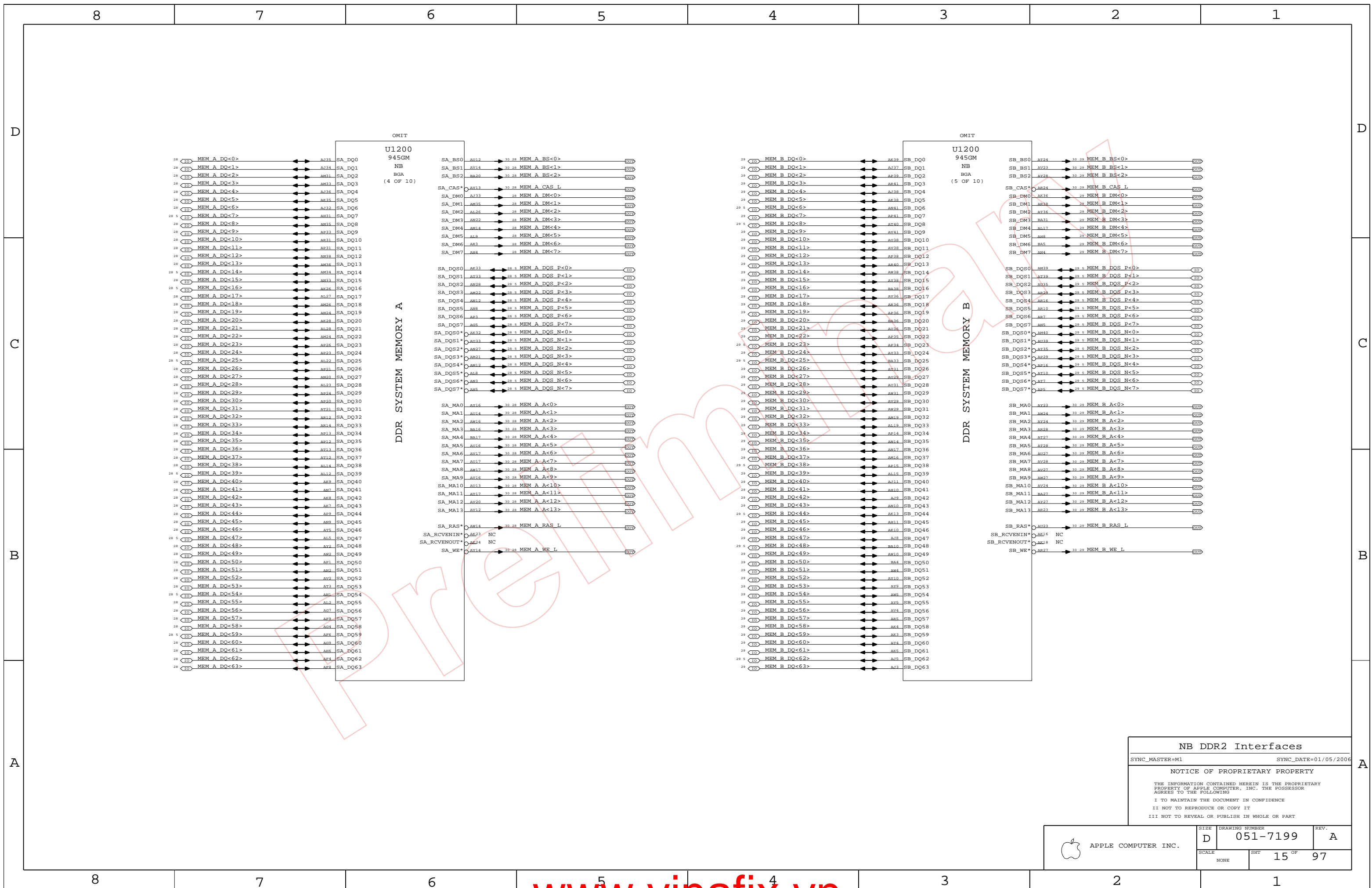
NB Misc Interfaces

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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SCALE	SHT	14 OF 97	
NONE			



NB DDR2 Interfaces

SYNC_MASTER=M1 SYNC_DATE=01/05/2006

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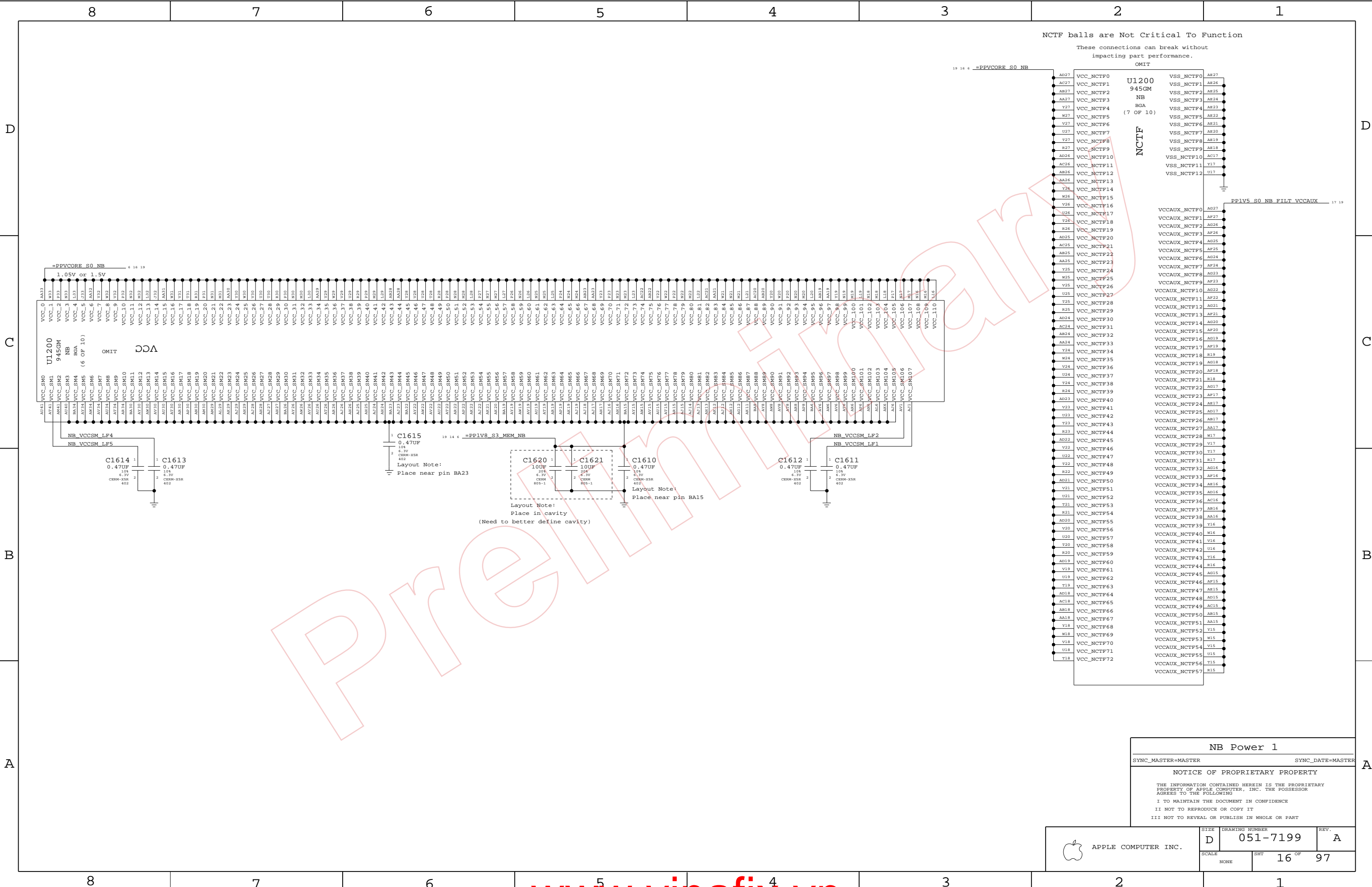
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7199	REV. A
	SCALE NONE	SHEET 15 OF 97	



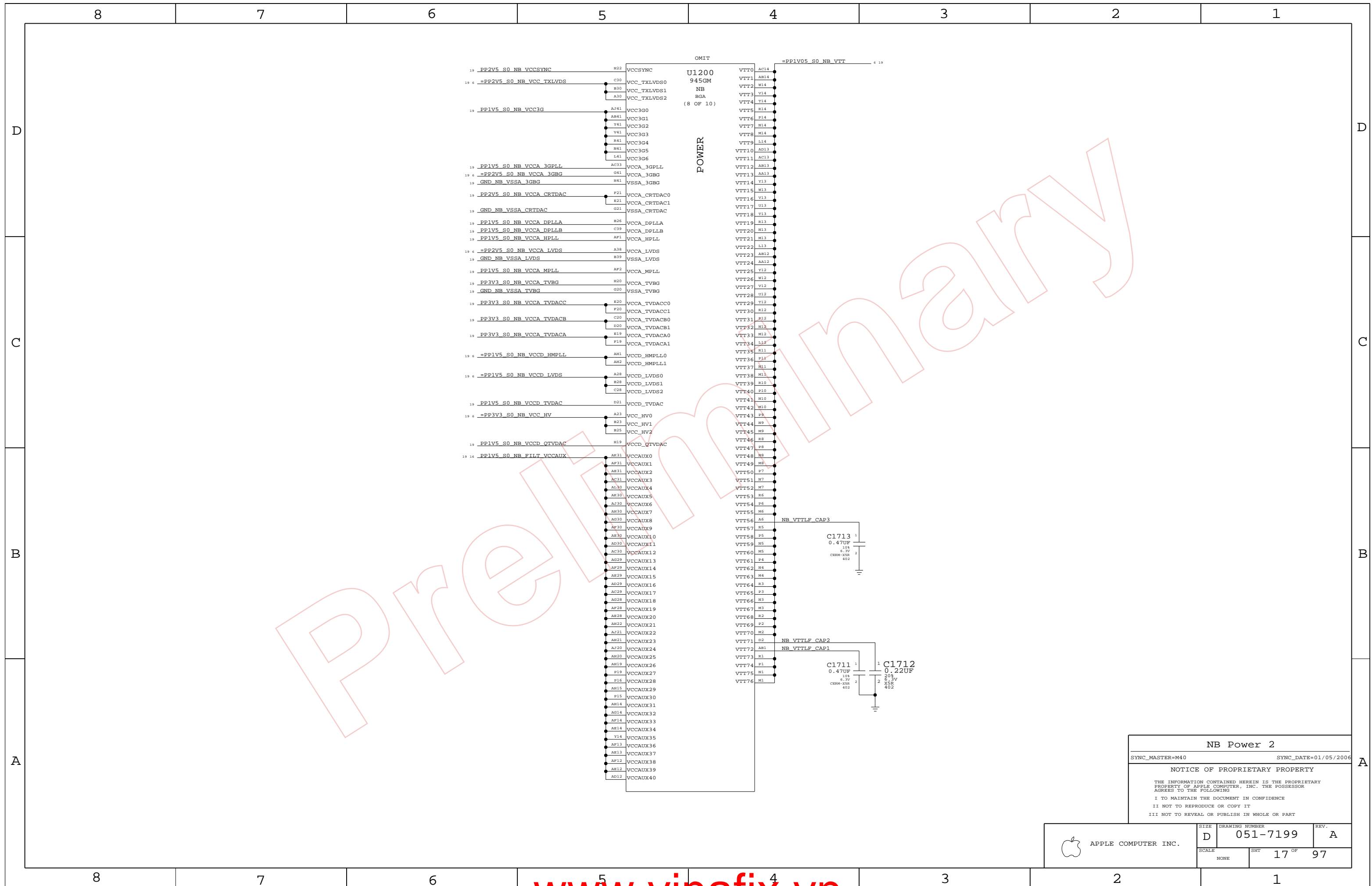
NCTF balls are Not Critical To Function
 These connections can break without impacting part performance.
 OMIT

U1200
 945GM
 NB
 BGA
 (7 OF 10)
 NCTF

VCC_NCTF0
 VCC_NCTF1
 VCC_NCTF2
 VCC_NCTF3
 VCC_NCTF4
 VCC_NCTF5
 VCC_NCTF6
 VCC_NCTF7
 VCC_NCTF8
 VCC_NCTF9
 VCC_NCTF10
 VCC_NCTF11
 VCC_NCTF12
 VCC_NCTF13
 VCC_NCTF14
 VCC_NCTF15
 VCC_NCTF16
 VCC_NCTF17
 VCC_NCTF18
 VCC_NCTF19
 VCC_NCTF20
 VCC_NCTF21
 VCC_NCTF22
 VCC_NCTF23
 VCC_NCTF24
 VCC_NCTF25
 VCC_NCTF26
 VCC_NCTF27
 VCC_NCTF28
 VCC_NCTF29
 VCC_NCTF30
 VCC_NCTF31
 VCC_NCTF32
 VCC_NCTF33
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 VCC_NCTF36
 VCC_NCTF37
 VCC_NCTF38
 VCC_NCTF39
 VCC_NCTF40
 VCC_NCTF41
 VCC_NCTF42
 VCC_NCTF43
 VCC_NCTF44
 VCC_NCTF45
 VCC_NCTF46
 VCC_NCTF47
 VCC_NCTF48
 VCC_NCTF49
 VCC_NCTF50
 VCC_NCTF51
 VCC_NCTF52
 VCC_NCTF53
 VCC_NCTF54
 VCC_NCTF55
 VCC_NCTF56
 VCC_NCTF57
 VSS_NCTF0
 VSS_NCTF1
 VSS_NCTF2
 VSS_NCTF3
 VSS_NCTF4
 VSS_NCTF5
 VSS_NCTF6
 VSS_NCTF7
 VSS_NCTF8
 VSS_NCTF9
 VSS_NCTF10
 VSS_NCTF11
 VSS_NCTF12

NB Power 1
 SYNC_MASTER=MASTER SYNC_DATE=MASTER
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	D	051-7199	A
SCALE	SHT	16 OF 97	
NONE			



NB Power 2

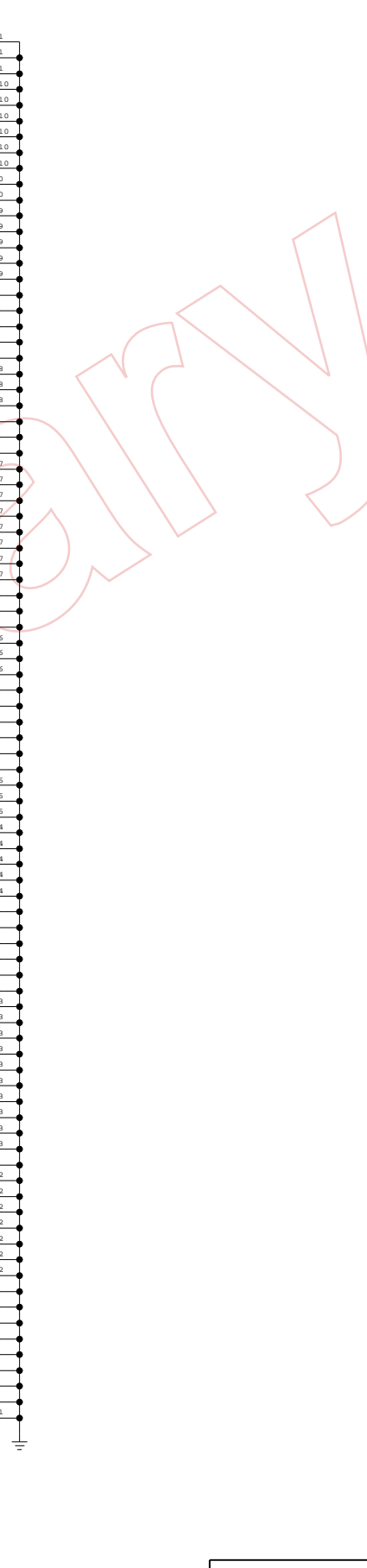
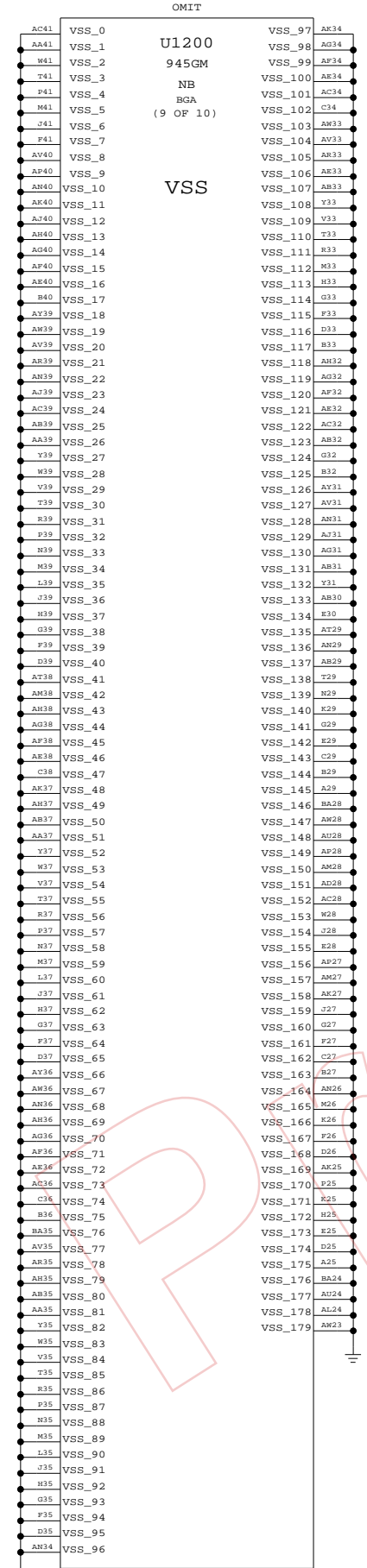
SYNC_MASTER=M40 SYNC_DATE=01/05/2006

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7199	REV. A
	SCALE NONE	SHEET 17 OF 97	



D
C
B
A

D
C
B
A

NB Grounds
 SYNC_MASTER=M1 SYNC_DATE=01/05/2006
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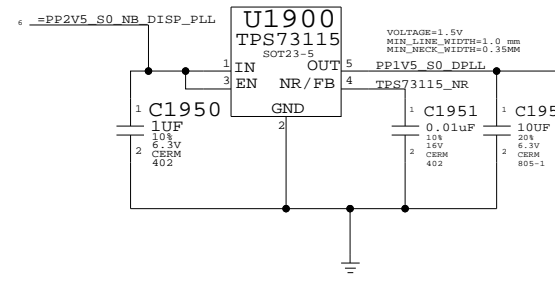
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	A
SCALE	SHT	18 OF 97	
NONE			

Power Interface

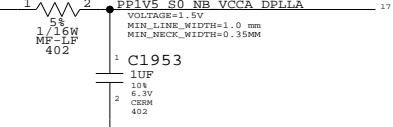
These are the power signals that leave the NB "block"

- PP1V05_S0_FSB_NB 5 6 12
- PPVCORE_S0_NB 6 16 19
- PP1V05_S0_NB_VTT 6 17 19
- PP1V5_S0_NB 6 19
- PP1V5_S0_NB_PCIE 6 13
- PP1V5_S0_NB_PLL 6 19
- PP1V5_S0_NB_TVDAC 6 19
- PP1V5_S0_NB_VCCD_HMPLL 6 17
- PP1V5_S0_NB_VCCD_LVDS 6 17 19
- PP1V5_S0_NB_VCCAUX 6 19
- PP1V8_S3_MEM_NB 6 14 16 19
- PP2V5_S0_NB_VCCSYNC 19 6
- PP2V5_S0_NB_VCC_TXLVDS 6 17 19
- PP2V5_S0_NB_VCCA_3GBG 6 19
- PP2V5_S0_NB_VCCA_LVDS 6 17 19
- PP3V3_S0_NB 6 14 20
- PP3V3_S0_NB_VCC_HV 6 17 19
- PP5V_S0_NB_TVDAC 6 19

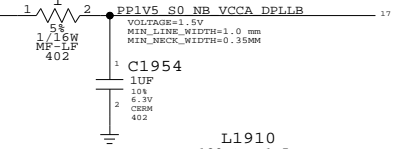
MCH DISPLAY PLL POWER LDO



MCH VCCA_DPLL FILTER



GMCH VCCA_DPLL_B FILTER



GMCH VCCD_LVDS BYPASS

(MCH LVDS DIGITAL 1.5V PWR)



GMCH VCCD_LVDS BYPASS

(MCH LVDS DIGITAL 2.5V PWR)

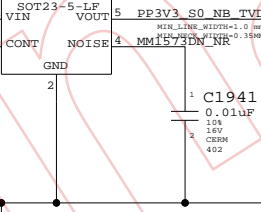


FILTERING REQUIRED FOR

INTEGRATED GFX (PG. 333)



U1901 MM157



Layout Note:
This 0.1uF cap should be within 5 mm of NB edge

Layout Note:
Route to caps, then GND

Layout Note:
These 2 caps should be within 6.35 mm of NB edge

Layout Note:
Route to caps, then GND

Layout Note:
These 2 caps should be within 6.35 mm of NB edge

Layout Note:
Route to caps, then GND

Layout Note:
These 8 caps should be within 6.35 mm of NB edge

Layout Note:
Route to caps, then GND

Layout Note:
Route to caps, then GND

Layout Note:
Route to caps, then GND

Layout Note:
Route to caps, then GND

Layout Note:
Route to caps, then GND

Layout Note:
Route to caps, then GND

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Route to caps, then GND

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Layout Note:
Route to caps, then GND

Layout Note:
Route to caps, then GND

NB (GM) Decoupling

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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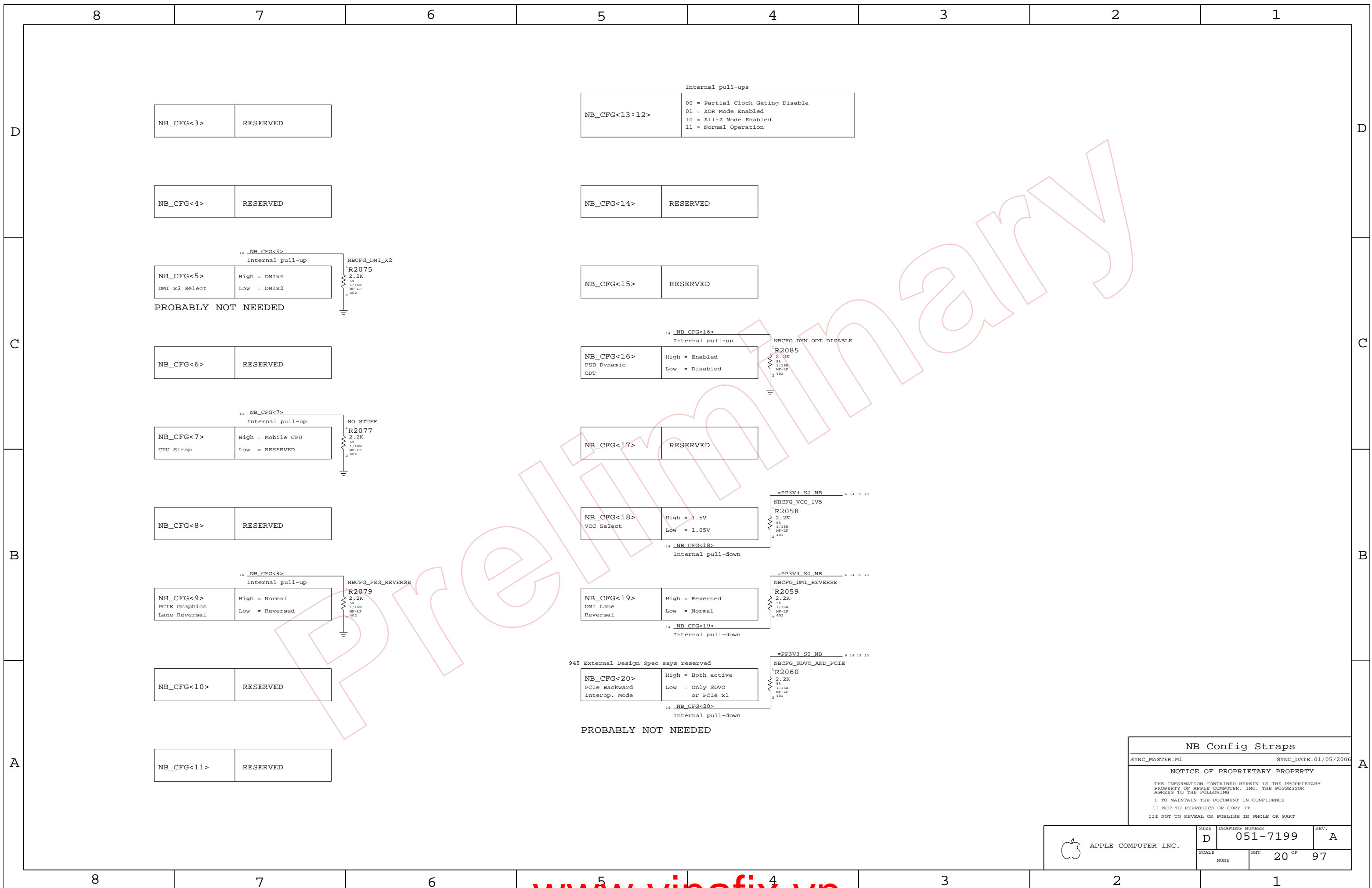
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D	051-7199	A
SCALE	SHT	19 OF 97
NONE		

APPLE COMPUTER INC.



Internal pull-ups

NB_CFG<13:12>	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal Operation
---------------	--

NB_CFG<14>	RESERVED
------------	----------

NB_CFG<15>	RESERVED
------------	----------

Internal pull-up

NB_CFG<16>	High = Enabled Low = Disabled
------------	----------------------------------

NB_CFG<17>	RESERVED
------------	----------

Internal pull-down

NB_CFG<18>	High = 1.5V Low = 1.05V
------------	----------------------------

Internal pull-down

NB_CFG<19>	High = Reversed Low = Normal
------------	---------------------------------

945 External Design Spec says reserved

Internal pull-down

NB_CFG<20>	High = Both active Low = Only SDVO or PCIe x1
------------	--

NB_CFG<3>	RESERVED
-----------	----------

NB_CFG<4>	RESERVED
-----------	----------

Internal pull-up

NB_CFG<5>	High = DMIX4 Low = DMIX2
-----------	-----------------------------

PROBABLY NOT NEEDED

NB_CFG<6>	RESERVED
-----------	----------

Internal pull-up

NB_CFG<7>	High = Mobile CPU Low = RESERVED
-----------	-------------------------------------

NB_CFG<8>	RESERVED
-----------	----------

Internal pull-up

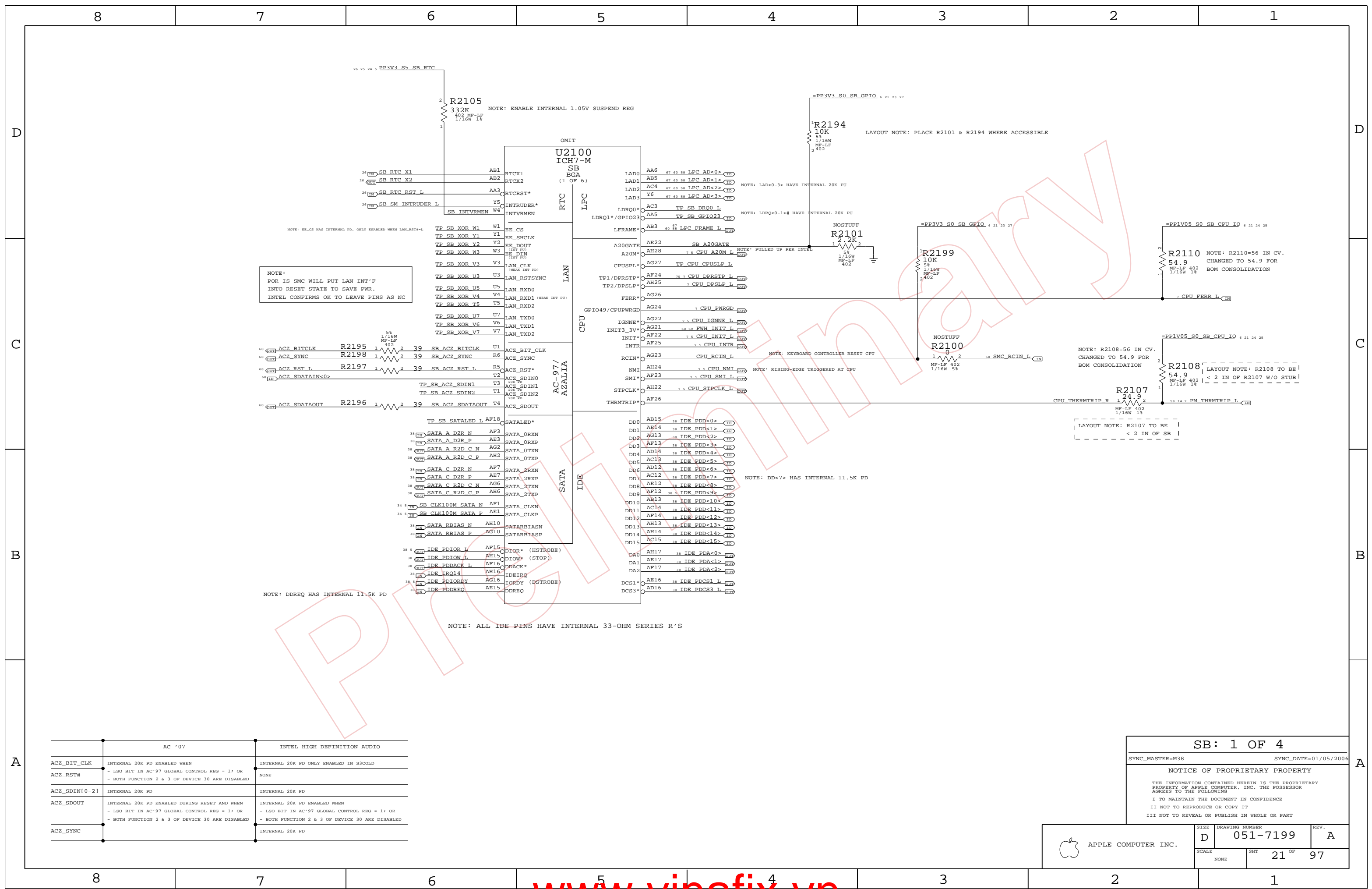
NB_CFG<9>	High = Normal Low = Reversed
-----------	---------------------------------

NB_CFG<10>	RESERVED
------------	----------

NB_CFG<11>	RESERVED
------------	----------

NB Config Straps
 SYNC_MASTER=M1 SYNC_DATE=01/05/2006
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	D	051-7199	A
SCALE	SHT	20 OF 97	
NONE			



NOTE:
 POR IS SMC WILL PUT LAN INT'F
 INTO RESET STATE TO SAVE PWR.
 INTEL CONFIRMS OK TO LEAVE PINS AS NC

NOTE: DDREQ HAS INTERNAL 11.5K PD

NOTE: ALL IDE PINS HAVE INTERNAL 33-OHM SERIES R'S

AC '07	INTEL HIGH DEFINITION AUDIO
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR
ACZ_RST#	NONE
ACZ_SDIN[0-2]	INTERNAL 20K PD
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
ACZ_SYNC	INTERNAL 20K PD

SB: 1 OF 4

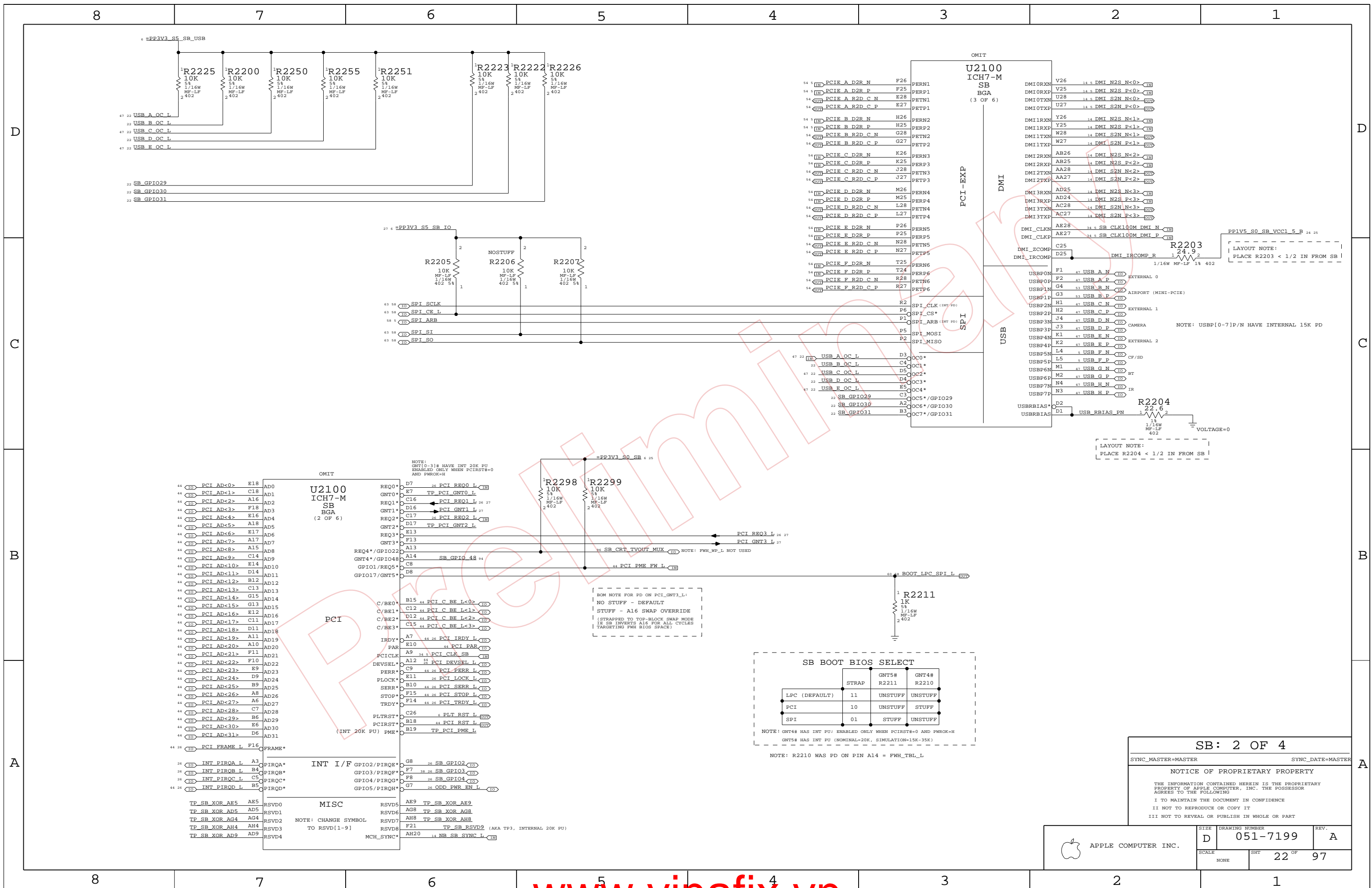
SYNC_MASTER=M38 SYNC_DATE=01/05/2006

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NONE			



SYNC_MASTER=MASTER SYNC_DATE=MASTER

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	D	051-7199	A
SCALE	SHT	22 OF	97
NONE			

SB BOOT BIOS SELECT

	STRAP	GNT5#	GNT4#
LPC (DEFAULT)	11	UNSTUFF	UNSTUFF
PCI	10	UNSTUFF	STUFF
SPI	01	STUFF	UNSTUFF

NOTE: GNT4# HAS INT PU: ENABLED ONLY WHEN PCIRST# = 0 AND FWR0K = H
 GNT5# HAS INT PU (NOMINAL = 20K, SIMULATION = 15K-35K)
 NOTE: R2210 WAS PD ON PIN A14 = FWH_TBL_L

BOM NOTE FOR PD ON PCI_GNT3_L:
 NO STUFF - DEFAULT
 STUFF - A16 SWAP OVERRIDE
 (STRAPPED TO TOP-BLOCK SWAP MODE
 IF SB INVERTS A16 FOR ALL CYCLES
 TARGETING FWH BIOS SPACE)

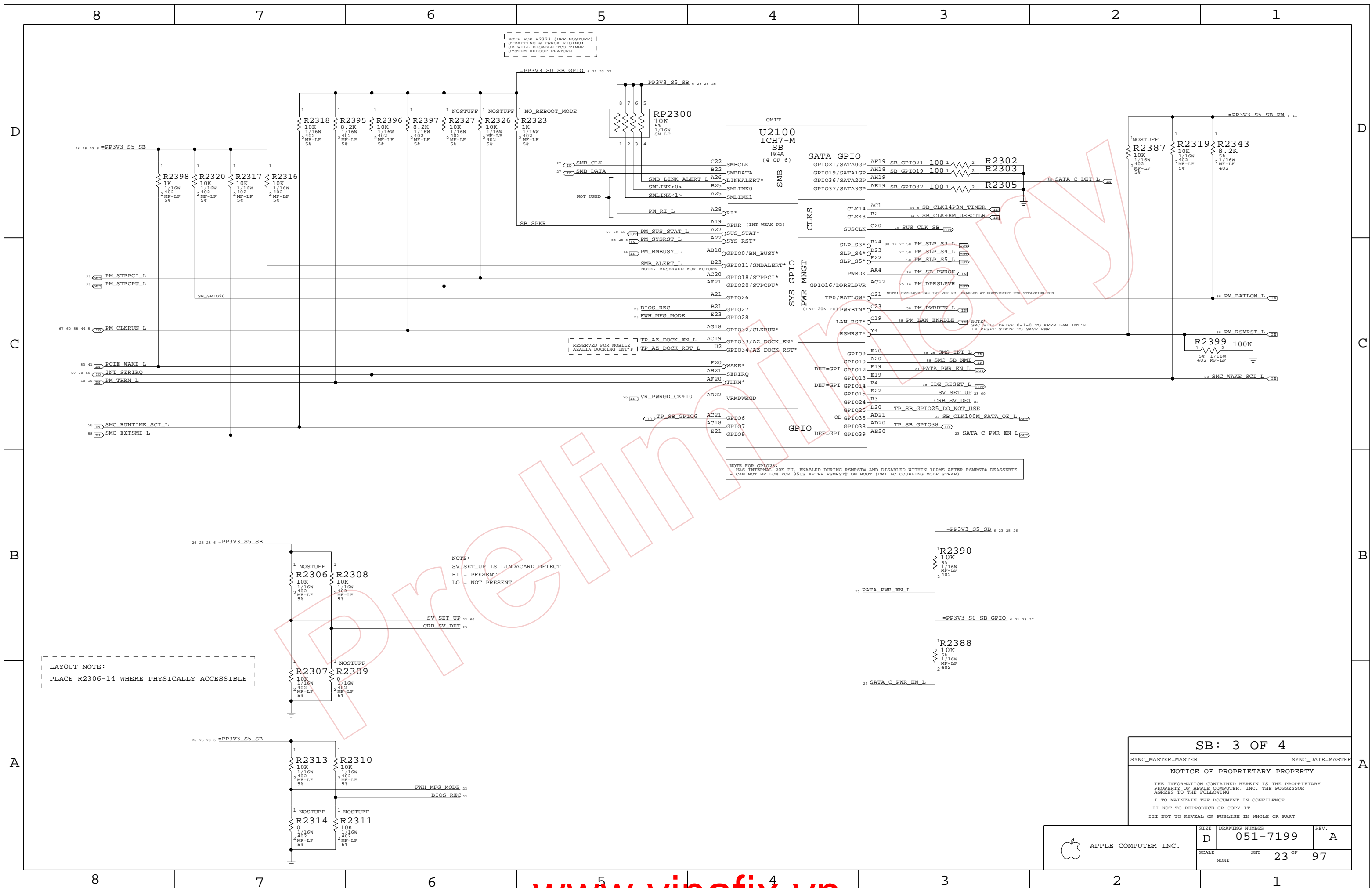
U2100
 ICH7-M
 SB
 BGA
 (2 OF 6)

PCI

INT I/F

MISC

NOTE: CHANGE SYMBOL TO RSV[1-9]
 MCH_SYNC*



NOTE FOR R2323 (DEF-NOSTUFF) | STRAPPING & PWROK RISING: SB WILL DISABLE TOO TIMER SYSTEM REBOOT FEATURE

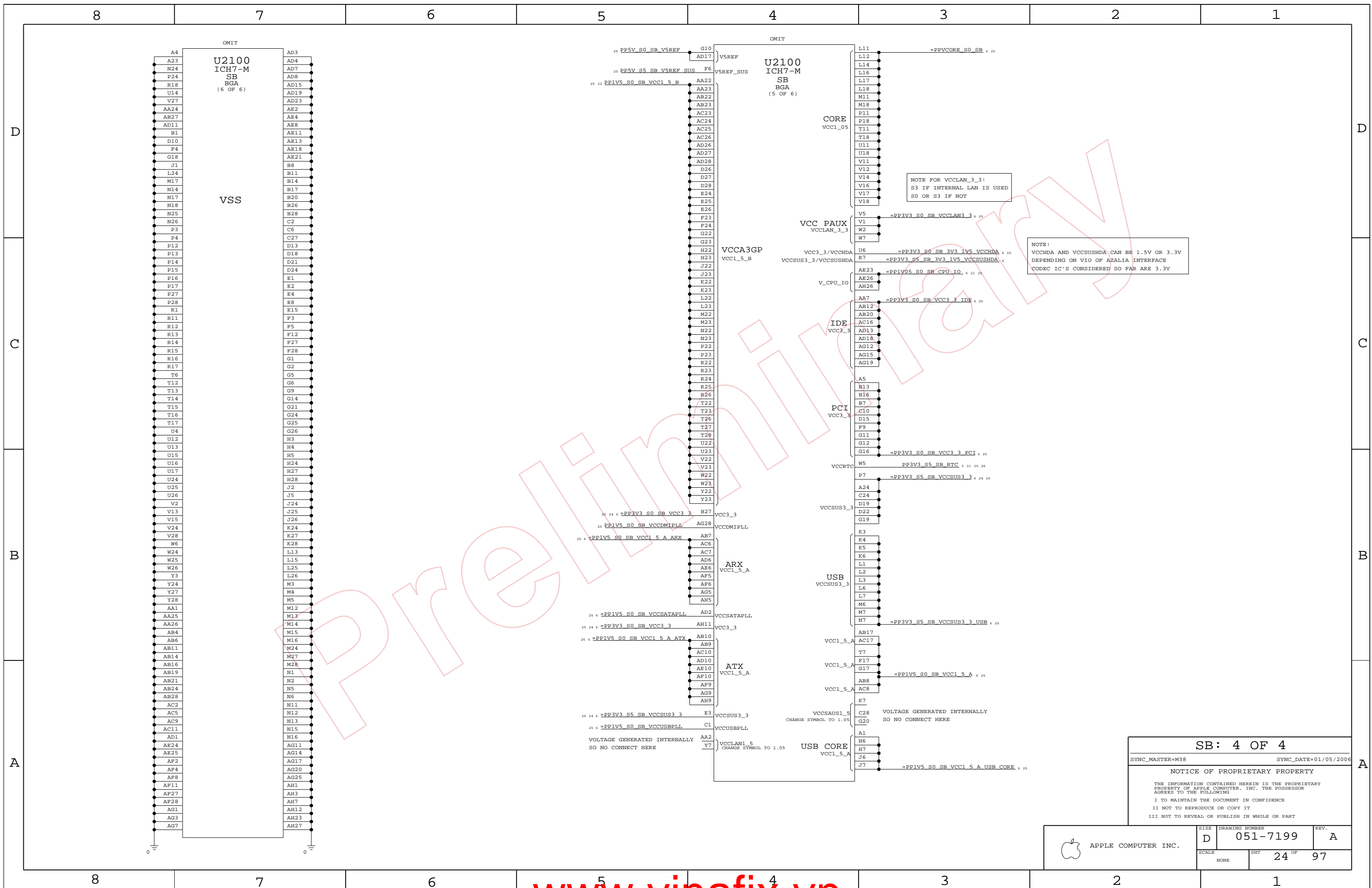
NOTE FOR GPIO25:
 * HAS INTERNAL 20K PU, ENABLED DURING RSMRST# AND DISABLED WITHIN 100MS AFTER RSMRST# DEASSERTS
 * CAN NOT BE LOW FOR 35US AFTER RSMRST# ON BOOT (DMI AC COUPLING MODE STRAP)

NOTE:
 SV_SET_UP IS LINDACARD DETECT
 HI = PRESENT
 LO = NOT PRESENT

LAYOUT NOTE:
 PLACE R2306-14 WHERE PHYSICALLY ACCESSIBLE

SB: 3 OF 4
 SYNC_MASTER=MASTER SYNC_DATE=MASTER
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SCALE	NONE	SHT	23 OF 97

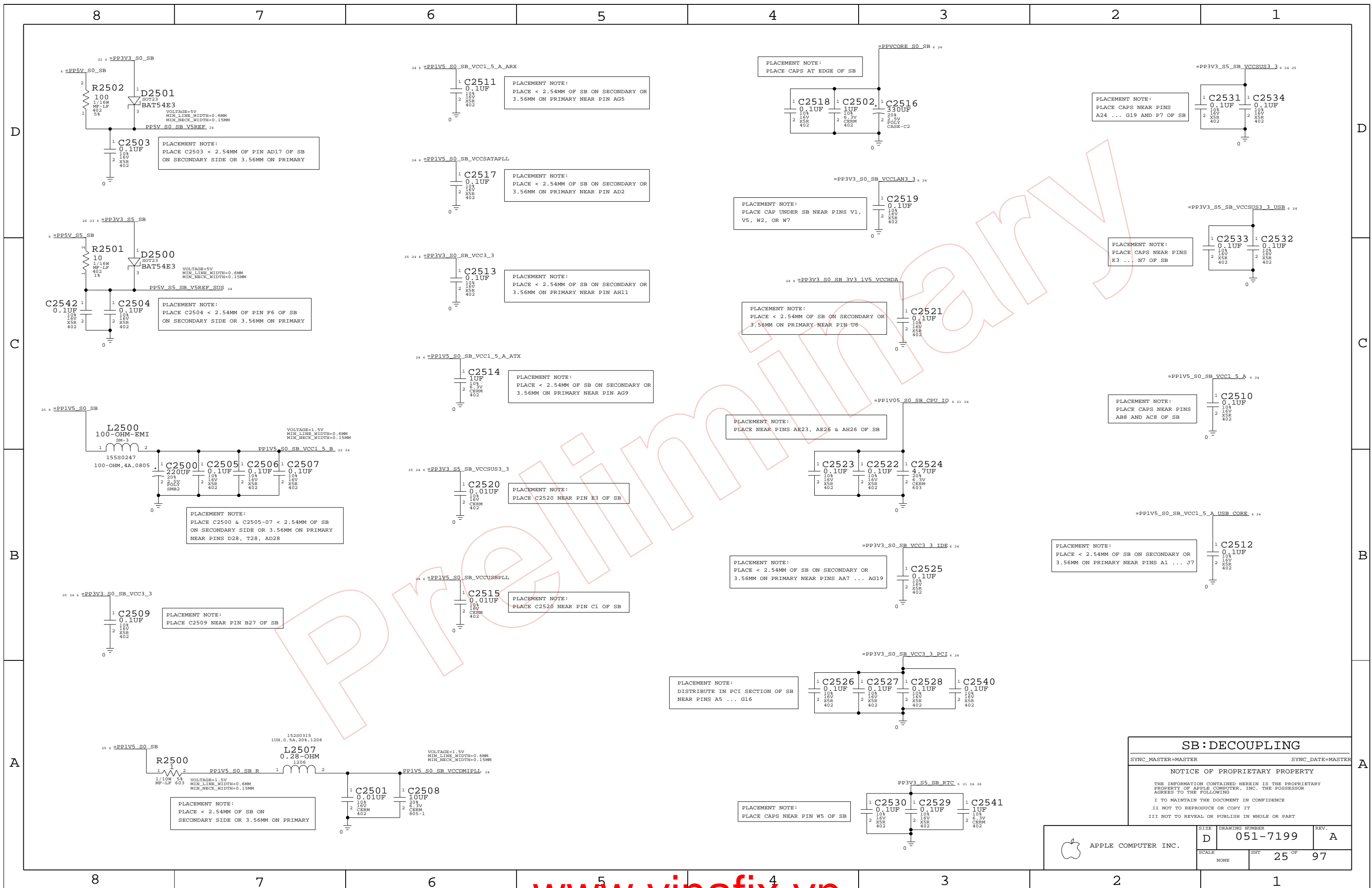


NOTE FOR VCCLAN_3_3:
S3 IF INTERNAL LAN IS USED
S0 OR S3 IF NOT

NOTE:
VCCCHDA AND VCCSUSHDA CAN BE 1.5V OR 3.3V
DEPENDING ON VIO OF AZALIA INTERFACE
CODER IC'S CONSIDERED SO FAR ARE 3.3V

SB: 4 OF 4	
SYNC_MASTER=M38	SYNC_DATE=01/05/2006
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	D	051-7199	A
SCALE	SHT	24 OF 97	
NONE			



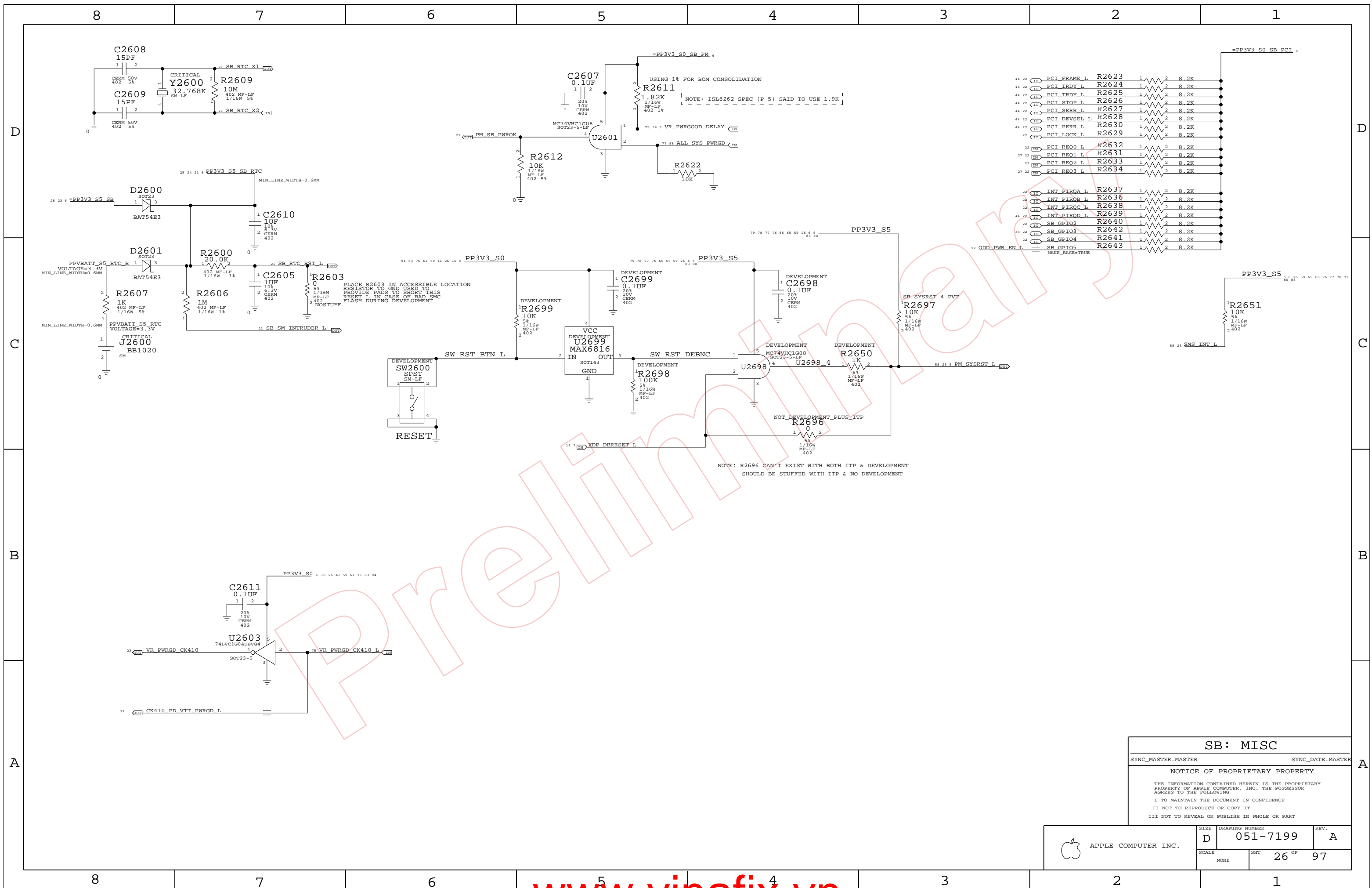
SB: DECOUPLING

SYNC_MASTER=MASTER SYNC_DATE=MASTER

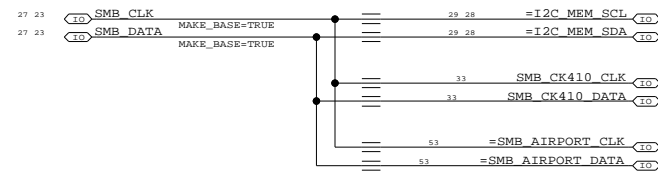
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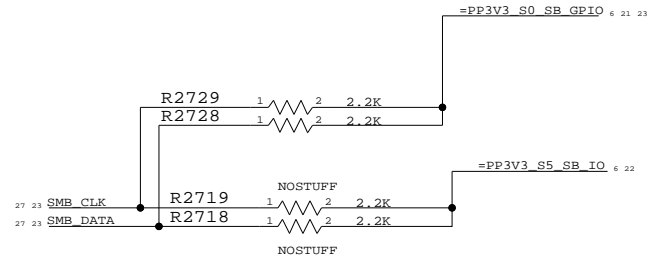
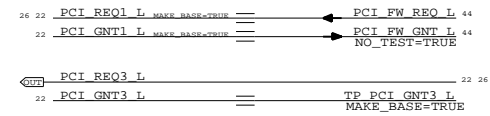
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	A
SCALE	SHT	25 OF	97
NONE			



SB I2C BUSSES



PCI CONTROL




Preliminary

SB: SMB HUB AND ALIAS

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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	D	051-7199	A
SCALE	SHT	27 OF 97	
NONE			

Page Notes

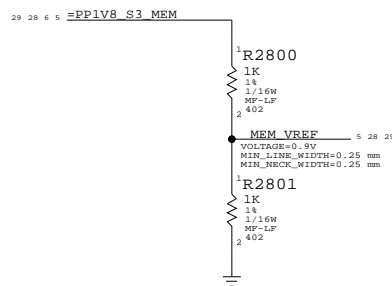
Power aliases required by this page:
 - =PP1V8_S3_MEM
 - =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
 - =I2C_MEM_SCL
 - =I2C_MEM_SDA

BOM options provided by this page:
 (NONE)

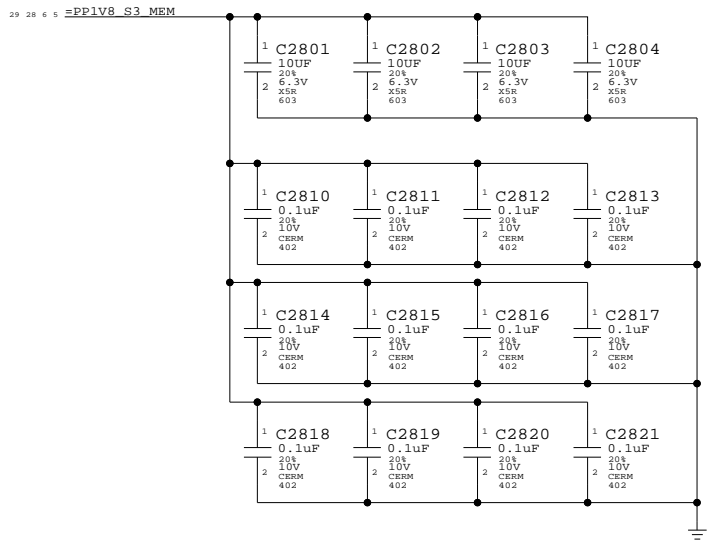
DDR2 VRef

One 0.1uF per connector



DDR2 Bypass Caps

(For return current)



DDR2 SO-DIMM Connector A

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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	D	051-7199	A
SCALE	SHT	28 OF	97
NONE			

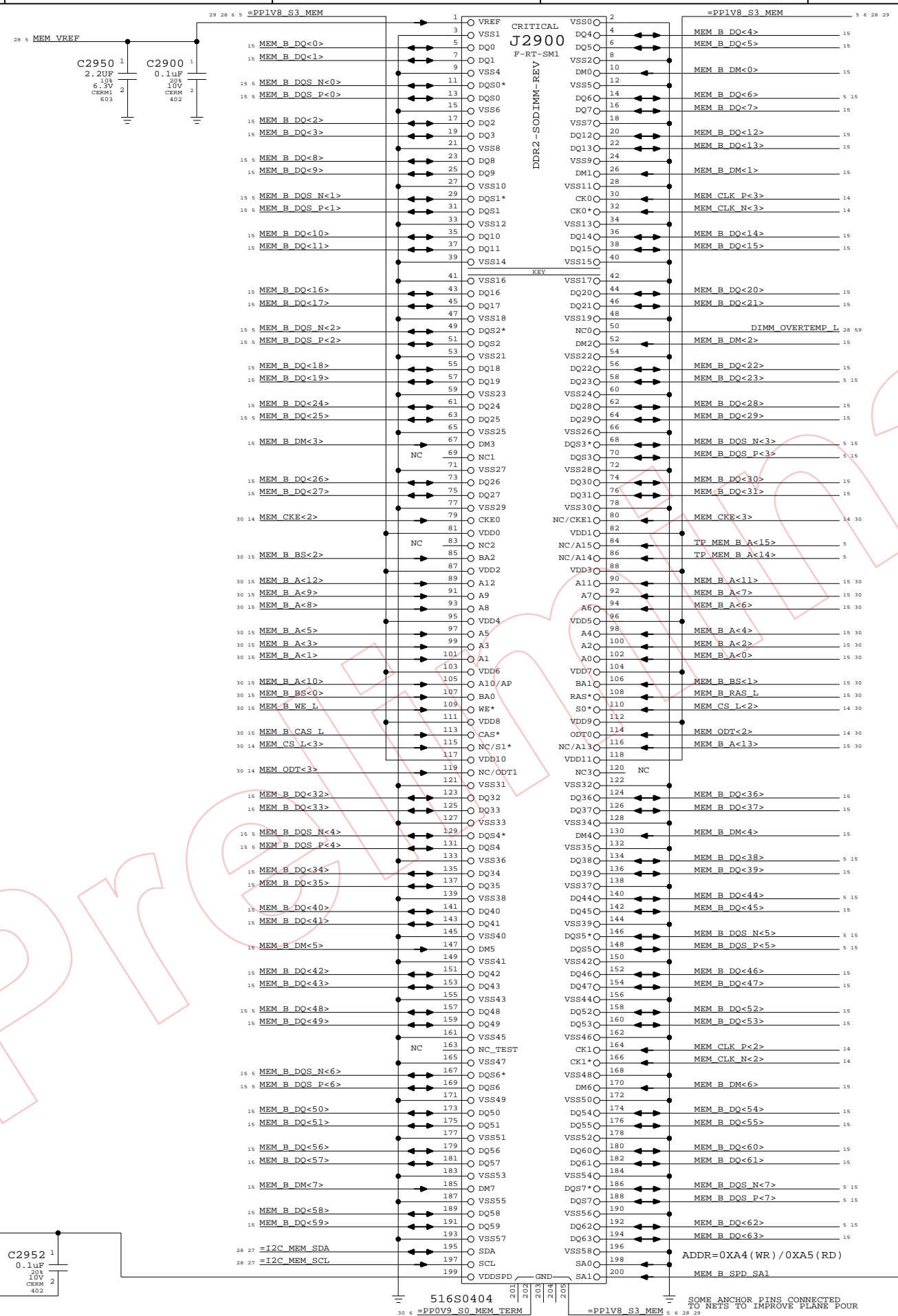
Page Notes

Power aliases required by this page:
 - =PP1V8_S3_MEM
 - =PPSPD_S0_MEM (2.5V - 3.3V)

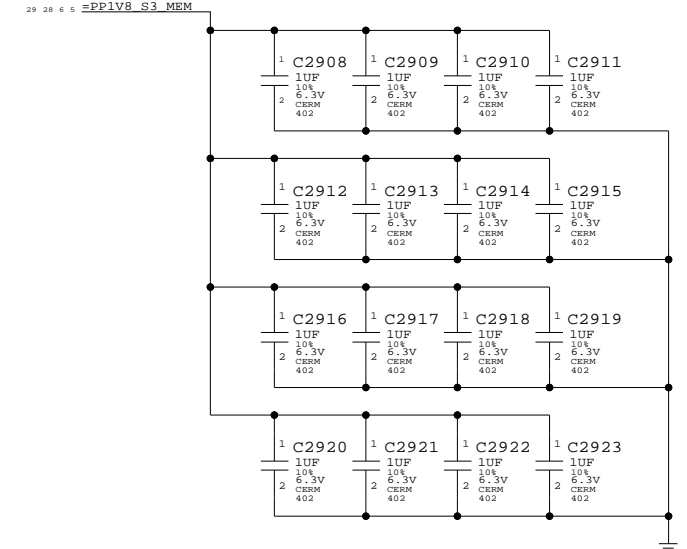
Signal aliases required by this page:
 - =I2C_MEM_SCL
 - =I2C_MEM_SDA

BOM options provided by this page:
 (NONE)

NOTE: This page does not supply VREF.
 The reference voltage must be provided by another page.



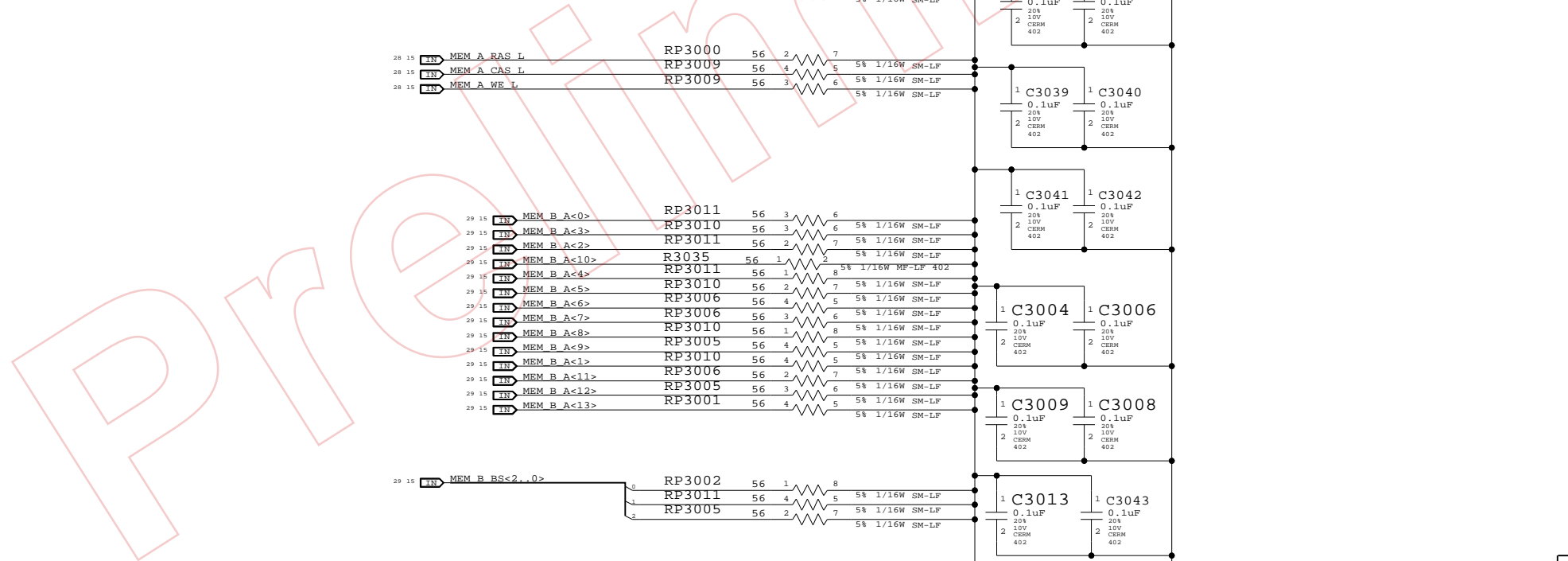
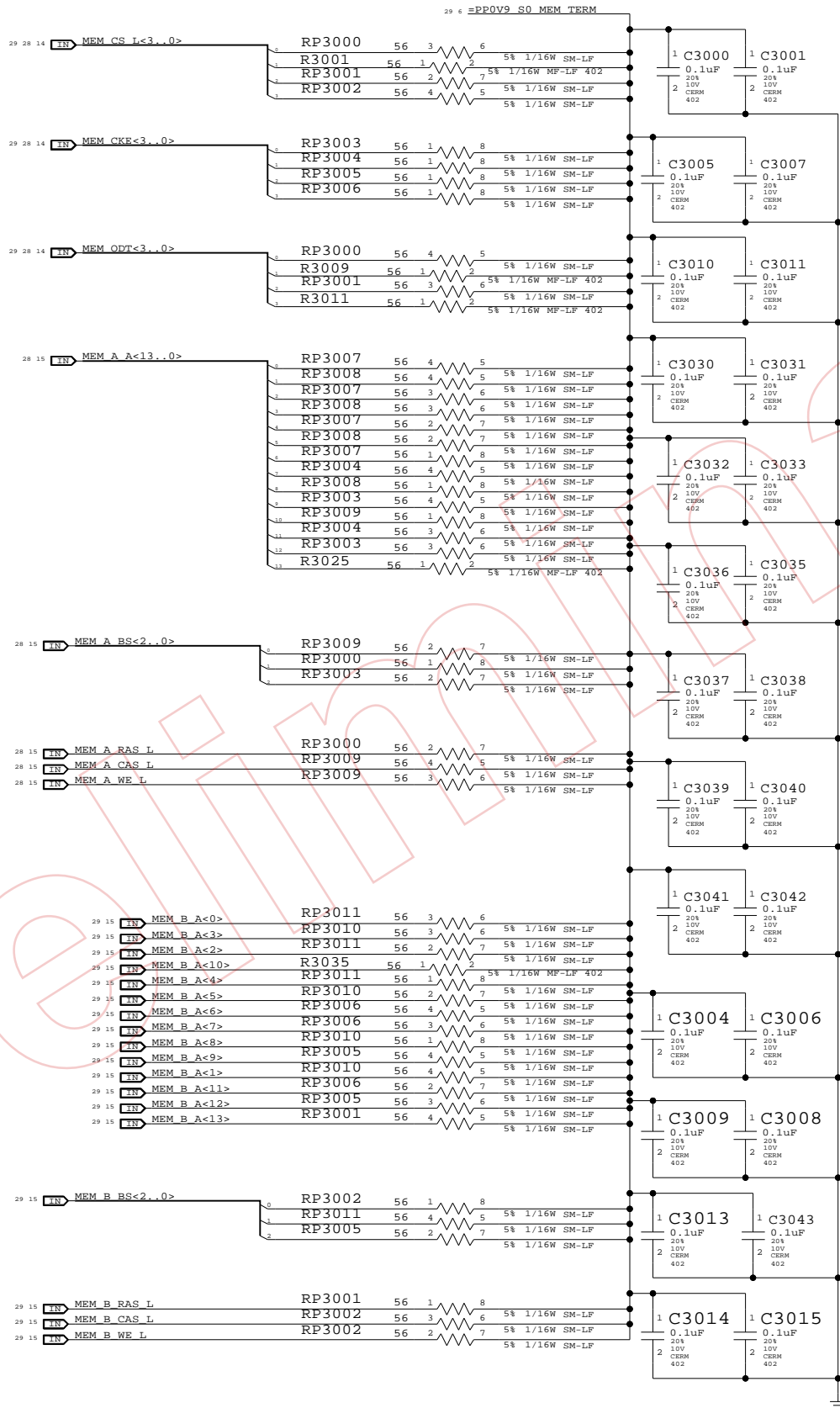
DDR2 Bypass Caps (For return current)



DDR2 SO-DIMM Connector B	
SYNC_MASTER=MASTER	SYNC_DATE=MASTER
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	A
SCALE	SHT	29 OF	97
NONE			

One cap for each side of every RPAK, one cap for every two discrete resistors
BOMOPTION shown at the top of each group applies to every part below it



Memory Active Termination

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	D	051-7199	A
SCALE	SHT	OF	
NONE	30	97	

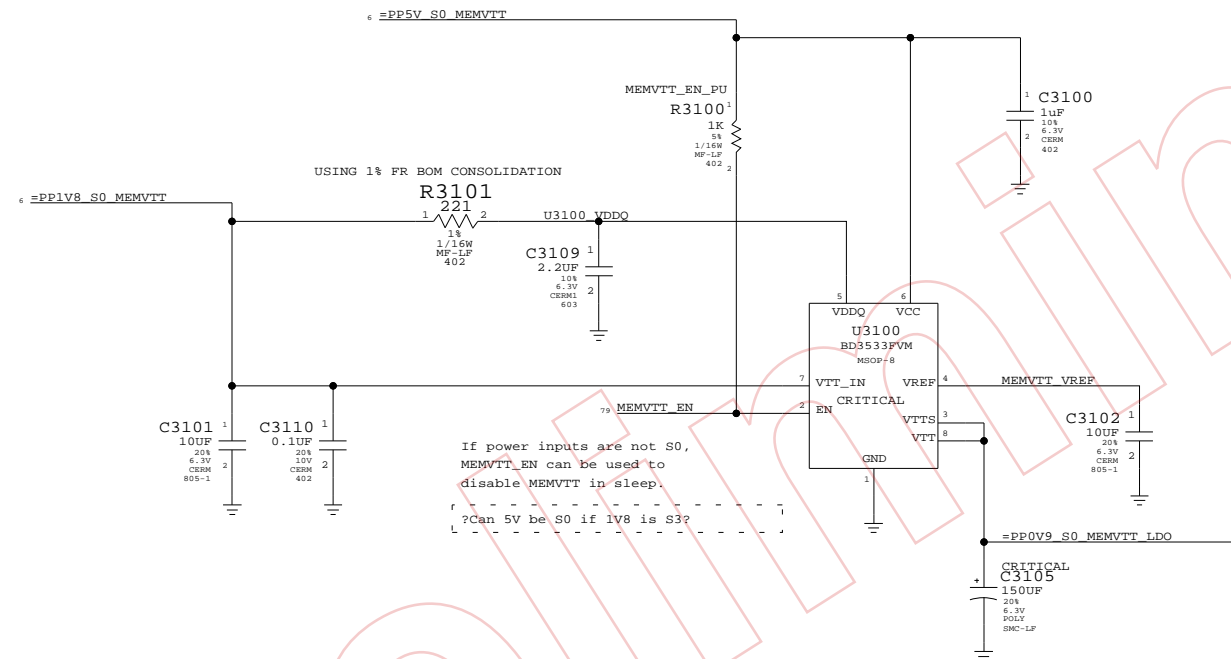
Page Notes

Power aliases required by this page:
 - =PP5V_S0_MEMVTT
 - =PP1V8_S0_MEMVTT
 - =PP0V9_S0_MEMVTT_LDO

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

DDR2 Vtt Regulator



Pre-Announcement

Memory Vtt Supply

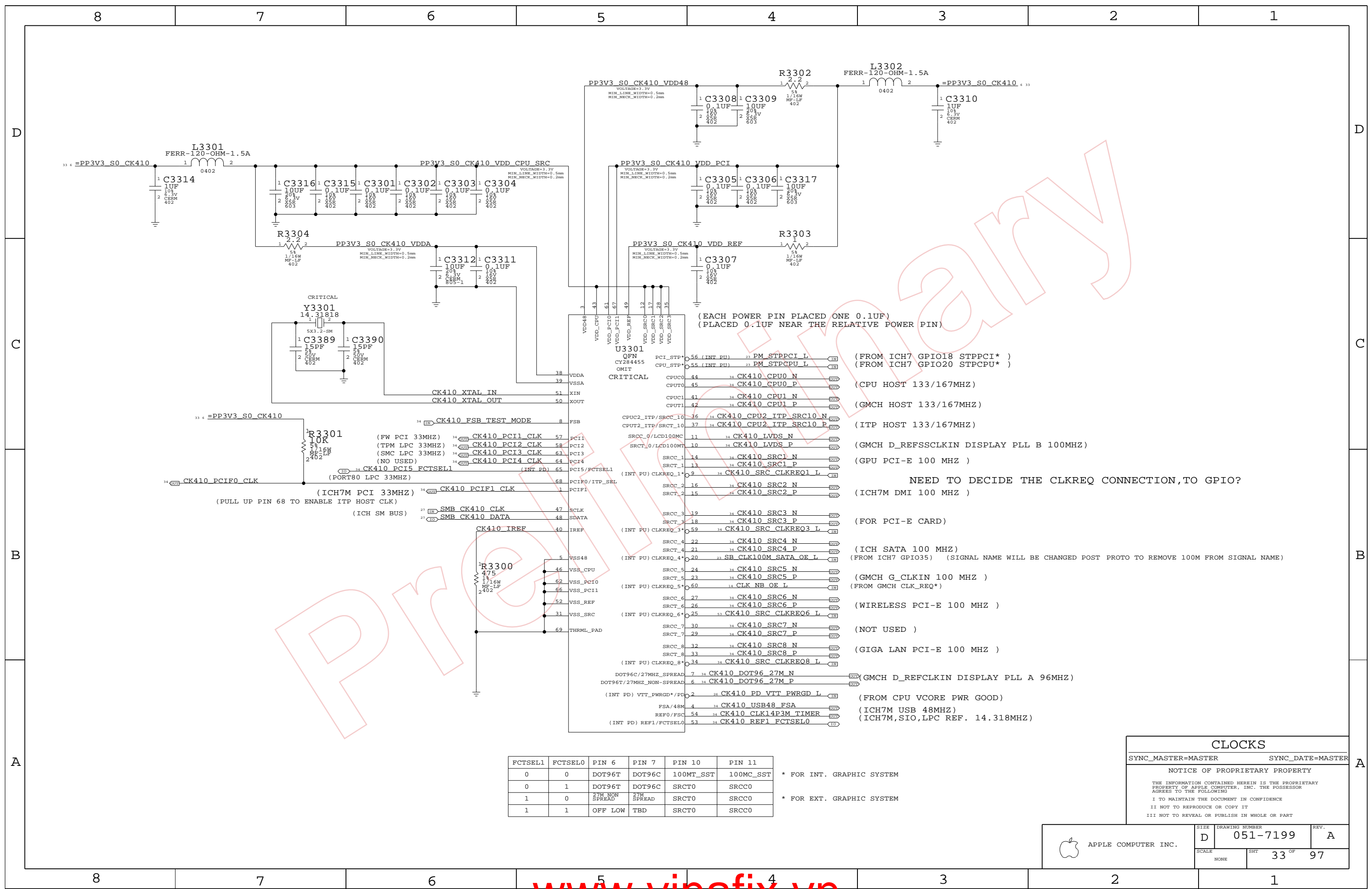
SYNC_MASTER=MASTER SYNC_DATE=MASTER

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7199	REV. A
	SCALE NONE	SHEET 31 OF 97	



(EACH POWER PIN PLACED ONE 0.1UF)
(PLACED 0.1UF NEAR THE RELATIVE POWER PIN)

- 56 (INT PU) 23 PM_STPPCI L (FROM ICH7 GPIO18 STPPCI*)
- 55 (INT PU) 23 PM_STPCPU L (FROM ICH7 GPIO20 STPCPU*)
- 44 34 CK410 CPU0 N (CPU HOST 133/167MHZ)
- 45 34 CK410 CPU0 P
- 41 34 CK410 CPU1 N (GMCH HOST 133/167MHZ)
- 42 34 CK410 CPU1 P
- 36 34 CK410 CPU2 ITP_SRC10_N (ITP HOST 133/167MHZ)
- 37 34 CK410 CPU2 ITP_SRC10_P
- 11 34 CK410 LVDS N (GMCH D_REFSSCLKIN DISPLAY PLL B 100MHZ)
- 10 34 CK410 LVDS P
- 14 34 CK410 SRC1 N (GPU PCI-E 100 MHZ)
- 13 34 CK410 SRC1 P
- 9 34 CK410 SRC_CLKREQ1 L (NEED TO DECIDE THE CLKREQ CONNECTION, TO GPIO?)
- 16 34 CK410 SRC2 N (ICH7M DMI 100 MHZ)
- 15 34 CK410 SRC2 P
- 19 34 CK410 SRC3 N (FOR PCI-E CARD)
- 18 34 CK410 SRC3 P
- 59 34 CK410 SRC_CLKREQ3 L
- 22 34 CK410 SRC4 N (ICH SATA 100 MHZ)
- 21 34 CK410 SRC4 P (FROM ICH7 GPIO35) (SIGNAL NAME WILL BE CHANGED POST PROTO TO REMOVE 100M FROM SIGNAL NAME)
- 20 34 SB_CLK100M_SATA_OE L
- 24 34 CK410 SRC5 N (GMCH G_CLKIN 100 MHZ)
- 23 34 CK410 SRC5 P (FROM GMCH CLK_REQ*)
- 60 34 CLK_NB_OE L
- 27 34 CK410 SRC6 N (WIRELESS PCI-E 100 MHZ)
- 26 34 CK410 SRC6 P
- 25 34 CK410 SRC_CLKREQ6 L
- 30 34 CK410 SRC7 N (NOT USED)
- 29 34 CK410 SRC7 P
- 32 34 CK410 SRC8 N (GIGA LAN PCI-E 100 MHZ)
- 33 34 CK410 SRC8 P
- 34 34 CK410 SRC_CLKREQ8 L
- 7 34 CK410 DOT96 27M N (GMCH D_REFCLKIN DISPLAY PLL A 96MHZ)
- 6 34 CK410 DOT96 27M P
- 2 34 CK410 PD_VTT_PWRGD L (FROM CPU VCORE PWR GOOD)
- 4 34 CK410 USB48_FSA (ICH7M USB 48MHZ)
- 54 34 CK410_CLK14P3M_TIMER (ICH7M, SIO, LPC REF. 14.318MHZ)
- 53 34 CK410_REF1_FCTSEL0

FCTSEL1	FCTSEL0	PIN 6	PIN 7	PIN 10	PIN 11
0	0	DOT96T	DOT96C	100MT_SST	100MC_SST
0	1	DOT96T	DOT96C	SRCT0	SRCC0
1	0	27M_NON_SPREAD	27M_SPREAD	SRCT0	SRCC0
1	1	OFF_LOW	TBD	SRCT0	SRCC0

* FOR INT. GRAPHIC SYSTEM
* FOR EXT. GRAPHIC SYSTEM

CLOCKS

SYNC_MASTER=MASTER SYNC_DATE=MASTER

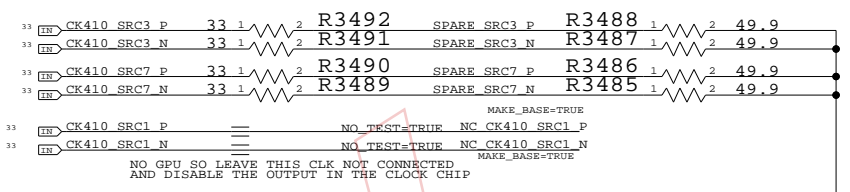
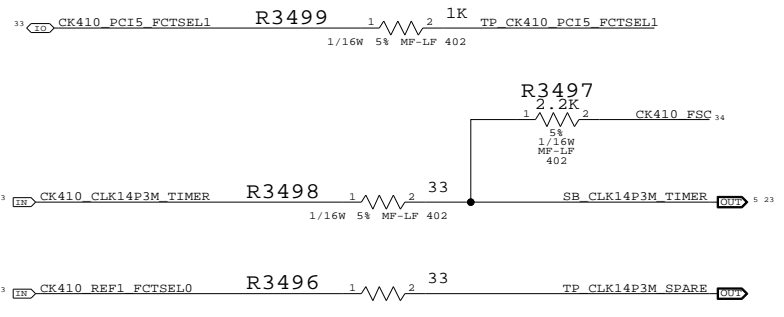
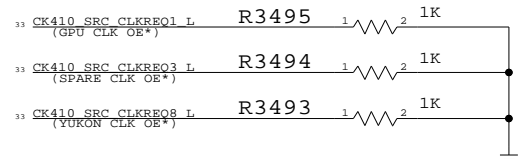
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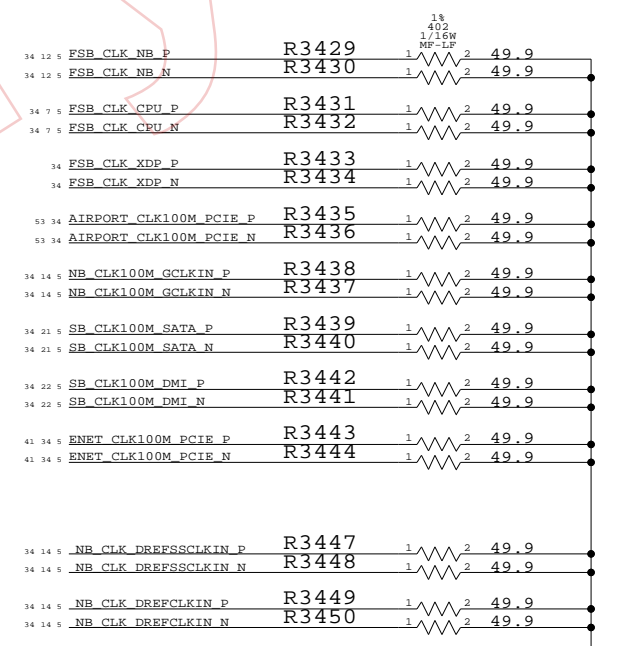
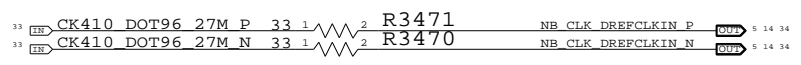
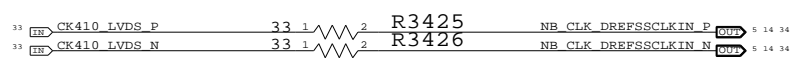
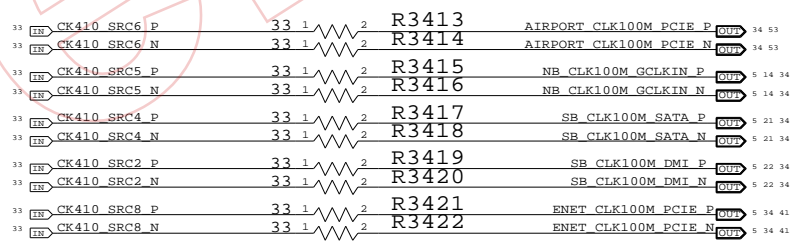
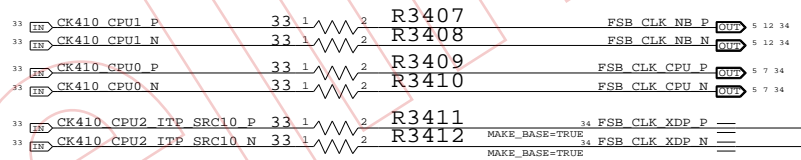
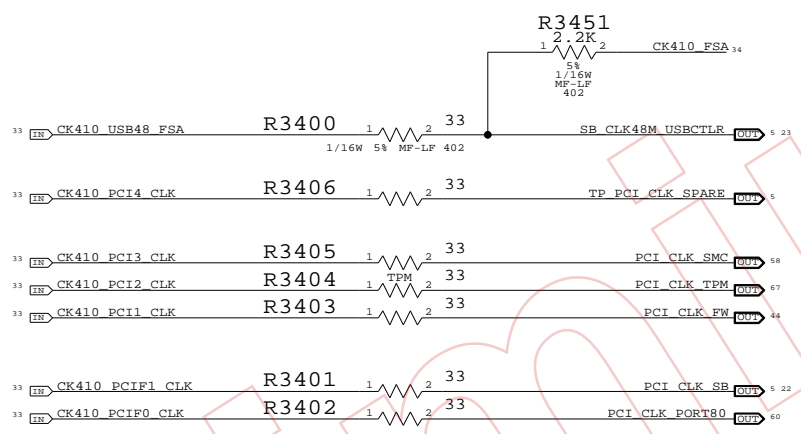
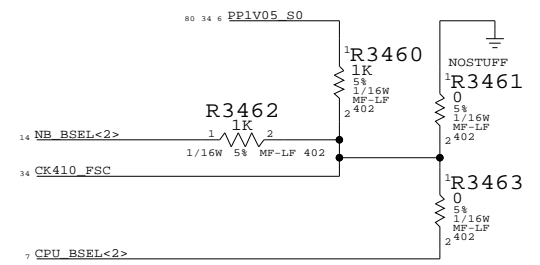
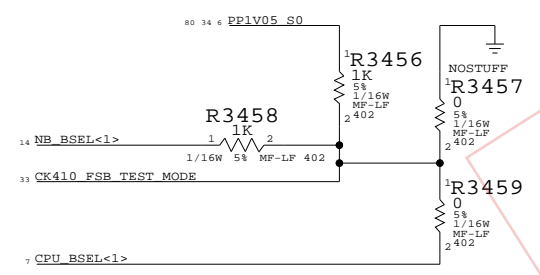
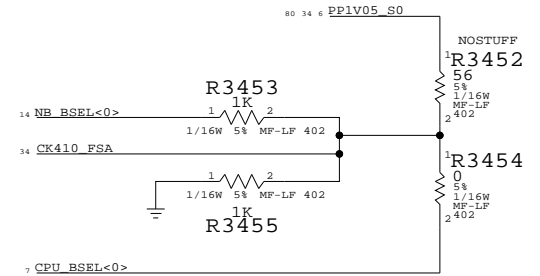
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	A
SCALE	SHT	33 OF 97	
NONE			

NOTE: USE THESE PULL-DOWNS IF NOT CONNECTED TO GPIO'S



FSB FREQUENCY SELECT:

	STUFF	NO STUFF
CPU DRIVEN	R3453 R3454 R3455	R3452 R3456 R3457
533MHZ (133MHZ CPU CLK)	R3453 R3454 R3455	R3452 R3456 R3457
667MHZ (166MHZ CPU CLK)	R3452 R3456 R3457	R3453 R3454 R3455



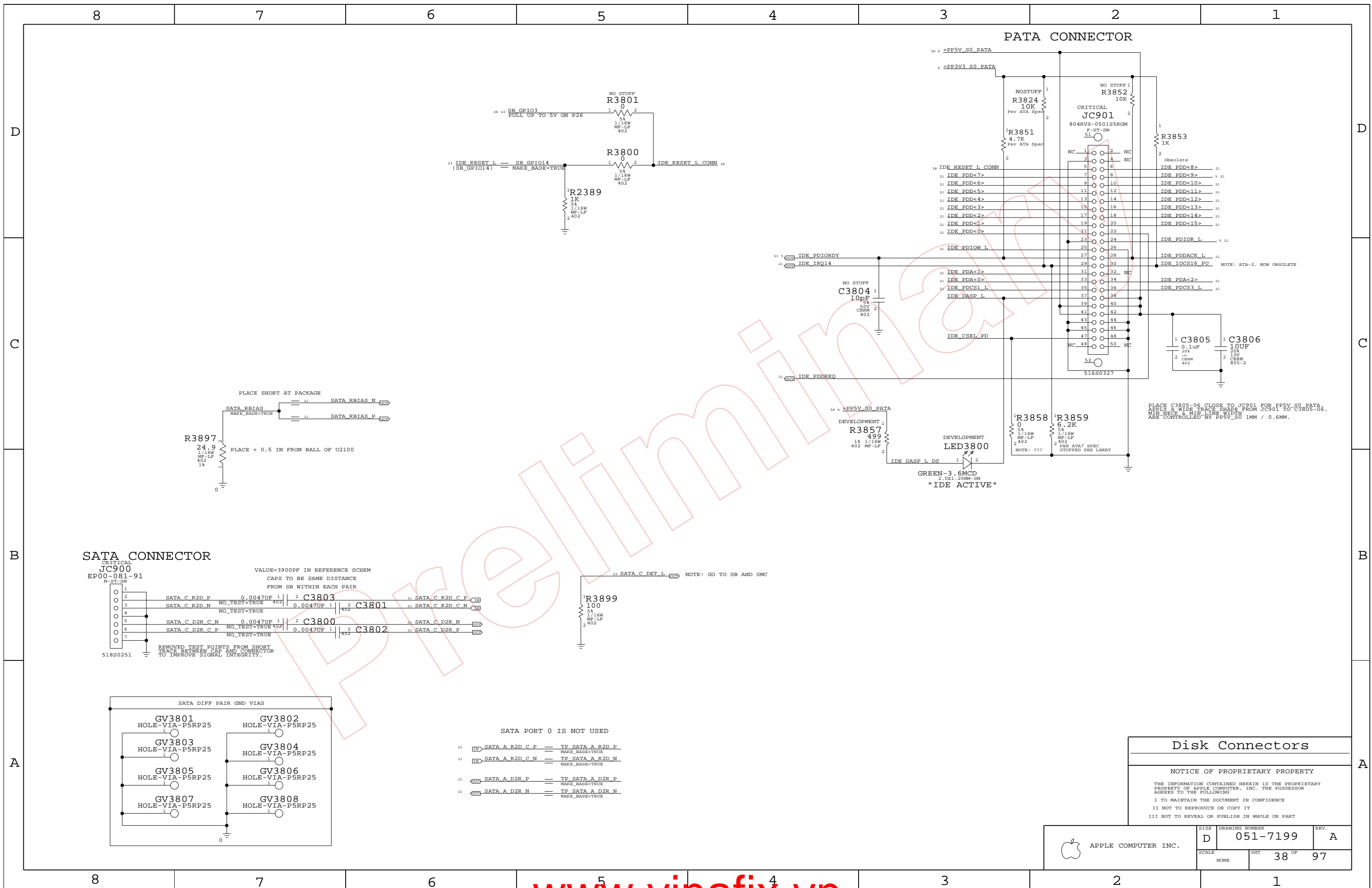
CLOCKS : TERMINATIONS

SYNC_MASTER=MASTER SYNC_DATE=MASTER

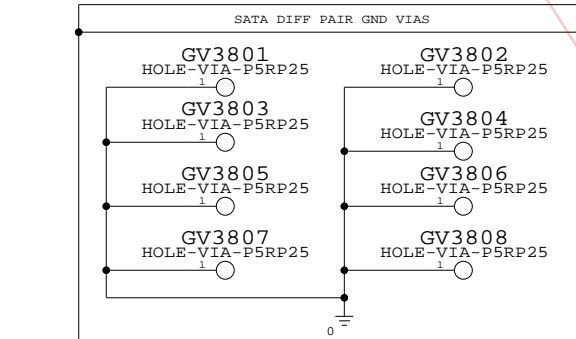
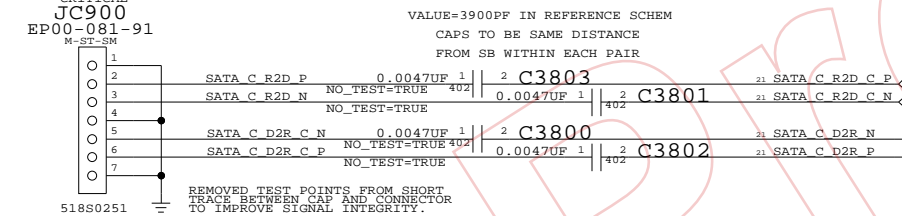
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	D	051-7199	A
SCALE	SHT	34 OF	97
NONE			



SATA CONNECTOR



- SATA PORT 0 IS NOT USED
- TP SATA A R2D P MAKE_BASE=TRUE
 - TP SATA A R2D N MAKE_BASE=TRUE
 - TP SATA A D2R P MAKE_BASE=TRUE
 - TP SATA A D2R N MAKE_BASE=TRUE

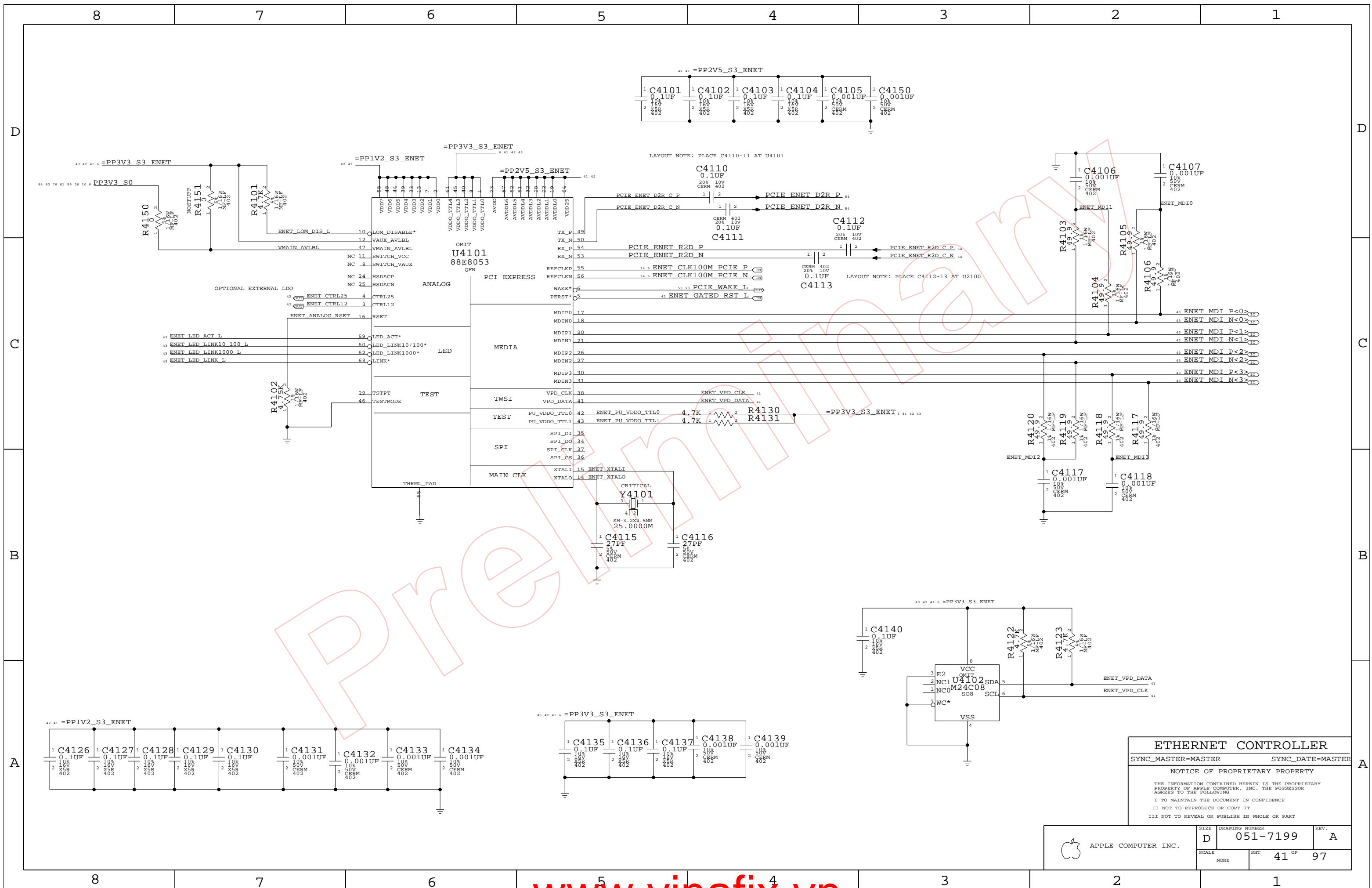
Disk Connectors

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	D	051-7199	A
SCALE	SHT	38 OF 97	
NONE			



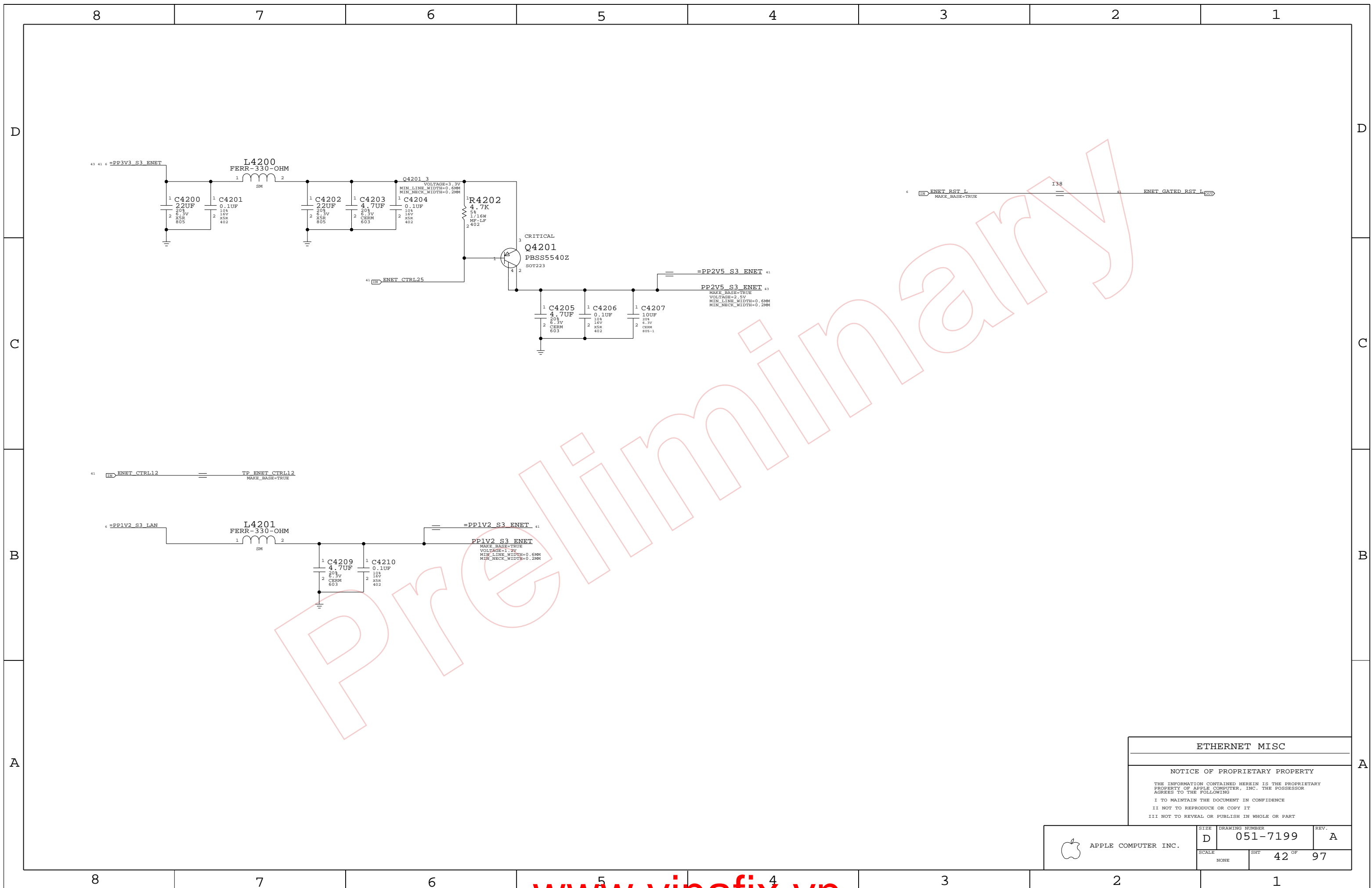
ETHERNET CONTROLLER

SYNC_MASTER=MASTER SYNC_DATA=MASTER

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7199	REV. A
	SCALE NONE	SHEET 41 OF 97	



Preliminary

ETHERNET MISC

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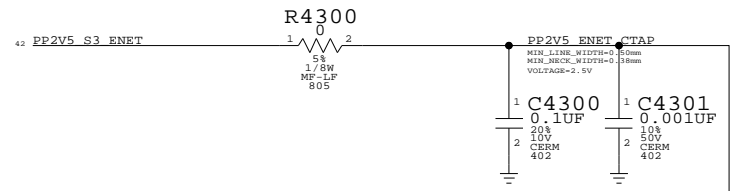
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	D	DRAWING NUMBER	051-7199	REV.	A
	SCALE	NONE	SHEET	42 OF 97		

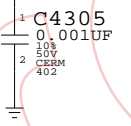
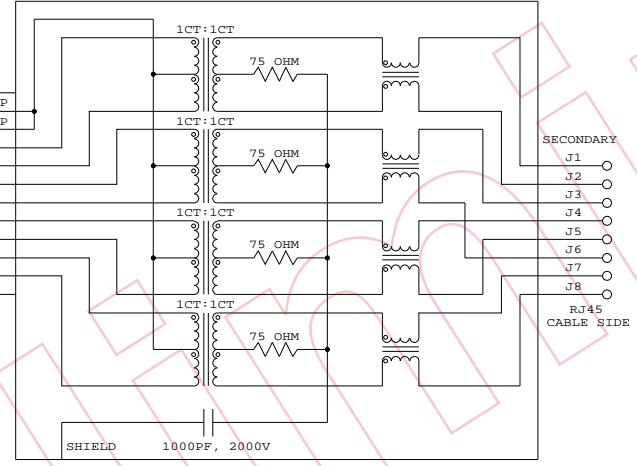
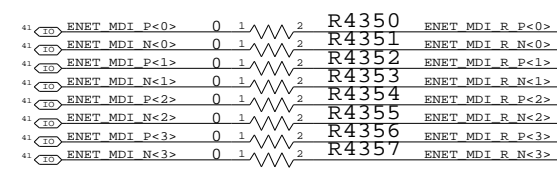
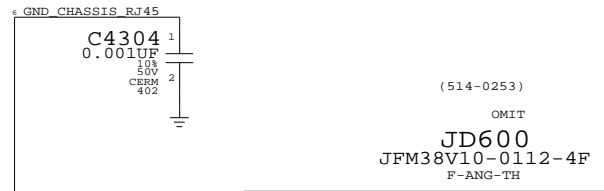
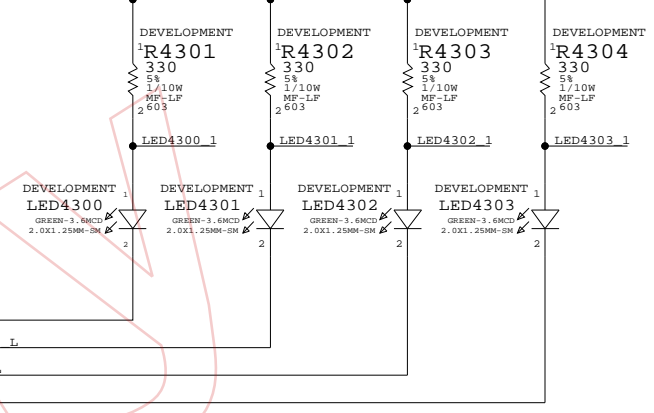
8 7 6 5 4 3 2 1

D
C
B
A

RESISTOR PADS USED AS PLACEHOLDER FOR INDUCTOR IF NEEDED



42 41 6 =PP3V3_S3_ENET



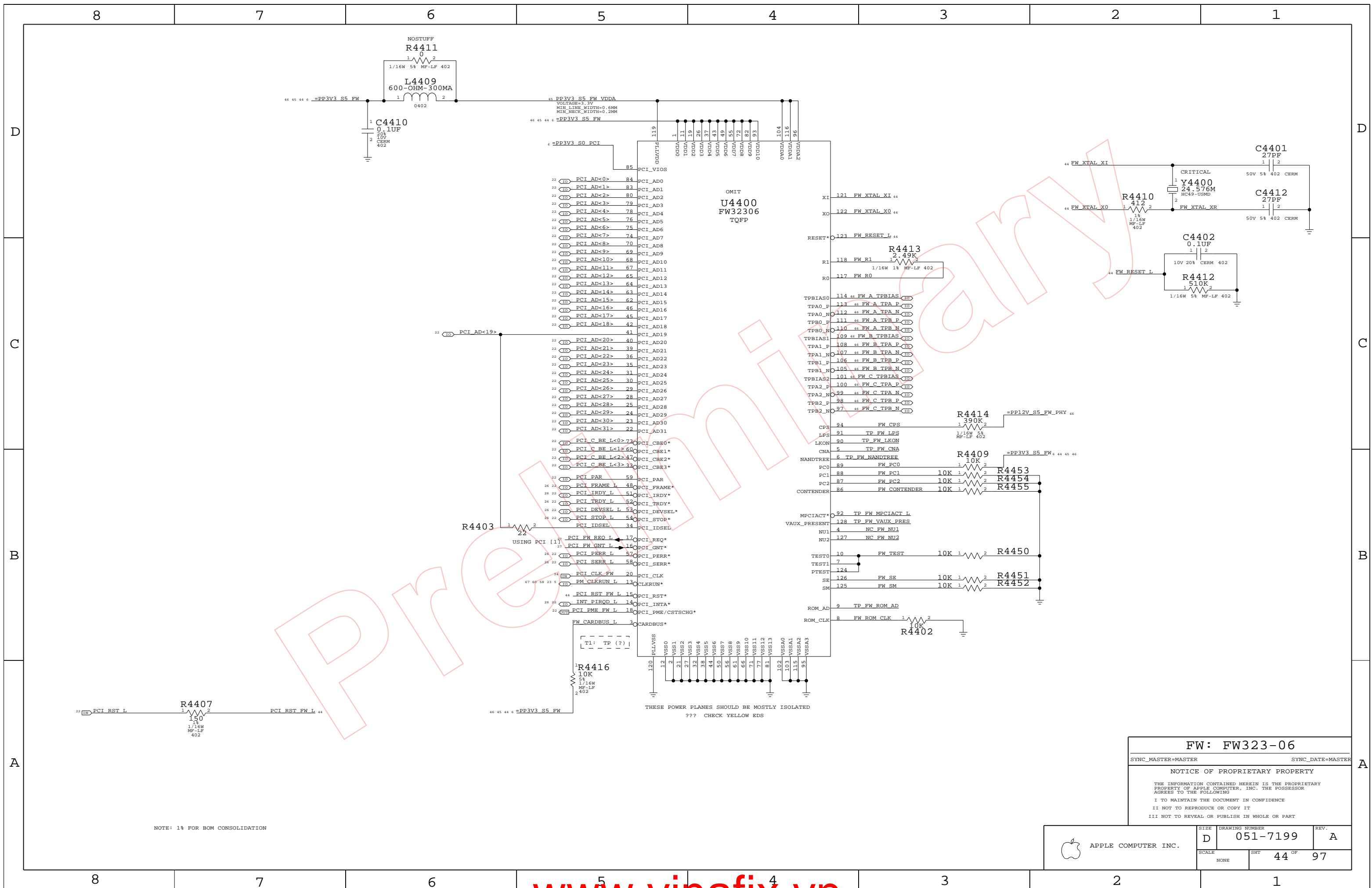
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0365	1	CON,RJ-45 7 DEGRESS, 243DEG C	JD600	CRITICAL	17_INCH_LCD

ETHERNET CONNECTOR

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	D	051-7199	A
SCALE	SHT	43 OF 97	
NONE			

8 7 6 5 4 3 2 1



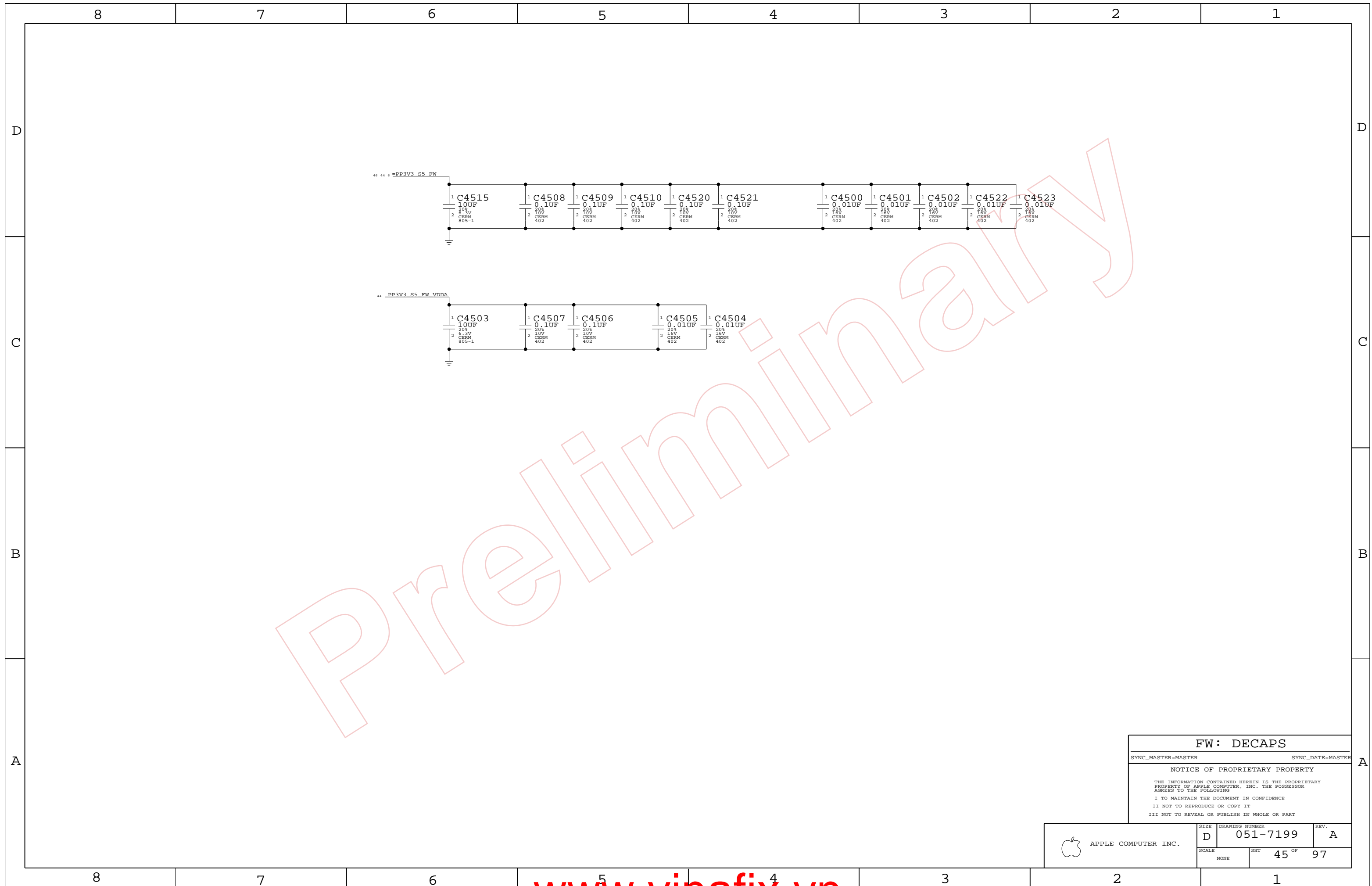
PRELIMINARY

THESE POWER PLANES SHOULD BE MOSTLY ISOLATED
 ??? CHECK YELLOW EDS

NOTE: 1% FOR BOM CONSOLIDATION

FW: FW323-06	
SYNC_MASTER=MASTER	SYNC_DATE=MASTER
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	SCALE NONE	SHEET 44 OF 97	



Preliminary

FW: DECAPS

SYNC_MASTER=MASTER SYNC_DATE=MASTER

NOTICE OF PROPRIETARY PROPERTY

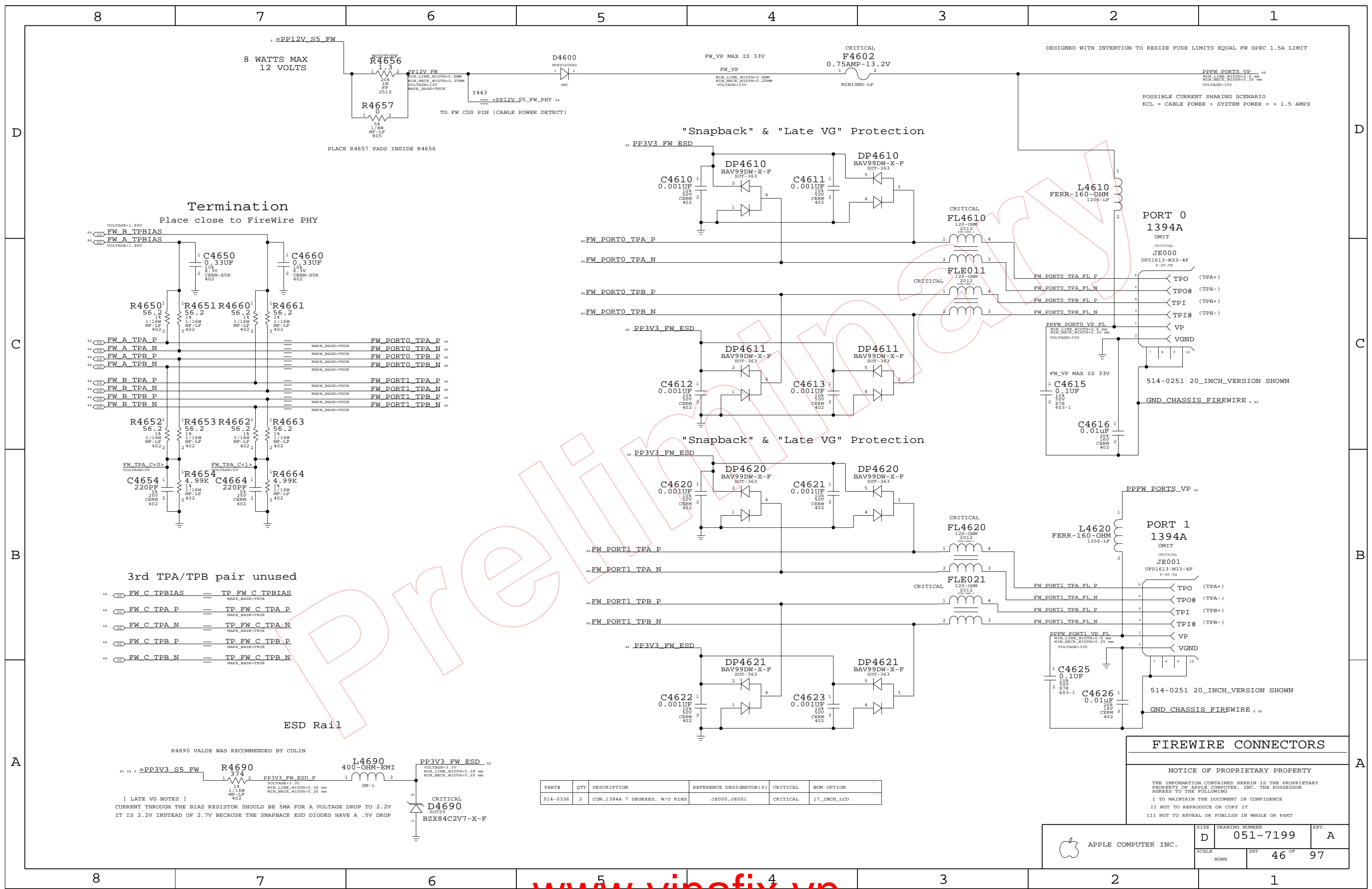
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APPLE COMPUTER INC.	SIZE	D	DRAWING NUMBER	051-7199	REV.	A
	SCALE	NONE	SHT	45 OF 97		



Termination
Place close to FireWire PHY

"Snapback" & "Late VG" Protection

"Snapback" & "Late VG" Protection

3rd TPA/TPB pair unused

ESD Rail

FIREWIRE CONNECTORS

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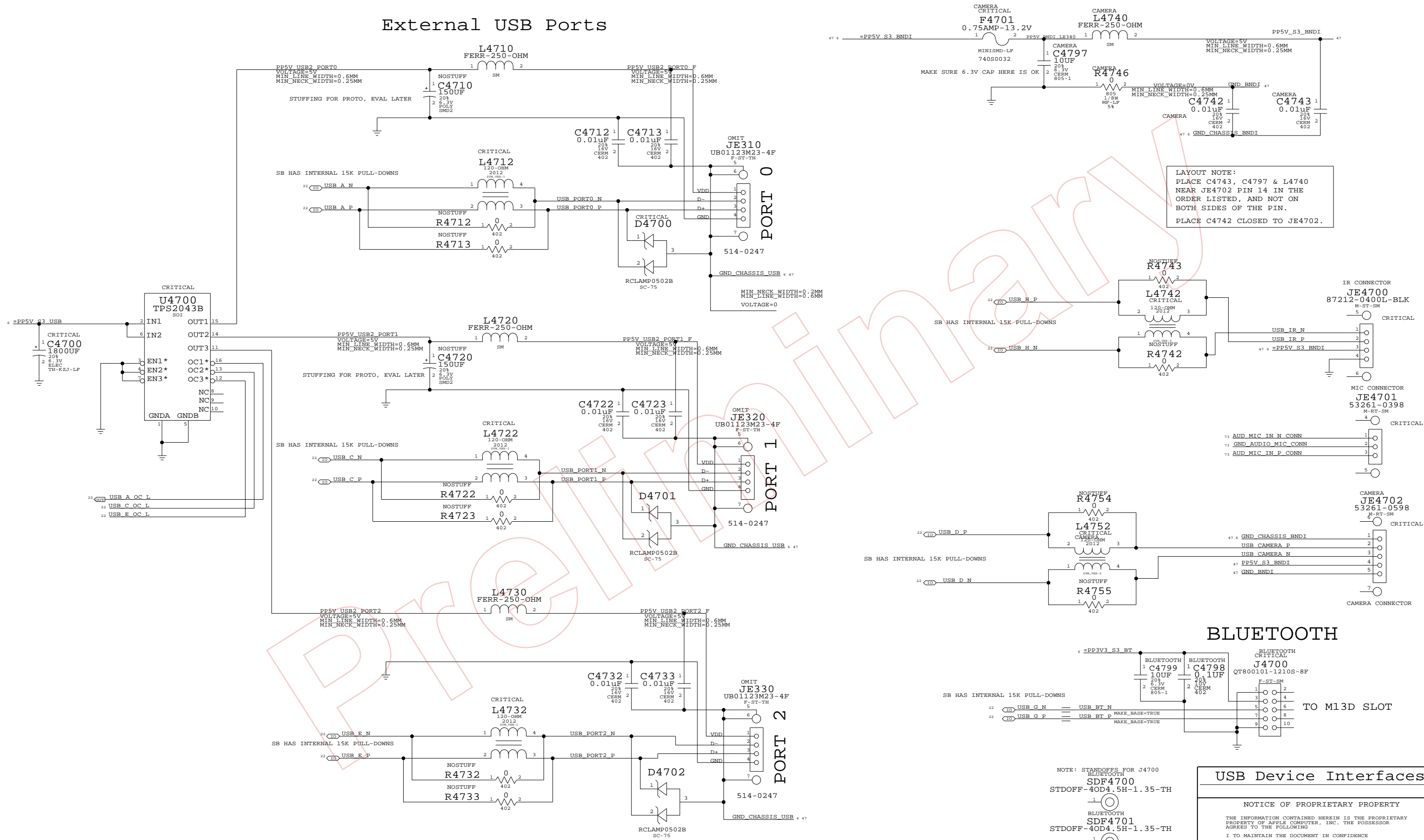
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0336	2	CON,1394A 7 DEGREES, W/O RIBS	JE000,JE001	CRITICAL	17_INCH_LCD

APPLE COMPUTER INC.

SCALE: NONE SHEET: 46 OF 97

DRAWING NUMBER: 051-7199 REV: A

External USB Ports



LAYOUT NOTE:
 PLACE C4743, C4797 & L4740
 NEAR JE4702 PIN 14 IN THE
 ORDER LISTED, AND NOT ON
 BOTH SIDES OF THE PIN.
 PLACE C4742 CLOSED TO JE4702.

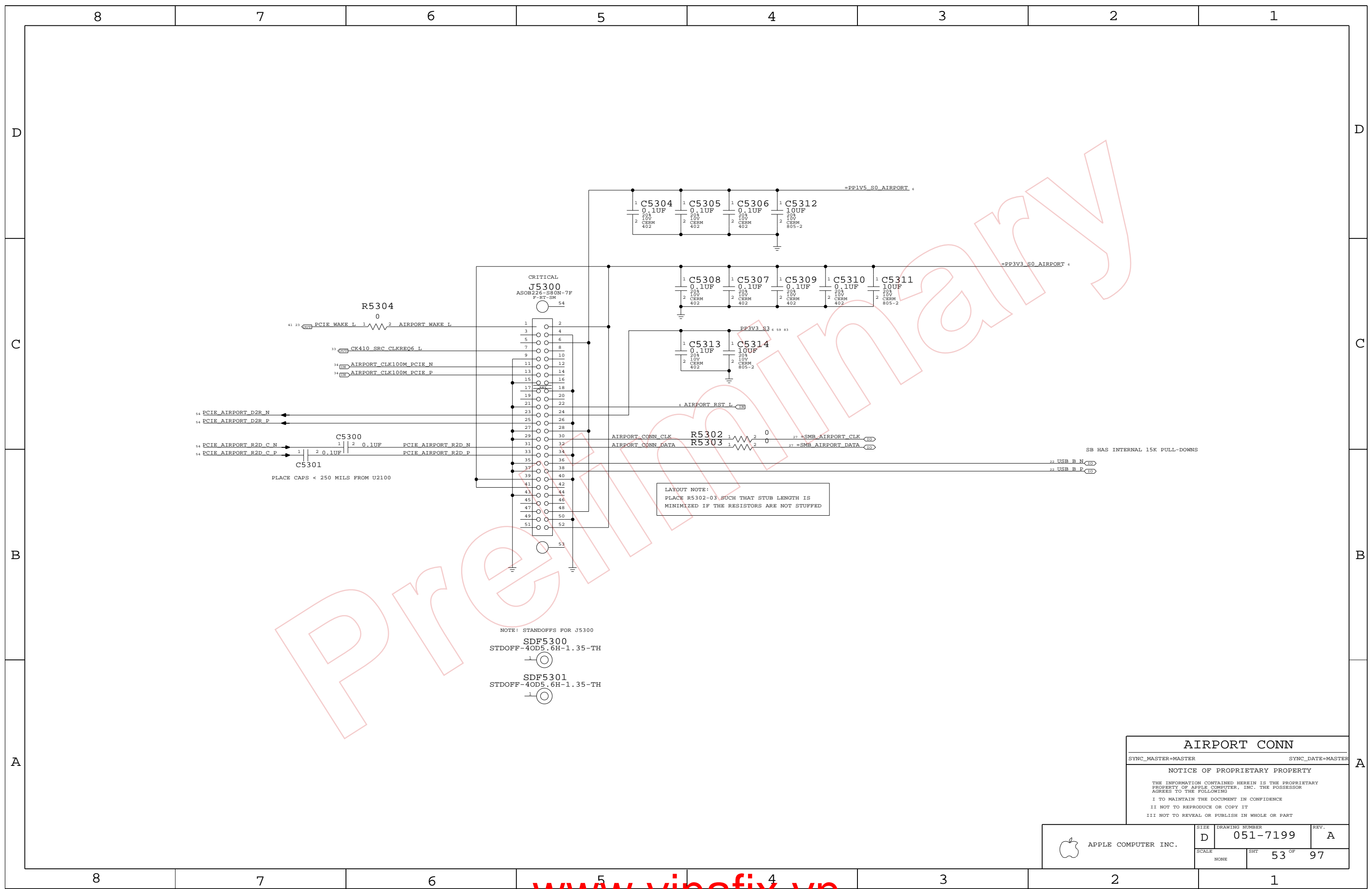
BLUETOOTH

USB Device Interfaces



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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0339	3	USB RECEPTACLE, 4P, UB1123-M50-4F	JE310, JE320, JE330	CRITICAL	17_INCH_LCD

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	A
SCALE	SHT	47 OF 97	
NONE			



PROTECTED

NOTE: STANDOFFS FOR J5300
 SDF5300
 STDOFF-40D5.6H-1.35-TH

 SDF5301
 STDOFF-40D5.6H-1.35-TH


LAYOUT NOTE:
 PLACE R5302-03 SUCH THAT STUB LENGTH IS
 MINIMIZED IF THE RESISTORS ARE NOT STUFFED

SB HAS INTERNAL 15K PULL-DOWNS

AIRPORT CONN

SYNC_MASTER=MASTER SYNC_DATE=MASTER


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 APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7199	REV. A
	SCALE NONE	SHEET 53 OF 97	

8

7

6

5

4

3

2

1

D

D

C

C

B

B

A

A

22 PCIE C R2D C N == TP PCIE C R2D C N
MAKE_BASE=TRUE

22 PCIE C R2D C P == TP PCIE C R2D C P
MAKE_BASE=TRUE

22 PCIE C D2R N == TP PCIE C D2R N
MAKE_BASE=TRUE

22 PCIE C D2R P == TP PCIE C D2R P
MAKE_BASE=TRUE

22 PCIE D R2D C N == TP PCIE D R2D C N
MAKE_BASE=TRUE

22 PCIE D R2D C P == TP PCIE D R2D C P
MAKE_BASE=TRUE

22 PCIE D D2R N == TP PCIE D D2R N
MAKE_BASE=TRUE

22 PCIE D D2R P == TP PCIE D D2R P
MAKE_BASE=TRUE

22 PCIE E R2D C N == TP PCIE E R2D C N
MAKE_BASE=TRUE

22 PCIE E R2D C P == TP PCIE E R2D C P
MAKE_BASE=TRUE

22 PCIE E D2R N == TP PCIE E D2R N
MAKE_BASE=TRUE

22 PCIE E D2R P == TP PCIE E D2R P
MAKE_BASE=TRUE

22 PCIE F R2D C N == TP PCIE F R2D C N
MAKE_BASE=TRUE

22 PCIE F R2D C P == TP PCIE F R2D C P
MAKE_BASE=TRUE

22 PCIE F D2R N == TP PCIE F D2R N
MAKE_BASE=TRUE

22 PCIE F D2R P == TP PCIE F D2R P
MAKE_BASE=TRUE

USED PCIE PORTS

22 PCIE A R2D C N == PCIE AIRPORT R2D C N 53
MAKE_BASE=TRUE

22 PCIE A R2D C P == PCIE AIRPORT R2D C P 53
MAKE_BASE=TRUE

22 5 PCIE A D2R N == PCIE AIRPORT D2R N 53
MAKE_BASE=TRUE

22 5 PCIE A D2R P == PCIE AIRPORT D2R P 53
MAKE_BASE=TRUE

22 PCIE B R2D C N == PCIE ENET R2D C N 41
MAKE_BASE=TRUE

22 PCIE B R2D C P == PCIE ENET R2D C P 41
MAKE_BASE=TRUE

22 5 PCIE B D2R N == PCIE ENET D2R N 41
MAKE_BASE=TRUE

22 5 PCIE B D2R P == PCIE ENET D2R P 41
MAKE_BASE=TRUE

PCIE PORT ALIASES

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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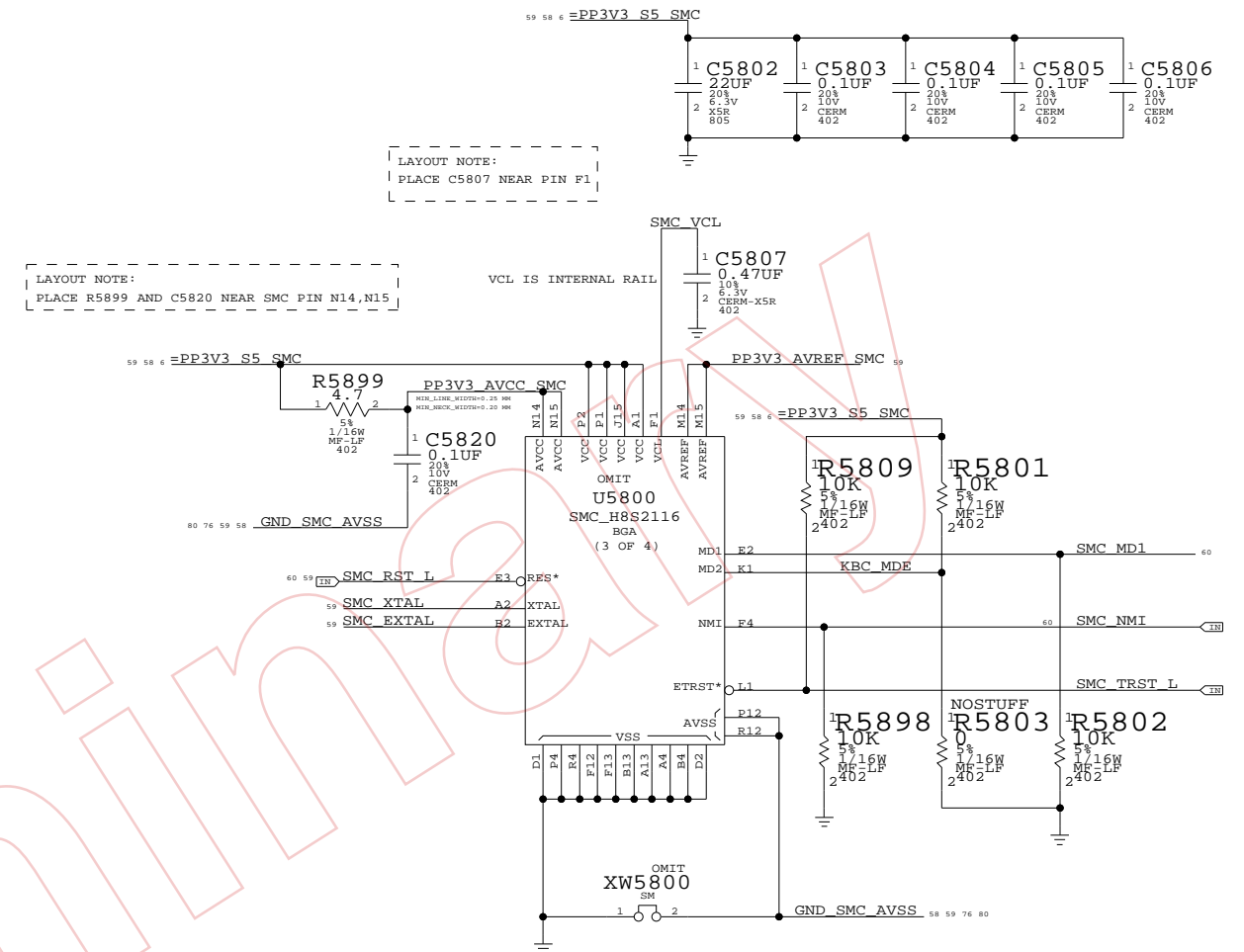
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	A
SCALE	SHT	54 OF 97	
NONE			

UNUSED PINS HAVE THE FORMAT SMC_XXX WHERE XXX IS THE PORT NUMBER. THEY ARE SET BY SOFTWARE TO BE DRIVEN OUTPUTS ALWAYS SO THEY CAN BE LEFT NO-CONNECTED.

SMC_H8S2116 (1 OF 4)		SMC_H8S2116 (2 OF 4)	
PM LAN ENABLE	B12 P10	PA0/KIN8*/PA2DC	PR0 M3 SMC CASE OPEN
SMC_RSTGATE_L	C13 P11	PA1/KIN9*/PA2DD	PR1*/ETCK M2 SMC TCK
ALL_SYS_PWRGD	A15 P12	PA2/KIN10*/PS2AC	PR2*/ETDI M1 SMC TDI
RSMRST_PWRGD	B14 P13	PA3/KIN11*/PS2AD	PR3*/ETDO L4 SMC TDO
SMC_SB_NMI	B15 P14	PA4/KIN12*/PS2BC	PR4*/ETMS L2 SMC TMS
PM_RSMRST_L	C14 P15	PA5/KIN13*/PS2BD	PF0/IRQ8*/PWM2 M7 SMC PF0
IMVP_VR_ON	D12 P16	PA6/KIN14*/PS2CC	PF1/IRQ9*/PWM3 P6 SMC PF1
PM_PWRBTN_L	C15 P17	PA7/KIN15*/PS2CD	PF2/IRQ10*/TMOY R6 SMC LID
SMC_P20	D13 P20	PB0/LSMI*	PF3/IRQ11*/TMOX N6 SMC CPU RESET 3 3 L
SMC_P21	D14 P21	PB1/LSCI	PF4/PWM4 M6 SMC BATT ISET
SMC_P22	D15 P22	PB2	PF5/PWM5 R5 SMC BATT VSET
SMC_P23	E12 P23	PB3	PF6/PWM6 P5 SMC SYS ISET
SMC_BATT_TRICKLE_EN_L	E14 P24	PB4	PF7/PWM7 N5 SMC SYS VSET
SMC_BATT_CHG_EN	E15 P25	PB5	PG0/EXIRQ8*/TMIX P9 SMC PROCHOT
SMC_P26	E13 P26	PB6	PG1/EXIRQ9*/TMIX R9 SMC XDP TCK 3 3
SMC_P27	F14 P27	PB7	PG2/EXIRQ10*/SDA2 N9 SMC BSA DATA
LPC_AD<0>	D9 P30/LAD0	PC0/TIOCA0/WUE8*	PG3/EXIRQ11*/SCL2 P8 SMC BSA CLK
LPC_AD<1>	C9 P31/LAD1	PC1/TIOCB0/WUE9*	PG4/EXIRQ12*/EXSDAA R8 SMC BSA S3 DATA
LPC_AD<2>	A9 P32/LAD2	PC2/TIOCC0/TCLKA/WUE10*	PG5/EXIRQ13*/EXSCLA M8 SMC BSA S3 CLK
LPC_AD<3>	B9 P33/LAD3	PC3/TIOCD0/TCLKB/WUE11*	PG6/EXIRQ14*/EXSDAB R7 SMC B S0 DATA
LPC_FRAME_L	D8 P34/LFRAME*	PC4/TIOCA1/WUE12*	PG7/EXIRQ15*/EXSCLB R7 SMC B S0 CLK
SMC_LRESET_L	C8 P35/LRESET*	PC5/TIOCB1/TCLKC/WUE13*	PH0/EXIRQ6* R1 SMC PROCHOT
PCI_CLK_SMC	A8 P36/LCLK	PC6/TIOCA2/WUE14*	PH1/EXIRQ7* R2 SMC THRMTRIP
INT_SERIRQ	D7 P37/SERIRQ	PC7/TIOCB2/TCLKD/WUE15*	PH2/FWE K2 SMC FWE
SMC_XDP_TMS	A5 P40/TMIO	PD0/AN8	PH3/EXEXCL C4 SMC ALS GAIN
SMC_SYS_LED_16B	B5 P41/TMO0	PD1/AN9	PH4 D4 SMC INT L
SMB_BSB_DATA	D5 P42/SDA1	PD2/AN10	PH5 B3 SMC ONOFF L
SMC_TPM_PP	C3 P43/TMI1/EXSCK1	PD3/AN11	
SMC_XDP_TRST_L	B1 P44/TMO1	PD4/AN12	
SMC_XDP_TCK	C2 P45	PD5/AN13	
SMC_SYS_LED	D3 P46/PWX0/PWM0	PD6/AN14	
SMC_SYS_KBDLED	C1 P47/PWX1/PWM1	PD7/AN15	
SMC_TX_L	G1 P50		
SMC_RX_L	G4 P51		
SMB_0_S0_CLK	F2 P52/SCL0		

SMC_H8S2116 (2 OF 4)		SMC_H8S2116 (3 OF 4)	
SMC_RCIN_L	R3 PA0/KIN8*/PA2DC	SMC_CASE_OPEN	PR0 M3
BOOT_LPC_SPI_L	P3 PA1/KIN9*/PA2DD	SMC_TCK	PR1*/ETCK M2
PM_SYSRST_L	R2 PA2/KIN10*/PS2AC	SMC_TDI	PR2*/ETDI M1
SMC_TPM_RESET_L	N3 PA3/KIN11*/PS2AD	SMC_TDO	PR3*/ETDO L4
PM_EXTRIS_L	R1 PA4/KIN12*/PS2BC	SMC_TMS	PR4*/ETMS L2
PM_THRM_L	N2 PA5/KIN13*/PS2BD	SMC_PF0	PF0/IRQ8*/PWM2 M7
SYS_ONEWIRE	M4 PA6/KIN14*/PS2CC	SMC_PF1	PF1/IRQ9*/PWM3 P6
PM_BATLOW_L	N1 PA7/KIN15*/PS2CD	SMC_LID	PF2/IRQ10*/TMOY R6
SMC_EXTSMI_L	B10 PB0/LSMI*	SMC_CPU_RESET_3_3_L	PF3/IRQ11*/TMOX N6
SMC_RUNTIME_SCI_L	A10 PB1/LSCI	SMC_BATT_ISET	PF4/PWM4 M6
SMC_ODD_DETECT	D10 PB2	SMC_BATT_VSET	PF5/PWM5 R5
ISENSE_CAL_EN	A11 PB3	SMC_SYS_ISET	PF6/PWM6 P5
SMC_EXCARD_CP	B11 PB4	SMC_SYS_VSET	PF7/PWM7 N5
SMC_EXCARD_PWR_EN	C11 PB5	SPI_CE_L	PG0/EXIRQ8*/TMIX P9
SMC_EXCARD_OC_L	A12 PB6	SMC_XDP_TCK_3_3	PG1/EXIRQ9*/TMIX R9
SMC_XDP_TDO_3_3	D11 PB7	SMB_BSA_DATA	PG2/EXIRQ10*/SDA2 N9
SMC_FAN_0_CTL	G14 PC0/TIOCA0/WUE8*	SMB_BSA_CLK	PG3/EXIRQ11*/SCL2 P8
SMC_FAN_1_CTL	G15 PC1/TIOCB0/WUE9*	SMB_A_S3_DATA	PG4/EXIRQ12*/EXSDAA R8
SMC_FAN_2_CTL	G13 PC2/TIOCC0/TCLKA/WUE10*	SMB_A_S3_CLK	PG5/EXIRQ13*/EXSCLA M8
SMC_FAN_3_CTL	G12 PC3/TIOCD0/TCLKB/WUE11*	SMB_B_S0_DATA	PG6/EXIRQ14*/EXSDAB R7
SMC_FAN_0_TACH	H14 PC4/TIOCA1/WUE12*	SMB_B_S0_CLK	PG7/EXIRQ15*/EXSCLB R7
SMC_FAN_1_TACH	H15 PC5/TIOCB1/TCLKC/WUE13*	SMC_PROCHOT	PH0/EXIRQ6* R1
SMC_FAN_2_TACH	H13 PC6/TIOCA2/WUE14*	SMC_THRMTRIP	PH1/EXIRQ7* R2
SMC_FAN_3_TACH	H12 PC7/TIOCB2/TCLKD/WUE15*	SMC_FWE	PH2/FWE K2
SMS_X_AXIS	M11 PD0/AN8	SMC_ALS_GAIN	PH3/EXEXCL C4
SMS_Y_AXIS	P11 PD1/AN9	SMC_INT_L	PH4 D4
SMS_Z_AXIS	R11 PD2/AN10	SMC_ONOFF_L	PH5 B3
SMC_ANALOG_ID	N11 PD3/AN11		
SMC_NB_ISENSE	P10 PD4/AN12		
SMC_MEM_ISENSE	R10 PD5/AN13		
ALS_LEFT	N10 PD6/AN14		
ALS_RIGHT	M10 PD7/AN15		

SMC_H8S2116 (4 OF 4)	
NC0	E15
NC1	A14
NC2	C12
NC3	C10
NC4	C5
NC5	A3
NC6	B8
NC7	E4
NC8	H4
NC9	M9
NC10	H4
NC11	NC22
NC12	E15
NC13	A14
NC14	C12
NC15	C10
NC16	C5
NC17	A3
NC18	B8
NC19	E4
NC20	H4
NC21	M9
NC22	NC



SMC

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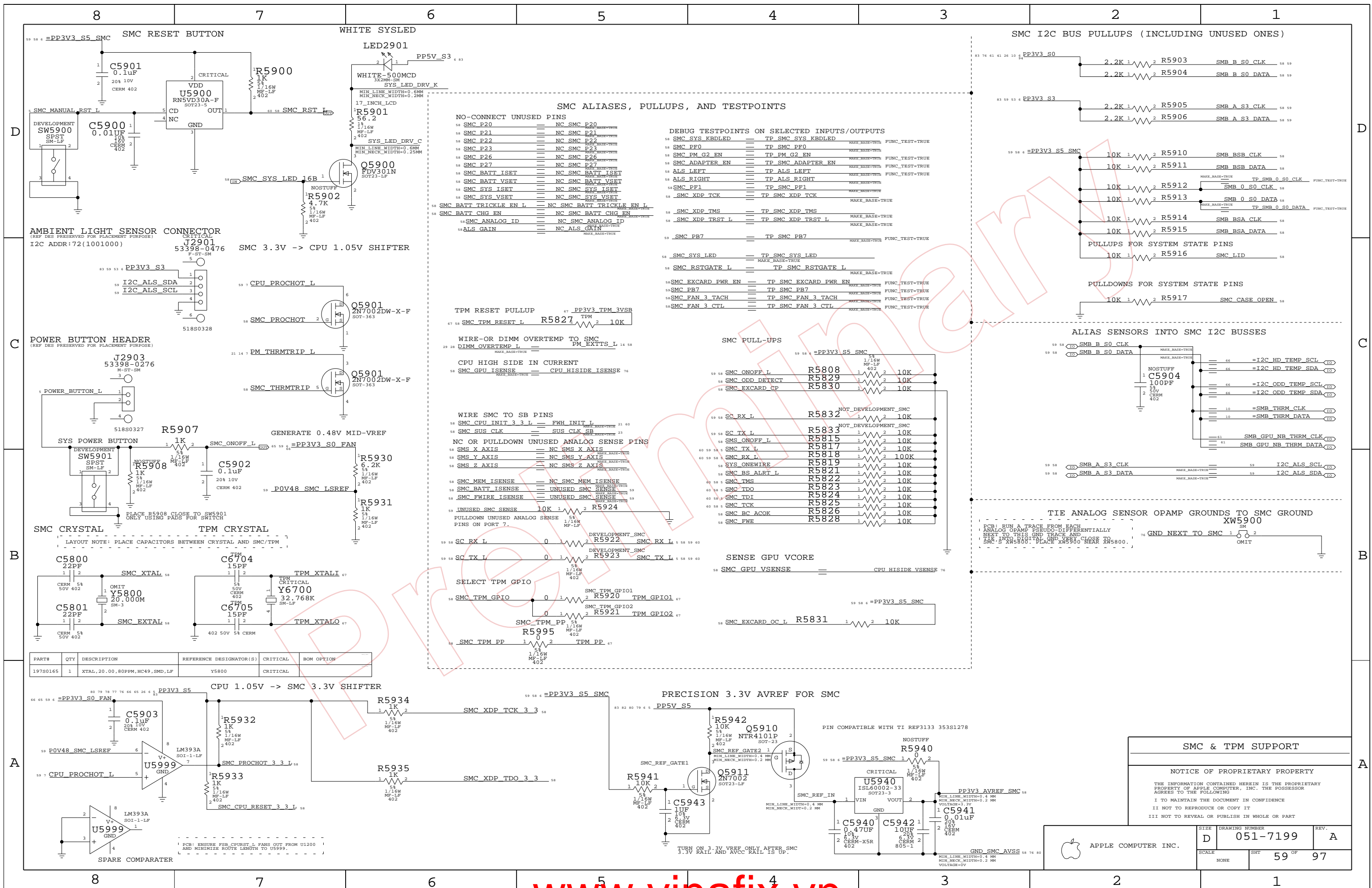
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	D	051-7199	A
SCALE	SHT	58 OF 97	
NONE			



SMC ALIASES, PULLUPS, AND TESTPOINTS

SMC Alias	TP Alias	MAKE_BASE=TRUE	FUNC_TEST=TRUE
NO-CONNECT UNUSED PINS			
SMC P20	NC SMC P20		
SMC P21	NC SMC P21		
SMC P22	NC SMC P22		
SMC P23	NC SMC P23		
SMC P26	NC SMC P26		
SMC P27	NC SMC P27		
SMC BATT ISET	NC SMC BATT ISET		
SMC BATT VSET	NC SMC BATT VSET		
SMC SYS ISET	NC SMC SYS ISET		
SMC SYS VSET	NC SMC SYS VSET		
SMC BATT TRICKLE EN L	NC SMC BATT TRICKLE EN L		
SMC BATT CHG EN	NC SMC BATT CHG EN		
SMC ANALOG ID	NC SMC ANALOG ID		
ALS GAIN	NC ALS GAIN		
SMC SYS LED	TP SMC SYS LED		
SMC RSTGATE L	TP SMC RSTGATE L		
SMC EXCARD PWR EN	TP SMC EXCARD PWR EN		
SMC PB7	TP SMC PB7		
SMC FAN 3 TACH	TP SMC FAN 3 TACH		
SMC FAN 3 CTL	TP SMC FAN 3 CTL		
SMC ONOFF L	R5808		
SMC ODD DETECT	R5829		
SMC EXCARD CP	R5830		
SC RX L	R5832		
SC TX L	R5833		
SMS ONOFF L	R5815		
SMC TX L	R5817		
SMC RX L	R5818		
SYS ONEWIRE	R5819		
SMC BS ALRT L	R5821		
SMC TMS	R5822		
SMC TDO	R5823		
SMC TDI	R5824		
SMC TCK	R5825		
SMC BC ACOK	R5826		
SMC FWE	R5828		
SMC GPU VSENSE	CPU HISIDE VSENSE		
SMC EXCARD OC L	R5831		
SMC CPU INIT 3 3 L	FWH INIT L		
SMC SUS CLK	SUS CLK SB		
NC OR PULLDOWN UNUSED ANALOG SENSE PINS			
SMS X AXIS	NC SMS X AXIS		
SMS Y AXIS	NC SMS Y AXIS		
SMS Z AXIS	NC SMS Z AXIS		
SMC MEM ISENSE	NC SMC MEM ISENSE		
SMC BATT ISENSE	UNUSED SMC BATT ISENSE		
SMC FWIRE ISENSE	UNUSED SMC FWIRE ISENSE		
UNUSED SMC SENSE	10K		
PULLDOWN UNUSED ANALOG SENSE PINS ON PORT 7			
SC RX L	R5922		
SC TX L	R5923		
SMC TPM GPIO	R5920		
SMC TPM GPIO2	R5921		
SMC TPM PP	R5995		
SMC TPM RESET L	R5827		
WIRE-OR DIMM OVERTEMP TO SMC DIMM OVERTEMP L	PM_EXITS_L		
CPU HIGH SIDE IN CURRENT			
SMC GPU ISENSE	CPU HISIDE ISENSE		

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0165	1	XTAL, 20.00, 80PPM, HC49, SMD, LF	Y5800	CRITICAL	

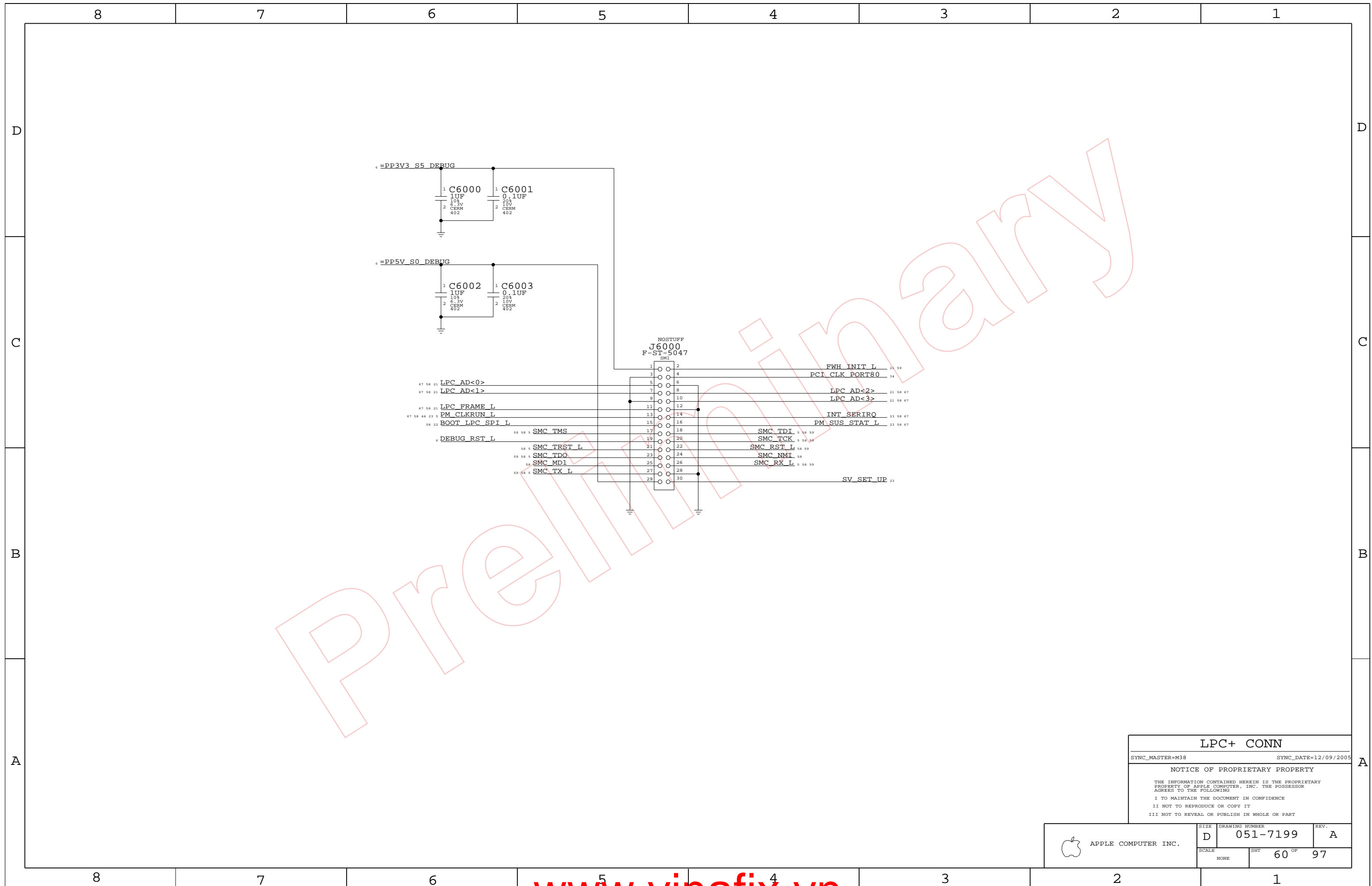
SMC & TPM SUPPORT

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SCALE	SHT	59 OF 97
NONE		



Pre-release material

LPC+ CONN

SYNC_MASTER=M38 SYNC_DATE=12/09/2005

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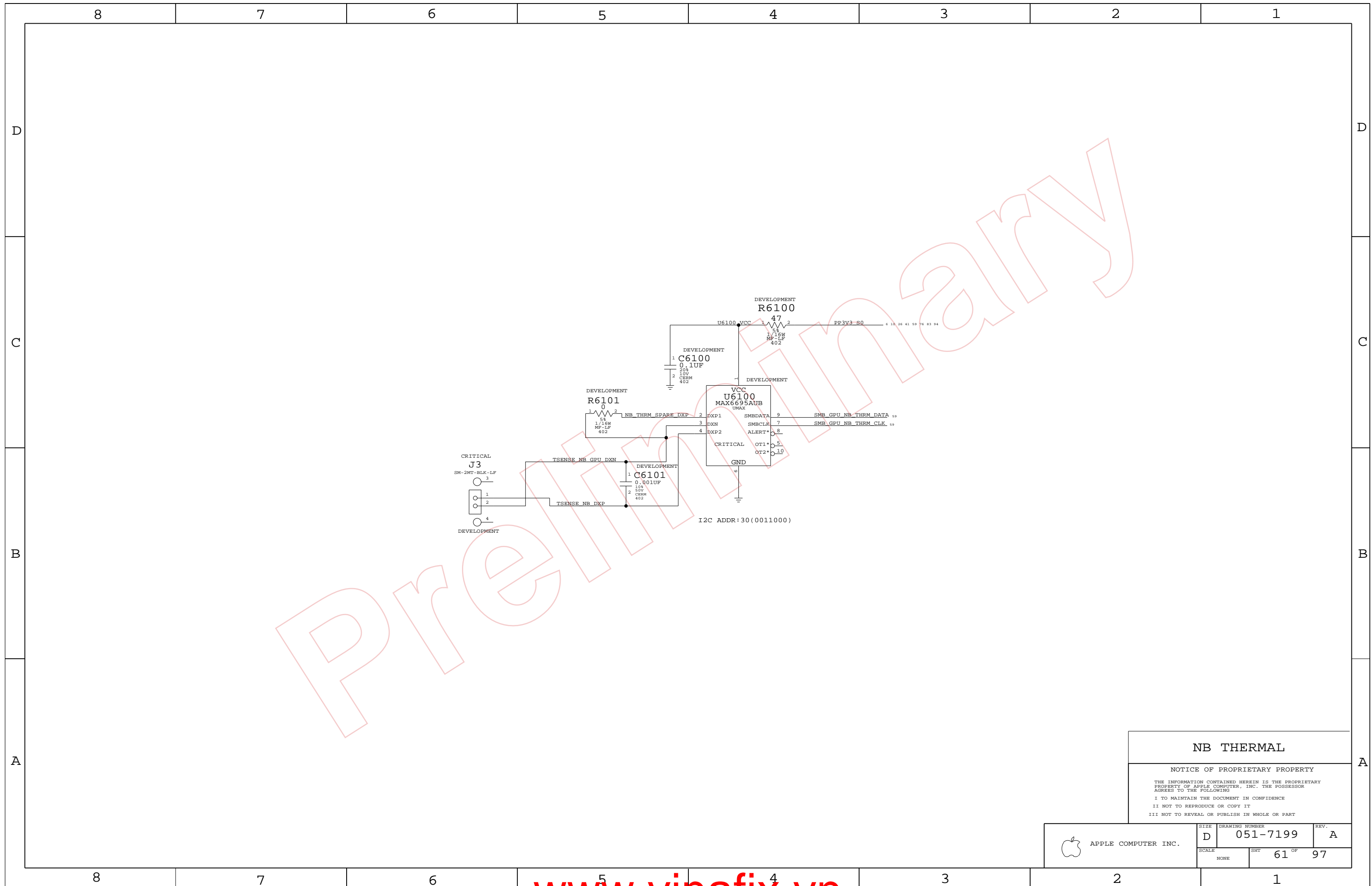
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SCALE		SHT	OF
NONE		60	97



Pre-release

NB THERMAL

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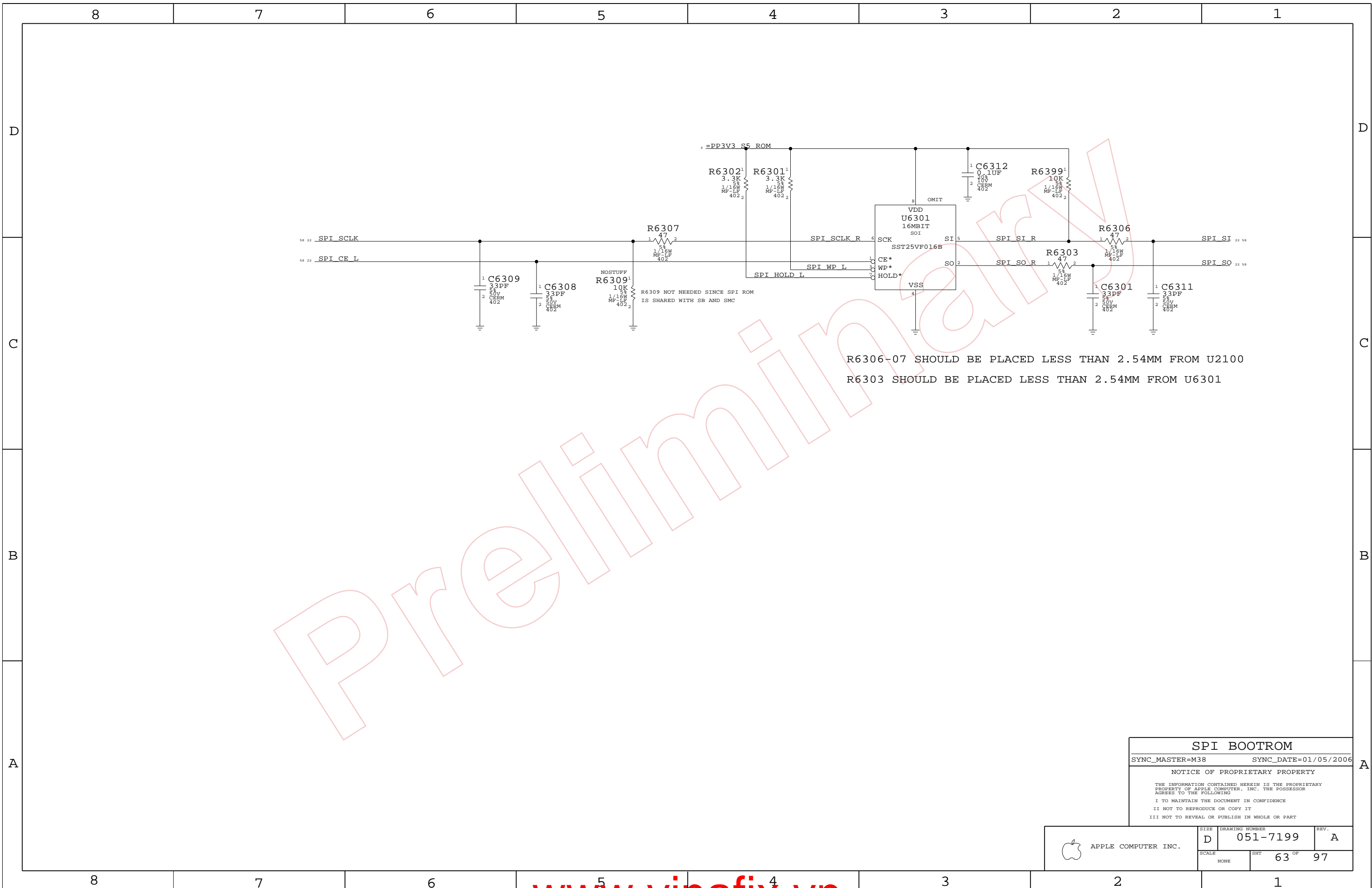
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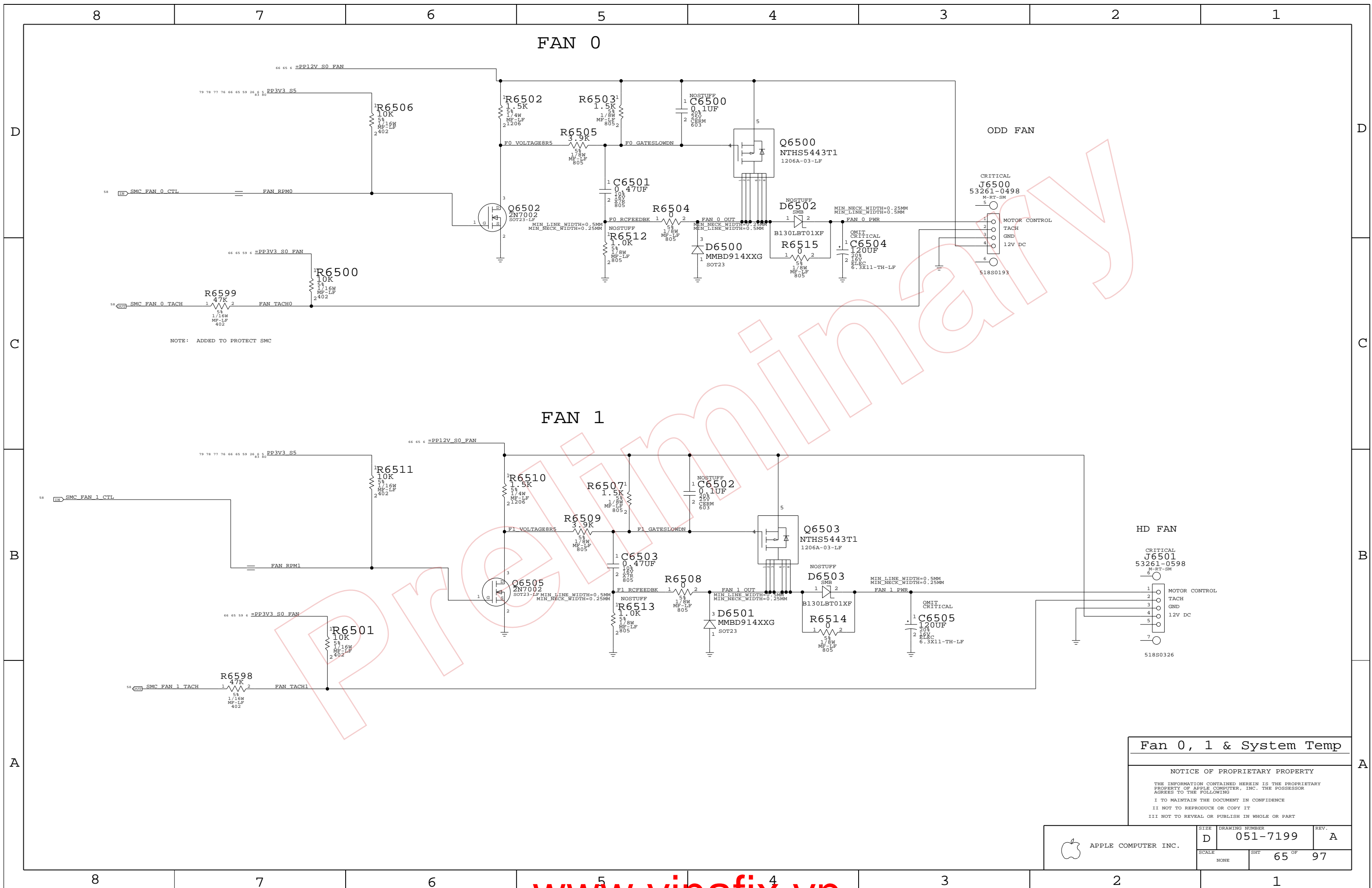
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7199	REV. A
	SCALE NONE	SHT 61 OF 97	



R6306-07 SHOULD BE PLACED LESS THAN 2.54MM FROM U2100
 R6303 SHOULD BE PLACED LESS THAN 2.54MM FROM U6301

SPI BOOTROM
 SYNC_MASTER=M38 SYNC_DATE=01/05/2006
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7199	REV. A
	SCALE NONE	SHIT 63 OF 97	



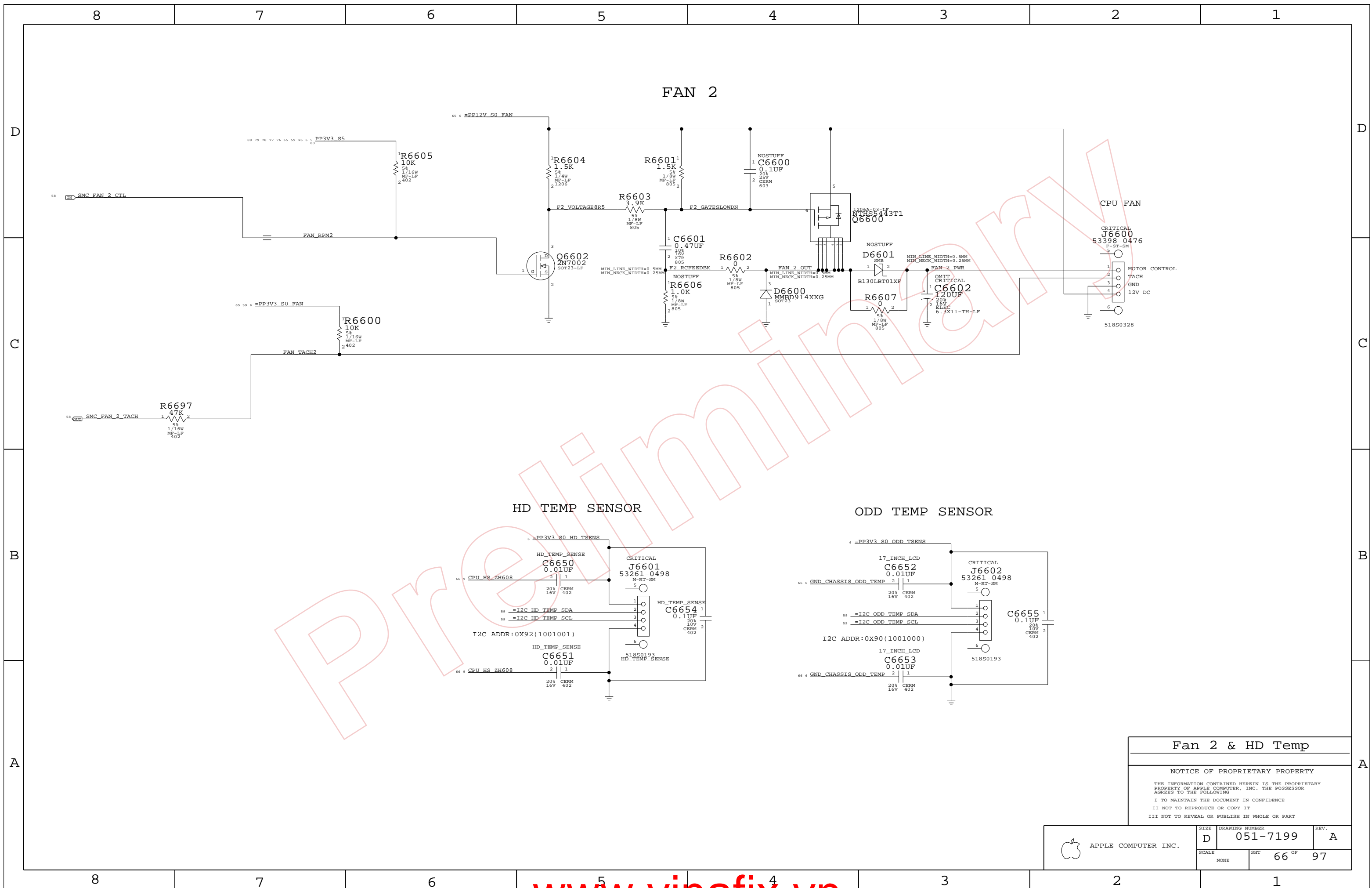
NOTE: ADDED TO PROTECT SMC

Fan 0, 1 & System Temp

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	D	051-7199	A
SCALE	SHT	65 OF	97
NONE			



FAN 2

HD TEMP SENSOR

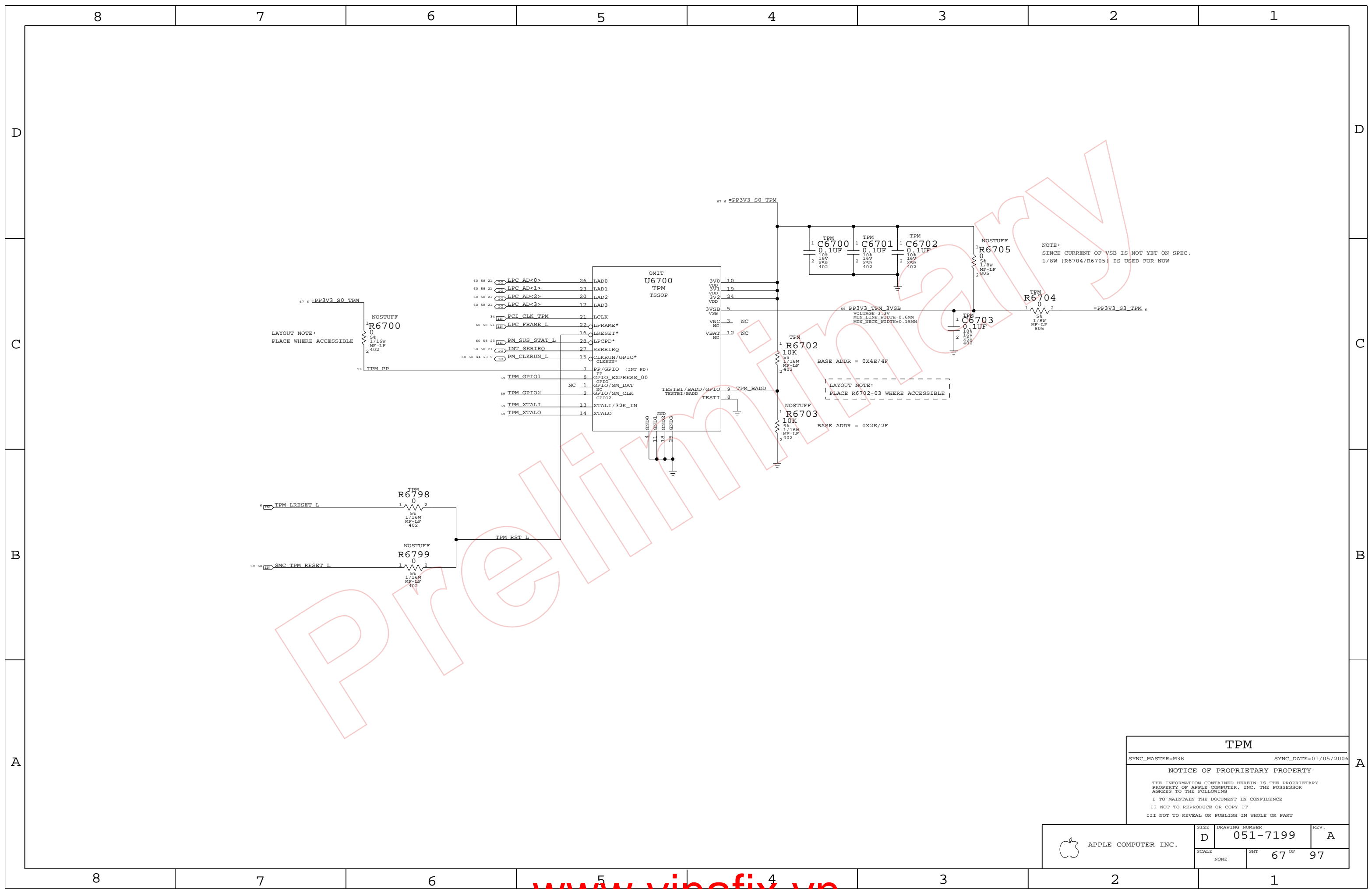
ODD TEMP SENSOR

Fan 2 & HD Temp

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	D	051-7199	A
SCALE	SHT	66 OF	97
NONE			



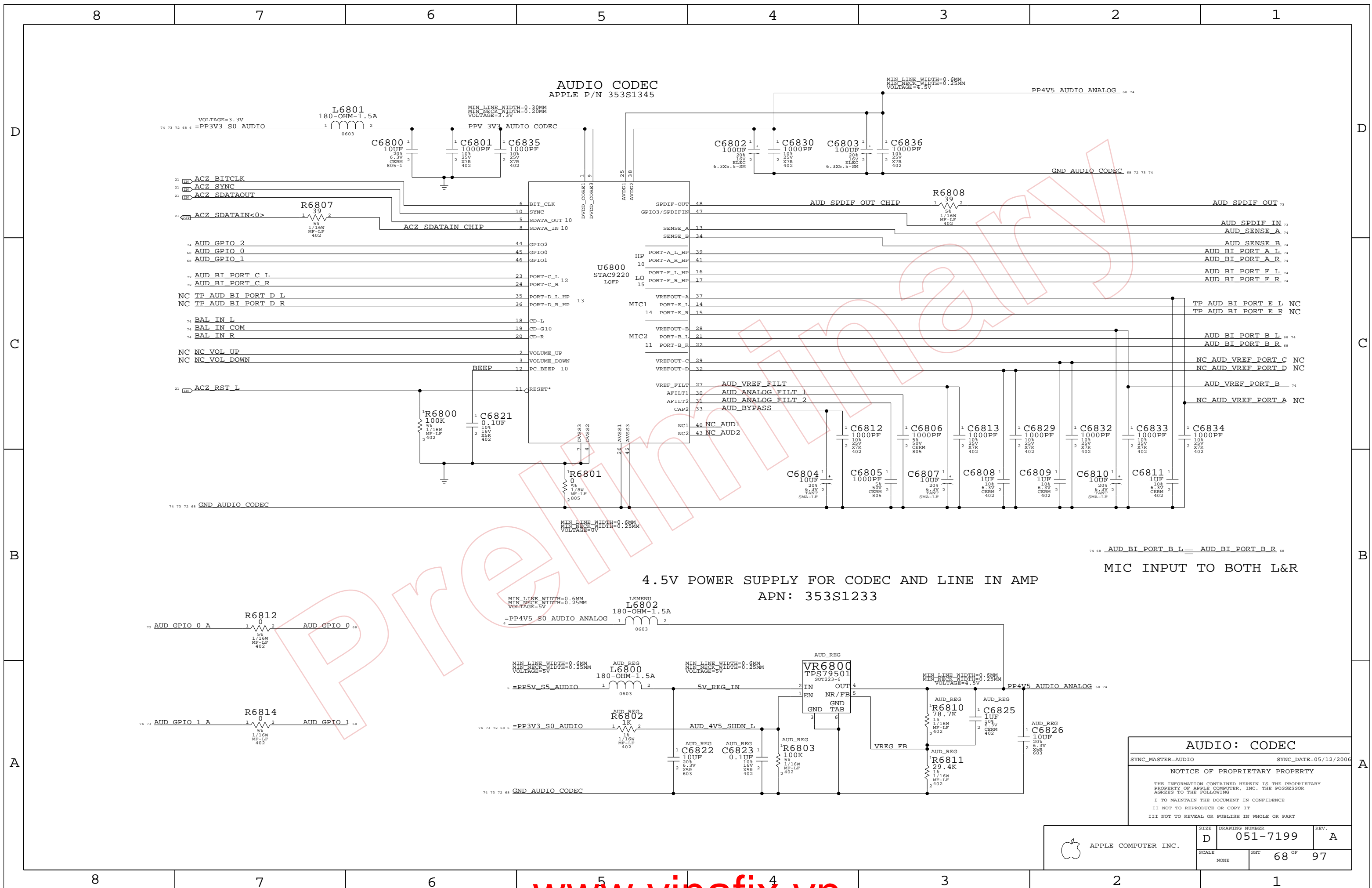
LAYOUT NOTE:
PLACE WHERE ACCESSIBLE

NOTE:
SINCE CURRENT OF VSB IS NOT YET ON SPEC,
1/8W (R6704/R6705) IS USED FOR NOW

LAYOUT NOTE:
PLACE R6702-03 WHERE ACCESSIBLE

TPM		
SYNC_MASTER=M38	SYNC_DATE=01/05/2006	
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	D	051-7199	A
SCALE	SHT	67 OF 97	
NONE			

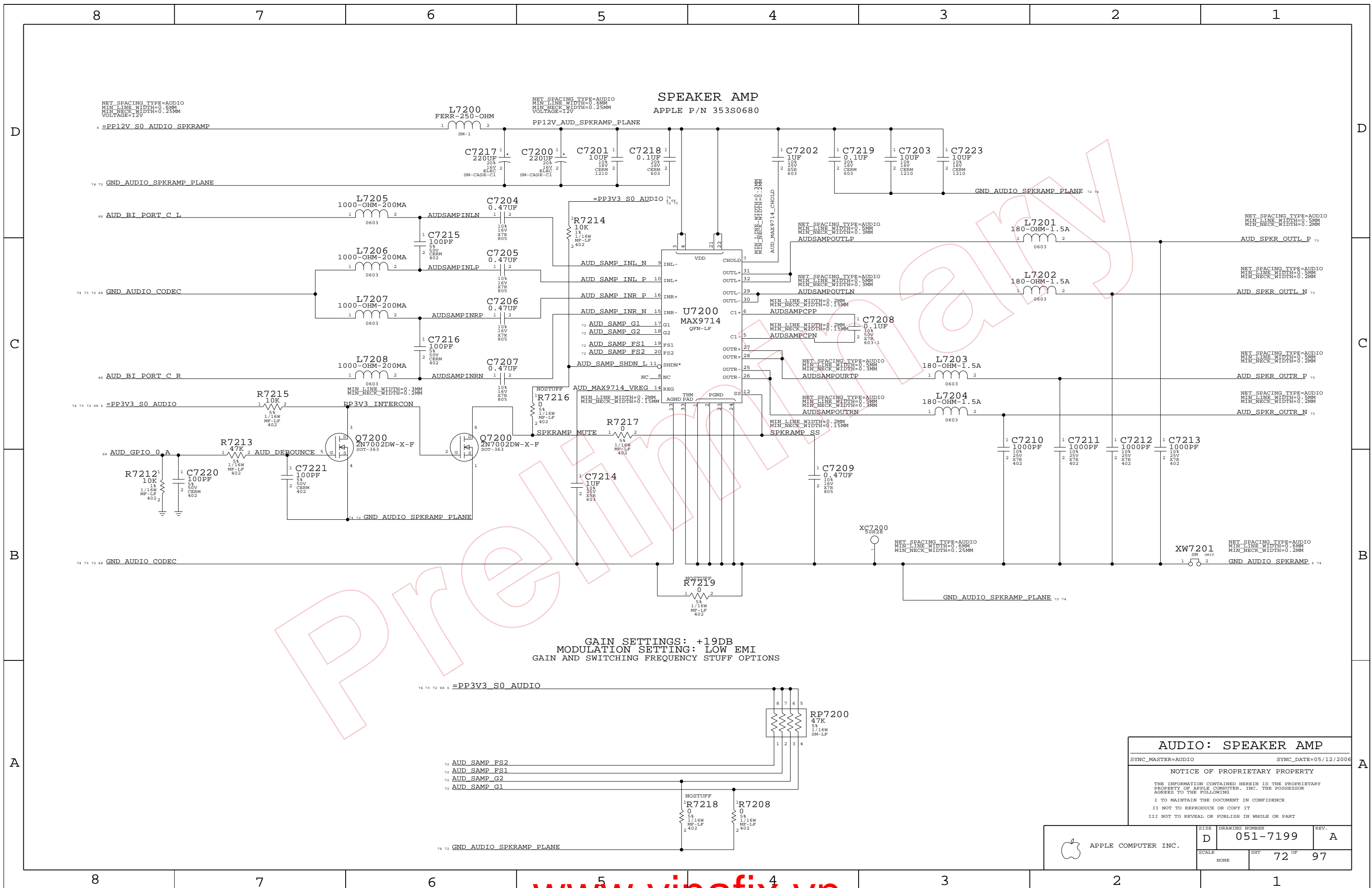


AUDIO CODEC
APPLE P/N 353S1345

4.5V POWER SUPPLY FOR CODEC AND LINE IN AMP
APN: 353S1233

AUDIO: CODEC
 SYNC_MASTER=AUDIO SYNC_DATE=05/12/2006
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	SCALE NONE	SHEET 68 OF 97	

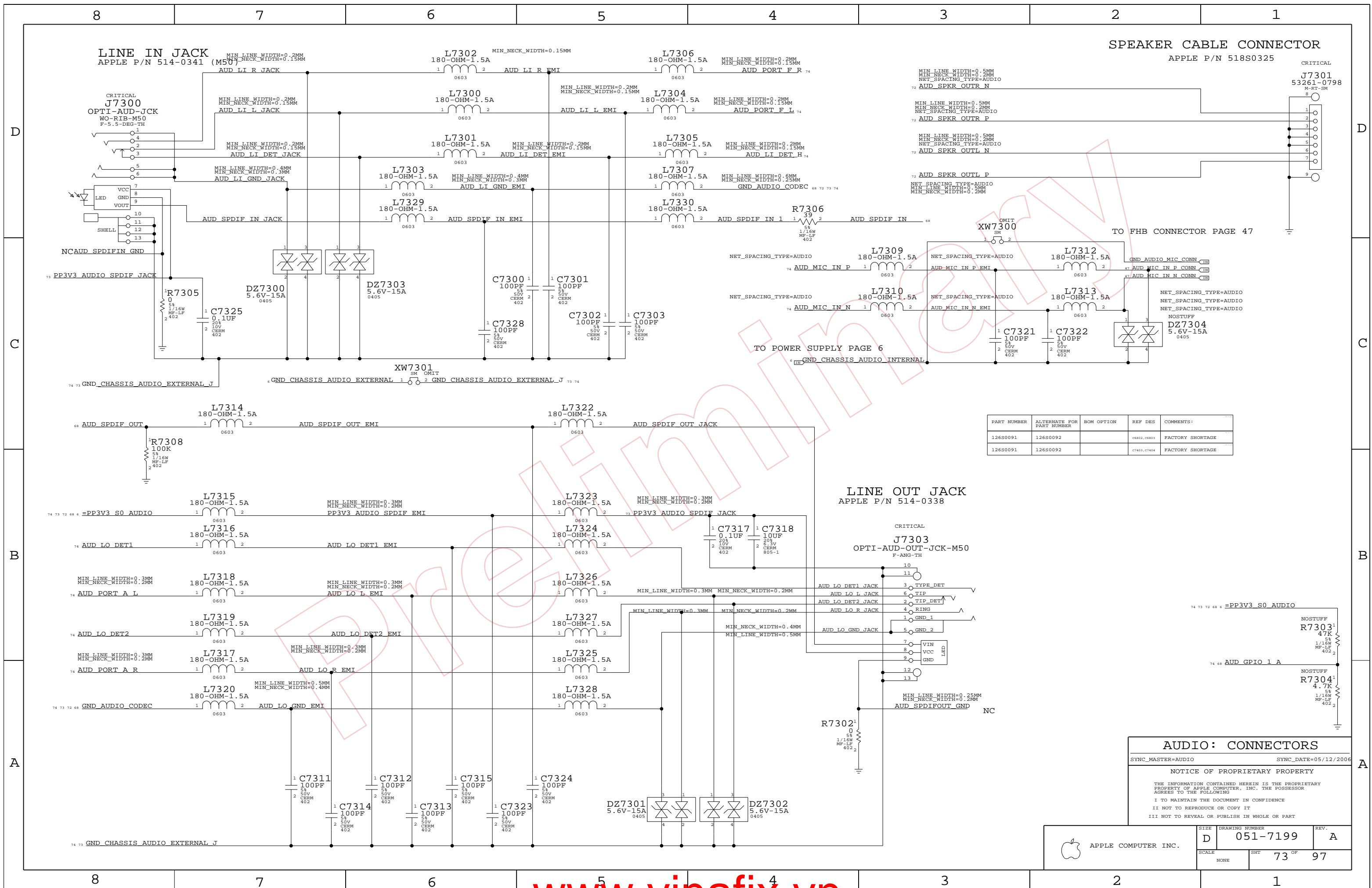


SPEAKER AMP
APPLE P/N 353S0680

GAIN SETTINGS: +19DB
MODULATION SETTING: LOW EMI
GAIN AND SWITCHING FREQUENCY STUFF OPTIONS

AUDIO: SPEAKER AMP
SYNC_MASTER=AUDIO SYNC_DATE=05/12/2006
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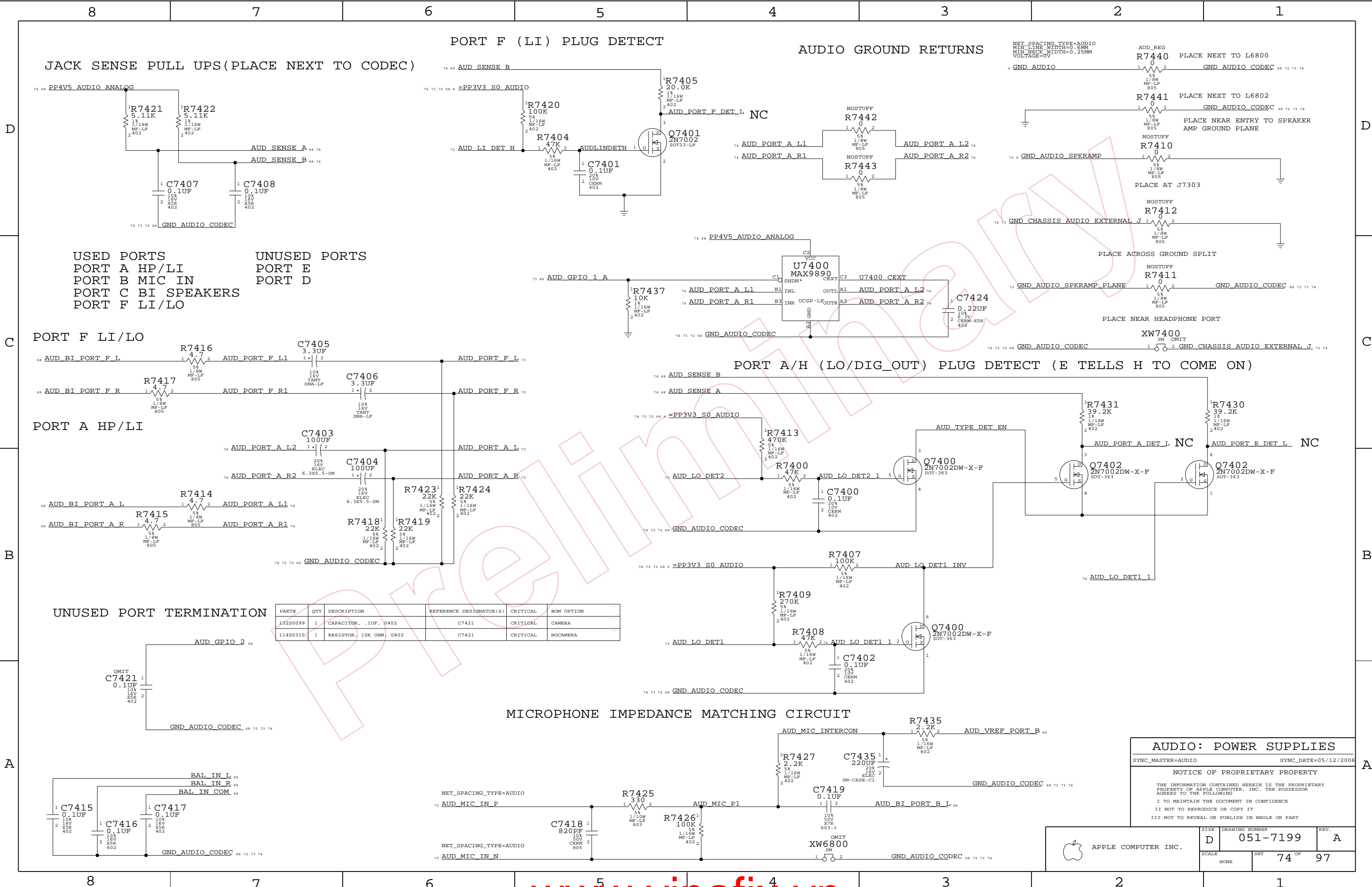
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	A
SCALE	SHT	72 OF 97	
NONE			



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
126S0091	126S0092		C8802, C8803	FACTORY SHORTAGE
126S0091	126S0092		C7453, C7454	FACTORY SHORTAGE

AUDIO: CONNECTORS
 SYNC_MASTER=AUDIO SYNC_DATE=05/12/2006
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	D	051-7199	A
SCALE	SHT	73 OF	97
NONE			

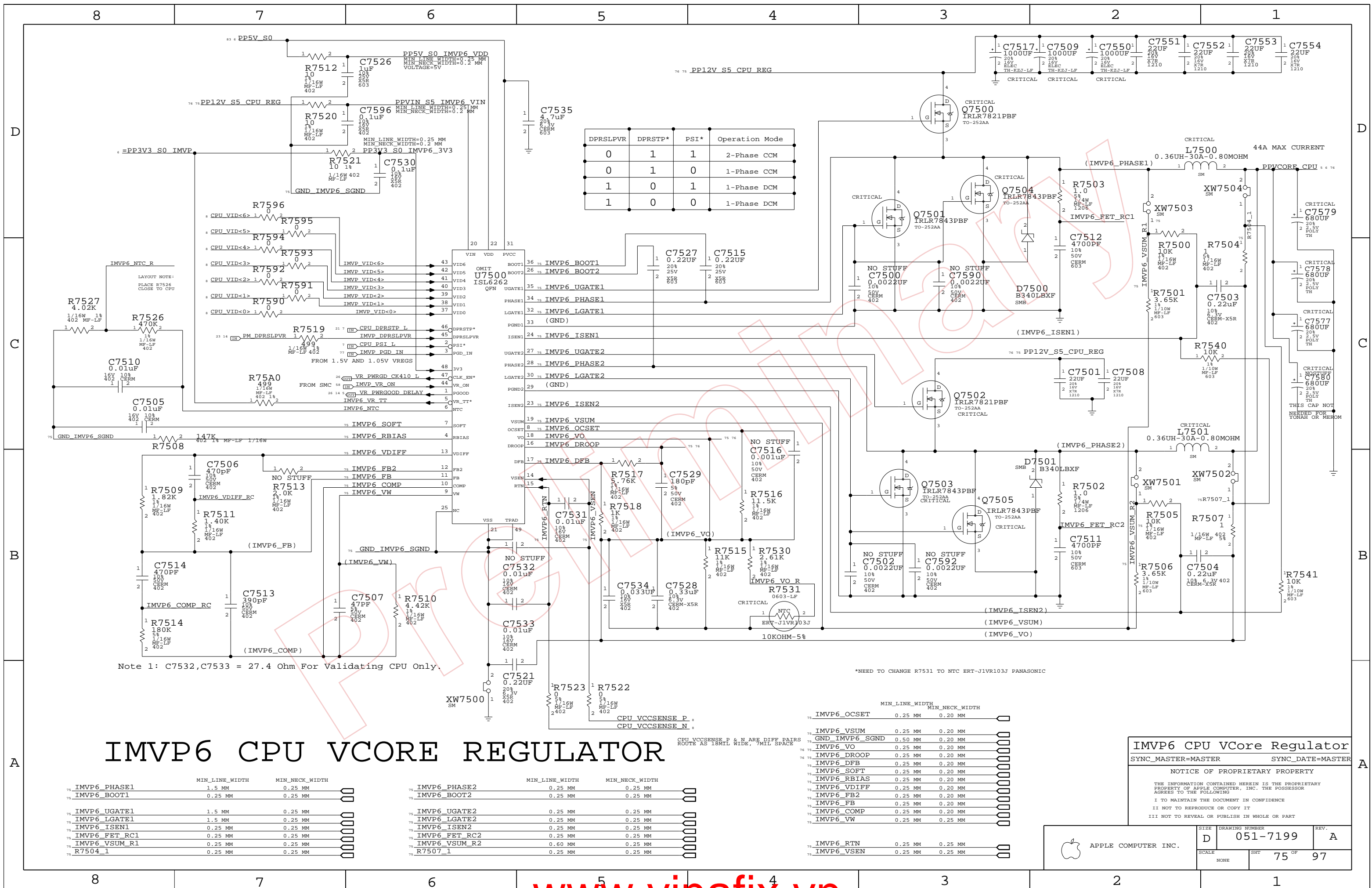


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
132S0099	1	CAPACITOR, .1UF, 0402	C7421	CRITICAL	CAMERA
11480315	1	RESISTOR, 10K OHM, 0402	C7421	CRITICAL	NOCAMERA

AUDIO: POWER SUPPLIES
 SYNC_MASTER=AUDIO SYNC_DATE=05/12/2006

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APPLE COMPUTER INC.	SCALE	DRAWING NUMBER	REV.
	NONE	D 051-7199	A
SHEET		74 OF 97	



DPRSLPVR	DPRSTP*	PSI*	Operation Mode
0	1	1	2-Phase CCM
0	1	0	1-Phase CCM
1	0	1	1-Phase DCM
1	0	0	1-Phase DCM

Note 1: C7532, C7533 = 27.4 Ohm For Validating CPU Only.

*NEED TO CHANGE R7531 TO NTC ERT-J1VR103J PANASONIC

IMVP6 CPU VCore Regulator

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
75 IMVP6_PHASE1	1.5 MM	0.25 MM
75 IMVP6_BOOT1	0.25 MM	0.25 MM
75 IMVP6_UGATE1	1.5 MM	0.25 MM
75 IMVP6_LGATE1	1.5 MM	0.25 MM
75 IMVP6_ISEN1	0.25 MM	0.25 MM
75 IMVP6_FET_RC1	0.25 MM	0.25 MM
75 IMVP6_VSUM_R1	0.25 MM	0.25 MM
75 R7504_1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
75 IMVP6_PHASE2	0.25 MM	0.25 MM
75 IMVP6_BOOT2	0.25 MM	0.25 MM
75 IMVP6_UGATE2	0.25 MM	0.25 MM
75 IMVP6_LGATE2	0.25 MM	0.25 MM
75 IMVP6_ISEN2	0.25 MM	0.25 MM
75 IMVP6_FET_RC2	0.25 MM	0.25 MM
75 IMVP6_VSUM_R2	0.60 MM	0.25 MM
75 R7507_1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
75 IMVP6_OCSET	0.25 MM	0.20 MM
75 IMVP6_VSUM	0.25 MM	0.20 MM
75 GND_IMVP6_SGND	0.50 MM	0.20 MM
75 IMVP6_VO	0.25 MM	0.20 MM
75 IMVP6_DROOP	0.25 MM	0.20 MM
75 IMVP6_DFB	0.25 MM	0.20 MM
75 IMVP6_SOFT	0.25 MM	0.20 MM
75 IMVP6_RBIAS	0.25 MM	0.20 MM
75 IMVP6_VDIFF	0.25 MM	0.20 MM
75 IMVP6_FB2	0.25 MM	0.20 MM
75 IMVP6_FB	0.25 MM	0.20 MM
75 IMVP6_COMP	0.25 MM	0.20 MM
75 IMVP6_VW	0.25 MM	0.25 MM
75 IMVP6_RTIN	0.25 MM	0.25 MM
75 IMVP6_VSEN	0.25 MM	0.25 MM

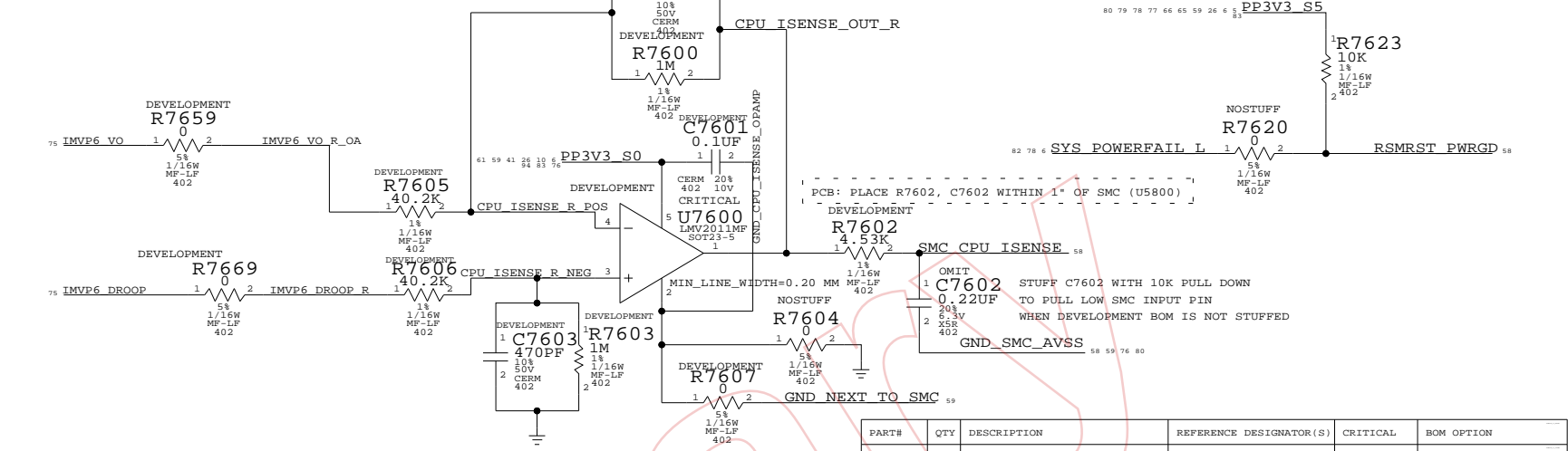
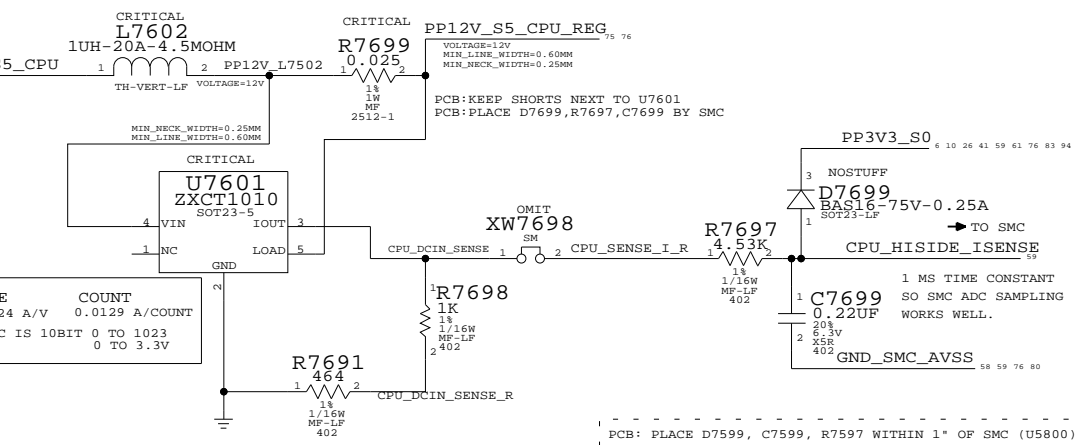
IMVP6 CPU VCore Regulator
 SYNC_MASTER=MASTER SYNC_DATE=MASTER

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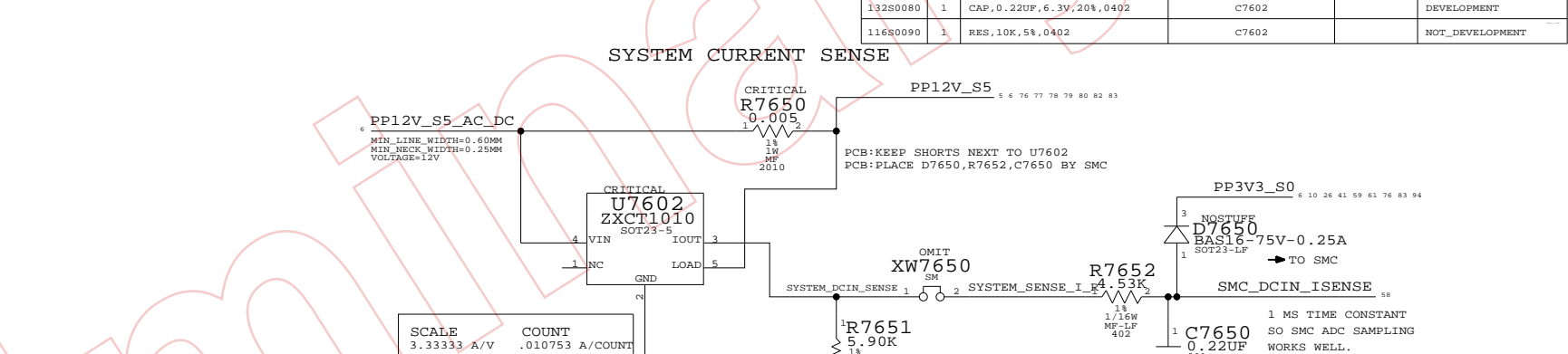
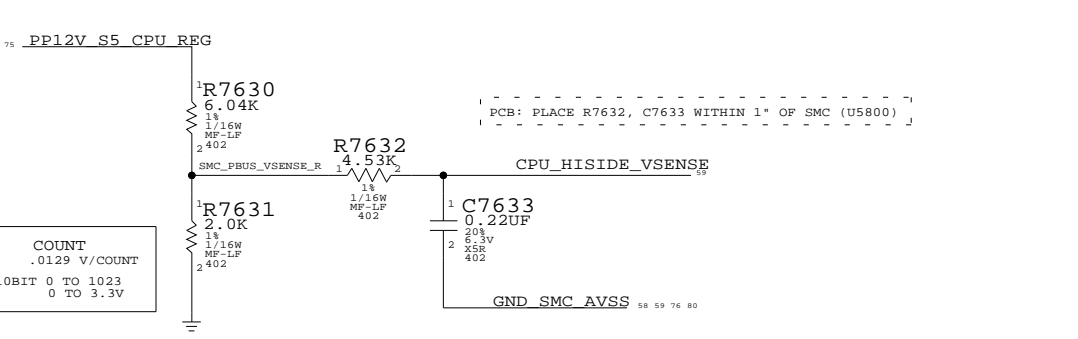
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	A
SCALE	SHEET	75 OF 97	
NONE			

PROCESSOR VCORE CURRENT SENSE
(MEASURING DC/DC INDUCTOR DCR TO DERIVE CPU CURRENT)

PROCESSOR VCORE CURRENT SENSE
(USING 12V INPUT CURRENT TO DERIVE CPU CURRENT)



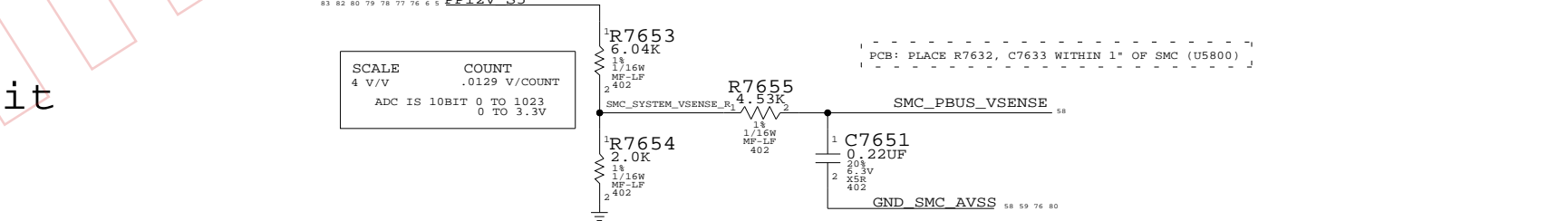
PROCESSOR DCIN VOLTAGE SENSE
(SCALING 12V INPUT VOLTAGE TO SMC)



SCALE	COUNT
2.73224 A/V	0.0129 A/COUNT
ADC IS 10BIT 0 TO 1023	
0 TO 3.3V	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
132S0080	1	CAP,0.22UF,6.3V,20%,0402	C7602		DEVELOPMENT
116S0090	1	RES,10K,5%,0402	C7602		NOT_DEVELOPMENT

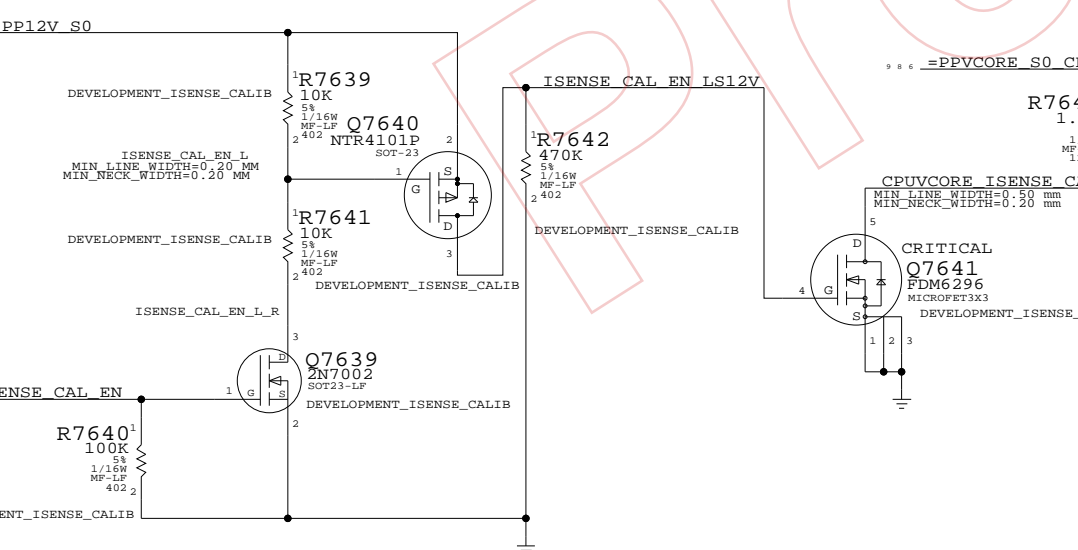
SYSTEM VOLTAGE SENSE
(SCALING 12V INPUT VOLTAGE TO SMC)



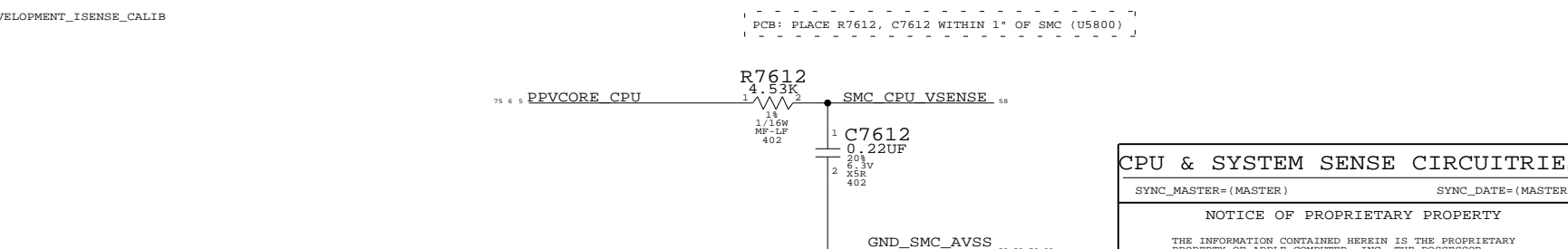
SCALE	COUNT
4 V/V	.0129 V/COUNT
ADC IS 10BIT 0 TO 1023	
0 TO 3.3V	

Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits

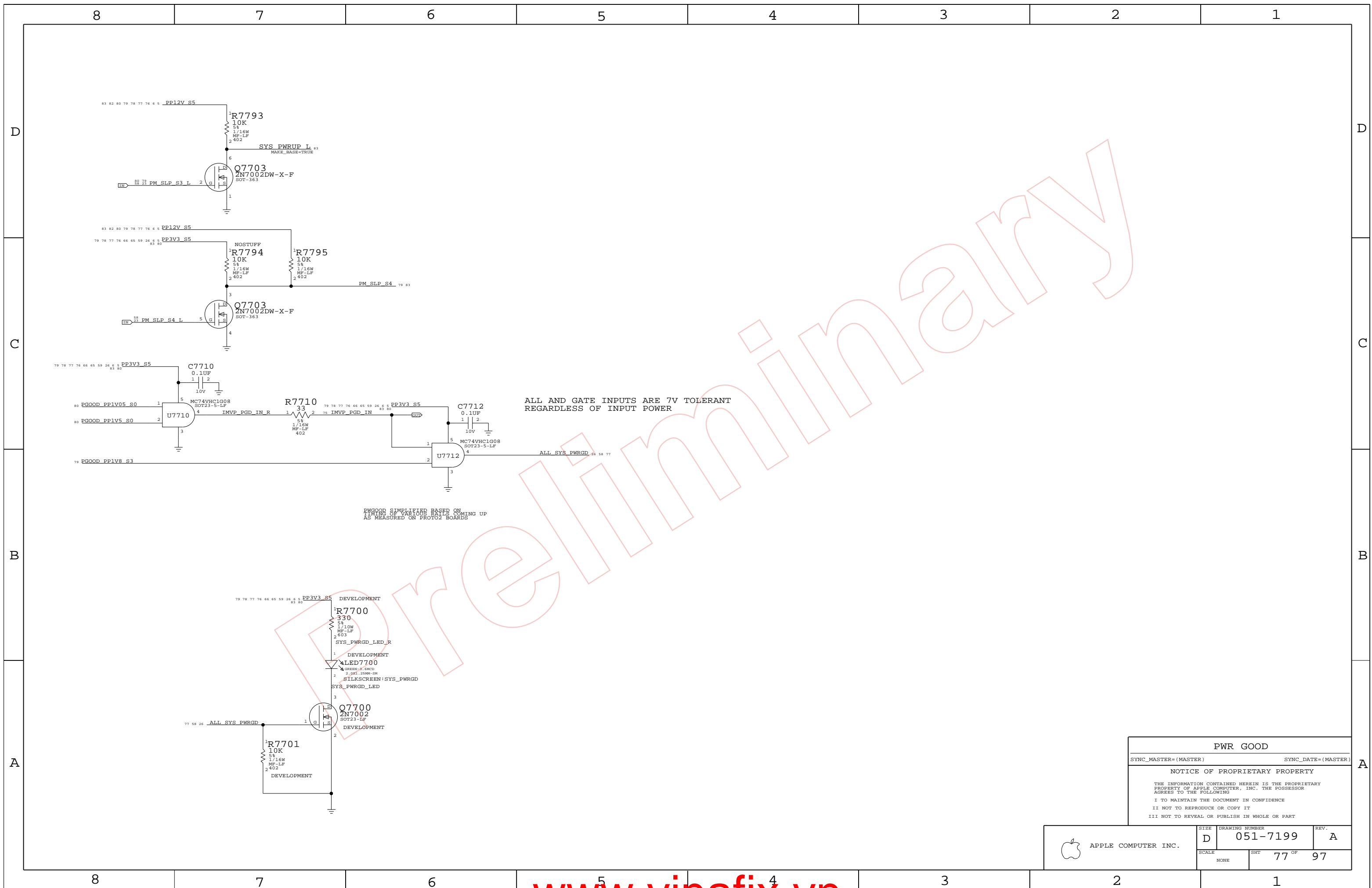


PROCESSOR VCORE SENSE



SCALE	COUNT
4 V/V	.0129 V/COUNT
ADC IS 10BIT 0 TO 1023	
0 TO 3.3V	

CPU & SYSTEM SENSE CIRCUITRIES
 SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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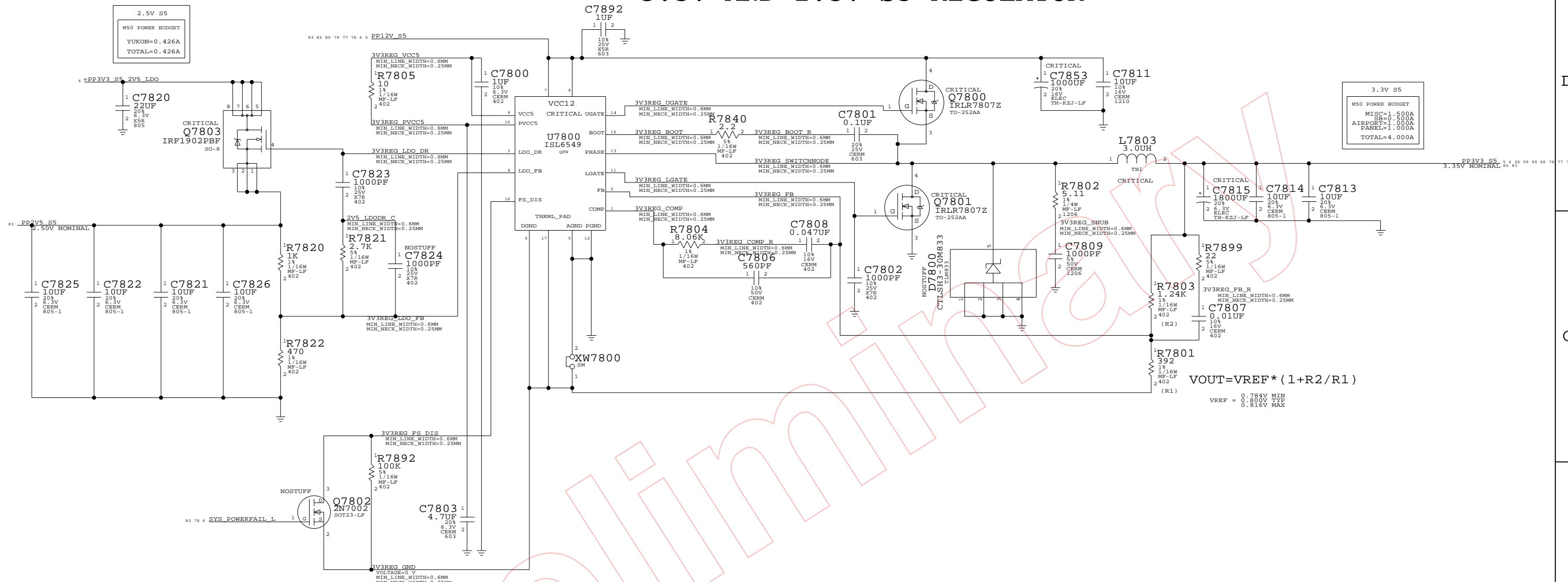
PWGOOD SIMPLIFIED BASED ON TIMING OF VARIOUS RAILS COMING UP AS MEASURED ON PROTOZ BOARDS

ALL AND GATE INPUTS ARE 7V TOLERANT REGARDLESS OF INPUT POWER

PWR GOOD
 SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	A
SCALE		SHT	77 OF 97
NONE			

3.3V AND 2.5V S5 REGULATOR



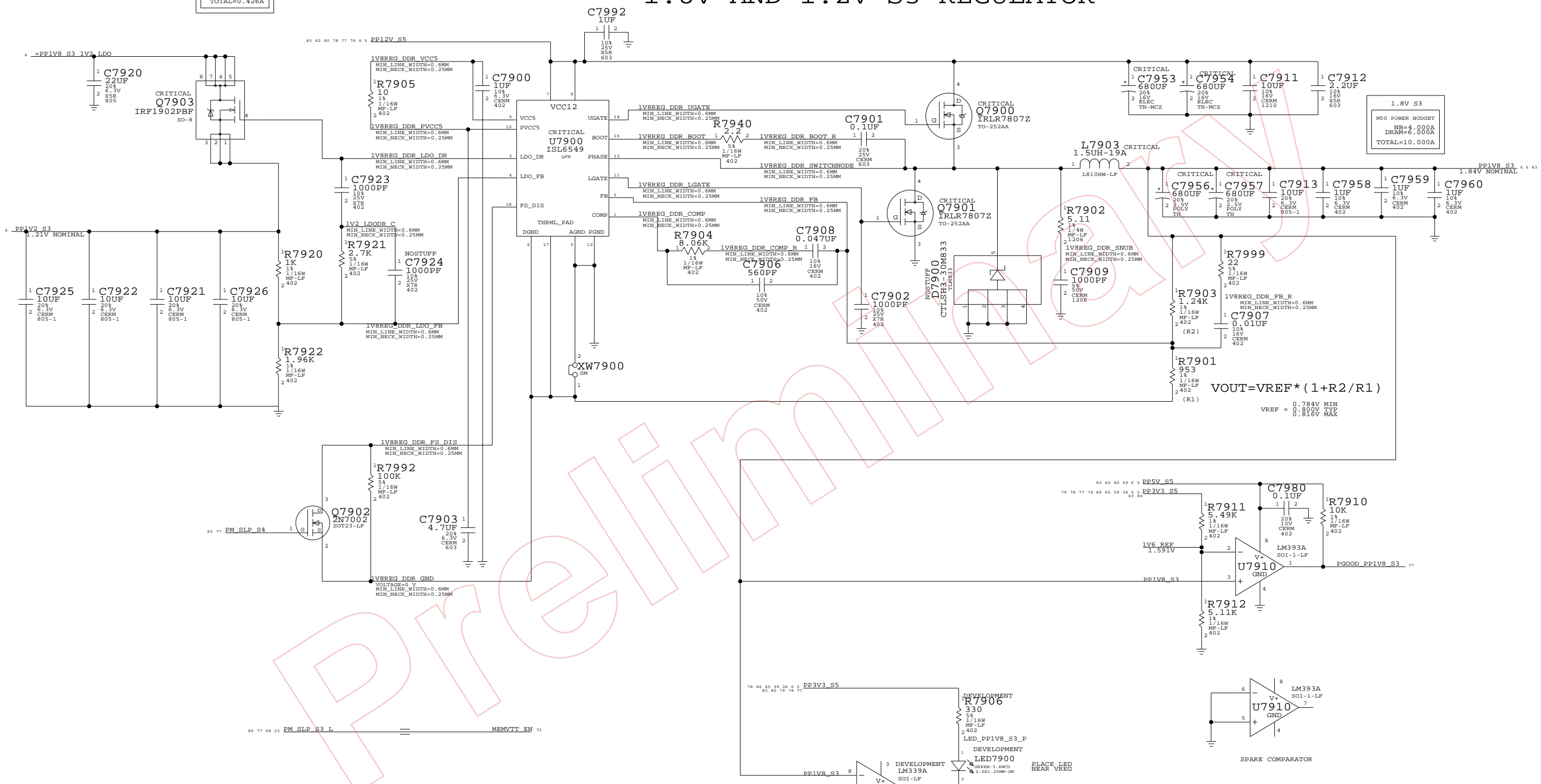
3V DC/DC 2.5V
 SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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	D	051-7199	A
SCALE	SHT	78 OF 97	
NONE			

1.8V AND 1.2V S3 REGULATOR

1.2V S3
MS0 POWER BUDGET
YUKON=0.426A
TOTAL=0.426A

1.8V S3
MS0 POWER BUDGET
NE=4.000A
DRAM=6.000A
TOTAL=10.000A



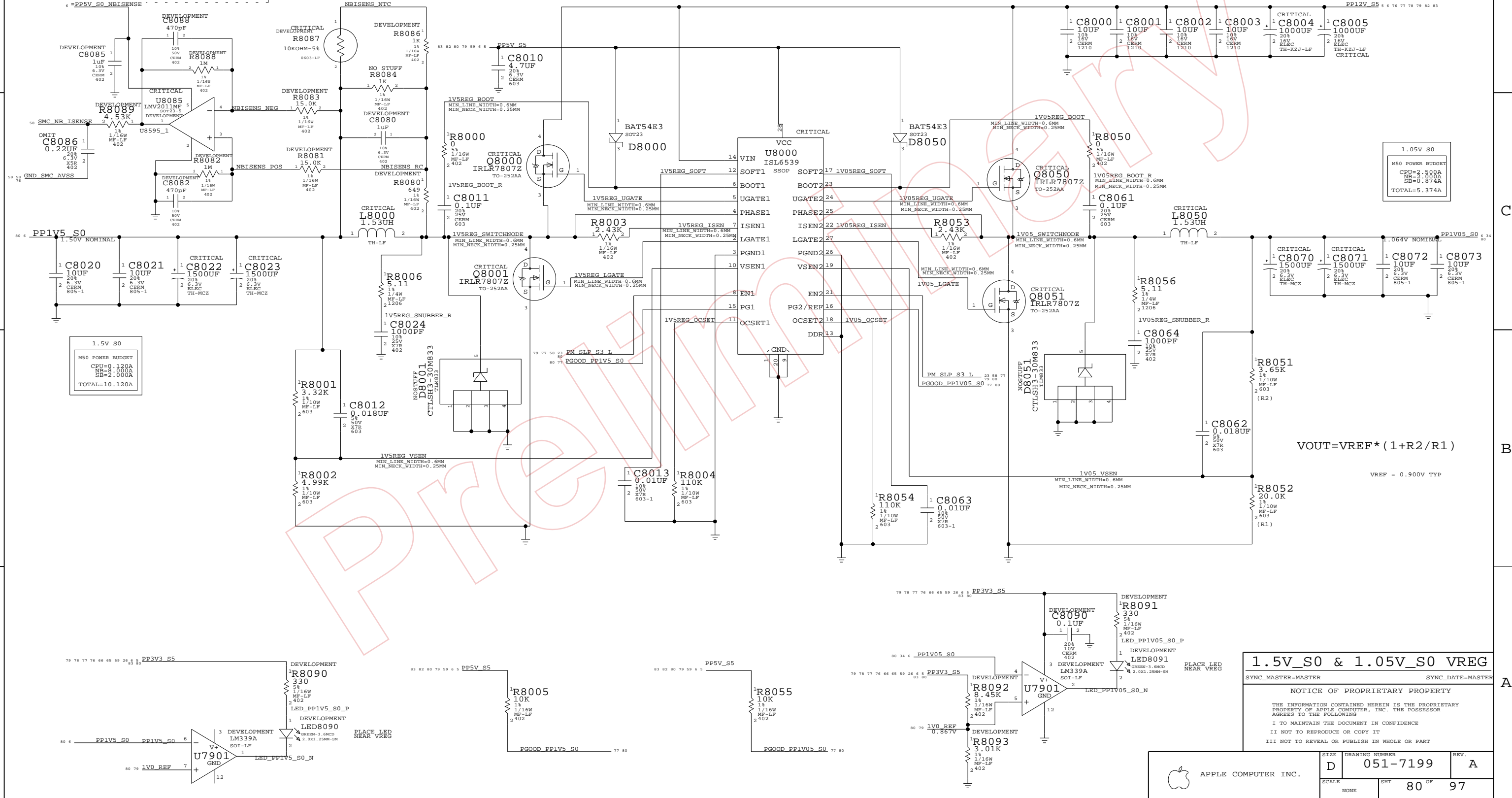
1.8V & 1.2V VREG
SYNC_MASTER=MASTER
SYNC_DATE=MASTER
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	D	051-7199	A
SCALE	SHT	79 OF 97	
NONE			

1.5V S0 AND 1.05V S0 RAILS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
13280080	1	CAP,0.22UF,6.3V,20%,0402	C8086		DEVELOPMENT
11650090	1	RES,10K,5%,0402	C8086		NOT_DEVELOPMENT

Placement Note:
KEEP C8080, R8080,
R8084 AND R8087
close to inductor



1.5V_S0 & 1.05V_S0 VREG

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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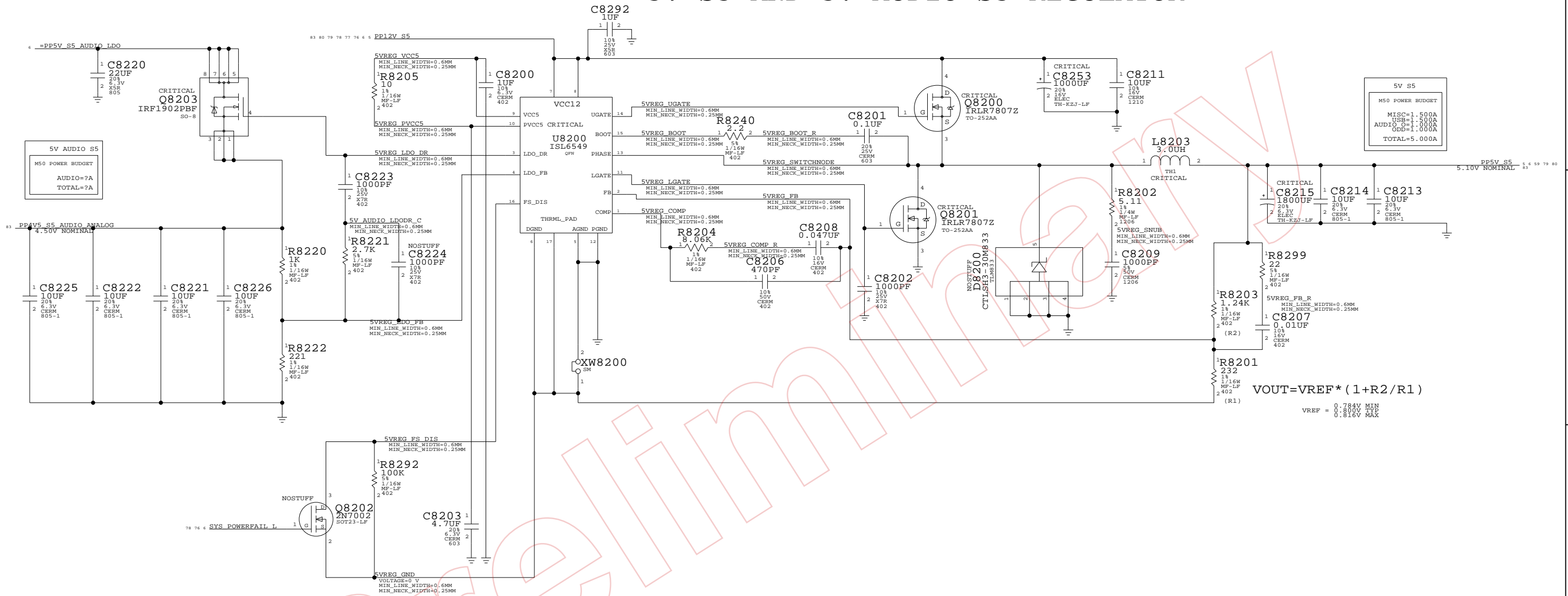
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II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	A
SCALE	SHT	80 OF	97
NONE			

5V S5 AND 5V AUDIO S5 REGULATOR



POWER SUPPLY 3.3V/5V MAIN SWITCH

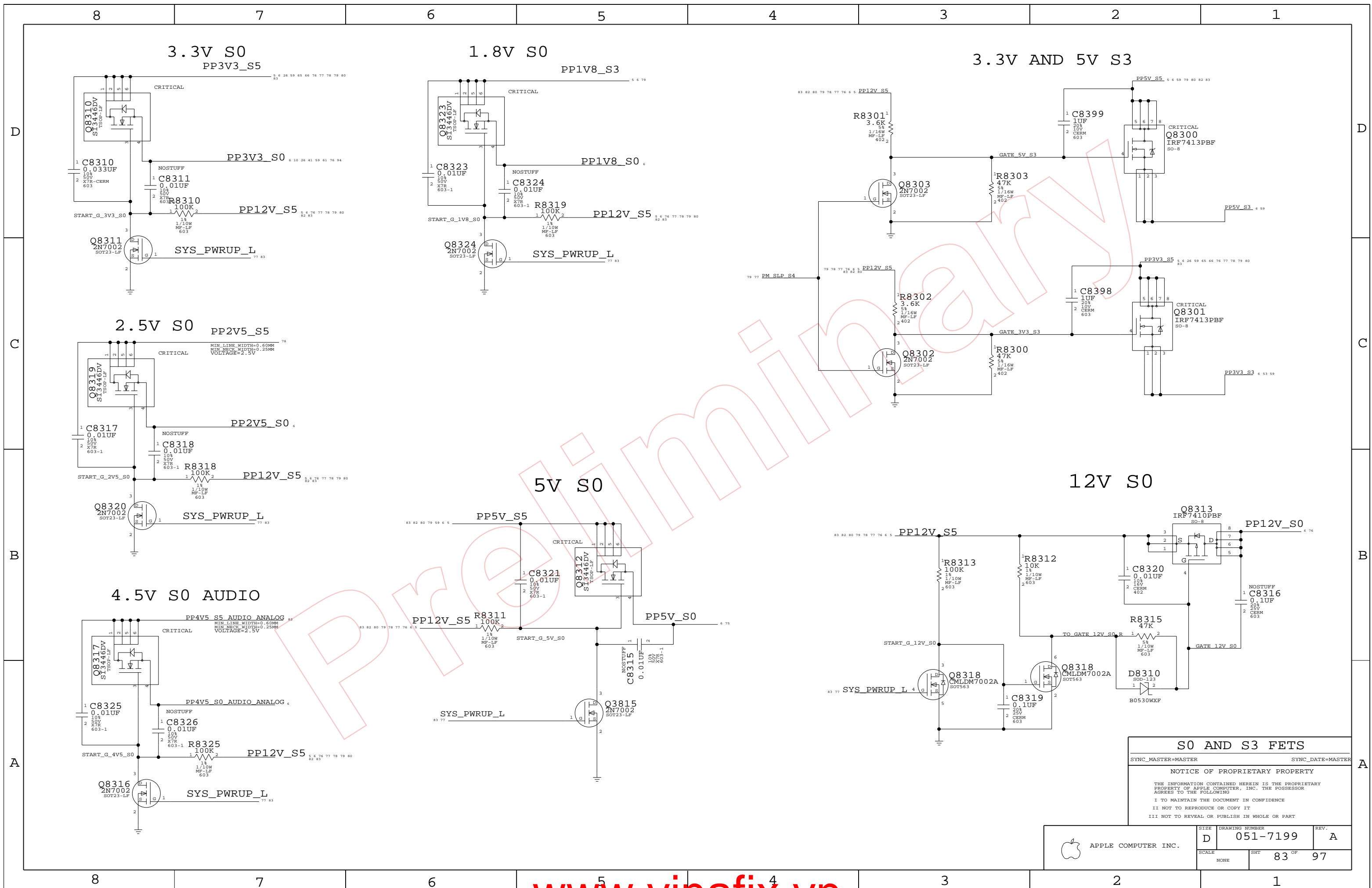
5V DC/DC

SYNC_MASTER=MASTER SYNC_DATE=MASTER

NOTICE OF PROPRIETARY PROPERTY

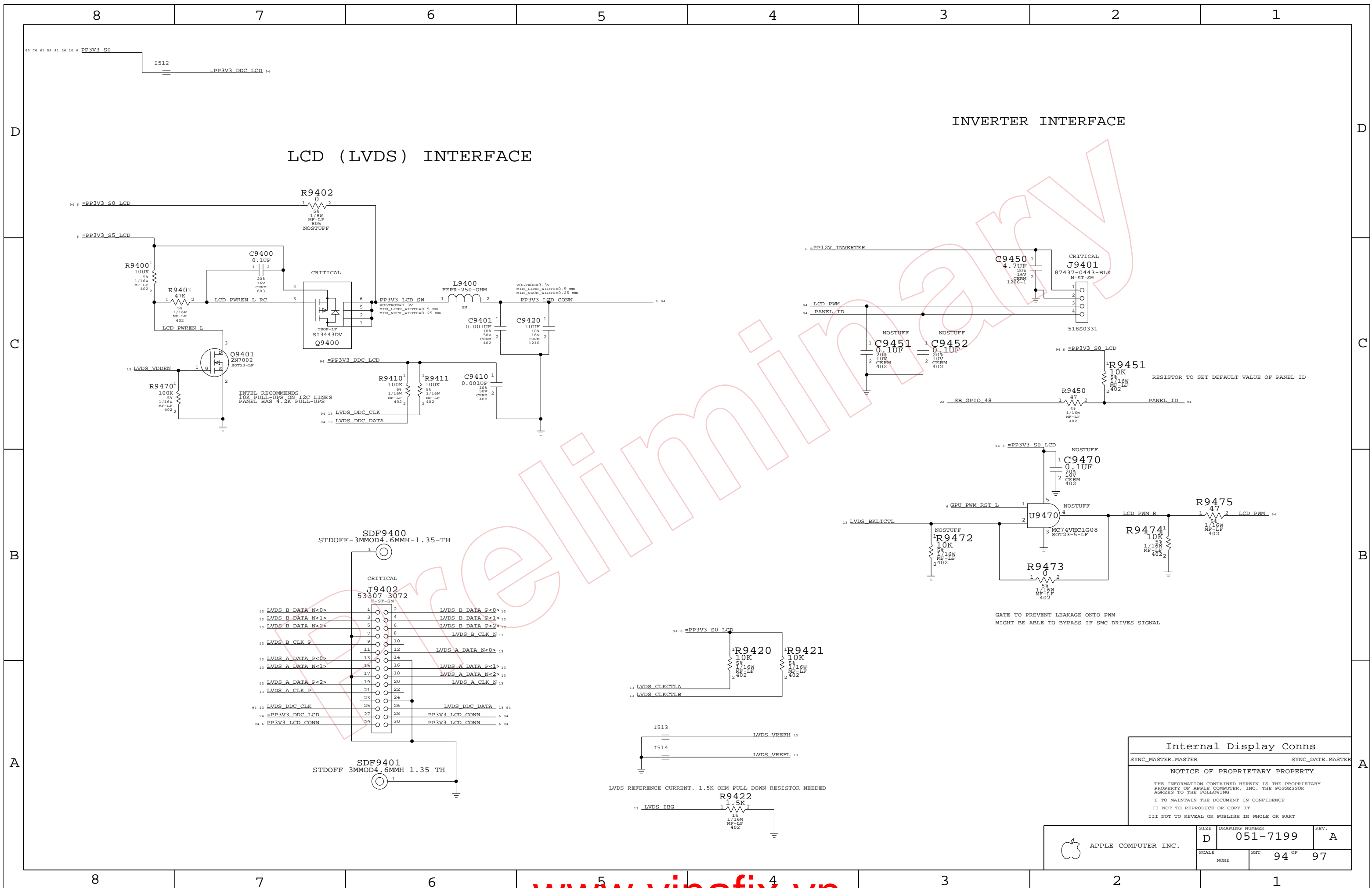
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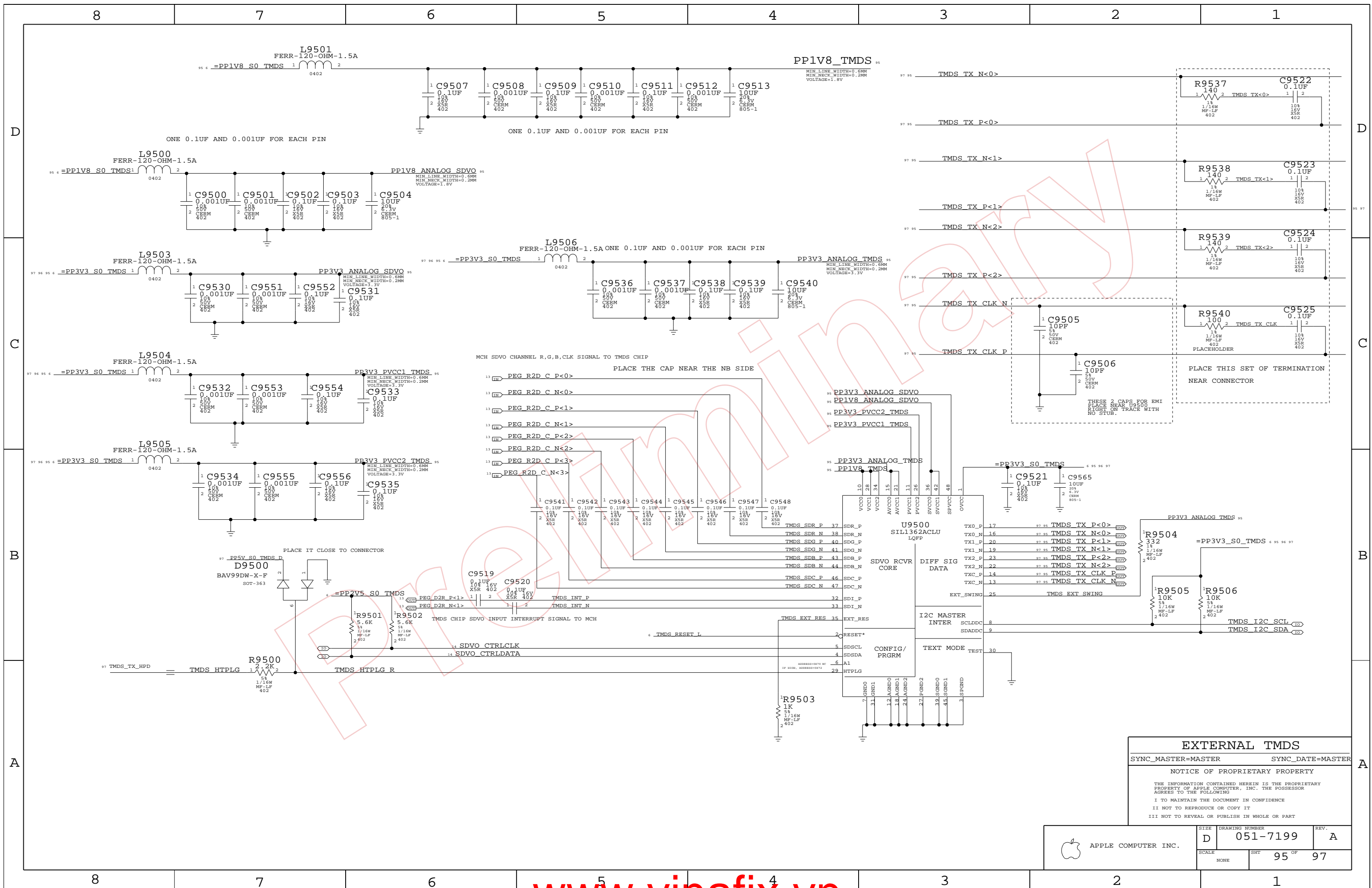
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	A
SCALE	SHT	82 OF	97
NONE			



S0 AND S3 FETS		
SYNC_MASTER=MASTER	SYNC_DATE=MASTER	
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	D	051-7199	A
SCALE	SHT	83 OF	97
NONE			





EXTERNAL TMSD

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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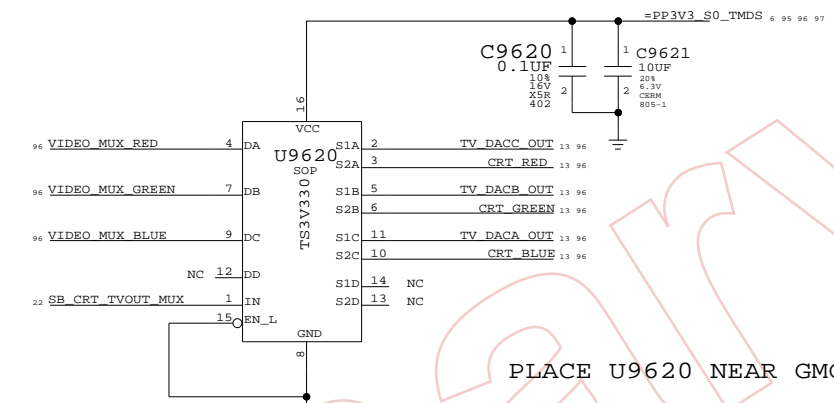
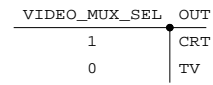
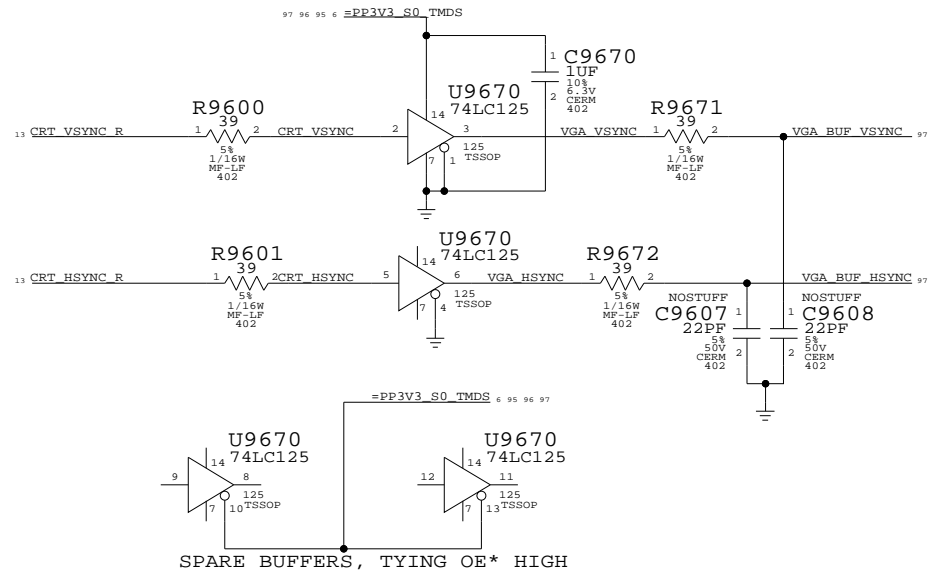
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III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

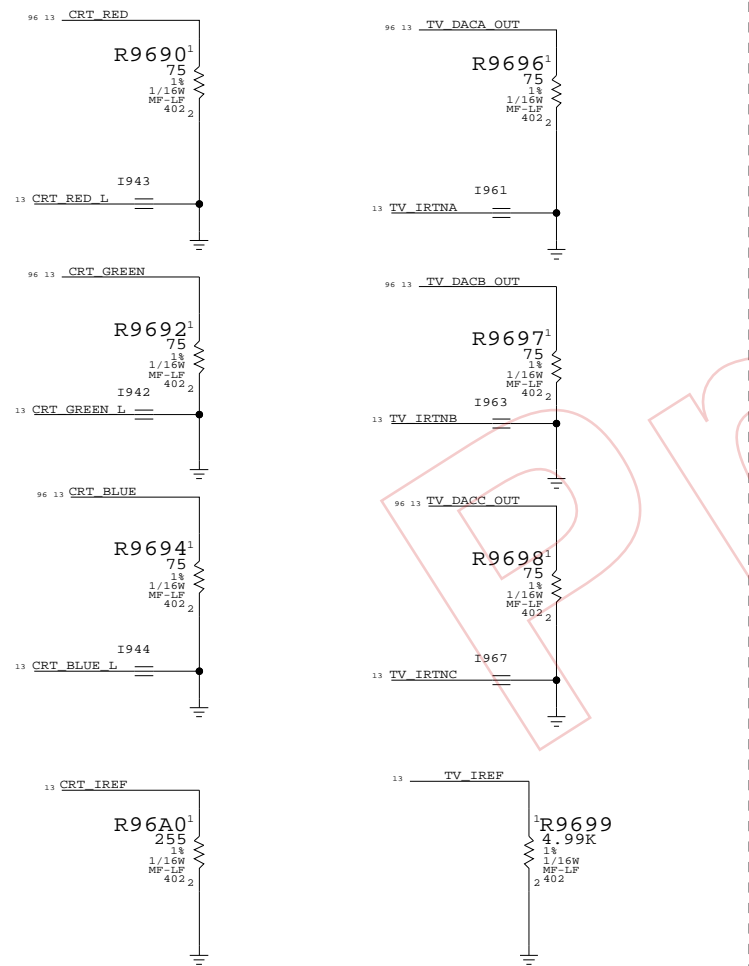
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7199	REV. A
	SCALE NONE	SHEET 95 OF 97	

VGA SYNC BUFFERS

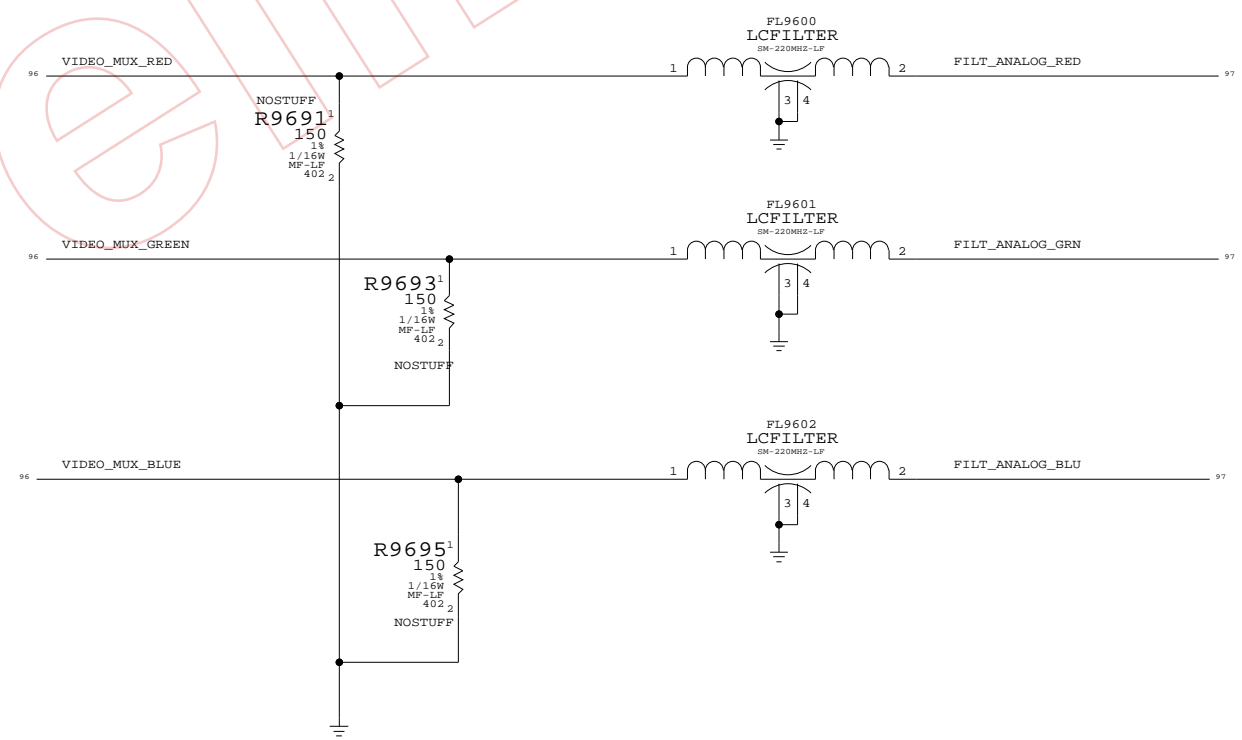


PLACE U9620 NEAR GMCH

PLACE RESISTORS AT NORTHBRIDGE

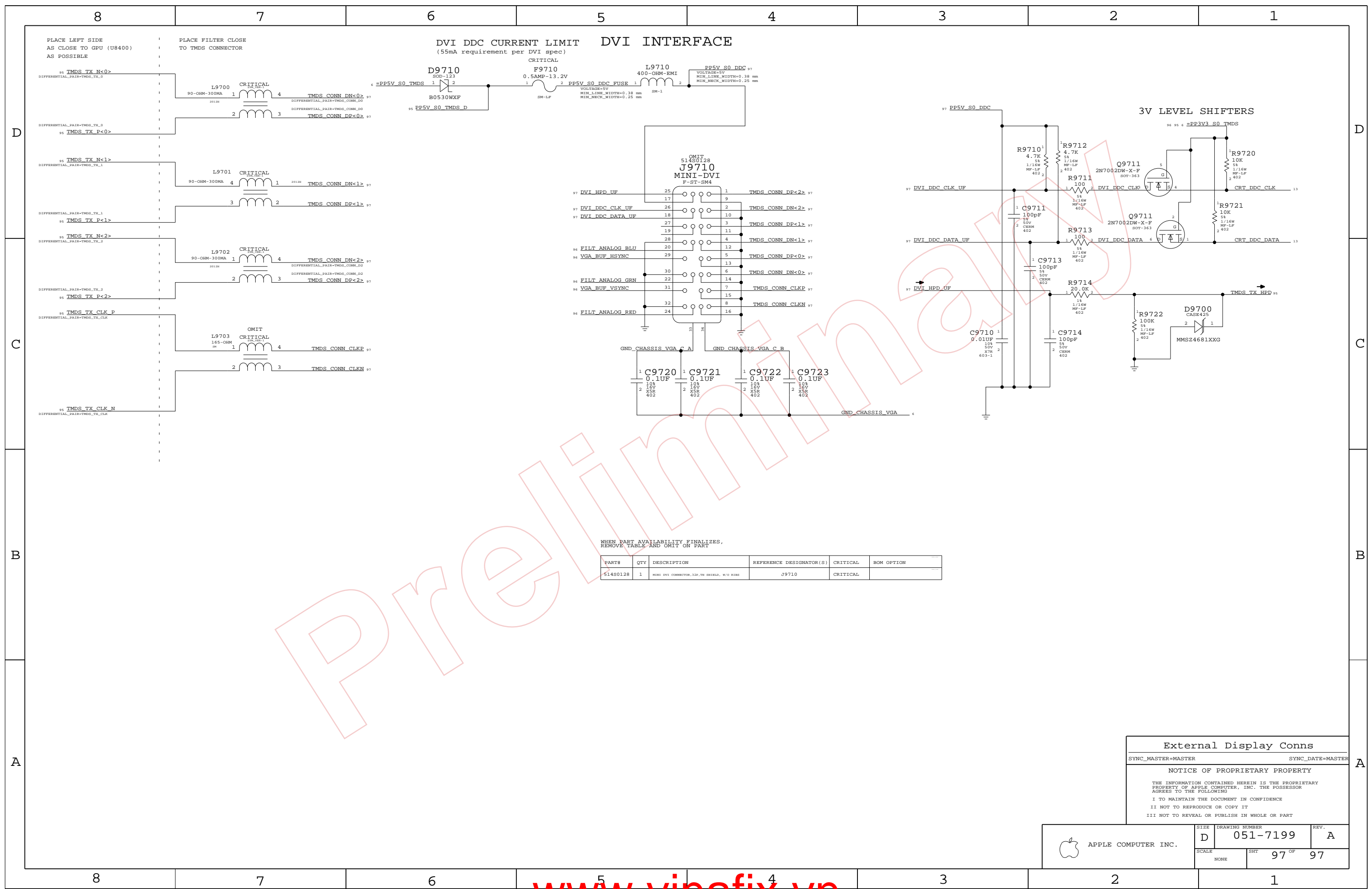


ANALOG FILTERING PLACE BY CONNECTOR



TMDS/Inverter/ExtVGA
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	A
SCALE	SHT	96 OF	97
NONE			



WHEN PART AVAILABILITY FINALIZES,
REMOVE TABLE AND OMIT ON PART

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514S0128	1	MINI DVI CONNECTOR, 25P, TR SHIELD, W/O BIAS	J9710	CRITICAL	

External Display Conns
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	A
SCALE	SHT	97 OF	97
NONE			