

# M38A - DVT

06/22/06

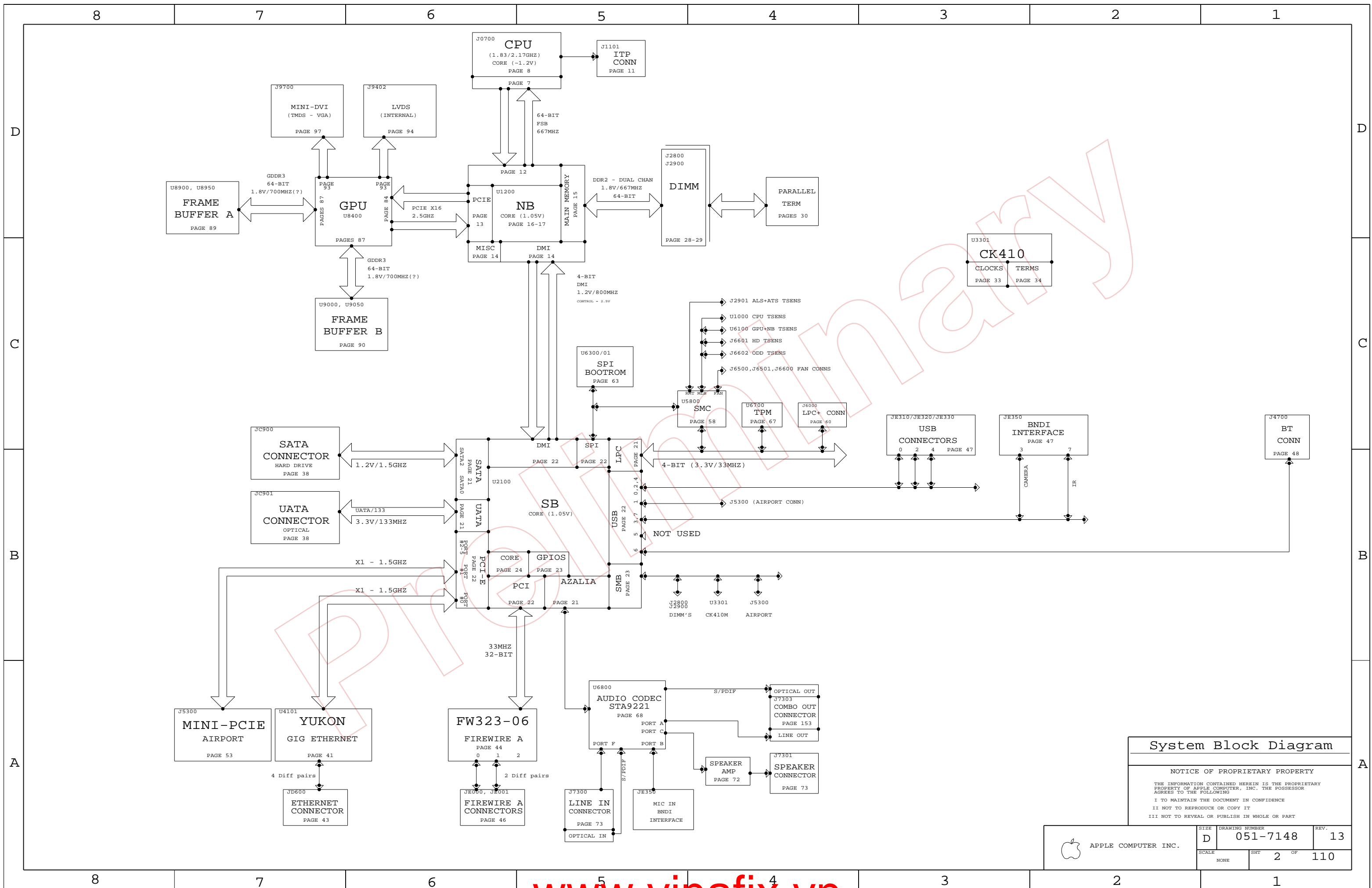
1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD	ENG APPD
				DATE	DATE
13		445818	ENGINEERING RELEASED	06/22/06	06/22/04

PAGE	DRI	PDF	CIRCUIT
1	JD	JD 1	TABLE OF CONTENTS
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3	RT	RT 3	POWER BLOCK DIAGRAM
4	JD	JD 4	TABLE ITEMS & REVISION HISTORY
5	JD	JD 5	FUNC TEST
6	RT	RT 6	POWER CONNECTOR / POWER ALIAS
(M42) 7	MS	JD 7	CPU - BUS INTERFACE
(M42) 8	MS	JD 8	CPU - PWR & GND
9	MS	JD 9	CPU - DECAPS
(M42) 10	MS	JD 10	CPU - THERMAL SENSOR
M42 11	MS	JD 11	CPU - ITP CONN
M1 12	PS	JH 12	NB - CPU INTERFACE
M1 13	PS	JH 13	NB - VIDEO INTERFACE
14	PS	JH 14	NB - MISC INTERFACES
M1 15	PS	JH 15	NB - DDR2 INTERFACE
M1 16	PS	JH 16	NB - POWER 1
M1 17	PS	JH 17	NB - POWER 2
M1 18	PS	JH 18	NB - GROUNDS
19	PS	JH 19	NB - DECAPS
M1 20	PS	JH 20	NB - CONFIG STRAPS
21	JD	JD 21	SB - RTC, LAN, AUDIO, ATA, CPU, LPC
22	JD	JD 22	SB - PCIE, SPI, USB, DMI, PCI
23	JD	JD 23	SB - SMB, GPIO, PM, CLKS
24	JD	JD 24	SB - POWERS AND GROUNDS
25	JD	JD 25	SB - DECAPS
26	JD	JD 26	SB - MISC
27	JD	JD 27	SB - SMB BUS CONNECTIONS
28	PS	JD 28	DDR2 - SO-DIMM CONN A
29	PS	JD 29	DDR2 - SO-DIMM CONN B (REVERSED)
30	PS	JD 30	DDR2 - TERMINATION
M1 31	RT	RT 31	DDR2 - VTT SUPPLY
M42 33	JD	JD 32	CLOCKS - GENERATOR
34	JD	JD 33	CLOCKS - TERMINATIONS
38	JD	JD 34	ATA (SATA AND IDE) CONN'S
(M42) 41	JD	JD 35	LAN - YUKON'S PCIE INTERFACE
42	JD	JD 36	LAN - YUKON'S PWR, MISC
43	JD	JD 37	LAN - CONN
44	JD	JD 38	FIREWIRE - FW323-06
45	JD	JD 39	FIREWIRE - DECAPS
46	JD	JD 40	FIREWIRE - CONN'S
47	JD	JD 41	USB - CONN'S

PAGE	DRI	PDF	CIRCUIT
53	JD	JD 43	PCI-E - AIRPORT MINI-PCIE CONN
54	JD	JD 44	PCI-E - UNUSED PORTS
58	MS	MS 45	SMC - H8S2116
59	MS	MS 46	SMC - SMB BUSSES, MISC
60	MS	MS 47	SMC - LPC+ CONN
61	JH	JH 48	SMC - GPU/NB THERMAL SENSOR
RX 63	MS	JD 49	SMC - SPI BOOTROM
65	MS	MS 50	SMC - FANS
66	MS	MS 51	SMC - FANS
67	JD	JD 52	SMC - TPM
SO 68	PT	JD 53	AUDIO - CODEC, VREG, MIC BIAS
SO 72	PT	JD 54	AUDIO - INTERNAL SPEAKER AMP
SO 73	PT	JD 55	AUDIO - I/O CONN'S, EMC
SO 74	PT	JD 56	AUDIO - DETECT TRANSLATORS
RP 75	RT	RT 57	VR - CPU CORE
RP 76	RT	RT 58	VR - CPU I-V SENSE CKT
RP 77	RT	RT 59	VR - "S0" 1.2V & 2.5V (GRAFIX)
RP 78	RT	RT 60	VR - "S0" 1.8V
RP 79	RT	RT 61	VR - "S3" 1.8V
RP 80	RT	RT 62	VR - "S0" 1.5V
RP 81	RT	RT 63	VR - "S0" 1.05V
RP 83	RT	RT 64	VR - "S3" 3.3V AND 5V
JH 84	JH	JH 65	GPU - M56 PCI-E
M1 85	JH	JH 66	GPU - VCORE SUPPLY
M1 86	JH	JH 67	GPU - M56 CORE PWR
M1 87	JH	JH 68	GPU - M56 FRAME BUFFER
M1 88	JH	JH 69	GPU - MISC
M1 89	JH	JH 70	GPU - GDDR SDRAM A
M1 90	JH	JH 71	GPU - GDDR SDRAM B
M1 91	JH	JH 72	GPU - M56 GPIO, DVO, MISC
M1 92	JH	JH 73	GPU - M56 CLOCKS
M1 93	JH	JH 74	GPU - M56 VIDEO INTERFACES
JH 94	JH	JH 75	GPU - INTERNAL DISPLAY CONN'S
JH 95	JH	JH 76	GPU - TP'S
JH 96	JH	JH 77	GPU - TMDS, INVERTER, EXT VGA
JH 97	JH	JH 78	GPU - EXTERNAL DISPLAY CONN'S

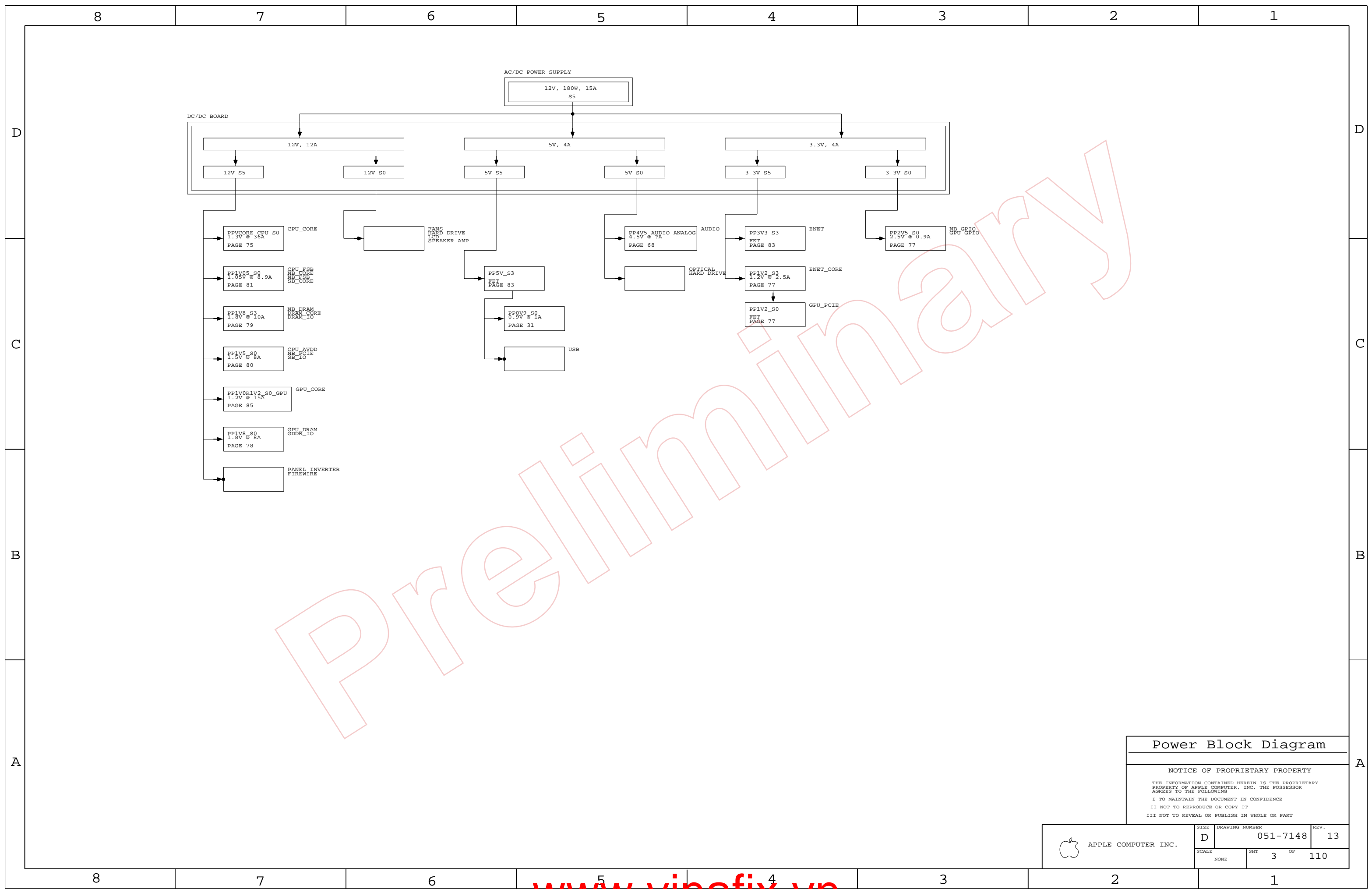
<p style="font-size: small;">DIMENSIONS ARE IN MILLIMETERS</p> <p>XX : _____</p> <p>X.XX : _____</p> <p>X.XXX : _____</p> <p>ANGLES : _____</p> <p style="font-size: x-small;">DO NOT SCALE DRAWING</p> <div style="text-align: center;"> <p style="font-size: x-small;">THIRD ANGLE PROJECTION</p> </div>	<p><b>METRIC</b></p>	<div style="text-align: right;"> <p>Apple Computer Inc.</p> </div> <p style="font-size: x-small; text-align: center;">NOTICE OF PROPRIETARY PROPERTY</p> <p style="font-size: x-small; text-align: center;">THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING</p> <p style="font-size: x-small; text-align: center;">I TO MAINTAIN THE DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART</p> <p style="text-align: center; font-weight: bold; font-size: large;">SCH, MLB, M38A</p> <p style="font-size: x-small; text-align: center;">DRAWING NUMBER <span style="float: right;">REV. 13</span></p> <p style="font-size: x-small; text-align: center;">SHT 1 OF 110</p>
<p>DRAPTR</p> <p>ENG APPD</p> <p>QA APPD</p> <p>RELEASE</p>	<p>DESIGN CK</p> <p>MFG APPD</p> <p>DESIGNER</p> <p>SCALE</p>	<p>TITLE</p> <p>SIZE D</p>



### System Block Diagram

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APPLE COMPUTER INC.	SIZE <b>D</b>	DRAWING NUMBER <b>051-7148</b>	REV. <b>13</b>
	SCALE NONE	SHEET <b>2</b>	OF <b>110</b>



Preliminary

**Power Block Diagram**

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	D	051-7148	13
SCALE	SHT	OF	
NONE	3	110	

8

7

6

5

4

3

2

1

COMMON

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
511S0025	1	IC,CPU-SKT,479BGA	J0700	CRITICAL	
338S0328	1	IC,945PM,NORTHBRIDGE	U1200	CRITICAL	
343S0385	1	IC,SB,652BGA	U2100	CRITICAL	
338S0344	1	IC,ATI,M56P,GRAFIXCTLR,880BGA,LF	U8400	CRITICAL	
359S0101	1	IC,CY28445-5,CLK GEN,68PIN QFN	U3301	CRITICAL	
338S0270	1	IC,88E8053,1GIGABIT ENET XCVR,64P QFN,SMD	U4101	CRITICAL	
(335S0382) 341S1797	1	IC,ENET LAN ROM	U4102	CRITICAL	
338S0279	1	IC,FW32306,1394A LINK,TQFP	U4400	CRITICAL	

341S1789	1	IC,TPM,TSSOP,28P	U6700	CRITICAL	LEMENU
UNSCREENED P/N 353S1465	1	IC,CPU VREG,IMVP,TWO PHASE	U7500	CRITICAL	

128S0078	3	CAP,EL,AL,330UF,20V,16V,10X12.7MM,SMD,LF	C7517,C7518,C7910	CRITICAL	
825-6447	1	MLB LABEL,48.0X4.8	X14	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
126S0096	126S0076		C7801	SANYO W16CK680EX 680UF 16V LP
126S0086	126S0078		C699,C940,C1900,C1901,C1968	SANYO W6CE330F8 330UF 6.3V LP
128S0080	128S0078		C7517,C7518,C7910	SANYO 16SVV330W 330UF 16V SMD LP
124-0338	124-0333		C7501,C8014	CAP,AL,EL,680UF,16V,RAD,10X12.5MM
138S0580	138S0552			22UF 0805
353S1321	353S1105		U7910	LM339
378S0141	378S0140		LED01,LED02,LED03	SMD
353S1461	353S1465		U7500	CPU REGULATOR - ISL9504

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-7148	1	PCB,SCHM,MLB,M38A	SCH1		17_INCH_LCD
820-2052	1	PCB,FAB,MLB,M38A	MLB1		17_INCH_LCD
341T0040	1	EFI ROM,M38A	U6301	CRITICAL	17_INCH_LCD
114S0264	1	3.01K,1%,1/16W,402,MF-LF	R8522		GPU_VCORE_1P2V
(341S1908 - DEVEL) (341S1909 - FINAL) (335S0384 - BLNK) 341T0039	1	IC,SMC,M38A	U5800	CRITICAL	17_INCH_LCD
338S0315	1	IC,ATI,M56LP,GRAFIX CTLR,880BGA,LF	U8400	CRITICAL	GPU_B26_LP
114S0287	1	5.11K,1%,1/16W,402,MF-LF	R8522		GPU_VCORE_0P953V
114S0281	1	4.53K,1%,1/16W,402,MF-LF	R8522		GPU_VCORE_1P0V
337S3299	1	2.00GHZ MEROM	CPU	CRITICAL	2P00_CPU
337S3293	1	2.16GHZ MEROM	CPU	CRITICAL	2P16_CPU

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
333S0354	4	IC,SURAM,GDDR3,8MX32,700MHZ,136FBGA	U8900,U8950,U9000,U9050	CRITICAL	ATI_FB_128M_SAMSUNG
333S0358	4	IC,SURAM,GDDR3,8MX32,700MHZ,136FBGA	U8900,U8950,U9000,U9050	CRITICAL	ATI_FB_128M_HYNIX
333S0376	4	IC,SURAM,GDDR3,8MX32,700MHZ,136FBGA	U8900,U8950,U9000,U9050	CRITICAL	ATI_FB_128M_INFINEON

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
333S0350	4	IC,SURAM,GDDR3,16MX32,700MHZ,136FBGA	U8900,U8950,U9000,U9050	CRITICAL	ATI_FB_256M_SAMSUNG
333S0351	4	IC,SURAM,GDDR3,16MX32,700MHZ,136FBGA	U8900,U8950,U9000,U9050	CRITICAL	ATI_FB_256M_HYNIX
333S0377	4	IC,SURAM,GDDR3,16MX32,700MHZ,136FBGA	U8900,U8950,U9000,U9050	CRITICAL	ATI_FB_256M_INFINEON

Table Items

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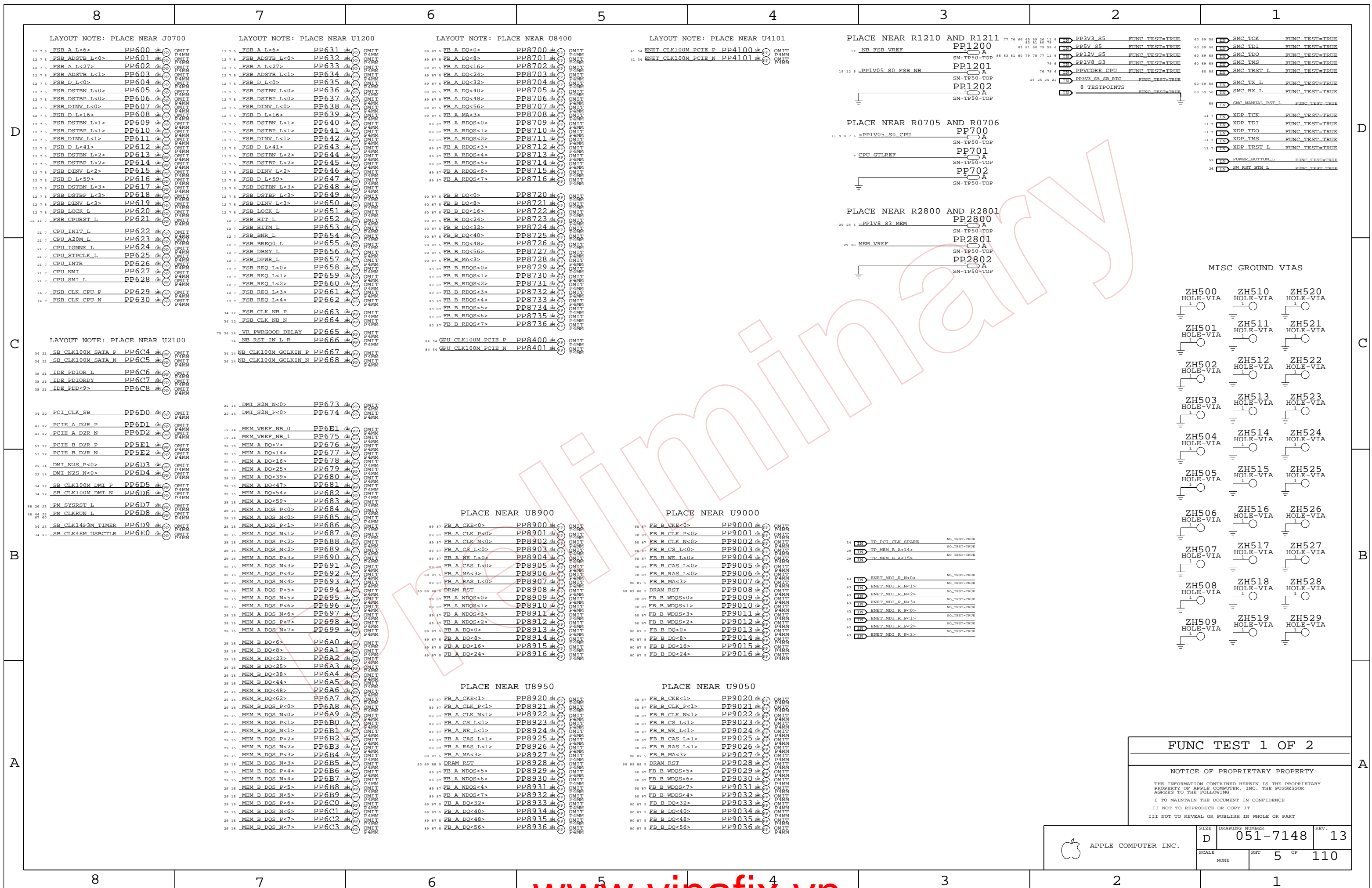
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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7148	13
SCALE	SHT	OF
NONE	4	110



LAYOUT NOTE: PLACE NEAR J0700

LAYOUT NOTE: PLACE NEAR U1200

LAYOUT NOTE: PLACE NEAR U8400

LAYOUT NOTE: PLACE NEAR U4101

PLACE NEAR R1210 AND R1211

PLACE NEAR R0705 AND R0706

PLACE NEAR R2800 AND R2801

MISC GROUND VIAS

PLACE NEAR U8900

PLACE NEAR U9000

PLACE NEAR U8950

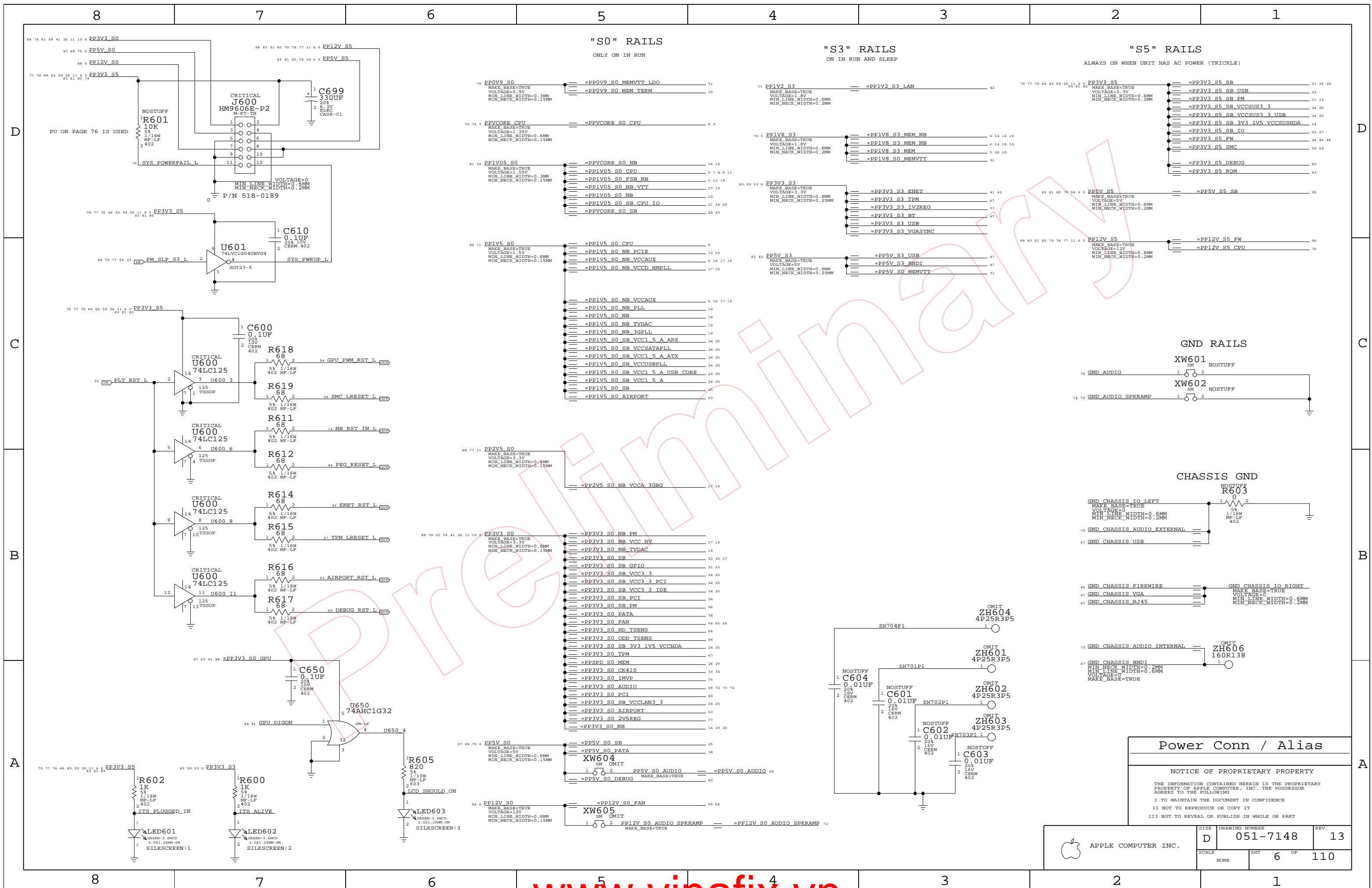
PLACE NEAR U9050

FUNC TEST 1 OF 2

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SCALE	SHEET	OF	
NONE	5	110	

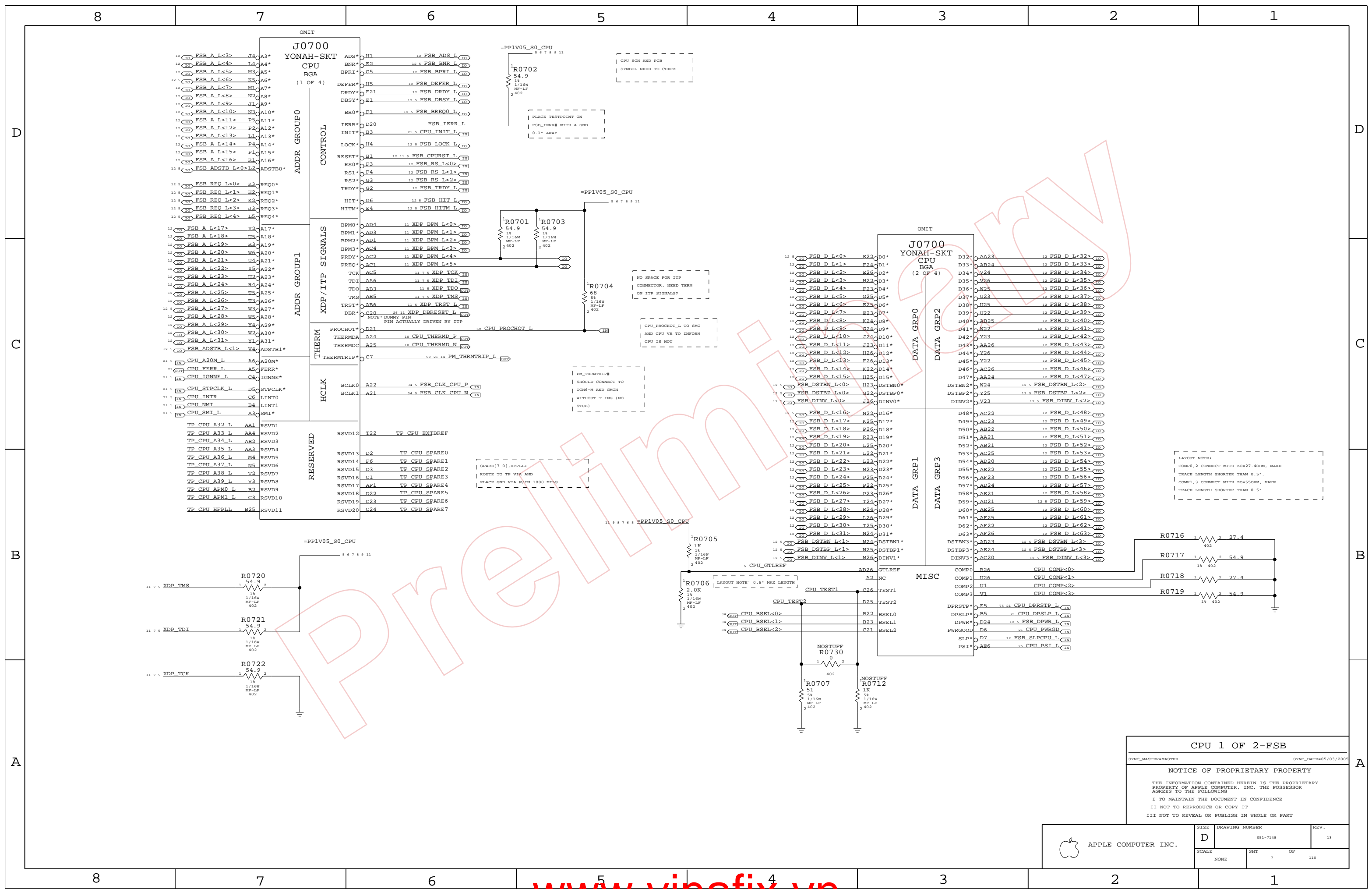


**Power Conn / Alias**

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	SCALE NONE	SHEET 6 OF 110	



**CPU 1 OF 2-FSB**

SYNC\_MASTER=MASTER SYNC\_DATE=05/03/2005

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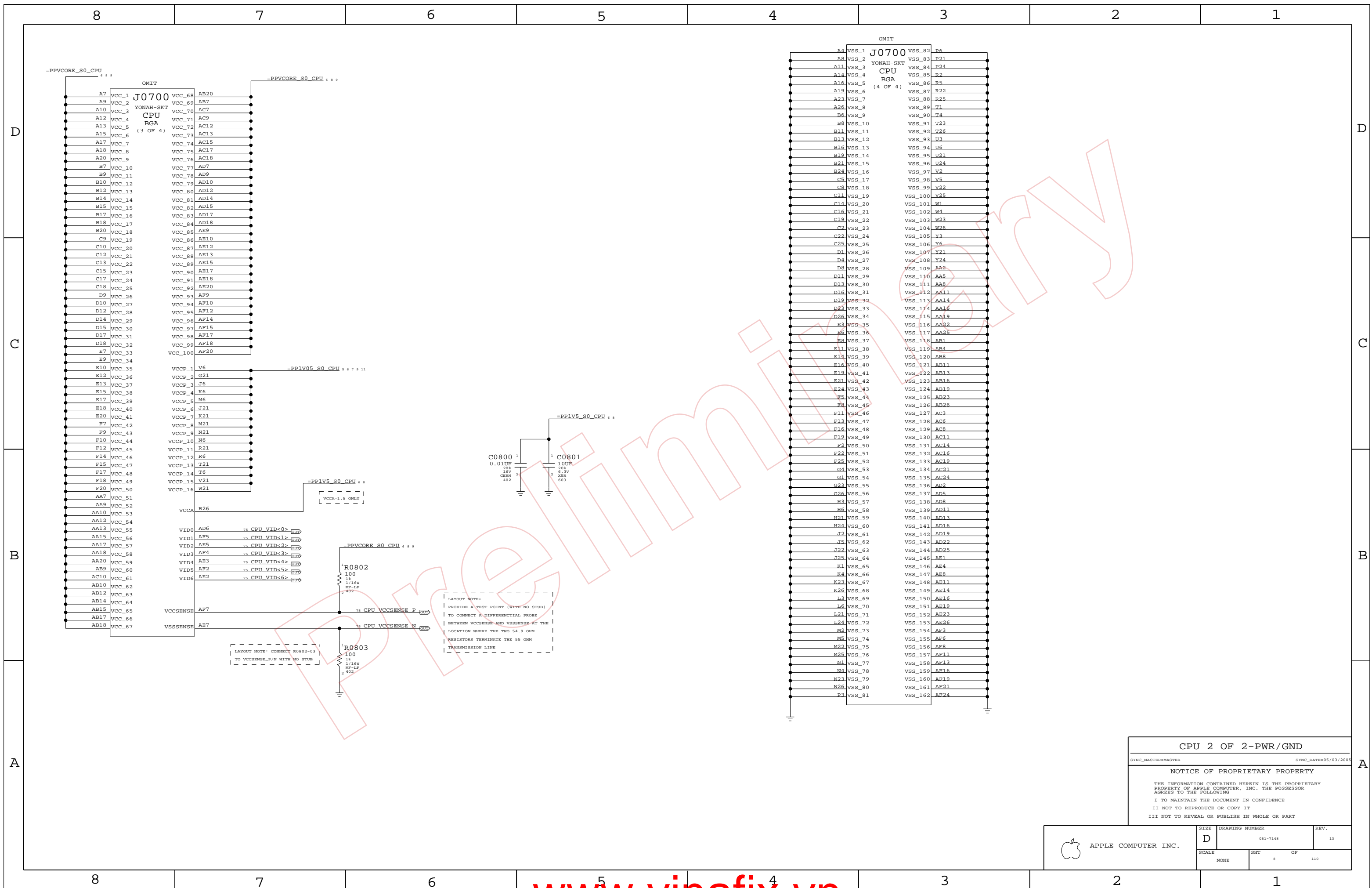
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SCALE	SHT	OF	110
NONE	7		



**CPU 2 OF 2-PWR/GND**

SYNC\_MASTER=MASTER SYNC\_DATE=05/03/2005

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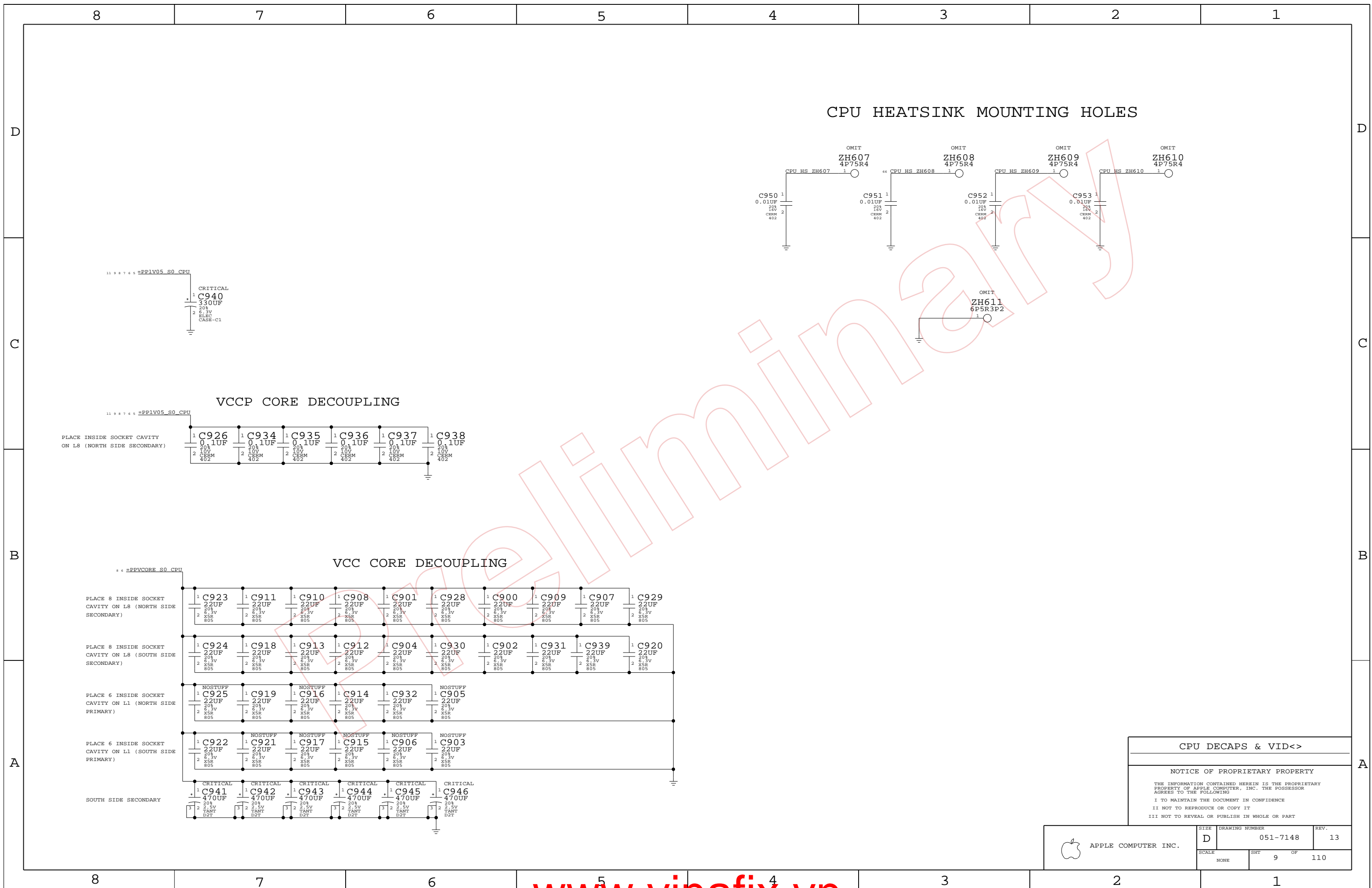
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	D	051-7148	13
SCALE	SHT OF		REV.
NONE	8 OF 110		





**CPU DECAPS & VID<>**


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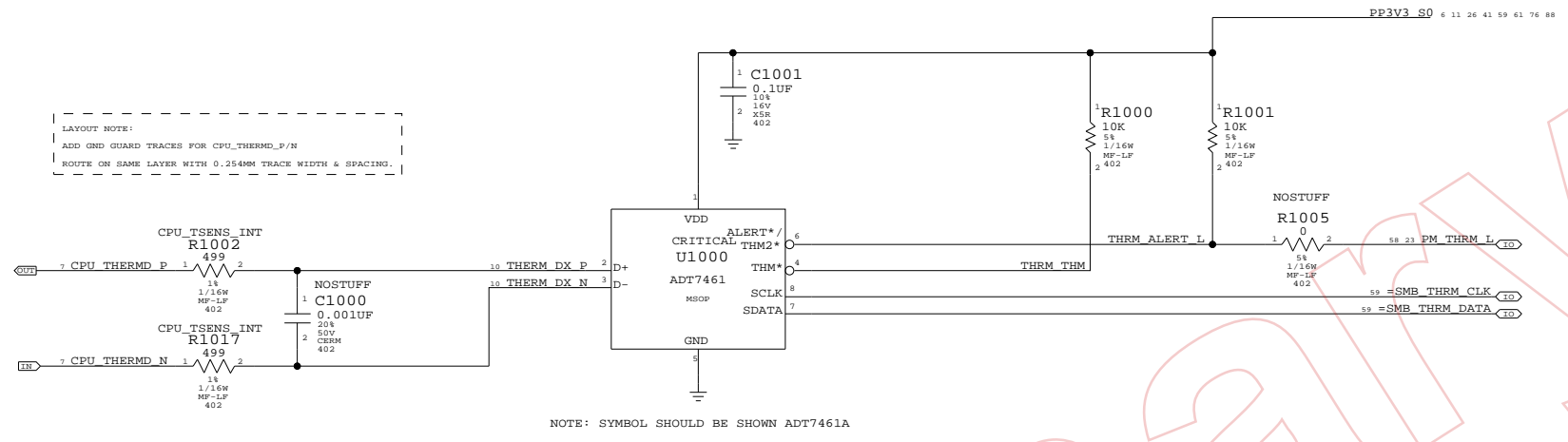
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	D	051-7148	13
SCALE	SHT	OF	REV.
NONE	9	110	

# CPU THERMAL SENSOR

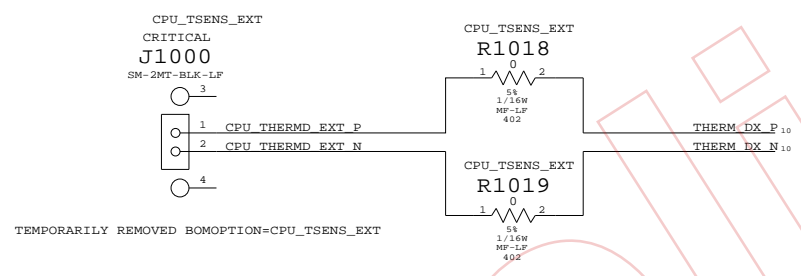
NOTE:  
IF CPU T DIODE TO BE READ IN OFF STATE,  
THEN THIS SHOULD BE S5

LAYOUT NOTE:  
ADD GND GUARD TRACKS FOR CPU\_THERMD\_P/N  
ROUTE ON SAME LAYER WITH 0.254MM TRACE WIDTH & SPACING.



NOTE: SYMBOL SHOULD BE SHOWN ADT7461A

LAYOUT NOTE:  
PLACE R1002 AND R1018 SUCH THAT THEY SHARE ONE PAD  
PLACE R1017 AND R1019 SUCH THAT THEY SHARE ONE PAD



TEMPORARILY REMOVED BOMOPTION=CPU\_TSENS\_EXT

CPU TEMP SENSOR

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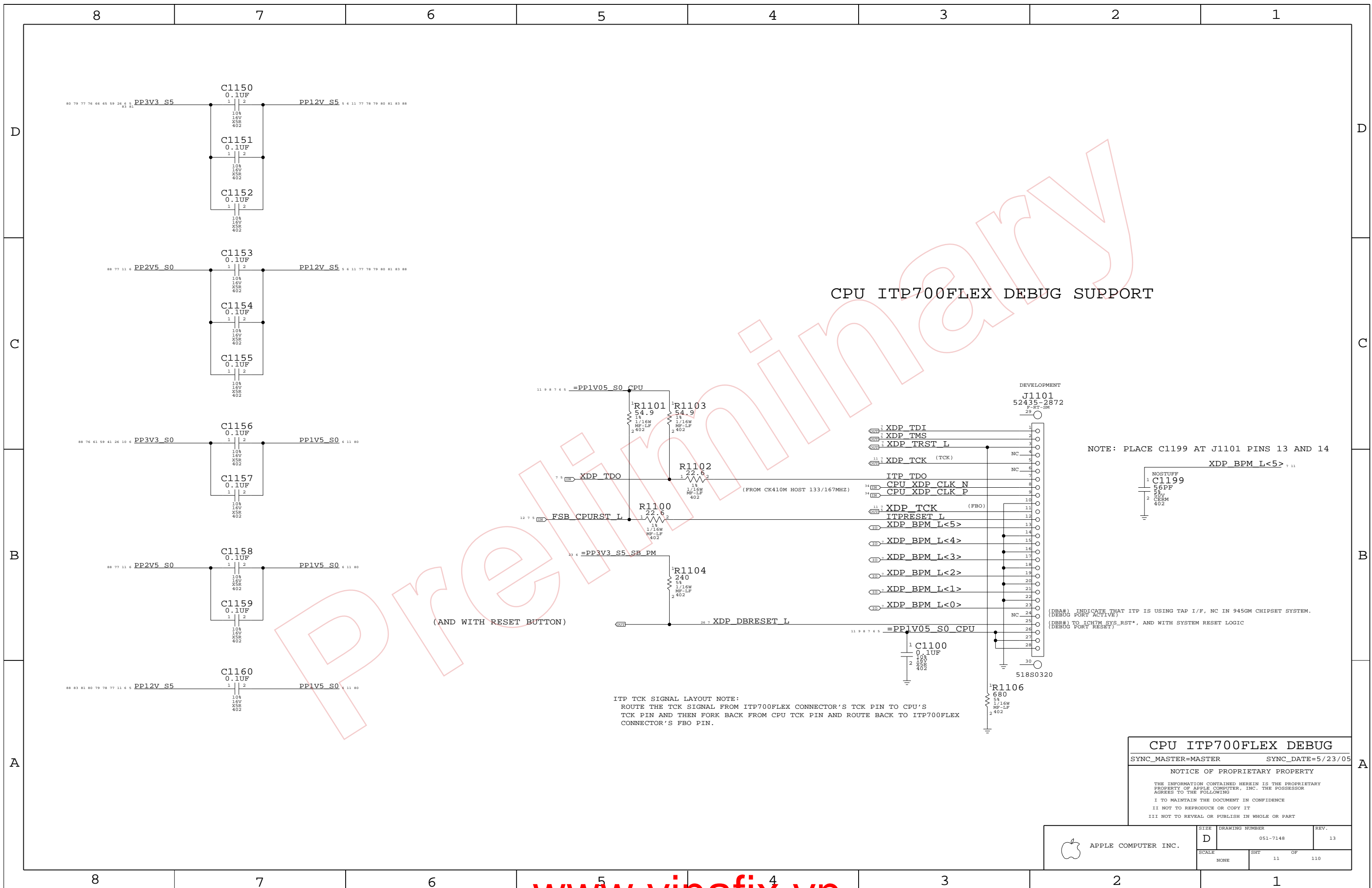
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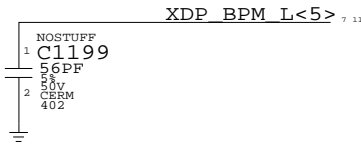
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	D	051-7148	13
SCALE	SHT		OF
NONE	10		110



CPU ITP700FLEX DEBUG SUPPORT

NOTE: PLACE C1199 AT J1101 PINS 13 AND 14

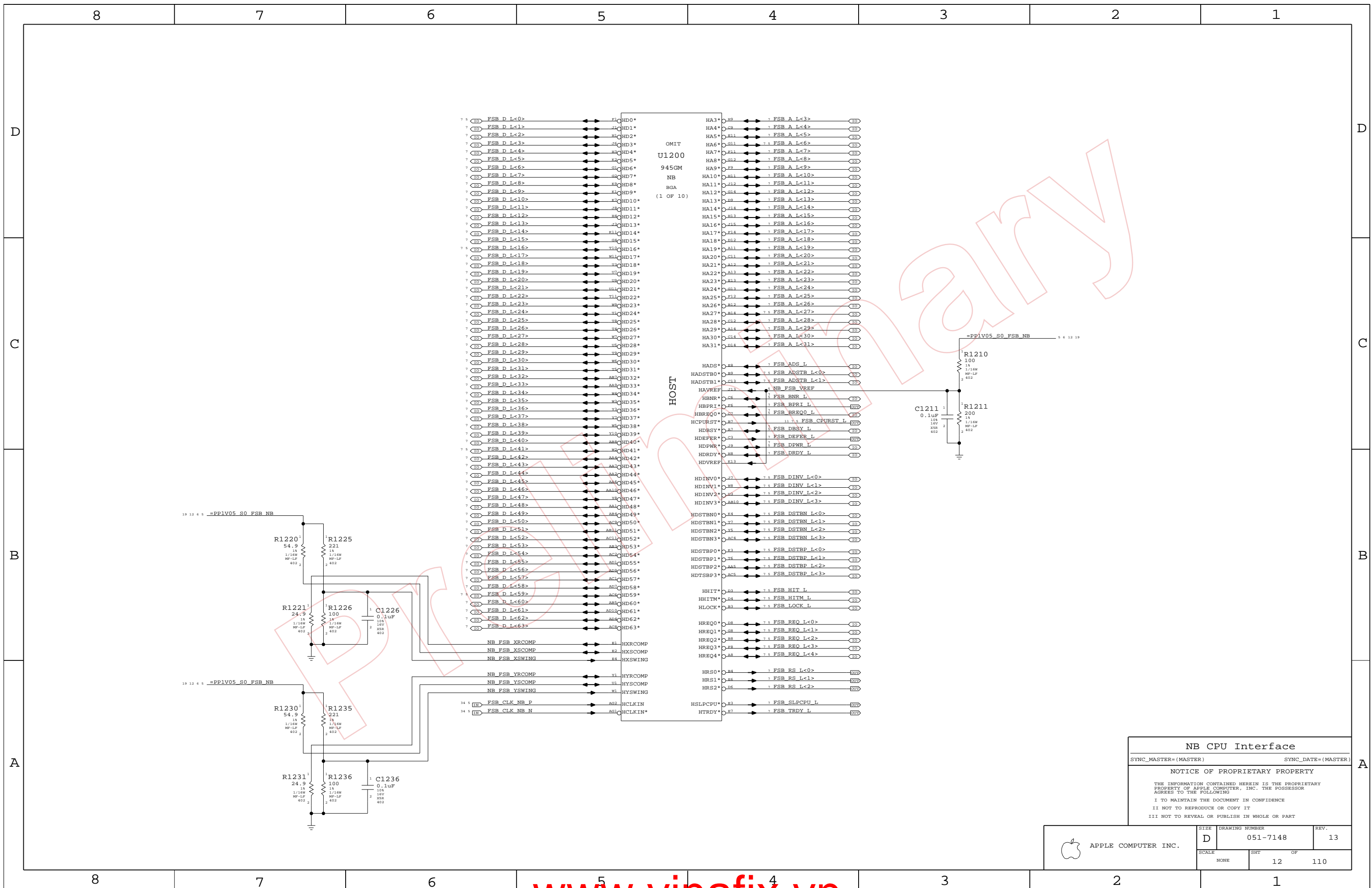


(DBA#) INDICATE THAT ITP IS USING TAP I/F, NC IN 945GM CHIPSET SYSTEM.  
 (DBB#) TO ICH7M SYS\_RST\*, AND WITH SYSTEM RESET LOGIC  
 (DBB#) TO ICH7M SYS\_RST\*, AND WITH SYSTEM RESET LOGIC  
 (DBB#) TO ICH7M SYS\_RST\*, AND WITH SYSTEM RESET LOGIC

ITP TCK SIGNAL LAYOUT NOTE:  
 ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S  
 TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX  
 CONNECTOR'S FBO PIN.

**CPU ITP700FLEX DEBUG**  
 SYNC\_MASTER=MASTER SYNC\_DATE=5/23/05  
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SCALE	SHT	OF	110
NONE	11		



**NB CPU Interface**

SYNC\_MASTER=(MASTER)      SYNC\_DATE=(MASTER)

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APPLE COMPUTER INC.	SIZE <b>D</b>	DRAWING NUMBER 051-7148	REV. 13
	SCALE NONE	SHEET 12	OF 110

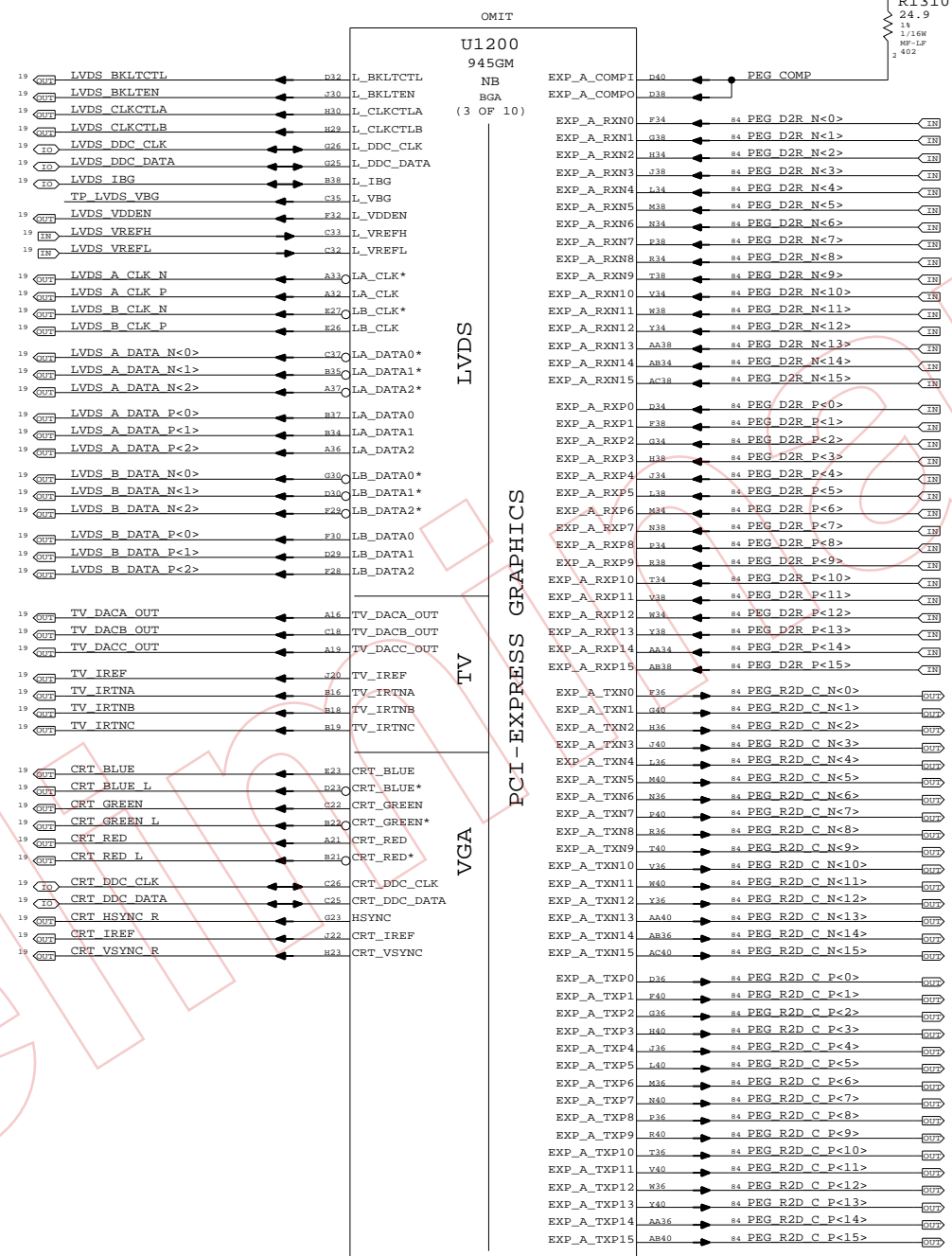
**LVDS Disable**  
 Can leave all signals NC if LVDS is not implemented  
 Tie VCC\_TXLVDS and VCCA\_LVDS to GND. If SDVO is used  
 VCCD\_LVDS must remain powered with proper decoupling.  
 Otherwise, tie VCCD\_LVDS to GND also.

**TV-Out Signal Usage:**  
 Composite: DACA only  
 S-Video: DACB & DACC only  
 Component: DACA, DACB & DACC

Unused DAC outputs must remain powered, but can omit  
 filtering components. Unused DAC outputs should  
 connect to GND through 75-ohm resistors.

**TV-Out Disable**  
 Tie DACx\_OUT, IRTNx, and IREF to 1.5V power rail.  
 Tie VCCD\_TVDAC, VCCD\_QTVDAC, VCCA\_TVDACx, and  
 VCCA\_TVVBG to 1.5V power rail. Tie VSSA\_TVVBG to GND.

**CRT Disable**  
 Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie  
 HSYNC and VSYNC to GND. Tie VCCA\_CRTDAC to VCC Core  
 rail, and tie VSSA\_CRTDAC and VCC\_SYNC to GND.



SDVO Alternate Function  
 SDVO\_TVCLKIN#  
 SDVO\_INT#  
 SDVO\_FLDSTALL#

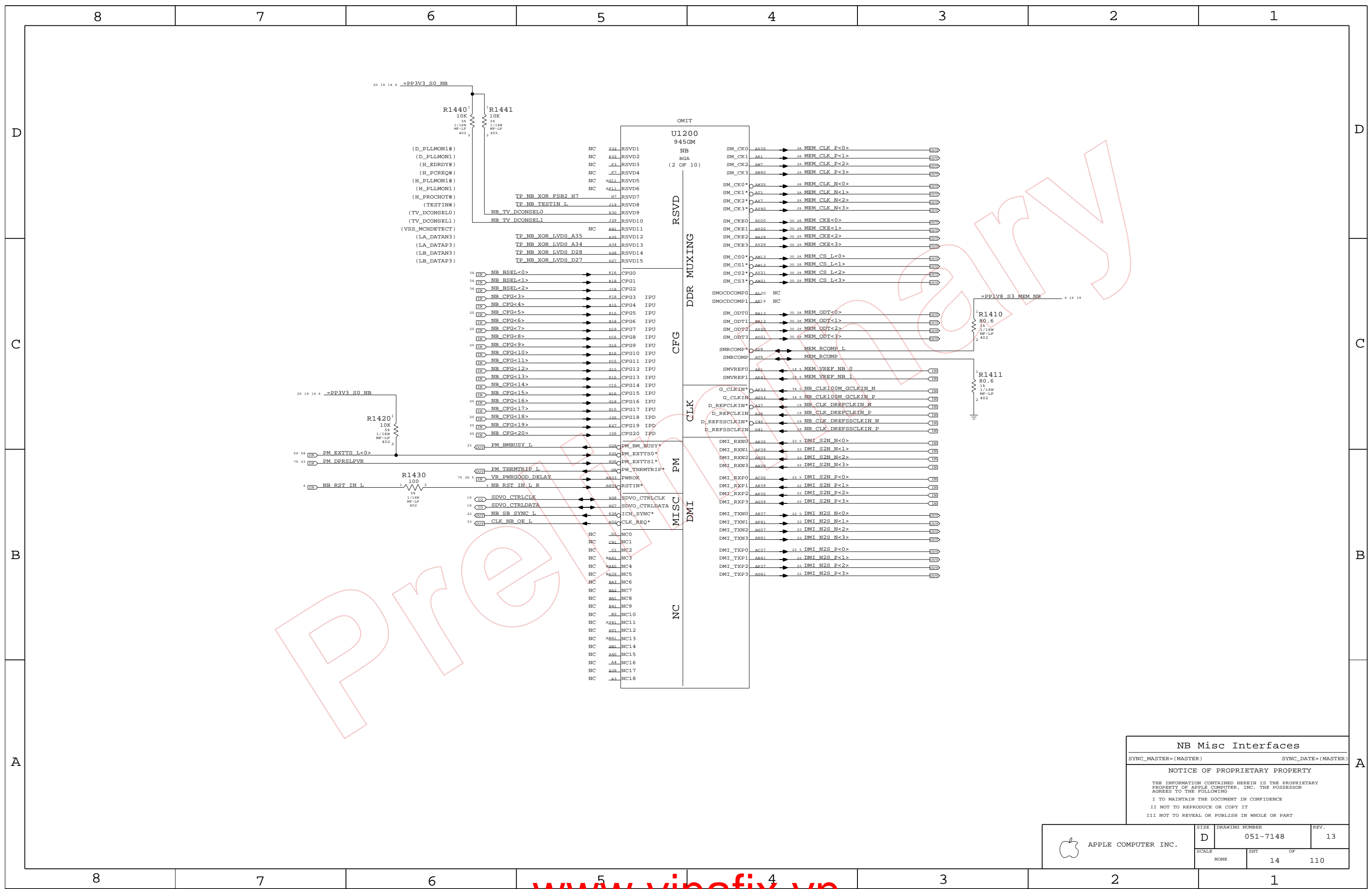
SDVO\_TVCLKIN  
 SDVO\_INT  
 SDVO\_FLDSTALL

SDVOB\_RED#  
 SDVOB\_GREEN#  
 SDVOB\_BLUE#  
 SDVOB\_CLKN  
 SDVOC\_RED#  
 SDVOC\_GREEN#  
 SDVOC\_BLUE#  
 SDVOC\_CLKN

SDVOB\_RED  
 SDVOB\_GREEN  
 SDVOB\_BLUE  
 SDVOB\_CLKP  
 SDVOC\_RED  
 SDVOC\_GREEN  
 SDVOC\_BLUE  
 SDVOC\_CLKP

**NB PEG / Video Interfaces**  
 SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)  
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SCALE	SHT OF		
NONE	13		110



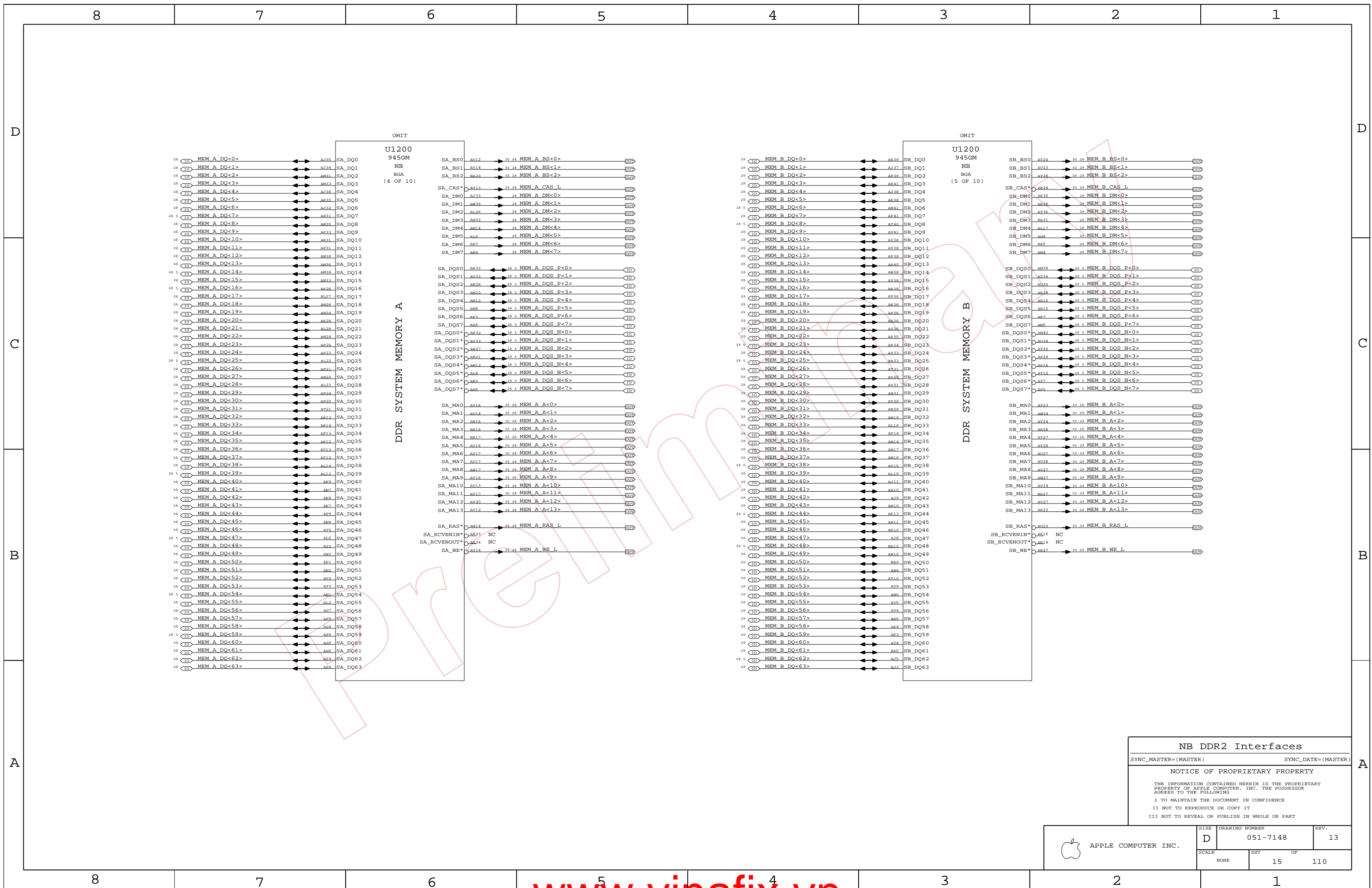
**NB Misc Interfaces**

SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	13
SCALE	SHT OF		
NONE	14		110



**NB DDR2 Interfaces**

SYNC\_MASTER=(MASTER)      SYNC\_DATE=(MASTER)

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	D	051-7148	13
SCALE	SHT	OF	
NONE	15	110	

NCTF balls are Not Critical To Function

These connections can break without impacting part performance.

OMIT

D

D

C

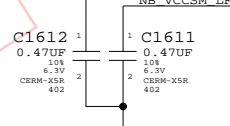
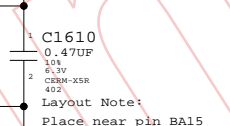
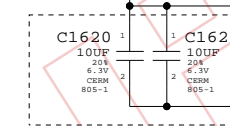
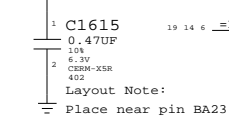
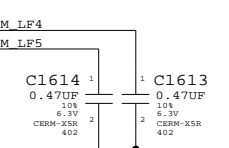
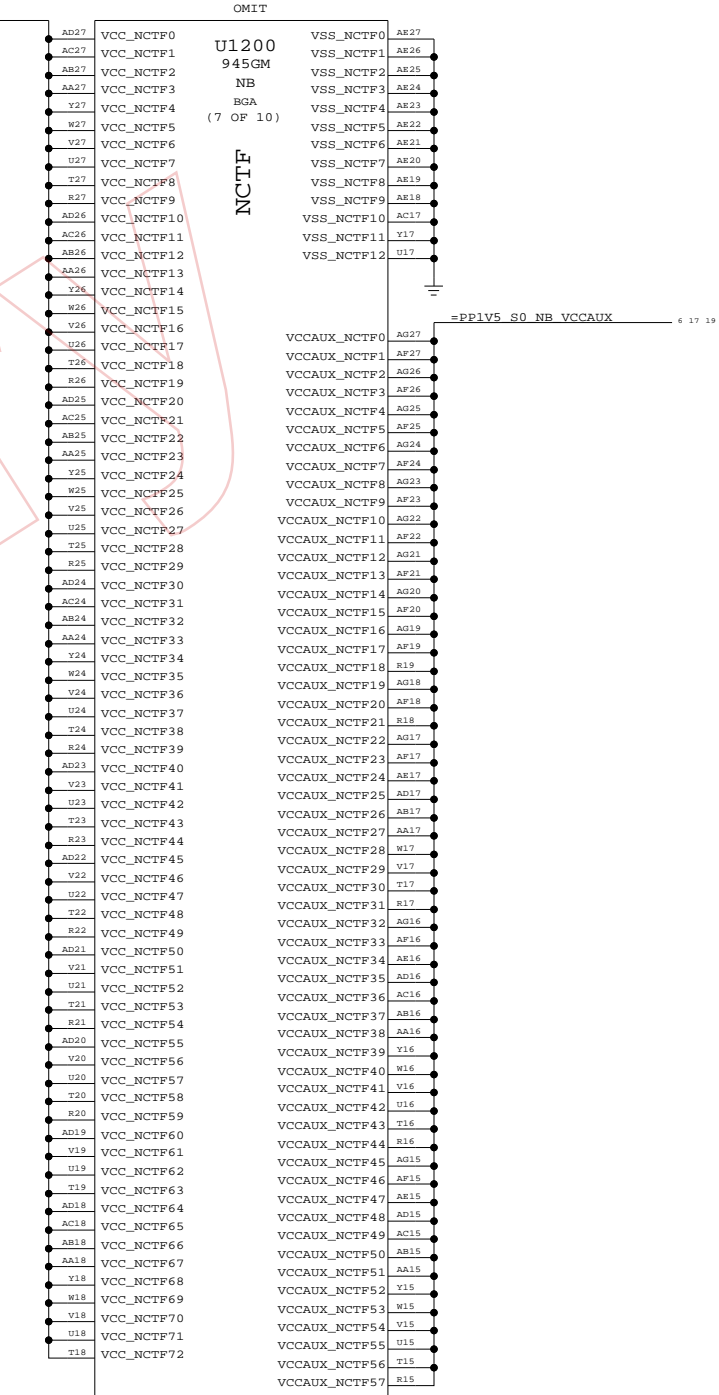
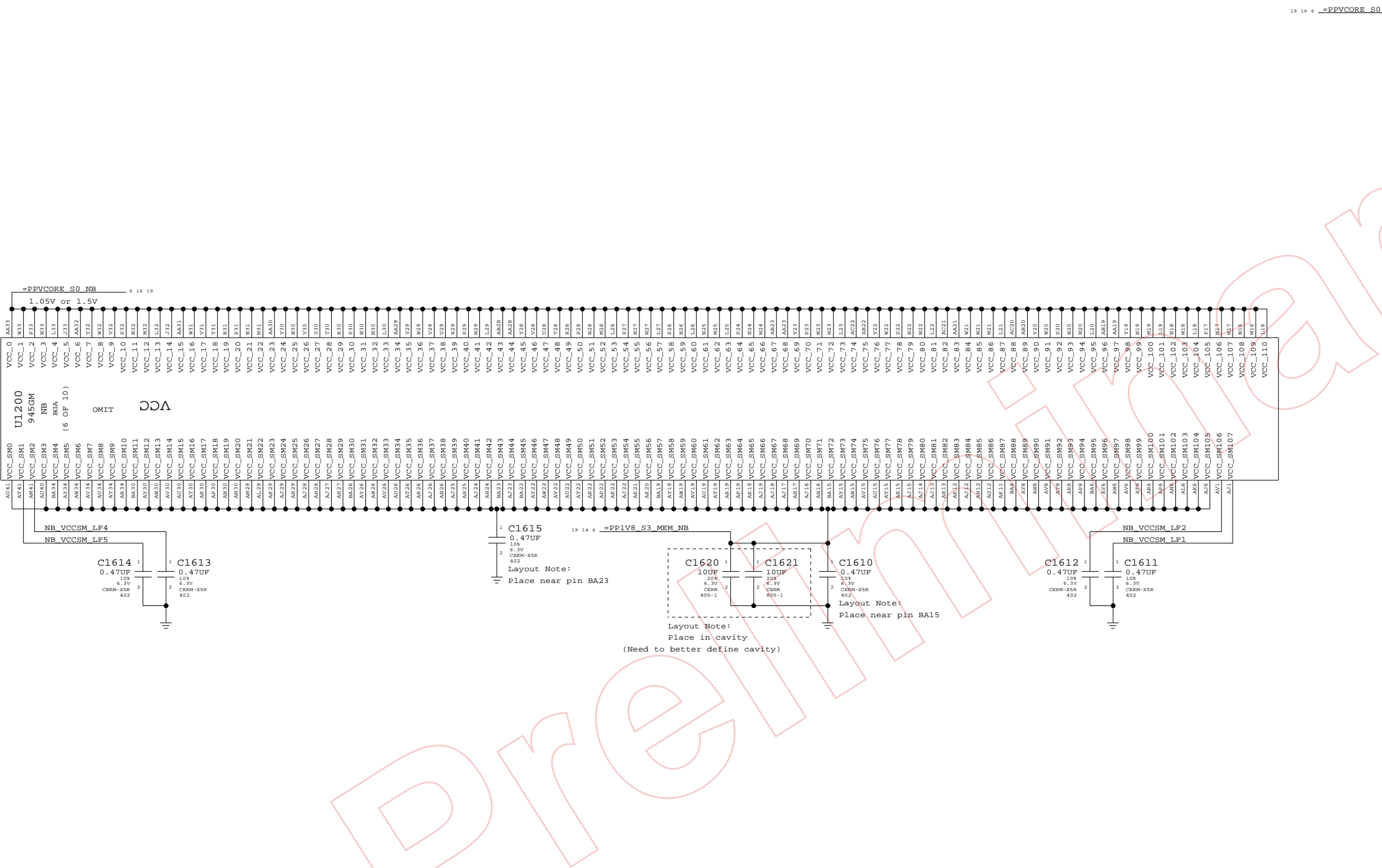
C

B

B

A

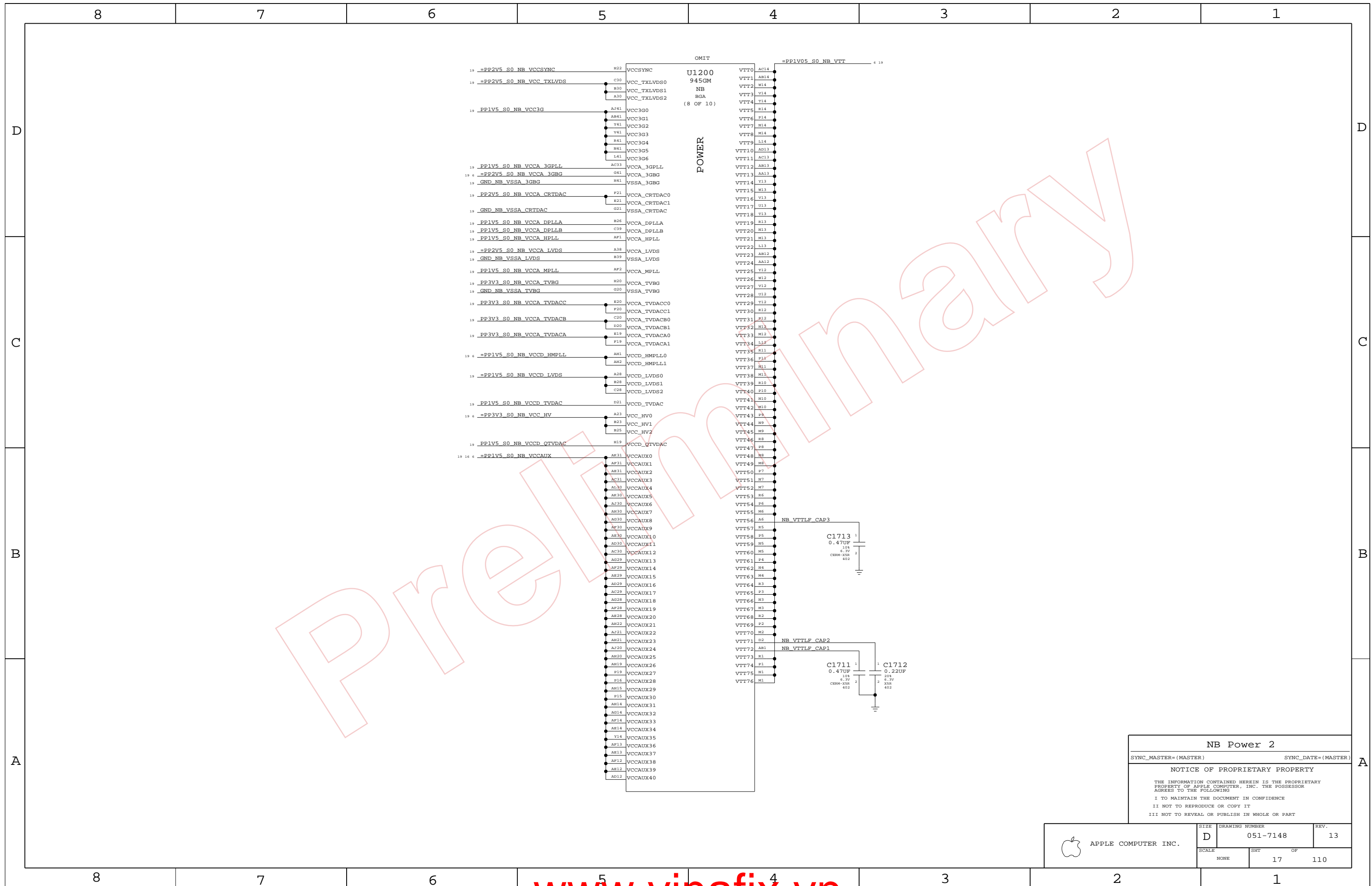
A



NB Power 1  
 SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)  
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	13
SCALE	SHT	OF	
NONE	16	110	





Pre-release material

**NB Power 2**

SYNC\_MASTER=(MASTER)      SYNC\_DATE=(MASTER)

**NOTICE OF PROPRIETARY PROPERTY**

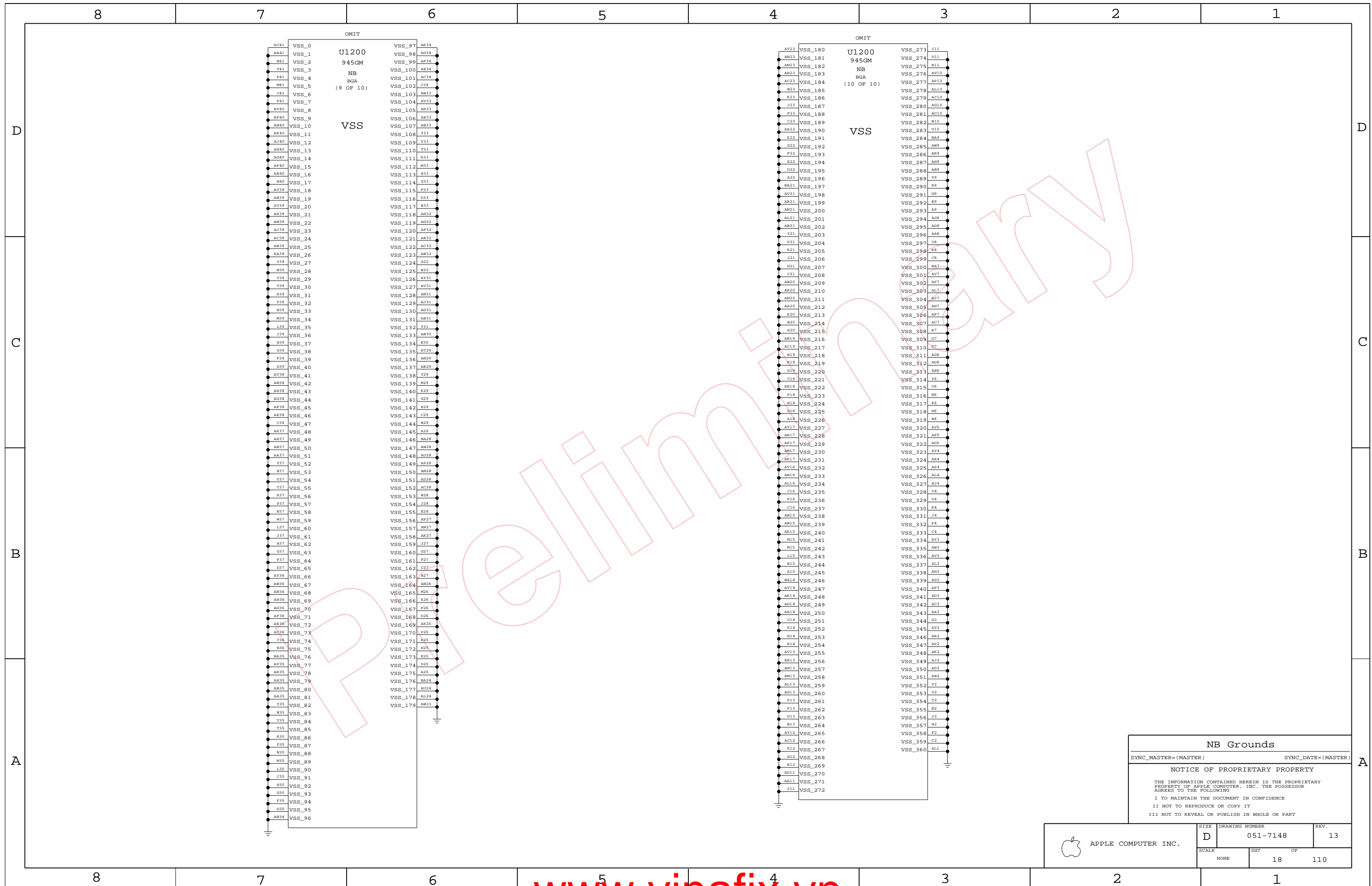
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APPLE COMPUTER INC.	SIZE <b>D</b>	DRAWING NUMBER 051-7148	REV. 13
	SCALE NONE	SHEET 17	OF 110



**NB Grounds**

SYNC\_MASTER=(MASTER)      SYNC\_DATE=(MASTER)

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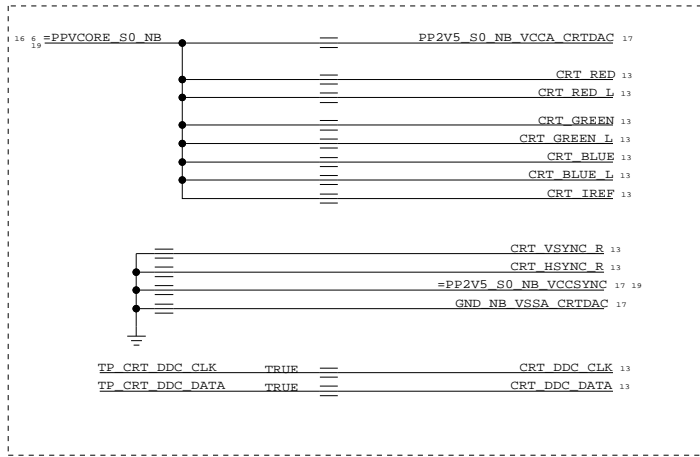
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	13
SCALE	SHT	OF	
NONE	18	110	

### Power Interface

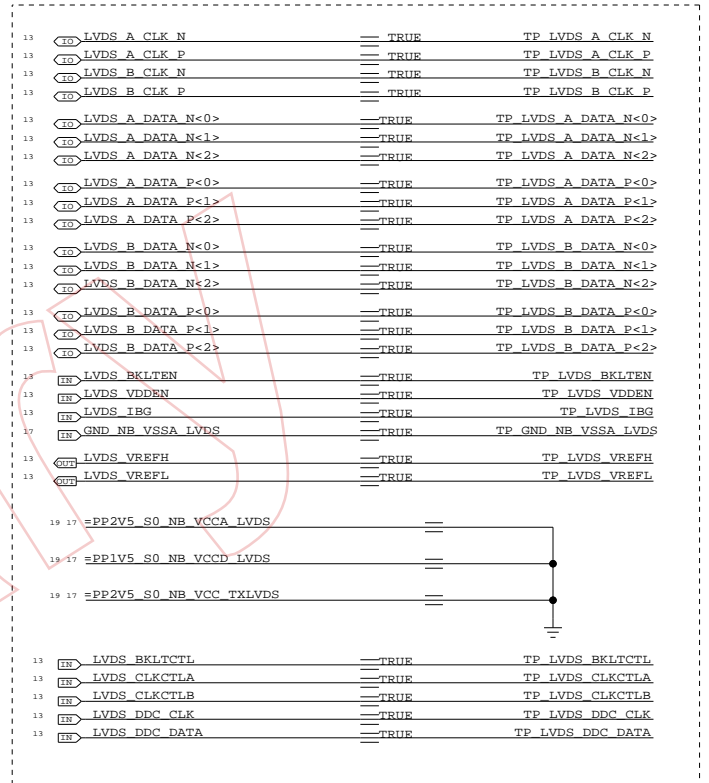
These are the power signals that leave the NB "block"

- =PP1V05\_S0\_FSB\_NB 5 6 12
- =PPVCORE\_S0\_NB 6 16 19
- =PP1V05\_S0\_NB 6 16 19
- =PP1V05\_S0\_NB\_VTT 6 17 19
- =PP1V5\_S0\_NB 6 19
- =PP1V5\_S0\_NB\_PCIE 6 13
- =PP1V5\_S0\_NB\_PLL 6 19
- =PP1V5\_S0\_NB\_TVDAC 6 19
- =PP1V5\_S0\_NB\_VCCD\_HMPLL 6 19
- =PP1V5\_S0\_NB\_VCCD\_LVDS 17 19
- =PP1V5\_S0\_NB\_VCCAUX 6 16 17 19
- =PP1V8\_S3\_MEM\_NB 6 14 16 19
- =PP2V5\_S0\_NB\_VCCSYNCR 17 19
- =PP2V5\_S0\_NB\_VCC\_TXLVDS 17 19
- =PP2V5\_S0\_NB\_VCCA\_3GBG 6 17 19
- =PP2V5\_S0\_NB\_VCCA\_LVDS 17 19
- =PP3V3\_S0\_NB 6 14 20
- =PP3V3\_S0\_NB\_TVDAC 6
- =PP3V3\_S0\_NB\_VCC\_HV 6 17 19

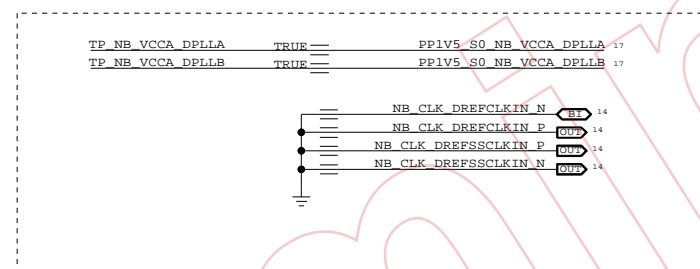
### TVOUT DISABLE



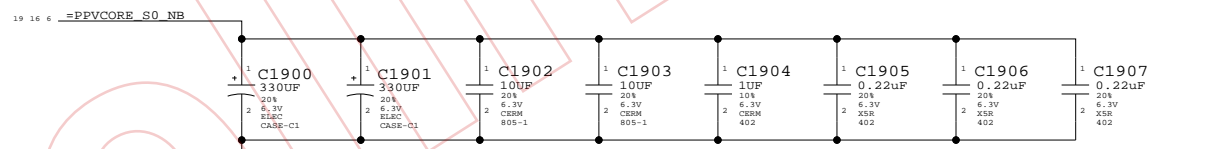
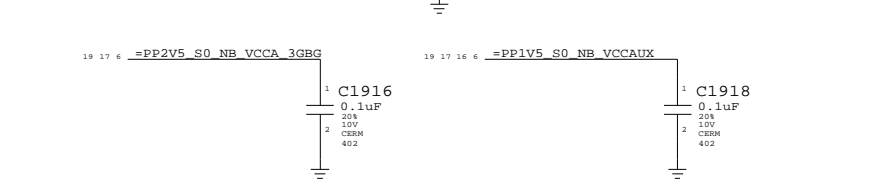
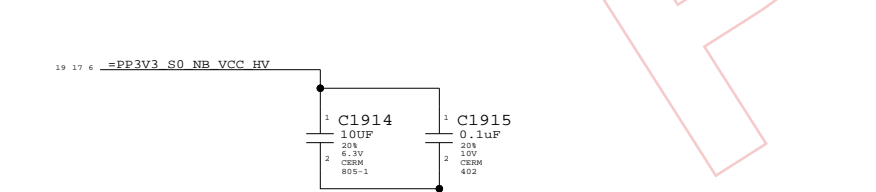
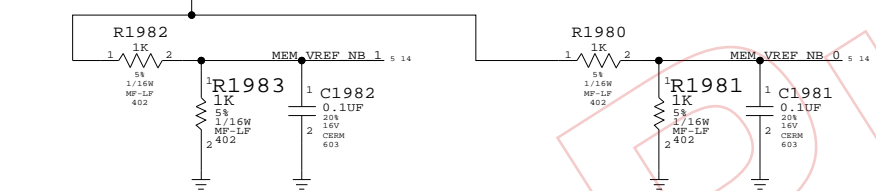
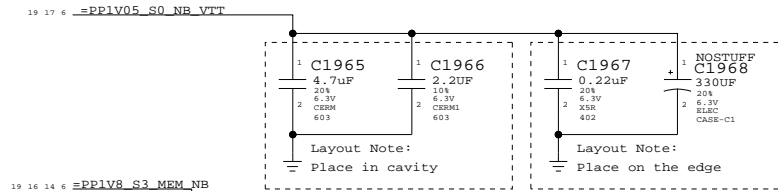
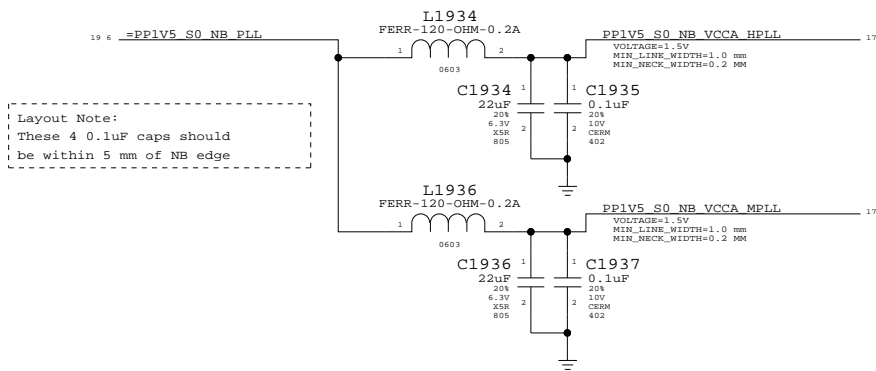
### LVDS DISABLE



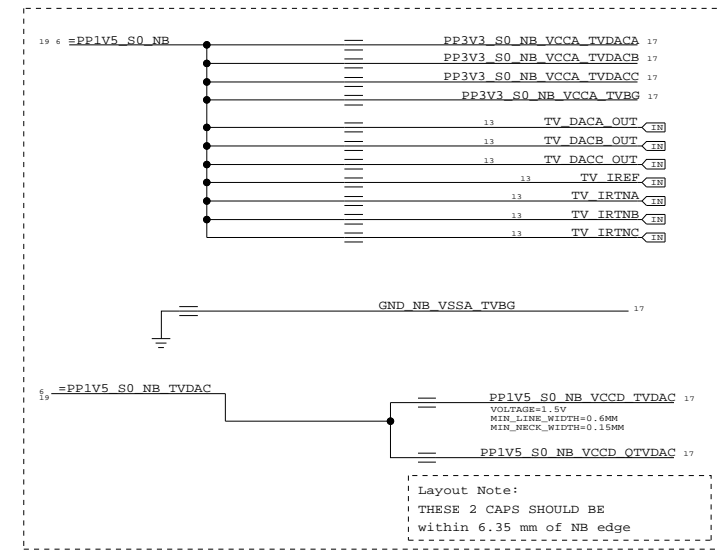
### DISPLAY DISABLE



Layout Note:  
These 4 0.1uF caps should be within 5 mm of NB edge



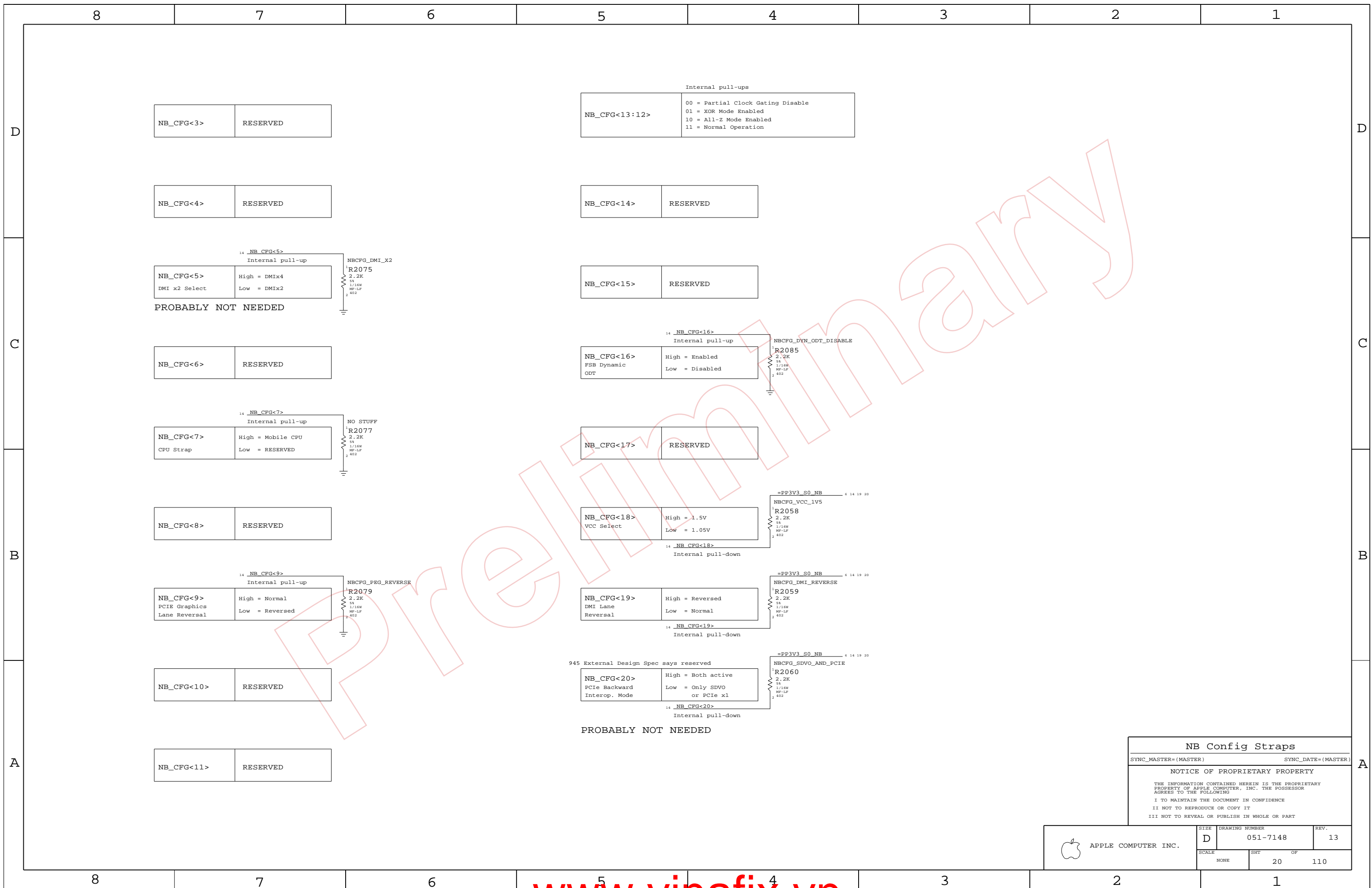
### TVOUT DISABLE



Layout Note:  
THESE 2 CAPS SHOULD BE WITHIN 6.35 mm OF NB EDGE

**NB (GM) Decoupling**  
 SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)  
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	D	051-7148	13
SCALE	NONE	SHT	OF
		19	110



Internal pull-ups

NB_CFG<13:12>	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal Operation
---------------	--

NB_CFG<3>	RESERVED
-----------	----------

NB_CFG<14>	RESERVED
------------	----------

NB_CFG<4>	RESERVED
-----------	----------

14 NB\_CFG<5>  
Internal pull-up

NB_CFG<5>	High = DMiX4 DMI x2 Select Low = DMiX2
-----------	--

PROBABLY NOT NEEDED

NBCFG\_DMI\_X2  
R2075  
2.2K  
5%  
1/16W  
MF-LP  
402

NB_CFG<15>	RESERVED
------------	----------

NB_CFG<6>	RESERVED
-----------	----------

14 NB\_CFG<16>  
Internal pull-up

NB_CFG<16>	High = Enabled FSB Dynamic Low = Disabled ODT
------------	--

NBCFG\_DYN\_ODT\_DISABLE  
R2085  
2.2K  
5%  
1/16W  
MF-LP  
402

14 NB\_CFG<7>  
Internal pull-up

NB_CFG<7>	High = Mobile CPU CPU Strap Low = RESERVED
-----------	--

NO STUFF  
R2077  
2.2K  
5%  
1/16W  
MF-LP  
402

NB_CFG<17>	RESERVED
------------	----------

NB_CFG<8>	RESERVED
-----------	----------

14 NB\_CFG<18>  
Internal pull-down

NB_CFG<18>	High = 1.5V VCC Select Low = 1.05V
------------	--

=PP3V3\_S0\_NB  
NBCFG\_VCC\_LV5  
R2058  
2.2K  
5%  
1/16W  
MF-LP  
402

14 NB\_CFG<9>  
Internal pull-up

NB_CFG<9>	High = Normal PCIe Graphics Lane Reversal Low = Reversed
-----------	---

NBCFG\_PEG\_REVERSE  
R2079  
2.2K  
5%  
1/16W  
MF-LP  
402

14 NB\_CFG<19>  
Internal pull-down

NB_CFG<19>	High = Reversed DMI Lane Reversal Low = Normal
------------	---

=PP3V3\_S0\_NB  
NBCFG\_DMI\_REVERSE  
R2059  
2.2K  
5%  
1/16W  
MF-LP  
402

NB_CFG<10>	RESERVED
------------	----------

945 External Design Spec says reserved

14 NB\_CFG<20>  
Internal pull-down

NB_CFG<20>	High = Both active PCIe Backward Interop. Mode Low = Only SDVO or PCIe x1
------------	---

=PP3V3\_S0\_NB  
NBCFG\_SDVO\_AND\_PCIE  
R2060  
2.2K  
5%  
1/16W  
MF-LP  
402

PROBABLY NOT NEEDED

NB_CFG<11>	RESERVED
------------	----------

**NB Config Straps**

SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)

**NOTICE OF PROPRIETARY PROPERTY**

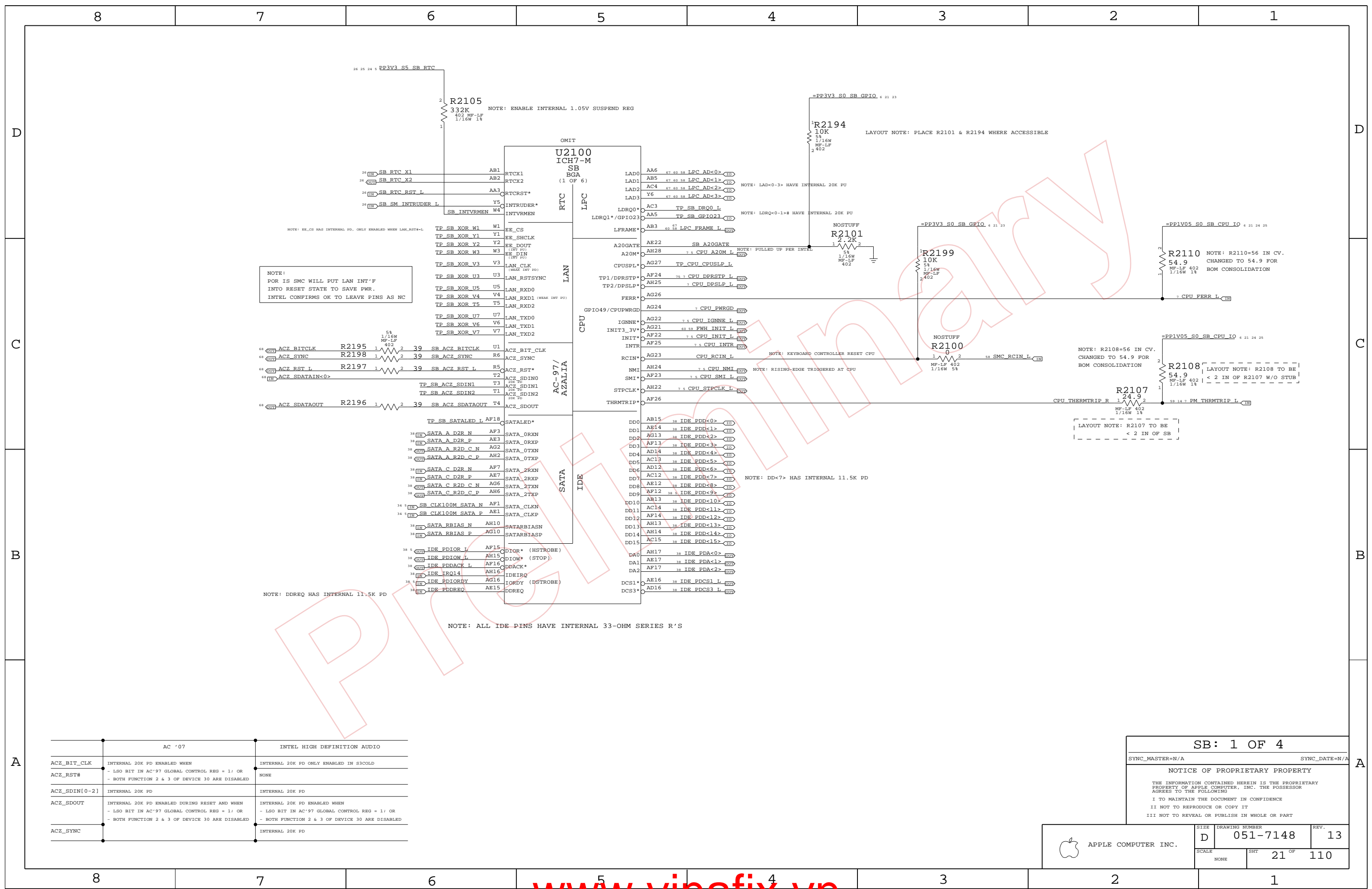
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	13
SCALE	SHT	OF	
NONE	20	110	



NOTE:  
 POR IS SMC WILL PUT LAN INT'F  
 INTO RESET STATE TO SAVE PWR.  
 INTEL CONFIRMS OK TO LEAVE PINS AS NC

NOTE: DDREQ HAS INTERNAL 11.5K PD

NOTE: ALL IDE PINS HAVE INTERNAL 33-OHM SERIES R'S

AC '07	INTEL HIGH DEFINITION AUDIO
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR
ACZ_RST#	NONE
ACZ_SDIN[0-2]	INTERNAL 20K PD
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
ACZ_SYNC	INTERNAL 20K PD

**SB: 1 OF 4**

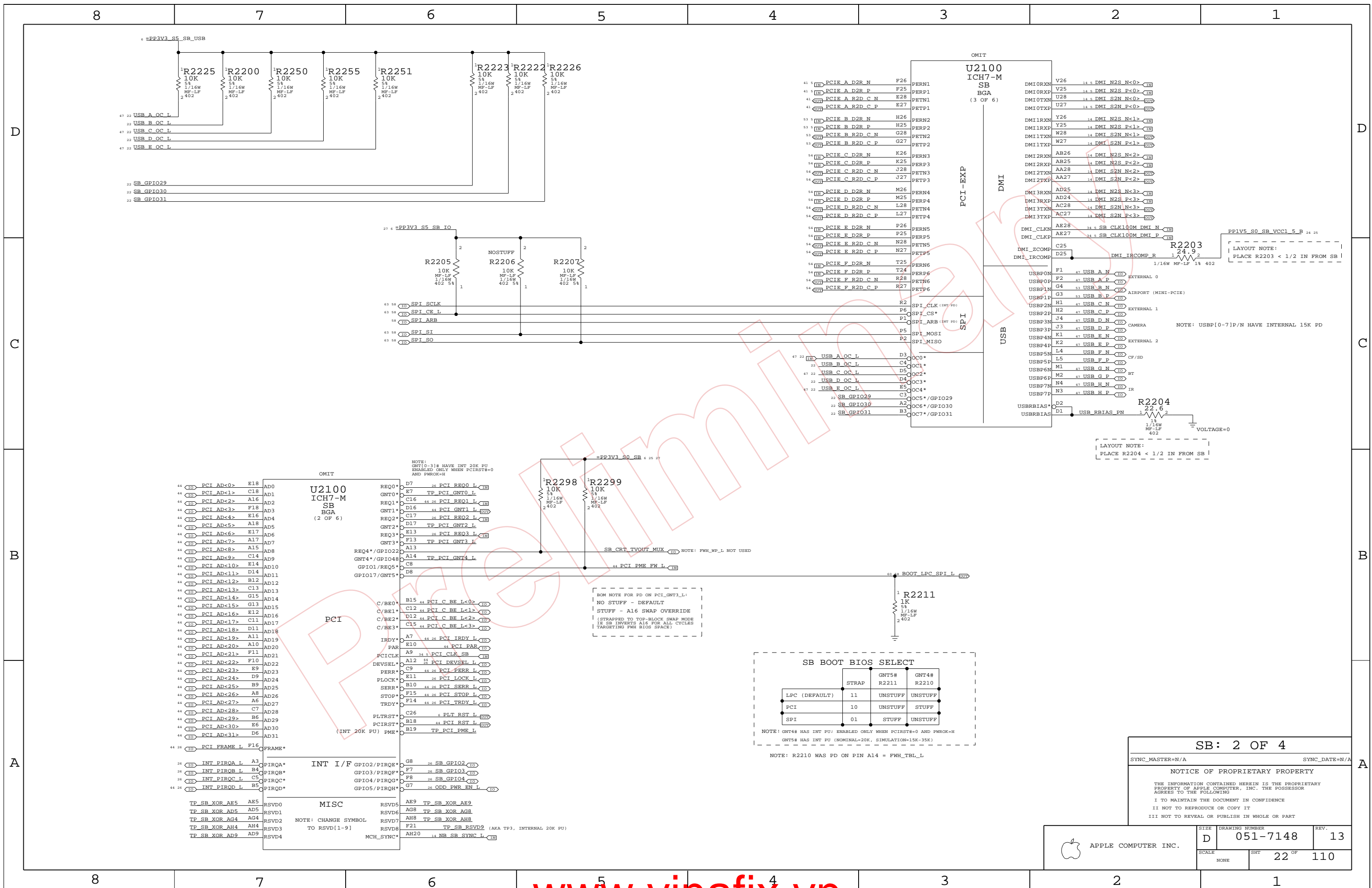
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	D	051-7148	13
SCALE	SHT	21 OF 110	
NONE			



**SB BOOT BIOS SELECT**

	STRAP	GNT5# R2211	GNT4# R2210
LPC (DEFAULT)	11	UNSTUFF	UNSTUFF
PCI	10	UNSTUFF	STUFF
SPI	01	STUFF	UNSTUFF

NOTE: GNT4# HAS INT PU; ENABLED ONLY WHEN PCIRST# = 0 AND FWR0K = H  
GNT5# HAS INT PU (NOMINAL = 20K, SIMULATION = 15K - 35K)  
NOTE: R2210 WAS PD ON PIN A14 = FWH\_TBL\_L

**SB: 2 OF 4**

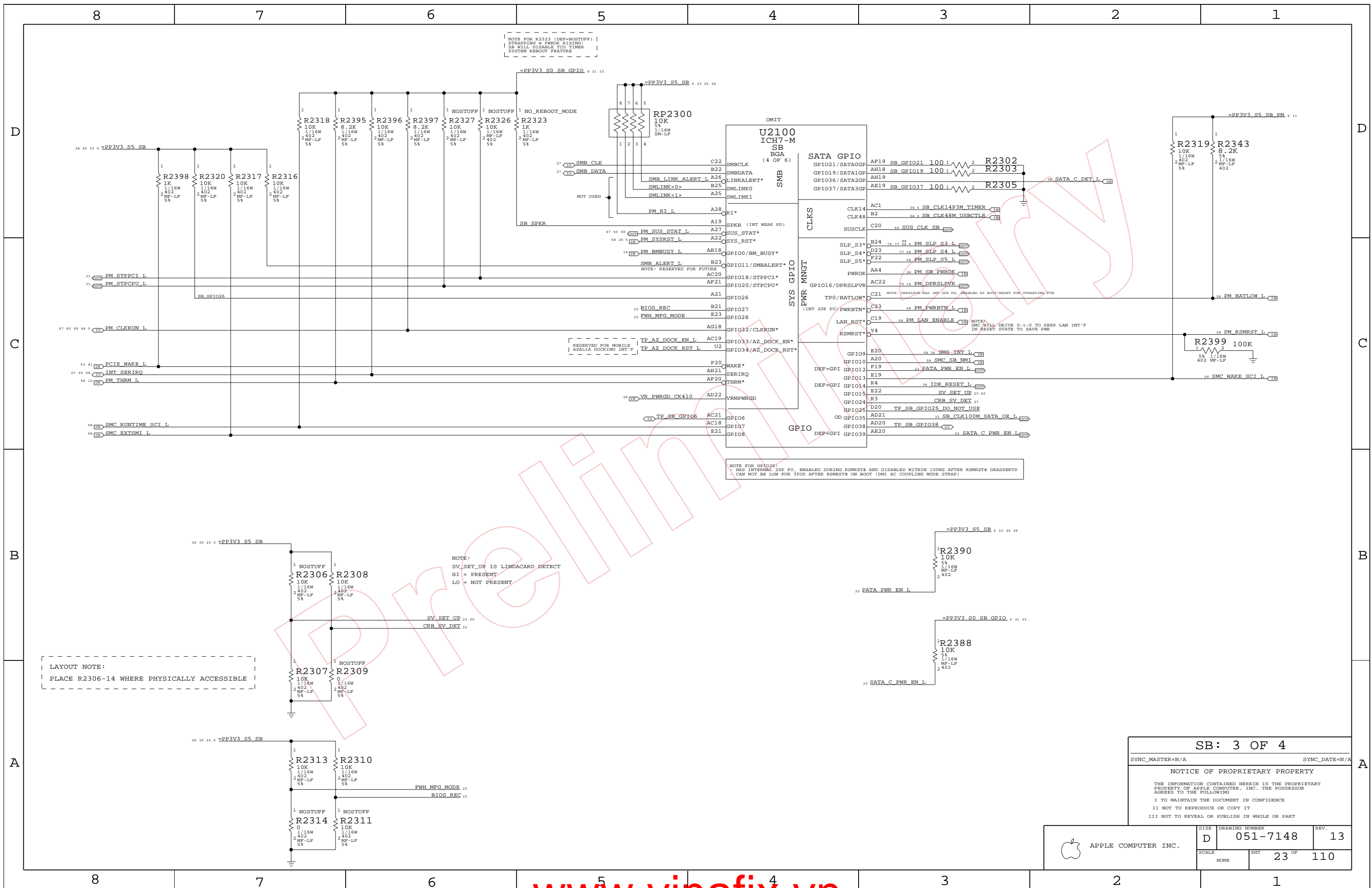
SYNC\_MASTER=N/A SYNC\_DATE=N/A

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	13
SCALE	SHT	22 OF	110
NONE			



NOTE FOR R2323 (DEF-NOSTUFF) | STRAPPING & PWROK RISING: SB WILL DISABLE TOO TIMER SYSTEM REBOOT FEATURE

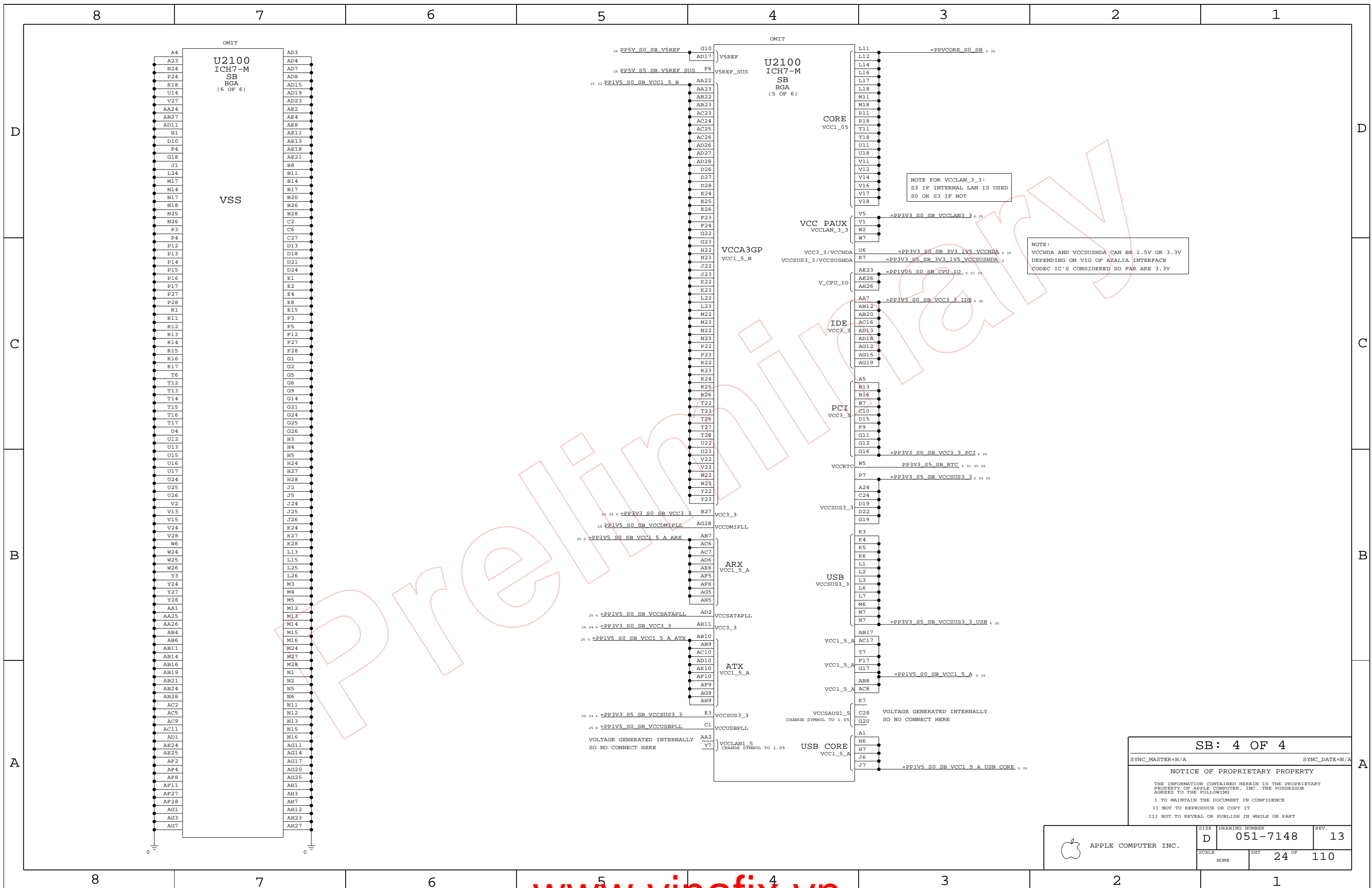
NOTE FOR GPIO25:  
 \* HAS INTERNAL 20K PU, ENABLED DURING RSMRST# AND DISABLED WITHIN 100MS AFTER RSMRST# DEASSERTS  
 \* CAN NOT BE LOW FOR 35US AFTER RSMRST# ON BOOT (DMI AC COUPLING MODE STRAP)

NOTE:  
 SV\_SET\_UP IS LINDACARD DETECT  
 HI = PRESENT  
 LO = NOT PRESENT

LAYOUT NOTE:  
 PLACE R2306-14 WHERE PHYSICALLY ACCESSIBLE

SB: 3 OF 4  
 SYNC\_MASTER=N/A SYNC\_DATE=N/A  
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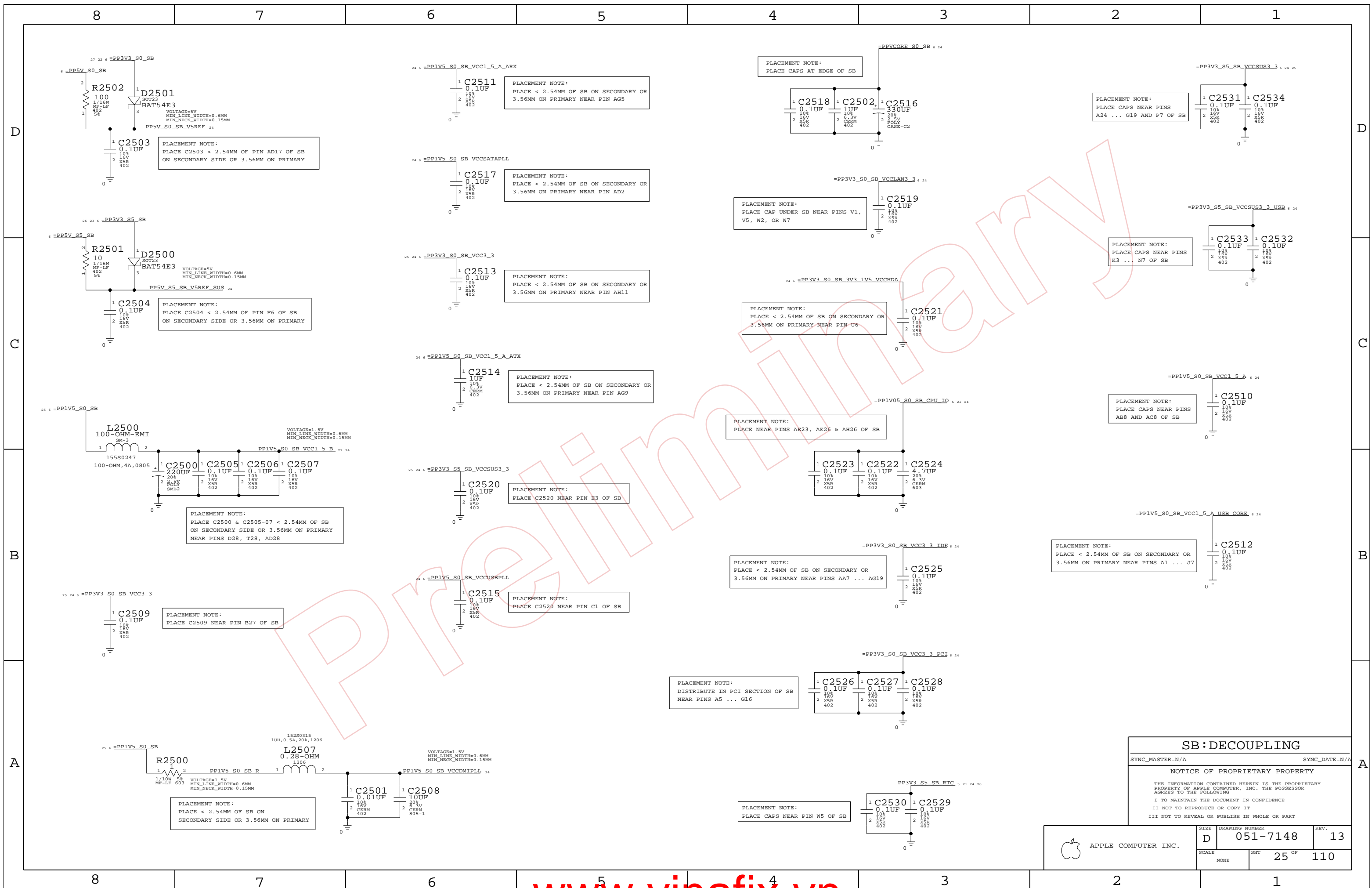
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	13
SCALE	NONE	SHT	23 OF 110



<b>SB: 4 OF 4</b>	
SYNC_MASTER=N/A	SYNC_DATE=N/A
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	13
SCALE	SHT	24 OF 110	
NONE			





**SB : DECOUPLING**

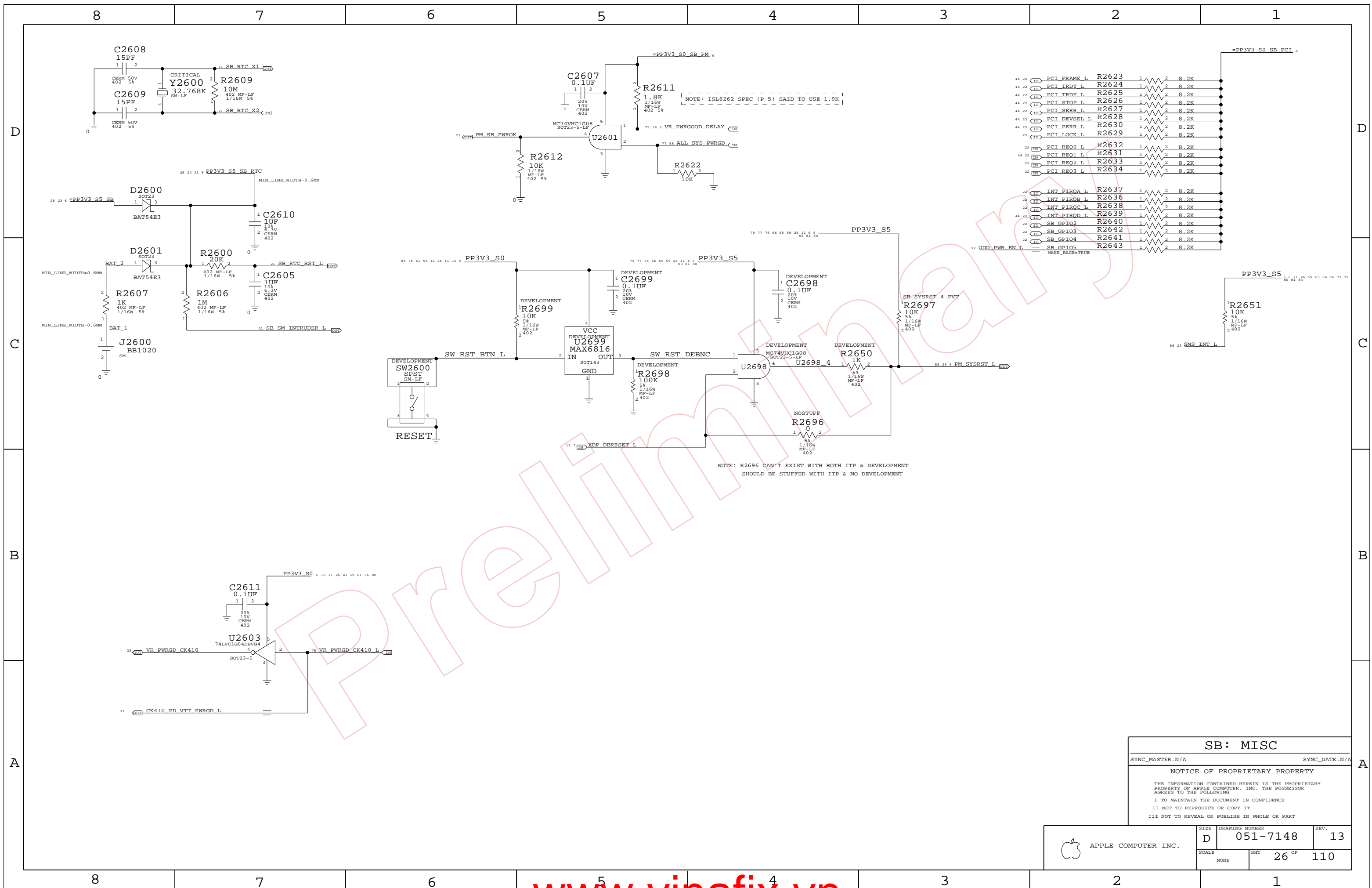
SYNC\_MASTER=N/A SYNC\_DATE=N/A

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	13
SCALE	SHT	25 OF	110
NONE			



**SB: MISC**

SYNC\_MASTER=N/A SYNC\_DATE=N/A

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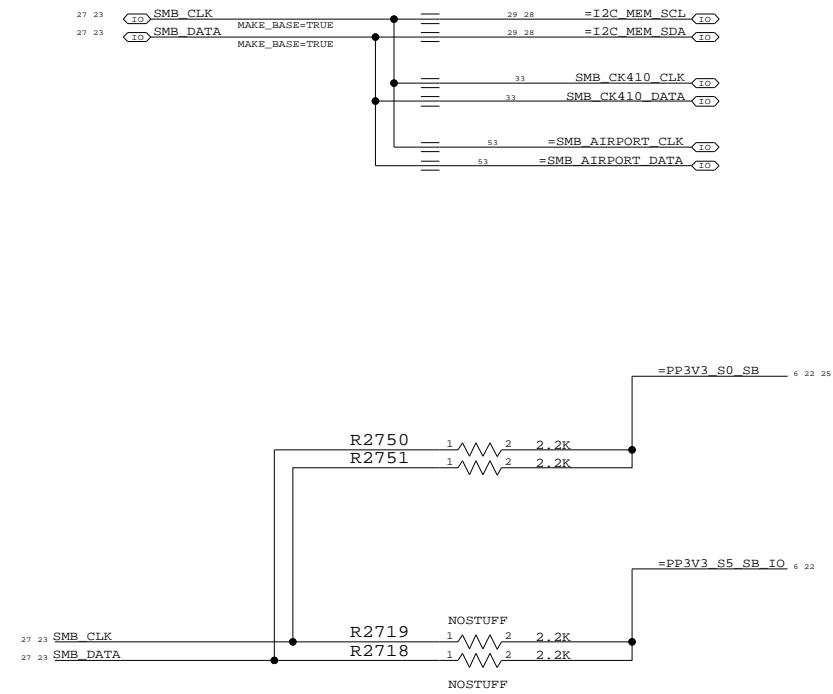
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	13
SCALE	SHT	26 OF	110
NONE			

# SB I2C BUSSES



Preliminary


## SB: SMB HUB

SYNC\_MASTER=N/A SYNC\_DATE=N/A

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 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	13
SCALE	SHT	27 OF 110	
NONE			

# Page Notes

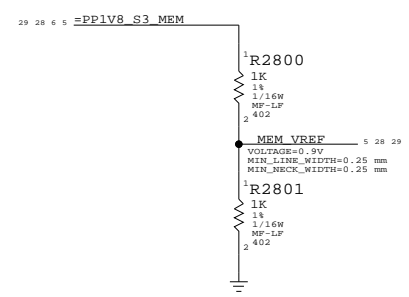
Power aliases required by this page:  
 - =PPIV8\_S3\_MEM  
 - =PPSPD\_S0\_MEM (2.5V - 3.3V)

Signal aliases required by this page:  
 - =I2C\_MEM\_SCL  
 - =I2C\_MEM\_SDA

BOM options provided by this page:  
 (NONE)

## DDR2 VRef

One 0.1uF per connector

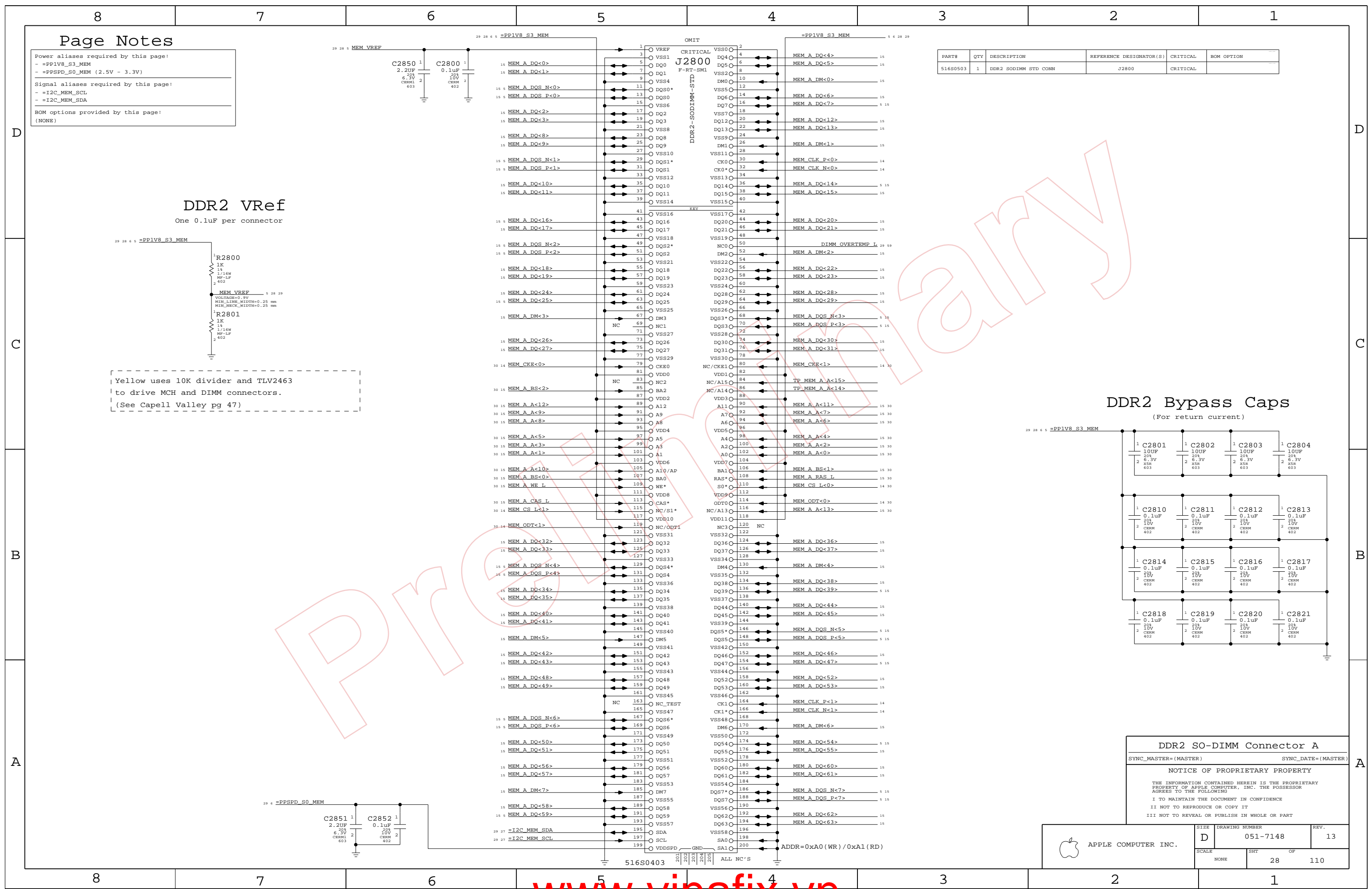


Yellow uses 10K divider and TLV2463 to drive MCH and DIMM connectors. (See Capell Valley pg 47)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
51680503	1	DDR2 SODIMM STD CONN	J2800	CRITICAL	

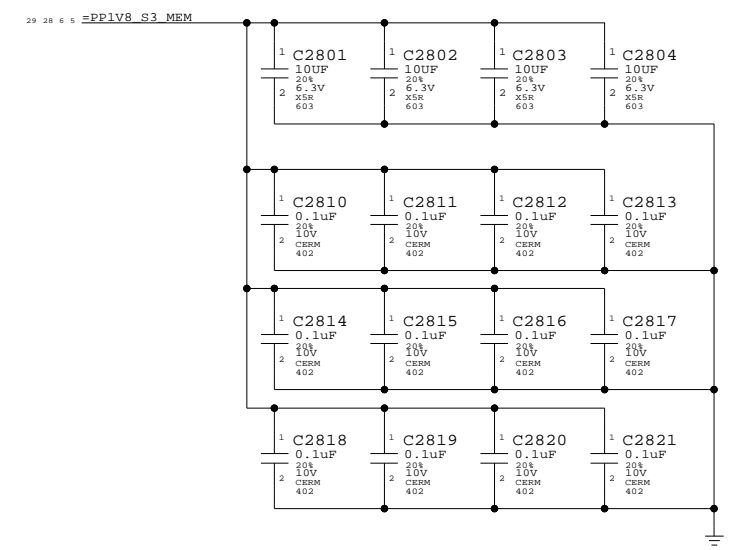
PRINT

www.vinafix.vn



## DDR2 Bypass Caps

(For return current)



DDR2 SO-DIMM Connector A			
SYNC_MASTER=(MASTER)		SYNC_DATE=(MASTER)	
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	DRAWING NUMBER		REV.
	D	051-7148	13
SCALE		SHT	OF
NONE		28	110

# Page Notes

Power aliases required by this page:  
 - =PP1V8\_S3\_MEM  
 - =PPSPD\_S0\_MEM (2.5V - 3.3V)

Signal aliases required by this page:  
 - =I2C\_MEM\_SCL  
 - =I2C\_MEM\_SDA

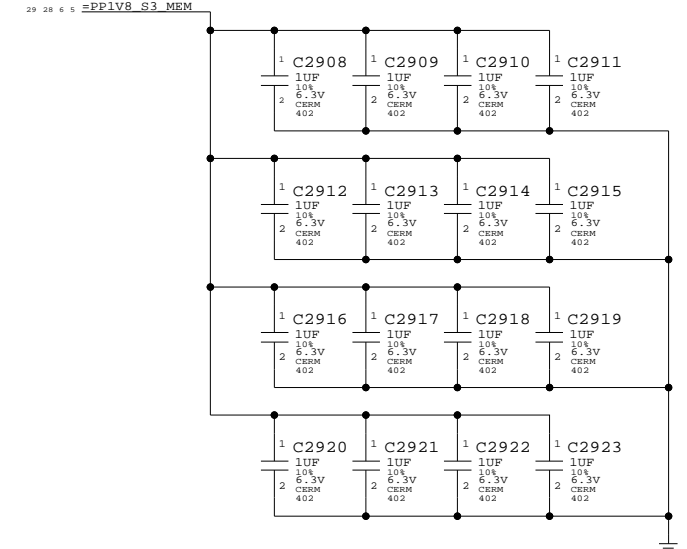
BOM options provided by this page:  
 (NONE)

NOTE: This page does not supply VREF.  
 The reference voltage must be provided by another page.



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
516S0504	1	DDR2 SODIMM REV CONN	J2900	CRITICAL	

## DDR2 Bypass Caps (For return current)



## DDR2 SO-DIMM Connector B

SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)

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APPLE COMPUTER INC.	SIZE <b>D</b>	DRAWING NUMBER 051-7148	REV. 13
	SCALE NONE	SHEET 29	OF 110

8

7

6

5

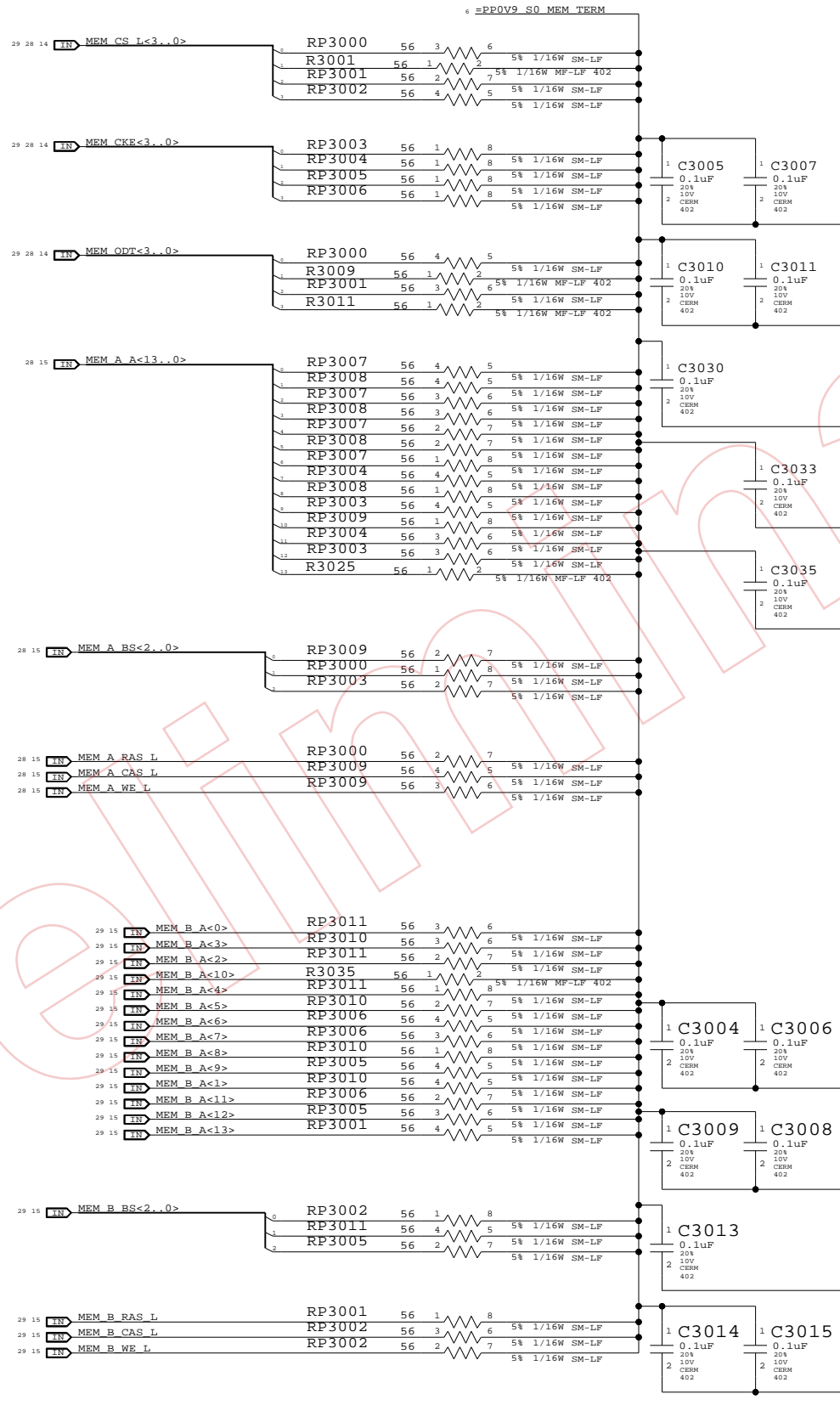
4

3

2

1

One cap for each side of every RPAK, one cap for every two discrete resistors  
BOMOPTION shown at the top of each group applies to every part below it



PRELIMINARY

Memory Active Termination

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	13
SCALE	SHT	OF	
NONE	30	110	

8

7

6

5

4

3

2

1

Page Notes

Power aliases required by this page:  
 - =PP5V\_S0\_MEMVTT  
 - =PP1V8\_S0\_MEMVTT  
 - =PP0V9\_S0\_MEMVTT\_LDO

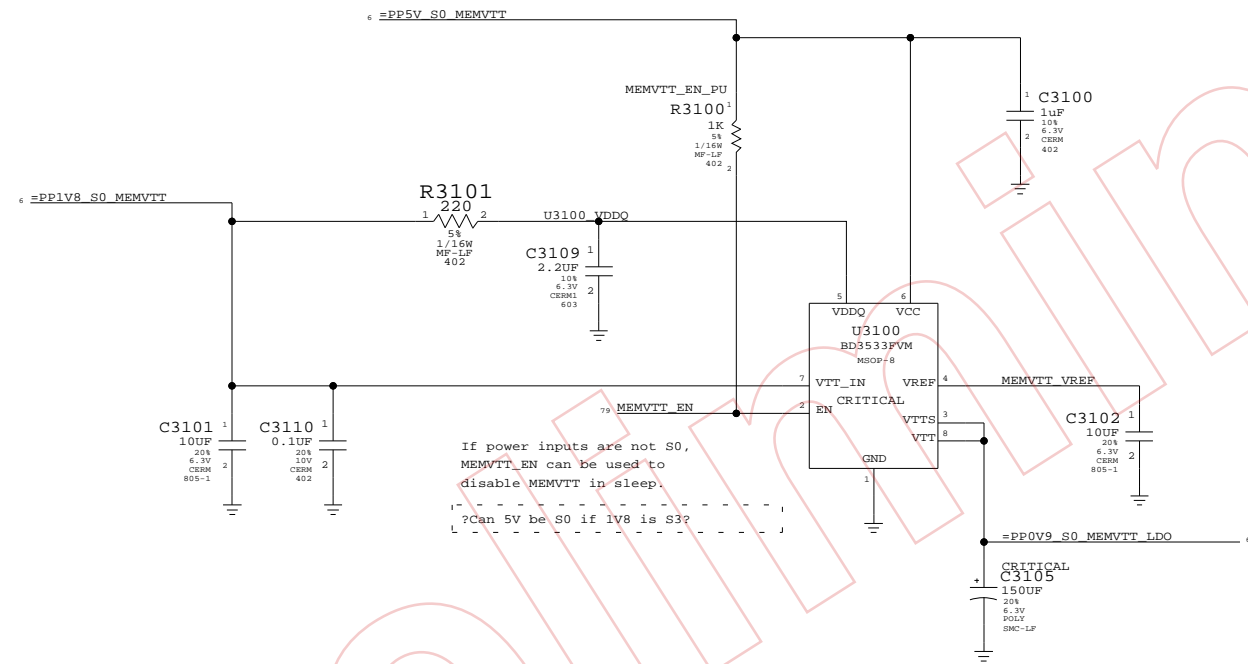
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Signal aliases required by this page:  
 (NONE)

---

BOM options provided by this page:  
 (NONE)

DDR2 Vtt Regulator



Pre-Announcement

**Memory Vtt Supply**

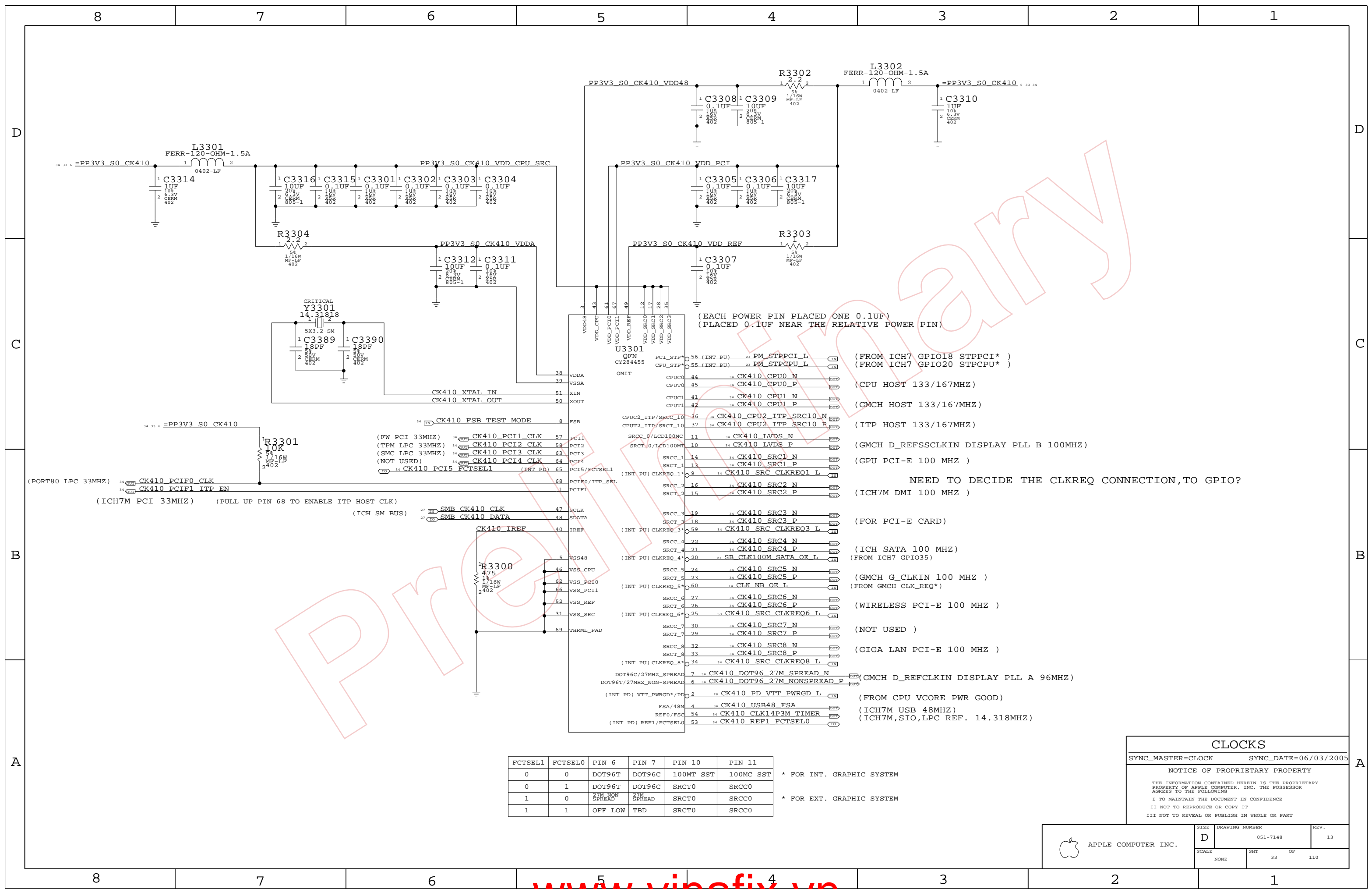
SYNC\_MASTER=(MASTER)      SYNC\_DATE=(MASTER)

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	SCALE NONE	SHT 31	OF 110



(EACH POWER PIN PLACED ONE 0.1UF)  
(PLACED 0.1UF NEAR THE RELATIVE POWER PIN)

- 56 (INT PU) 23 PM\_STPPCI L (FROM ICH7 GPIO18 STPPCI\*)
- 55 (INT PU) 23 PM\_STPCPU L (FROM ICH7 GPIO20 STPCPU\*)
- 44 34 CK410 CPU0 N (CPU HOST 133/167MHZ)
- 45 34 CK410 CPU0 P
- 41 34 CK410 CPU1 N (GMCH HOST 133/167MHZ)
- 42 34 CK410 CPU1 P
- 36 34 CK410 CPU2 ITP\_SRC10\_N (ITP HOST 133/167MHZ)
- 37 34 CK410 CPU2 ITP\_SRC10\_P
- 11 34 CK410 LVDS N (GMCH D\_REFSSCLKIN DISPLAY PLL B 100MHZ)
- 10 34 CK410 LVDS P
- 14 34 CK410 SRC1 N (GPU PCI-E 100 MHZ)
- 13 34 CK410 SRC1 P
- 9 34 CK410 SRC CLKREQ1 L (NEED TO DECIDE THE CLKREQ CONNECTION, TO GPIO?)
- 16 34 CK410 SRC2 N (ICH7M DMI 100 MHZ)
- 15 34 CK410 SRC2 P
- 19 34 CK410 SRC3 N (FOR PCI-E CARD)
- 18 34 CK410 SRC3 P
- 59 34 CK410 SRC CLKREQ3 L (ICH SATA 100 MHZ)
- 22 34 CK410 SRC4 N (FROM ICH7 GPIO35)
- 21 34 CK410 SRC4 P
- 20 34 SB\_CLK100M\_SATA\_OE L
- 24 34 CK410 SRC5 N (GMCH G\_CLKIN 100 MHZ)
- 23 34 CK410 SRC5 P (FROM GMCH CLK\_REQ\*)
- 60 34 CLK\_NB\_OE L
- 27 34 CK410 SRC6 N (WIRELESS PCI-E 100 MHZ)
- 26 34 CK410 SRC6 P
- 25 34 CK410 SRC CLKREQ6 L (NOT USED)
- 30 34 CK410 SRC7 N (GIGA LAN PCI-E 100 MHZ)
- 29 34 CK410 SRC7 P
- 32 34 CK410 SRC8 N
- 33 34 CK410 SRC8 P
- 34 34 CK410 SRC CLKREQ8 L
- 7 34 CK410 DOT96 27M SPREAD N (GMCH D\_REFCLKIN DISPLAY PLL A 96MHZ)
- 6 34 CK410 DOT96 27M NONSPREAD P
- 2 34 CK410 PD VTT\_PWRGD L (FROM CPU VCORE PWR GOOD)
- 4 34 CK410 USB48\_FSA (ICH7M USB 48MHZ)
- 54 34 CK410 CLK14P3M\_TIMER (ICH7M, SIO, LPC REF. 14.318MHZ)
- 53 34 CK410 REF1\_FCTSEL0

FCTSEL1	FCTSEL0	PIN 6	PIN 7	PIN 10	PIN 11
0	0	DOT96T	DOT96C	100MT_SST	100MC_SST
0	1	DOT96T	DOT96C	SRCT0	SRCC0
1	0	27M NON SPREAD	27M SPREAD	SRCT0	SRCC0
1	1	OFF LOW	TBD	SRCT0	SRCC0

\* FOR INT. GRAPHIC SYSTEM  
\* FOR EXT. GRAPHIC SYSTEM

**CLOCKS**

SYNC\_MASTER=CLOCK      SYNC\_DATE=06/03/2005

**NOTICE OF PROPRIETARY PROPERTY**

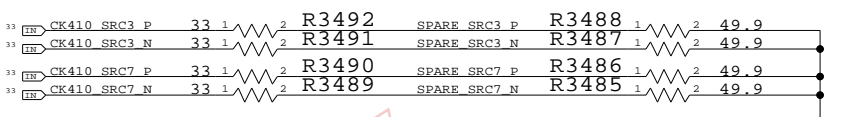
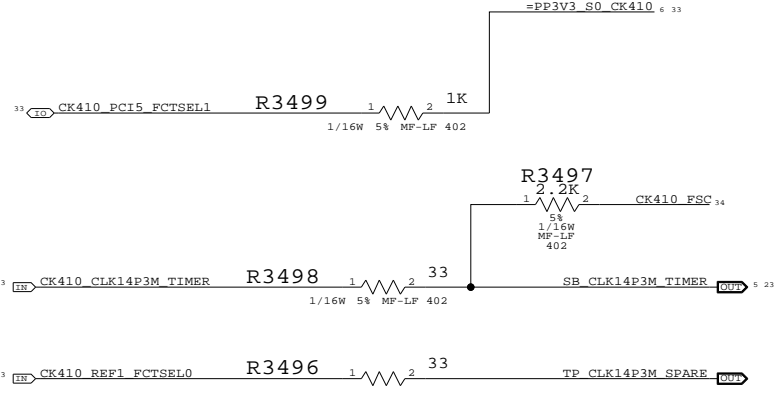
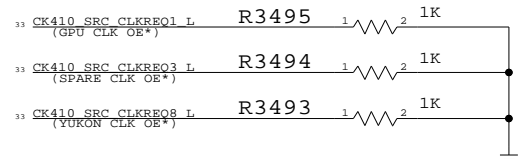
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	D	051-7148	13
SCALE	SHT	OF	110
NONE	33		

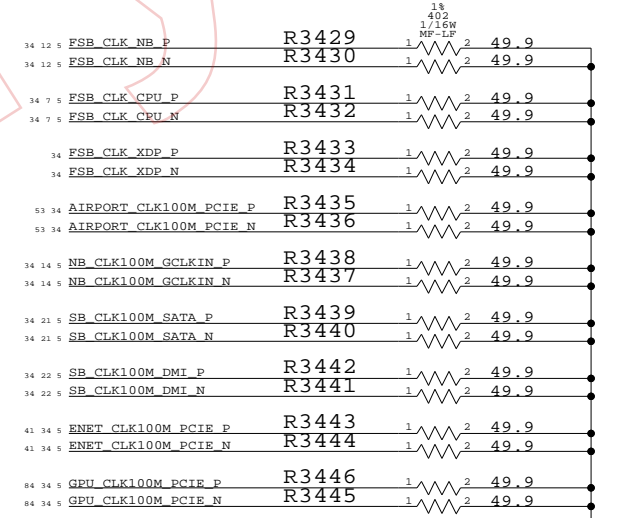
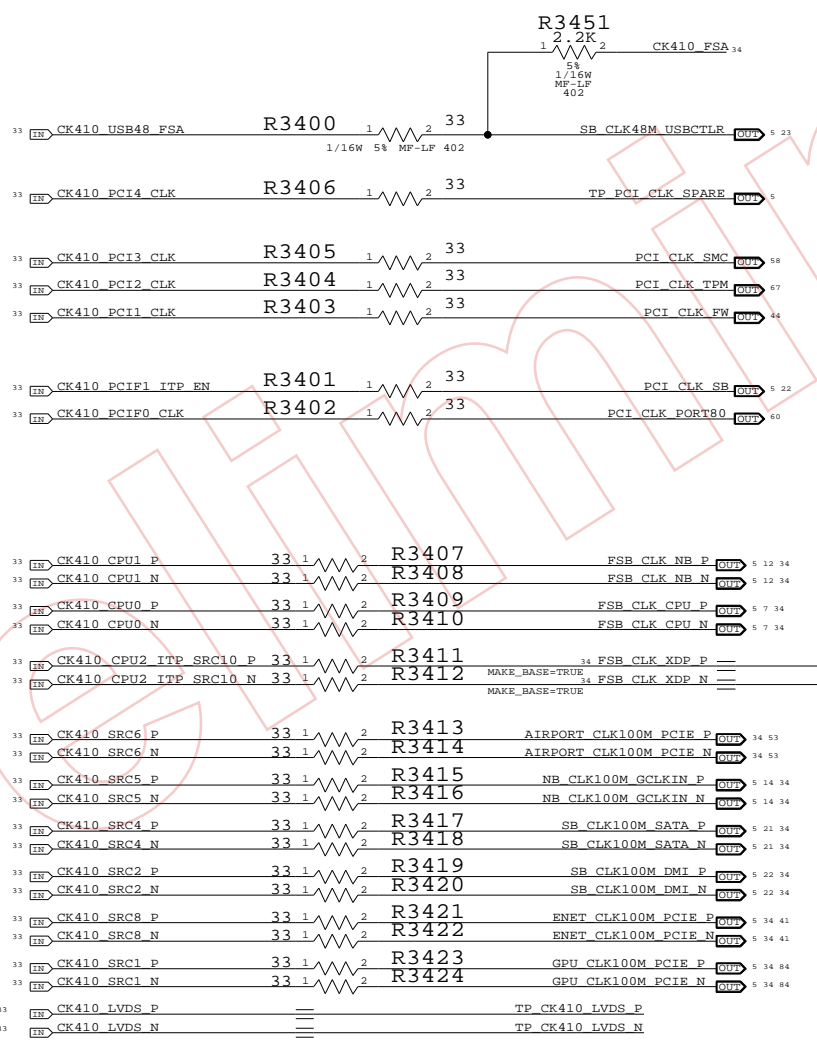
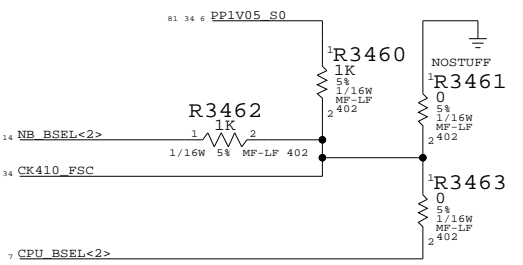
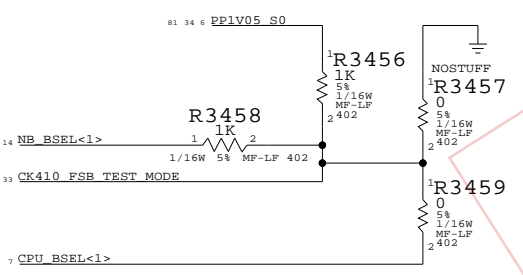
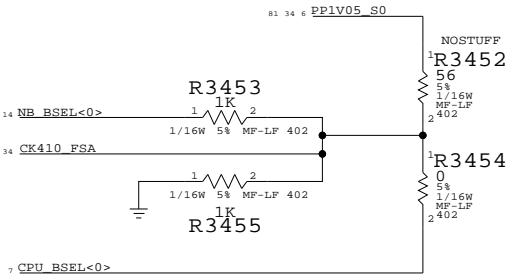


NOTE: USE THESE PULL-DOWNS IF NOT CONNECTED TO GPIO'S



FSB FREQUENCY SELECT:

	STUFF	NO STUFF
CPU DRIVEN	R3453 R3454 R3455	R3456 R3457
533MHZ (133MHZ CPU CLK)	R3452 R3454 R3455	R3456 R3457
667MHZ (166MHZ CPU CLK)	R3452 R3454 R3455	R3456 R3457



**CLOCKS: TERMINATIONS**

SYNC\_MASTER=N/A SYNC\_DATE=N/A

NOTICE OF PROPRIETARY PROPERTY

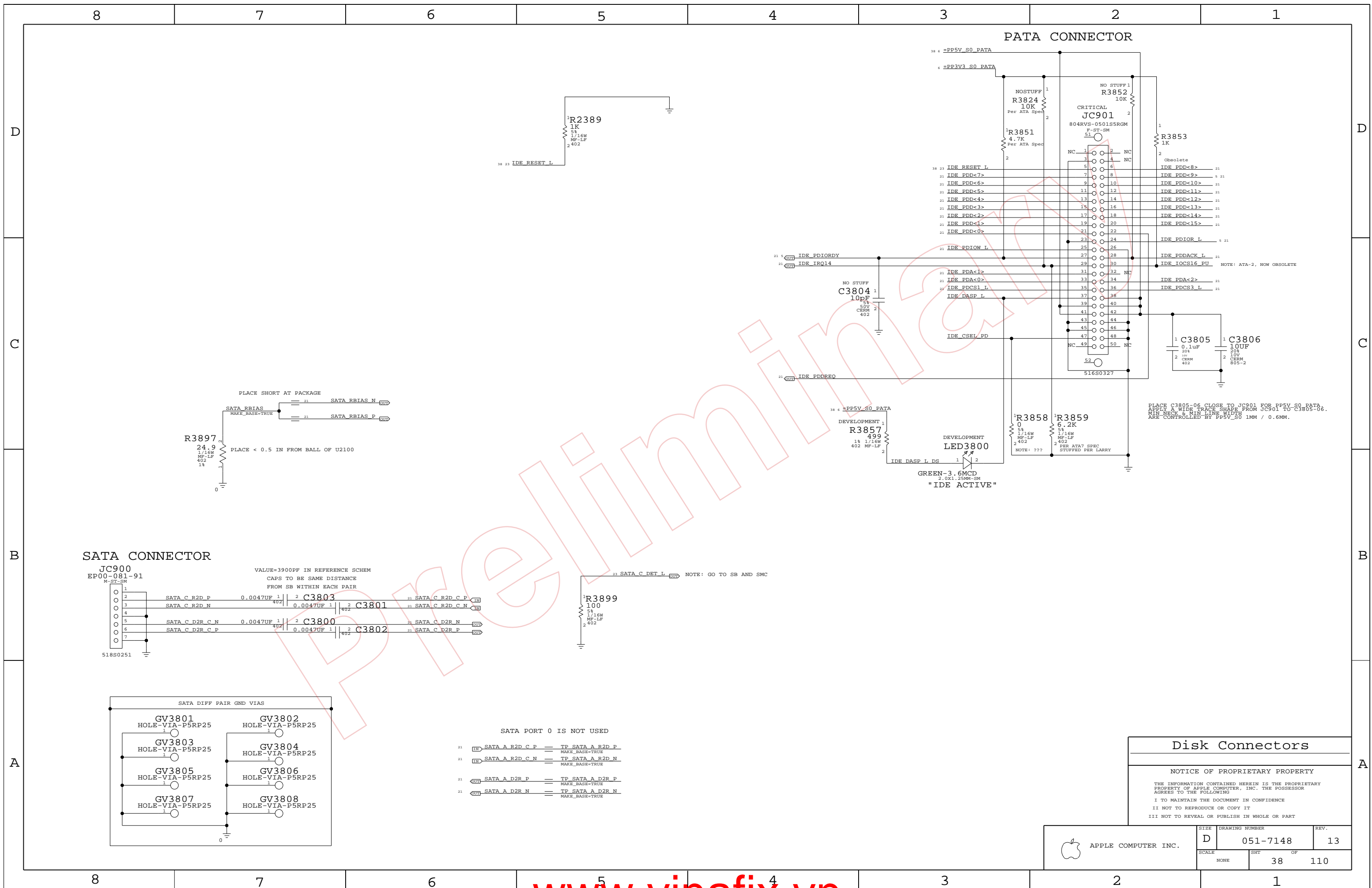
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	D	051-7148	13
SCALE	SHT	OF	110
NONE	34		



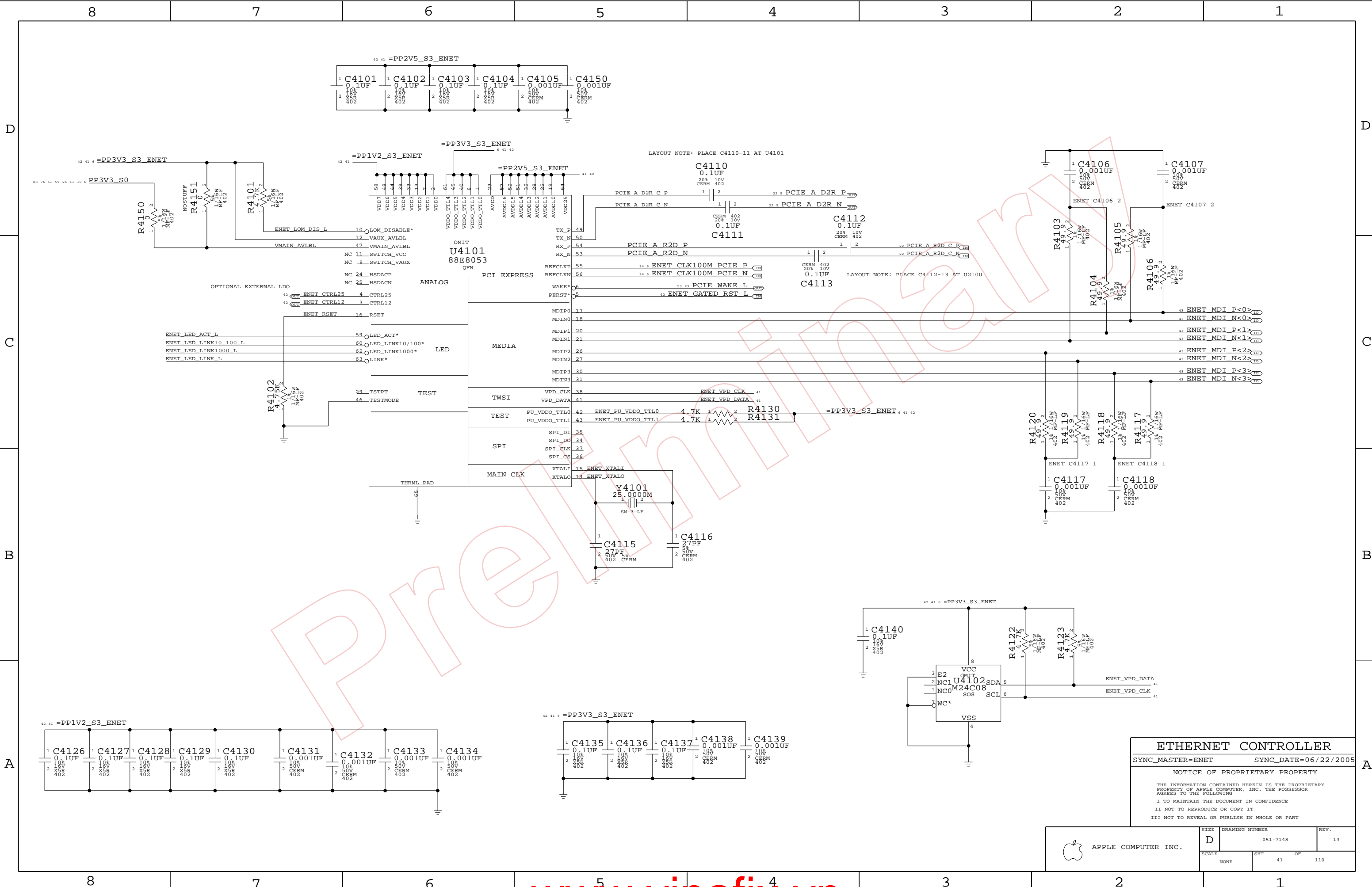
**Disk Connectors**

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	SCALE NONE	SHT <b>38</b>	OF <b>110</b>



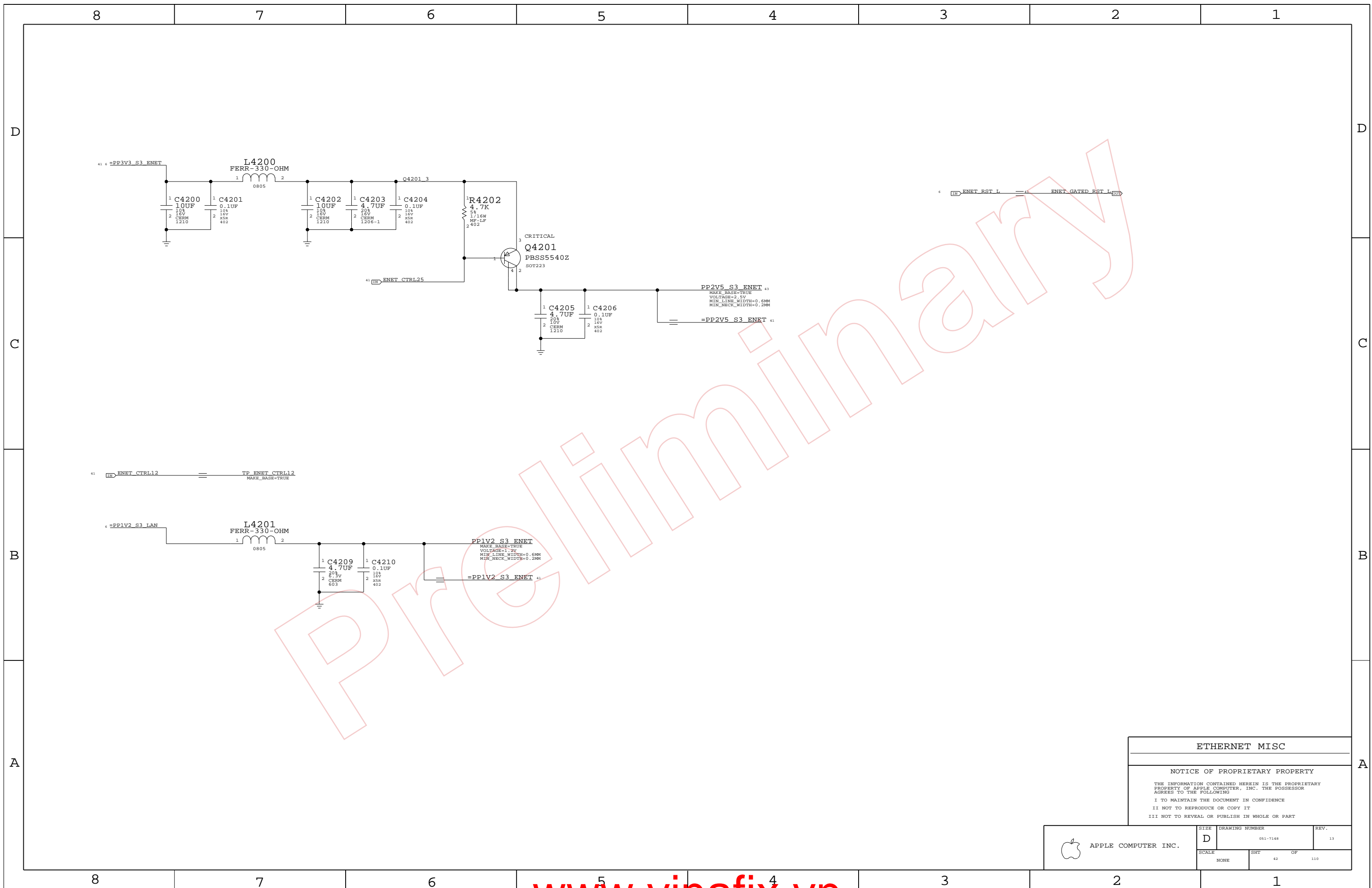
**ETHERNET CONTROLLER**

SYNC\_MASTER=ENET SYNC\_DATE=06/22/2005

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	SCALE NONE	SHEET 41	OF 110



**ETHERNET MISC**

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APPLE COMPUTER INC.	SIZE <b>D</b>	DRAWING NUMBER 051-7148	REV. 13
	SCALE NONE	SHEET 42	OF 110

8 7 6 5 4 3 2 1

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D

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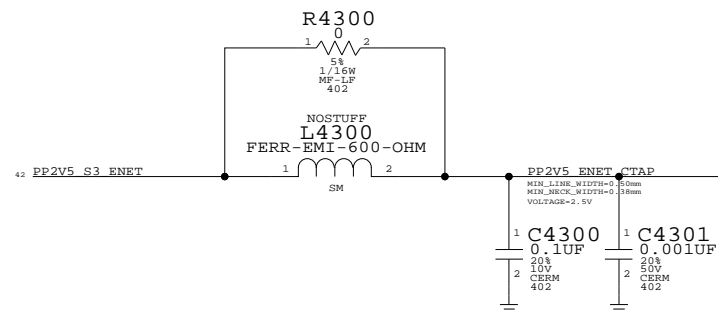
C

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B

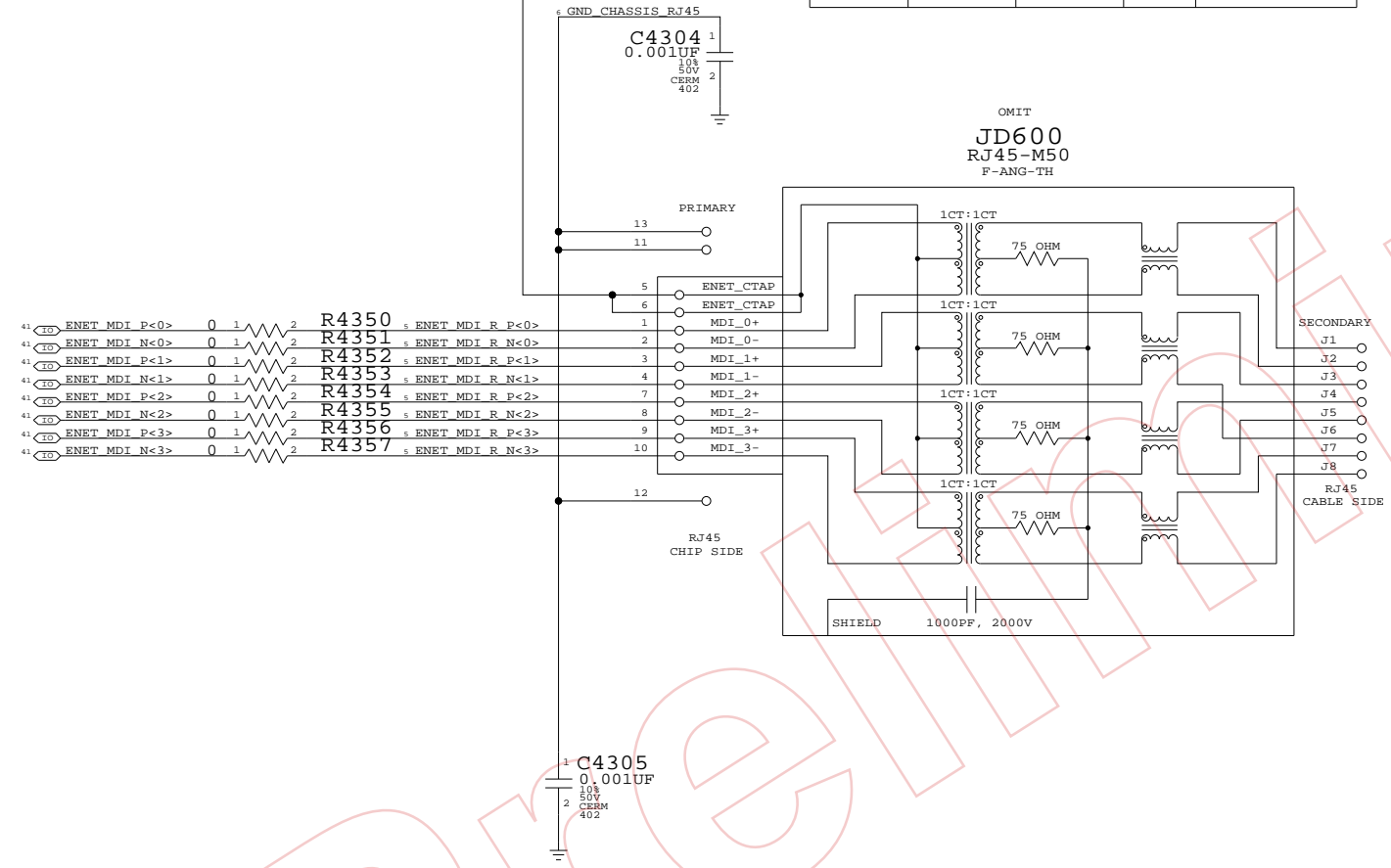
A

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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0366	1	FOXCONN AND DELTA RJ45	JD600	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
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**ETHERNET CONNECTOR**

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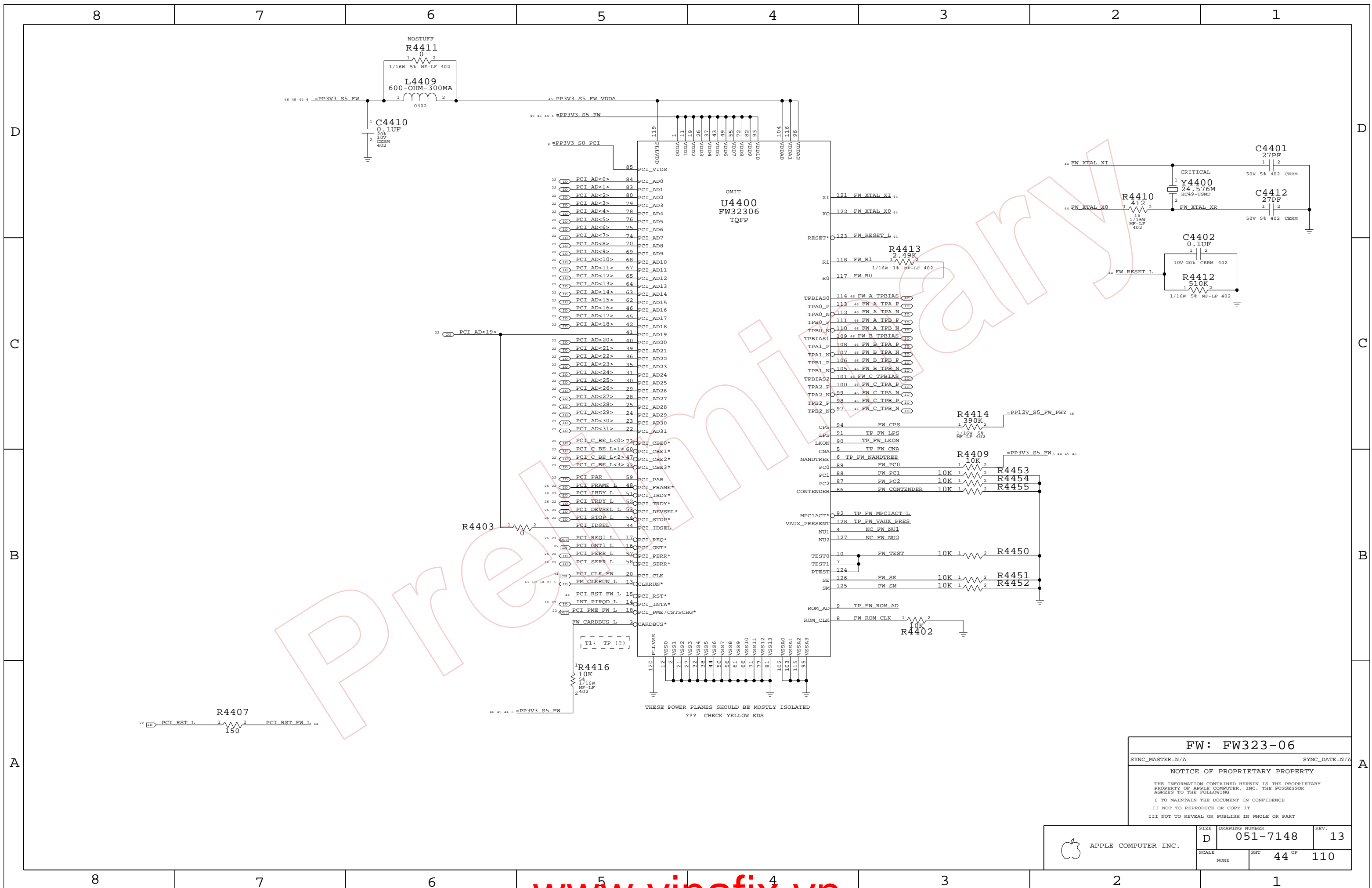
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	13
SCALE		SHT OF	
NONE		43 OF 110	

8 7 6 5 4 3 2 1



**FW: FW323-06**

SYNC\_MASTER=N/A SYNC\_DATE=N/A

**NOTICE OF PROPRIETARY PROPERTY**

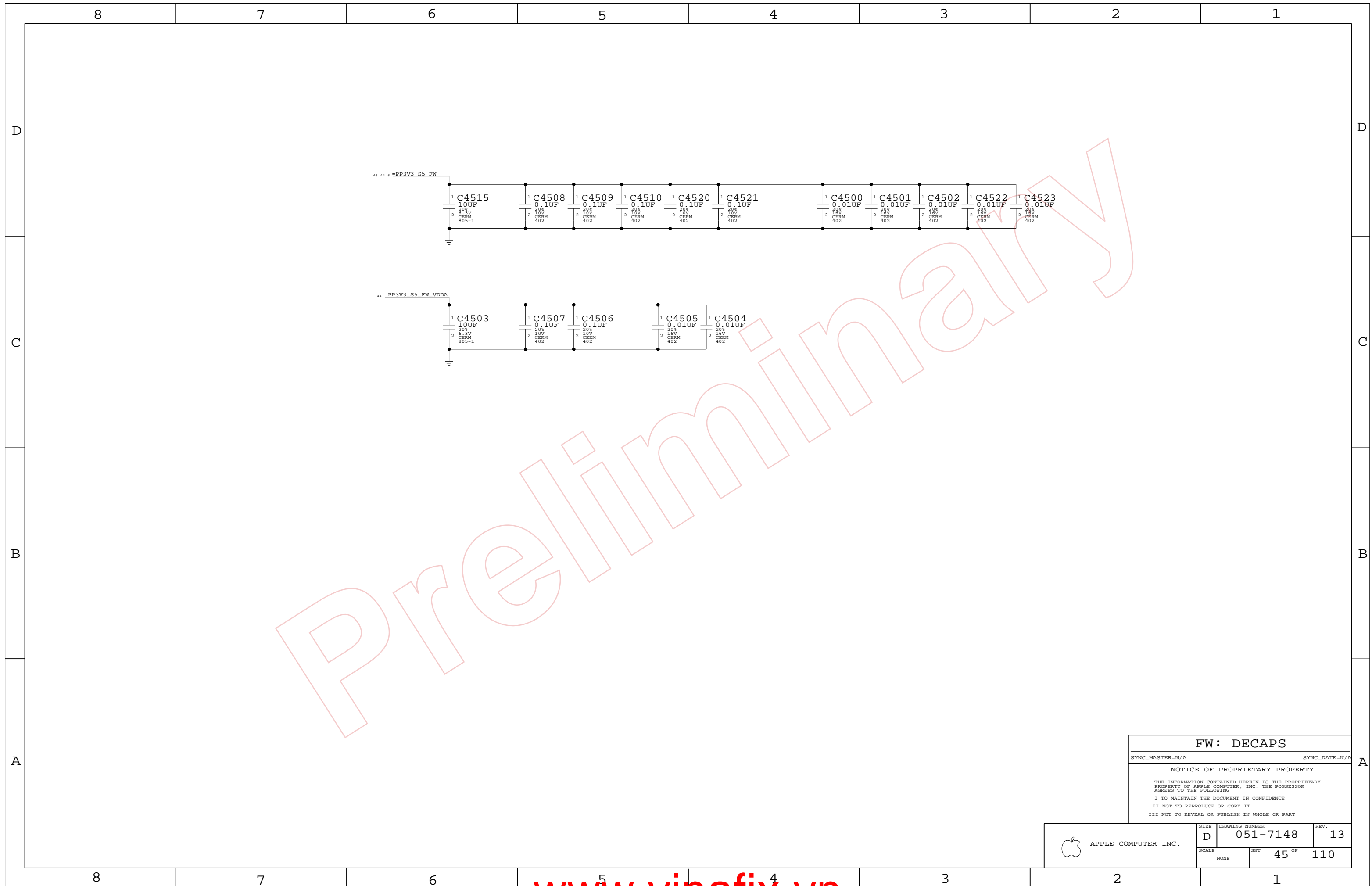
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7148	REV. 13
	SCALE NONE	SHEETS 44 OF 110	



Preliminary

**FW: DECAPS**

SYNC\_MASTER=N/A SYNC\_DATE=N/A

**NOTICE OF PROPRIETARY PROPERTY**

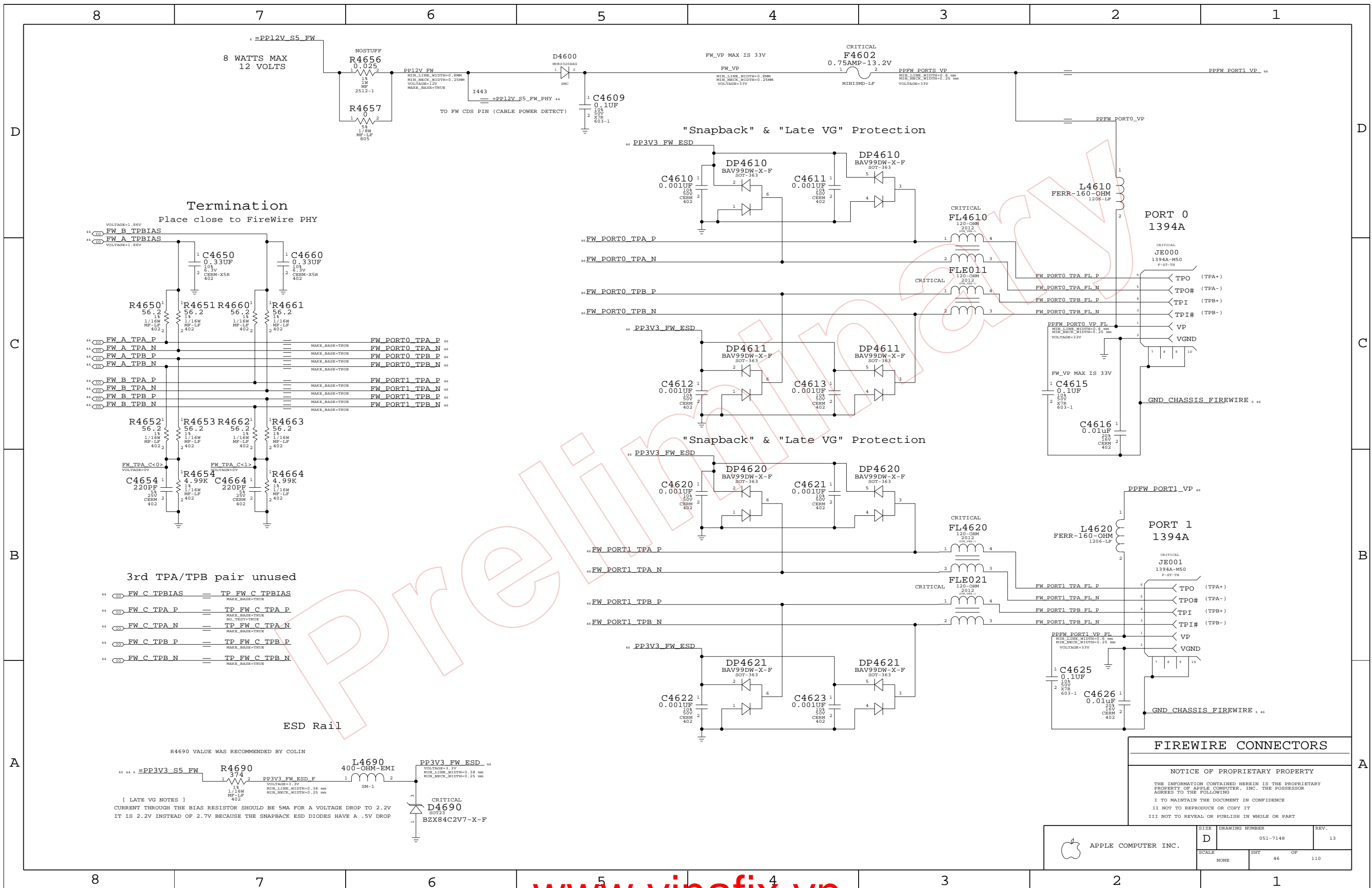
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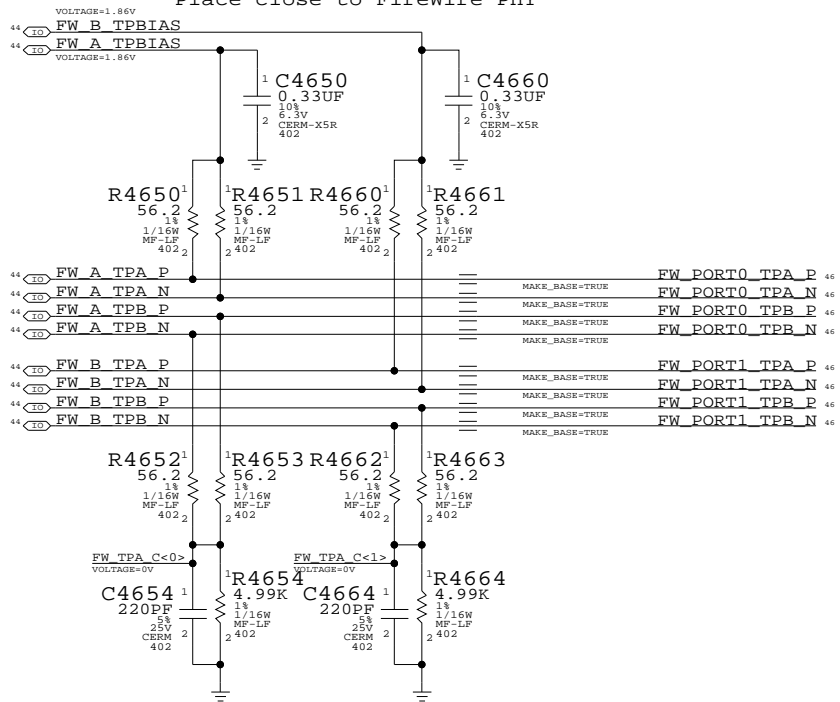
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III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

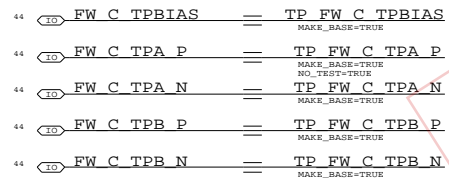
APPLE COMPUTER INC.	SIZE	D	DRAWING NUMBER	051-7148	REV.	13
	SCALE	NONE	SHT	45 OF	110	



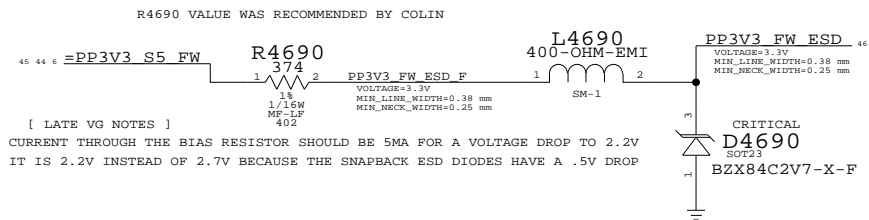
**Termination**  
Place close to FireWire PHY



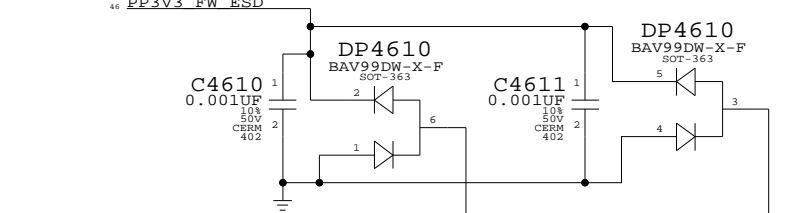
3rd TPA/TPB pair unused



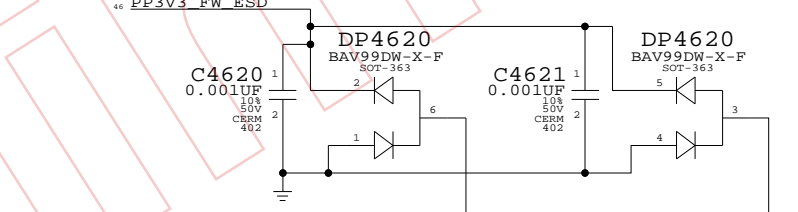
ESD Rail



"Snapback" & "Late VG" Protection



"Snapback" & "Late VG" Protection



FIREWIRE CONNECTORS

NOTICE OF PROPRIETARY PROPERTY

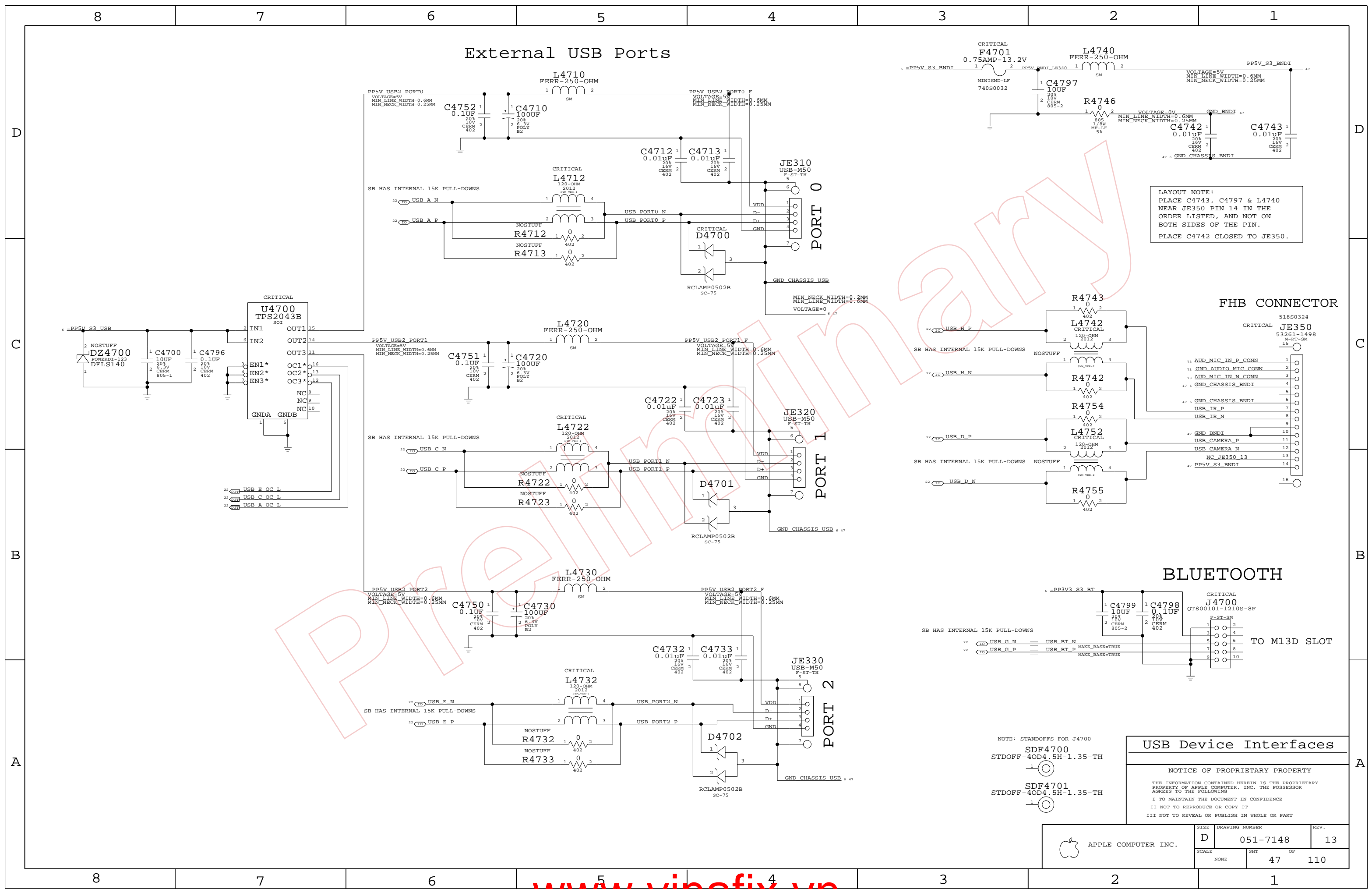
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	D	051-7148	13
SCALE	SHT	OF	110
NONE	46		

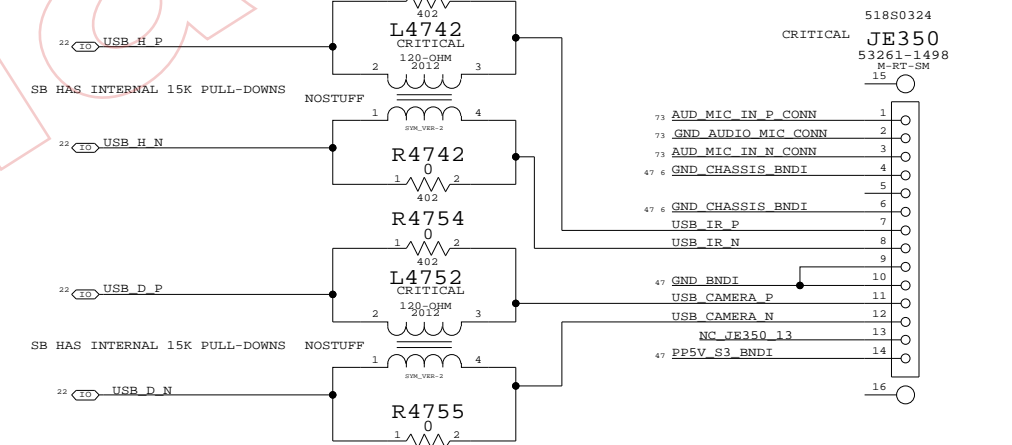


# External USB Ports

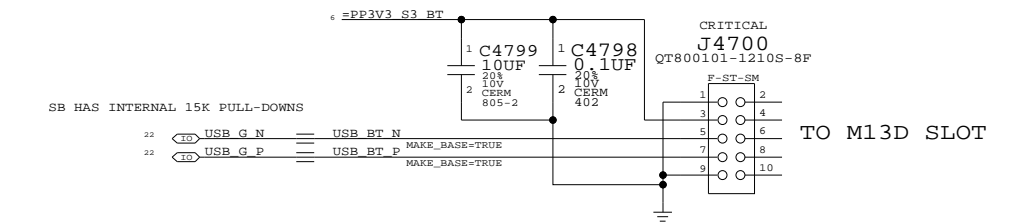


LAYOUT NOTE:  
 PLACE C4743, C4797 & L4740  
 NEAR JE350 PIN 14 IN THE  
 ORDER LISTED, AND NOT ON  
 BOTH SIDES OF THE PIN.  
 PLACE C4742 CLOSED TO JE350.

## FHB CONNECTOR



## BLUETOOTH

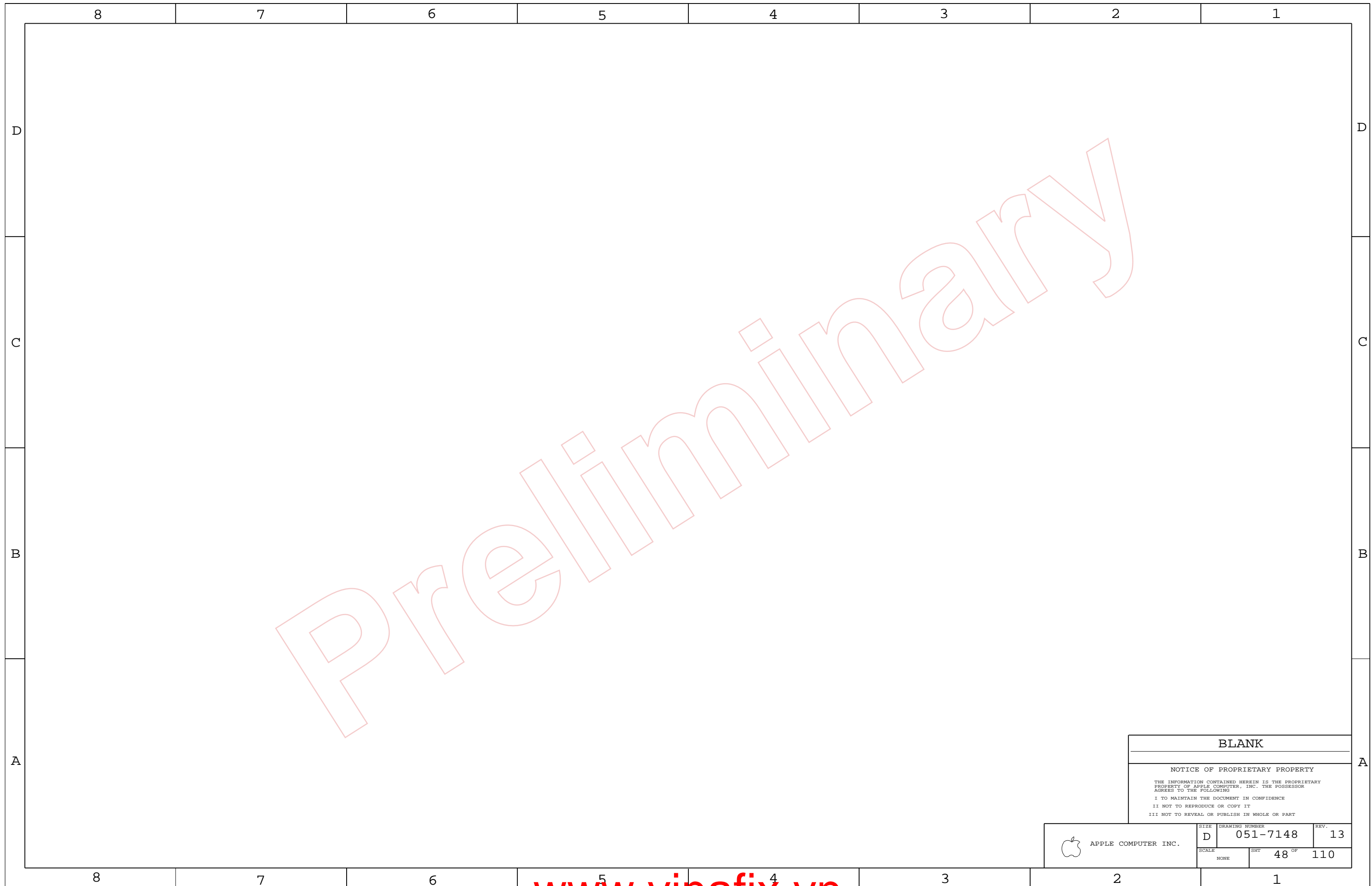


NOTE: STANDOFFS FOR J4700  
 SDF4700  
 STDOFF-40D4.5H-1.35-TH  
 SDF4701  
 STDOFF-40D4.5H-1.35-TH

## USB Device Interfaces

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	13
SCALE	NONE	SHT	OF
		47	110



Preliminary

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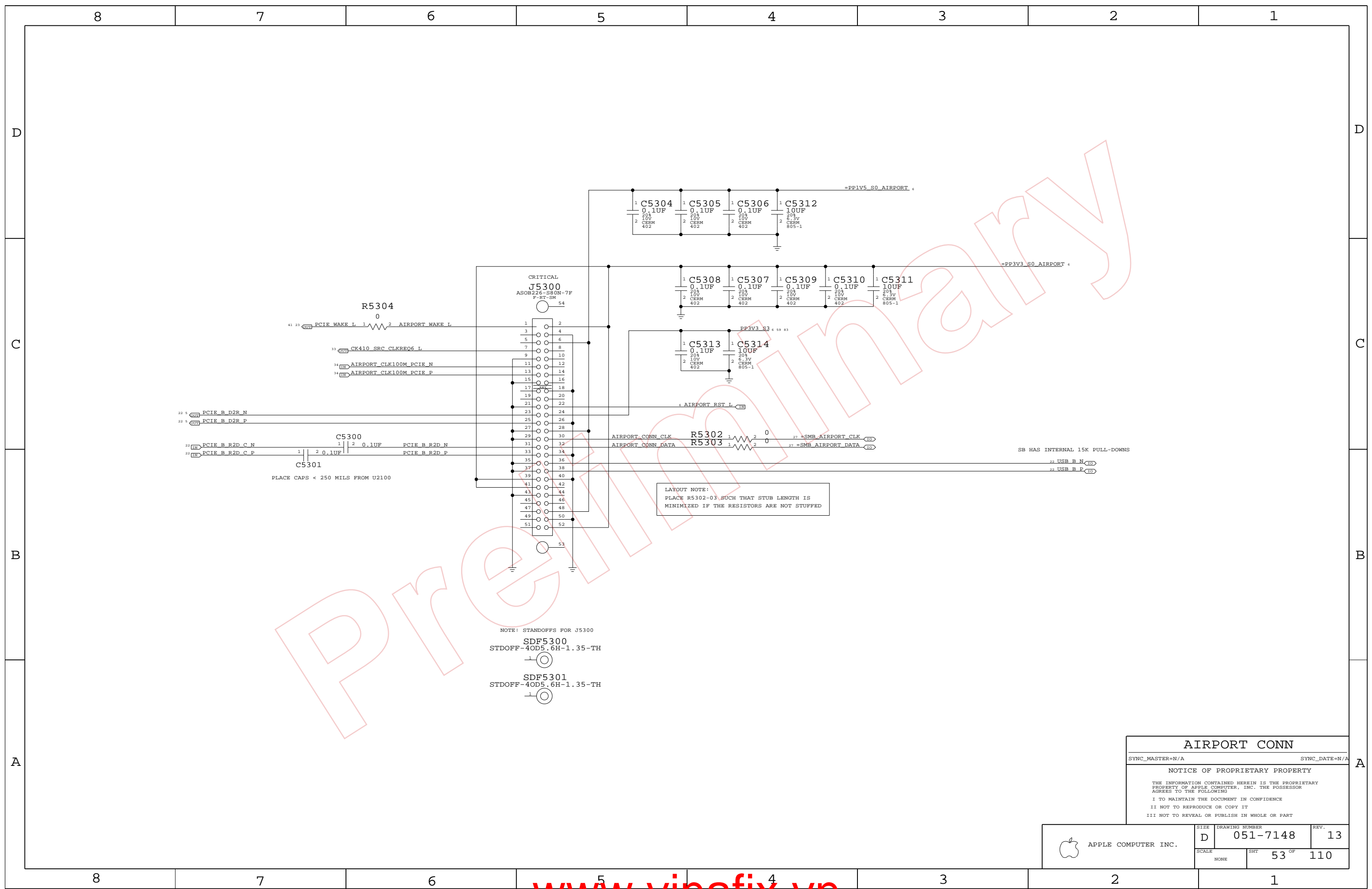
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

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III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

 APPLE COMPUTER INC.	<small>SIZE</small> D	<small>DRAWING NUMBER</small> 051-7148	<small>REV.</small> 13
	<small>SCALE</small> NONE	<small>SHT</small> 48 OF	<small>110</small>



PROTECTED

NOTE: STANDOFFS FOR J5300  
 SDF5300  
 STDOFF-40D5.6H-1.35-TH  
  
 SDF5301  
 STDOFF-40D5.6H-1.35-TH  


LAYOUT NOTE:  
 PLACE R5302-03 SUCH THAT STUB LENGTH IS  
 MINIMIZED IF THE RESISTORS ARE NOT STUFFED

SB HAS INTERNAL 15K PULL-DOWNS

**AIRPORT CONN**

SYNC\_MASTER=N/A SYNC\_DATE=N/A


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 APPLE COMPUTER INC.	SIZE <b>D</b>	DRAWING NUMBER <b>051-7148</b>	REV. <b>13</b>
	SCALE NONE	SHEET <b>53</b> OF	TOTAL SHEETS <b>110</b>

8

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22	IN	PCIE C R2D C N	==	TP PCIE C R2D C N	MAKE_BASE=TRUE
22	IN	PCIE C R2D C P	==	TP PCIE C R2D C P	MAKE_BASE=TRUE
22	OUT	PCIE C D2R N	==	TP PCIE C D2R N	MAKE_BASE=TRUE
22	OUT	PCIE C D2R P	==	TP PCIE C D2R P	MAKE_BASE=TRUE
22	IN	PCIE D R2D C N	==	TP PCIE D R2D C N	MAKE_BASE=TRUE
22	IN	PCIE D R2D C P	==	TP PCIE D R2D C P	MAKE_BASE=TRUE
22	OUT	PCIE D D2R N	==	TP PCIE D D2R N	MAKE_BASE=TRUE
22	OUT	PCIE D D2R P	==	TP PCIE D D2R P	MAKE_BASE=TRUE
22	IN	PCIE E R2D C N	==	TP PCIE E R2D C N	MAKE_BASE=TRUE
22	IN	PCIE E R2D C P	==	TP PCIE E R2D C P	MAKE_BASE=TRUE
22	OUT	PCIE E D2R N	==	TP PCIE E D2R N	MAKE_BASE=TRUE
22	OUT	PCIE E D2R P	==	TP PCIE E D2R P	MAKE_BASE=TRUE
22	IN	PCIE F R2D C N	==	TP PCIE F R2D C N	MAKE_BASE=TRUE
22	IN	PCIE F R2D C P	==	TP PCIE F R2D C P	MAKE_BASE=TRUE
22	OUT	PCIE F D2R N	==	TP PCIE F D2R N	MAKE_BASE=TRUE
22	OUT	PCIE F D2R P	==	TP PCIE F D2R P	MAKE_BASE=TRUE

Preliminary

**PCIE UNUSED PORTS**  
 SYNC\_MASTER=N/A SYNC\_DATE=N/A

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	D	051-7148	13
SCALE	SHT	OF	
NONE	54	110	

8

7

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5

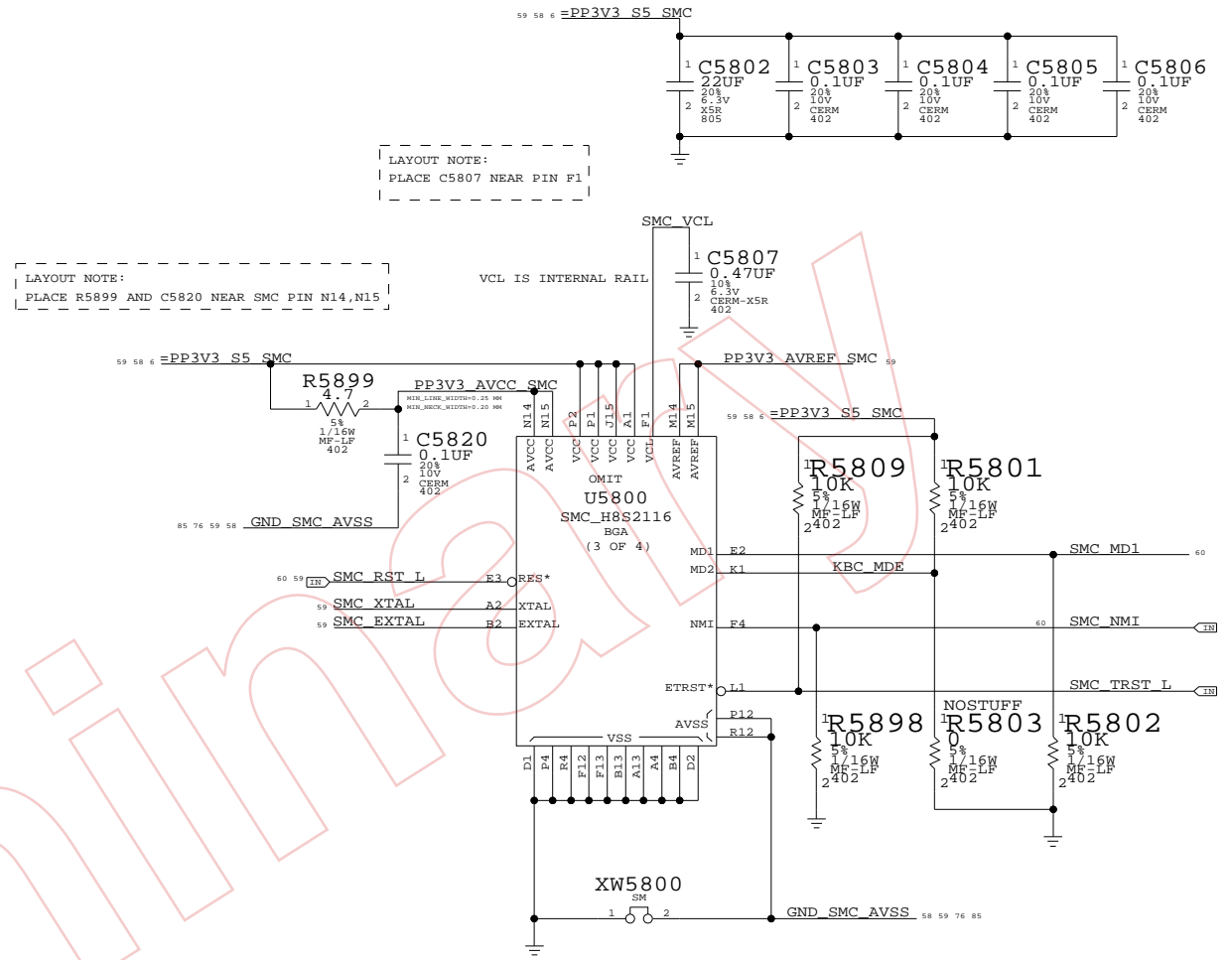
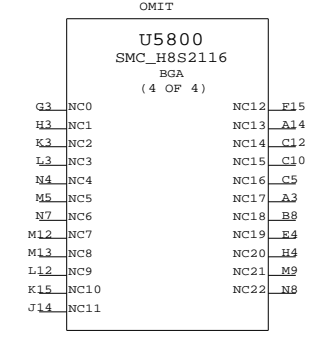
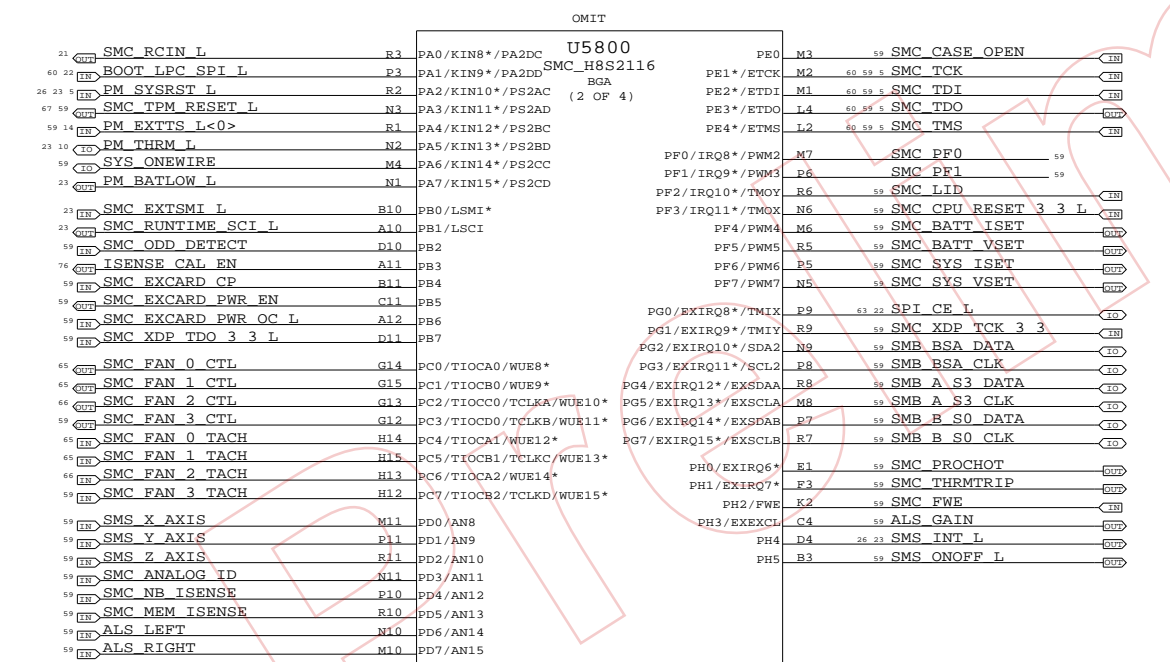
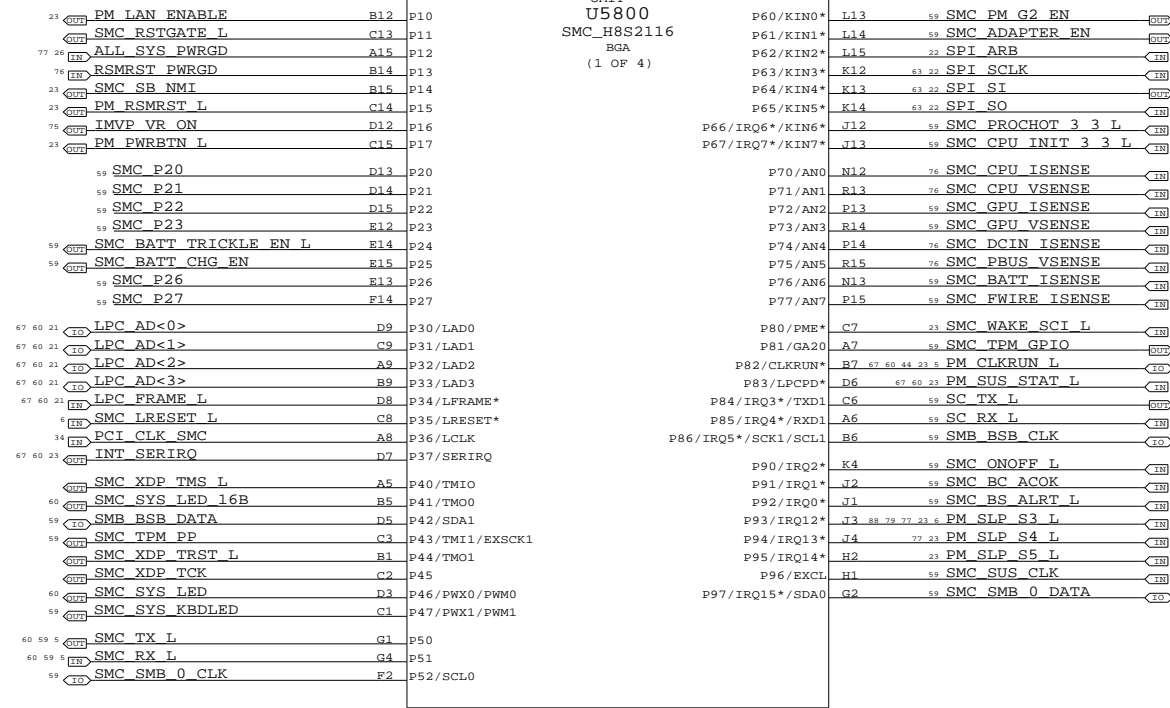
4

3

2

1

UNUSED PINS HAVE THE FORMAT SMC\_XXX WHERE XXX IS THE PORT NUMBER. THEY ARE SET BY SOFTWARE TO BE DRIVEN OUTSIDE ALWAYS SO THEY CAN BE LEFT NO-CONNECTED.



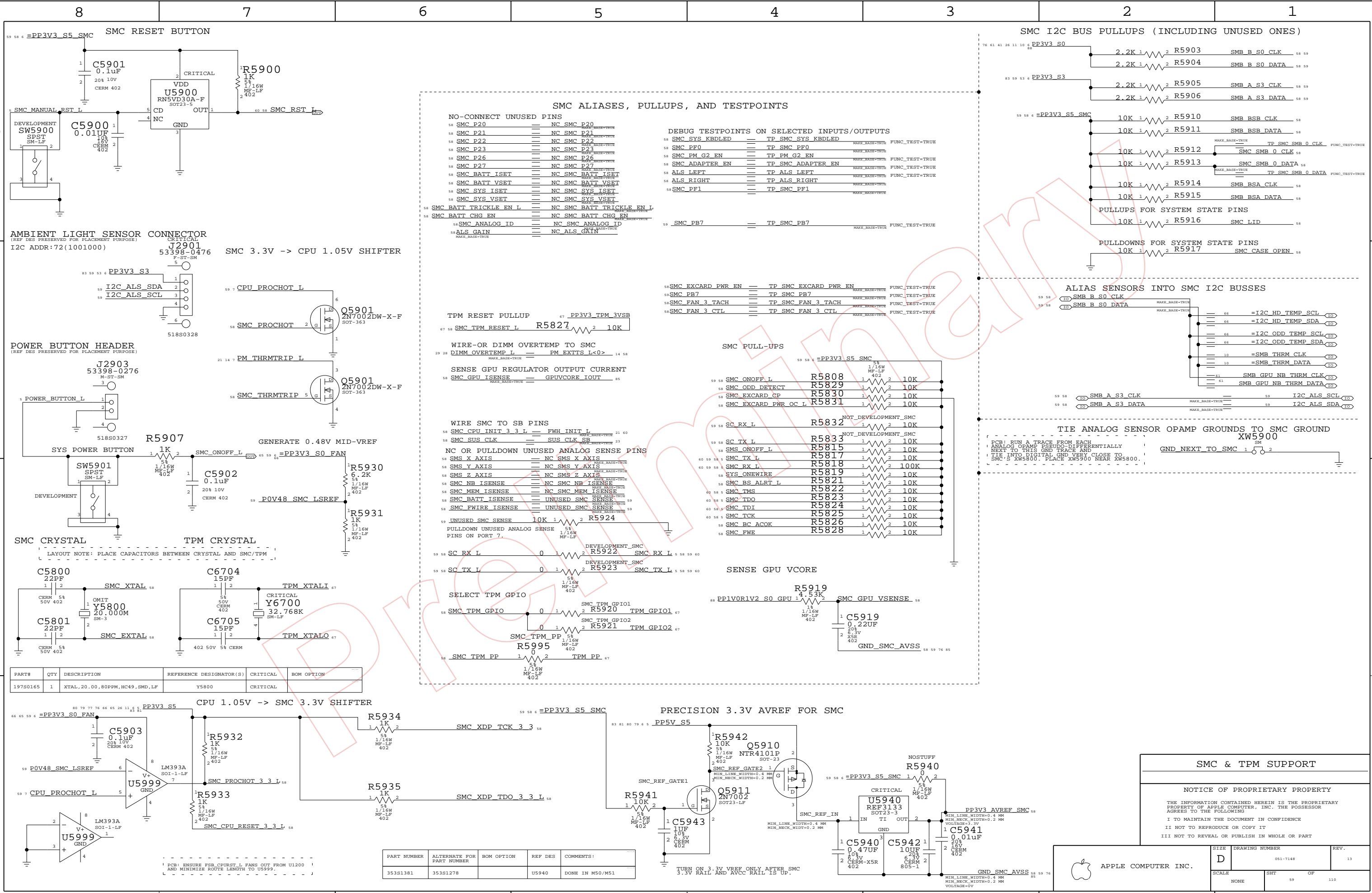
LAYOUT NOTE:  
PLACE C5807 NEAR PIN F1

LAYOUT NOTE:  
PLACE R5899 AND C5820 NEAR SMC PIN N14, N15

SMC  
SYNC\_MASTER=N/A SYNC\_DATE=N/A

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D 051-7148 13  
SCALE NONE SHEET 58 OF 110



### SMC ALIASES, PULLUPS, AND TESTPOINTS

NO-CONNECT UNUSED PINS			
58 SMC P20	==	NC SMC P20	
58 SMC P21	==	NC SMC P21	
58 SMC P22	==	NC SMC P22	
58 SMC P23	==	NC SMC P23	
58 SMC P26	==	NC SMC P26	
58 SMC P27	==	NC SMC P27	
58 SMC BATT ISET	==	NC SMC BATT ISET	
58 SMC BATT VSET	==	NC SMC BATT VSET	
58 SMC SYS ISET	==	NC SMC SYS ISET	
58 SMC SYS VSET	==	NC SMC SYS VSET	
58 SMC BATT TRICKLE EN L	==	NC SMC BATT TRICKLE EN L	
58 SMC BATT CHG EN	==	NC SMC BATT CHG EN	
58 SMC ANALOG ID	==	NC SMC ANALOG ID	
58 ALS GAIN	==	NC ALS GAIN	

DEBUG TESTPOINTS ON SELECTED INPUTS/OUTPUTS			
58 SMC SYS_KBDLED	==	TP_SMC_SYS_KBDLED	MAKE_BASE=TRUE FUNC_TEST=TRUE
58 SMC_PFO	==	TP_SMC_PFO	MAKE_BASE=TRUE
58 SMC_PM_G2_EN	==	TP_PM_G2_EN	MAKE_BASE=TRUE FUNC_TEST=TRUE
58 SMC_ADAPTER_EN	==	TP_SMC_ADAPTER_EN	MAKE_BASE=TRUE FUNC_TEST=TRUE
58 ALS_LEFT	==	TP_ALS_LEFT	MAKE_BASE=TRUE FUNC_TEST=TRUE
58 ALS_RIGHT	==	TP_ALS_RIGHT	MAKE_BASE=TRUE FUNC_TEST=TRUE
58 SMC_PPF1	==	TP_SMC_PPF1	MAKE_BASE=TRUE
58 SMC_PB7	==	TP_SMC_PB7	MAKE_BASE=TRUE FUNC_TEST=TRUE

SMC PULL-UPS			
58 SMC_ONOFF_L	==	R5808	10K
58 SMC_ODD_DETECT	==	R5829	10K
58 SMC_EXCARD_CP	==	R5830	10K
58 SMC_EXCARD_PWR_OC_L	==	R5831	10K
58 SC_RX_L	==	R5832	10K
58 SC_TX_L	==	R5833	10K
58 SMC_ONOFF_L	==	R5815	10K
58 SMC_TX_L	==	R5817	10K
58 SMC_RX_L	==	R5818	100K
58 SMC_ONEWIRE	==	R5819	10K
58 SMC_BS_ALERT_L	==	R5821	10K
58 SMC_TMS	==	R5822	10K
58 SMC_TDO	==	R5823	10K
58 SMC_TDI	==	R5824	10K
58 SMC_TCK	==	R5825	10K
58 SMC_BC_ACOK	==	R5826	10K
58 SMC_FWE	==	R5828	10K

WIRE SMC TO SB PINS			
58 SMC_CPU_INIT_3_3_L	==	FWH_INIT_L	21 60
58 SMC_SUS_CLK	==	SUS_CLK_SB	23

NC OR PULLDOWN UNUSED ANALOG SENSE PINS			
58 SMC_X_AXIS	==	NC_SMC_X_AXIS	
58 SMC_Y_AXIS	==	NC_SMC_Y_AXIS	
58 SMC_Z_AXIS	==	NC_SMC_Z_AXIS	
58 SMC_NB_ISENSE	==	NC_SMC_NB_ISENSE	
58 SMC_MEM_ISENSE	==	NC_SMC_MEM_ISENSE	
58 SMC_BATT_ISENSE	==	UNUSED_SMC_ISENSE	
58 SMC_FWIRE_ISENSE	==	UNUSED_SMC_ISENSE	

SELECT TPM GPIO			
58 SMC_TPM_GPIO	==	R5920	TPM_GPIO1
58 SMC_TPM_PP	==	R5921	TPM_GPIO2

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0165	1	XTAL, 20.00, 80PPM, HC49, SMD, LF	Y5800	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
35381381	35381278		U5940	DONE IN M50/M51

**SMC & TPM SUPPORT**

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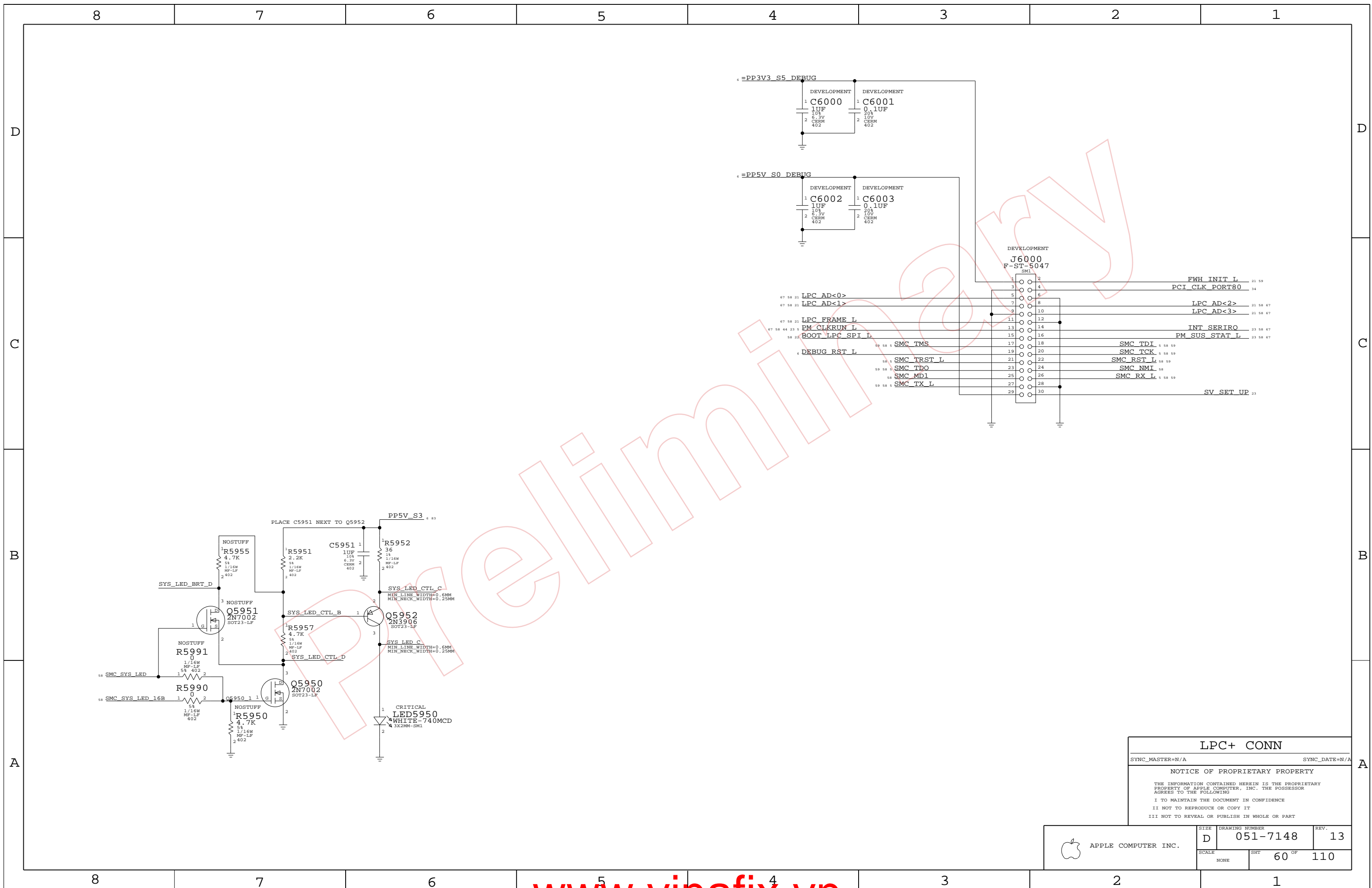
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SIZE	DRAWING NUMBER	REV.
D	051-7148	13

APPLE COMPUTER INC.

SCALE	SHT	OF
NONE	59	110



**LPC+ CONN**

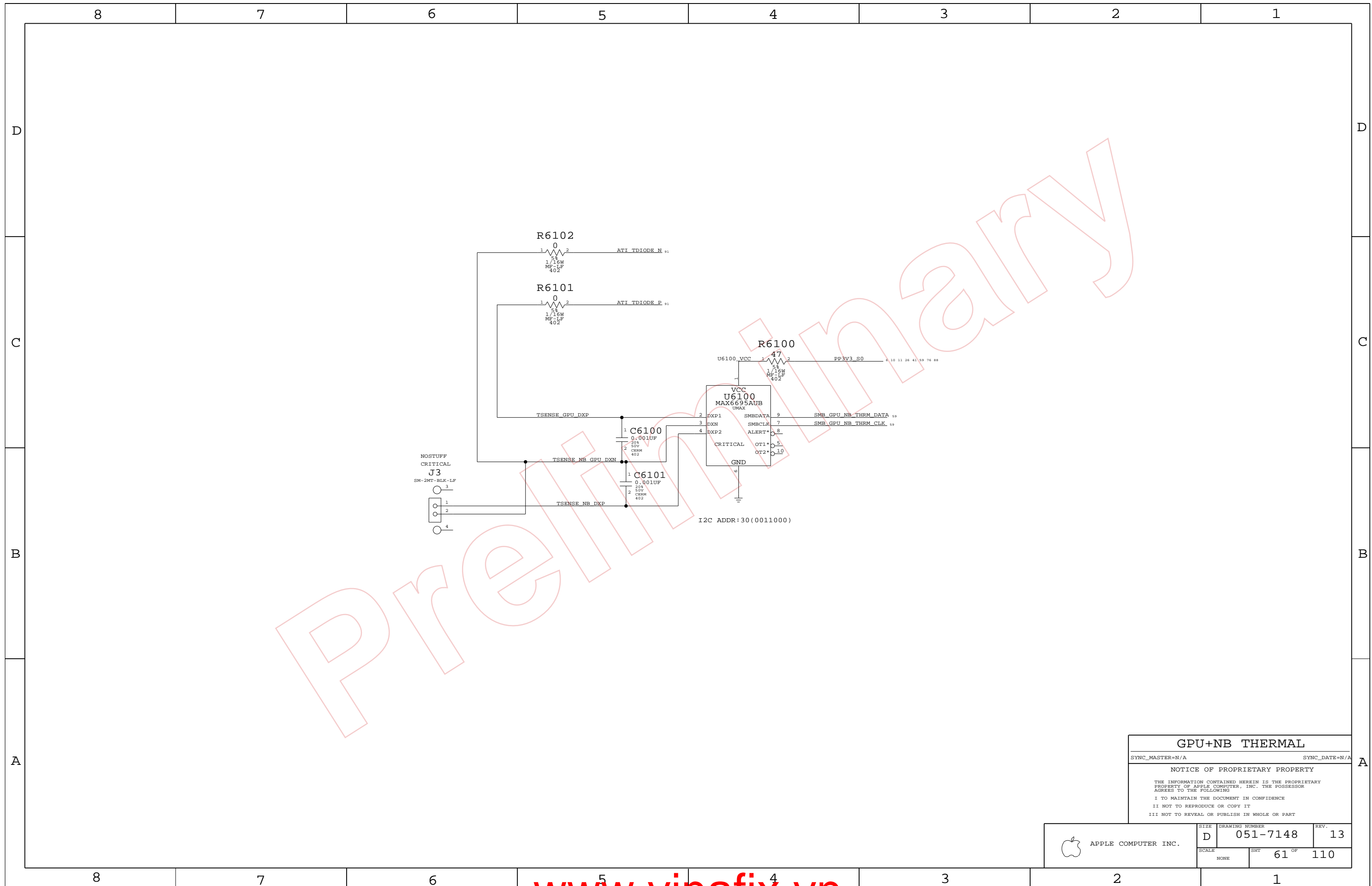
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APPLE COMPUTER INC.	SIZE <b>D</b>	DRAWING NUMBER <b>051-7148</b>	REV. <b>13</b>
	SCALE NONE	SHT 60 OF	110



Preiminary

**GPU+NB THERMAL**

SYNC\_MASTER=N/A SYNC\_DATE=N/A

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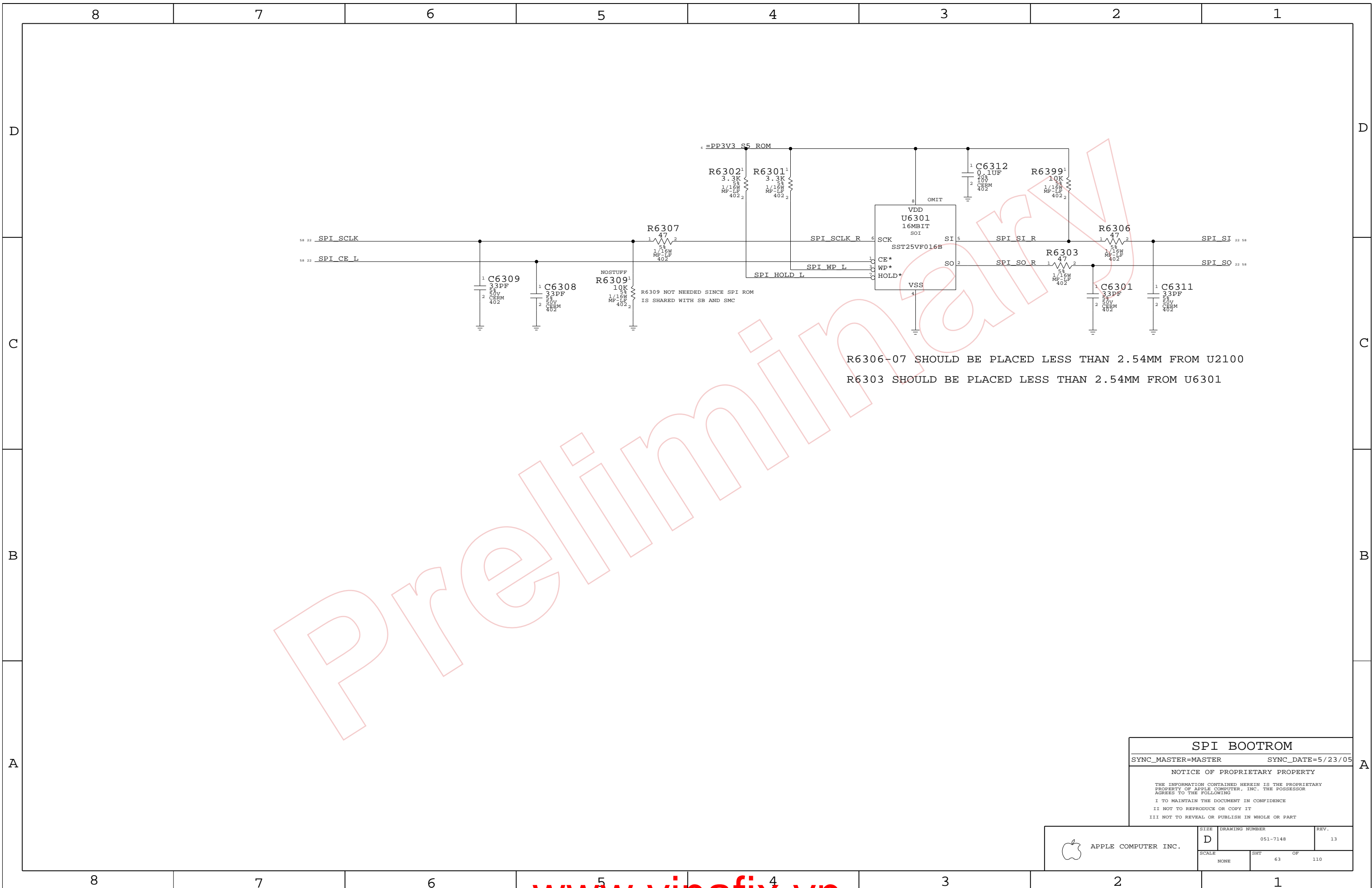
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	13
SCALE		SHT	OF
NONE		61	110





R6306-07 SHOULD BE PLACED LESS THAN 2.54MM FROM U2100  
 R6303 SHOULD BE PLACED LESS THAN 2.54MM FROM U6301


**SPI BOOTROM**

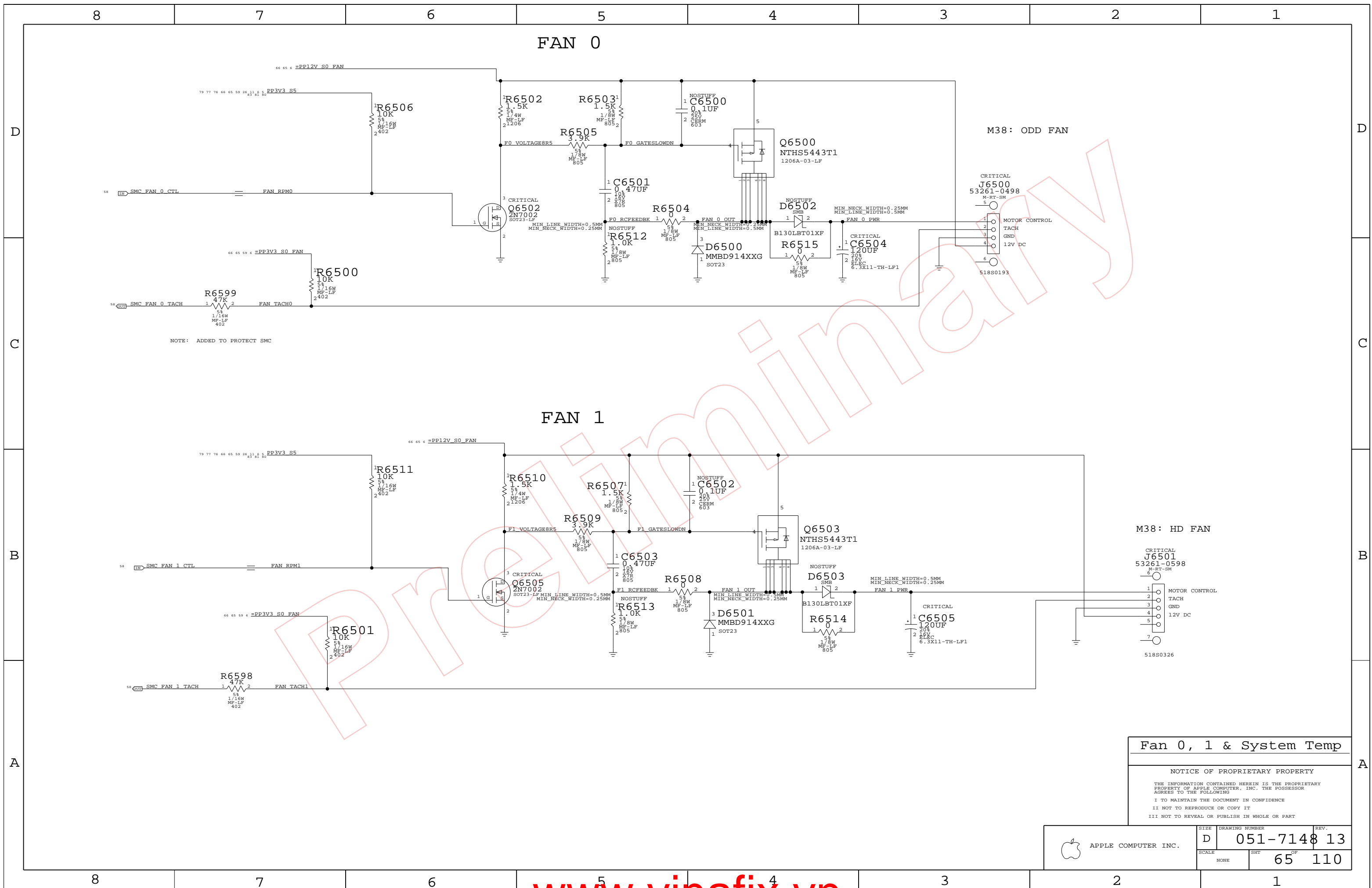
SYNC\_MASTER=MASTER      SYNC\_DATE=5/23/05

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 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	13
SCALE	SHT	OF	
NONE	63	110	

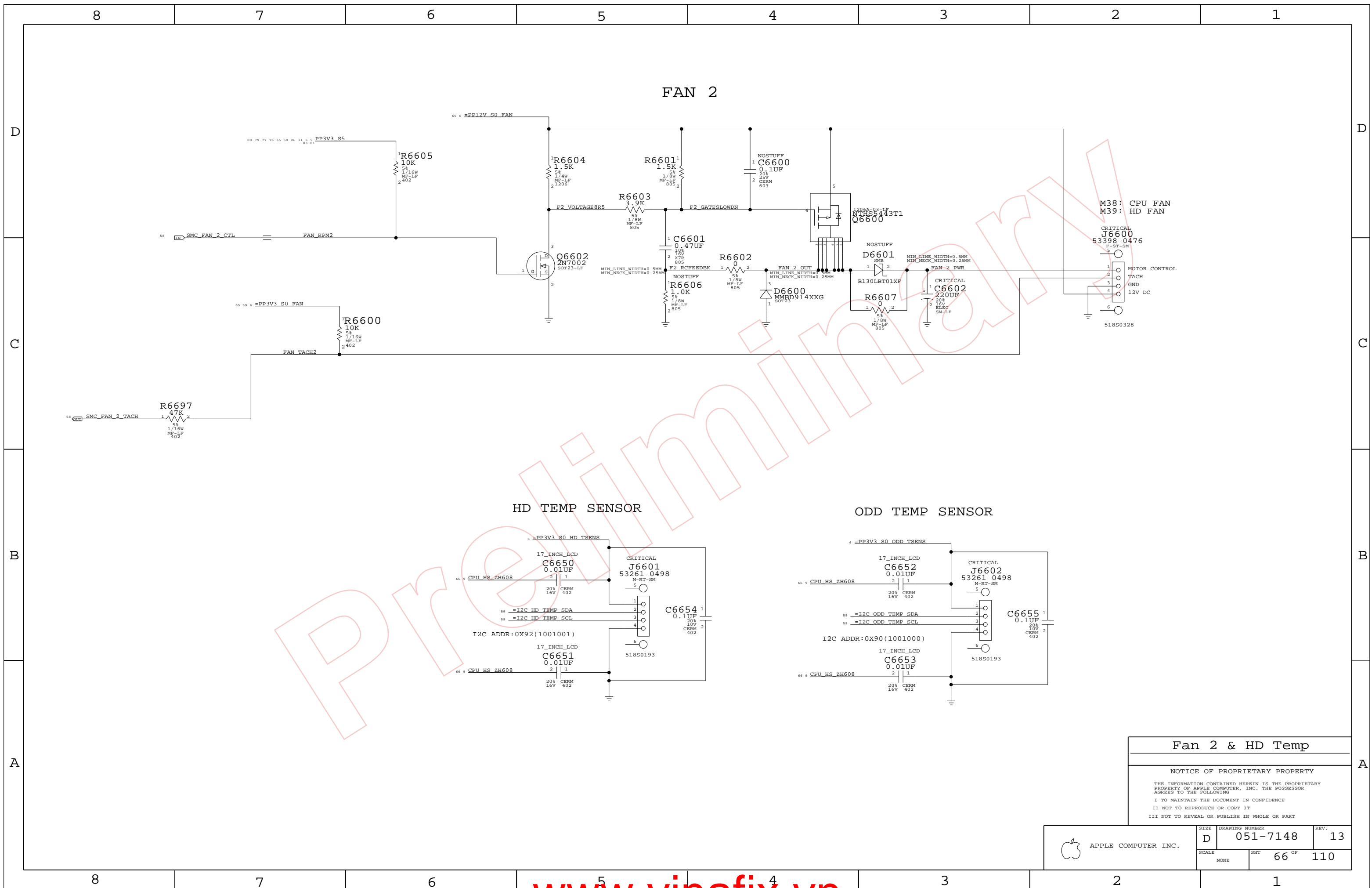


Fan 0, 1 & System Temp

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	13
SCALE	SHT	OF	
NONE	65	110	



FAN 2

HD TEMP SENSOR

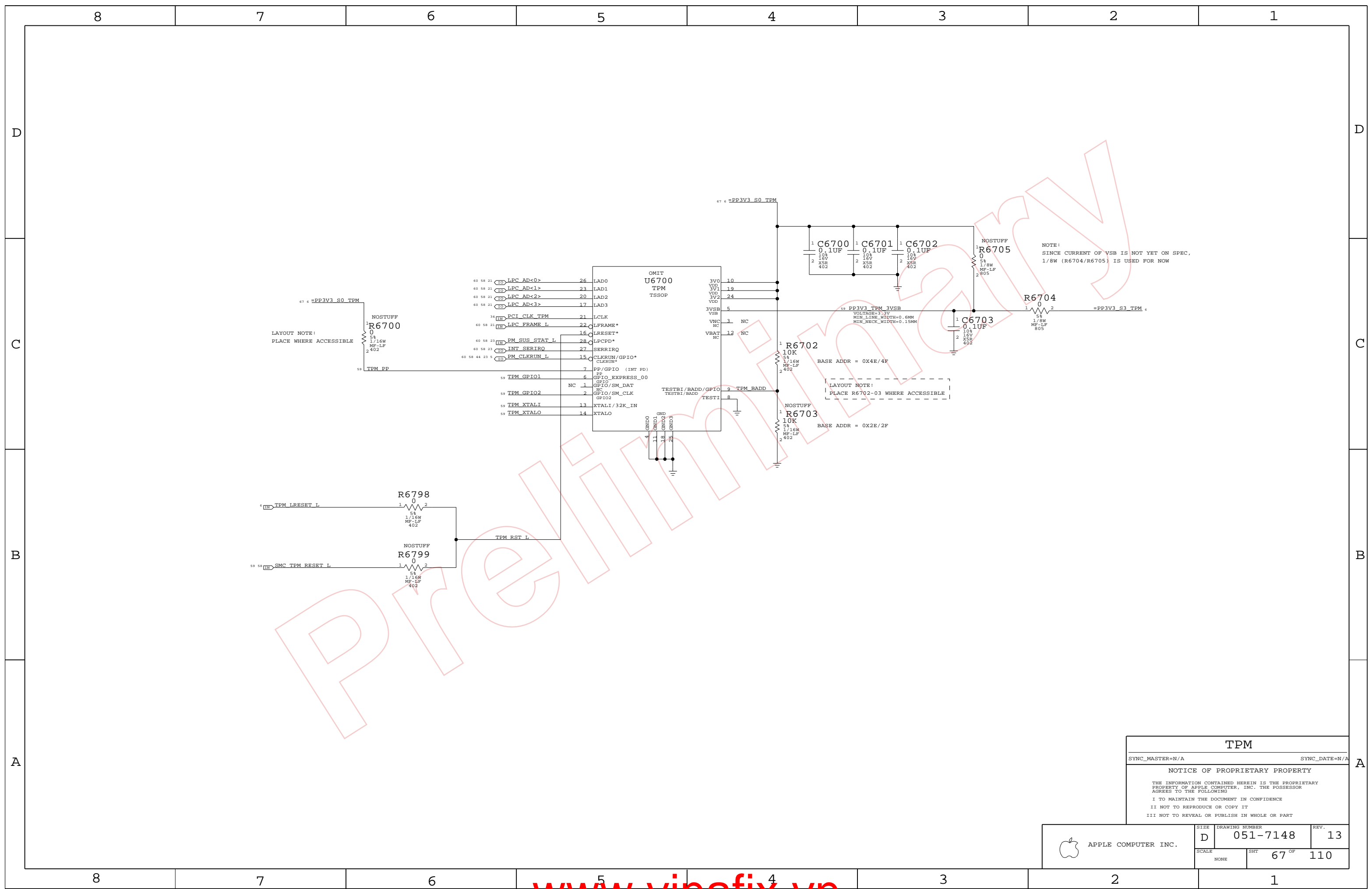
ODD TEMP SENSOR

Fan 2 & HD Temp

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	13
SCALE	SHT	OF	
NONE	66	110	



LAYOUT NOTE:  
PLACE WHERE ACCESSIBLE

LAYOUT NOTE:  
PLACE R6702-03 WHERE ACCESSIBLE

NOTE:  
SINCE CURRENT OF VSB IS NOT YET ON SPEC,  
1/8W (R6704/R6705) IS USED FOR NOW

**TPM**

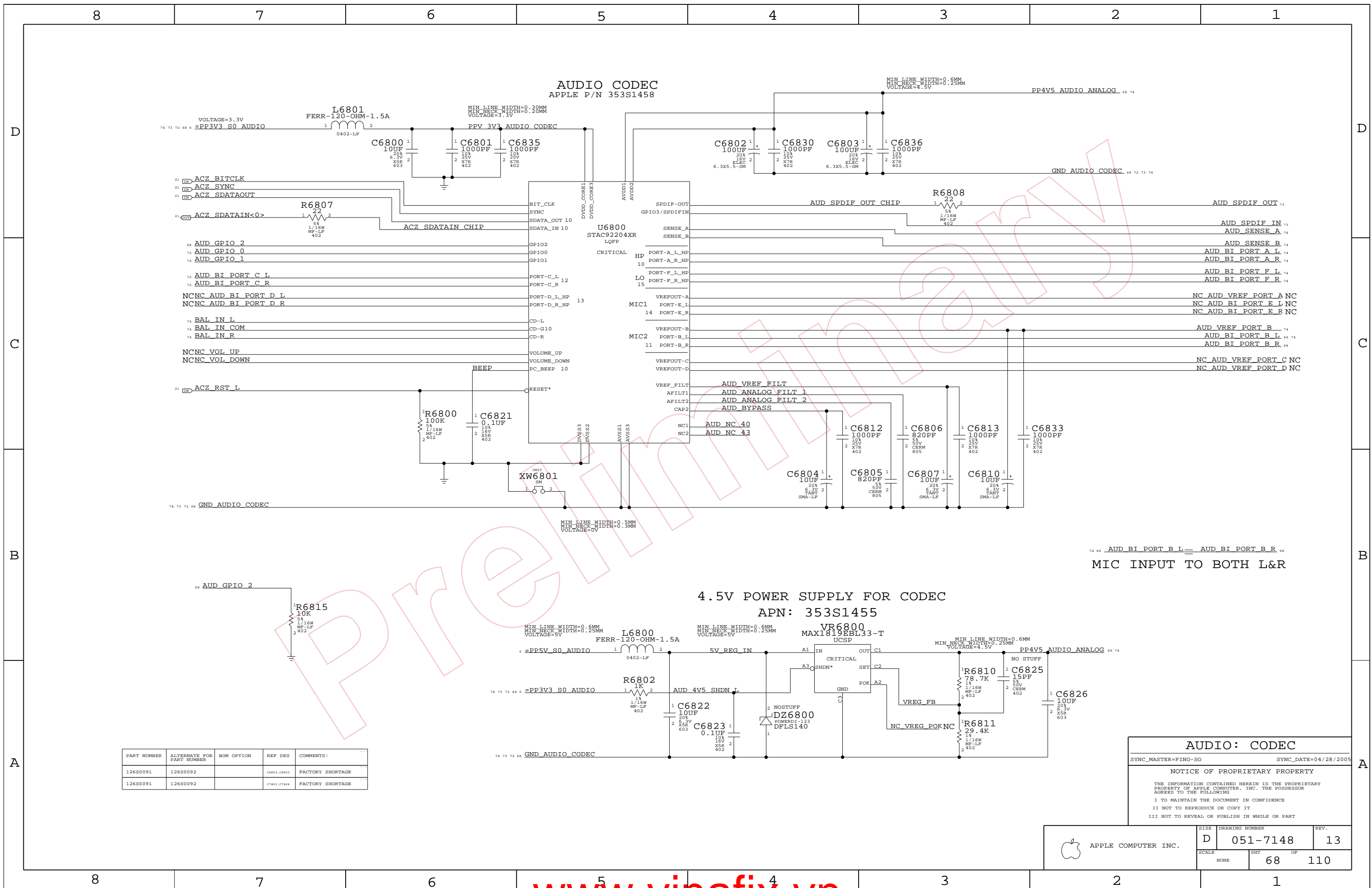
SYNC\_MASTER=N/A SYNC\_DATE=N/A

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	D	051-7148	13
SCALE	SHT	67 OF 110	
NONE			



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
126S0091	126S0092		C6802, C6803	FACTORY SHORTAGE
126S0091	126S0092		C7403, C7404	FACTORY SHORTAGE

**AUDIO: CODEC**

SYNC\_MASTER=FINO-SO      SYNC\_DATE=04/28/2005

**NOTICE OF PROPRIETARY PROPERTY**

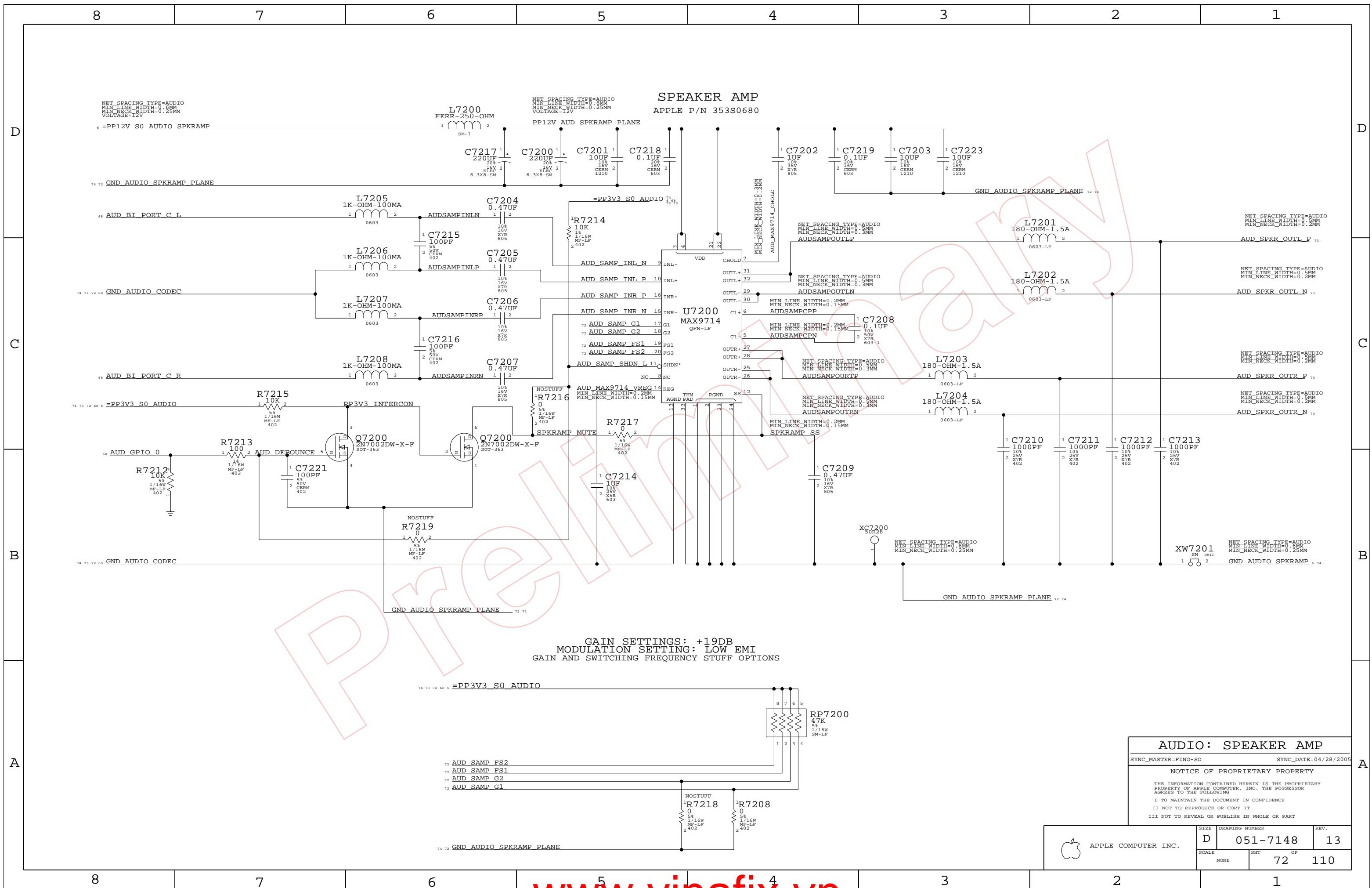
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	13
SCALE	NONE	SHT OF	68 110



**SPEAKER AMP**  
APPLE P/N 353S0680

GAIN SETTINGS: +19DB  
MODULATION SETTING: LOW EMI  
GAIN AND SWITCHING FREQUENCY STUFF OPTIONS

**AUDIO: SPEAKER AMP**  
SYNC\_MASTER=FINO-SO SYNC\_DATE=04/28/2005

NOTICE OF PROPRIETARY PROPERTY

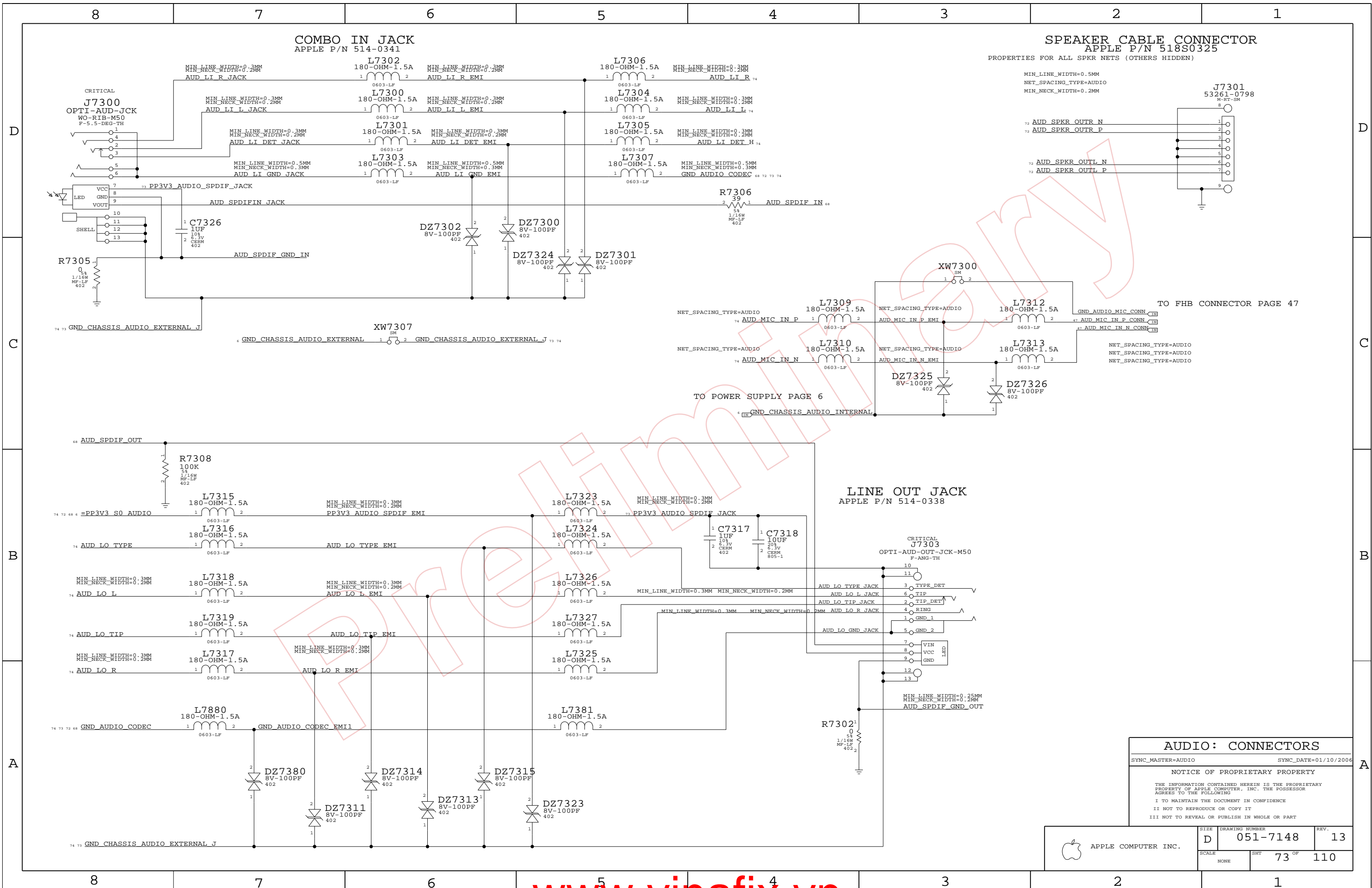
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	13
SCALE	NONE	SHT OF	72 OF 110



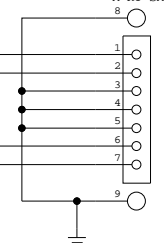
**SPEAKER CABLE CONNECTOR**  
APPLE P/N 518S0325

PROPERTIES FOR ALL SPKR NETS (OTHERS HIDDEN)

MIN\_LINE\_WIDTH=0.5MM  
NET\_SPACING\_TYPE=AUDIO  
MIN\_NECK\_WIDTH=0.2MM

J7301  
53261-0798  
M-RT-SM

72 AUD\_SPKR\_OUTR\_N  
72 AUD\_SPKR\_OUTR\_P  
72 AUD\_SPKR\_OUTL\_N  
72 AUD\_SPKR\_OUTL\_P



**COMBO IN JACK**  
APPLE P/N 514-0341

**LINE OUT JACK**  
APPLE P/N 514-0338

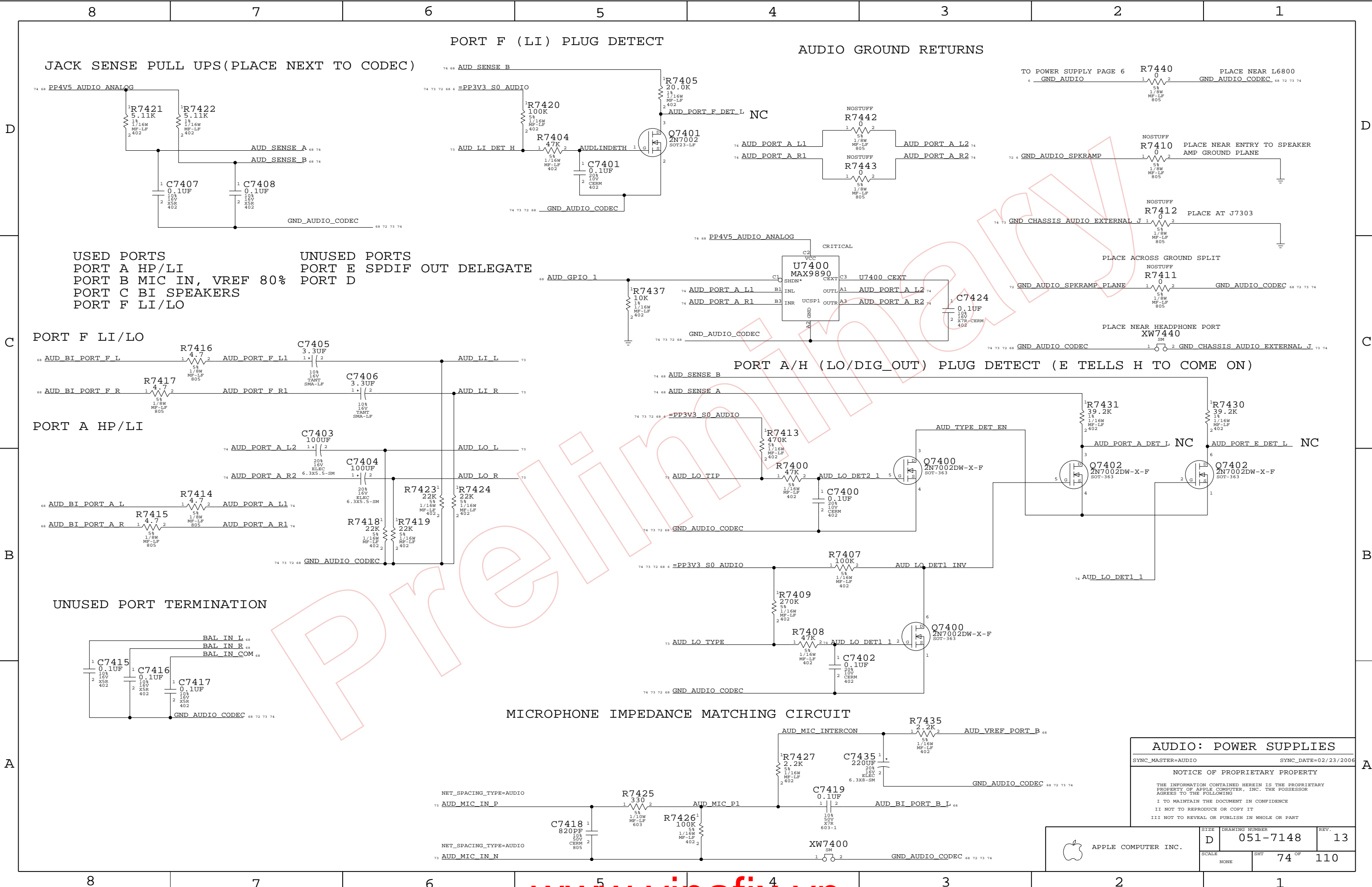
**AUDIO: CONNECTORS**

SYNC\_MASTER=AUDIO SYNC\_DATE=01/10/2006

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	D	051-7148	13
SCALE	SHT	73 OF	110
NONE			



JACK SENSE PULL UPS (PLACE NEXT TO CODEC)

PORT F (LI) PLUG DETECT

AUDIO GROUND RETURNS

USED PORTS  
 PORT A HP/LI  
 PORT B MIC IN, VREF 80%  
 PORT C BI SPEAKERS  
 PORT F LI/LO

UNUSED PORTS  
 PORT E SPDIF OUT DELEGATE  
 PORT D

PORT F LI/LO

PORT A HP/LI

UNUSED PORT TERMINATION

MICROPHONE IMPEDANCE MATCHING CIRCUIT

AUDIO: POWER SUPPLIES

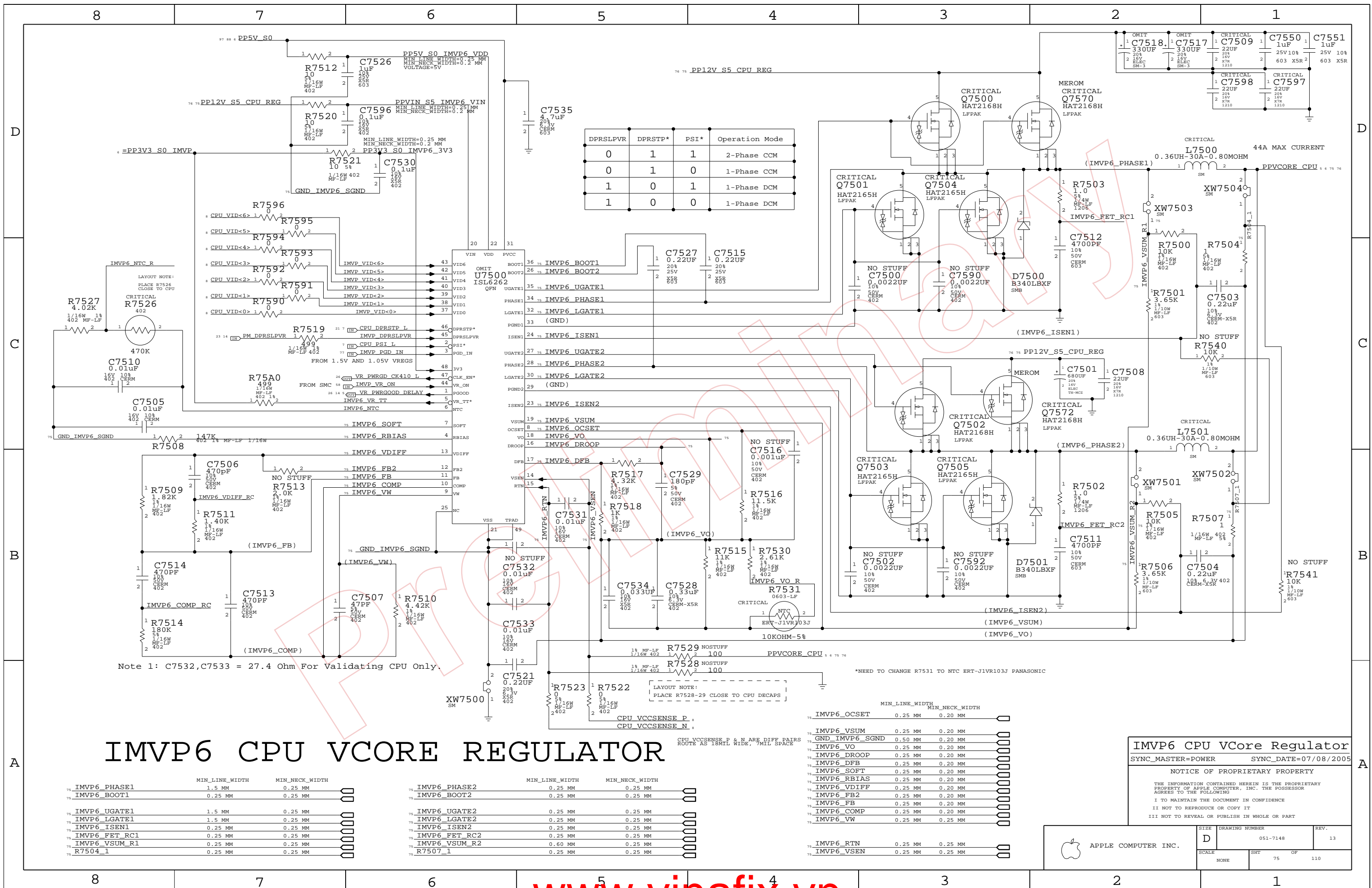
SYNC\_MASTER=AUDIO SYNC\_DATE=02/23/2006

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	D	051-7148	13
SCALE	SHT	74 OF	110
NONE			





DPRSLPVR	DPRSTP*	PSI*	Operation Mode
0	1	1	2-Phase CCM
0	1	0	1-Phase CCM
1	0	1	1-Phase DCM
1	0	0	1-Phase DCM

# IMVP6 CPU VCore Regulator

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
75 IMVP6_PHASE1	1.5 MM	0.25 MM
75 IMVP6_BOOT1	0.25 MM	0.25 MM
75 IMVP6_UGATE1	1.5 MM	0.25 MM
75 IMVP6_LGATE1	1.5 MM	0.25 MM
75 IMVP6_ISEN1	0.25 MM	0.25 MM
75 IMVP6_FET_RC1	0.25 MM	0.25 MM
75 IMVP6_VSUM_R1	0.25 MM	0.25 MM
75 R7504_1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
75 IMVP6_PHASE2	0.25 MM	0.25 MM
75 IMVP6_BOOT2	0.25 MM	0.25 MM
75 IMVP6_UGATE2	0.25 MM	0.25 MM
75 IMVP6_LGATE2	0.25 MM	0.25 MM
75 IMVP6_ISEN2	0.25 MM	0.25 MM
75 IMVP6_FET_RC2	0.25 MM	0.25 MM
75 IMVP6_VSUM_R2	0.60 MM	0.25 MM
75 R7507_1	0.25 MM	0.25 MM

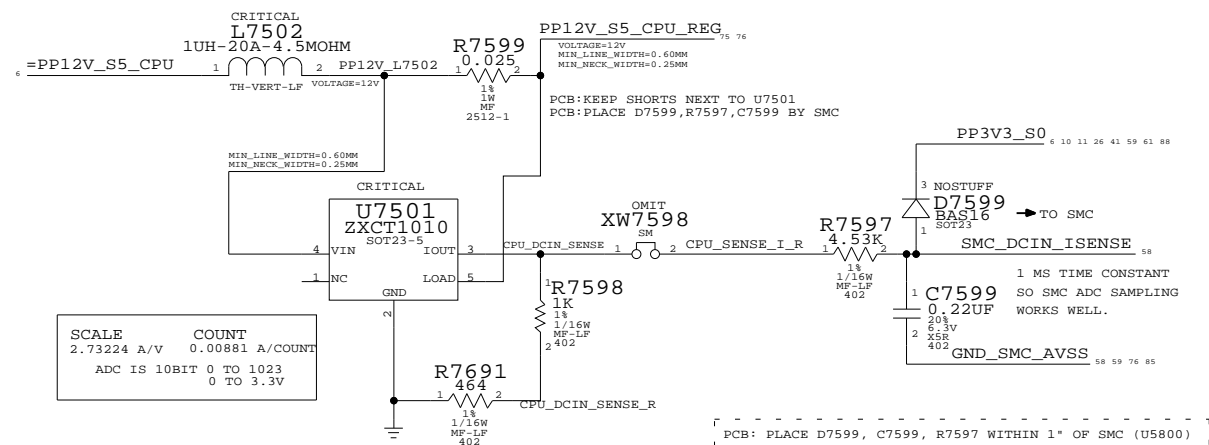
	MIN_LINE_WIDTH	MIN_NECK_WIDTH
75 IMVP6_OCSET	0.25 MM	0.20 MM
75 IMVP6_VSUM	0.25 MM	0.20 MM
75 GND_IMVP6_SGND	0.50 MM	0.20 MM
75 IMVP6_VO	0.25 MM	0.20 MM
75 IMVP6_DROOP	0.25 MM	0.20 MM
75 IMVP6_DFB	0.25 MM	0.20 MM
75 IMVP6_SOFT	0.25 MM	0.20 MM
75 IMVP6_RBIAS	0.25 MM	0.20 MM
75 IMVP6_VDIFF	0.25 MM	0.20 MM
75 IMVP6_FB2	0.25 MM	0.20 MM
75 IMVP6_FB	0.25 MM	0.20 MM
75 IMVP6_COMP	0.25 MM	0.20 MM
75 IMVP6_VW	0.25 MM	0.25 MM
75 IMVP6_RTIN	0.25 MM	0.25 MM
75 IMVP6_VSEN	0.25 MM	0.25 MM

**IMVP6 CPU VCore Regulator**  
 SYNC\_MASTER=POWER SYNC\_DATE=07/08/2005

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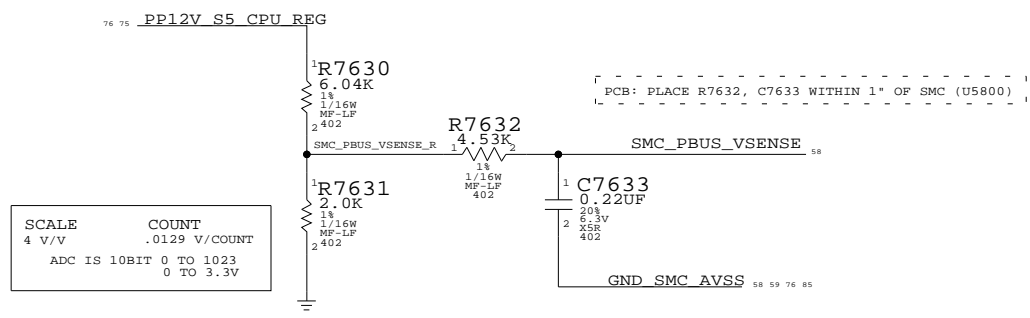
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	13
SCALE	SHEET	OF	
NONE	75	110	

**PROCESSOR VCORE CURRENT SENSE**  
(USING 12V INPUT CURRENT TO DERIVE CPU CURRENT)



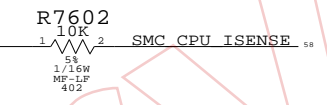
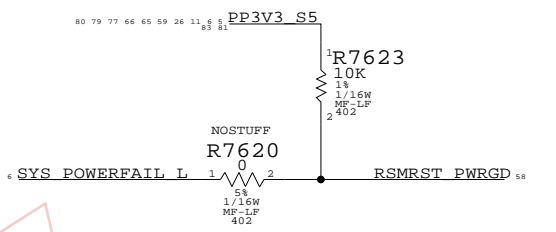
SCALE COUNT  
2.73224 A/V 0.00881 A/COUNT  
ADC IS 10BIT 0 TO 1023  
0 TO 3.3V

**PROCESSOR DCIN VOLTAGE SENSE**  
(SCALING 12V INPUT VOLTAGE TO SMC)

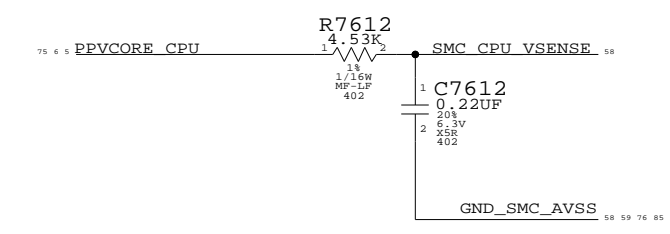


SCALE COUNT  
4 V/V .0129 V/COUNT  
ADC IS 10BIT 0 TO 1023  
0 TO 3.3V

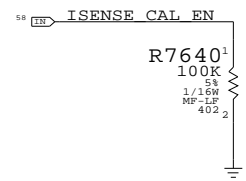
**SMC PWRGD PULLUP**



**PROCESSOR VCORE SENSE**

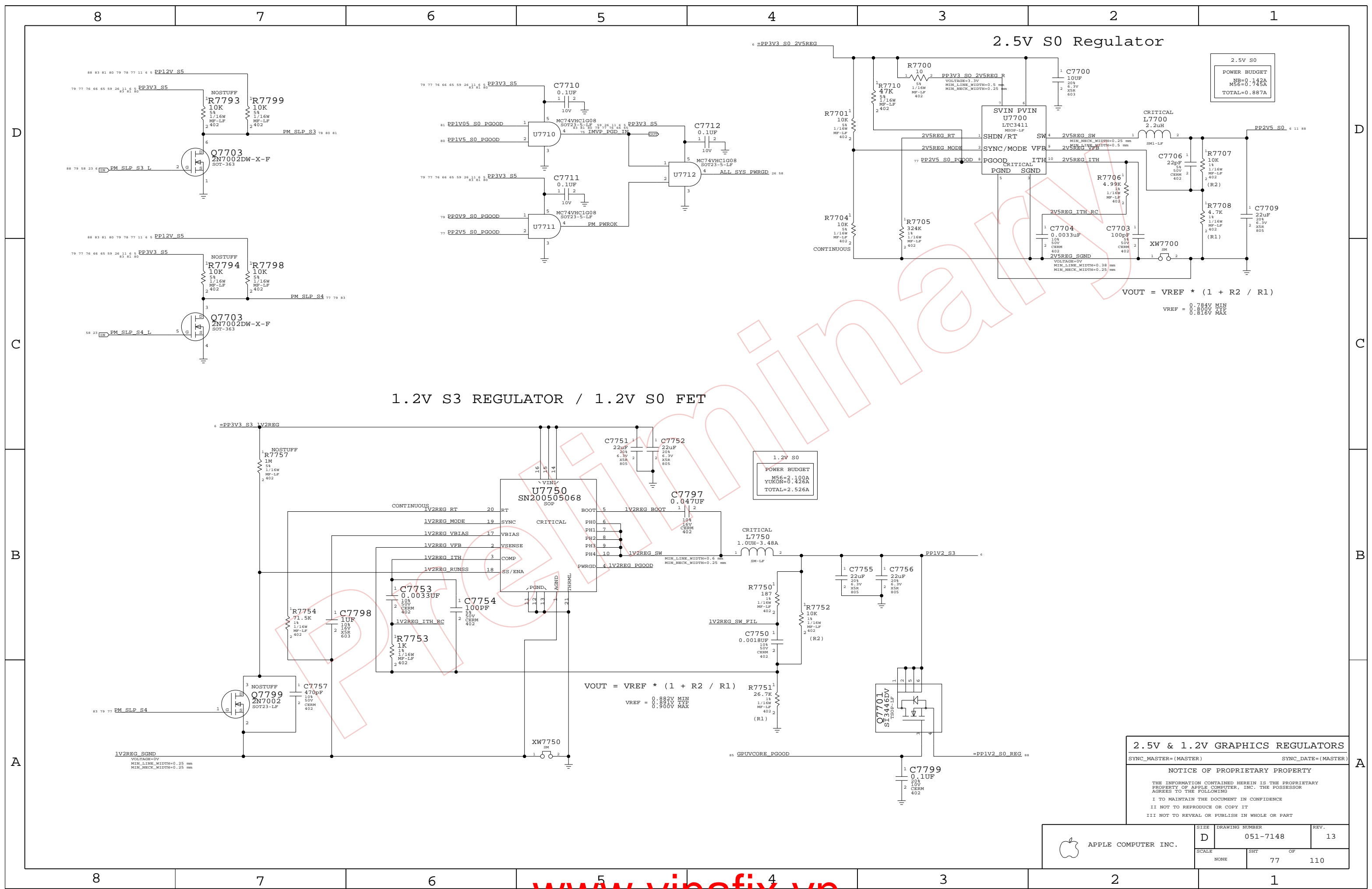


**Current Sense Calibration Circuit**  
Switches in fixed load on power supplies to calibrate current sense circuits



**CPU SENSE CIRCUITRIES**  
SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)  
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	13
SCALE	SHT	76 OF	110
NONE			



**2.5V & 1.2V GRAPHICS REGULATORS**

SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)

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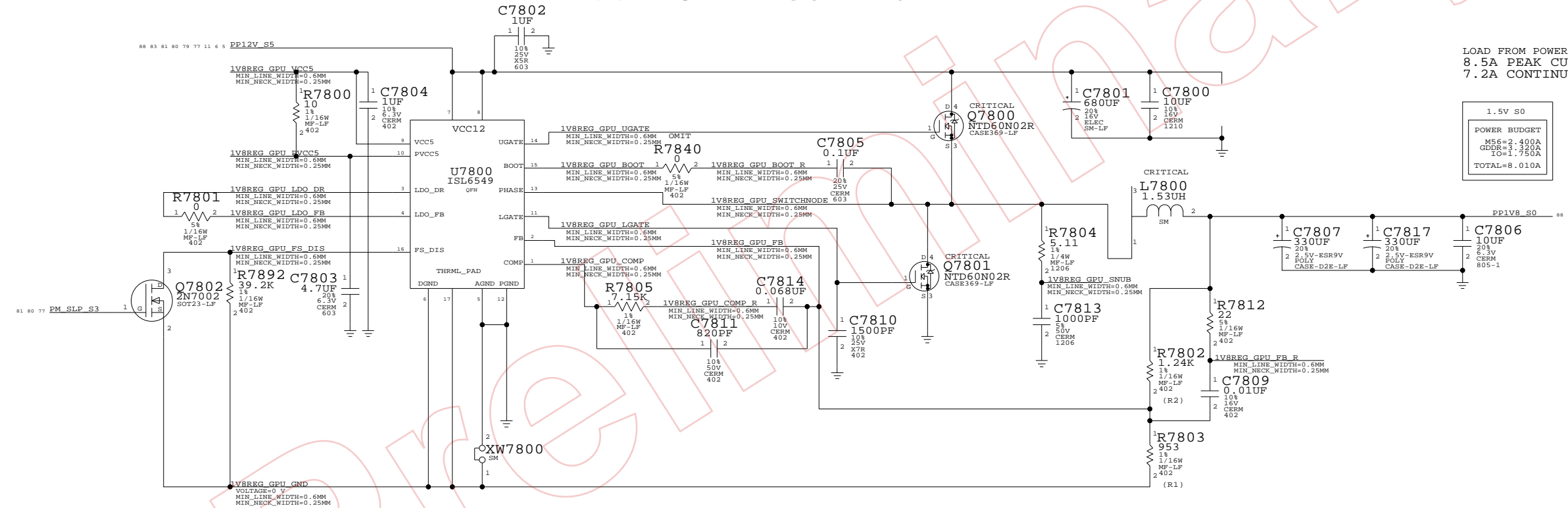
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	13
SCALE	SHT	OF	
NONE	77	110	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
11480514	1	5.11 OHM 0402 1% 1/16W LF	R7840		

### 1.8V S0 REGULATOR



LOAD FROM POWER BUDGET  
8.5A PEAK CURRENT DRAW  
7.2A CONTINUOUS CURRENT DRAW

1.5V S0	
POWER BUDGET	
M56=2.400A	
GDDR=3.300A	
IO=1.750A	
TOTAL=8.010A	

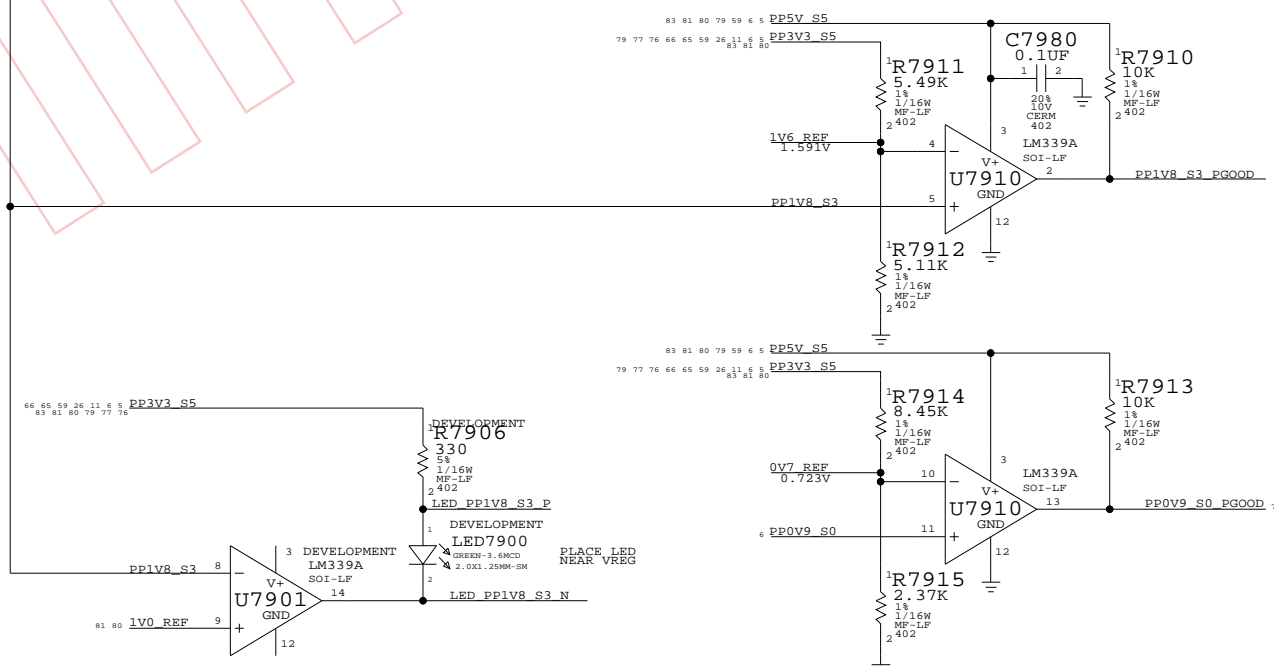
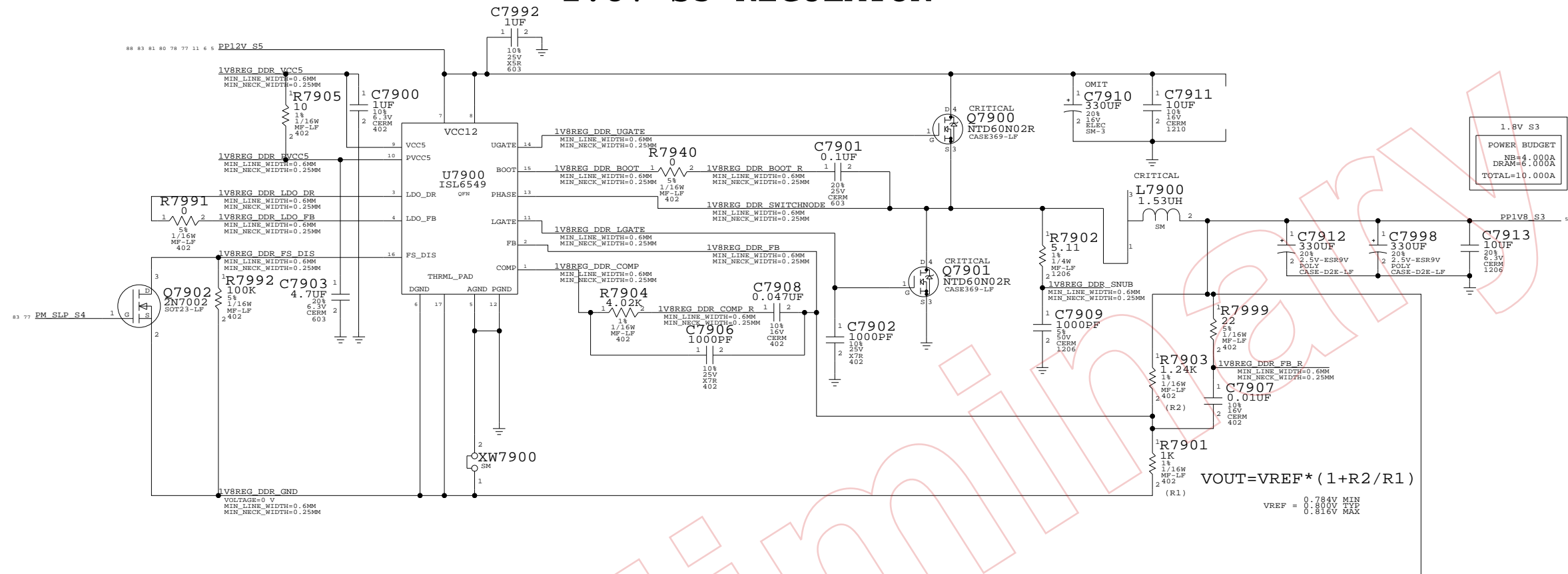
$$V_{OUT} = V_{REF} * (1 + R2/R1)$$

VREF = 0.784V MIN  
VREF = 0.800V TYP  
VREF = 0.816V MAX

**1.8V GDDR REGULATOR**  
 SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)  
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	13
SCALE	SHT	78 OF 110	
NONE			

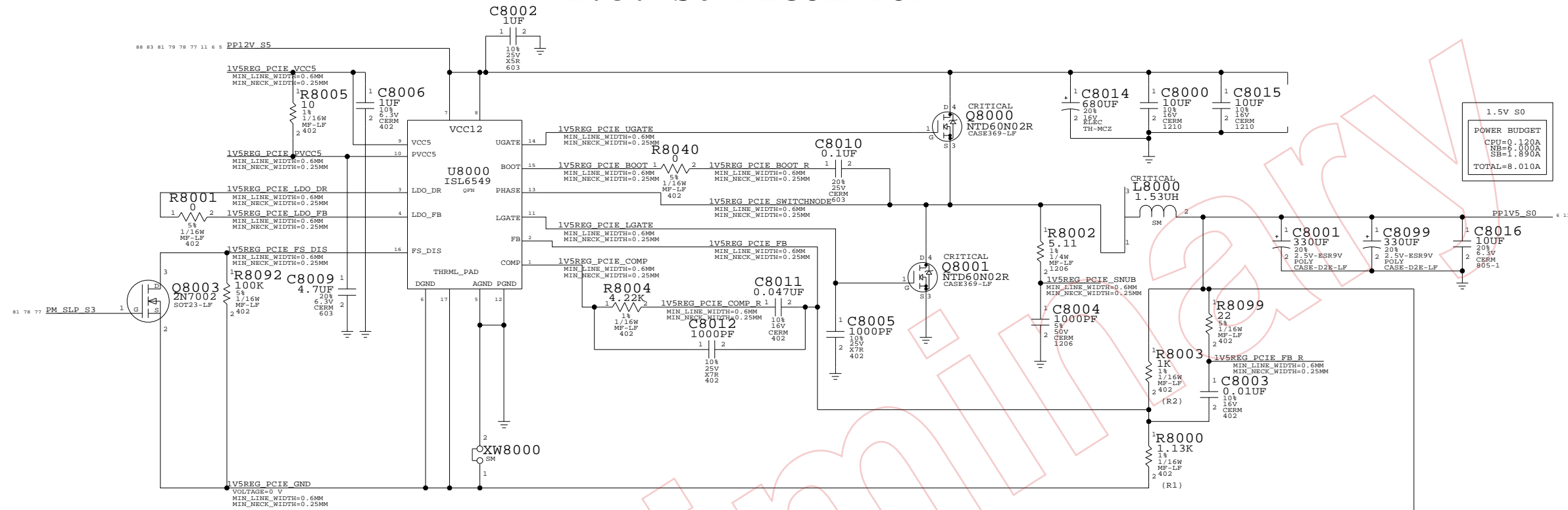
# 1.8V S3 REGULATOR



**1.8V Vreg**  
 SYNC\_MASTER=M23-PC SYNC\_DATE=04/12/2005  
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	D	051-7148	13
SCALE	SHT	79 OF	110
NONE			

# 1.5V S0 REGULATOR

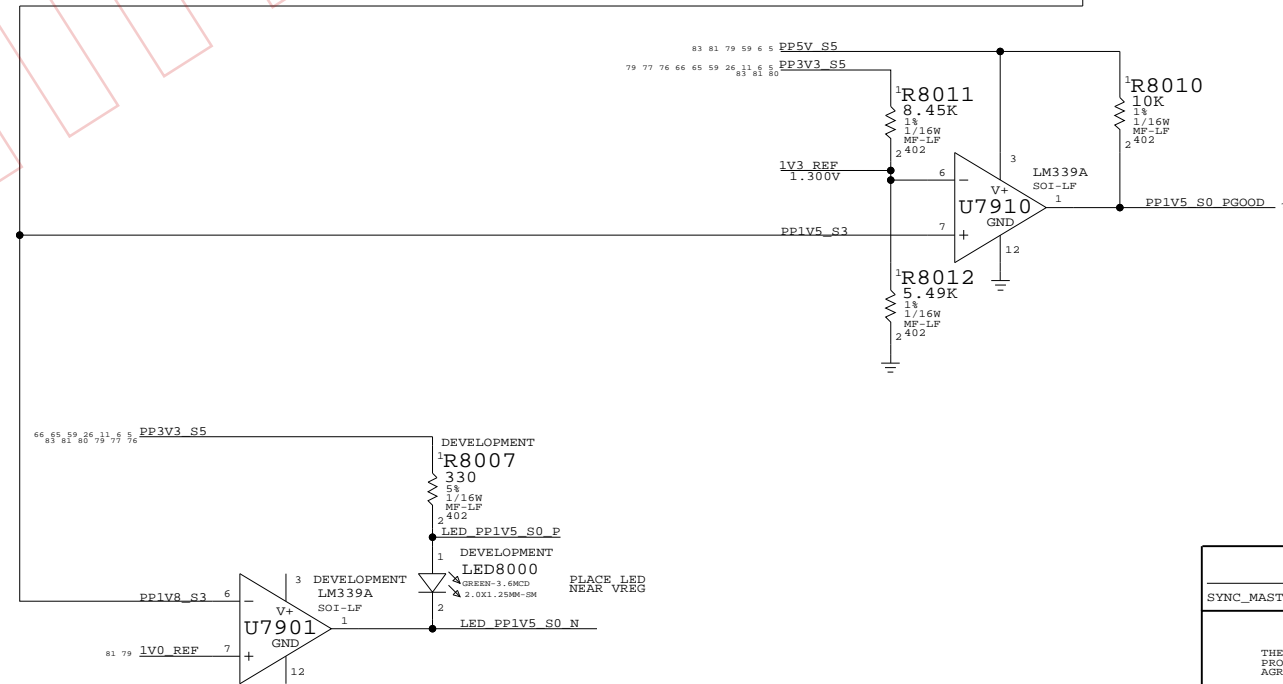


$$V_{OUT} = V_{REF} * (1 + R2/R1)$$

$$V_{REF} = 0.784V \text{ MIN}$$

$$0.800V \text{ TYP}$$

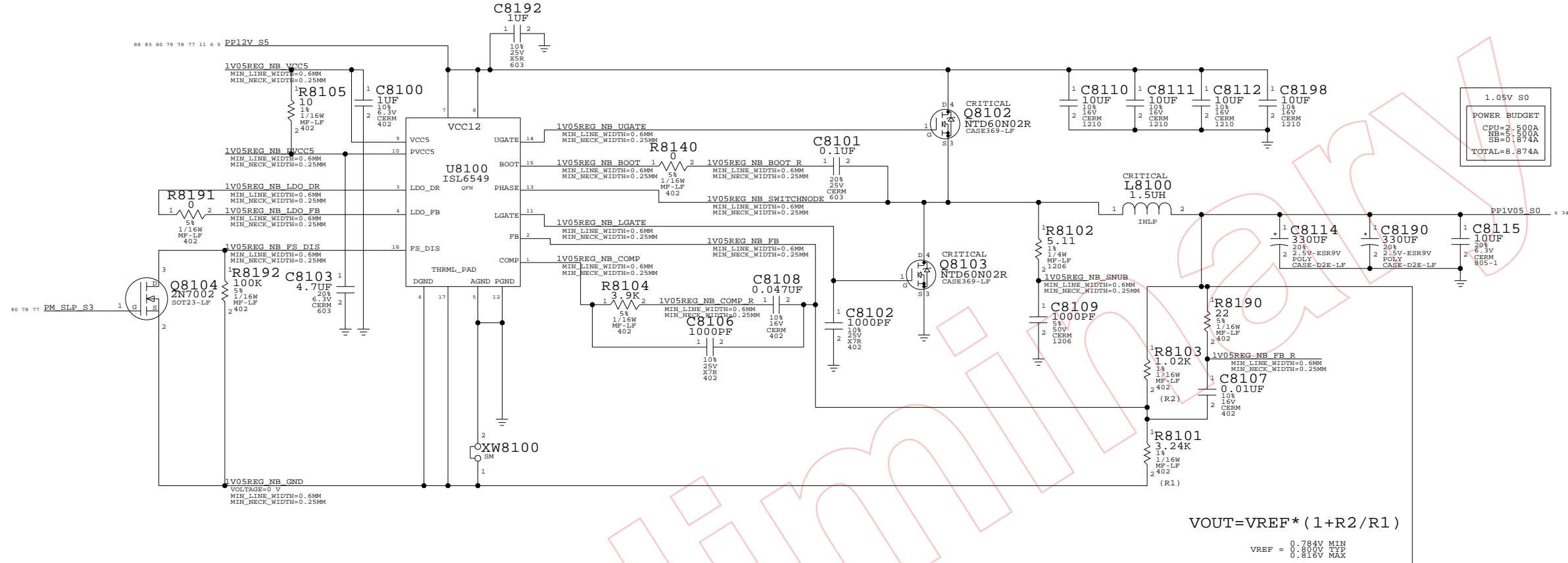
$$0.816V \text{ MAX}$$



**1.5V Vreg**  
 SYNC\_MASTER=FINO-PC SYNC\_DATE=05/18/2005  
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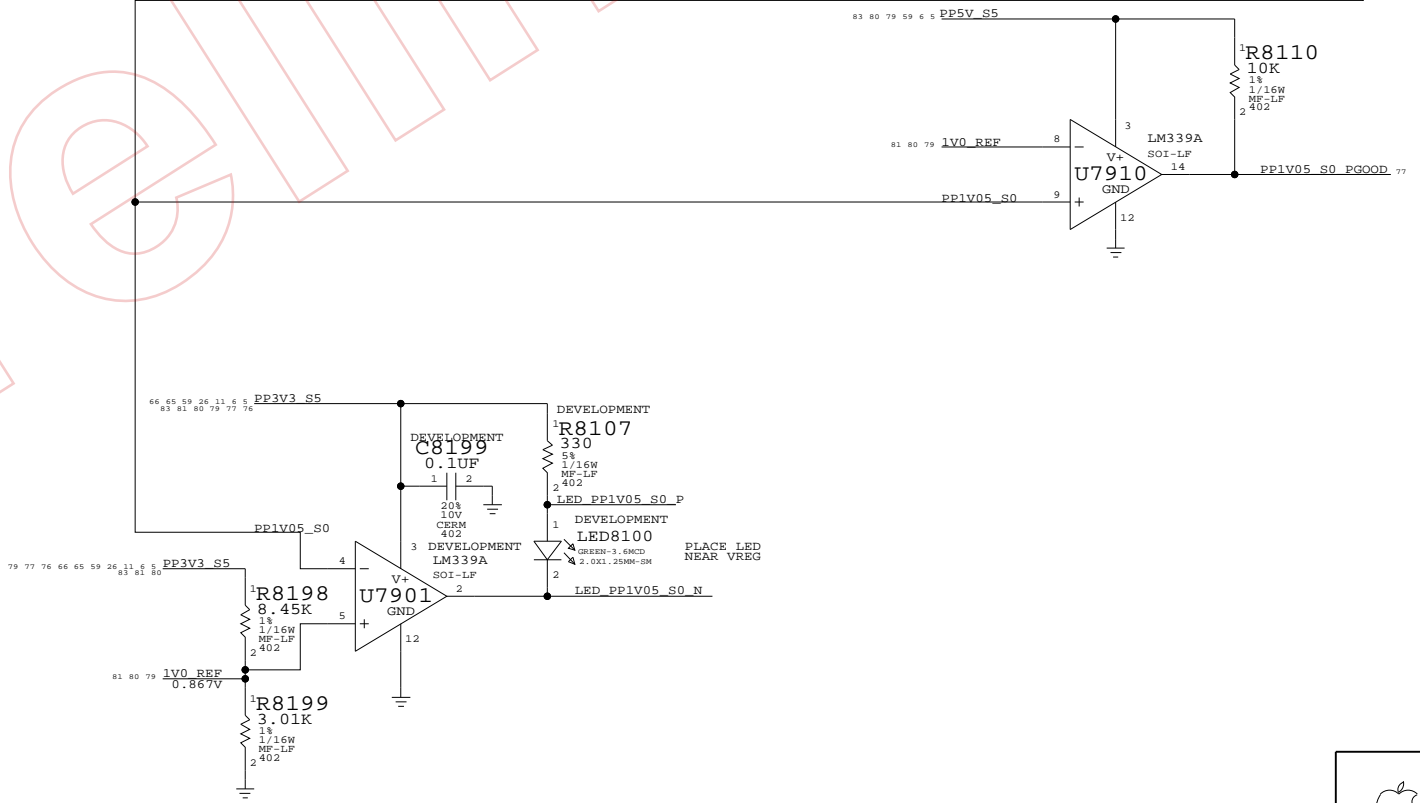
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	13
SCALE	SHT	80 OF	110
NONE			

# 1.05V S0 REGULATOR



$V_{OUT} = V_{REF} * (1 + R2/R1)$

$V_{REF} = 0.784V \text{ MIN}$   
 $0.800V \text{ TYP}$   
 $0.816V \text{ MAX}$



**1.05V VREG**

SYNC\_MASTER=M38-RT SYNC\_DATE=05/18/2005

**NOTICE OF PROPRIETARY PROPERTY**

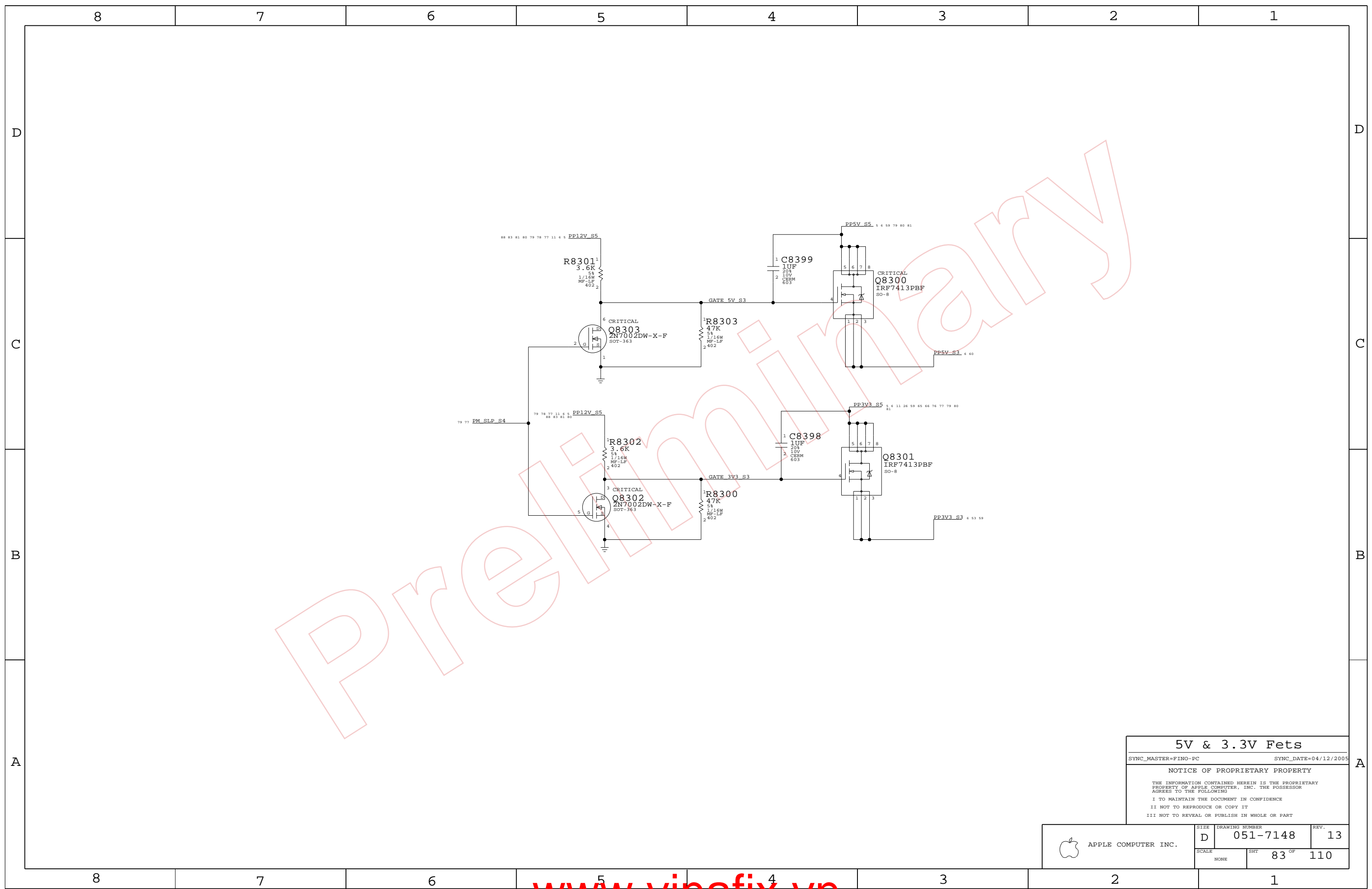
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	13
SCALE	SHT	81 OF	110
NONE			



5V & 3.3V Fets

SYNC\_MASTER=FINO-PC SYNC\_DATE=04/12/2005

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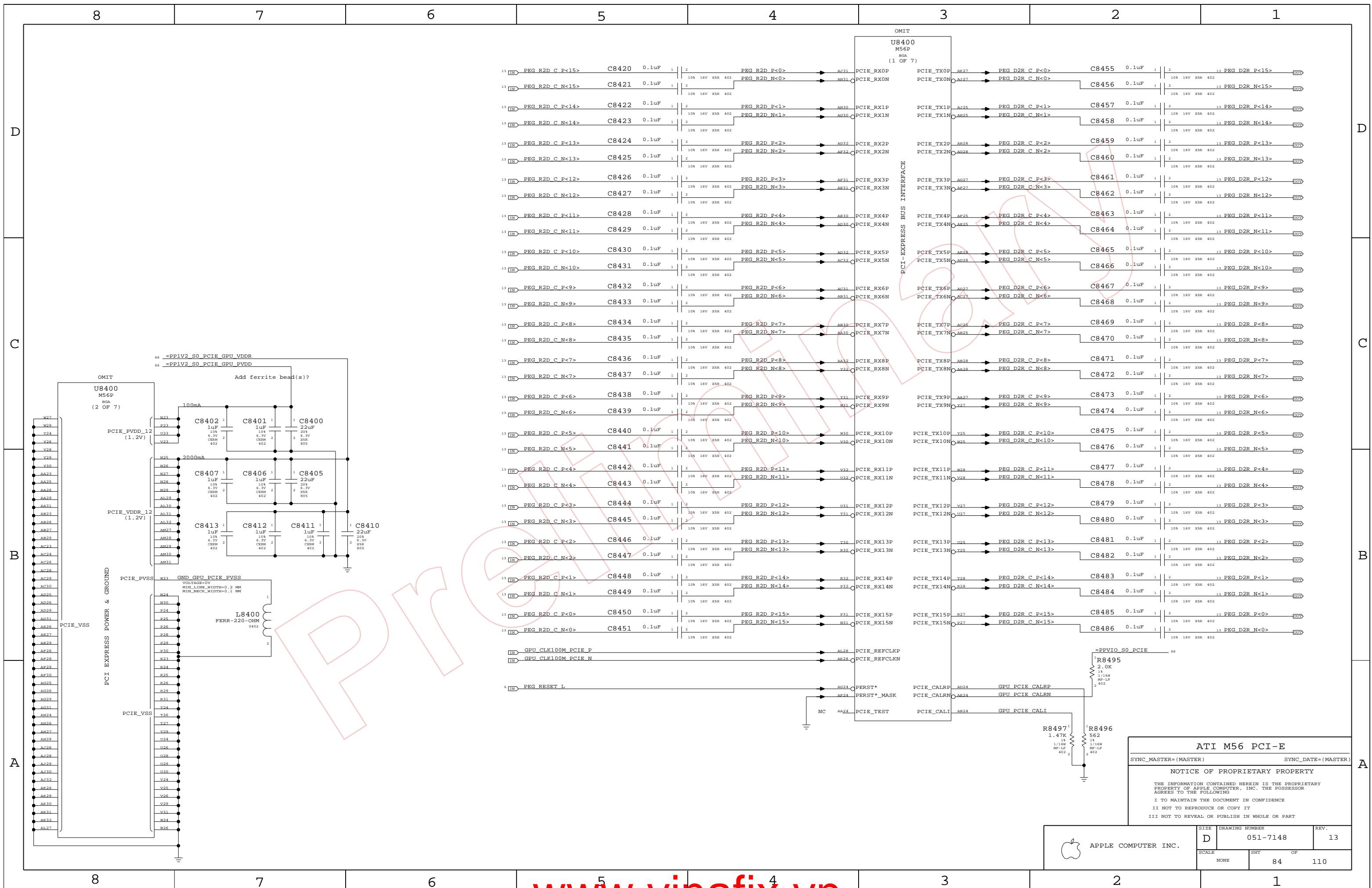
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	13
SCALE	SHT	83 OF	110
NONE			





**ATI M56 PCI-E**

SYNC\_MASTER=(MASTER)      SYNC\_DATE=(MASTER)

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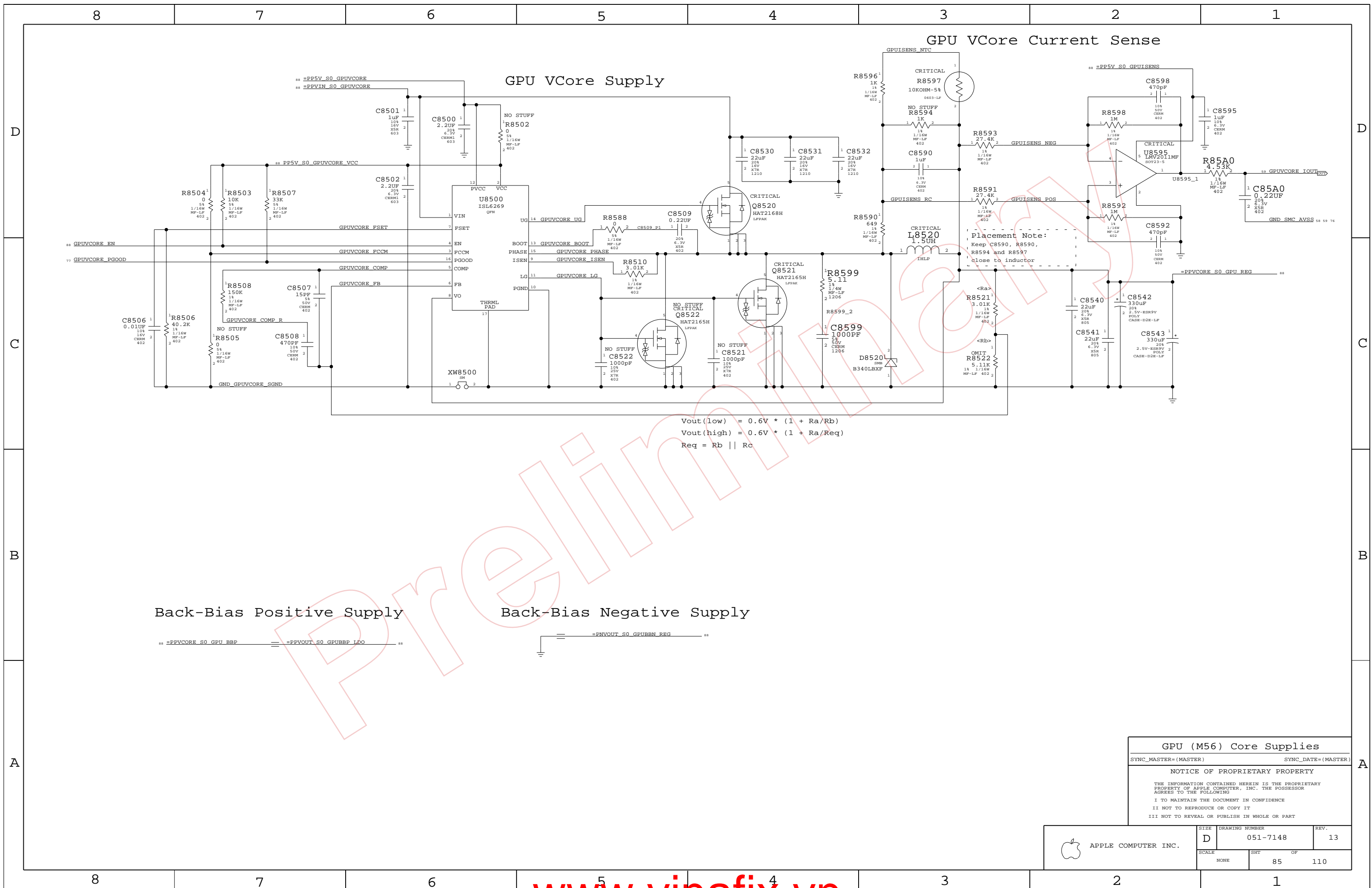
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 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	13
SCALE	SHT	OF	
NONE	84	110	



**GPU (M56) Core Supplies**

SYNC\_MASTER=(MASTER)      SYNC\_DATE=(MASTER)

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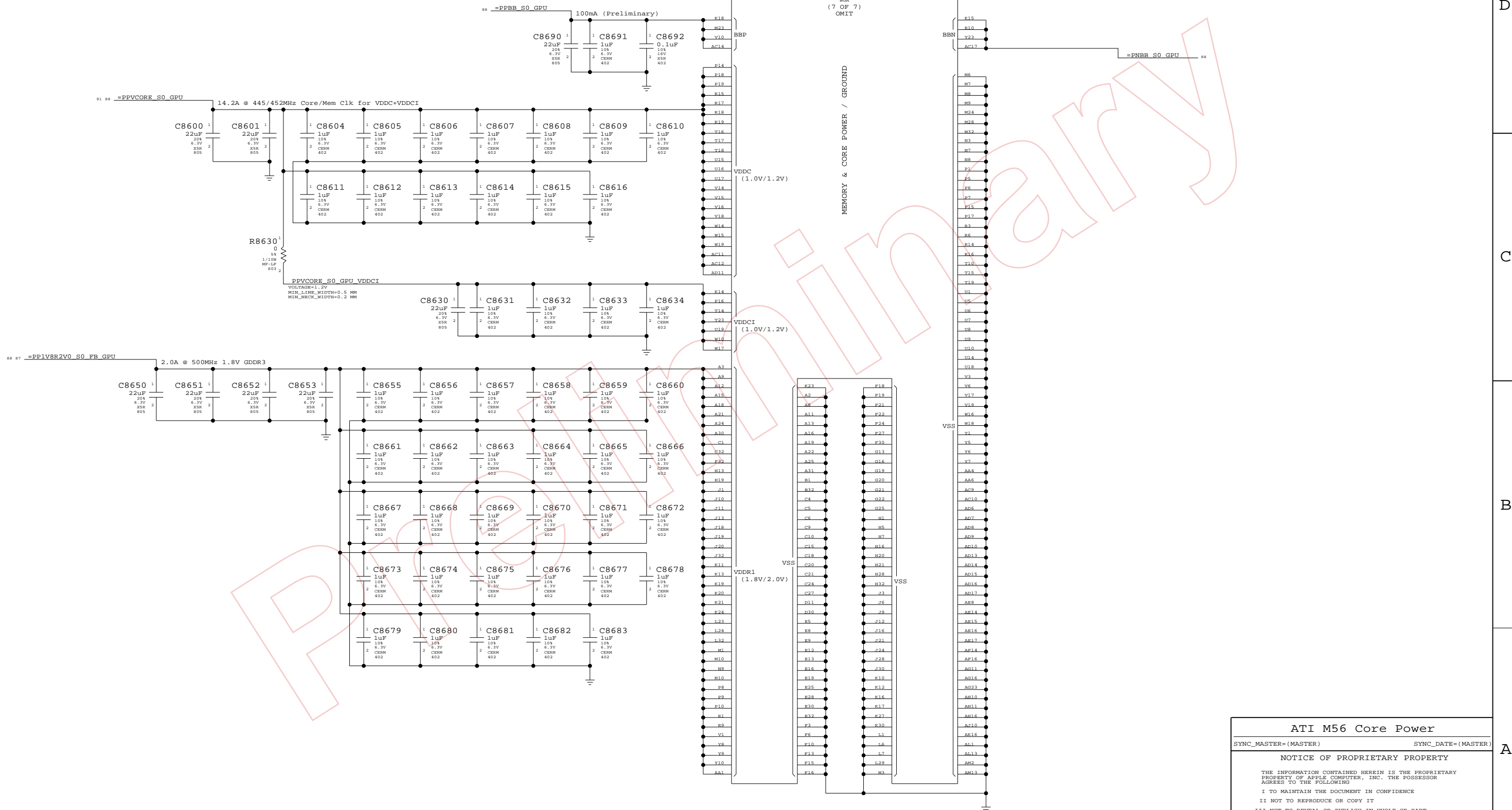
APPLE COMPUTER INC.	SIZE <b>D</b>	DRAWING NUMBER 051-7148	REV. 13
	SCALE NONE	SHEET OF 85 OF 110	

Page Notes

Power aliases required by this page:  
 - =PP1V5\_GPU\_VDD15  
 - =PP1VR1V3\_GPU\_VCORE

Signal aliases required by this page:  
 (NONE)

BOM options provided by this page:  
 (NONE)



ATI M56 Core Power

SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)

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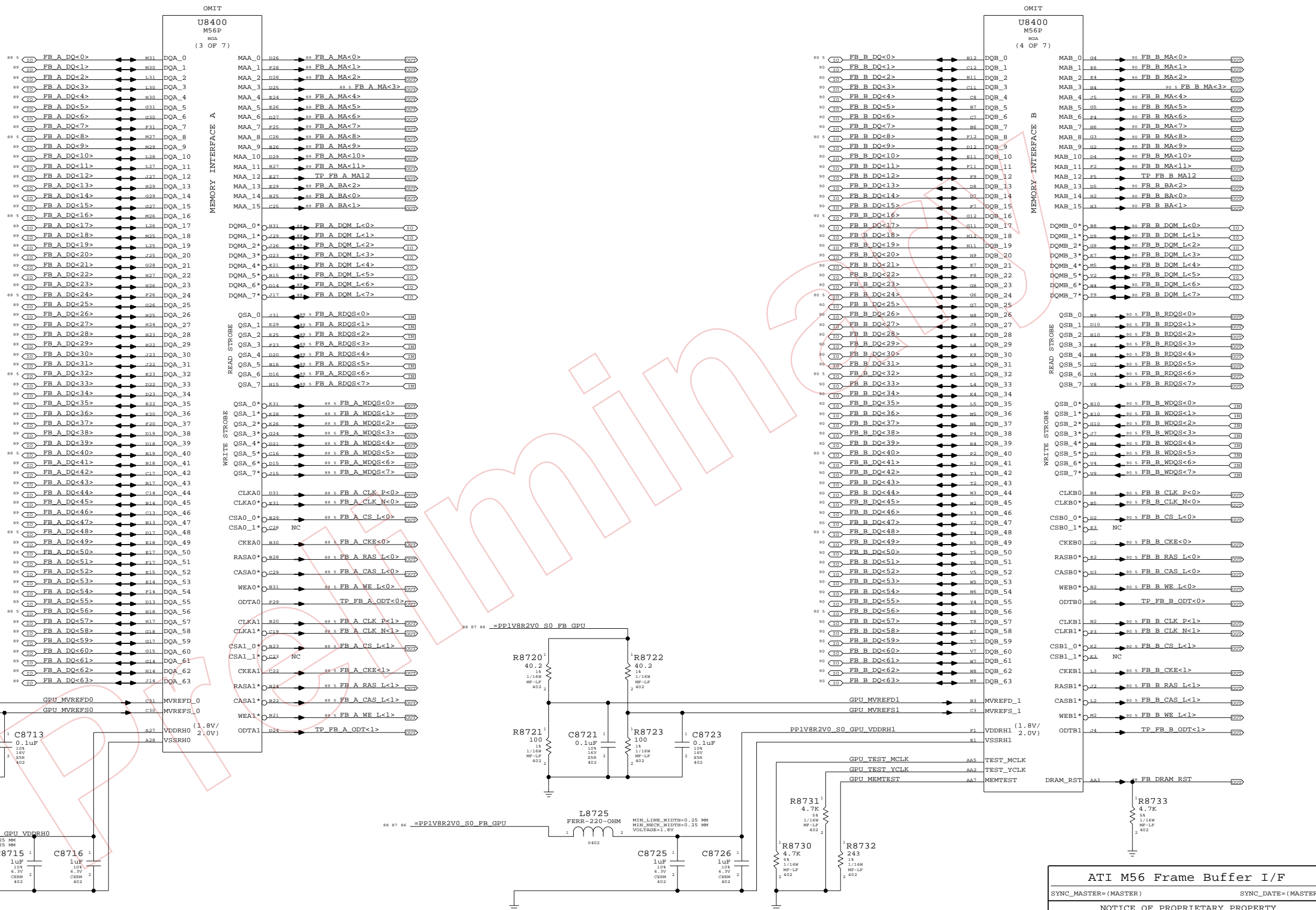
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	13
SCALE	SHT	OF	
NONE	86	110	

Page Notes

Power aliases required by this page:
- =PP1V8R2V0\_S0\_FB\_GPU
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
(NONE)



ATI M56 Frame Buffer I/F
SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)
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Table with columns: SIZE, DRAWING NUMBER, REV., SCALE, SHEET, OF, PART NUMBER. Values include: SIZE D, DRAWING NUMBER 051-7148, REV. 13, SCALE NONE, SHEET 87 OF 110.

8

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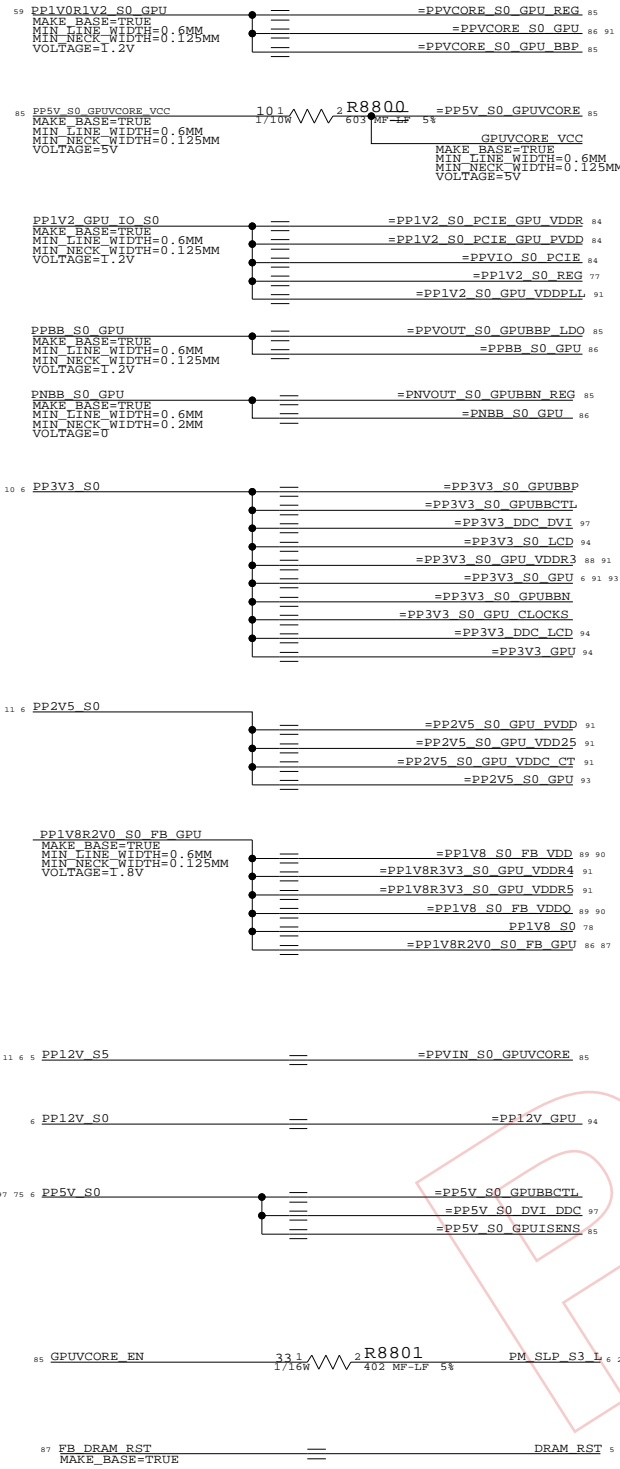
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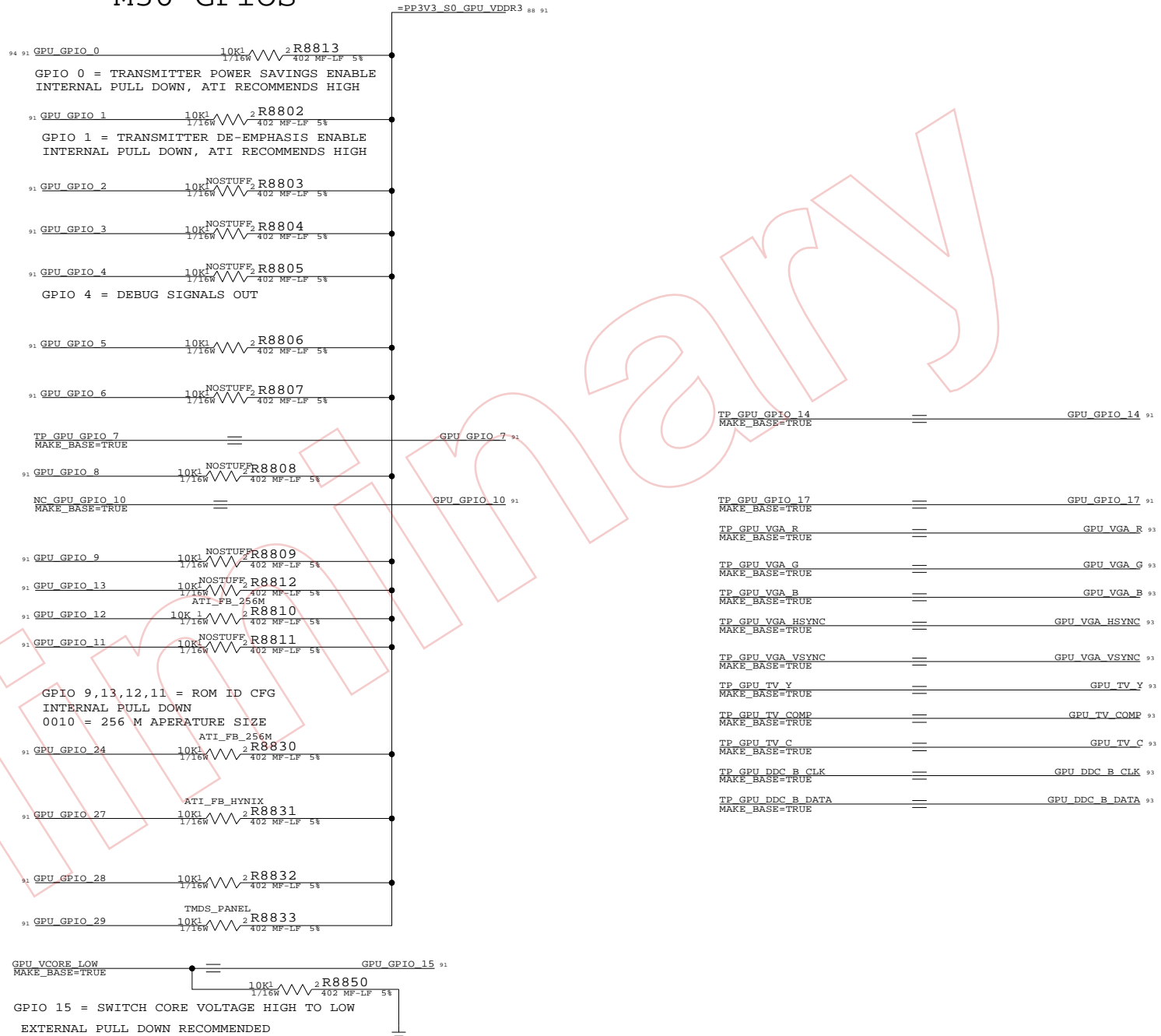
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### "S0" GPU RAILS

ONLY ON IN RUN



### M56 GPIOs

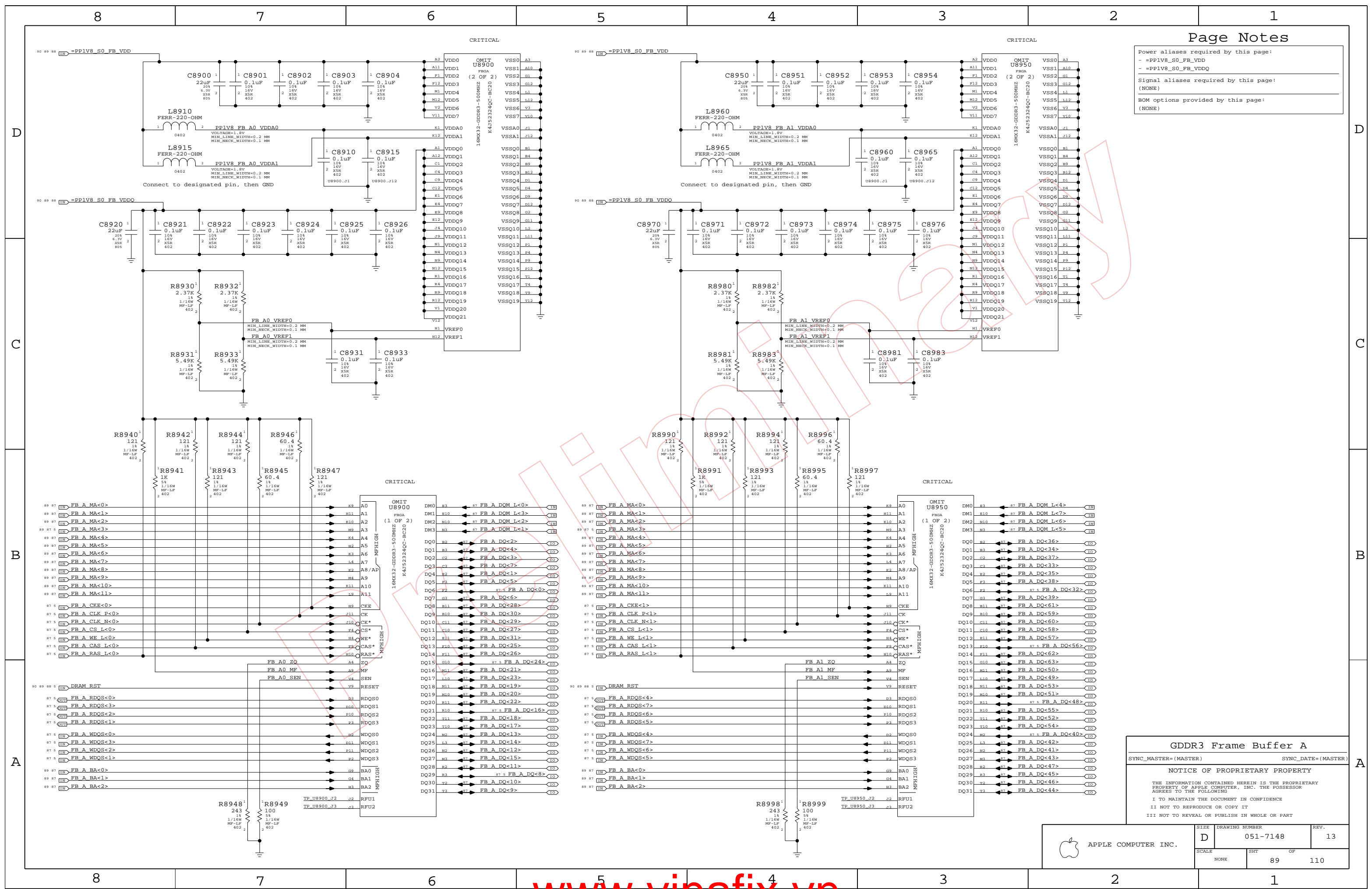


### GPU MISC

Power aliases required by this page:  
 - =PPIV8\_S0\_FB\_VDD  
 - =PPIV8\_S0\_FB\_VDDQ

Signal aliases required by this page:  
 (NONE)

BOM options provided by this page:  
 (NONE)



**GDDR3 Frame Buffer A**

SYNC\_MASTER=(MASTER)      SYNC\_DATE=(MASTER)

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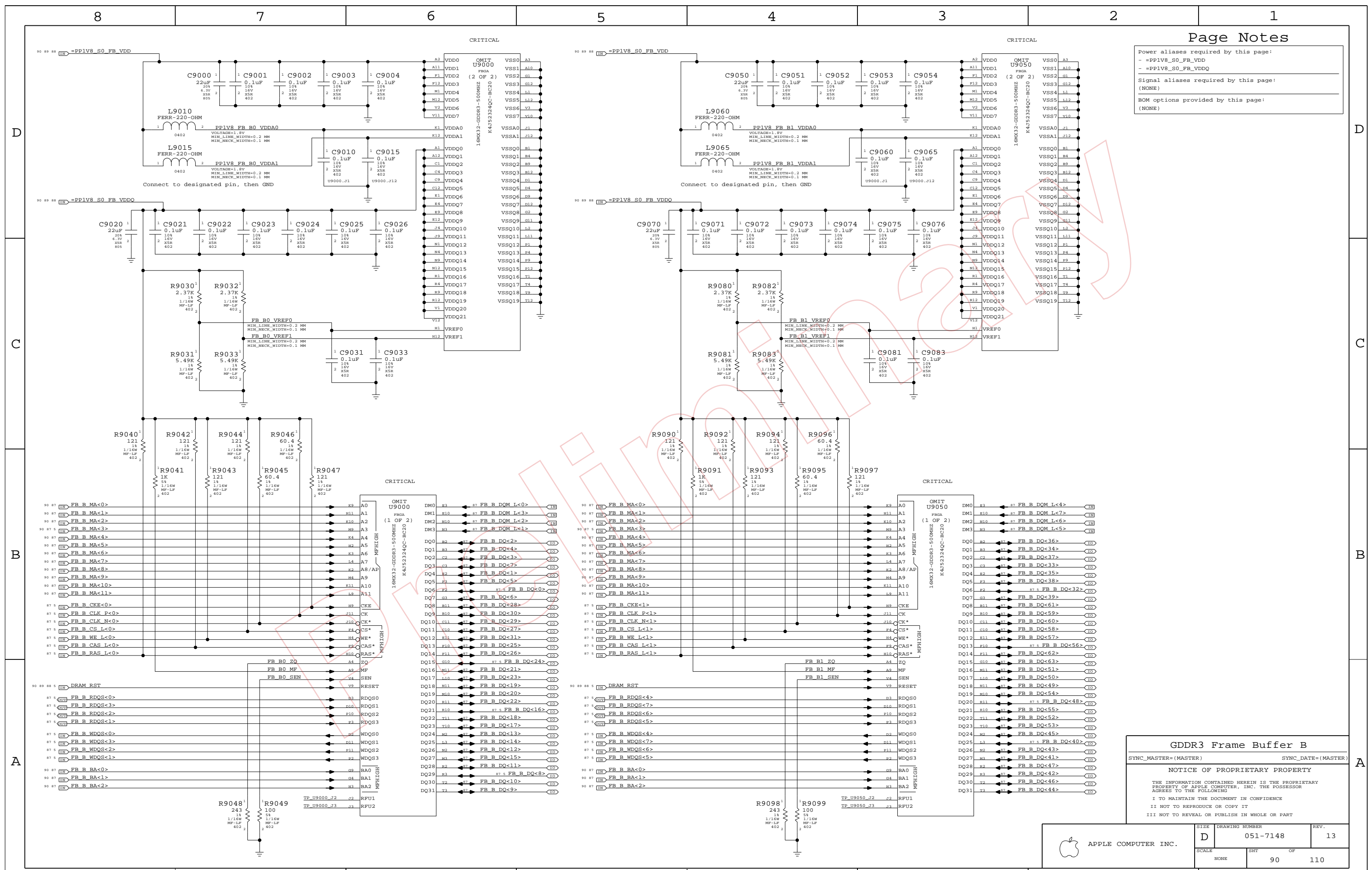
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	13
SCALE	SHT	OF	
NONE	89	110	

Power aliases required by this page:  
 - =PPIV8\_S0\_FB\_VDD  
 - =PPIV8\_S0\_FB\_VDDQ

Signal aliases required by this page:  
 (NONE)

BOM options provided by this page:  
 (NONE)



**GDDR3 Frame Buffer B**

SYNC\_MASTER=(MASTER)      SYNC\_DATE=(MASTER)

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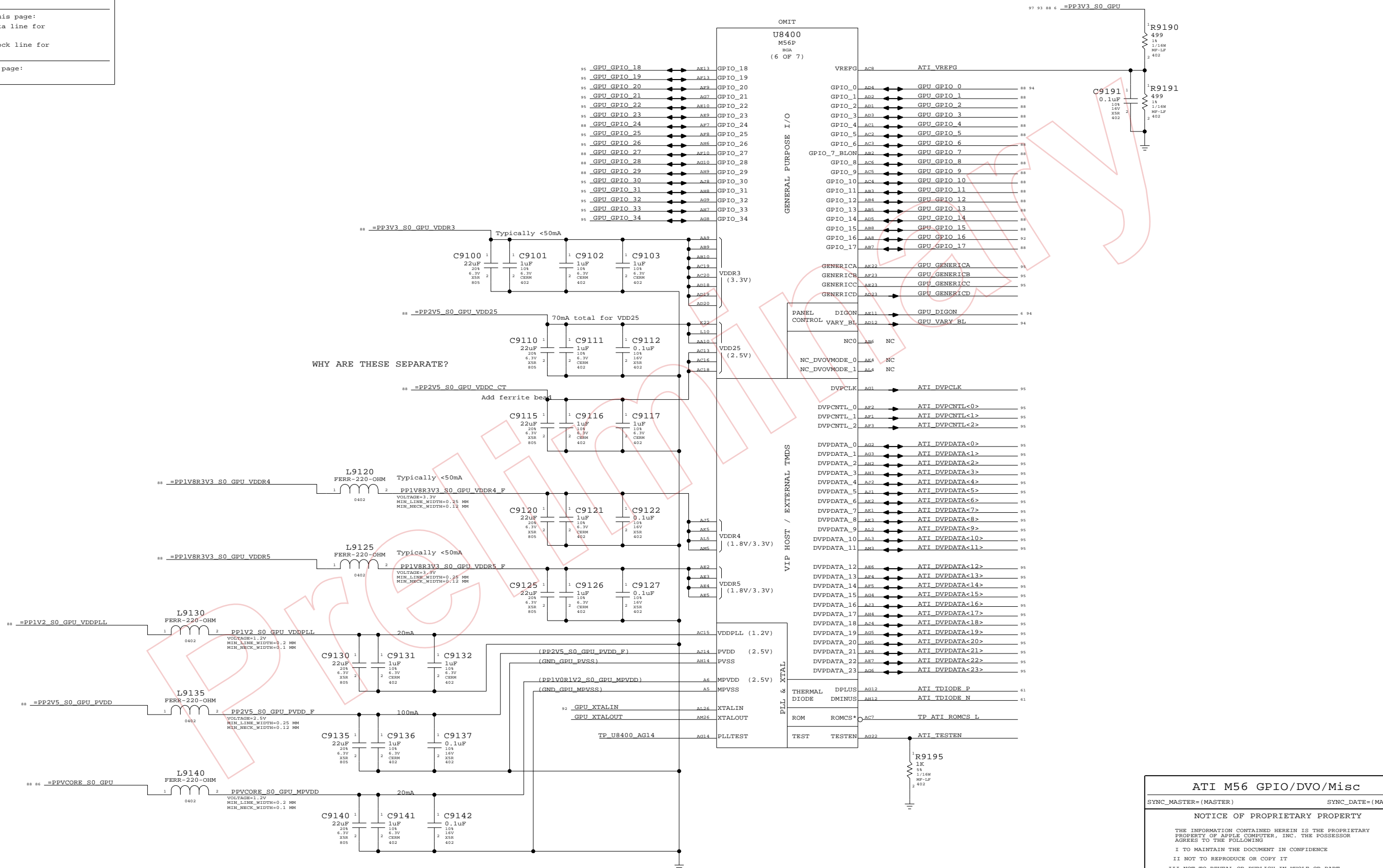
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### Page Notes

Power aliases required by this page:  
- =PP3V3\_GPU\_GPIOS  
- =PP2V5\_PVDD  
- =PP1V8\_GPU\_LVDS\_PLL

Signal aliases required by this page:  
- =I2C\_GPU\_TMDS\_SDA - I2C data line for external TMDS transmitters  
- =I2C\_GPU\_TMDS\_SCL - I2C clock line for external TMDS transmitters

BOM options provided by this page:  
(NONE)



**ATI M56P GPIO/DVO/Misc**

SYNC\_MASTER=(MASTER)      SYNC\_DATE=(MASTER)

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	13
SCALE	SHT	OF	
NONE	91	110	



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### Page Notes

Power aliases required by this page:

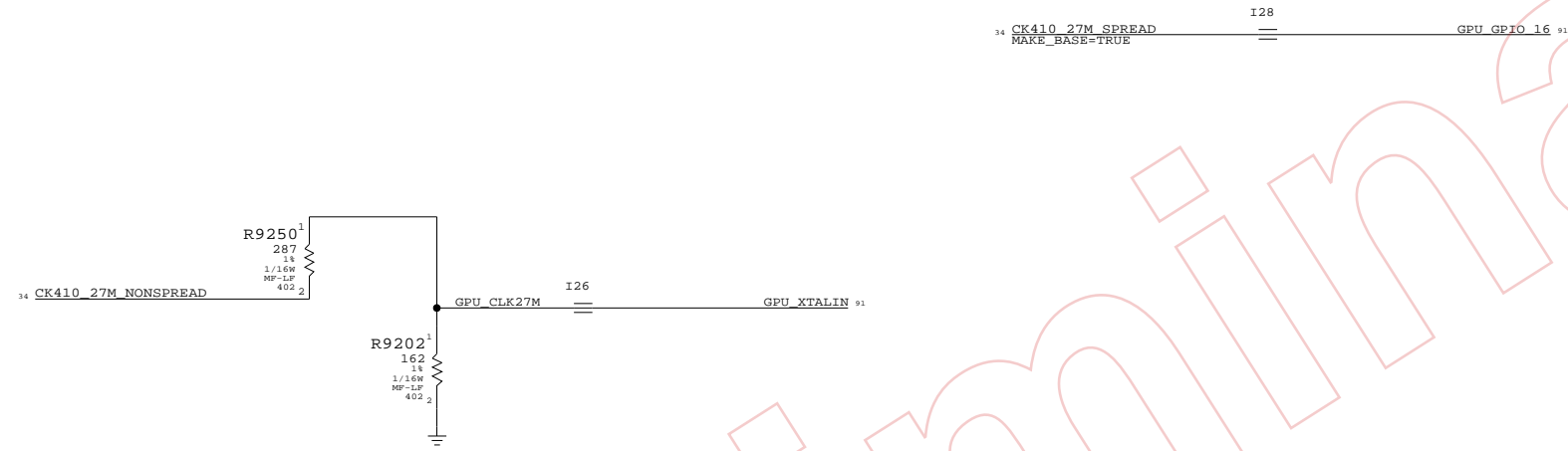
- =PP3V3\_GPU\_CLOCKS      - =PP3V3\_GPU\_PWRSEQ
- =PPVIN\_GPU\_LVDDR\_LDO    - =PP2V5\_GPU\_PWRSEQ
- =PP2V5\_GPU\_LVDDR\_LDO    - =PP1V8\_GPU\_PWRSEQ
- =PP1V5\_GPU\_PWRSEQ

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

- GPU\_SS                      - GPU\_LVDDR\_2V8



Preliminary


### GPU CLOCKS

SYNC\_MASTER=BOZEMAN      SYNC\_DATE=05/21/2005

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	D	051-7148	13
SCALE	SHT	OF	
NONE	92	110	

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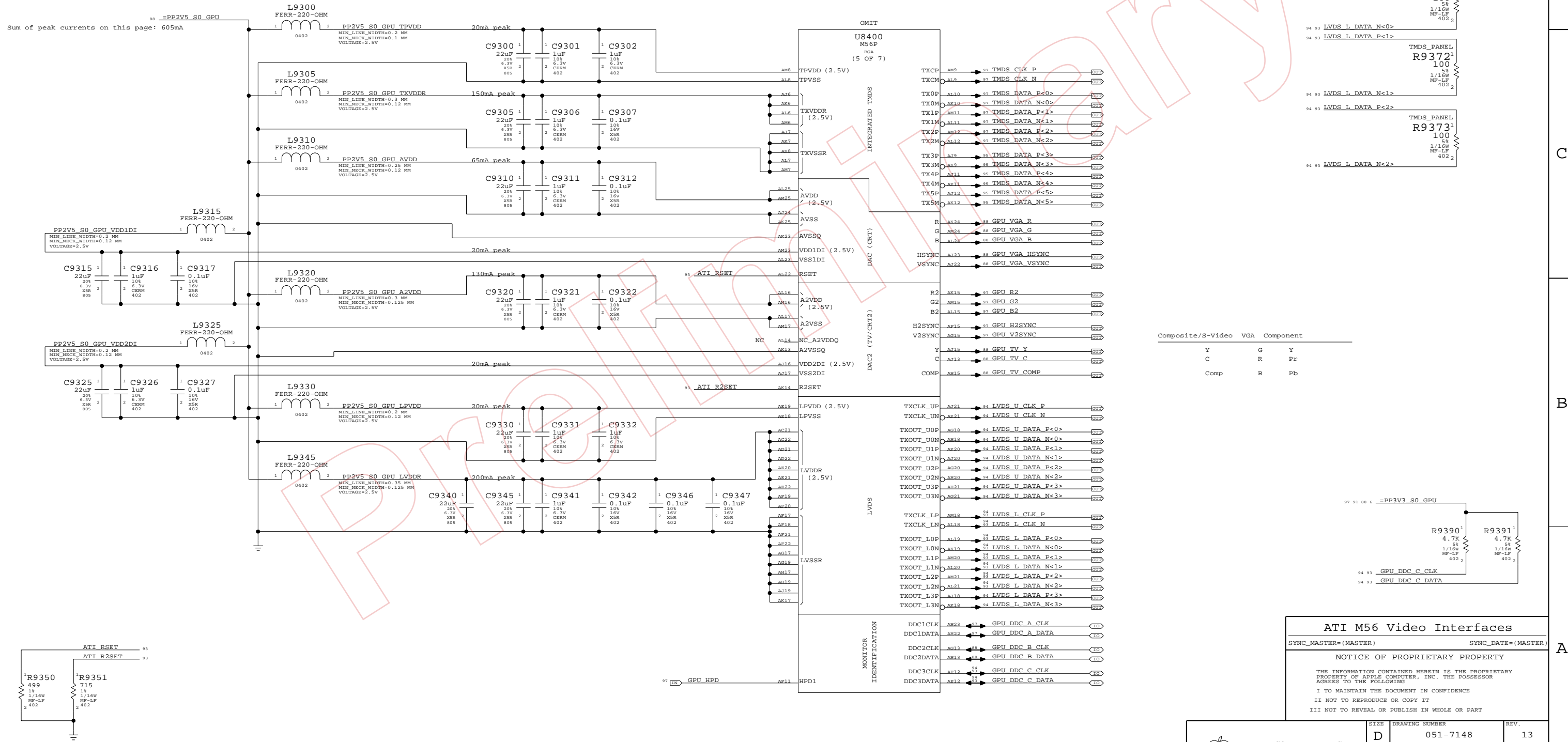
Page Notes

Power aliases required by this page:  
 - =PP2V5\_S0\_GPU  
 - =PP1V8R2V5\_S0\_GPU\_LVDDR

Signal aliases required by this page:  
 (NONE)

BOM options provided by this page:  
 (NONE)

TERMINATION FOR TMDS USAGE OF LVDS PINS  
 PLACE CLOSE TO GPU (U8400)



**ATI M56 Video Interfaces**

SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)

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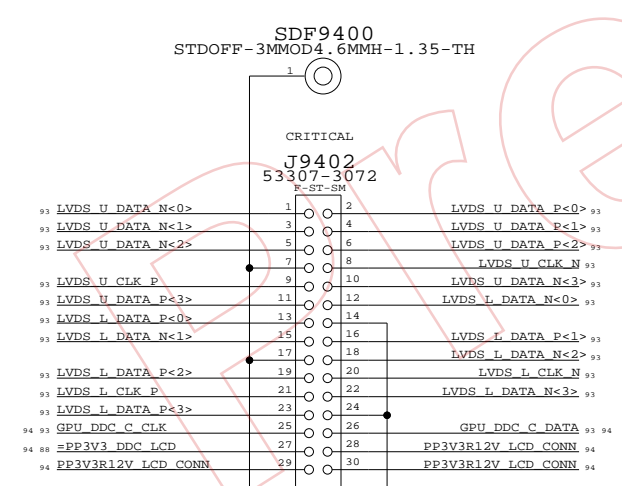
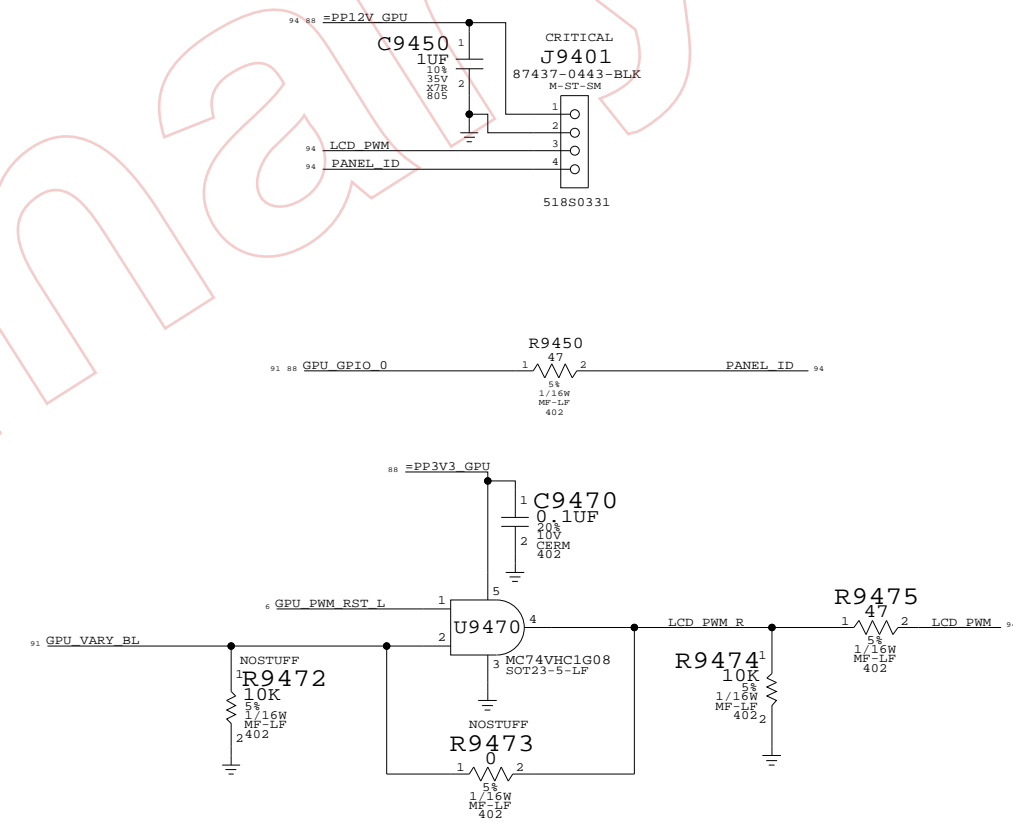
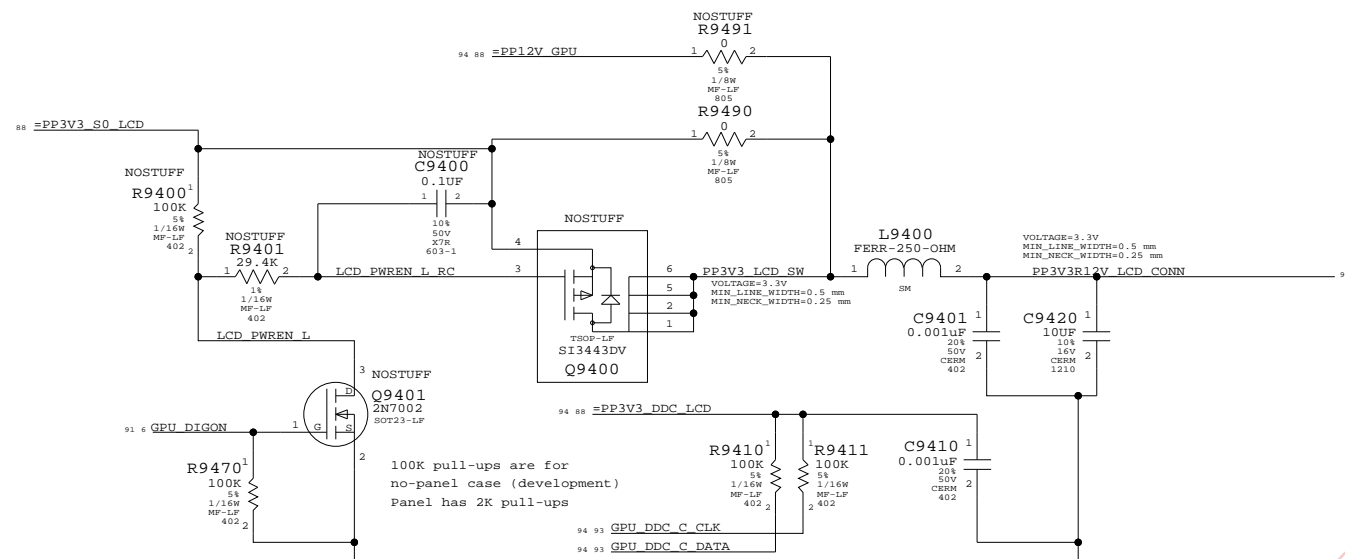
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	13
SCALE	SHT	OF	
NONE	93	110	

# LCD (LVDS) INTERFACE

# INVERTER INTERFACE



GATE TO PREVENT LEAKAGE ONTO PWM  
MIGHT BE ABLE TO BYPASS IF SMC DRIVES SIGNAL

**Internal Display Conns**  
 SYNC\_MASTER=BOZEMAN SYNC\_DATE=04/27/2005  
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	D	051-7148	13
SCALE	SHT	OF	
NONE	94	110	

8

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TP_GPU_GENERICC == GPU_GENERICC 91
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C

C

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### M56 TPS


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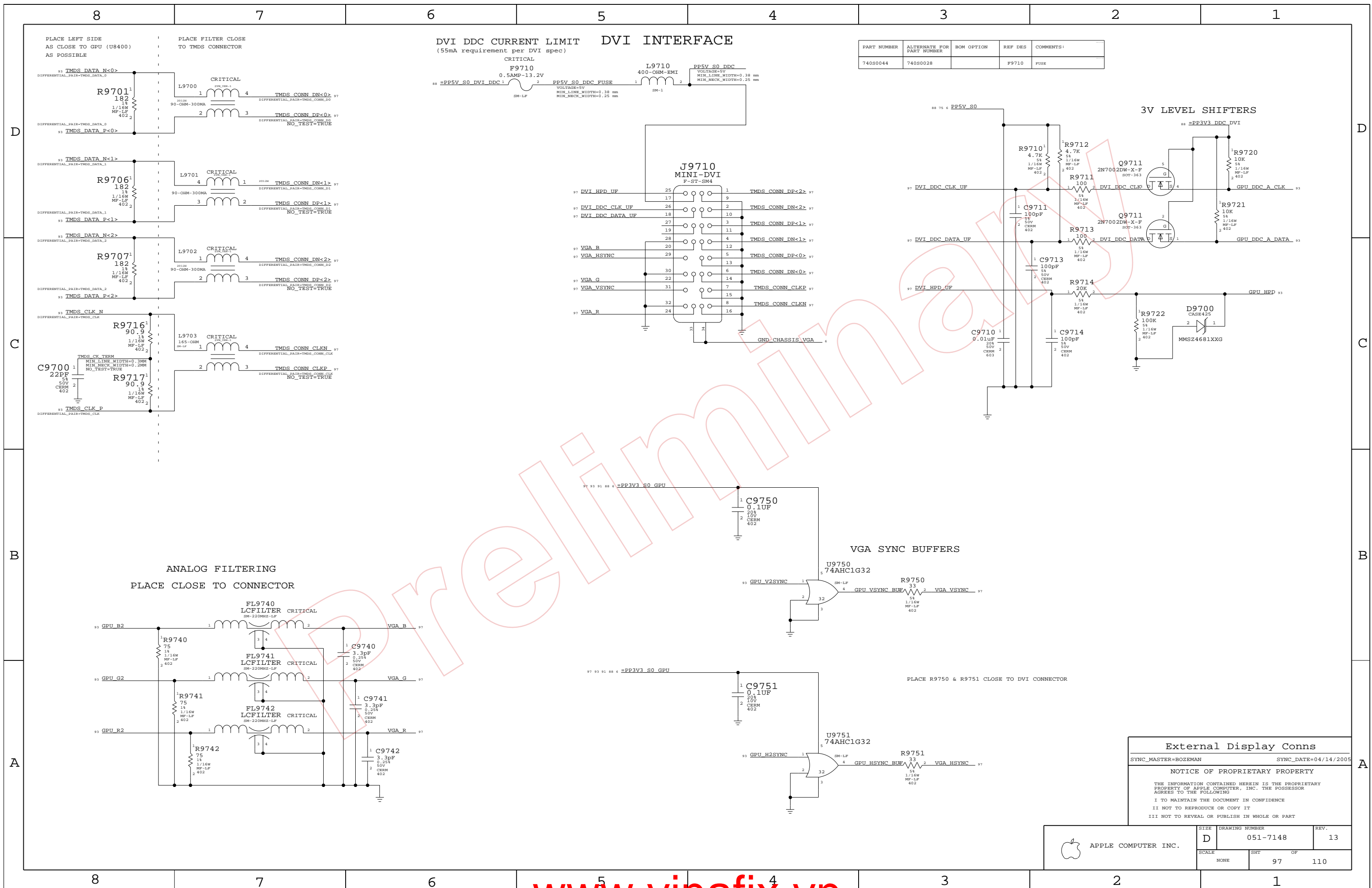
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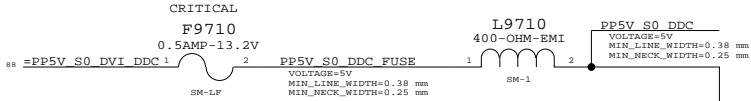
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SCALE	SHT	OF	
NONE	95	110	

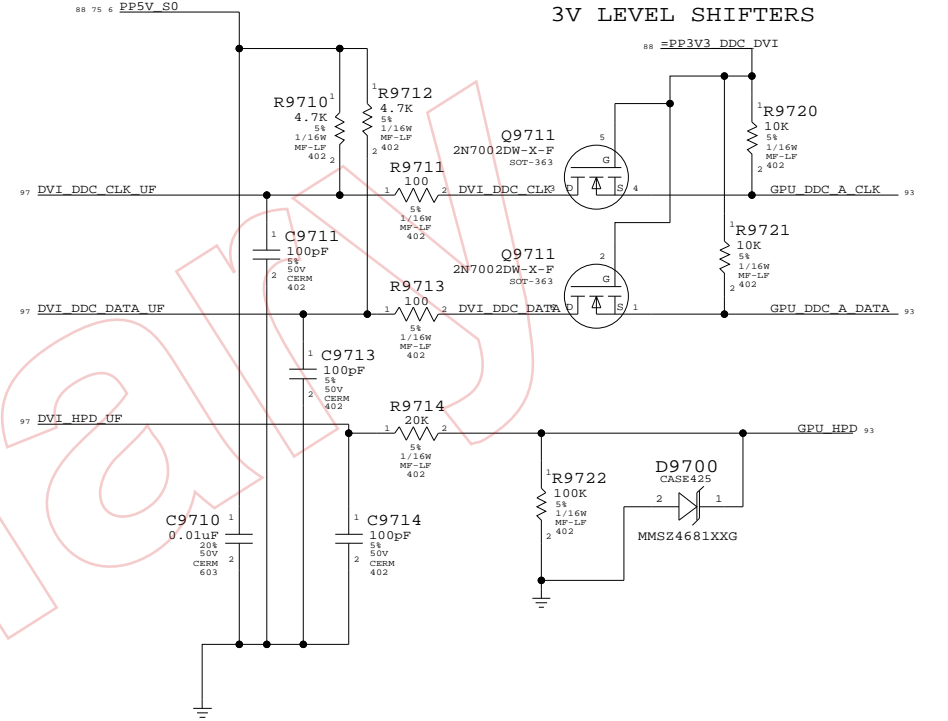


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
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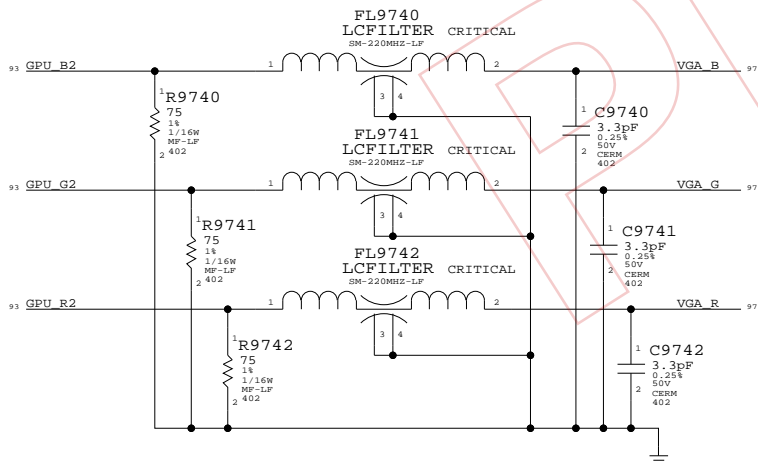
**DVI DDC CURRENT LIMIT DVI INTERFACE**  
(55mA requirement per DVI spec)



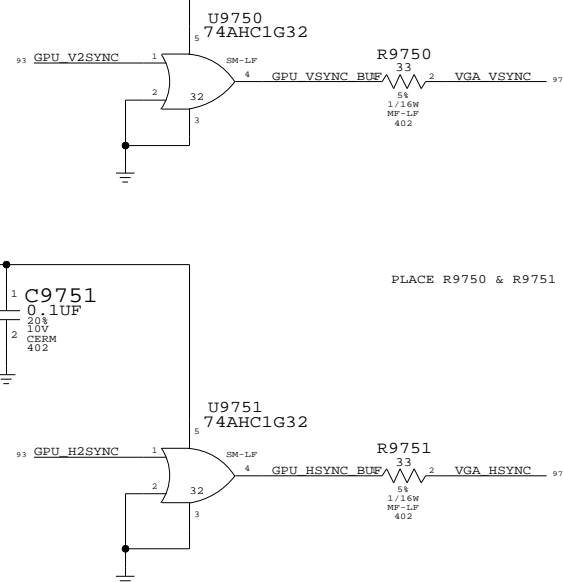
**3V LEVEL SHIFTERS**



**ANALOG FILTERING**  
PLACE CLOSE TO CONNECTOR



**VGA SYNC BUFFERS**



**External Display Conns**

SYNC\_MASTER=BOZEMAN SYNC\_DATE=04/14/2005

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SCALE	SHT	OF	
NONE	97	110	



8	7	6	5	4	3	2	1
D							D
C							C
B							B
A							A
8	7	6	5	4	3	2	1

Table with columns numbered 8 to 1. Each column contains lists of hardware components and their associated IDs. The table is organized into four main sections: A (rows 1-12), B (rows 13-24), C (rows 25-36), and D (rows 37-48). The components include various peripherals, memory, and internal chips like the M38A series. The IDs are numerical strings of varying lengths.





Main table containing columns 1-8 and rows A-D. Each cell contains a list of hardware components and their corresponding part numbers.



8			7			6			5			4			3			2			1		
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C8436 CAP_402 m38a[84C5]	C9345 CAP_805 m38a[93A6]	C9346 CAP_402 m38a[93A5]					





