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- 1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
- 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
- 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

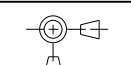
IMAC 5,2 -- REV D

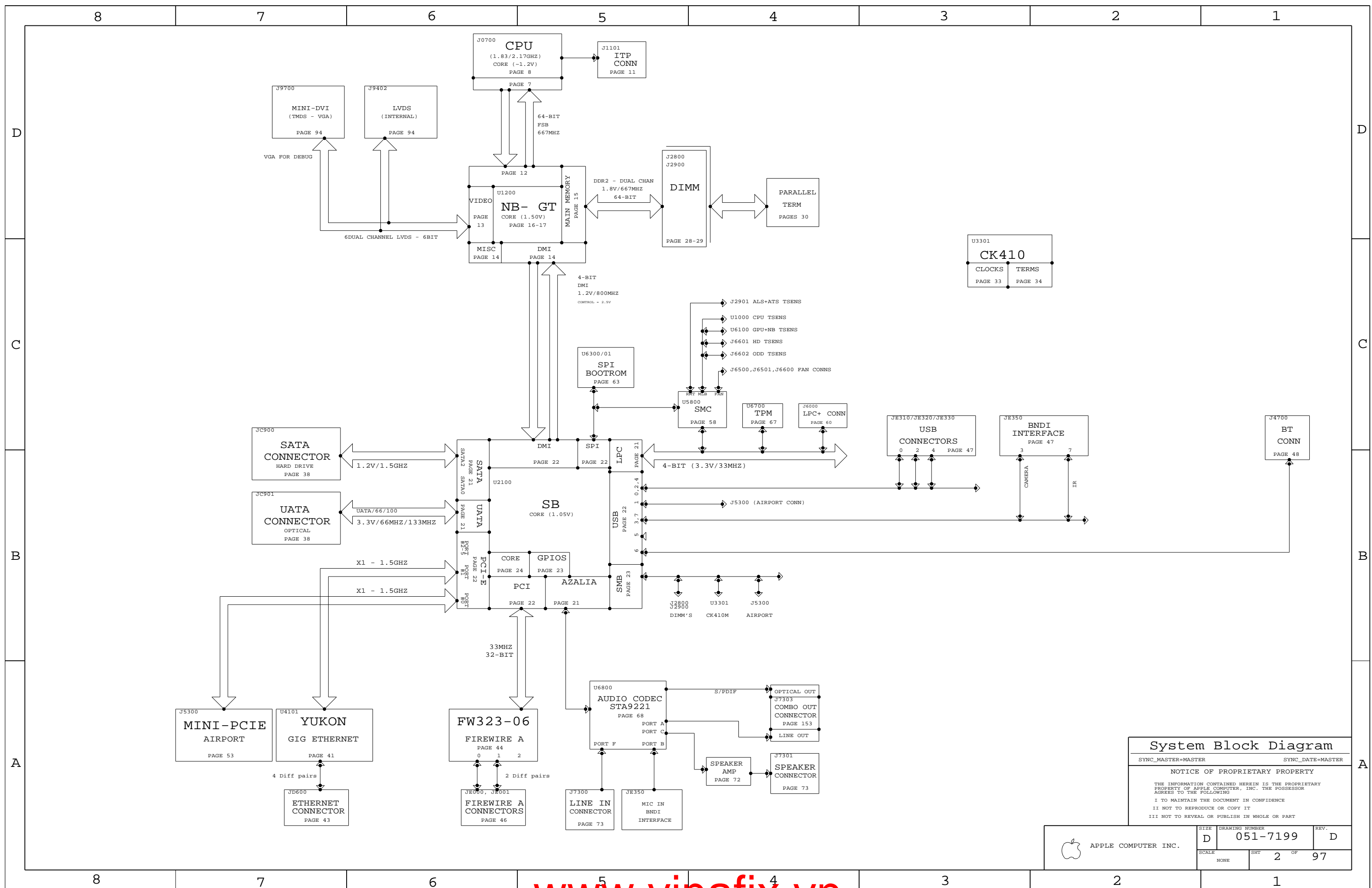
10/6/06

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD	ENG APPD
D		466215	PRODUCTION RELEASED	10/09/06	06/22/04

PDF	CSA	CONTENTS	SYNC	MASTER	DATE
2	2	System Block Diagram	MASTER	MASTER	
3	3	Power Block Diagram	MASTER	MASTER	
4	4	Table Items	MASTER	MASTER	
5	5	FUNC TEST 1 OF 2	MASTER	MASTER	
6	6	Power Conn / Alias	MASTER	MASTER	
7	7	CPU 1 OF 2-FSB	MASTER	MASTER	
8	8	CPU 2 OF 2-PWR/GND	MASTER	MASTER	
9	9	CPU DECAPS & VID<>	MASTER	MASTER	
10	10	CPU TEMP SENSOR	MASTER	MASTER	
11	11	CPU ITP700FLEX DEBUG	M38	01/05/2006	
12	12	NB CPU Interface	M1	01/05/2006	
13	13	NB PEG / Video Interfaces	M1	01/05/2006	
14	14	NB Misc Interfaces	MASTER	MASTER	
15	15	NB DDR2 Interfaces	M1	01/05/2006	
16	16	NB Power 1	MASTER	MASTER	
17	17	NB Power 2	M40	01/05/2006	
18	18	NB Grounds	M1	01/05/2006	
19	19	NB (GM) Decoupling	(MASTER)	(MASTER)	
20	20	NB Config Straps	M1	01/05/2006	
21	21	SB: 1 OF 4	M38	01/05/2006	
22	22	SB: 2 OF 4	MASTER	MASTER	
23	23	SB: 3 OF 4	MASTER	MASTER	
24	24	SB: 4 OF 4	M38	01/05/2006	
25	25	SB: DECOUPLING	MASTER	MASTER	
26	26	SB: MISC	MASTER	MASTER	
27	27	SB: SMB HUB AND ALIAS	MASTER	MASTER	
28	28	DDR2 SO-DIMM Connector A	MASTER	MASTER	
29	29	DDR2 SO-DIMM Connector B	MASTER	MASTER	
30	30	Memory Active Termination	MASTER	MASTER	
31	31	Memory Vtt Supply	MASTER	MASTER	
32	33	CLOCKS	MASTER	MASTER	
33	34	CLOCKS: TERMINATIONS	MASTER	MASTER	
34	38	Disk Connectors	MASTER	MASTER	
35	41	ETHERNET CONTROLLER	MASTER	MASTER	
36	42	ETHERNET MISC	MASTER	MASTER	
37	43	ETHERNET CONNECTOR	MASTER	MASTER	

PDF	CSA	CONTENTS	SYNC	MASTER	DATE
38	44	FW: FW323-06	MASTER	MASTER	
39	45	FW: DECAPS	MASTER	MASTER	
40	46	FIREWIRE CONNECTORS	MASTER	MASTER	
41	47	USB Device Interfaces	MASTER	MASTER	
42	53	AIRPORT CONN	MASTER	MASTER	
43	54	PCIE PORT ALIASES	MASTER	MASTER	
44	58	SMC	M1	01/05/2006	
45	59	SMC & TPM SUPPORT	(MASTER)	(MASTER)	
46	60	LPC+ CONN	M38	12/09/2005	
47	61	NB THERMAL	MASTER	MASTER	
48	63	SPI BOOTROM	M38	01/05/2006	
49	65	Fan 0, 1 & System Temp	MASTER	MASTER	
50	66	Fan 2 & HD Temp	MASTER	MASTER	
51	67	TPM	M38	01/05/2006	
52	68	AUDIO: CODEC	AUDIO	05/12/2006	
53	72	AUDIO: SPEAKER AMP	AUDIO	05/12/2006	
54	73	AUDIO: CONNECTORS	AUDIO	05/12/2006	
55	74	AUDIO: POWER SUPPLIES	AUDIO	05/12/2006	
56	75	IMVP6 CPU VCore Regulator	MASTER	MASTER	
57	76	CPU & SYSTEM SENSE CIRCUI	(MASTER)	(MASTER)	
58	77	PWR GOOD	(MASTER)	(MASTER)	
59	78	3V DC/DC 2.5V	(MASTER)	(MASTER)	
60	79	1.8V & 1.2V VREG	MASTER	MASTER	
61	80	1.5V_S0 & 1.05V_S0 VREG	MASTER	MASTER	
62	82	5V DC/DC	MASTER	MASTER	
63	83	S0 AND S3 FETS	MASTER	MASTER	
64	94	Internal Display Conns	MASTER	MASTER	
65	95	EXTERNAL TMDS	MASTER	MASTER	
66	96	TMDS/Inverter/ExtVGA	MASTER	MASTER	
67	97	External Display Conns	MASTER	MASTER	

DIMENSIONS ARE IN MILLIMETERS		METRIC		Apple Computer Inc.	
XX :	_____	DRAPTER	/	DESIGN CK	/
X.XX :	_____	ENG APPD	/	MFG APPD	/
X.XXX :	_____	QA APPD	/	DESIGNER	/
ANGLES :	_____	RELEASE	/	SCALE	NONE
DO NOT SCALE DRAWING		MATERIAL/FINISH NOTED AS APPLICABLE		SIZE	D
 THIRD ANGLE PROJECTION		DRAWING NUMBER		051-7199	REV. D
SHT 1 OF 97					



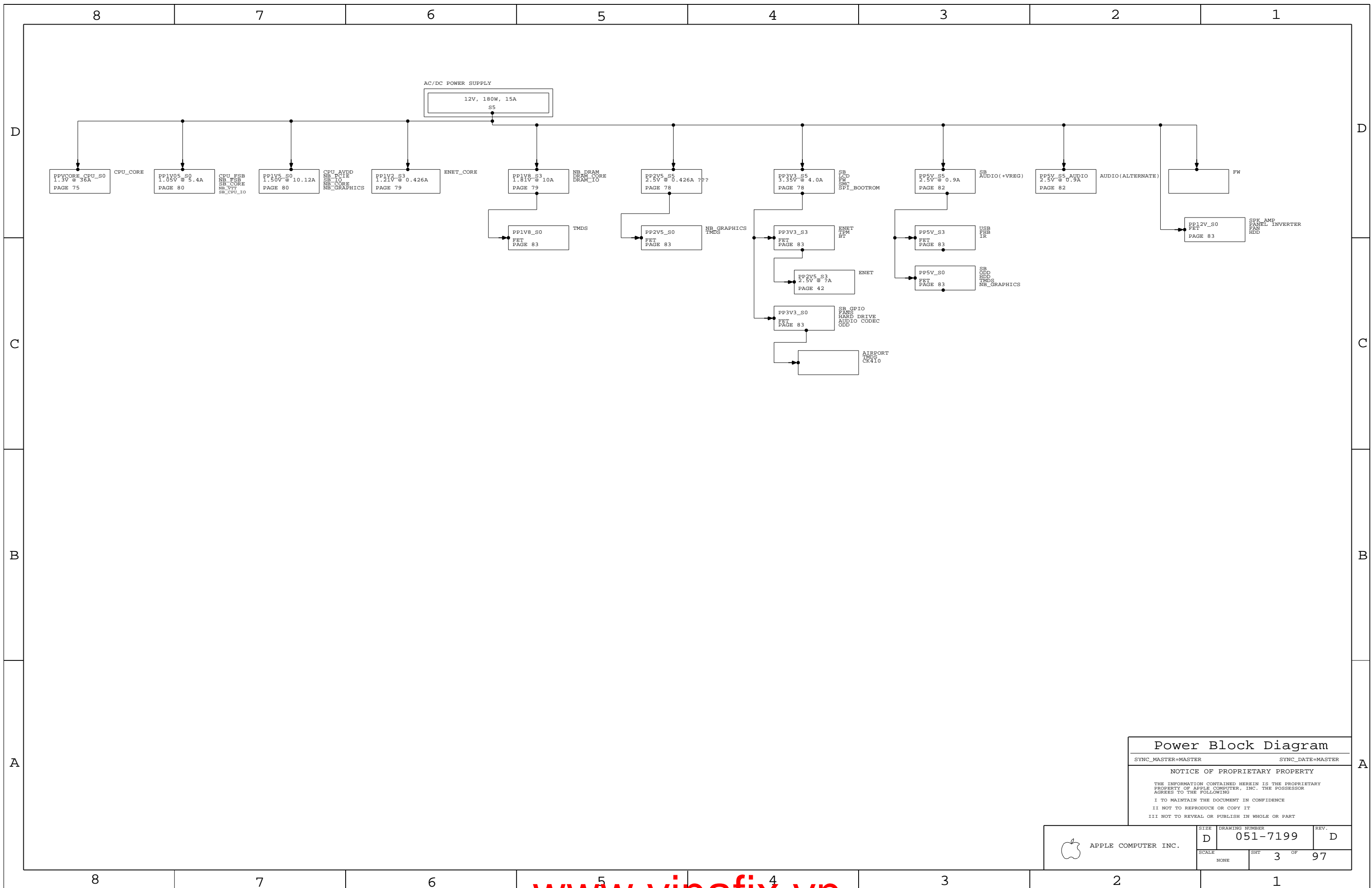
System Block Diagram

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	D
SCALE	SHT	OF	REV.
NONE	2	97	



Power Block Diagram

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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	D	051-7199	D
SCALE	SHT	OF	REV.
NONE	3	97	

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COMMON

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
511S0025	1	IC,CPU-SKT,479BGA	J0700	CRITICAL	
338S0298	1	IC,945GT,NORTHBRIDGE	U1200	CRITICAL	
343S0385	1	IC,SB,652BGA	U2100	CRITICAL	
742-0048	1	BAT,COIN,3V,220MAH,CR2032	BT2600	CRITICAL	
359S0101	1	IC,CY28445-5,CLK GEN,68PIN QFN	U3301	CRITICAL	
338S0270	1	IC,88E8053,1GIGABIT ENET XCVR,64P QFN,MD	U4101	CRITICAL	
(335S0382) 341S1797	1	IC,ENET LAN ROM	U4102	CRITICAL	
338S0279	1	IC,FW32306,1394A LINK,TQFP	U4400	CRITICAL	
338S0274 341T0022	1	IC,SMC,M50	U5800	CRITICAL	
341S1789	1	IC,TPM,TSSOP,28P	U6700	CRITICAL	TPM
353S1461	1	IC,CPU VREG,IMVP,TWO PHASE	U7500	CRITICAL	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-7199	1	PCB,SCHM,MLB,M50	SCH1		
820-1960	1	PCB,FAB,MLB,M50	MLB1		
(335S0384) 341T0042	1	EFI ROM,M50A	U6301	CRITICAL	
337S3386	1	M50 MEROM CPU	CPU	CRITICAL	MEROM

341S1859 IC EFI BOOTROM DEV M50
 337S3242 M38 CPU(C0)
 337S3280 M50 1.83G LOW SPEED CPU (D0)
 USE BOM OPTION MEROM FOR MEROM PROCESSOR

OPS REQUESTED QUAL PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
155S0295	1	CHOKE,COMMON_MODE,1650HM,4PIN	L9703	CRITICAL	
124-0359	3	PCAP,120UF,16V,20%,ELEC	C6505,C6504,C6602	CRITICAL	

ALTERNATE PARTS

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
126S0091	126S0092		C625	FACTORY SHORTAGE
353S1278	353S1381		U5940	SMC VREF
378S0141	378S0140		LX2601,LX2602,LX2603	
353S1465	353S1461		U7500	CPU VREG, OLD DIE,SCREENED PART
124-0338	124-0333		C7953,C7954	FOR SUPPLY
124-0361	124-0339		C7577,C7578,C7579,C7956,C7957	SANYO CAP
138S0598	138S0512		C624,C7201,C7203,C7232,C7811,C911,C8000,C8001,C8002,C8003,C8211,C9420	FOR SUPPLY
155S0321	155S0164		L9700,L9701,L9702	FOR SUPPLY

MECHANICAL PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
603-9187	1	SUBASSY, M50 NB HEATSINK	HS2	CRITICAL	
603-9186	1	SUBASSY, M50 CPU HEATSINK	HS1	CRITICAL	
725-0668	1	MYLAR WASHER	WASH1	CRITICAL	
725-0720	1	MYLAR BLACK LED CVR, M50	CVR1	CRITICAL	
825-6447	1	BARCODE LABEL, M50A	[EEE:WZE]	CRITICAL	MEROM

Table Items

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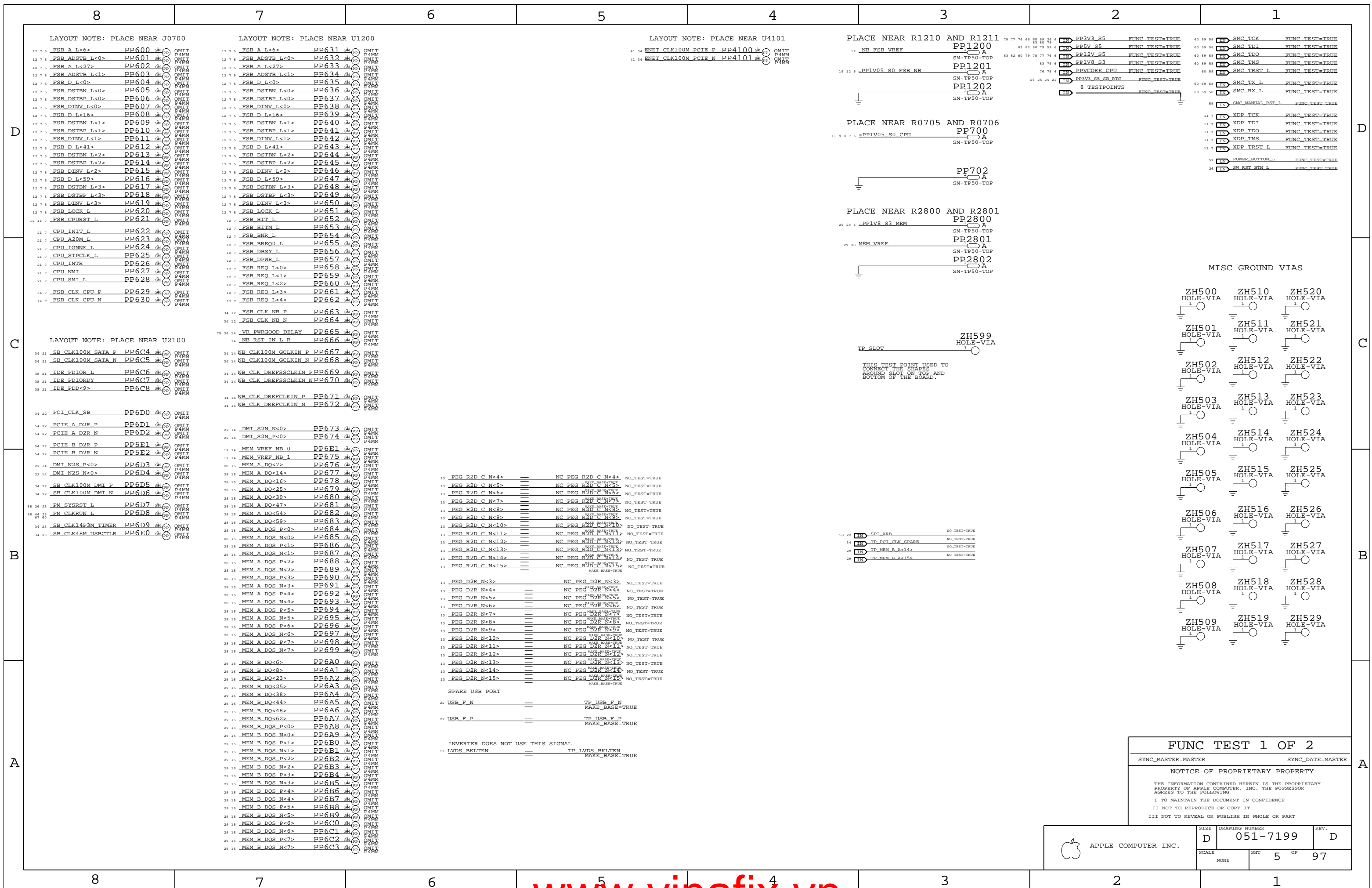
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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7199	D
SCALE	SHT	OF
NONE	4	97



LAYOUT NOTE: PLACE NEAR J0700

12 7 5 FSB A L<6> PP600 OMIT P4MM
 12 7 5 FSB ADSTB L<0> PP601 OMIT P4MM
 12 7 5 FSB A L<27> PP602 OMIT P4MM
 12 7 5 FSB ADSTB L<1> PP603 OMIT P4MM
 12 7 5 FSB D L<0> PP604 OMIT P4MM
 12 7 5 FSB DSTBN L<0> PP605 OMIT P4MM
 12 7 5 FSB DSTBP L<0> PP606 OMIT P4MM
 12 7 5 FSB DINV L<0> PP607 OMIT P4MM
 12 7 5 FSB D L<16> PP608 OMIT P4MM
 12 7 5 FSB DSTBN L<1> PP609 OMIT P4MM
 12 7 5 FSB DSTBP L<1> PP610 OMIT P4MM
 12 7 5 FSB DINV L<1> PP611 OMIT P4MM
 12 7 5 FSB D L<41> PP612 OMIT P4MM
 12 7 5 FSB DSTBN L<2> PP613 OMIT P4MM
 12 7 5 FSB DSTBP L<2> PP614 OMIT P4MM
 12 7 5 FSB DINV L<2> PP615 OMIT P4MM
 12 7 5 FSB D L<59> PP616 OMIT P4MM
 12 7 5 FSB DSTBN L<3> PP617 OMIT P4MM
 12 7 5 FSB DSTBP L<3> PP618 OMIT P4MM
 12 7 5 FSB DINV L<3> PP619 OMIT P4MM
 12 7 5 FSB LOCK L PP620 OMIT P4MM
 12 7 5 FSB CPURST L PP621 OMIT P4MM
 21 7 CPU INIT L PP622 OMIT P4MM
 21 7 CPU A20M L PP623 OMIT P4MM
 21 7 CPU IGNNE L PP624 OMIT P4MM
 21 7 CPU STPCLK L PP625 OMIT P4MM
 21 7 CPU INTR PP626 OMIT P4MM
 21 7 CPU NMI PP627 OMIT P4MM
 21 7 CPU SMI L PP628 OMIT P4MM
 34 7 FSB CLK CPU P PP629 OMIT P4MM
 34 7 FSB CLK CPU N PP630 OMIT P4MM

LAYOUT NOTE: PLACE NEAR U1200

12 7 5 FSB A L<6> PP631 OMIT P4MM
 12 7 5 FSB ADSTB L<0> PP632 OMIT P4MM
 12 7 5 FSB A L<27> PP633 OMIT P4MM
 12 7 5 FSB ADSTB L<1> PP634 OMIT P4MM
 12 7 5 FSB D L<0> PP635 OMIT P4MM
 12 7 5 FSB DSTBN L<0> PP636 OMIT P4MM
 12 7 5 FSB DSTBP L<0> PP637 OMIT P4MM
 12 7 5 FSB DINV L<0> PP638 OMIT P4MM
 12 7 5 FSB D L<16> PP639 OMIT P4MM
 12 7 5 FSB DSTBN L<1> PP640 OMIT P4MM
 12 7 5 FSB DSTBP L<1> PP641 OMIT P4MM
 12 7 5 FSB DINV L<1> PP642 OMIT P4MM
 12 7 5 FSB D L<41> PP643 OMIT P4MM
 12 7 5 FSB DSTBN L<2> PP644 OMIT P4MM
 12 7 5 FSB DSTBP L<2> PP645 OMIT P4MM
 12 7 5 FSB DINV L<2> PP646 OMIT P4MM
 12 7 5 FSB D L<59> PP647 OMIT P4MM
 12 7 5 FSB DSTBN L<3> PP648 OMIT P4MM
 12 7 5 FSB DSTBP L<3> PP649 OMIT P4MM
 12 7 5 FSB DINV L<3> PP650 OMIT P4MM
 12 7 5 FSB LOCK L PP651 OMIT P4MM
 12 7 5 FSB HIT L PP652 OMIT P4MM
 12 7 5 FSB HITM L PP653 OMIT P4MM
 12 7 5 FSB BNR L PP654 OMIT P4MM
 12 7 5 FSB BRQ0 L PP655 OMIT P4MM
 12 7 5 FSB DBSY L PP656 OMIT P4MM
 12 7 5 FSB DPWR L PP657 OMIT P4MM
 12 7 5 FSB REQ L<0> PP658 OMIT P4MM
 12 7 5 FSB REQ L<1> PP659 OMIT P4MM
 12 7 5 FSB REQ L<2> PP660 OMIT P4MM
 12 7 5 FSB REQ L<3> PP661 OMIT P4MM
 12 7 5 FSB REQ L<4> PP662 OMIT P4MM

LAYOUT NOTE: PLACE NEAR U4100

41 34 ENET CLK100M PCIE P PP4100 OMIT P4MM
 41 34 ENET CLK100M PCIE N PP4101 OMIT P4MM

PLACE NEAR R1210 AND R1211

12 NB_FSB_VREF PP1200
 SM-TP50-TOP
 PP1201
 A
 19 12 6 =PP1V05_S0_FSB_NB PP1202
 SM-TP50-TOP
 A

PLACE NEAR R0705 AND R0706

11 9 8 7 =PP1V05_S0_CPU PP700
 SM-TP50-TOP
 A

PP702
 A
 SM-TP50-TOP

PLACE NEAR R2800 AND R2801

29 28 6 =PP1V8_S3_MEM PP2800
 SM-TP50-TOP
 A
 29 28 MEM_VREF PP2801
 SM-TP50-TOP
 A
 PP2802
 A
 SM-TP50-TOP

78 77 76 66 65 59 26 58
 83 82 80 79 78 77 76 6
 83 76 6
 76 75 6
 26 25 24 21

EN PP3V3_S5_FUNC_TEST=TRUE
 EN PP5V_S5_FUNC_TEST=TRUE
 EN PP12V_S5_FUNC_TEST=TRUE
 EN PP1V8_S3_FUNC_TEST=TRUE
 EN PPVCORE_CPU_FUNC_TEST=TRUE
 EN PP3V3_S5_SB_RTC_FUNC_TEST=TRUE
 EN 8_TESTPOINTS_FUNC_TEST=TRUE

60 59 58 SMC_TCK_FUNC_TEST=TRUE
 60 59 58 SMC_TDI_FUNC_TEST=TRUE
 60 59 58 SMC_TDO_FUNC_TEST=TRUE
 60 59 58 SMC_TMS_FUNC_TEST=TRUE
 60 58 SMC_TRST_L_FUNC_TEST=TRUE
 60 59 58 SMC_TX_L_FUNC_TEST=TRUE
 60 59 58 SMC_RX_L_FUNC_TEST=TRUE
 59 SMC_MANUAL_RST_L_FUNC_TEST=TRUE
 11 7 XDP_TCK_FUNC_TEST=TRUE
 11 7 XDP_TDI_FUNC_TEST=TRUE
 11 7 XDP_TDO_FUNC_TEST=TRUE
 11 7 XDP_TMS_FUNC_TEST=TRUE
 11 7 XDP_TRST_L_FUNC_TEST=TRUE
 59 POWER_BUTTON_L_FUNC_TEST=TRUE
 26 SW_RST_BTN_L_FUNC_TEST=TRUE

LAYOUT NOTE: PLACE NEAR U2100

34 21 SB_CLK100M_SATA_P PP6C4 OMIT P4MM
 34 21 SB_CLK100M_SATA_N PP6C5 OMIT P4MM
 38 21 IDE_PDIOR_L PP6C6 OMIT P4MM
 38 21 IDE_PDIORDY PP6C7 OMIT P4MM
 38 21 IDE_PDD<9> PP6C8 OMIT P4MM

34 12 FSB_CLK_NB_P PP663 OMIT P4MM
 34 12 FSB_CLK_NB_N PP664 OMIT P4MM
 75 26 14 VR_PWRGOOD_DELAY PP665 OMIT P4MM
 14 NB_RST_IN_L_R PP666 OMIT P4MM
 34 14 NB_CLK100M_GCLKIN_P PP667 OMIT P4MM
 34 14 NB_CLK100M_GCLKIN_N PP668 OMIT P4MM
 34 14 NB_CLK_DREFSSCLKIN_P PP669 OMIT P4MM
 34 14 NB_CLK_DREFSSCLKIN_N PP670 OMIT P4MM
 34 14 NB_CLK_DREFCLKIN_P PP671 OMIT P4MM
 34 14 NB_CLK_DREFCLKIN_N PP672 OMIT P4MM

34 21 PCI_CLK_SB PP6D0 OMIT P4MM
 54 22 PCIE_A_D2R_P PP6D1 OMIT P4MM
 54 22 PCIE_A_D2R_N PP6D2 OMIT P4MM
 54 22 PCIE_B_D2R_P PP5E1 OMIT P4MM
 54 22 PCIE_B_D2R_N PP5E2 OMIT P4MM
 22 14 DMI_N2S_P<0> PP6D3 OMIT P4MM
 22 14 DMI_N2S_N<0> PP6D4 OMIT P4MM
 34 22 SB_CLK100M_DMI_P PP6D5 OMIT P4MM
 34 22 SB_CLK100M_DMI_N PP6D6 OMIT P4MM
 58 26 23 PM_SYSRST_L PP6D7 OMIT P4MM
 58 41 23 PM_CLKRUN_L PP6D8 OMIT P4MM
 34 23 SB_CLK14PM_TIMER PP6D9 OMIT P4MM
 34 23 SB_CLK48M_USBCNTLR PP6E0 OMIT P4MM

ZH500 HOLE-VIA
 ZH510 HOLE-VIA
 ZH520 HOLE-VIA
 ZH501 HOLE-VIA
 ZH511 HOLE-VIA
 ZH521 HOLE-VIA
 ZH502 HOLE-VIA
 ZH512 HOLE-VIA
 ZH522 HOLE-VIA
 ZH503 HOLE-VIA
 ZH513 HOLE-VIA
 ZH523 HOLE-VIA
 ZH504 HOLE-VIA
 ZH514 HOLE-VIA
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 ZH507 HOLE-VIA
 ZH517 HOLE-VIA
 ZH527 HOLE-VIA
 ZH508 HOLE-VIA
 ZH518 HOLE-VIA
 ZH528 HOLE-VIA
 ZH509 HOLE-VIA
 ZH519 HOLE-VIA
 ZH529 HOLE-VIA

MISC GROUND VIAS

THIS TEST POINT USED TO CONNECT THE SHAPES AROUND SLOT ON TOP AND BOTTOM OF THE BOARD.

13 PEG_R2D_C_N<4> NC_PEG_R2D_C_N<4> NO_TEST=TRUE
 13 PEG_R2D_C_N<5> NC_PEG_R2D_C_N<5> NO_TEST=TRUE
 13 PEG_R2D_C_N<6> NC_PEG_R2D_C_N<6> NO_TEST=TRUE
 13 PEG_R2D_C_N<7> NC_PEG_R2D_C_N<7> NO_TEST=TRUE
 13 PEG_R2D_C_N<8> NC_PEG_R2D_C_N<8> NO_TEST=TRUE
 13 PEG_R2D_C_N<9> NC_PEG_R2D_C_N<9> NO_TEST=TRUE
 13 PEG_R2D_C_N<10> NC_PEG_R2D_C_N<10> NO_TEST=TRUE
 13 PEG_R2D_C_N<11> NC_PEG_R2D_C_N<11> NO_TEST=TRUE
 13 PEG_R2D_C_N<12> NC_PEG_R2D_C_N<12> NO_TEST=TRUE
 13 PEG_R2D_C_N<13> NC_PEG_R2D_C_N<13> NO_TEST=TRUE
 13 PEG_R2D_C_N<14> NC_PEG_R2D_C_N<14> NO_TEST=TRUE
 13 PEG_R2D_C_N<15> NC_PEG_R2D_C_N<15> NO_TEST=TRUE

13 PEG_D2R_N<3> NC_PEG_D2R_N<3> NO_TEST=TRUE
 13 PEG_D2R_N<4> NC_PEG_D2R_N<4> NO_TEST=TRUE
 13 PEG_D2R_N<5> NC_PEG_D2R_N<5> NO_TEST=TRUE
 13 PEG_D2R_N<6> NC_PEG_D2R_N<6> NO_TEST=TRUE
 13 PEG_D2R_N<7> NC_PEG_D2R_N<7> NO_TEST=TRUE
 13 PEG_D2R_N<8> NC_PEG_D2R_N<8> NO_TEST=TRUE
 13 PEG_D2R_N<9> NC_PEG_D2R_N<9> NO_TEST=TRUE
 13 PEG_D2R_N<10> NC_PEG_D2R_N<10> NO_TEST=TRUE
 13 PEG_D2R_N<11> NC_PEG_D2R_N<11> NO_TEST=TRUE
 13 PEG_D2R_N<12> NC_PEG_D2R_N<12> NO_TEST=TRUE
 13 PEG_D2R_N<13> NC_PEG_D2R_N<13> NO_TEST=TRUE
 13 PEG_D2R_N<14> NC_PEG_D2R_N<14> NO_TEST=TRUE
 13 PEG_D2R_N<15> NC_PEG_D2R_N<15> NO_TEST=TRUE

SPARE USB PORT

22 USB_F_N TP_USB_F_N MAKE_BASE=TRUE
 22 USB_F_P TP_USB_F_P MAKE_BASE=TRUE

INVERTER DOES NOT USE THIS SIGNAL

13 LVDS_BKLTEN TP_LVDS_BKLTEN MAKE_BASE=TRUE

FUNC TEST 1 OF 2		
SYNC_MASTER=MASTER	SYNC_DATE=MASTER	
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APPLE COMPUTER INC.	SCALE	SHEET	REV.
	NONE	5 OF 97	D

"S0" RAILS

ONLY ON IN RUN

"S3" RAILS

ON IN RUN AND SLEEP

"S5" RAILS

ALWAYS ON WHEN UNIT HAS AC POWER (TRICKLE)

82 78 76 SYS POWERFAIL L I632 POWER_GOOD

PP0V9_S0 MAKE_BASE=TRUE VOLTAGE=0.9V MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.15MM

PP1V2_S3 MAKE_BASE=TRUE VOLTAGE=1.8V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM

PP3V3_S5 MAKE_BASE=TRUE VOLTAGE=3.3V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM

PPVCORE_CPU MAKE_BASE=TRUE VOLTAGE=1.25V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.15MM

PP1V8_S3 MAKE_BASE=TRUE VOLTAGE=1.8V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM

PP5V_S5 MAKE_BASE=TRUE VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM

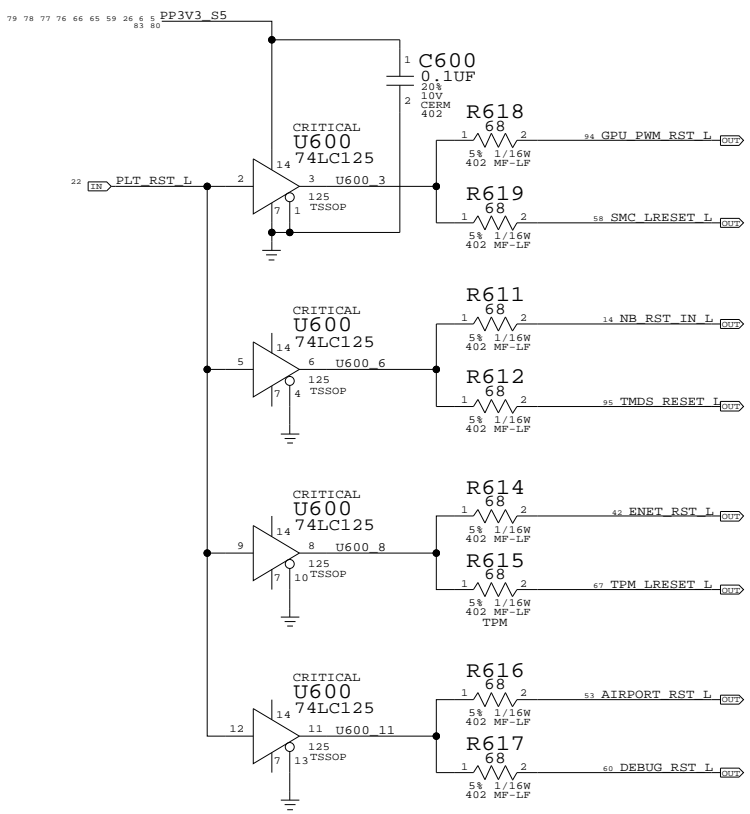
PP1V05_S0 MAKE_BASE=TRUE VOLTAGE=1.05V MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.15MM

PP3V3_S3 MAKE_BASE=TRUE VOLTAGE=3.3V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM

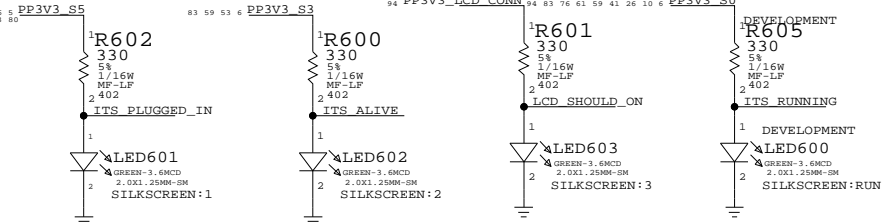
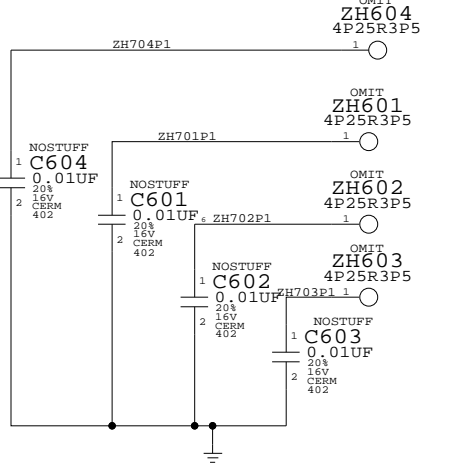
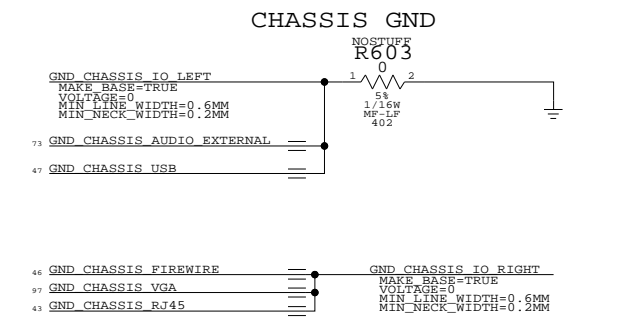
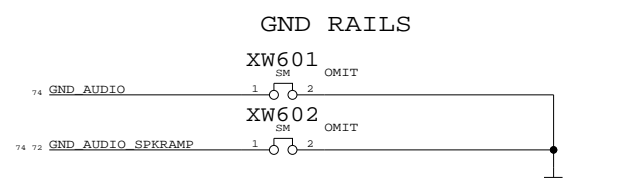
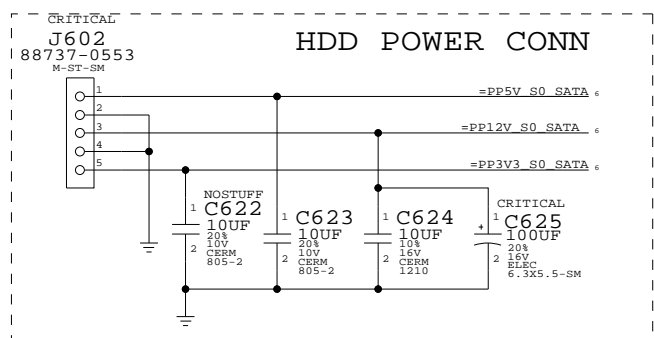
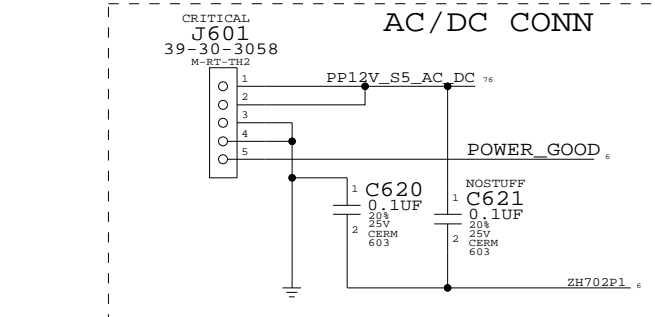
PP1V5_S0 MAKE_BASE=TRUE VOLTAGE=0 V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.15MM

PP5V_S3 MAKE_BASE=TRUE VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM

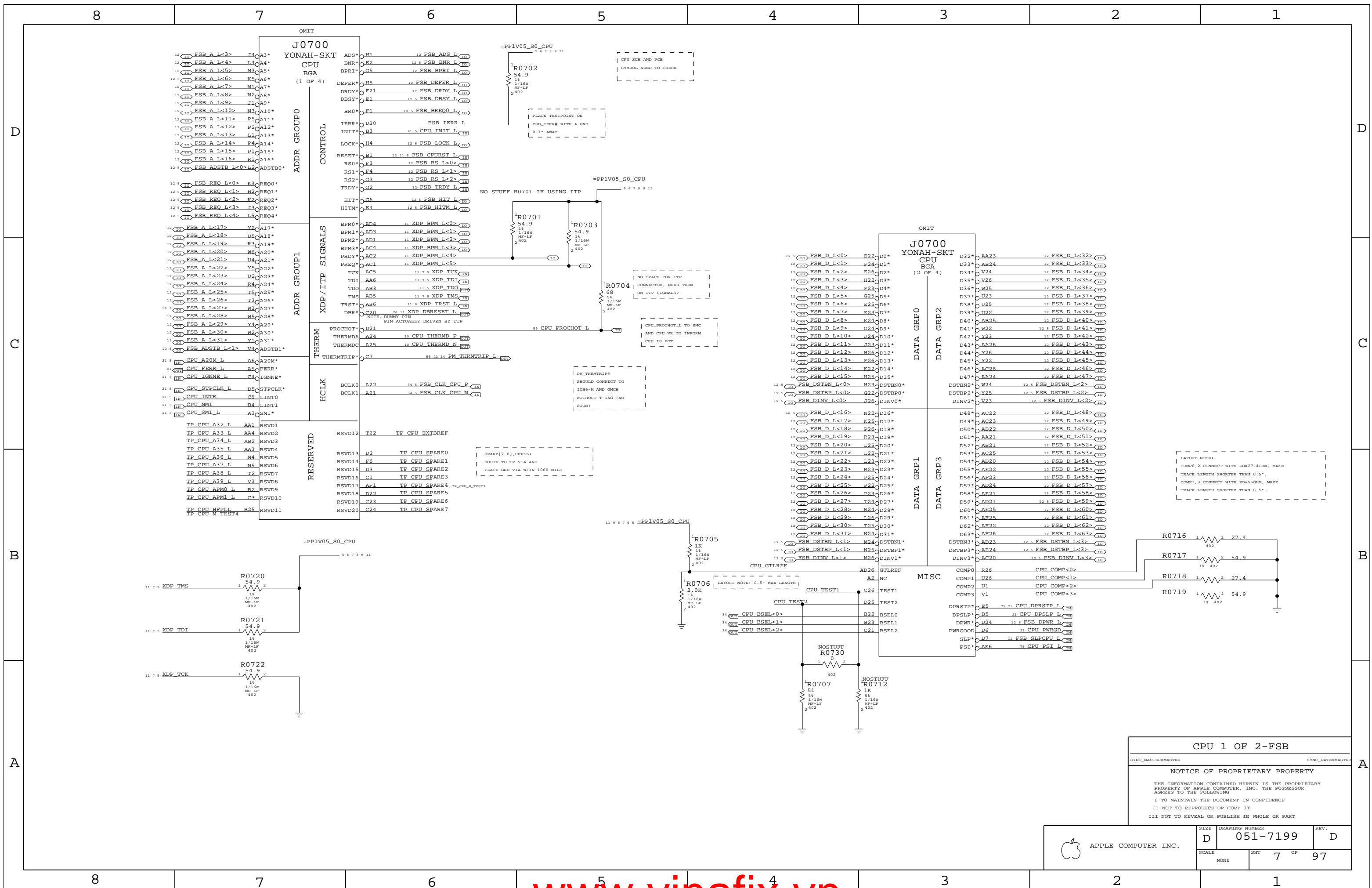
PP12V_S5 MAKE_BASE=TRUE VOLTAGE=12V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM



- List of power rail connections including PP0V9_S0, PPVCORE_CPU, PP1V05_S0, PP1V5_S0, PP1V8_S3, PP2V5_S0, PP3V3_S0, PP3V3_S3, PP3V3_S5, PP4V5_S0_AUDIO_ANALOG, PP5V_S0, and PP12V_S0.



Power Conn / Alias table with columns for SYNC_MASTER, SYNC_DATE, and NOTICE OF PROPRIETARY PROPERTY.



CPU 1 OF 2-FSB

SYNC_MASTER-MASTER SYNC_DATE-MASTER

NOTICE OF PROPRIETARY PROPERTY

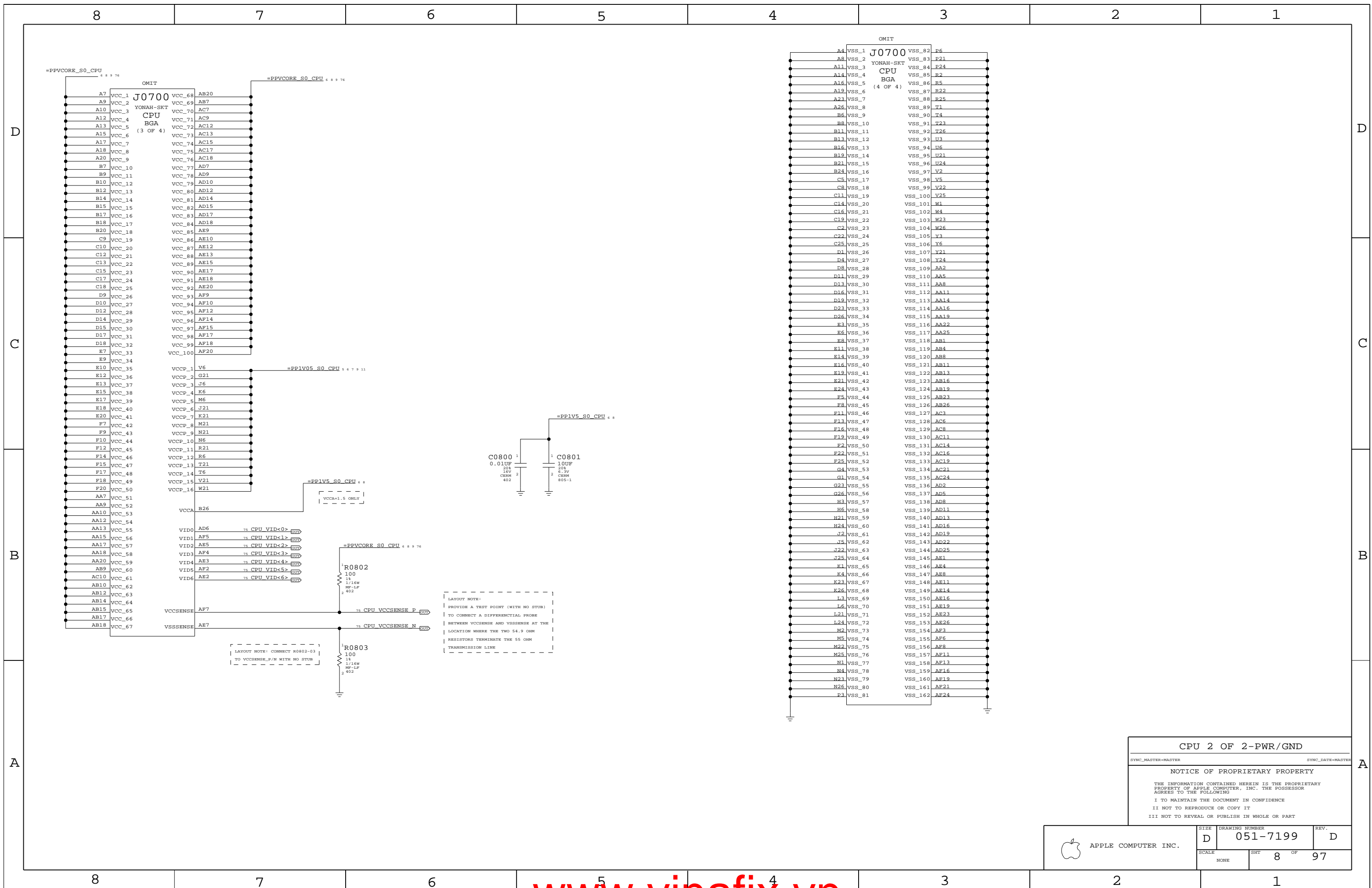
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	D
SCALE	SHT	7 OF	97
NONE			



CPU 2 OF 2-PWR/GND

SYNC_MASTER=MASTER SYNC_DATE=MASTER

NOTICE OF PROPRIETARY PROPERTY

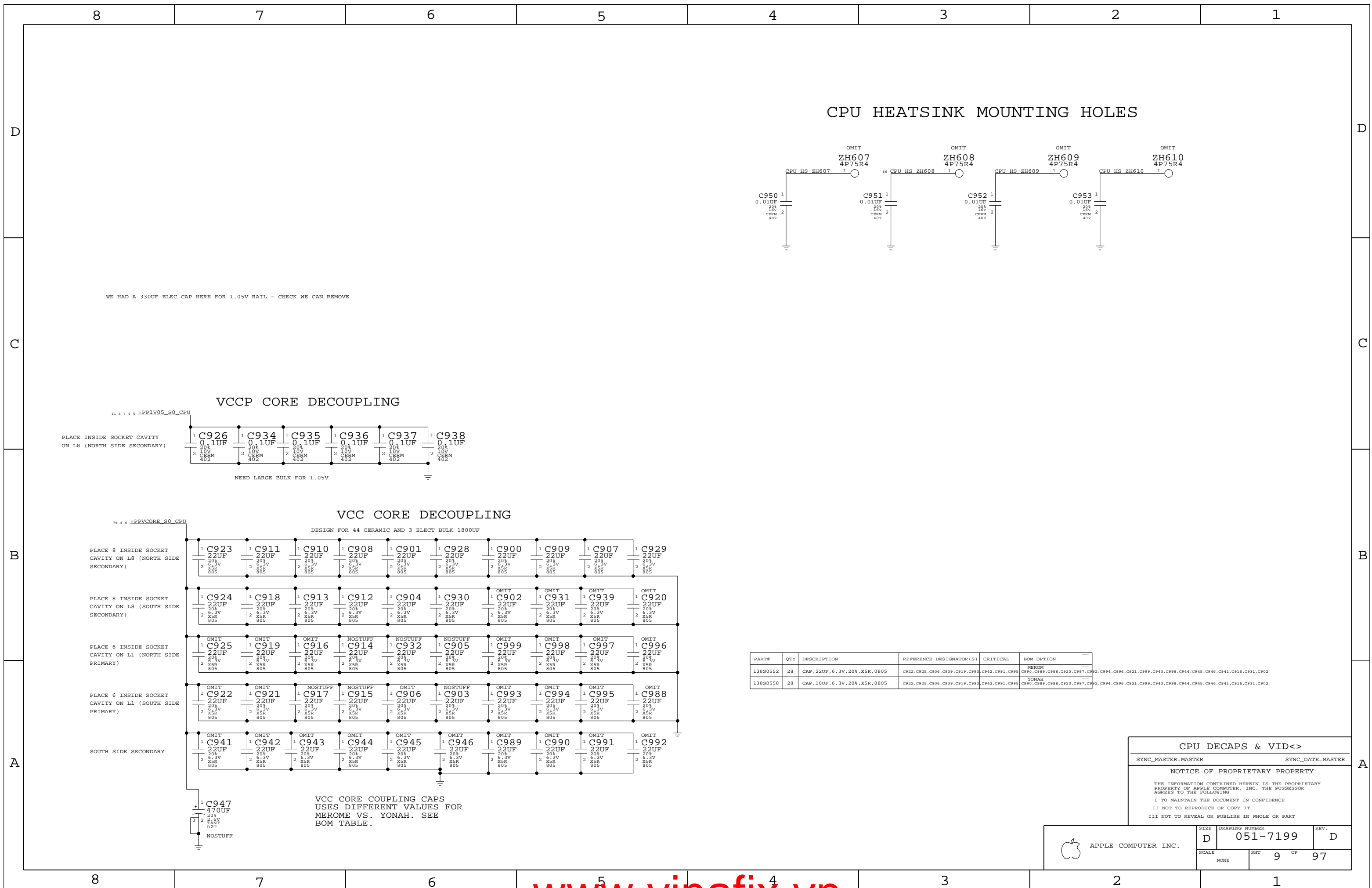
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

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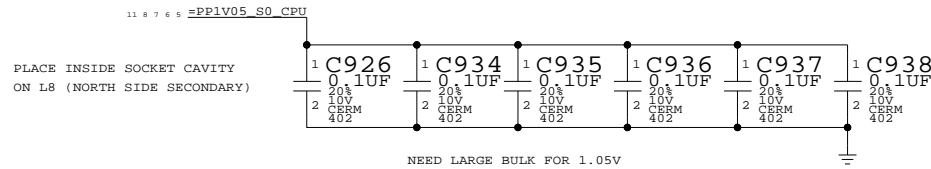
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	D
SCALE	SHT	OF	REV.
NONE	8	97	



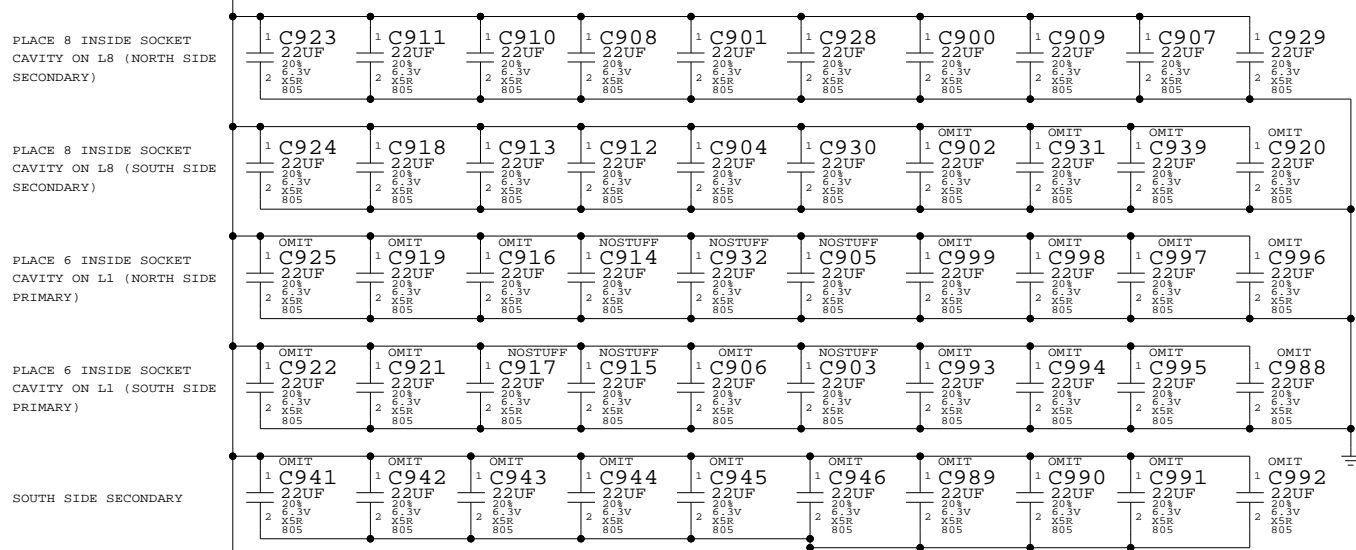
WE HAD A 330UF ELEC CAP HERE FOR 1.05V RAIL - CHECK WE CAN REMOVE

VCCP CORE DECOUPLING



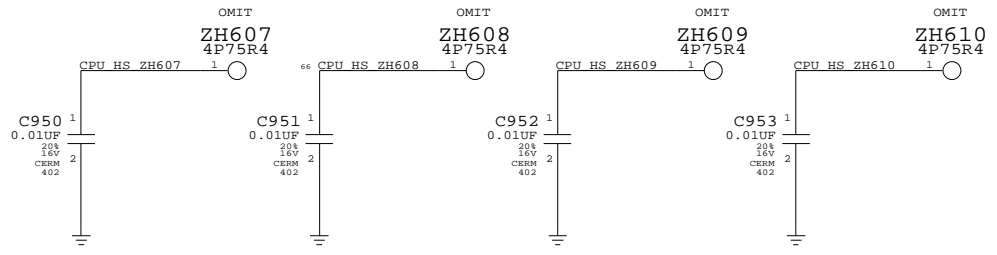
VCC CORE DECOUPLING

DESIGN FOR 44 CERAMIC AND 3 ELECT BULK 1800UF



VCC CORE COUPLING CAPS USES DIFFERENT VALUES FOR MEROME VS. YONAH. SEE BOM TABLE.

CPU HEATSINK MOUNTING HOLES



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
138S0552	28	CAP, 22UF, 6.3V, 20%, X5R, 0805	C922, C925, C906, C939, C919, C993, C942, C991, C995		MEROME C990, C989, C988, C920, C997, C992, C994, C996, C921, C999, C943, C998, C944, C945, C946, C941, C916, C931, C902
138S0558	28	CAP, 10UF, 6.3V, 20%, X5R, 0805	C922, C925, C906, C939, C919, C993, C942, C991, C995		YONAH C990, C989, C988, C920, C997, C992, C994, C996, C921, C999, C943, C998, C944, C945, C946, C941, C916, C931, C902

CPU DECAPS & VID<>

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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APPLE COMPUTER INC.

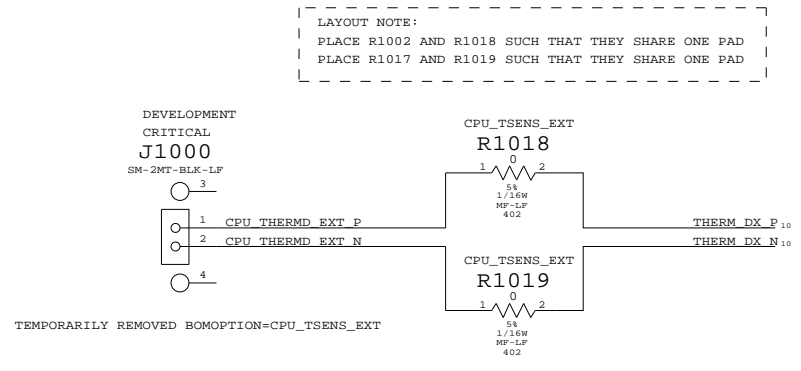
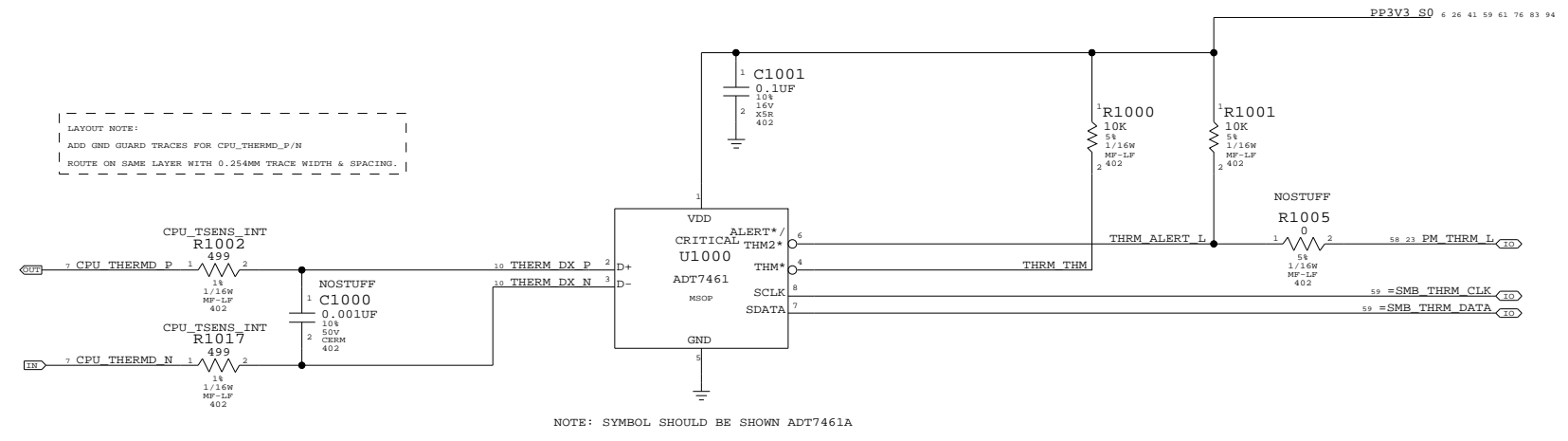
SCALE NONE SHEET 9 OF 97

DRAWING NUMBER 051-7199

REV. D

CPU THERMAL SENSOR

NOTE:
IF CPU T DIODE TO BE READ IN OFF STATE,
THEN THIS SHOULD BE S5



CPU TEMP SENSOR

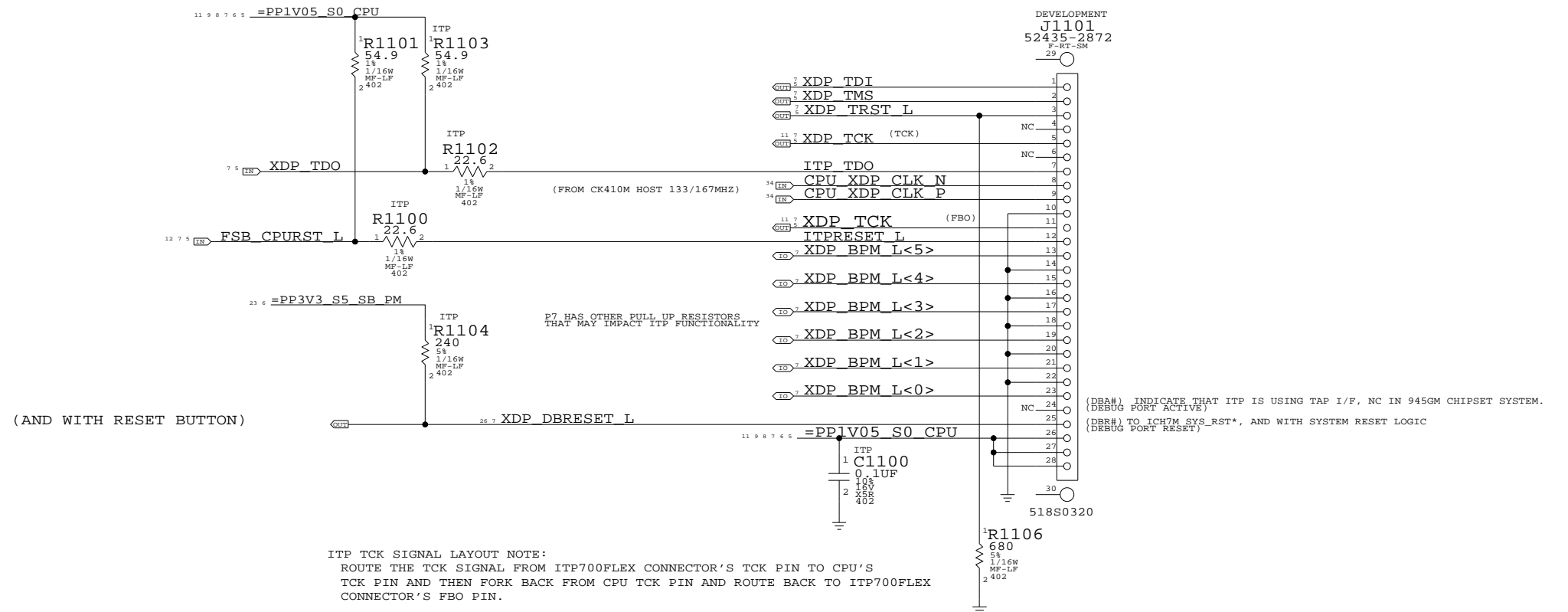
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	D	051-7199	D
SCALE	SHT	10 OF 97	
NONE			

CPU ITP700FLEX DEBUG SUPPORT



CPU ITP700FLEX DEBUG

SYNC_MASTER=M38 SYNC_DATE=01/05/2006

NOTICE OF PROPRIETARY PROPERTY

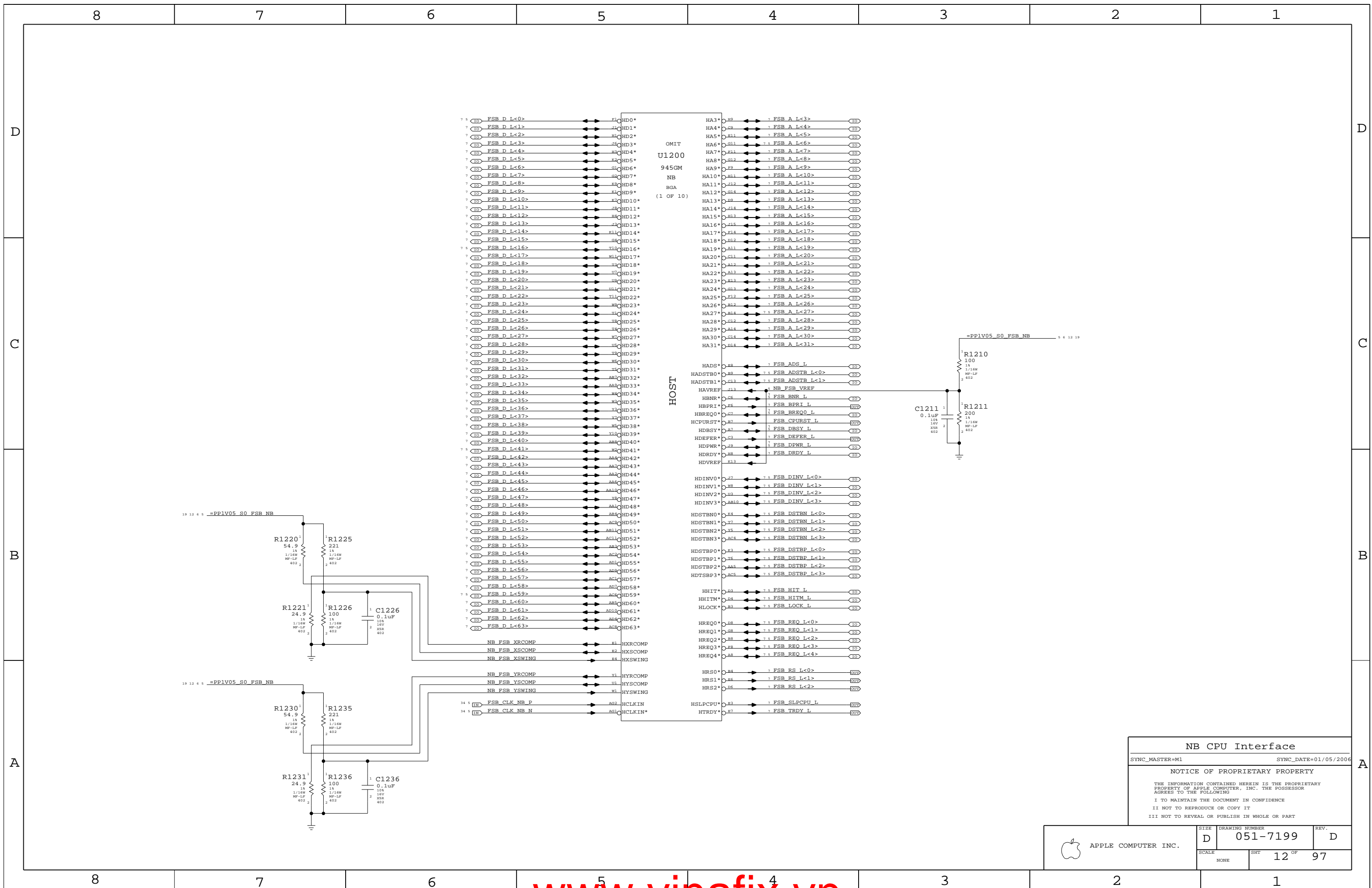
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SCALE	SHT	11 OF	97
NONE			



NB CPU Interface

SYNC_MASTER=M1 SYNC_DATE=01/05/2006

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7199	REV. D
	SCALE NONE	SHEET 12 OF 97	

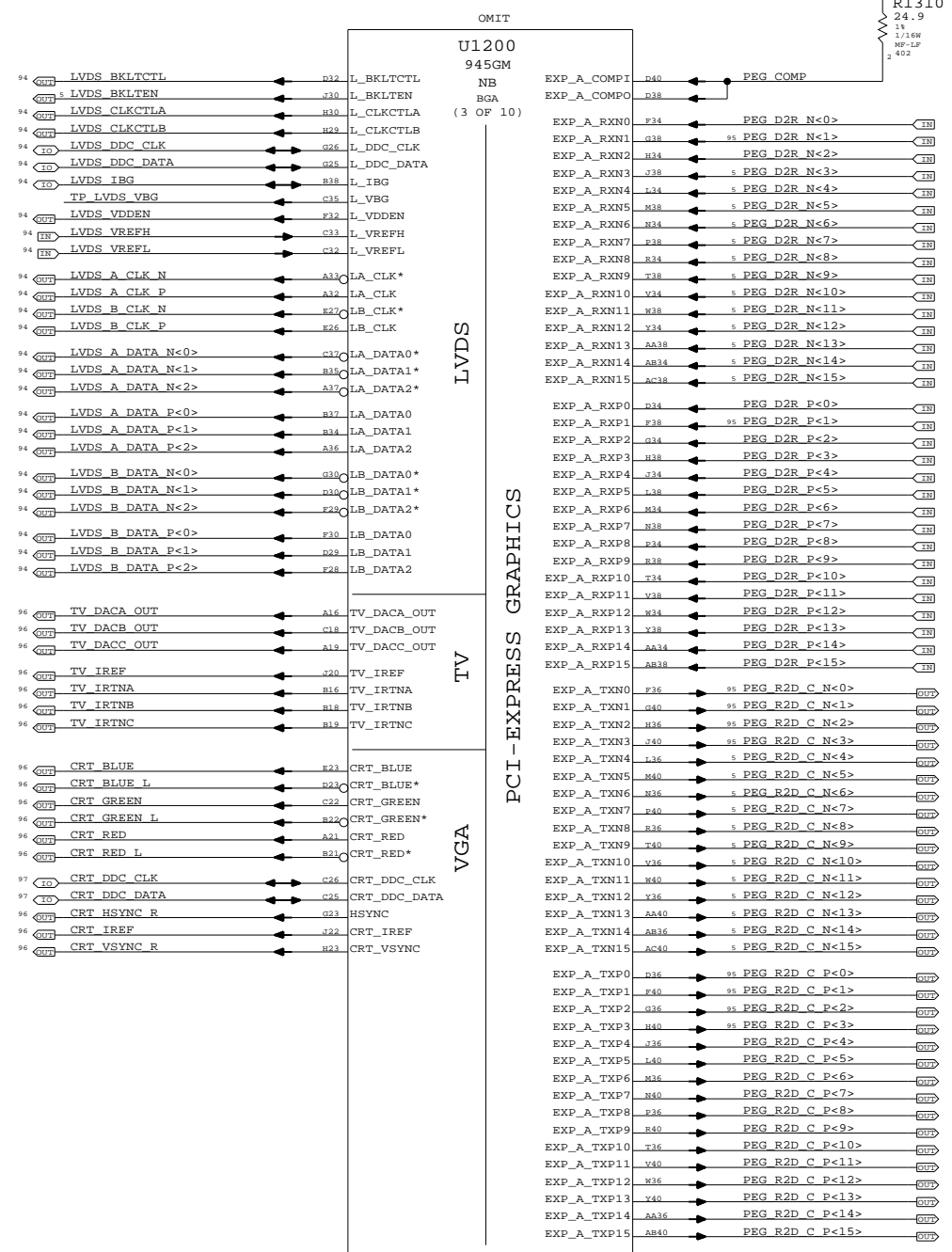
LVDS Disable
 Can leave all signals NC if LVDS is not implemented
 Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
 VCCD_LVDS must remain powered with proper decoupling.
 Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:
 Composite: DACA only
 S-Video: DACB & DACC only
 Component: DACA, DACB & DACC

Unused DAC outputs must remain powered, but can omit
 filtering components. Unused DAC outputs should
 connect to GND through 75-ohm resistors.

TV-Out Disable
 Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail.
 Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and
 VCCA_TVVBG to 1.5V power rail. Tie VSSA_TVVBG to GND.

CRT Disable
 Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie
 HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core
 rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.



SDVO Alternate Function

SDVO_TVCLKIN#
 SDVO_INT#
 SDVO_FLDSTALL#

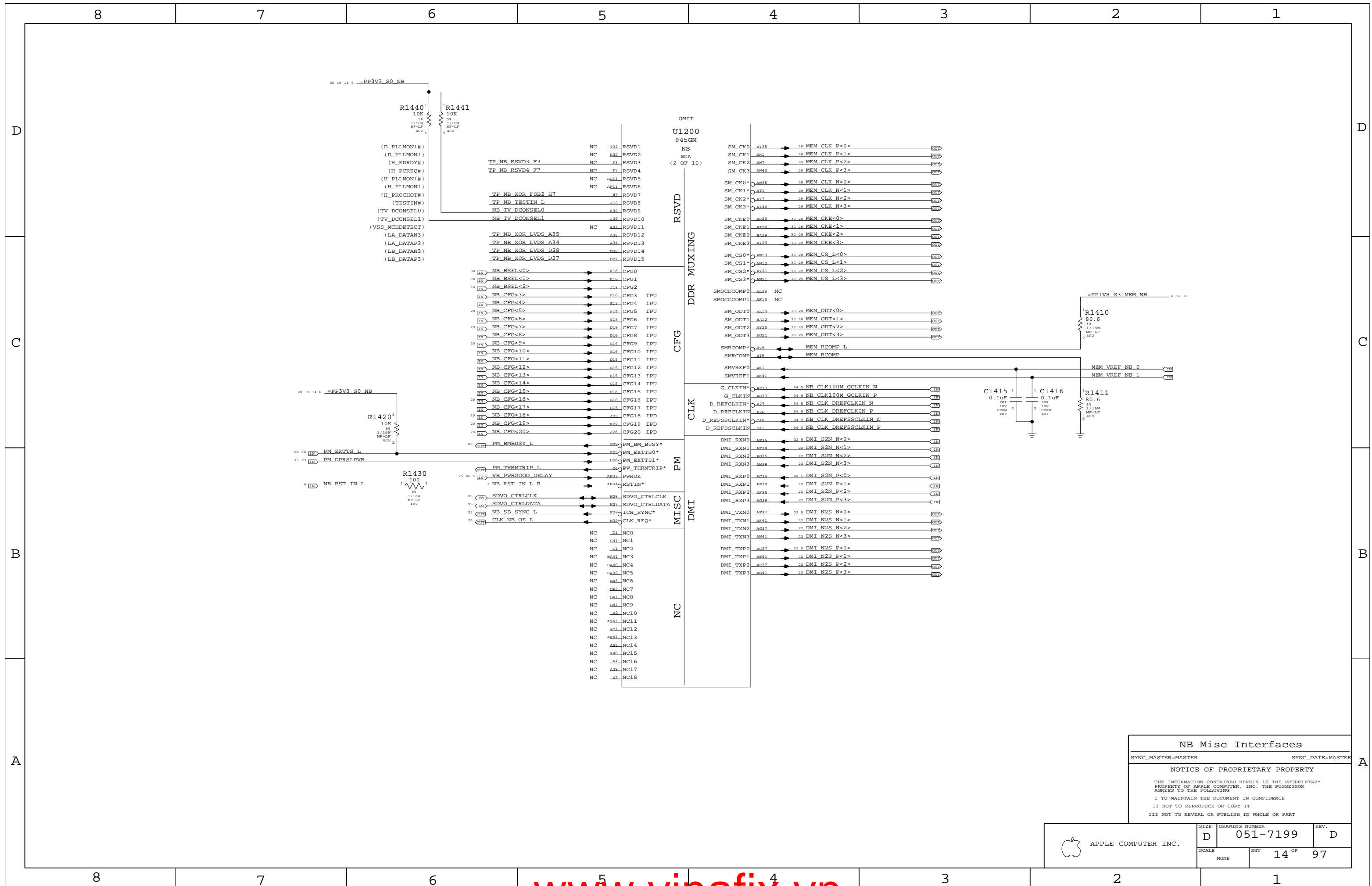
SDVO_TVCLKIN
 SDVO_INT
 SDVO_FLDSTALL

SDVOB_RED#
 SDVOB_GREEN#
 SDVOB_BLUE#
 SDVOB_CLKN
 SDVOC_RED#
 SDVOC_GREEN#
 SDVOC_BLUE#
 SDVOC_CLKN

SDVOB_RED
 SDVOB_GREEN
 SDVOB_BLUE
 SDVOB_CLKP
 SDVOC_RED
 SDVOC_GREEN
 SDVOC_BLUE
 SDVOC_CLKP

NB PEG / Video Interfaces
 SYNC_MASTER=M1 SYNC_DATE=01/05/2006
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	D
SCALE	SHT	13 OF 97	
NONE			



NB Misc Interfaces

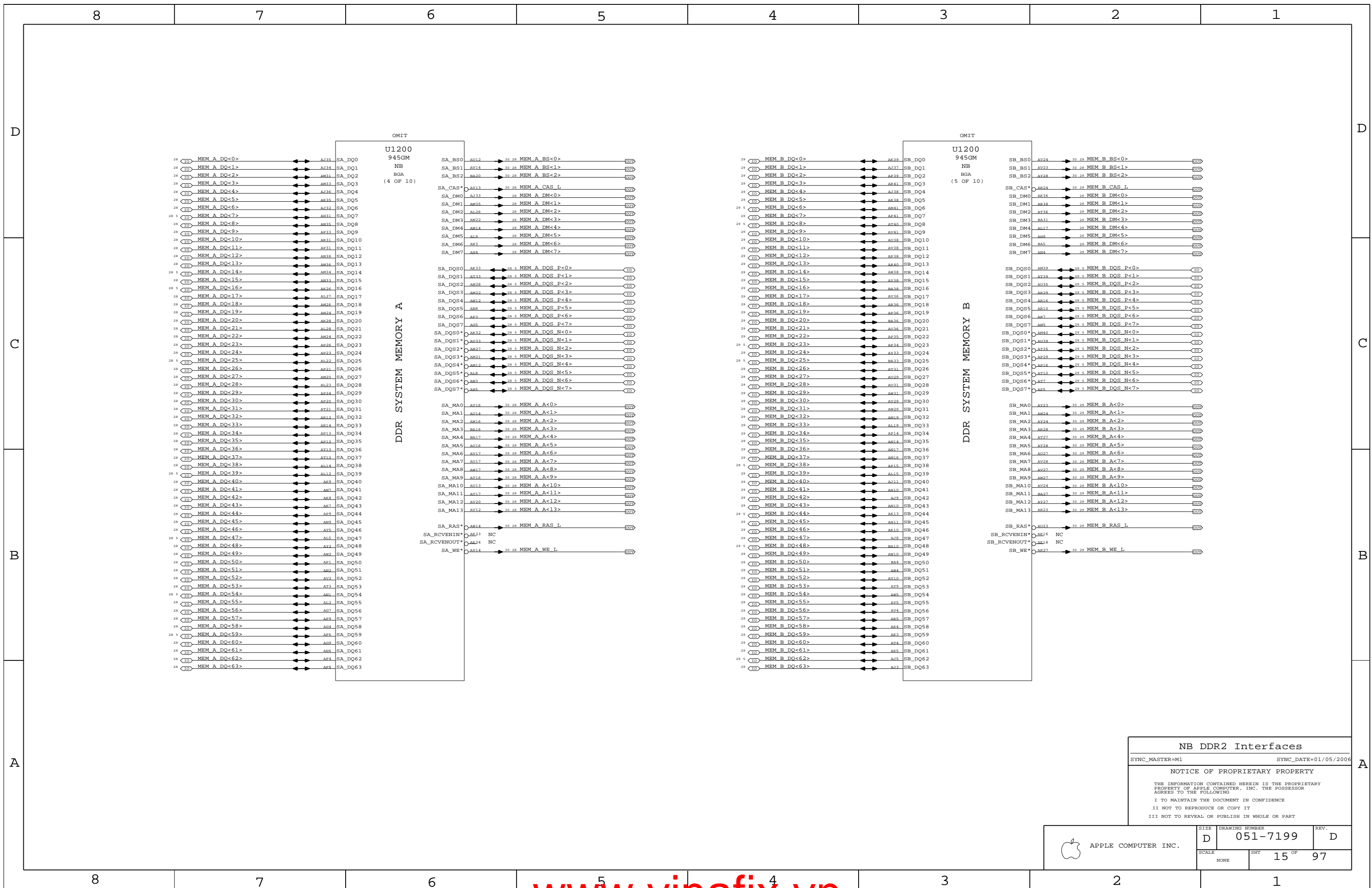
SYNC_MASTER=MASTER SYNC_DATE=MASTER

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7199	REV. D
	SCALE NONE	SHEET 14 OF 97	



NB DDR2 Interfaces

SYNC_MASTER=M1 SYNC_DATE=01/05/2006

NOTICE OF PROPRIETARY PROPERTY

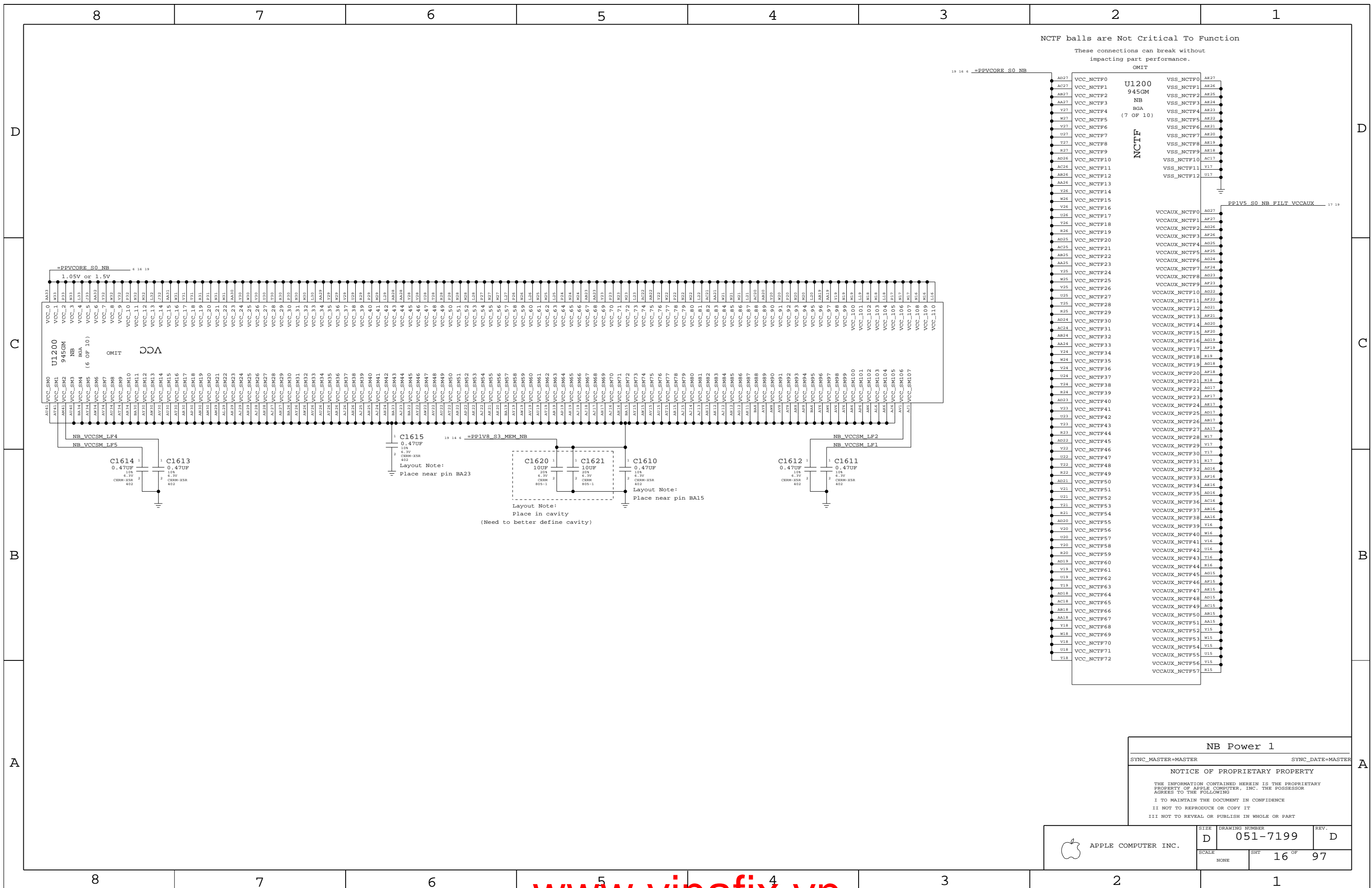
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	D	051-7199	D
SCALE	SHT	15 OF	97
NONE			



NCTF balls are Not Critical To Function
 These connections can break without impacting part performance.
 OMIT

U1200
 945GM
 NB
 BGA
 (7 OF 10)
 NCTF

VCC

VCCAUX

VCCAUX

VCCAUX

VCCAUX

VCCAUX

VCCAUX

VCCAUX

VCCAUX

VCCAUX

VCCAUX

VCCAUX

VCCAUX

VCCAUX

VCCAUX

VCCAUX

VCCAUX

VCCAUX

VCCAUX

VCCAUX

VCCAUX

VCCAUX

VCCAUX

VCCAUX

VCCAUX

VCCAUX

VCCAUX

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VCCAUX

VCCAUX

VCCAUX

VCCAUX

VCCAUX

VCCAUX

VCCAUX

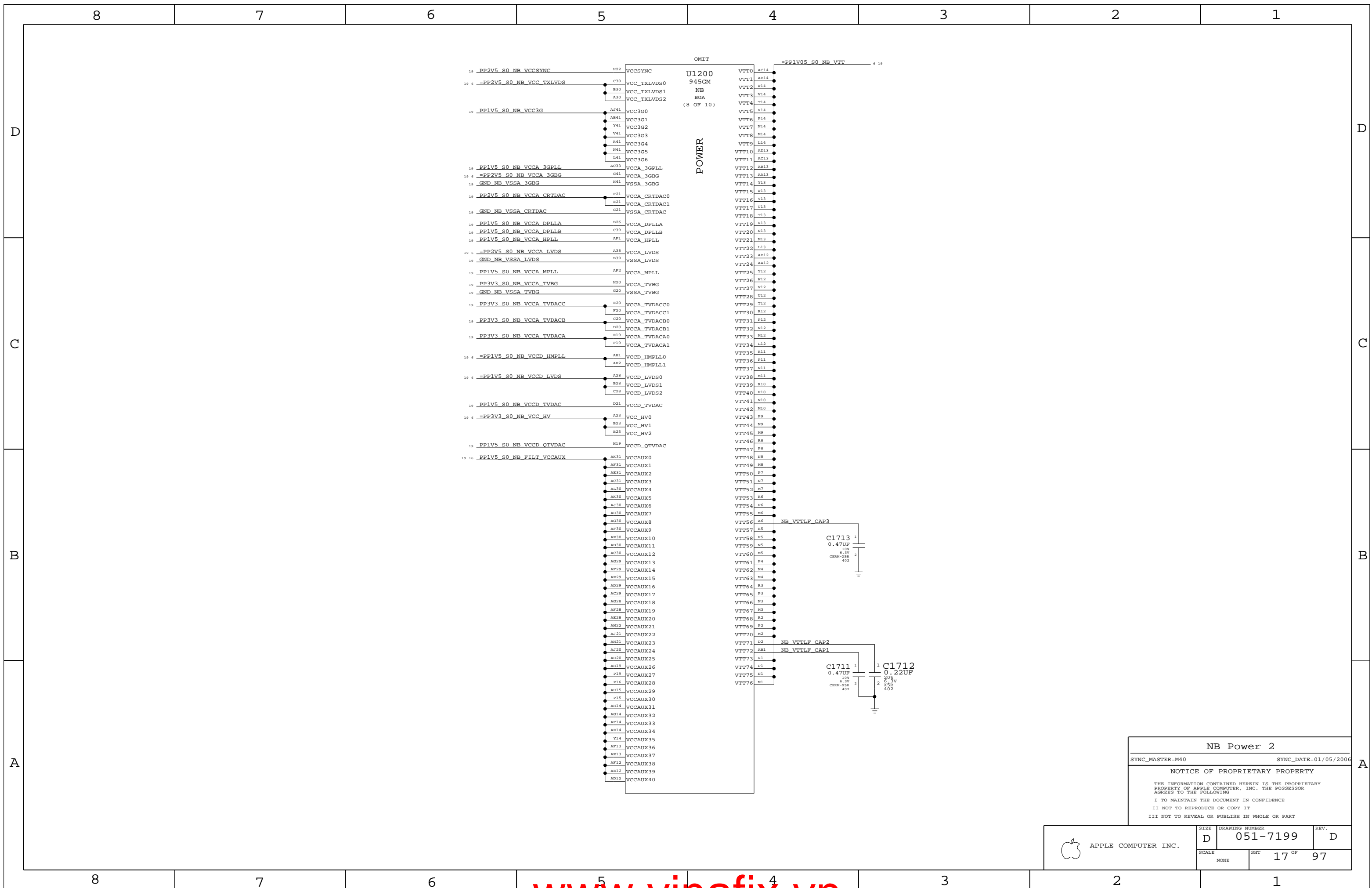
VCCAUX

VCCAUX

VCCAUX

NB Power 1
 SYNC_MASTER=MASTER SYNC_DATE=MASTER
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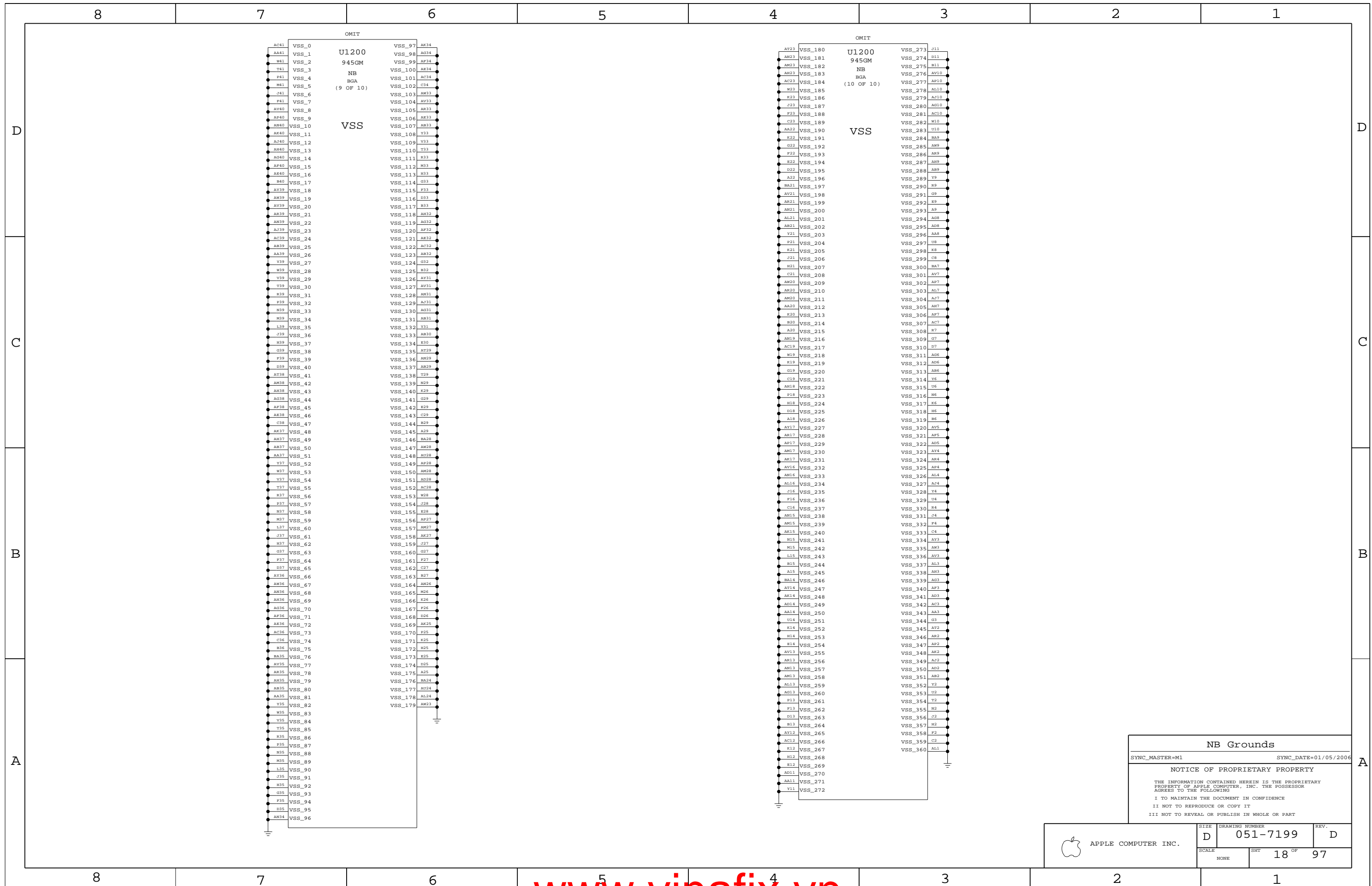
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	D
SCALE	SHT	16 OF	97
NONE			



NB Power 2
 SYNC_MASTER=M40 SYNC_DATE=01/05/2006

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	D
SCALE	NONE	SHT	17 OF 97



NB Grounds

SYNC_MASTER=M1 SYNC_DATE=01/05/2006

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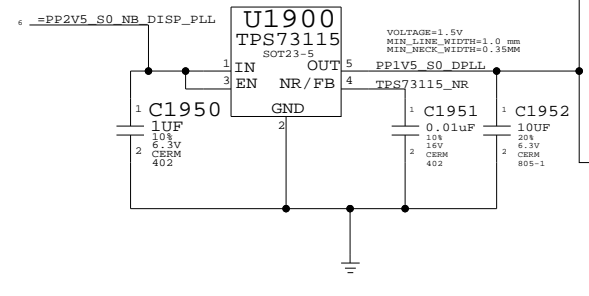
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7199	REV. D
	SCALE NONE	SHT 18 OF 97	

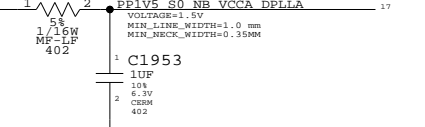
Power Interface
These are the power signals that leave the NB "block"

- PP1V05_S0_FSB_NB 5 6 12
- PPVCORE_S0_NB 6 16 19
- PP1V05_S0_NB_VTT 6 17 19
- PP1V5_S0_NB 6 19
- PP1V5_S0_NB_PCIE 6 13
- PP1V5_S0_NB_PLL 6 19
- PP1V5_S0_NB_TVDAC 6 19
- PP1V5_S0_NB_VCCD_HMPLL 6 17
- PP1V5_S0_NB_VCCD_LVDS 6 17 19
- PP1V5_S0_NB_VCCAUX 6 19
- PP1V8_S3_MEM_NB 6 14 16 19
- PP2V5_S0_NB_VCCSYNC 19 6
- PP2V5_S0_NB_VCC_TXLVDS 6 17 19
- PP2V5_S0_NB_VCCA_3BG 6 19
- PP2V5_S0_NB_VCCA_LVDS 6 17 19
- PP3V3_S0_NB 6 14 20
- PP3V3_S0_NB_VCC_HV 6 17 19
- PP5V_S0_NB_TVDAC 6 19

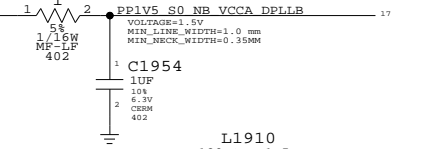
MCH DISPLAY PLL POWER LDO



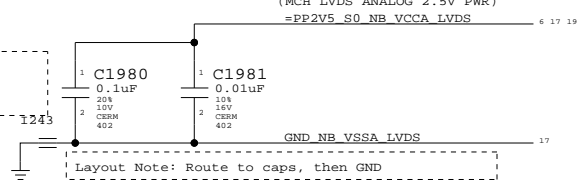
MCH VCCA_DPLLA FILTER
(MCH DISPLAY A PLL 1.5V PWR)



GMCH VCCA_DPLL_B FILTER
(MCH DISPLAY B PLL 1.5V PWR)



MCH VCCA_LVDS FILTER
(MCH LVDS ANALOG 2.5V PWR)

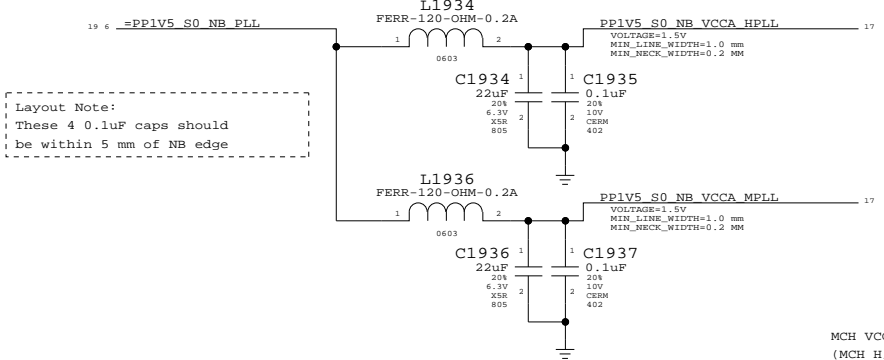


Layout Note:
This 0.1uF cap should be within 5 mm of NB edge

Layout Note: Route to caps, then GND

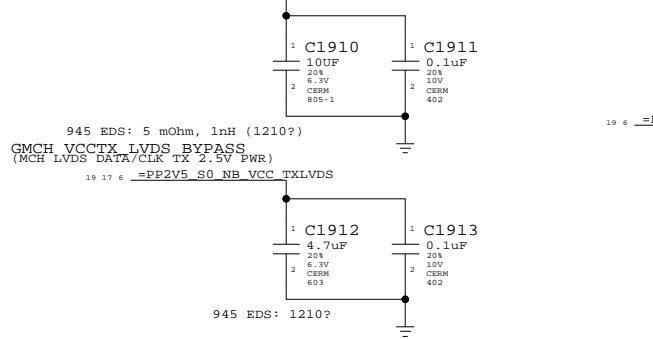
Layout Note:
These 2 caps should be within 6.35 mm of NB edge

Layout Note: Route to caps, then GND

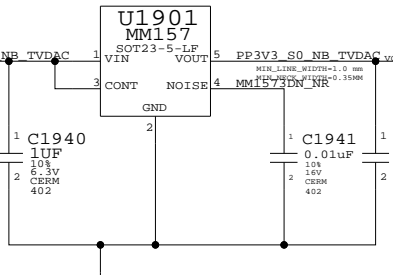


Layout Note:
These 4 0.1uF caps should be within 5 mm of NB edge

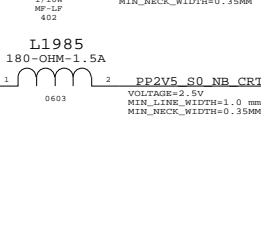
GMCH VCCD_LVDS BYPASS
(MCH LVDS DIGITAL 1.5V PWR)



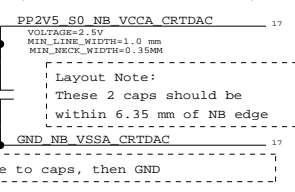
FILTERING REQUIRED FOR INTEGRATED GFX (PG. 333)



MCH VCCA_CRDACC BYPASS
(MCH CRDACC ANALOG 2.5V PWR)



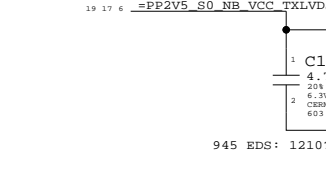
MCH VCCA_CRDACC BYPASS
(MCH CRDACC ANALOG 2.5V PWR)



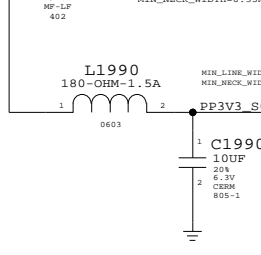
Layout Note:
These 2 caps should be within 6.35 mm of NB edge

Layout Note: Route to caps, then GND

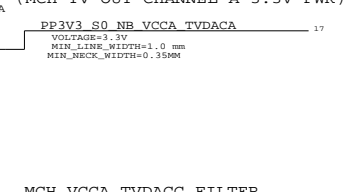
GMCH VCCD_TX LVDS BYPASS
(MCH LVDS DIGITAL TX 2.5V PWR)



MCH VCCA_TVDACC FILTER
(MCH TV OUT CHANNEL A 3.3V PWR)



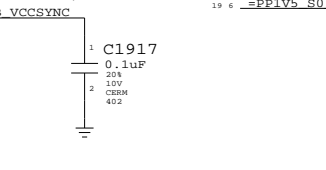
MCH VCCA_TVDACC FILTER
(MCH TV OUT CHANNEL A 3.3V PWR)



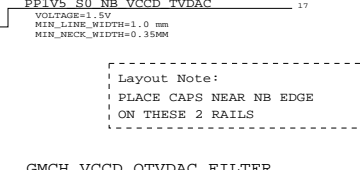
Layout Note:
These 8 caps should be within 6.35 mm of NB edge

Layout Note: Route to caps, then GND

MCH VCCSYNC BYPASS
(MCH H/V SYNC 2.5V PWR)

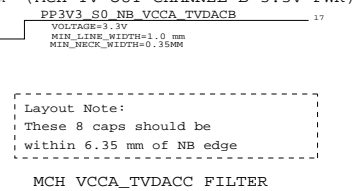


GMCH VCCD_TVDAC FILTER
(MCH TVDAC DEDICATED PWR 1.5V)

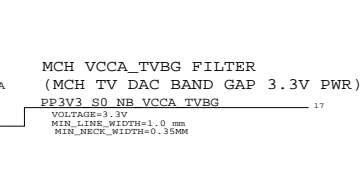


Layout Note:
PLACE CAPS NEAR NB EDGE ON THESE 2 RAILS

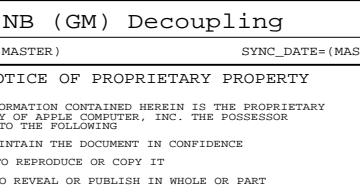
MCH VCCA_TVDACC FILTER
(MCH TV OUT CHANNEL B 3.3V PWR)



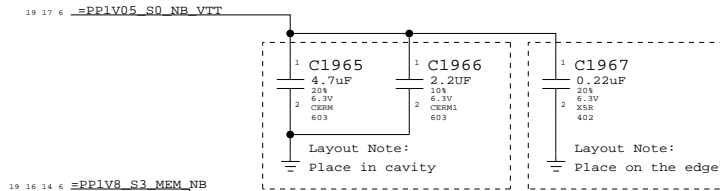
MCH VCCA_TVDACC FILTER
(MCH TV OUT CHANNEL C 3.3V PWR)



MCH VCCA_TVBG FILTER
(MCH TV DAC BAND GAP 3.3V PWR)

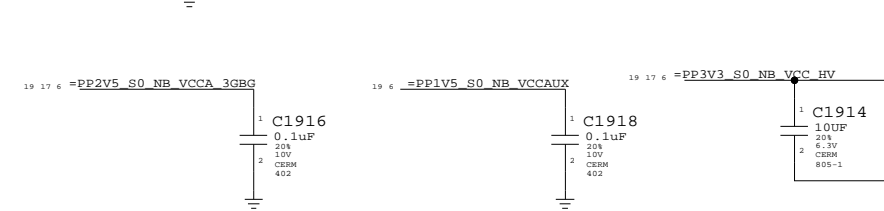
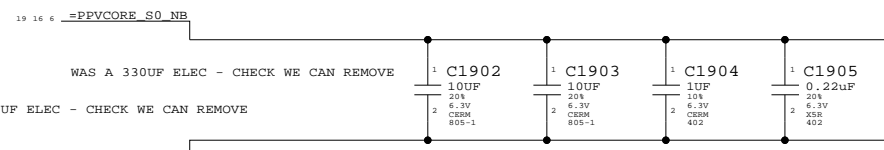
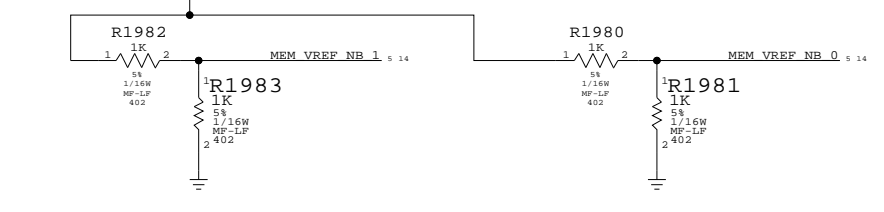


Layout Note:
Route to caps, then GND

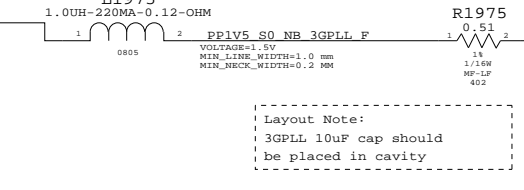


Layout Note:
Place in cavity

Layout Note:
Place on the edge



PP1V5_S0_NB_3GPLL



Layout Note:
Place L and C close to MCH

Layout Note:
10uF caps should be close to MCH on opposite side.

Layout Note:
3GPLL 10uF cap should be placed in cavity

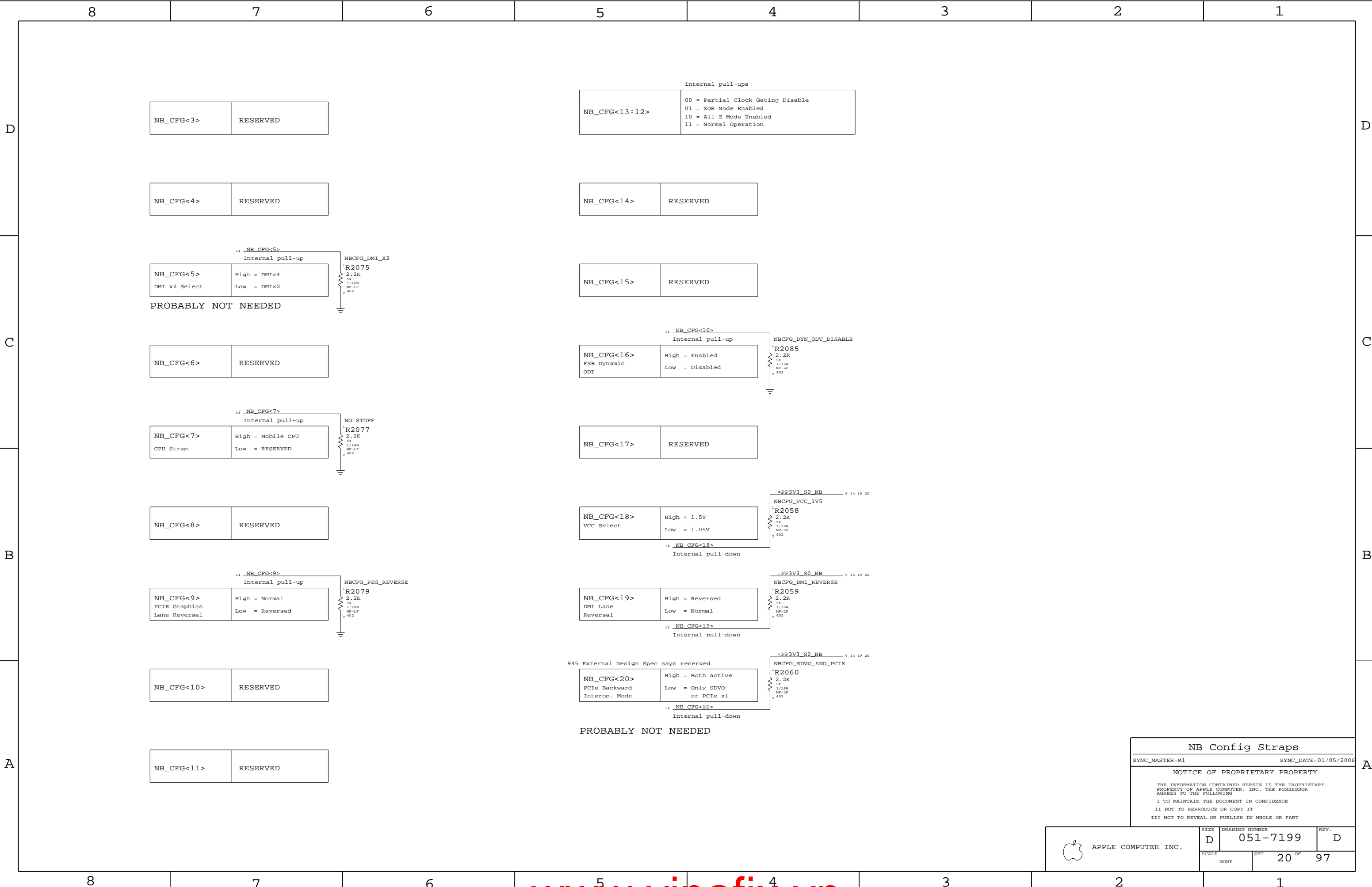
Layout Note: Route to caps, then GND

NB (GM) Decoupling

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	D
SCALE	SHT	19 OF 97	
NONE			



NB_CFG<3>	RESERVED
-----------	----------

Internal pull-ups

NB_CFG<13:12>	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal Operation
---------------	----------------------------------------------------------------------------------------------------------------

NB_CFG<4>	RESERVED
-----------	----------

NB_CFG<14>	RESERVED
------------	----------

14 NB_CFG<5>
Internal pull-up

NB_CFG<5>	High = DMiX4 DMI x2 Select Low = DMiX2
-----------	----------------------------------------------

PROBABLY NOT NEEDED

NBCFG_DMI_X2
R2075
2.2K
5%
1/16W
MF-LP
2 402

NB_CFG<15>	RESERVED
------------	----------

NB_CFG<6>	RESERVED
-----------	----------

14 NB_CFG<16>
Internal pull-up

NB_CFG<16>	High = Enabled FSB Dynamic Low = Disabled ODT
------------	--------------------------------------------------------

NBCFG_DYN_ODT_DISABLE
R2085
2.2K
5%
1/16W
MF-LP
2 402

14 NB_CFG<7>
Internal pull-up

NB_CFG<7>	High = Mobile CPU CPU Strap Low = RESERVED
-----------	--------------------------------------------------

NO STUFF
R2077
2.2K
5%
1/16W
MF-LP
2 402

NB_CFG<17>	RESERVED
------------	----------

NB_CFG<8>	RESERVED
-----------	----------

=PP3V3_S0_NB 6 14 19 20

NB_CFG<18>	High = 1.5V VCC Select Low = 1.05V
------------	------------------------------------------

NBCFG_VCC_1V5
R2058
2.2K
5%
1/16W
MF-LP
2 402

14 NB_CFG<18>
Internal pull-down

14 NB_CFG<9>
Internal pull-up

NB_CFG<9>	High = Normal PCIe Graphics Lane Reversal Low = Reversed
-----------	-------------------------------------------------------------------

NBCFG_PEG_REVERSE
R2079
2.2K
5%
1/16W
MF-LP
2 402

=PP3V3_S0_NB 6 14 19 20

NB_CFG<19>	High = Reversed DMI Lane Reversal Low = Normal
------------	---------------------------------------------------------

NBCFG_DMI_REVERSE
R2059
2.2K
5%
1/16W
MF-LP
2 402

14 NB_CFG<19>
Internal pull-down

NB_CFG<10>	RESERVED
------------	----------

945 External Design Spec says reserved

NB_CFG<20>	High = Both active PCIe Backward Interop. Mode Low = Only SDVO or PCIe x1
------------	---------------------------------------------------------------------------------------

=PP3V3_S0_NB 6 14 19 20
NBCFG_SDVO_AND_PCIE
R2060
2.2K
5%
1/16W
MF-LP
2 402

14 NB_CFG<20>
Internal pull-down

PROBABLY NOT NEEDED

NB_CFG<11>	RESERVED
------------	----------

NB Config Straps

SYNC_MASTER=M1 SYNC_DATE=01/05/2006

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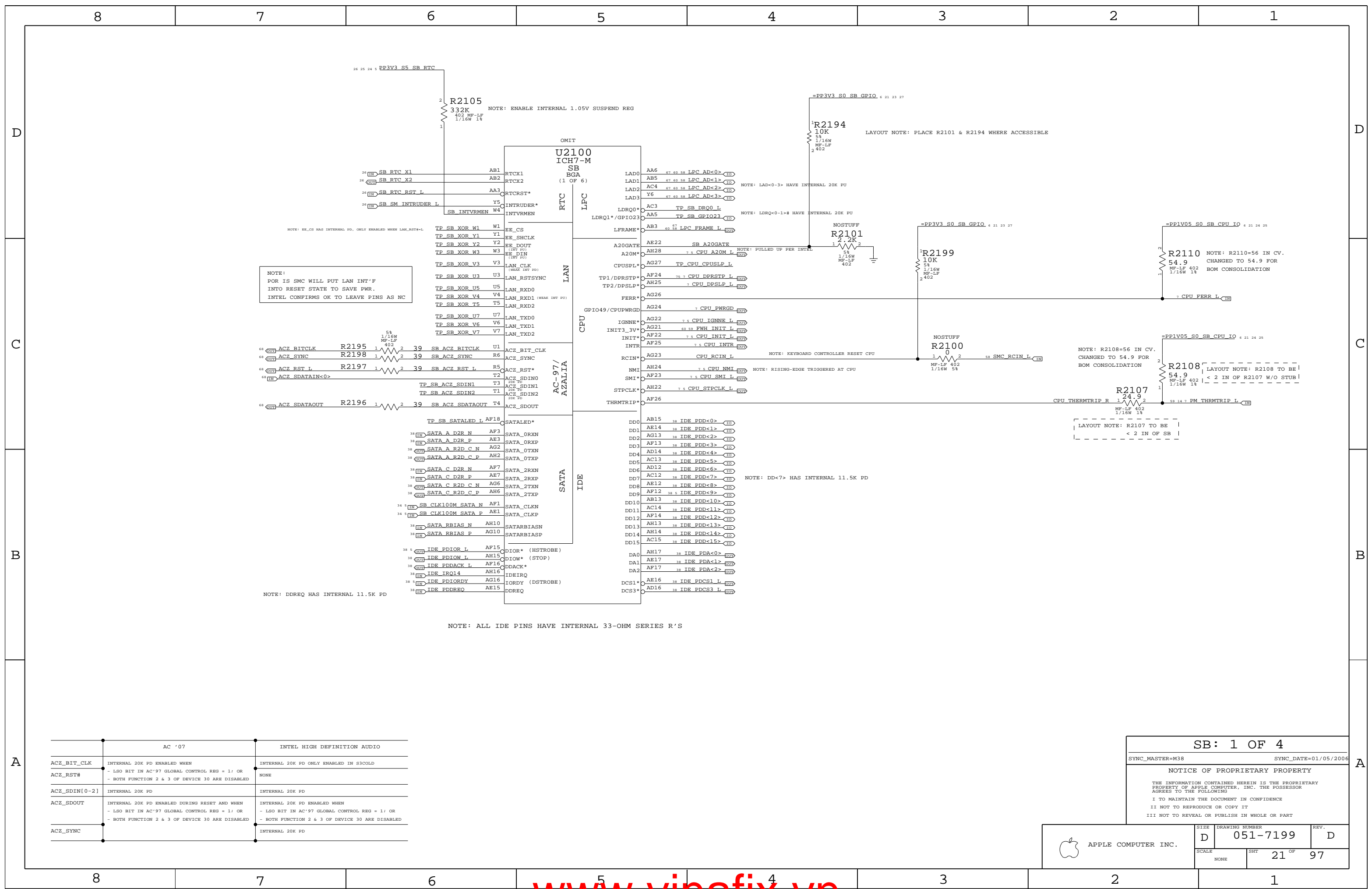
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	D	051-7199	D
SCALE		SHT	OF
NONE		20	97



NOTE:
POR IS SMC WILL PUT LAN INT'F INTO RESET STATE TO SAVE PWR. INTEL CONFIRMS OK TO LEAVE PINS AS NC

NOTE: DDREQ HAS INTERNAL 11.5K PD

NOTE: ALL IDE PINS HAVE INTERNAL 33-OHM SERIES R'S

AC '07	INTEL HIGH DEFINITION AUDIO
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR
ACZ_RST#	NONE
ACZ_SDIN[0-2]	INTERNAL 20K PD
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
ACZ_SYNC	INTERNAL 20K PD

SB: 1 OF 4

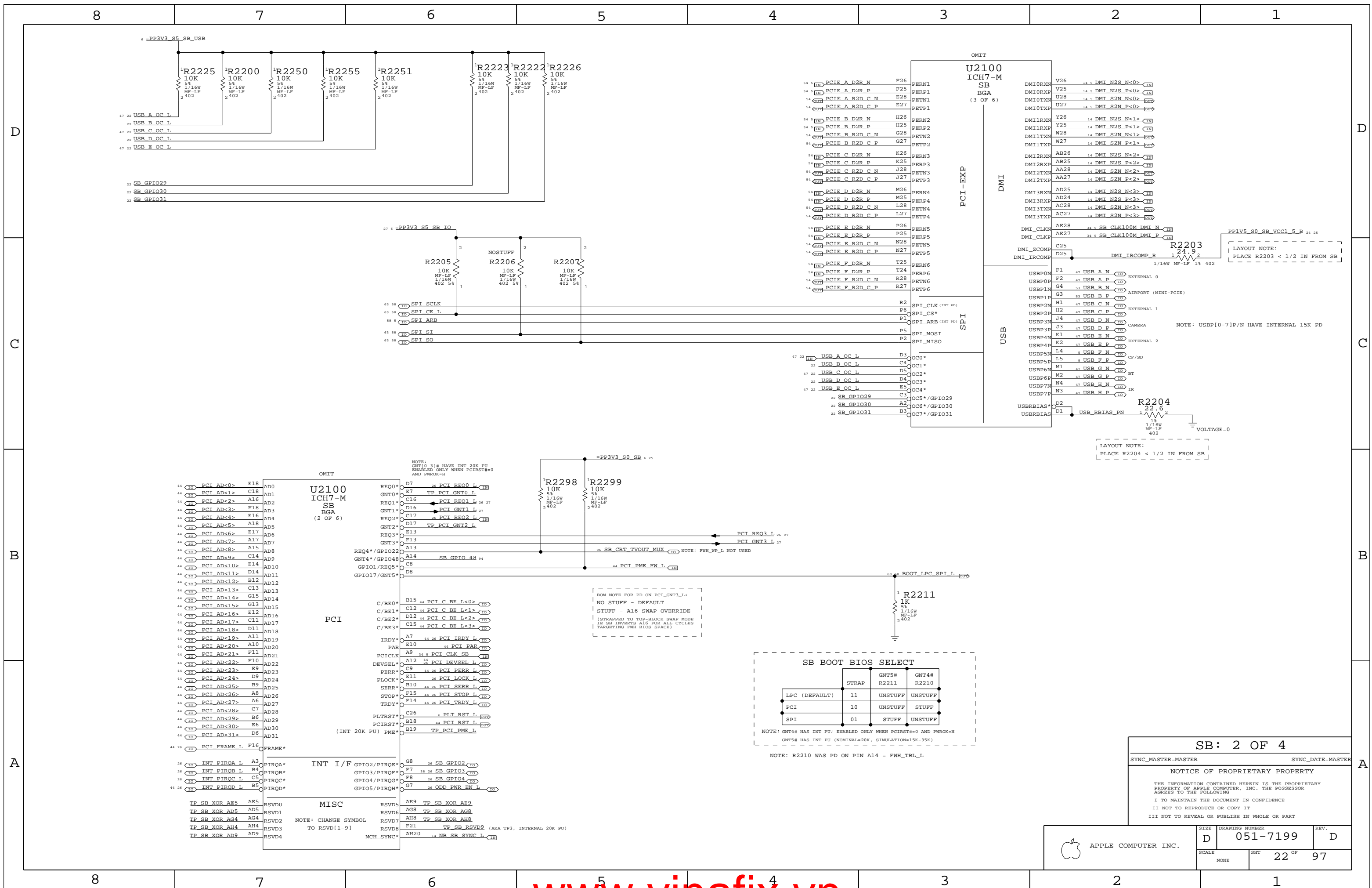
SYNC_MASTER=M38 SYNC_DATE=01/05/2006

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	D	051-7199	D
SCALE	SHT	21 OF 97	
NONE			



SB BOOT BIOS SELECT

	STRAP	GNT5# R2211	GNT4# R2210
LPC (DEFAULT)	11	UNSTUFF	UNSTUFF
PCI	10	UNSTUFF	STUFF
SPI	01	STUFF	UNSTUFF

NOTE: GNT4# HAS INT PU: ENABLED ONLY WHEN PCIRST#0 AND FWR0#-H
GNT5# HAS INT PU (NOMINAL=20K, SIMULATION=15K-35K)
NOTE: R2211 WAS PD ON PIN A14 = FWH_TBL_L

SB: 2 OF 4

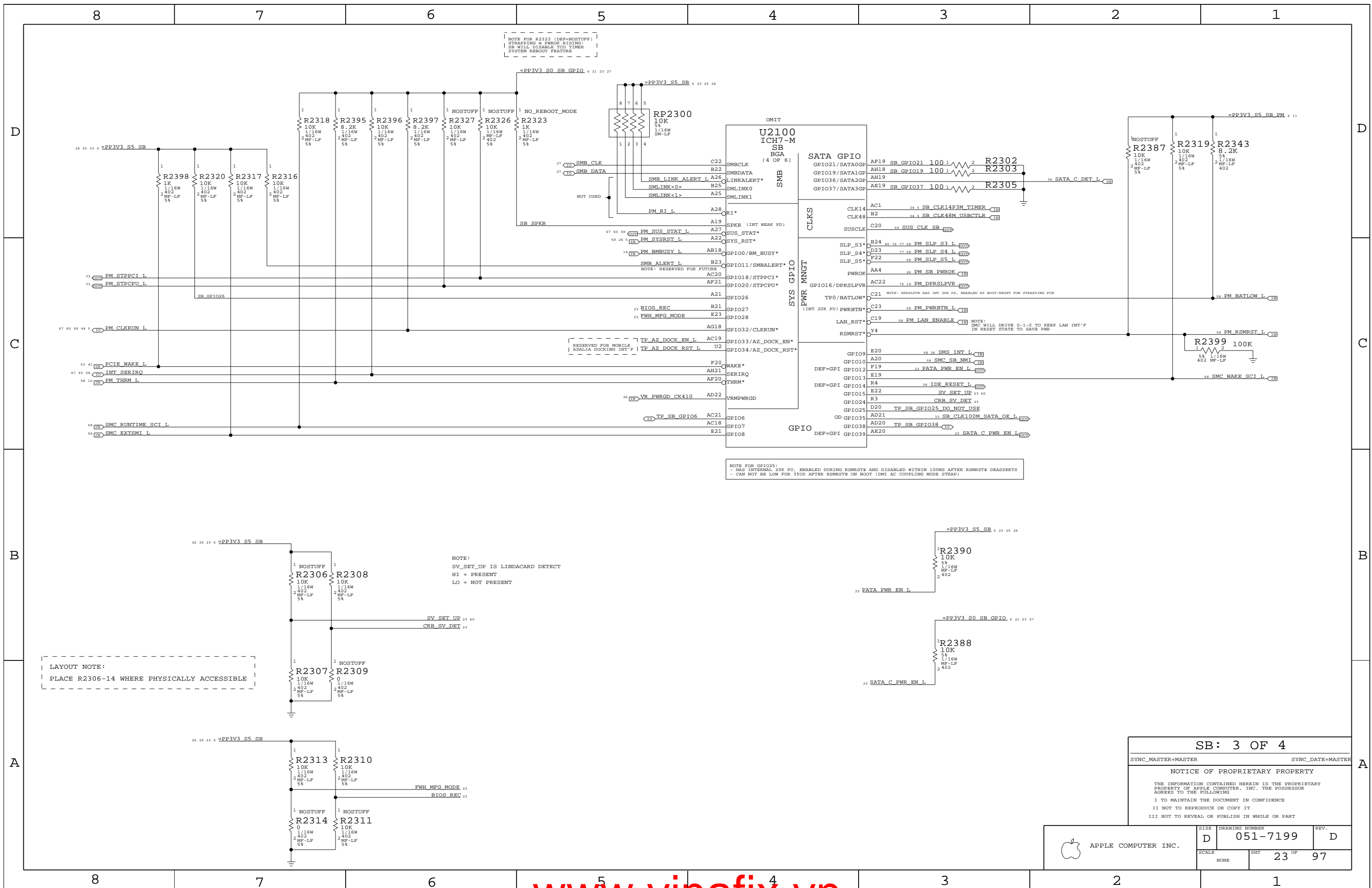
SYNC_MASTER=MASTER SYNC_DATE=MASTER

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	NONE	051-7199	D
SHEET		22 OF 97	



NOTE FOR R2323 (DEF-NOSTUFF)
STRAPPING & PWROK RISING:
SB WILL DISABLE TOO TIMER
SYSTEM REBOOT FEATURE

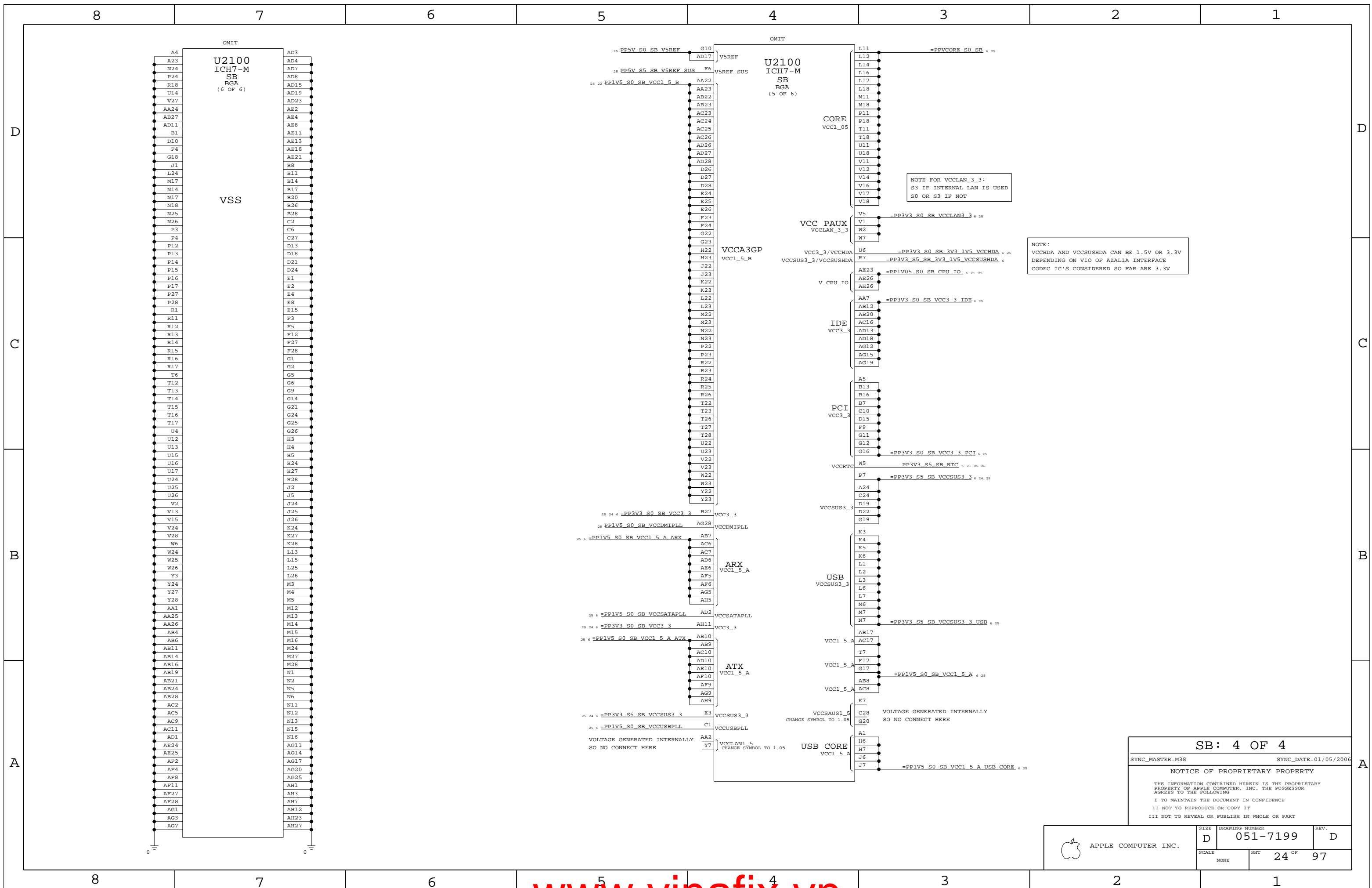
NOTE FOR GPIO25:
- HAS INTERNAL 20K PU, ENABLED DURING RSMRST# AND DISABLED WITHIN 100MS AFTER RSMRST# DEASSERTS
- CAN NOT BE LOW FOR 35US AFTER RSMRST# ON BOOT (EMI AC COUPLING MODE STRAP)

NOTE:
SV_SET_UP IS LINDACARD DETECT
HI = PRESENT
LO = NOT PRESENT

LAYOUT NOTE:
PLACE R2306-14 WHERE PHYSICALLY ACCESSIBLE

SB: 3 OF 4
SYNC_MASTER=MASTER SYNC_DATE=MASTER
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APPLE COMPUTER INC.
DRAWING NUMBER: 051-7199
SCALE: NONE SHT: 23 OF 97
REV: D



SB: 4 OF 4

SYNC_MASTER=M38 SYNC_DATE=01/05/2006

NOTICE OF PROPRIETARY PROPERTY

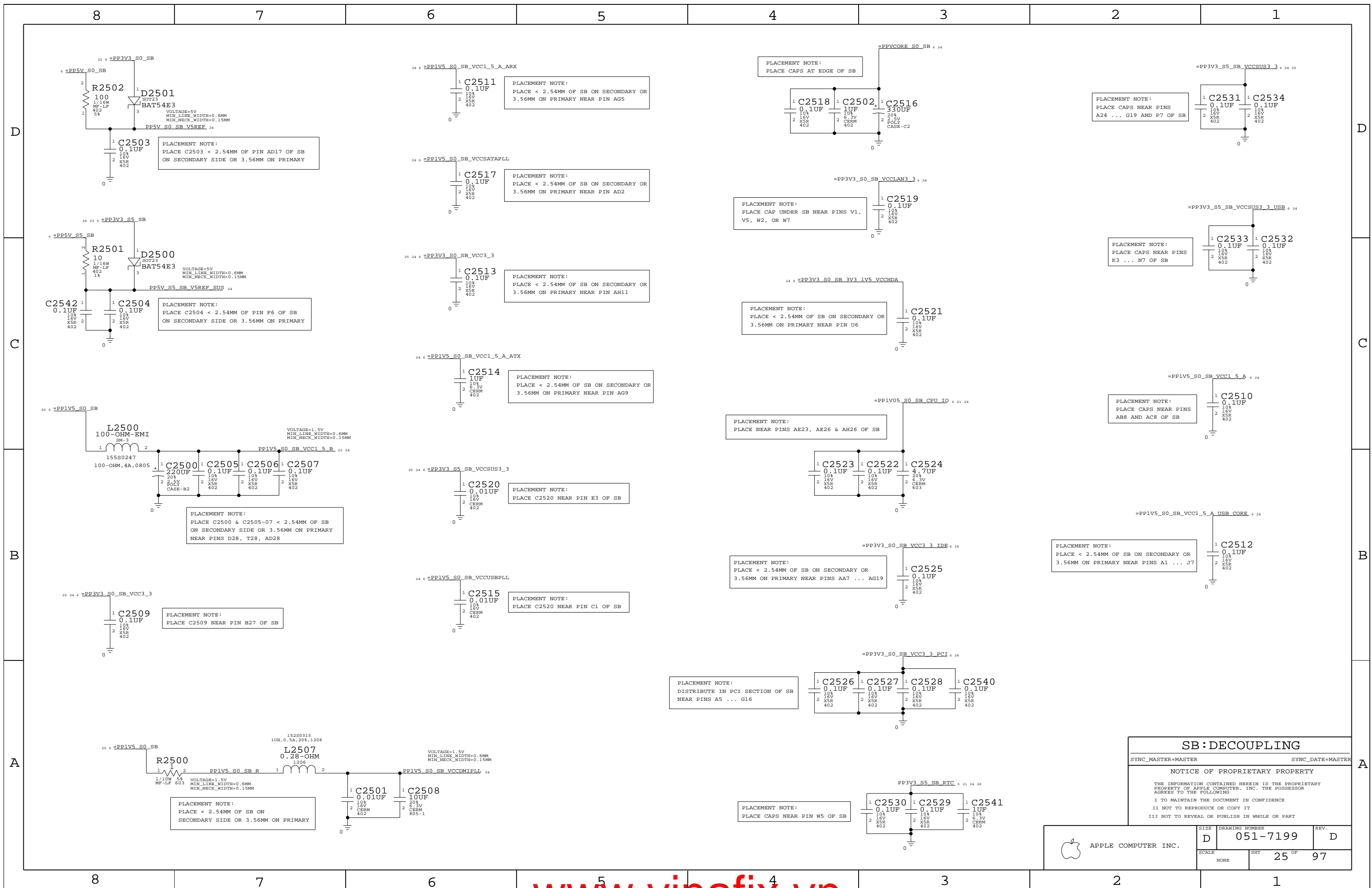
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	D	051-7199	D
SCALE	SHT	REV.	
NONE	24 OF	97	



SB : DECOUPLING

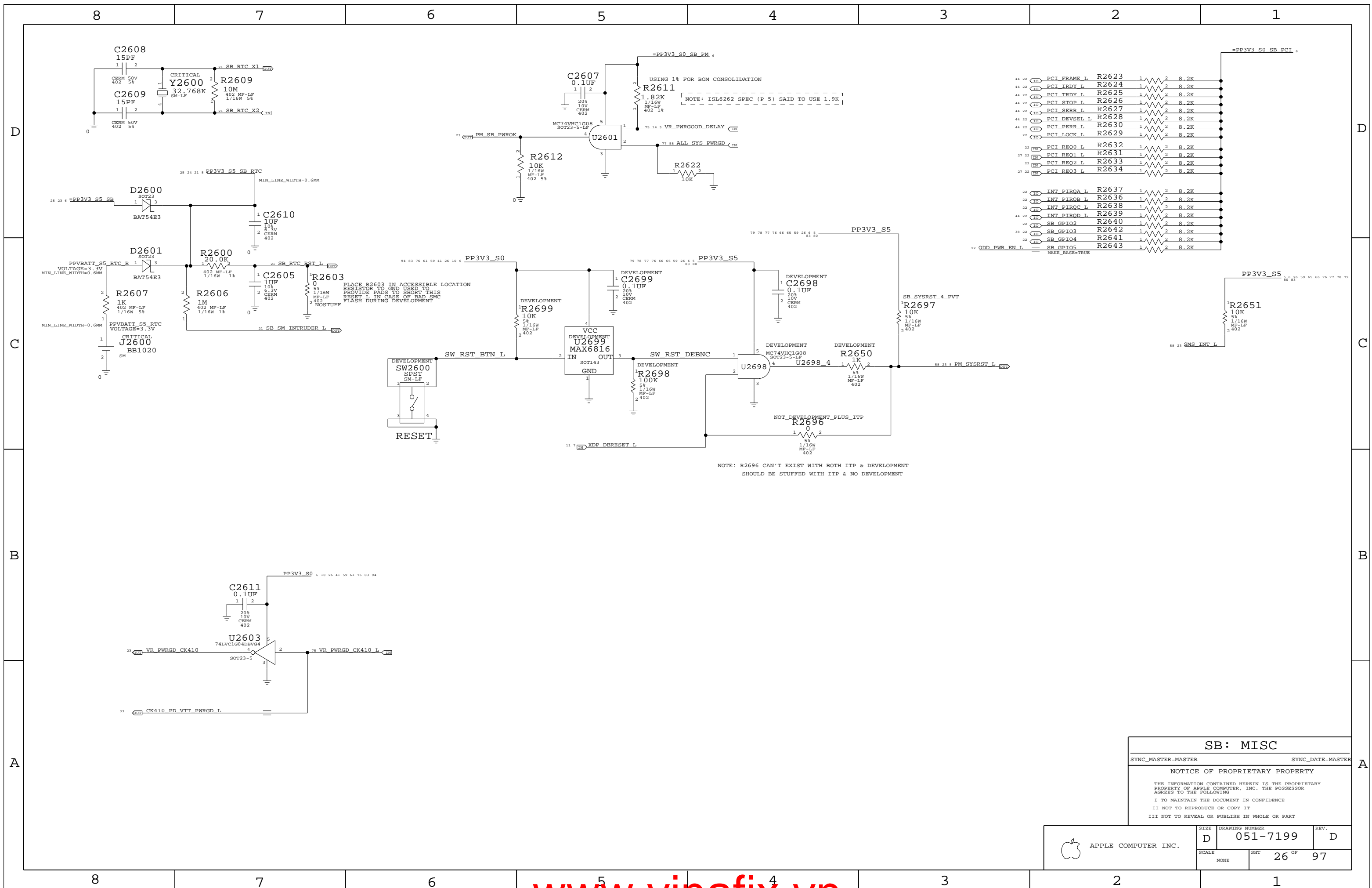
SYNC_MASTER=MASTER SYNC_DATE=MASTER

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	D	051-7199	D
SCALE	SHT	25 OF	97
NONE			



8

7

6

5

4

3

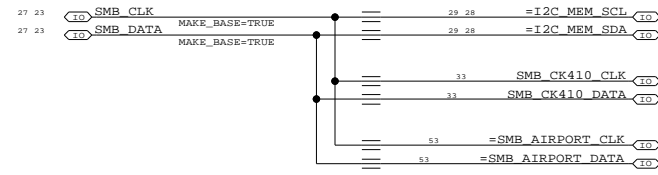
2

1

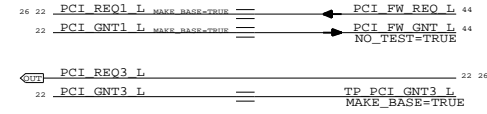
D

D

SB I2C BUSSES

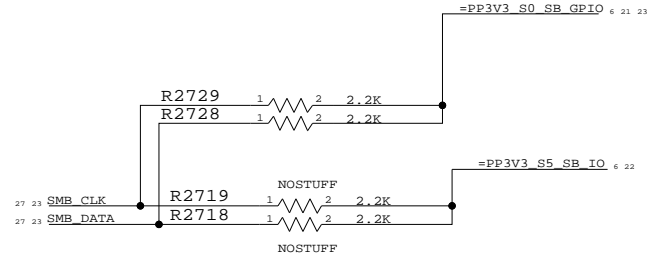


PCI CONTROL



C

C



B

B

A

A

SB: SMB HUB AND ALIAS

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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	D	051-7199	D
SCALE	SHT	27 OF 97	
NONE			

8

7

6

5

4

3

2

1

Page Notes

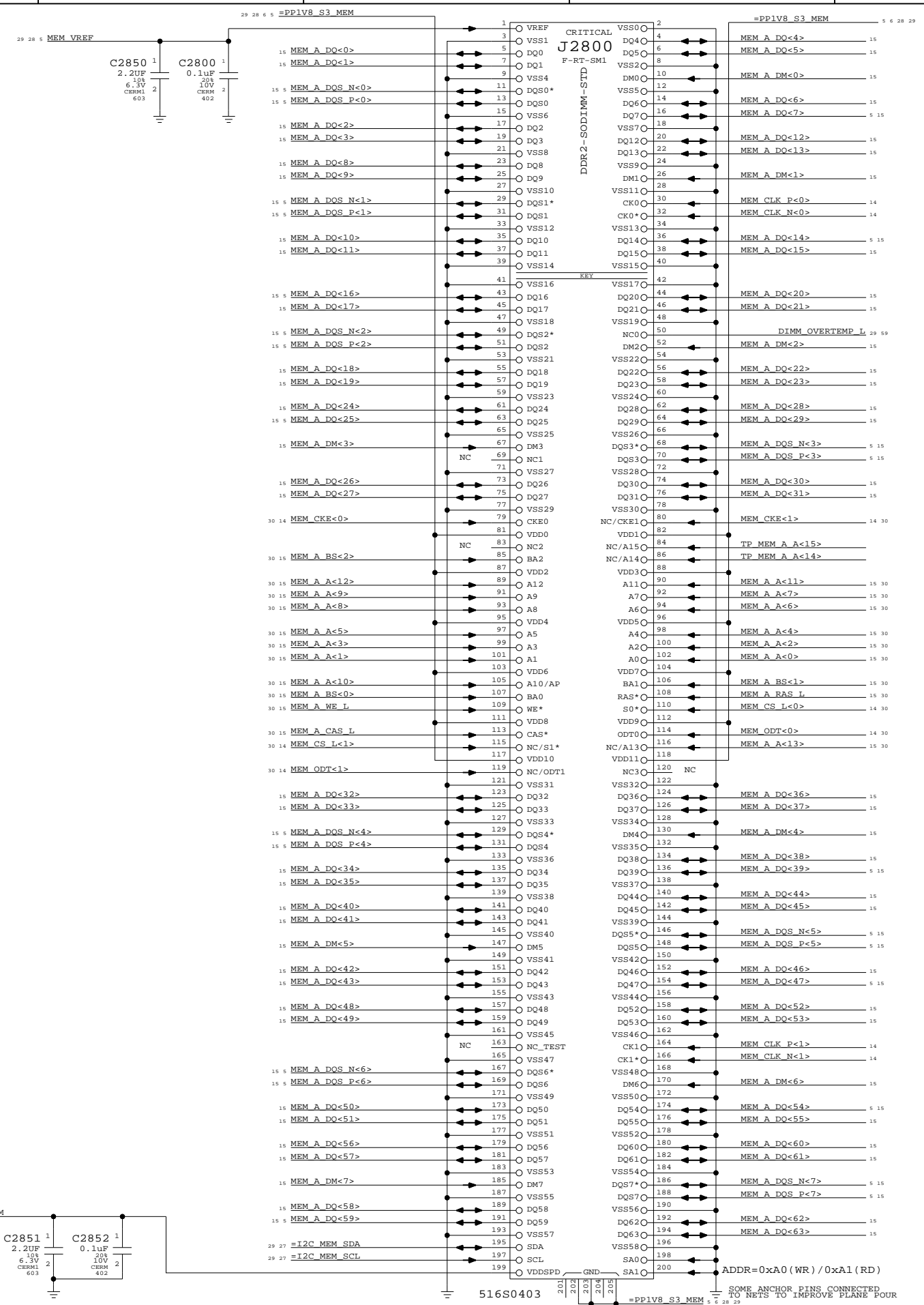
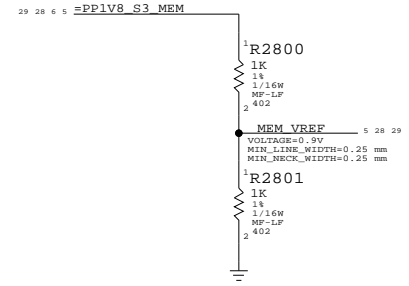
Power aliases required by this page:
- =PPIV8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_MEM_SCL
- =I2C_MEM_SDA

BOM options provided by this page:
(NONE)

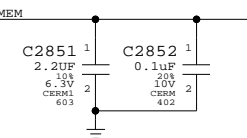
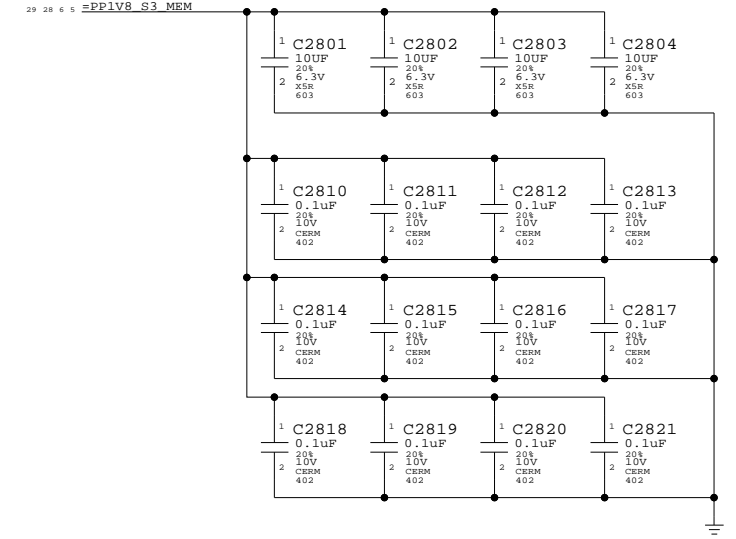
DDR2 VRef

One 0.1uF per connector



DDR2 Bypass Caps

(For return current)



DDR2 SO-DIMM Connector A

SYNC_MASTER=MASTER SYNC_DATE=MASTER

NOTICE OF PROPRIETARY PROPERTY

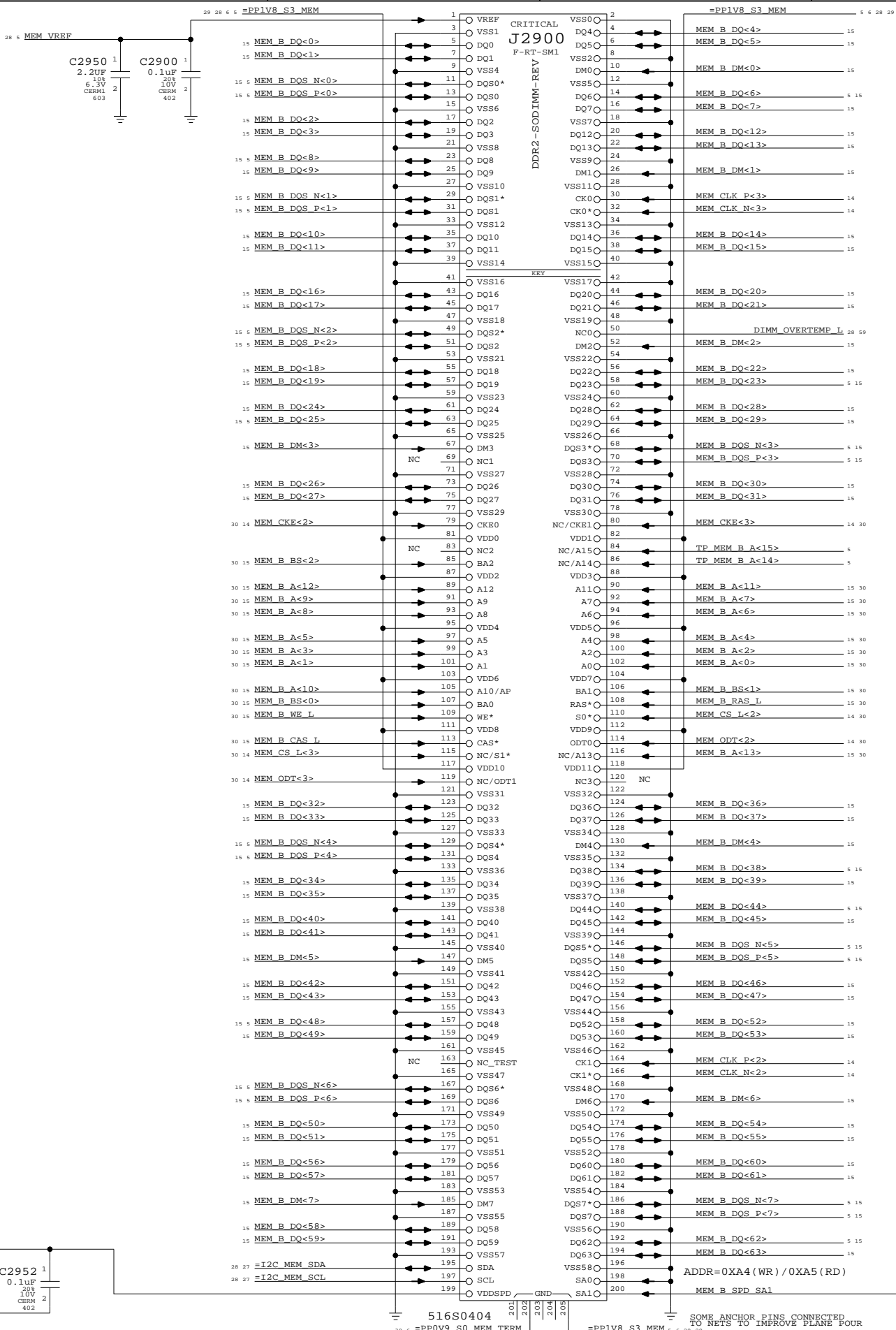
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	D	051-7199	D
SCALE	SHT	28 OF	97
NONE			

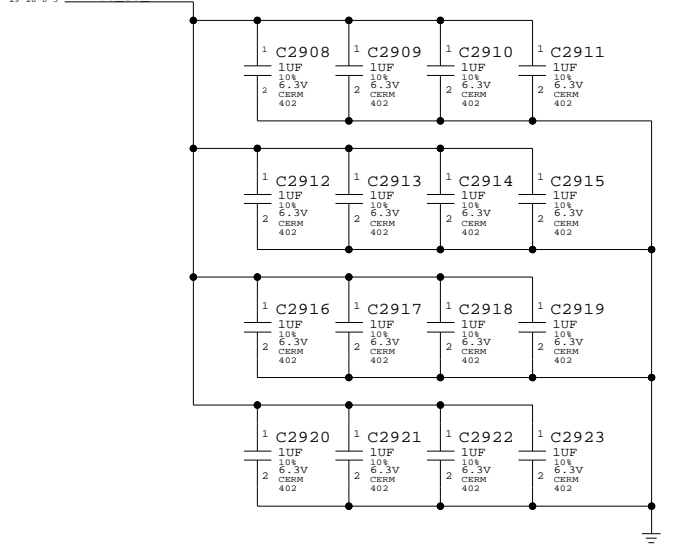
Page Notes

- Power aliases required by this page:
 - =PP1V8_S3_MEM
 - =PPSPD_S0_MEM (2.5V - 3.3V)
- Signal aliases required by this page:
 - =I2C_MEM_SCL
 - =I2C_MEM_SDA
- BOM options provided by this page:
(NONE)
- NOTE: This page does not supply VREF.
The reference voltage must be provided by another page.



DDR2 Bypass Caps

(For return current)



DDR2 SO-DIMM Connector B

SYNC_MASTER=MASTER SYNC_DATE=MASTER

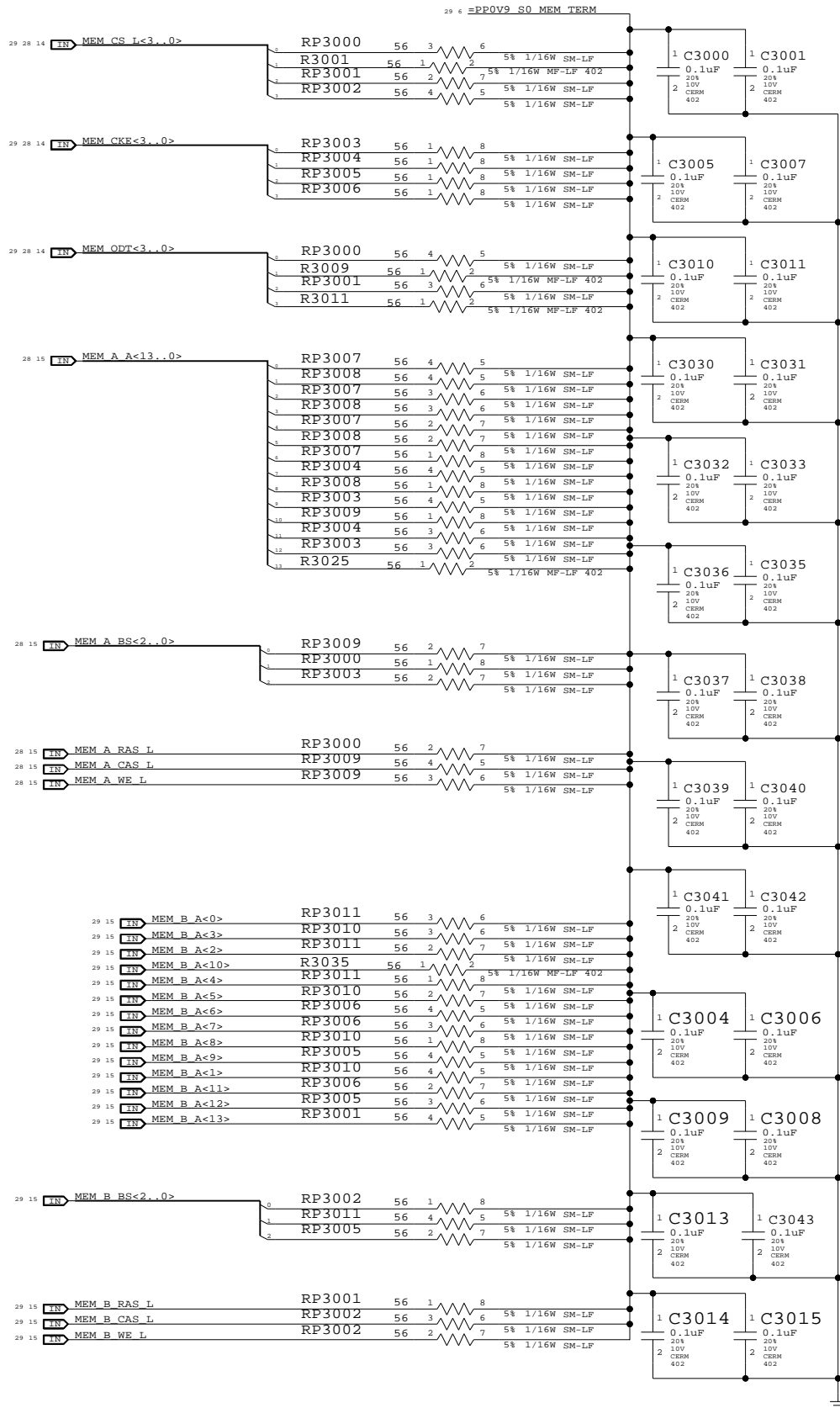
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SCALE NONE	SHEET 29	OF 97	SIZE	DRAWING NUMBER	REV.
			D	051-7199	D

One cap for each side of every RPAK, one cap for every two discrete resistors
BOMOPTION shown at the top of each group applies to every part below it



Memory Active Termination

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	D	051-7199	D
SCALE	SHT	30 OF	97
NONE			

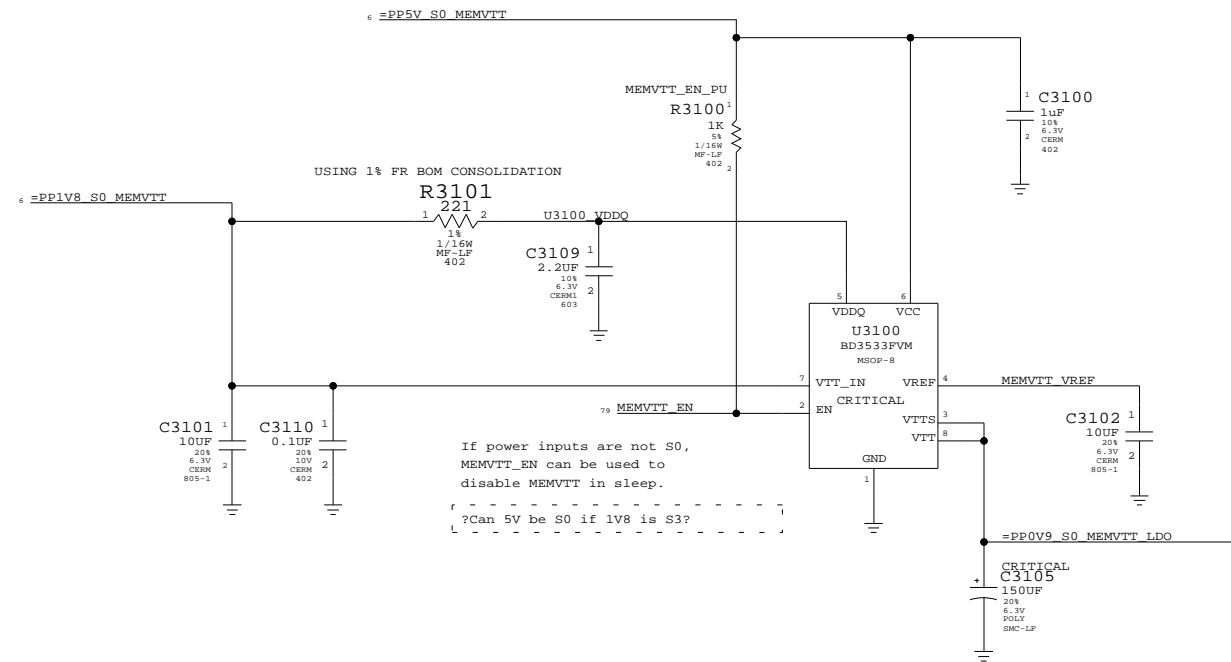
Page Notes

Power aliases required by this page:
 - =PP5V_S0_MEMVTT
 - =PP1V8_S0_MEMVTT
 - =PP0V9_S0_MEMVTT_LDO

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

DDR2 Vtt Regulator



Memory Vtt Supply

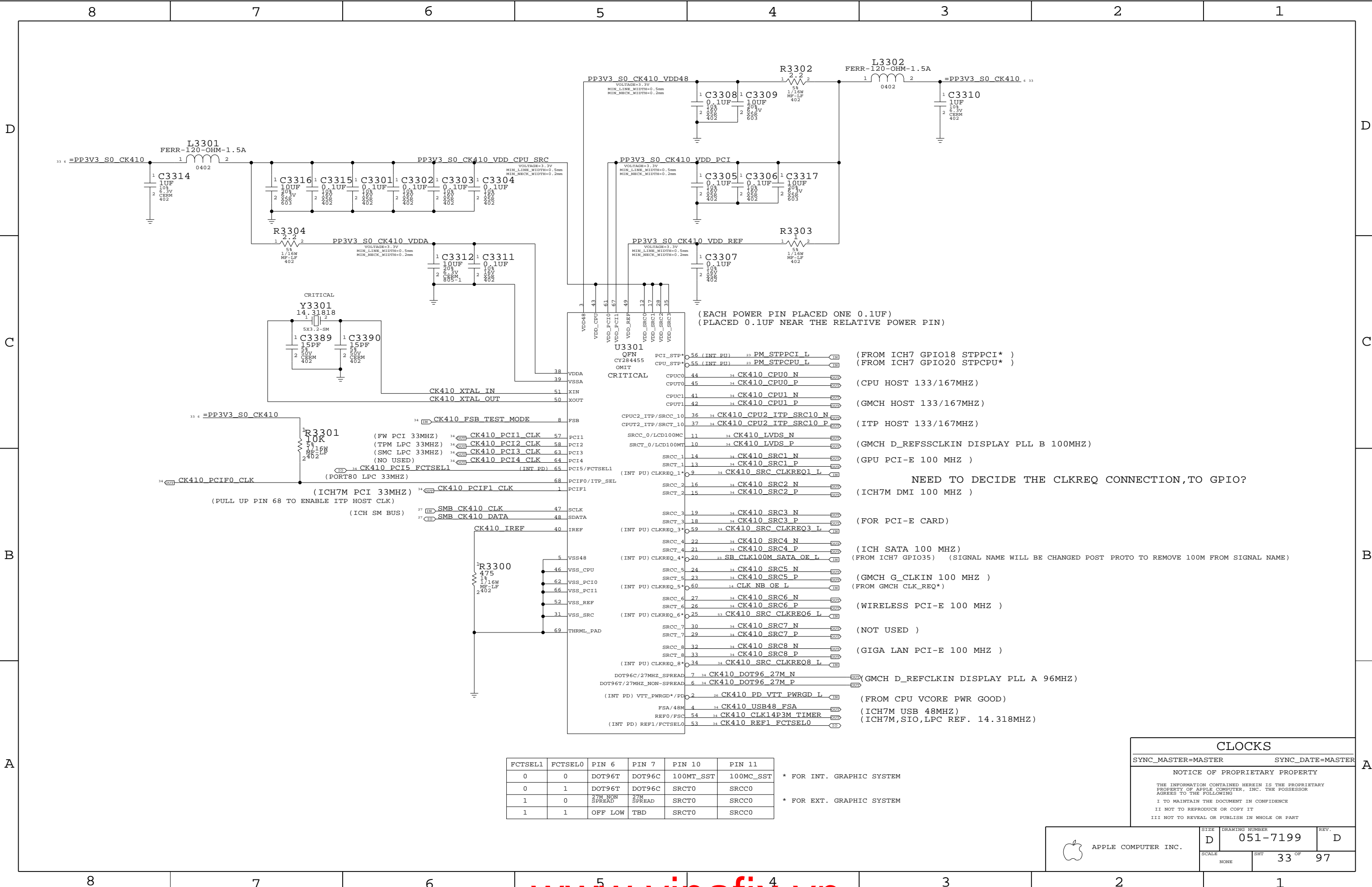
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	D	051-7199	D
SCALE	SHT	31 OF 97	
NONE			



(EACH POWER PIN PLACED ONE 0.1UF)
(PLACED 0.1UF NEAR THE RELATIVE POWER PIN)

- 56 (INT PU) 23 PM_STPPCI_L (FROM ICH7 GPIO18 STPPCI*)
- 55 (INT PU) 23 PM_STPCPU_L (FROM ICH7 GPIO20 STPCPU*)
- 44 34 CK410_CPU0_N (CPU HOST 133/167MHZ)
- 45 34 CK410_CPU0_P
- 41 34 CK410_CPU1_N (GMCH HOST 133/167MHZ)
- 42 34 CK410_CPU1_P
- 36 34 CK410_CPU2_ITP_SRC10_N (ITP HOST 133/167MHZ)
- 37 34 CK410_CPU2_ITP_SRC10_P
- 11 34 CK410_LVDS_N (GMCH D_REFSSCLKIN DISPLAY PLL B 100MHZ)
- 10 34 CK410_LVDS_P
- 14 34 CK410_SRC1_N (GPU PCI-E 100 MHZ)
- 13 34 CK410_SRC1_P
- 9 34 CK410_SRC_CLKREQ1_L (NEED TO DECIDE THE CLKREQ CONNECTION, TO GPIO?)
- 16 34 CK410_SRC2_N (ICH7M DMI 100 MHZ)
- 15 34 CK410_SRC2_P
- 19 34 CK410_SRC3_N (FOR PCI-E CARD)
- 18 34 CK410_SRC3_P
- 59 34 CK410_SRC_CLKREQ3_L (FROM ICH7 GPIO35) (SIGNAL NAME WILL BE CHANGED POST PROTO TO REMOVE 100M FROM SIGNAL NAME)
- 22 34 CK410_SRC4_N (ICH SATA 100 MHZ)
- 21 34 CK410_SRC4_P
- 20 34 SB_CLK100M_SATA_OE_L (FROM GMCH CLK_REQ*)
- 24 34 CK410_SRC5_N (GMCH G_CLKIN 100 MHZ)
- 23 34 CK410_SRC5_P
- 60 34 CLK_NB_OE_L (FROM GMCH CLK_REQ*)
- 27 34 CK410_SRC6_N (WIRELESS PCI-E 100 MHZ)
- 26 34 CK410_SRC6_P
- 25 34 CK410_SRC_CLKREQ6_L (NOT USED)
- 30 34 CK410_SRC7_N (GIGA LAN PCI-E 100 MHZ)
- 29 34 CK410_SRC7_P
- 32 34 CK410_SRC8_N
- 33 34 CK410_SRC8_P
- 34 34 CK410_SRC_CLKREQ8_L
- 7 34 CK410_DOT96_27M_N (GMCH D_REFCLKIN DISPLAY PLL A 96MHZ)
- 6 34 CK410_DOT96_27M_P
- 2 34 CK410_PD_VTT_PWRGD_L (FROM CPU VCORE PWR GOOD)
- 4 34 CK410_USB48_FSA (ICH7M USB 48MHZ)
- 54 34 CK410_CLK14P3M_TIMER (ICH7M, SIO, LPC REF. 14.318MHZ)
- 53 34 CK410_REF1_FCTSELO

(PULL UP PIN 68 TO ENABLE ITP HOST CLK)

FCTSEL1	FCTSELO	PIN 6	PIN 7	PIN 10	PIN 11
0	0	DOT96T	DOT96C	100MT_SST	100MC_SST
0	1	DOT96T	DOT96C	SRCT0	SRCC0
1	0	27M_NON_SPREAD	27M_SPREAD	SRCT0	SRCC0
1	1	OFF_LOW	TBD	SRCT0	SRCC0

* FOR INT. GRAPHIC SYSTEM

* FOR EXT. GRAPHIC SYSTEM

CLOCKS

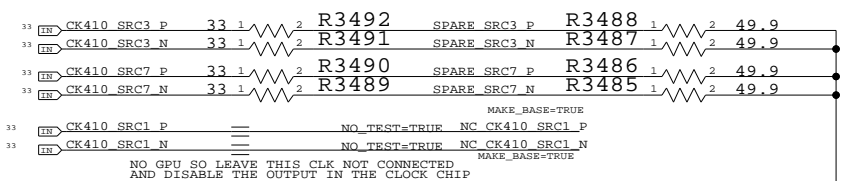
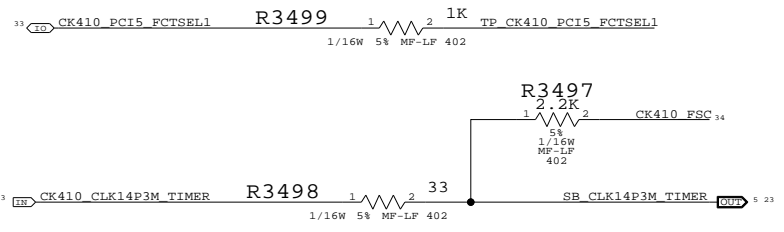
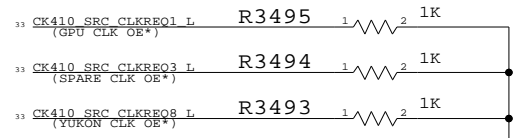
SYNC_MASTER=MASTER SYNC_DATE=MASTER

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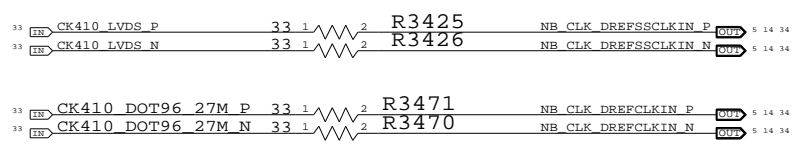
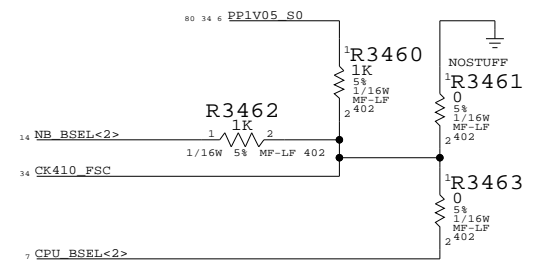
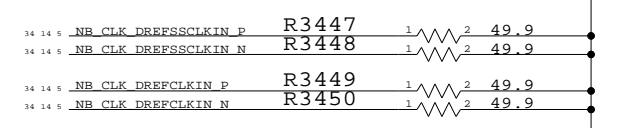
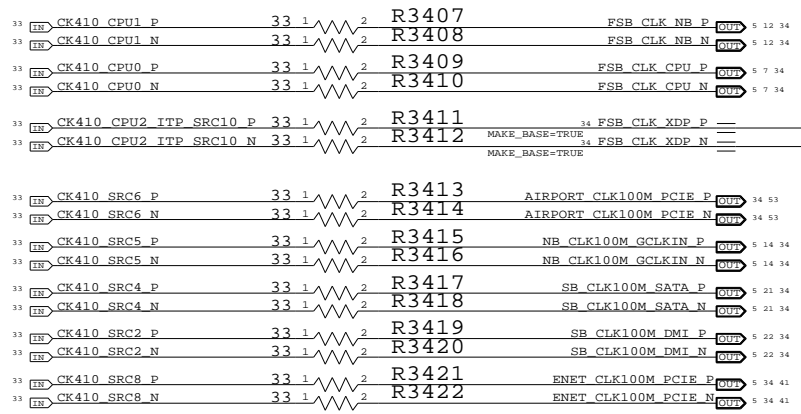
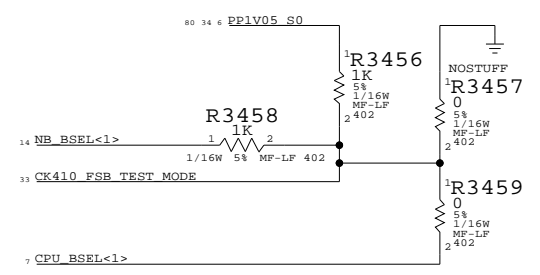
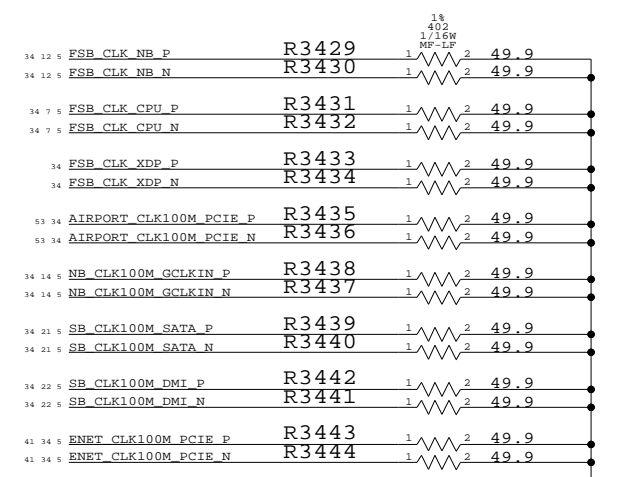
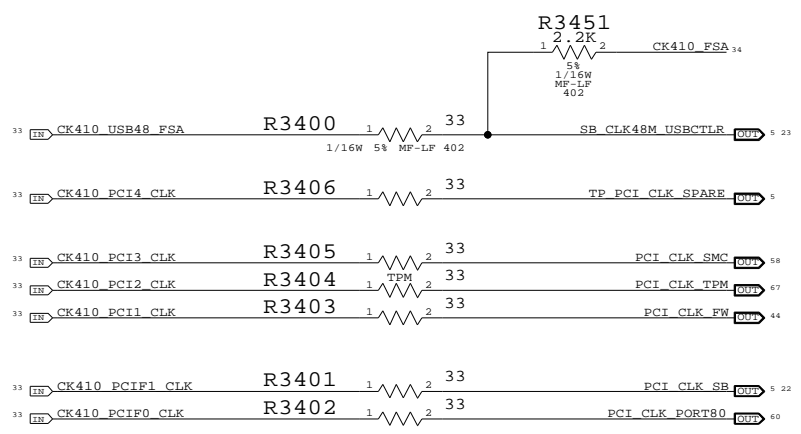
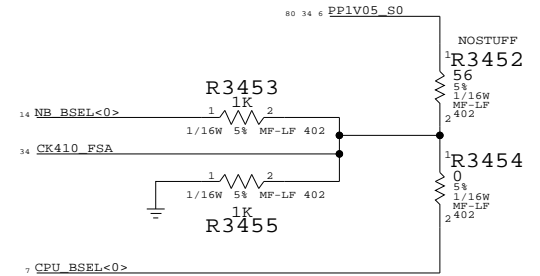
APPLE COMPUTER INC.	DRAWING NUMBER	REV.
	D 051-7199	D
SCALE	SHT	OF
NONE	33	97

NOTE: USE THESE PULL-DOWNS IF NOT CONNECTED TO GPIO'S



FSB FREQUENCY SELECT:

	STUFF	NO STUFF
CPU DRIVEN	R3453 R3454 R3455	R3456 R3457
533MHZ (133MHZ CPU CLK)	R3453 R3454 R3455	R3456 R3457
667MHZ (166MHZ CPU CLK)	R3452 R3461	R3458 R3459



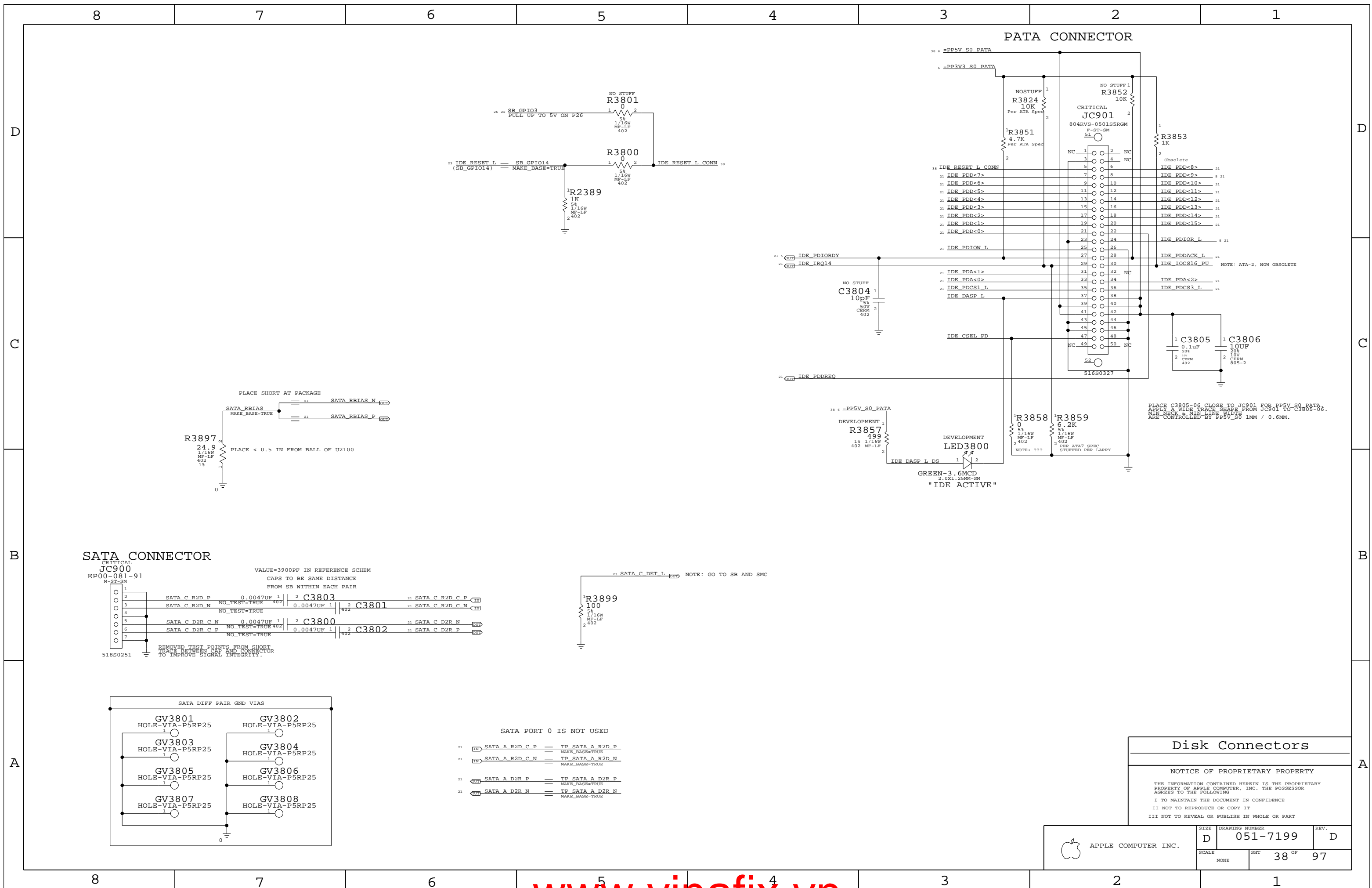
CLOCKS: TERMINATIONS

SYNC_MASTER=MASTER SYNC_DATE=MASTER

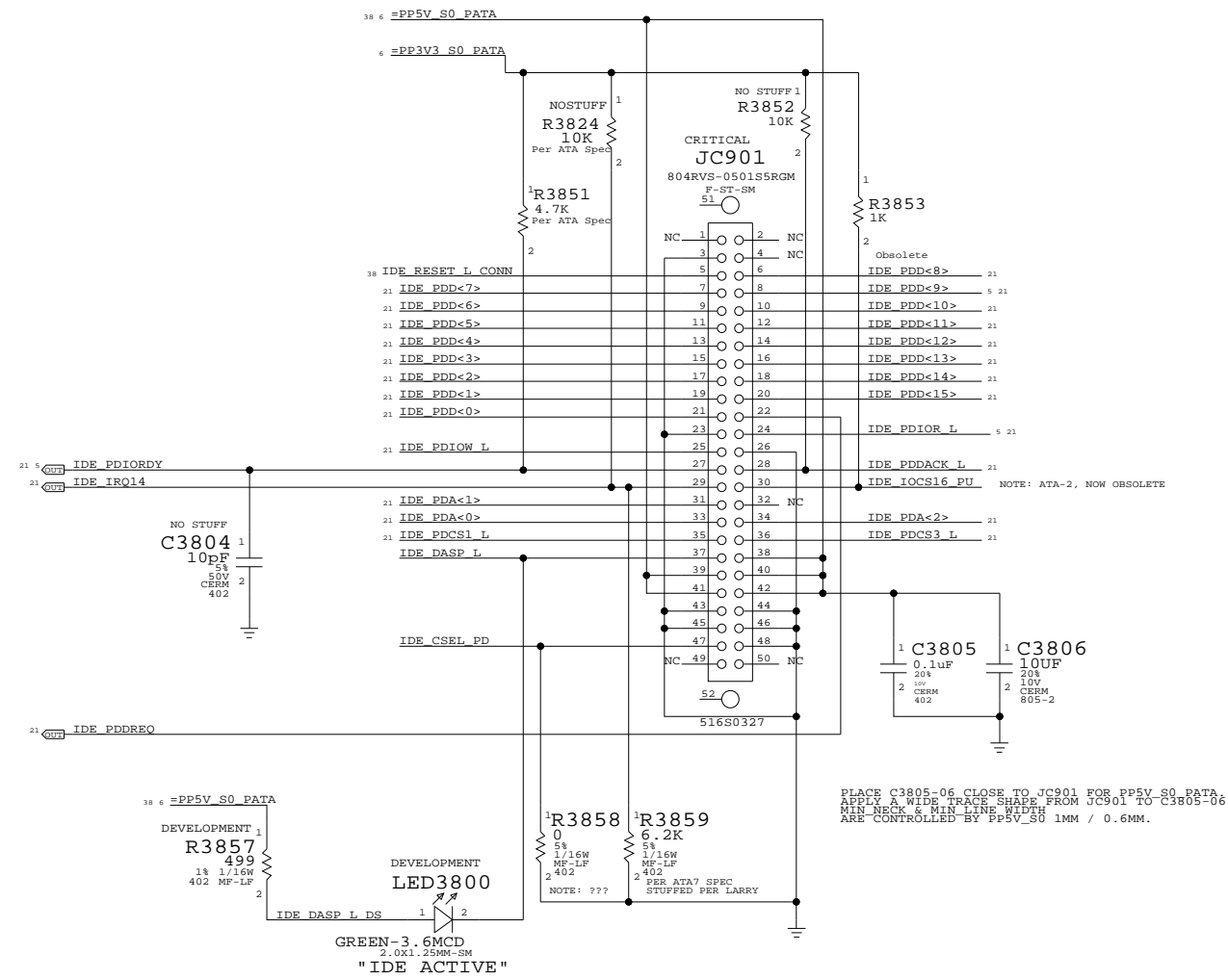
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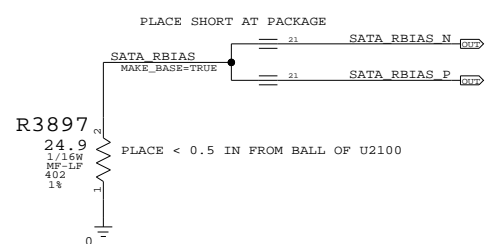
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	D
SCALE	SHT	34 OF	97
NONE			



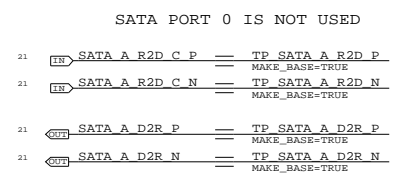
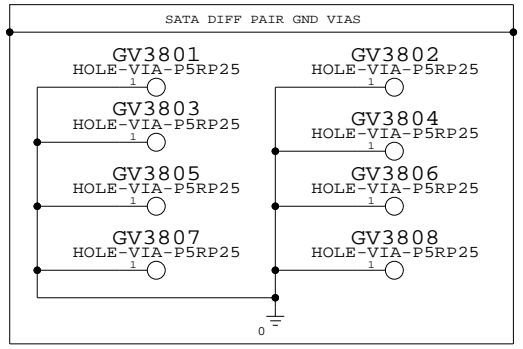
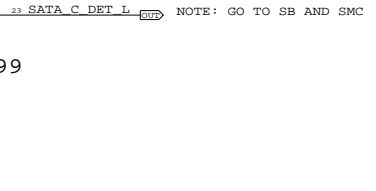
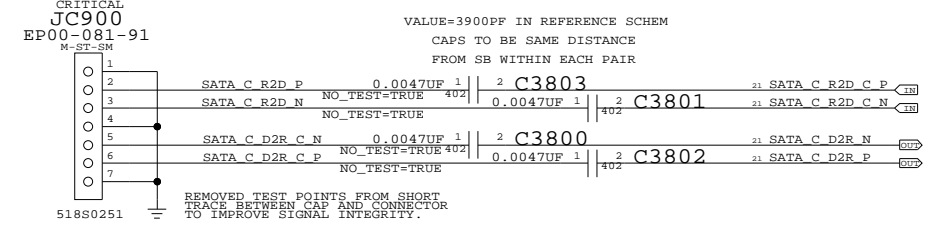
PATA CONNECTOR



PLACE C3805-06 CLOSE TO JC901 FOR PP5V_S0_PATA. APPLY A WIDE TRACE SHAPE FROM JC901 TO C3805-06. MIN NECK & MIN LINE WIDTH ARE CONTROLLED BY PP5V_S0 1MM / 0.6MM.



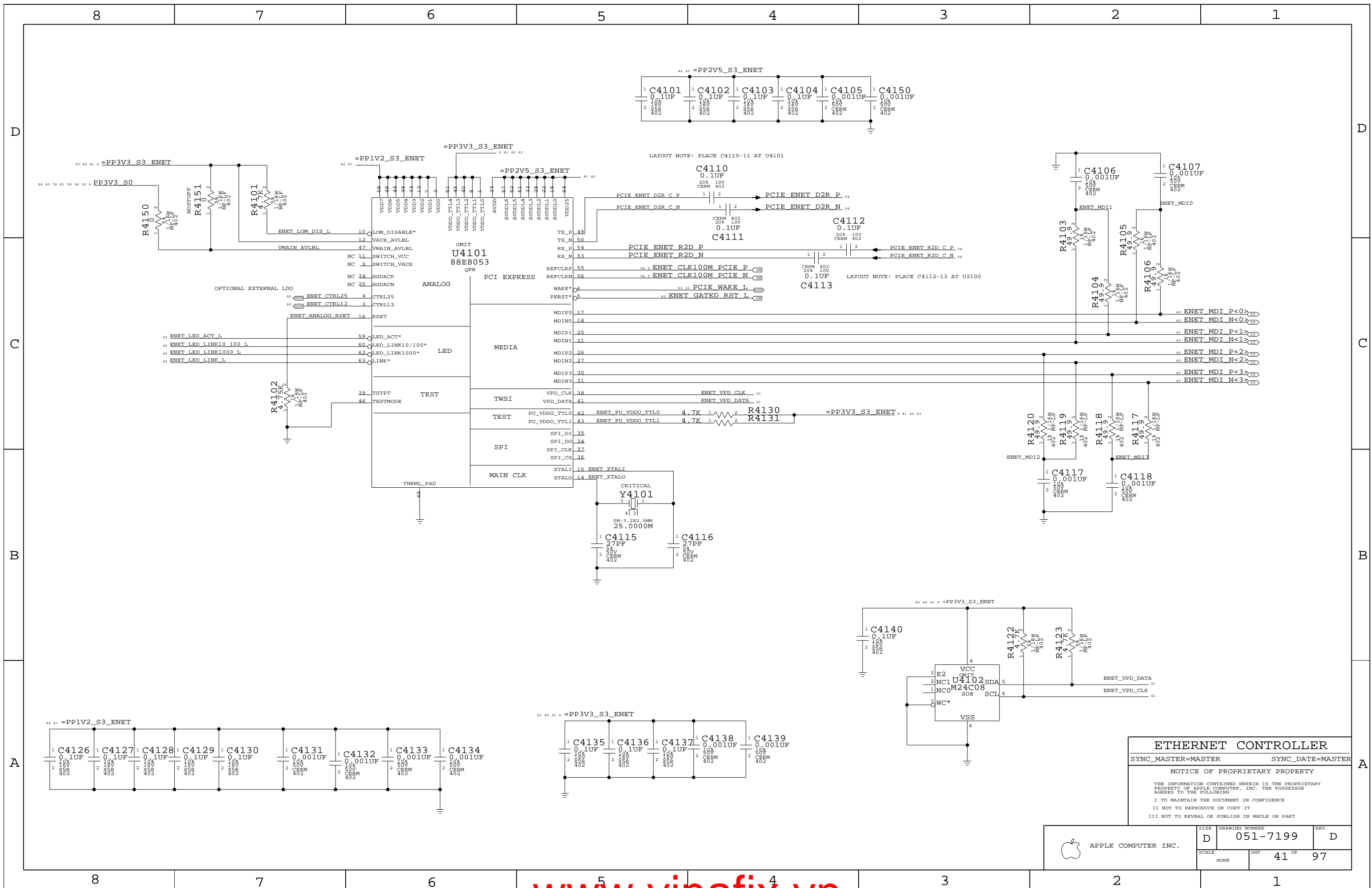
SATA CONNECTOR



Disk Connectors

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	D	051-7199	D
SCALE	SHT	38 OF	97
NONE			



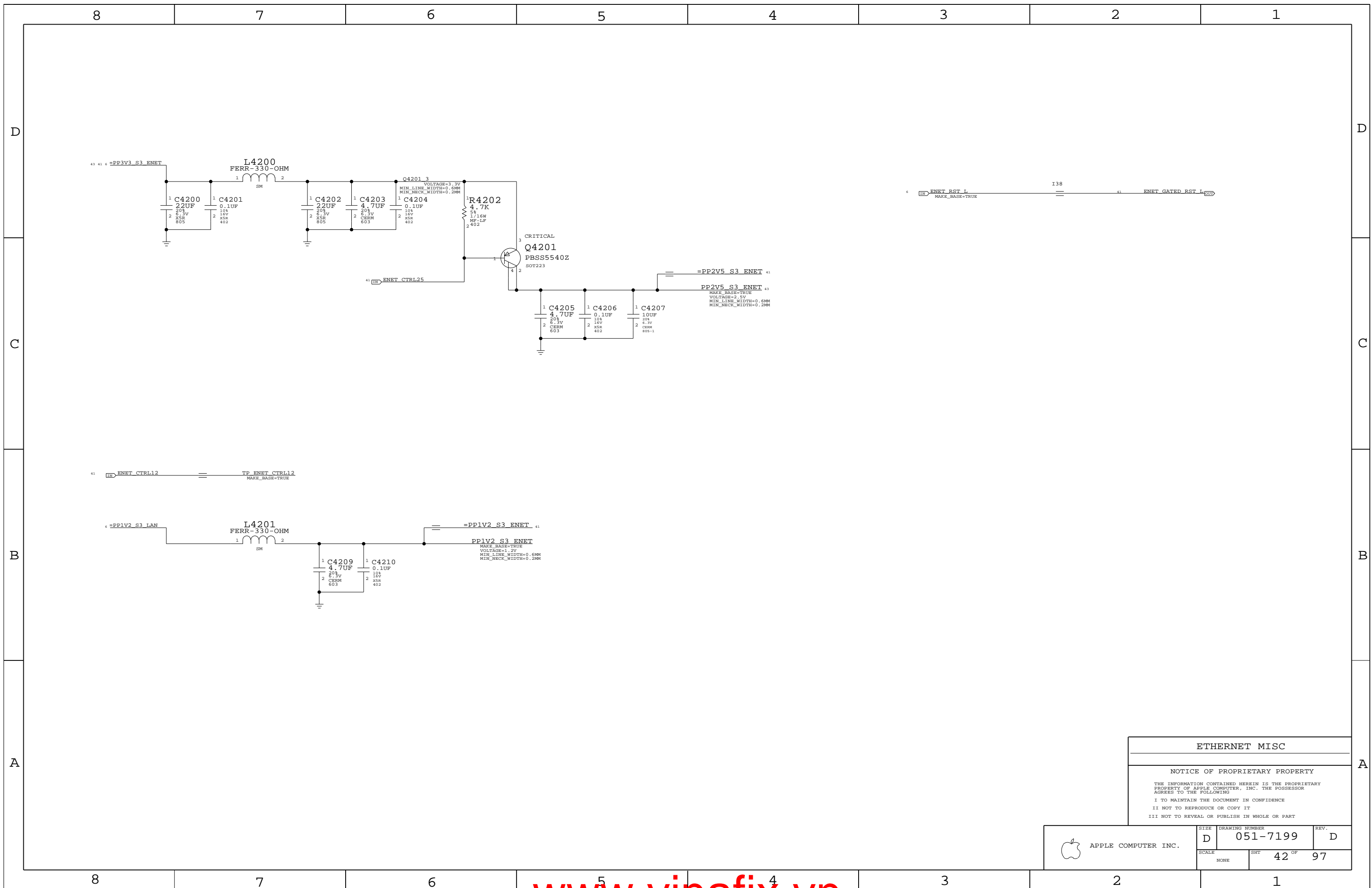
ETHERNET CONTROLLER

SYNC_MASTER=MASTER SYNC_DATA=MASTER

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	D	051-7199	D
SCALE	SHT	41 OF 97	
NONE			



ETHERNET MISC

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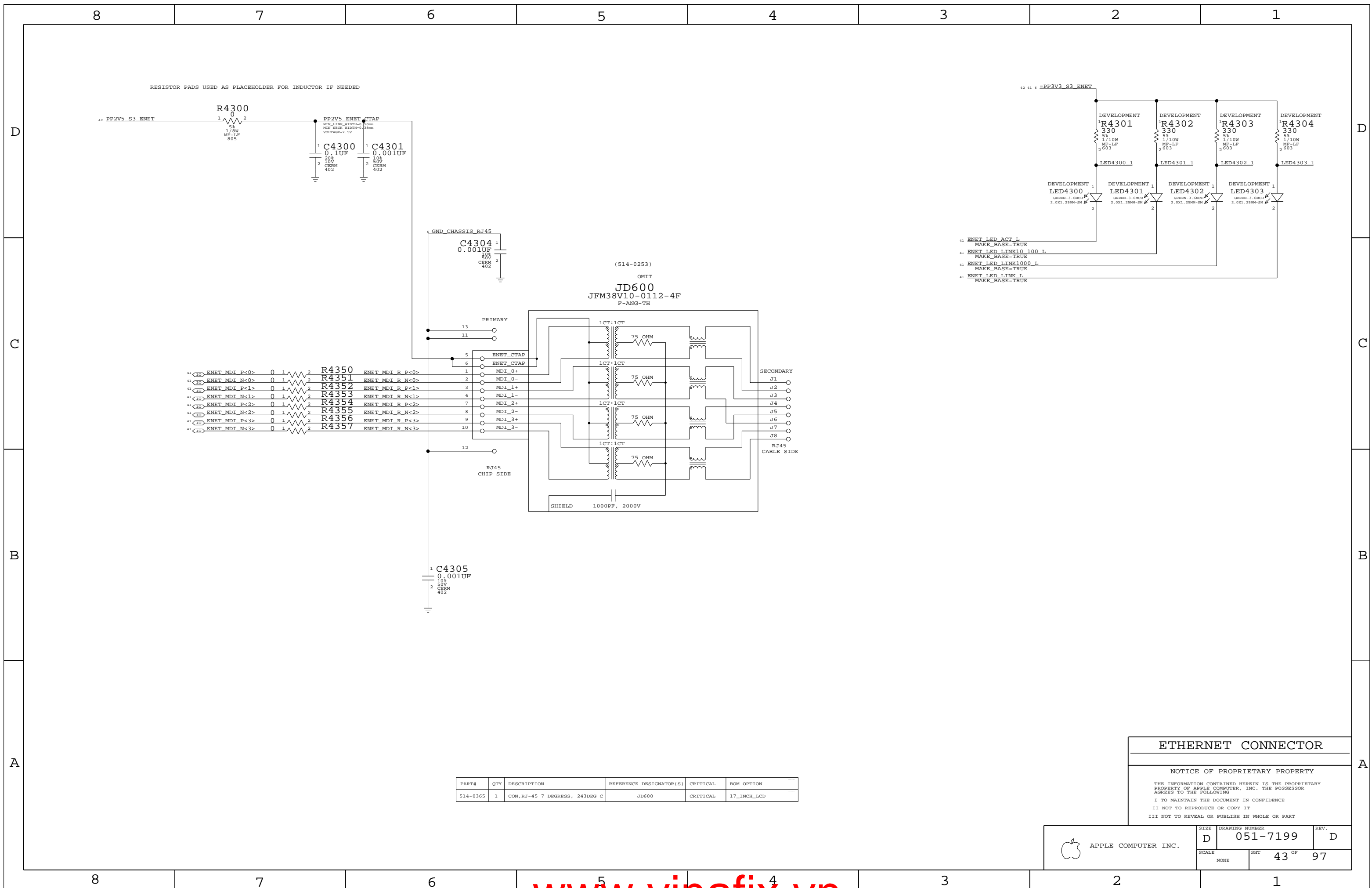
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7199	REV. D
	SCALE NONE	SHT 42 OF 97	



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0365	1	CON,RJ-45 7 DEGRESS, 243DEG C	JD600	CRITICAL	17_INCH_LCD

ETHERNET CONNECTOR

NOTICE OF PROPRIETARY PROPERTY

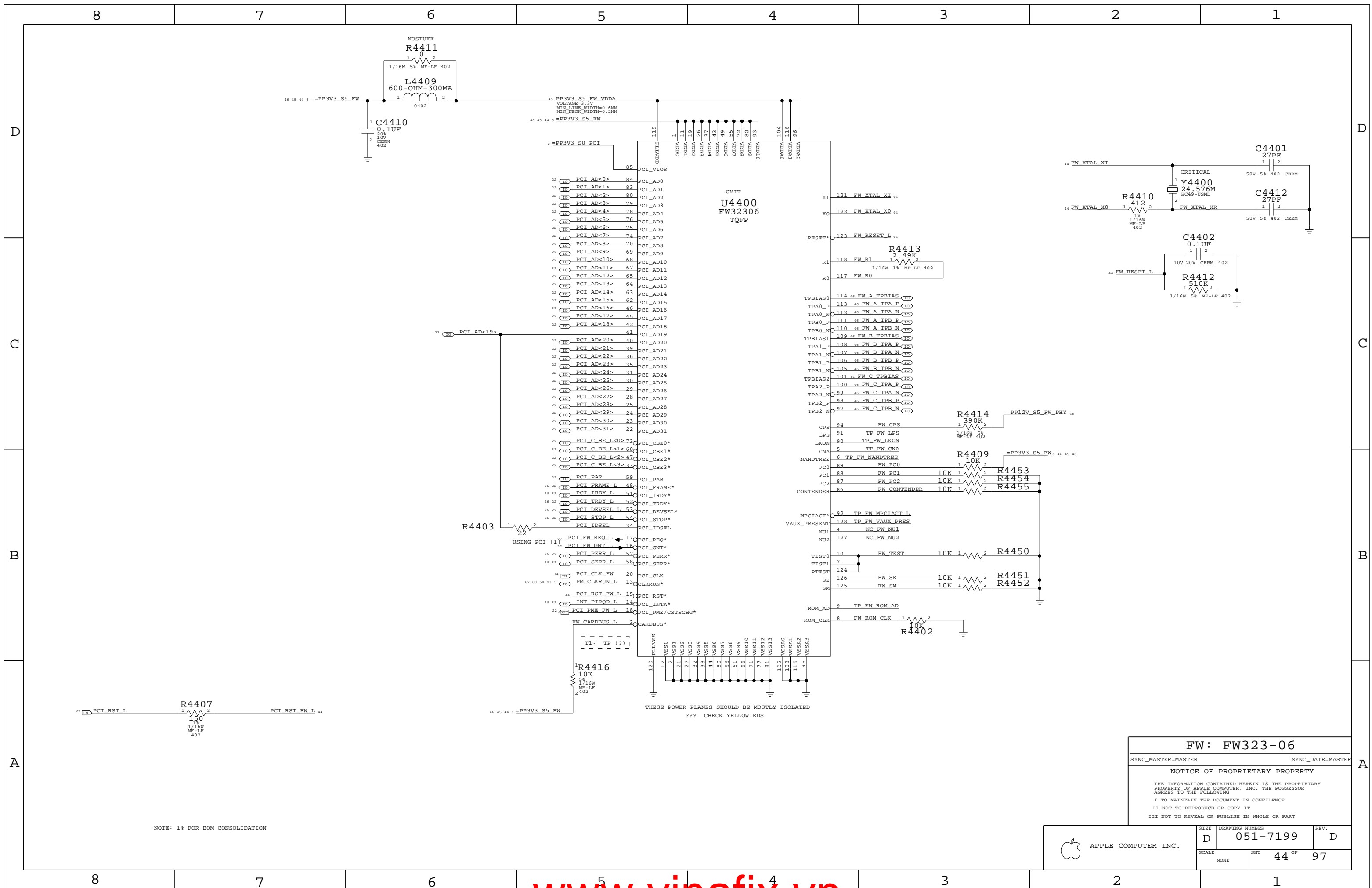
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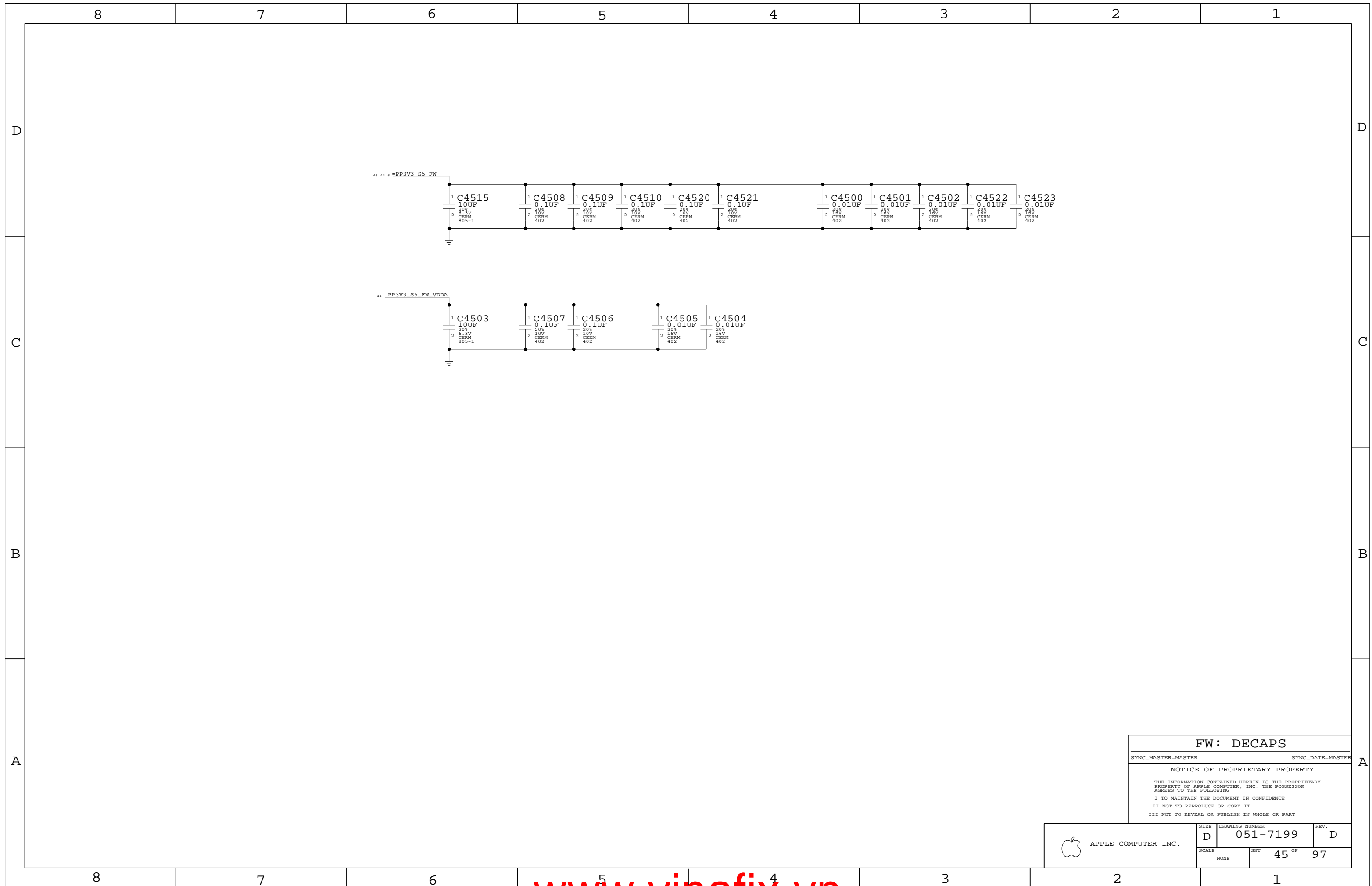
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	D
SCALE	SHT	43 OF 97	
NONE			



NOTE: 1% FOR BOM CONSOLIDATION

FW: FW323-06
 SYNC_MASTER=MASTER SYNC_DATE=MASTER
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	D
SCALE	SHT	44 OF	97
NONE			



FW: DECAPS

SYNC_MASTER=MASTER SYNC_DATE=MASTER

NOTICE OF PROPRIETARY PROPERTY

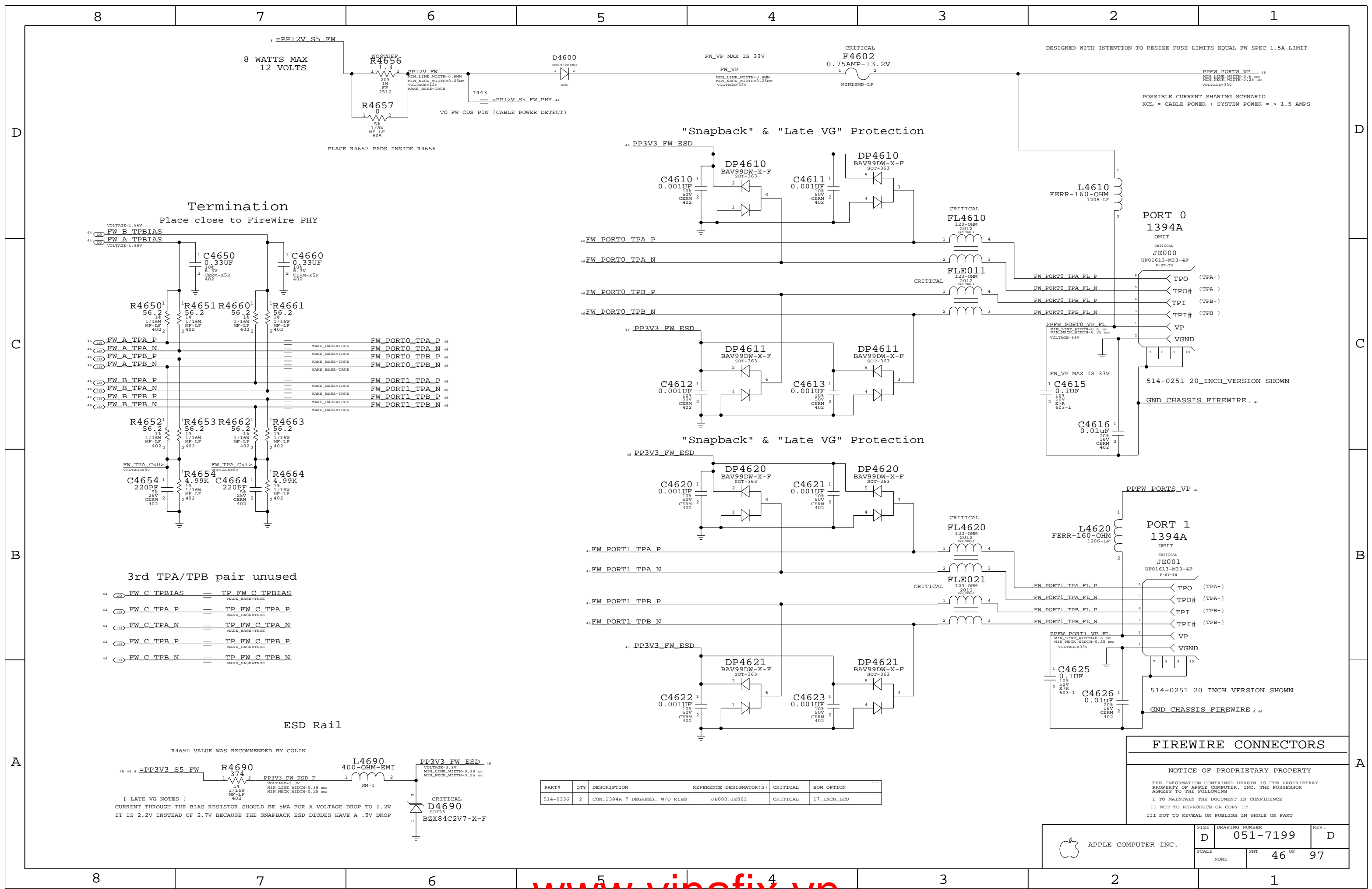
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7199	REV. D
	SCALE NONE	SHIT 45 OF 97	



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0336	2	CON,1394A 7 DEGREES, W/O RIBS	JE000,JE001	CRITICAL	17_INCH_LCD

FIREWIRE CONNECTORS

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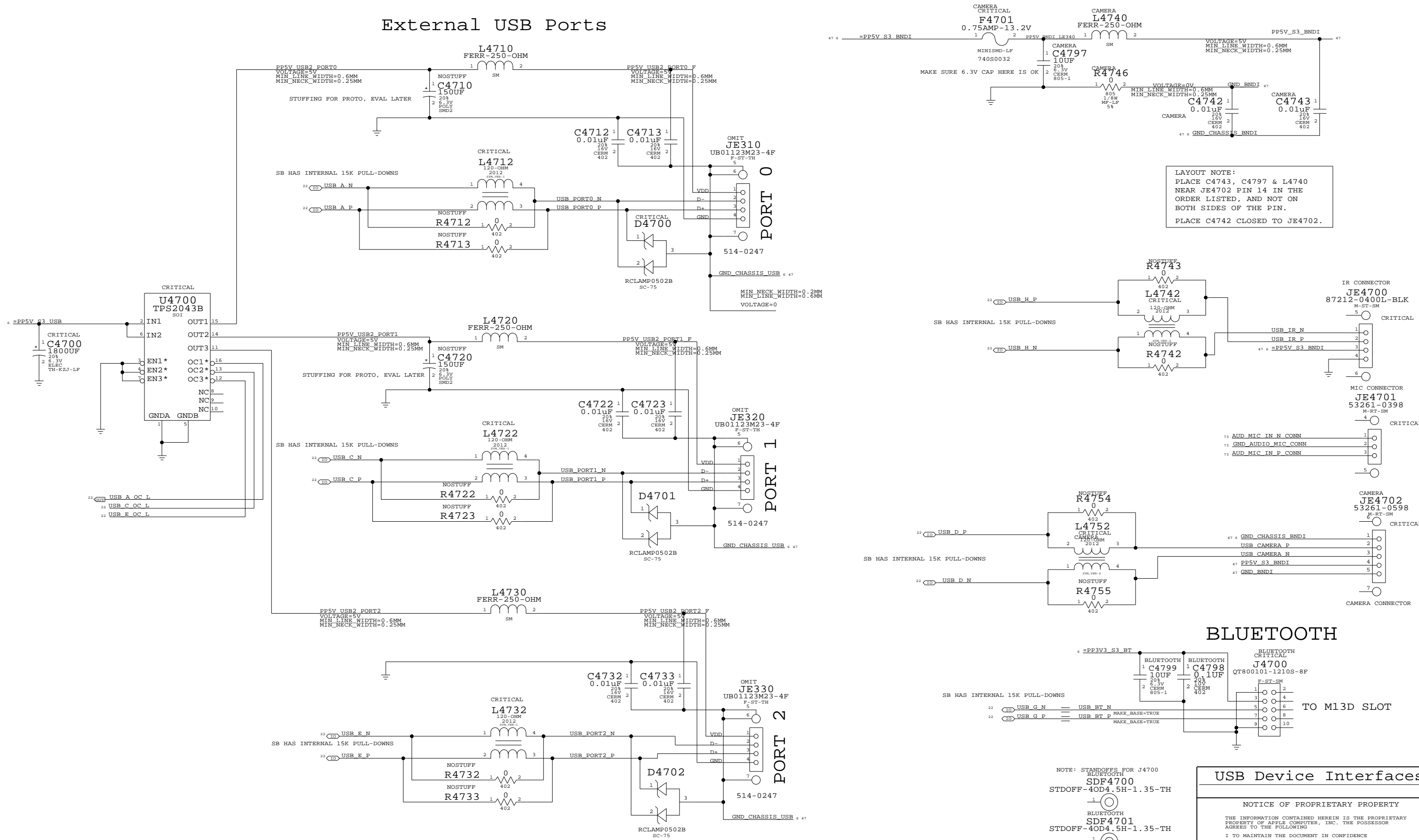
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7199	REV. D
	SCALE NONE	SHEET 46 OF 97	

External USB Ports



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0339	3	USB RECEPTACLE, 4P, UB1123-M50-4F	JE310, JE320, JE330	CRITICAL	17_INCH_LCD

USB Device Interfaces

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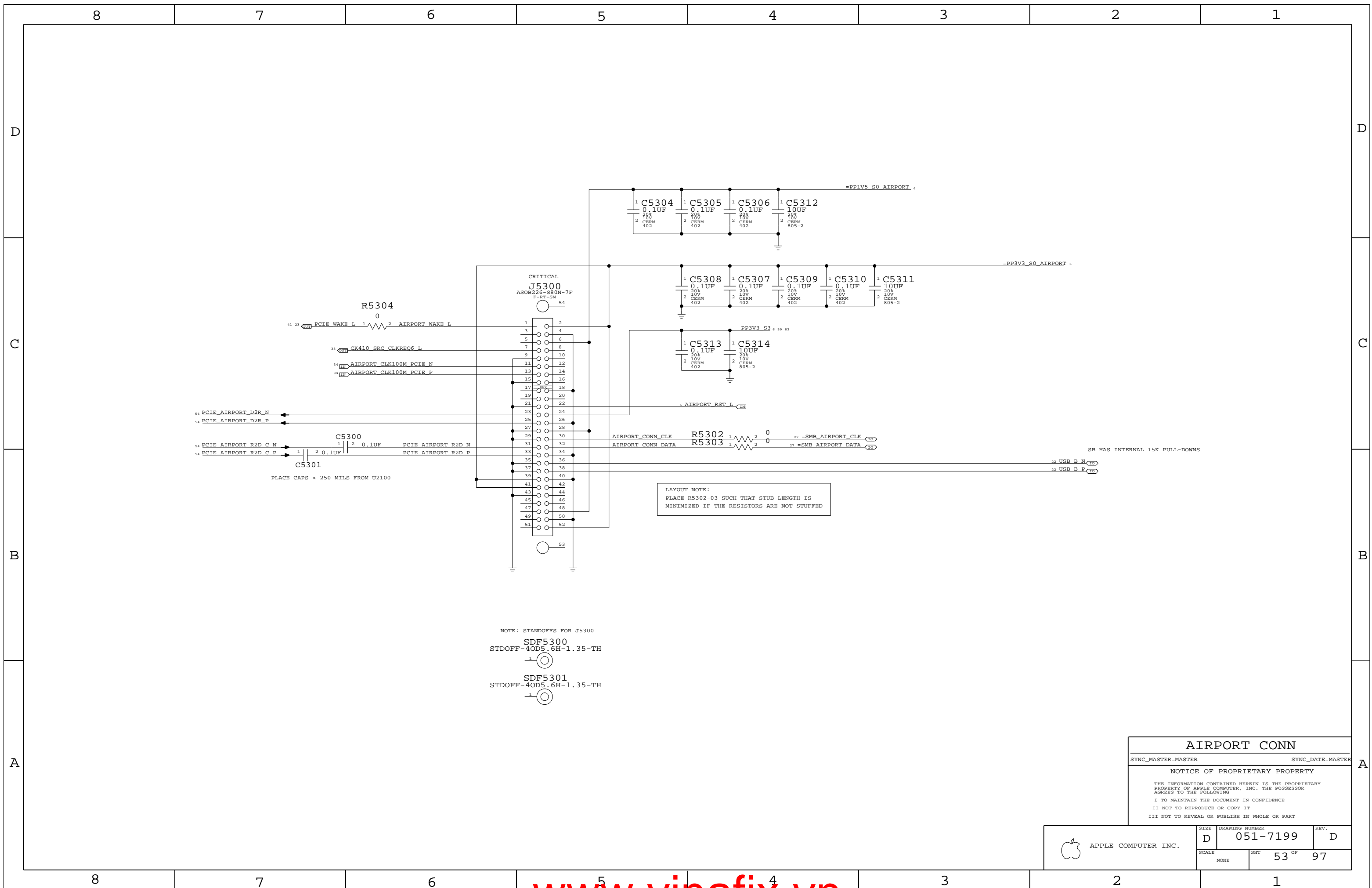
II NOT TO REPRODUCE OR COPY IT

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NOTE: STANDBY FOR J4700 BLUETOOTH SDF4700 STDOFF-40D4.5H-1.35-TH

BLUETOOTH SDF4701 STDOFF-40D4.5H-1.35-TH

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	D
SCALE	SHT	47 OF	97
NONE			



LAYOUT NOTE:
 PLACE R5302-03 SUCH THAT STUB LENGTH IS
 MINIMIZED IF THE RESISTORS ARE NOT STUFFED

NOTE: STANDOFFS FOR J5300
 SDF5300
 STDOFF-40D5.6H-1.35-TH
 SDF5301
 STDOFF-40D5.6H-1.35-TH

SB HAS INTERNAL 15K PULL-DOWNS

PLACE CAPS < 250 MILS FROM U2100

AIRPORT CONN
 SYNC_MASTER=MASTER SYNC_DATE=MASTER
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	D
SCALE	SHT	53 OF 97	
NONE			

8

7

6

5

4

3

2

1

D

D

C

C

B

B

A

A

22 PCIE C R2D C N == TP PCIE C R2D C N
MAKE_BASE=TRUE

22 PCIE C R2D C P == TP PCIE C R2D C P
MAKE_BASE=TRUE

22 PCIE C D2R N == TP PCIE C D2R N
MAKE_BASE=TRUE

22 PCIE C D2R P == TP PCIE C D2R P
MAKE_BASE=TRUE

22 PCIE D R2D C N == TP PCIE D R2D C N
MAKE_BASE=TRUE

22 PCIE D R2D C P == TP PCIE D R2D C P
MAKE_BASE=TRUE

22 PCIE D D2R N == TP PCIE D D2R N
MAKE_BASE=TRUE

22 PCIE D D2R P == TP PCIE D D2R P
MAKE_BASE=TRUE

22 PCIE E R2D C N == TP PCIE E R2D C N
MAKE_BASE=TRUE

22 PCIE E R2D C P == TP PCIE E R2D C P
MAKE_BASE=TRUE

22 PCIE E D2R N == TP PCIE E D2R N
MAKE_BASE=TRUE

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MAKE_BASE=TRUE

22 PCIE F R2D C N == TP PCIE F R2D C N
MAKE_BASE=TRUE

22 PCIE F R2D C P == TP PCIE F R2D C P
MAKE_BASE=TRUE

22 PCIE F D2R N == TP PCIE F D2R N
MAKE_BASE=TRUE

22 PCIE F D2R P == TP PCIE F D2R P
MAKE_BASE=TRUE

USED PCIE PORTS

22 PCIE A R2D C N == PCIE AIRPORT R2D C N 53
MAKE_BASE=TRUE

22 PCIE A R2D C P == PCIE AIRPORT R2D C P 53
MAKE_BASE=TRUE

22 5 PCIE A D2R N == PCIE AIRPORT D2R N 53
MAKE_BASE=TRUE

22 5 PCIE A D2R P == PCIE AIRPORT D2R P 53
MAKE_BASE=TRUE

22 PCIE B R2D C N == PCIE ENET R2D C N 41
MAKE_BASE=TRUE

22 PCIE B R2D C P == PCIE ENET R2D C P 41
MAKE_BASE=TRUE

22 5 PCIE B D2R N == PCIE ENET D2R N 41
MAKE_BASE=TRUE

22 5 PCIE B D2R P == PCIE ENET D2R P 41
MAKE_BASE=TRUE

PCIE PORT ALIASES

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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	D	051-7199	D
SCALE	SHT	54 OF 97	
NONE			

8

7

6

5

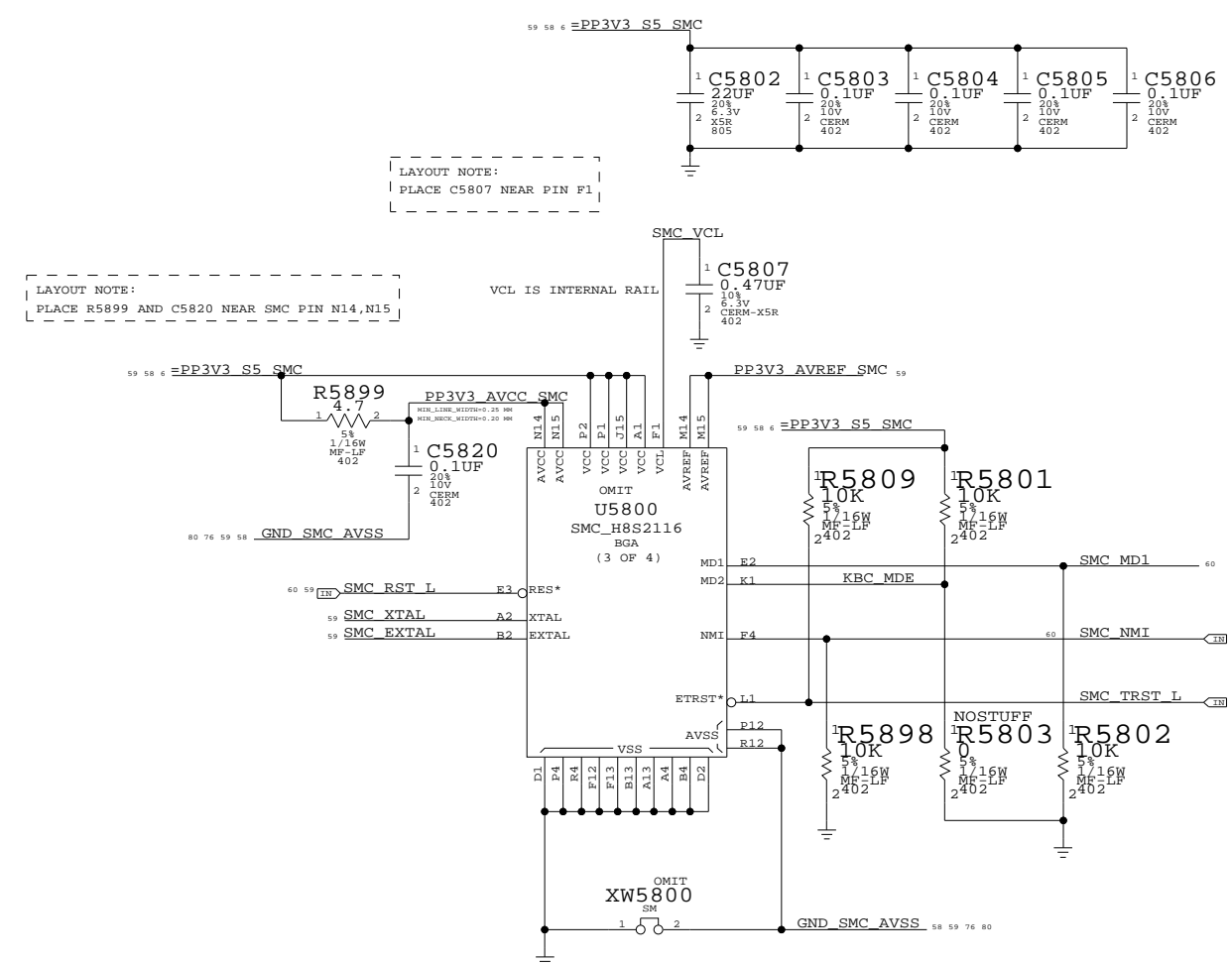
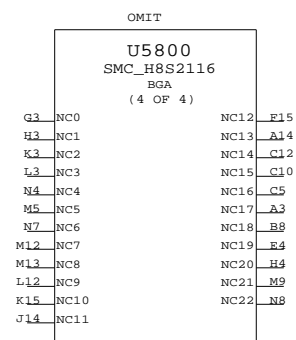
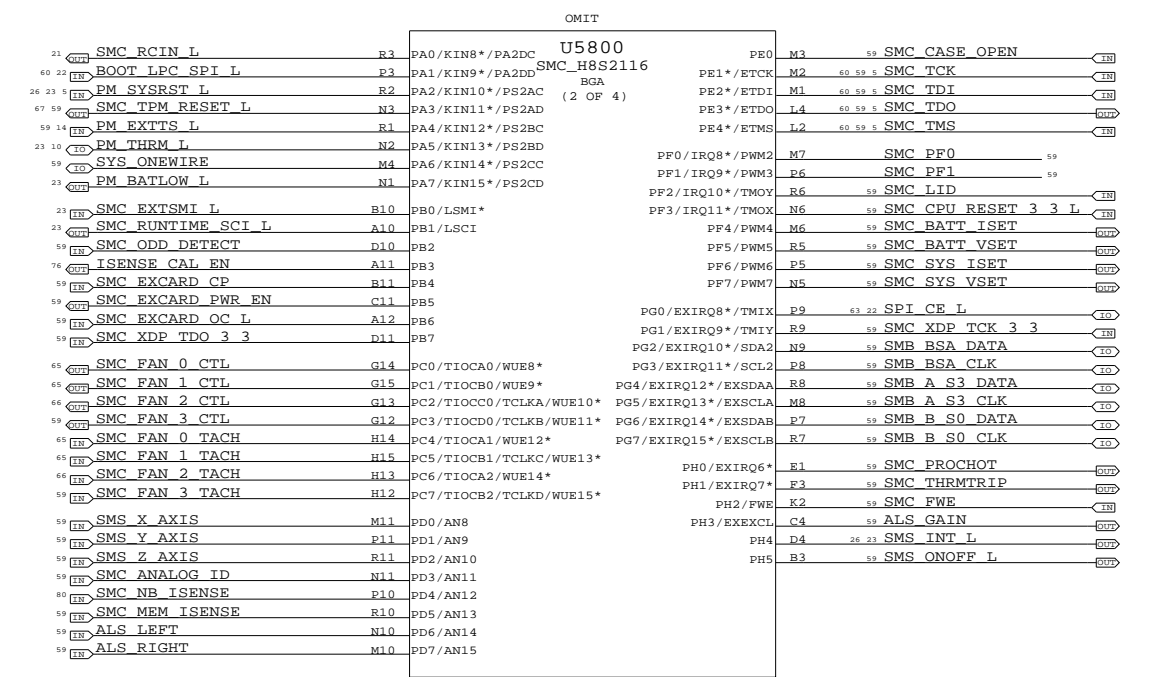
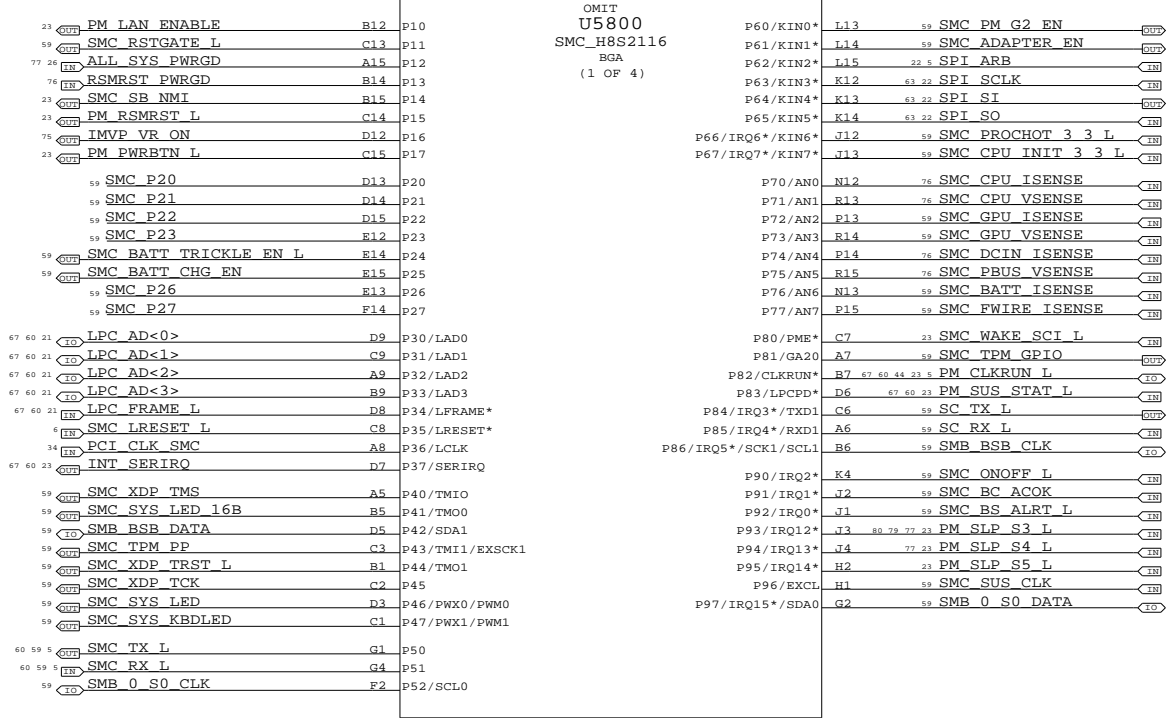
4

3

2

1

UNUSED PINS HAVE THE FORMAT SMC_XXX WHERE XXX IS THE PORT NUMBER. THEY ARE SET BY SOFTWARE TO BE DRIVEN OUTPUTS ALWAYS SO THEY CAN BE LEFT NO-CONNECTED.



SMC

NOTICE OF PROPRIETARY PROPERTY

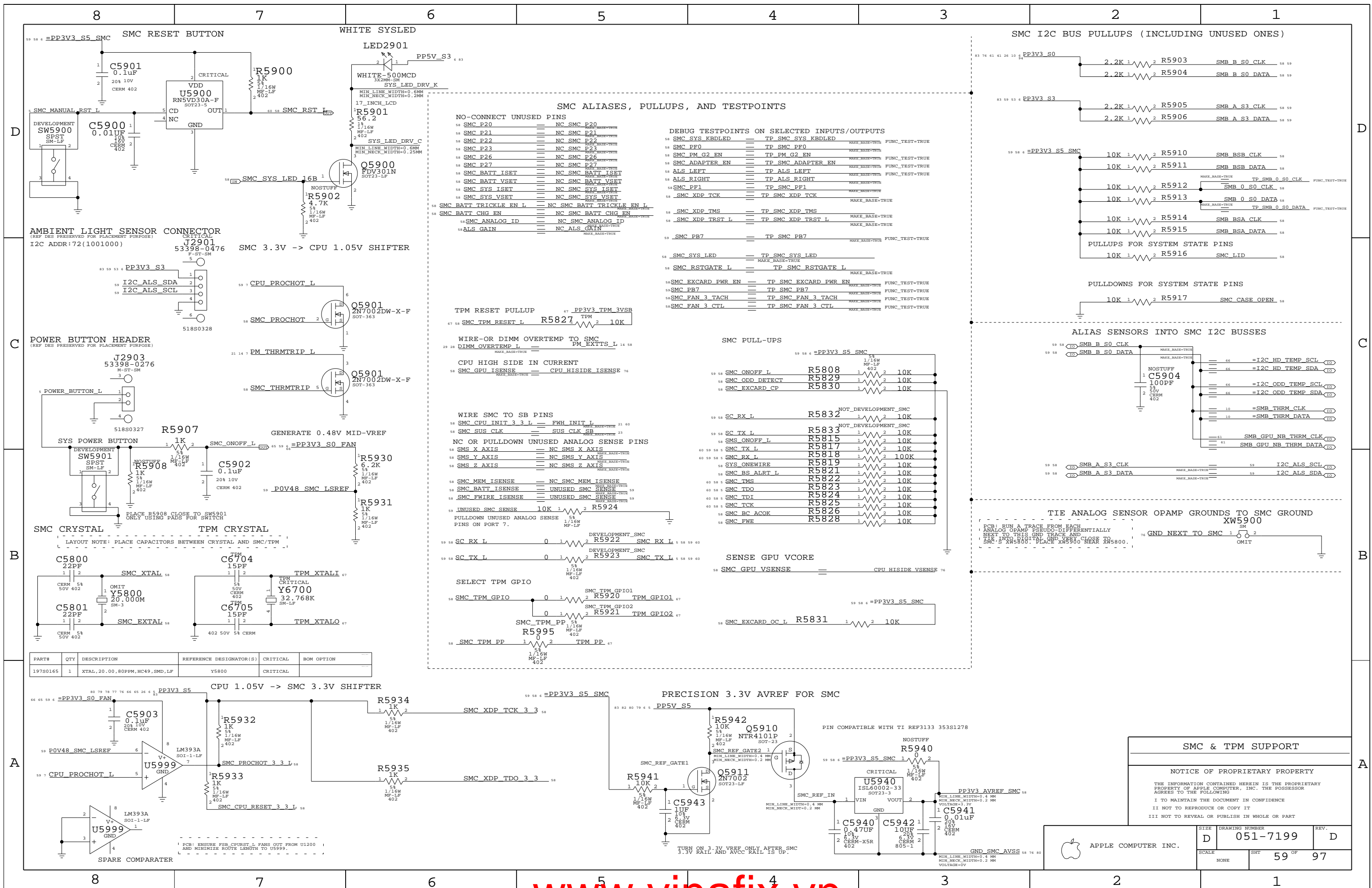
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	D	051-7199	D
SCALE		SHT	REV.
NONE		58 OF	97



SMC ALIASES, PULLUPS, AND TESTPOINTS

NO-CONNECT UNUSED PINS	DEBUG TESTPOINTS ON SELECTED INPUTS/OUTPUTS
58 SMC P20 == NC SMC P20	58 SMC SYS_KBDLED == TP_SMC_SYS_KBDLED MAKE_BASE=TRUE FUNC_TEST=TRUE
58 SMC P21 == NC SMC P21	58 SMC PF0 == TP_SMC_PF0 MAKE_BASE=TRUE
58 SMC P22 == NC SMC P22	58 SMC PM_G2_EN == TP_PM_G2_EN MAKE_BASE=TRUE
58 SMC P23 == NC SMC P23	58 SMC_ADAPTER_EN == TP_SMC_ADAPTER_EN MAKE_BASE=TRUE FUNC_TEST=TRUE
58 SMC P26 == NC SMC P26	58 ALS_LEFT == TP_ALS_LEFT MAKE_BASE=TRUE FUNC_TEST=TRUE
58 SMC P27 == NC SMC P27	58 ALS_RIGHT == TP_ALS_RIGHT MAKE_BASE=TRUE FUNC_TEST=TRUE
58 SMC_BATT_ISET == NC SMC_BATT_ISET	58 SMC_PFI == TP_SMC_PFI MAKE_BASE=TRUE
58 SMC_BATT_VSET == NC SMC_BATT_VSET	58 SMC_XDP_TCK == TP_SMC_XDP_TCK MAKE_BASE=TRUE
58 SMC_SYS_ISET == NC SMC_SYS_ISET	58 SMC_XDP_TMS == TP_SMC_XDP_TMS MAKE_BASE=TRUE
58 SMC_SYS_VSET == NC SMC_SYS_VSET	58 SMC_XDP_TRST_L == TP_SMC_XDP_TRST_L MAKE_BASE=TRUE
58 SMC_BATT_TRICKLE_EN_L == NC SMC_BATT_TRICKLE_EN_L	58 SMC_PB7 == TP_SMC_PB7 MAKE_BASE=TRUE FUNC_TEST=TRUE
58 SMC_BATT_CHG_EN == NC SMC_BATT_CHG_EN	58 SMC_SYS_LED == TP_SMC_SYS_LED MAKE_BASE=TRUE
58 SMC_ANALOG_ID == NC SMC_ANALOG_ID	58 SMC_RSTGATE_L == TP_SMC_RSTGATE_L MAKE_BASE=TRUE
58 ALS_GAIN == NC ALS_GAIN MAKE_BASE=TRUE	58 SMC_EXCARD_PWR_EN == TP_SMC_EXCARD_PWR_EN MAKE_BASE=TRUE FUNC_TEST=TRUE
	58 SMC_PB7 == TP_SMC_PB7 MAKE_BASE=TRUE FUNC_TEST=TRUE
	58 SMC_FAN_3_TACH == TP_SMC_FAN_3_TACH MAKE_BASE=TRUE FUNC_TEST=TRUE
	58 SMC_FAN_3_CTL == TP_SMC_FAN_3_CTL MAKE_BASE=TRUE FUNC_TEST=TRUE

SMC PULL-UPS
58 SMC_ONOFF_L == R5808 10K
58 SMC_ODD_DETECT == R5829 10K
58 SMC_EXCARD_CP == R5830 10K
58 SC_RX_L == R5832 10K
58 SC_TX_L == R5833 10K
58 SMS_ONOFF_L == R5815 10K
58 SMC_TX_L == R5817 10K
58 SMC_RX_L == R5818 100K
58 SYS_ONEWIRE == R5819 10K
58 SMC_BS_ALERT_L == R5821 10K
58 SMC_TMS == R5822 10K
58 SMC_TDO == R5823 10K
58 SMC_TDI == R5824 10K
58 SMC_TCK == R5825 10K
58 SMC_BC_ACOK == R5826 10K
58 SMC_FWE == R5828 10K

SMC PULL-UPS
58 SMC_GPU_VSENSE == CPU_HISIDE_VSENSE 76
58 SMC_EXCARD_OC_L == R5831 10K

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0165	1	XTAL, 20.00, 80PPM, HC49, SMD, LF	Y5800	CRITICAL	

SMC & TPM SUPPORT

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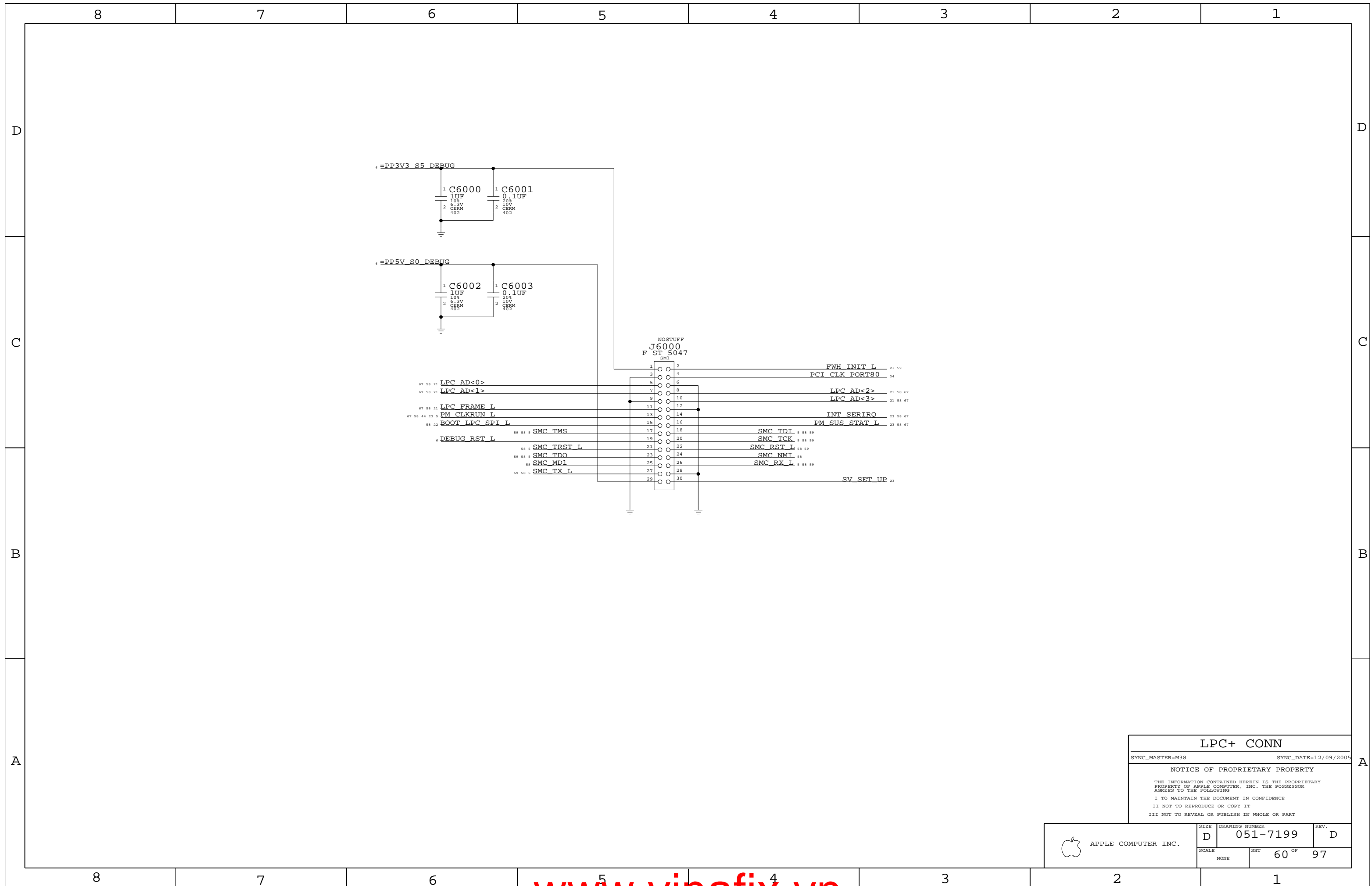
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SCALE	SHT	59 OF 97
NONE		



LPC+ CONN

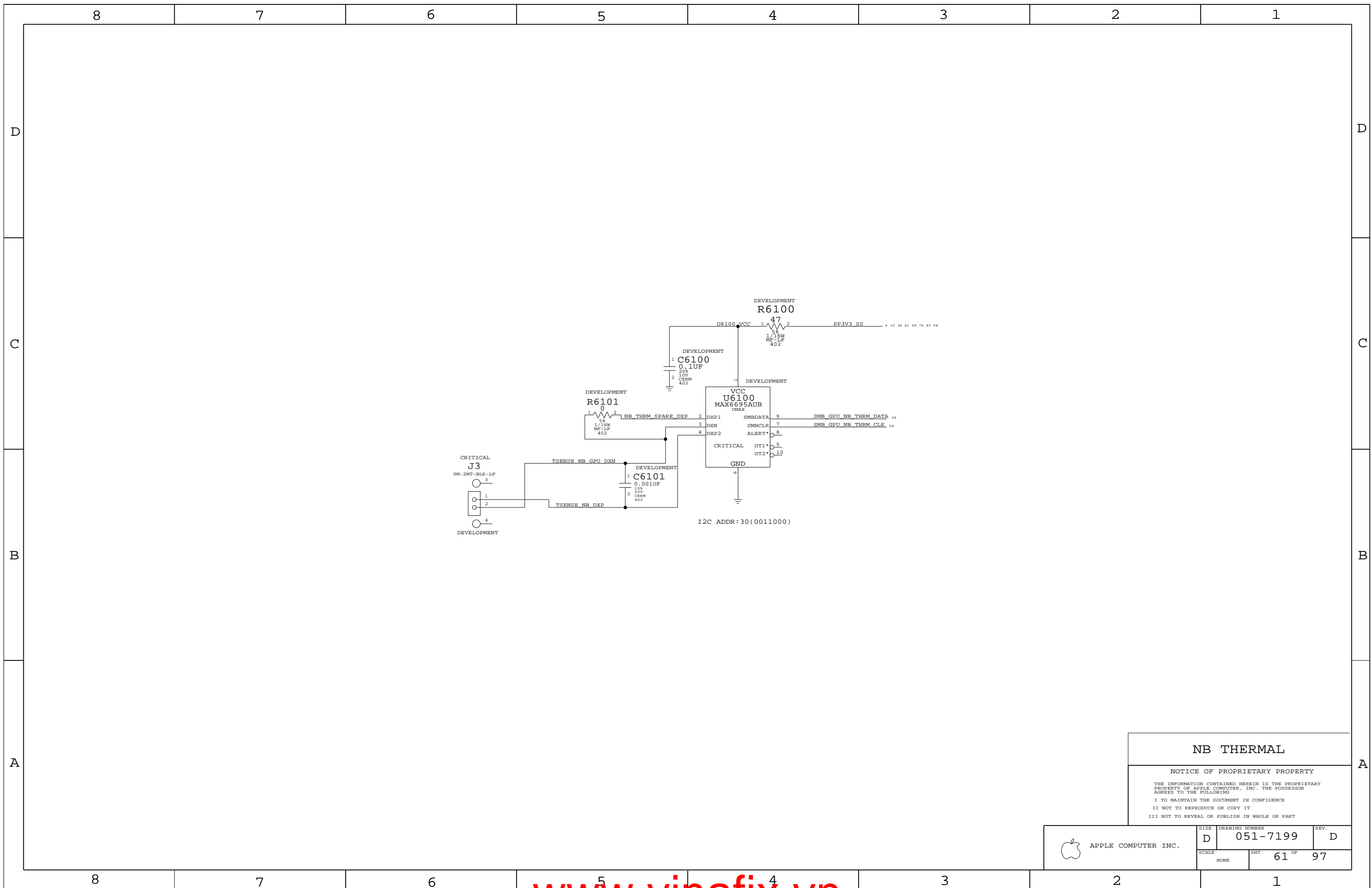
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	SCALE NONE	SHT 60 OF 97	



NB THERMAL

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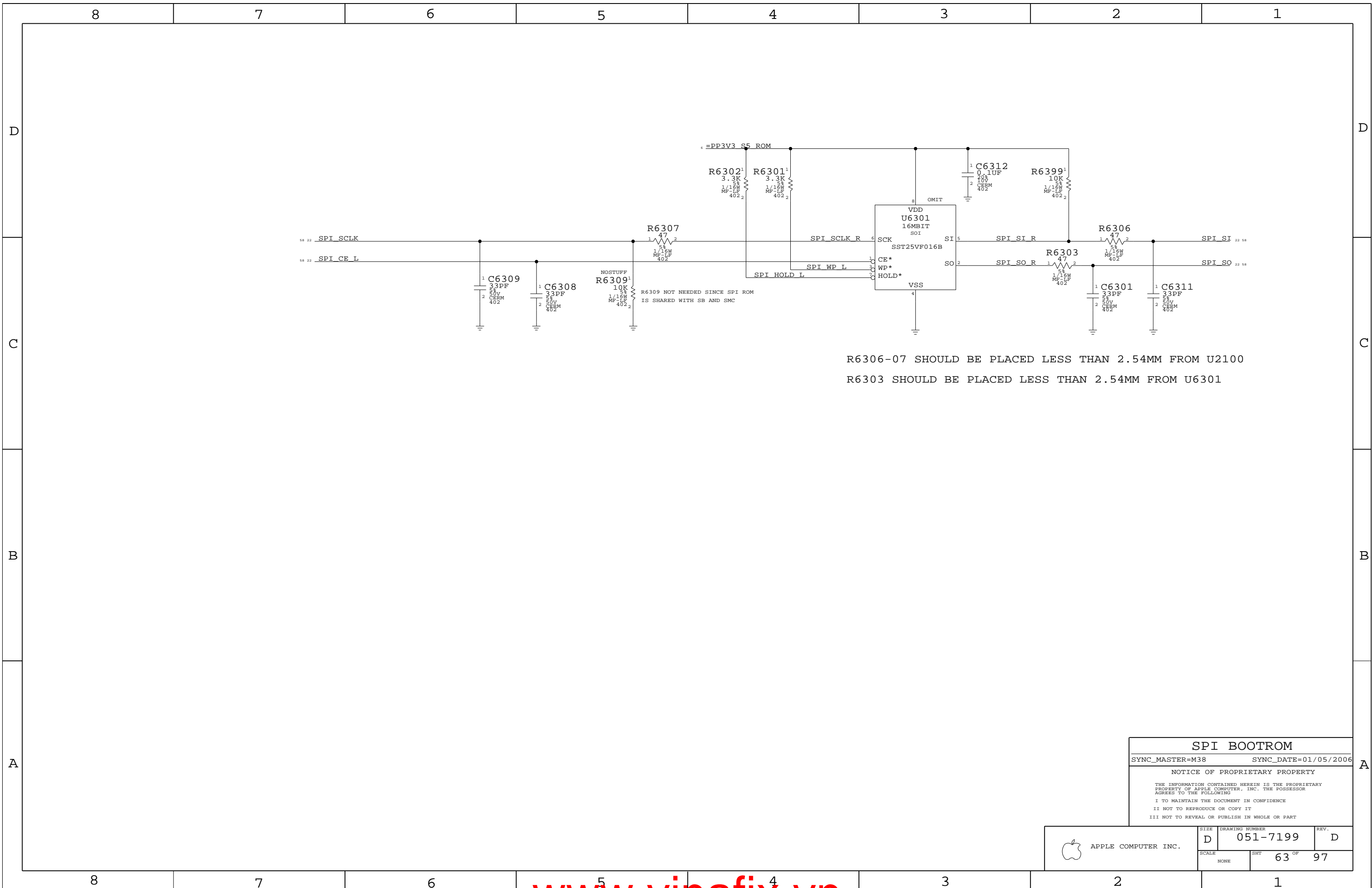
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	D	051-7199	D
SCALE	SHT	OF	
NONE	61	97	



R6306-07 SHOULD BE PLACED LESS THAN 2.54MM FROM U2100
 R6303 SHOULD BE PLACED LESS THAN 2.54MM FROM U6301

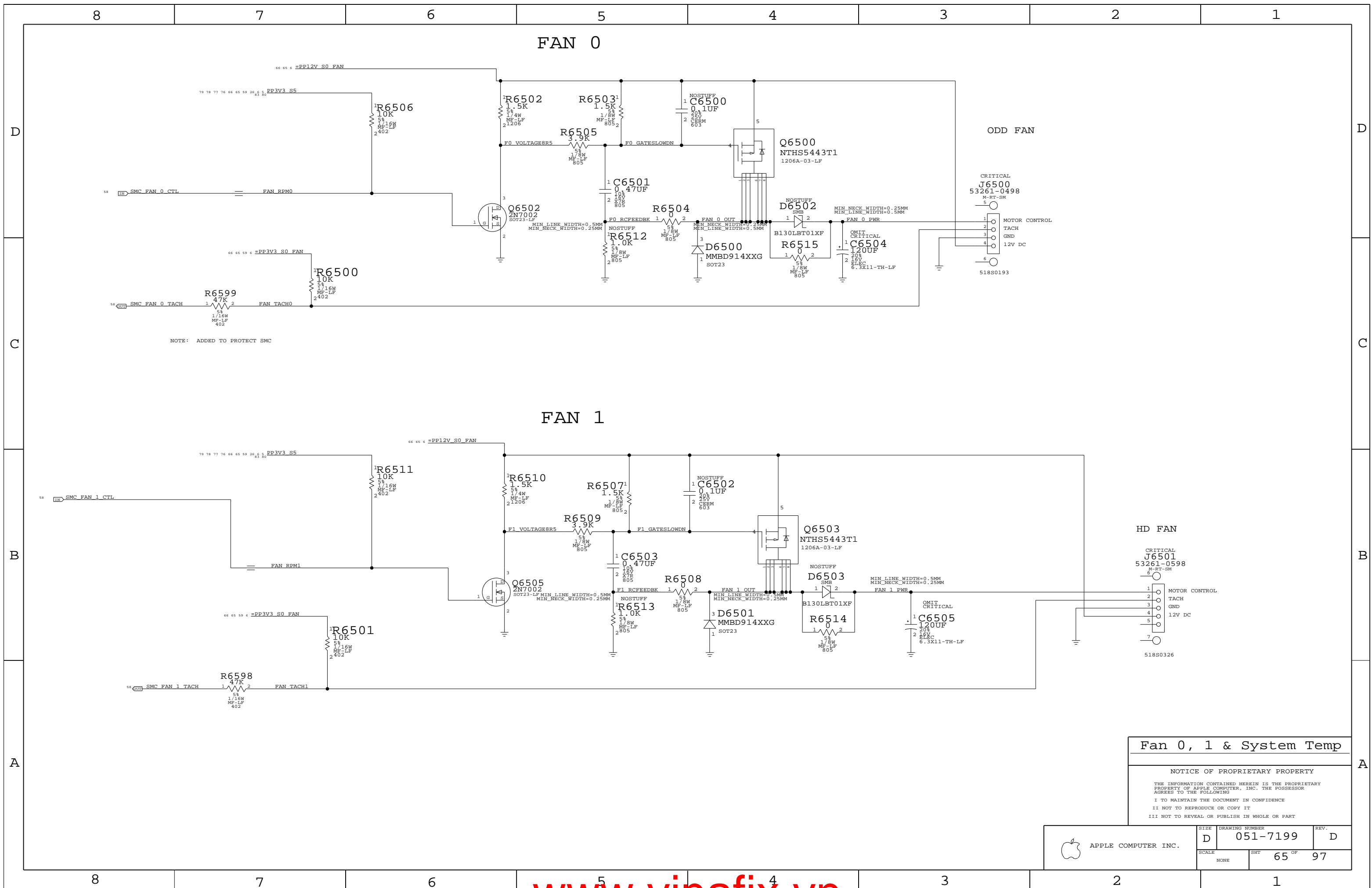
SPI BOOTROM
 SYNC_MASTER=M38 SYNC_DATE=01/05/2006

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	SCALE NONE	SHT 63 OF 97	



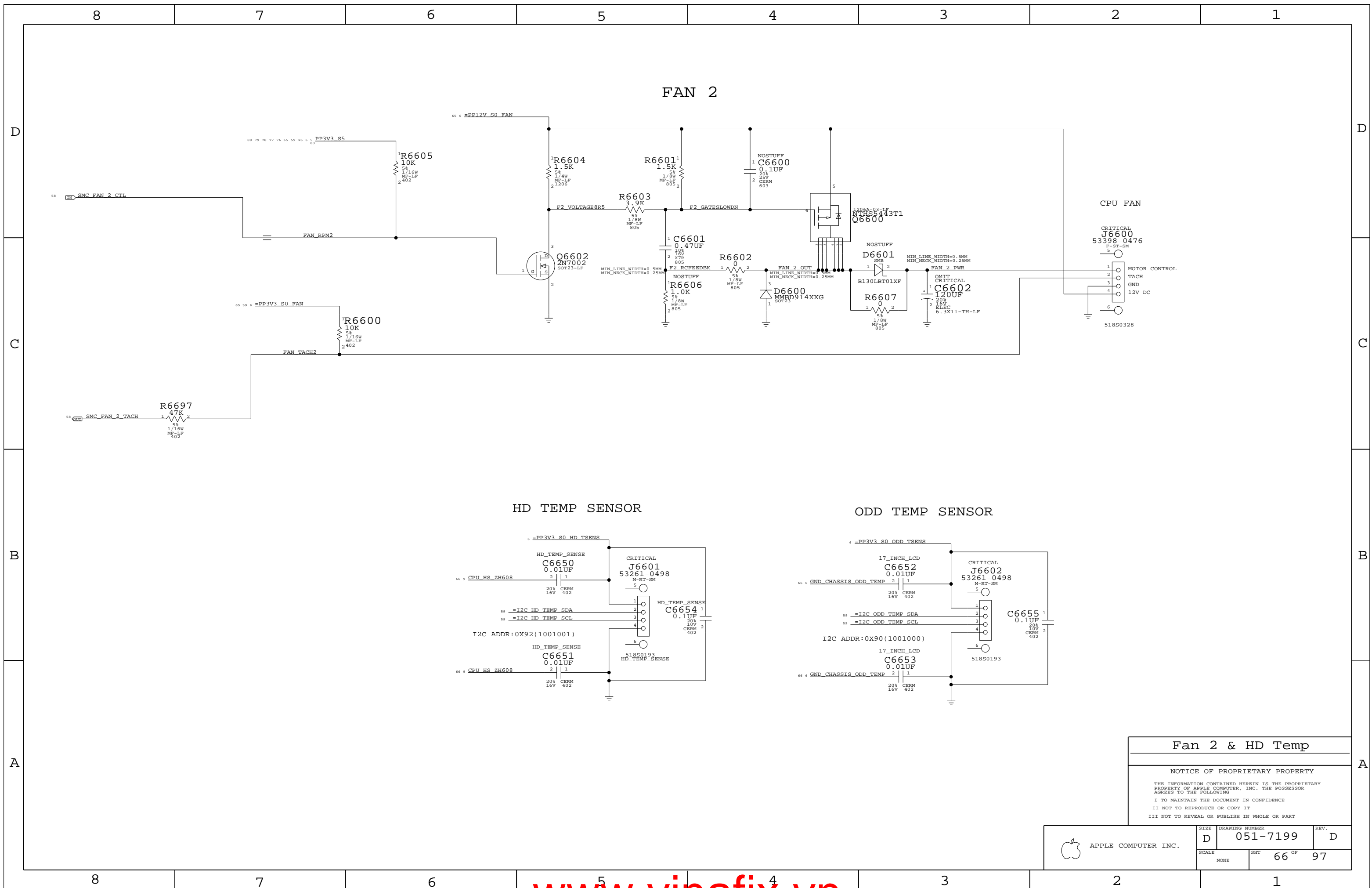
FAN 0

FAN 1

Fan 0, 1 & System Temp

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SCALE	SHT	65 OF	97
NONE			



HD TEMP SENSOR

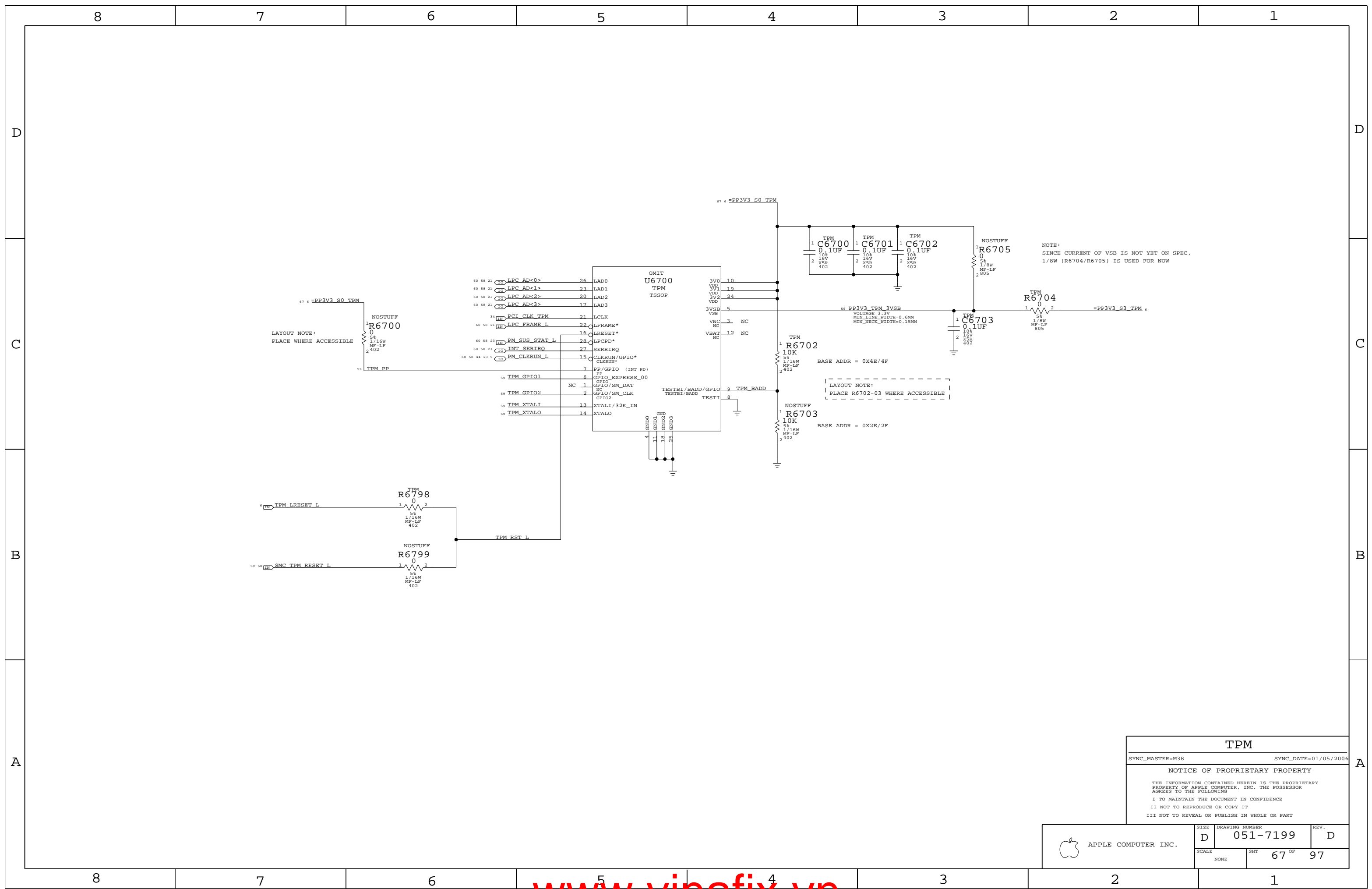
ODD TEMP SENSOR

Fan 2 & HD Temp

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	D	051-7199	D
SCALE	SHT	66 OF	97
NONE			



LAYOUT NOTE:
PLACE WHERE ACCESSIBLE

LAYOUT NOTE:
PLACE R6702-03 WHERE ACCESSIBLE

NOTE:
SINCE CURRENT OF VSB IS NOT YET ON SPEC,
1/8W (R6704/R6705) IS USED FOR NOW

TPM

SYNC_MASTER=M38 SYNC_DATE=01/05/2006

NOTICE OF PROPRIETARY PROPERTY

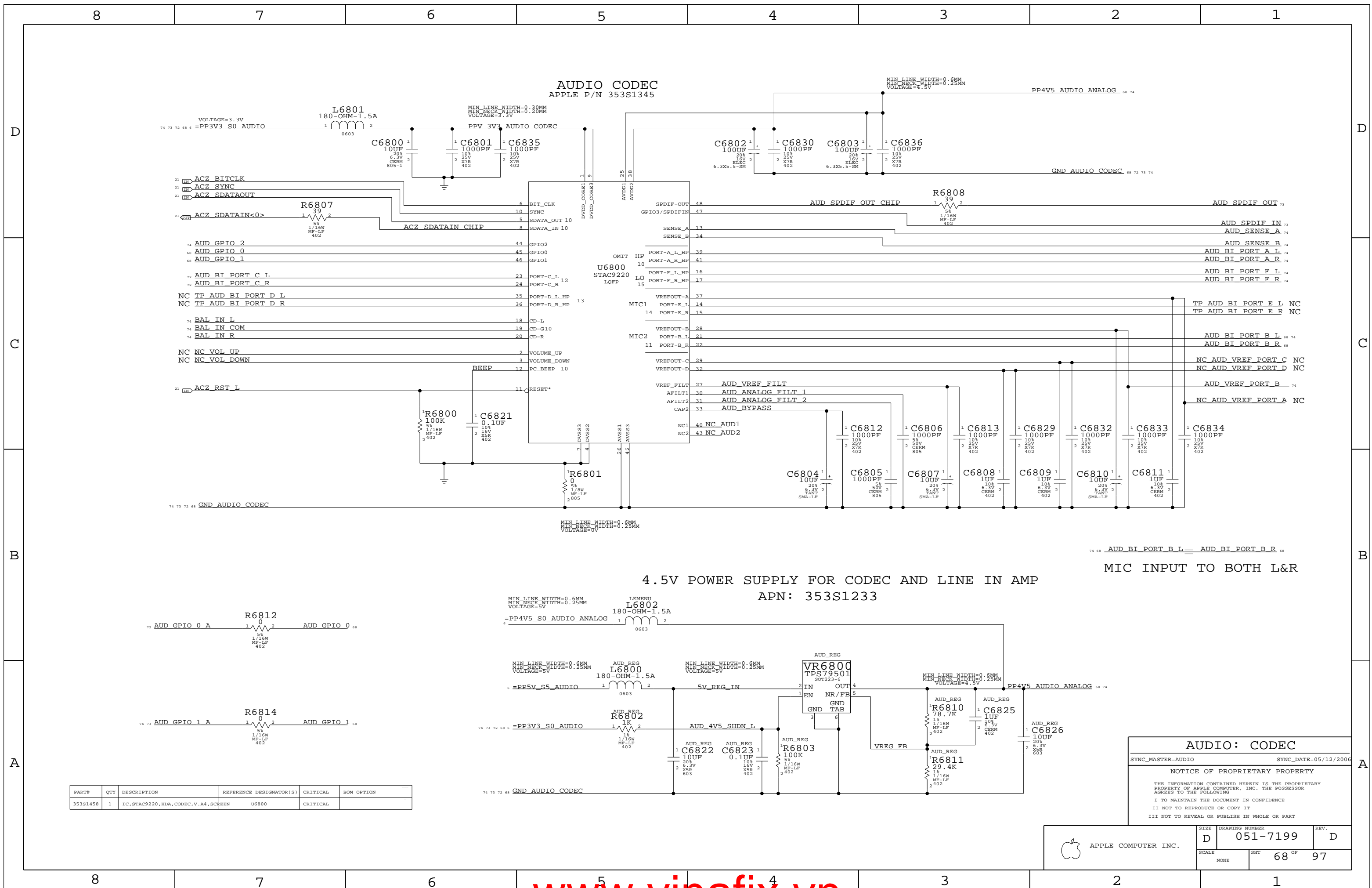
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	SCALE NONE	SHT 67 OF 97	



AUDIO CODEC
APPLE P/N 353S1345

4.5V POWER SUPPLY FOR CODEC AND LINE IN AMP
APN: 353S1233

AUDIO: CODEC

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S1458	1	IC, STAC9220, HDA, CODEC, V.A4, SCREEN	U6800	CRITICAL	

SYNC_MASTER=AUDIO SYNC_DATE=05/12/2006

NOTICE OF PROPRIETARY PROPERTY

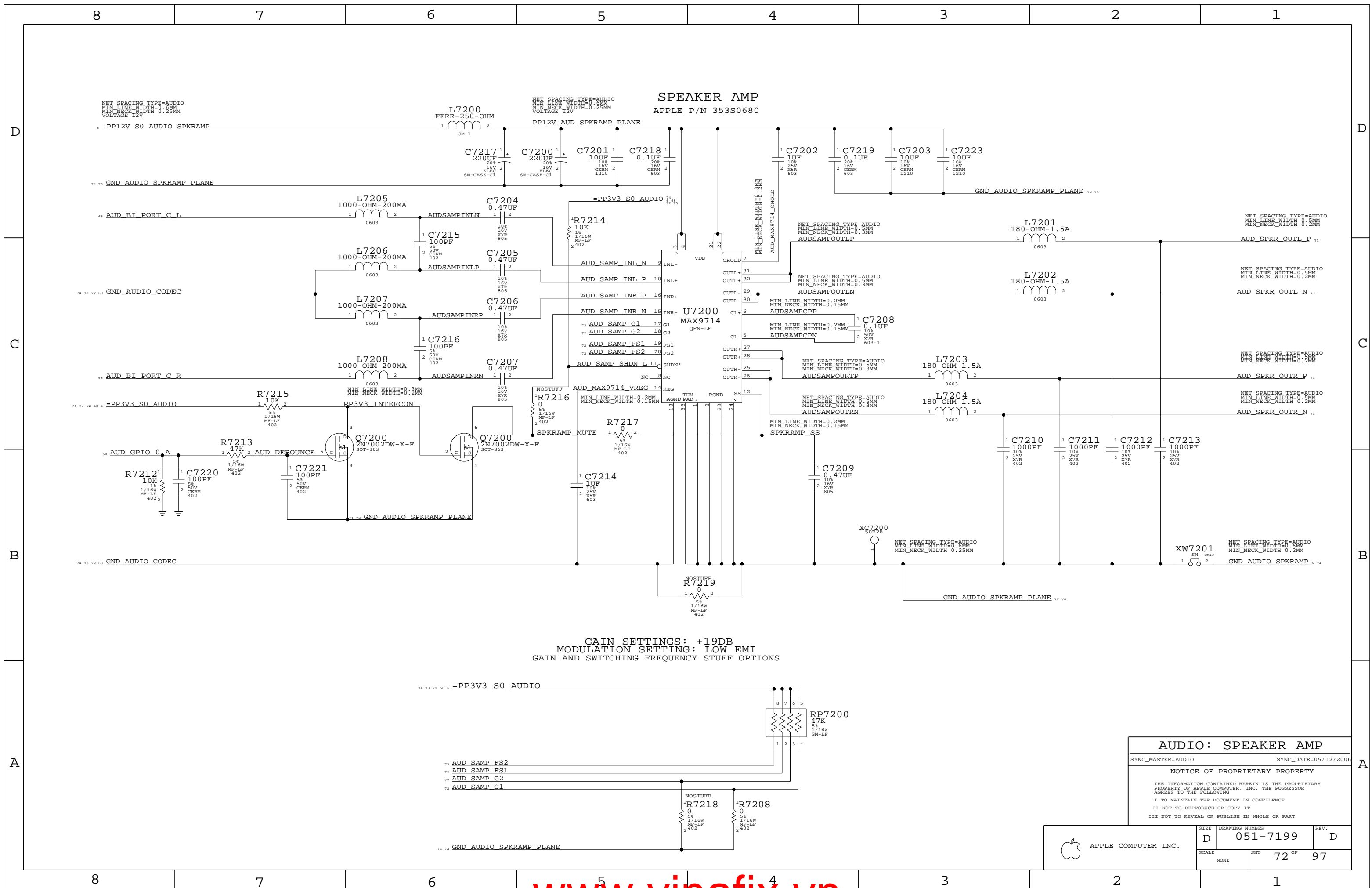
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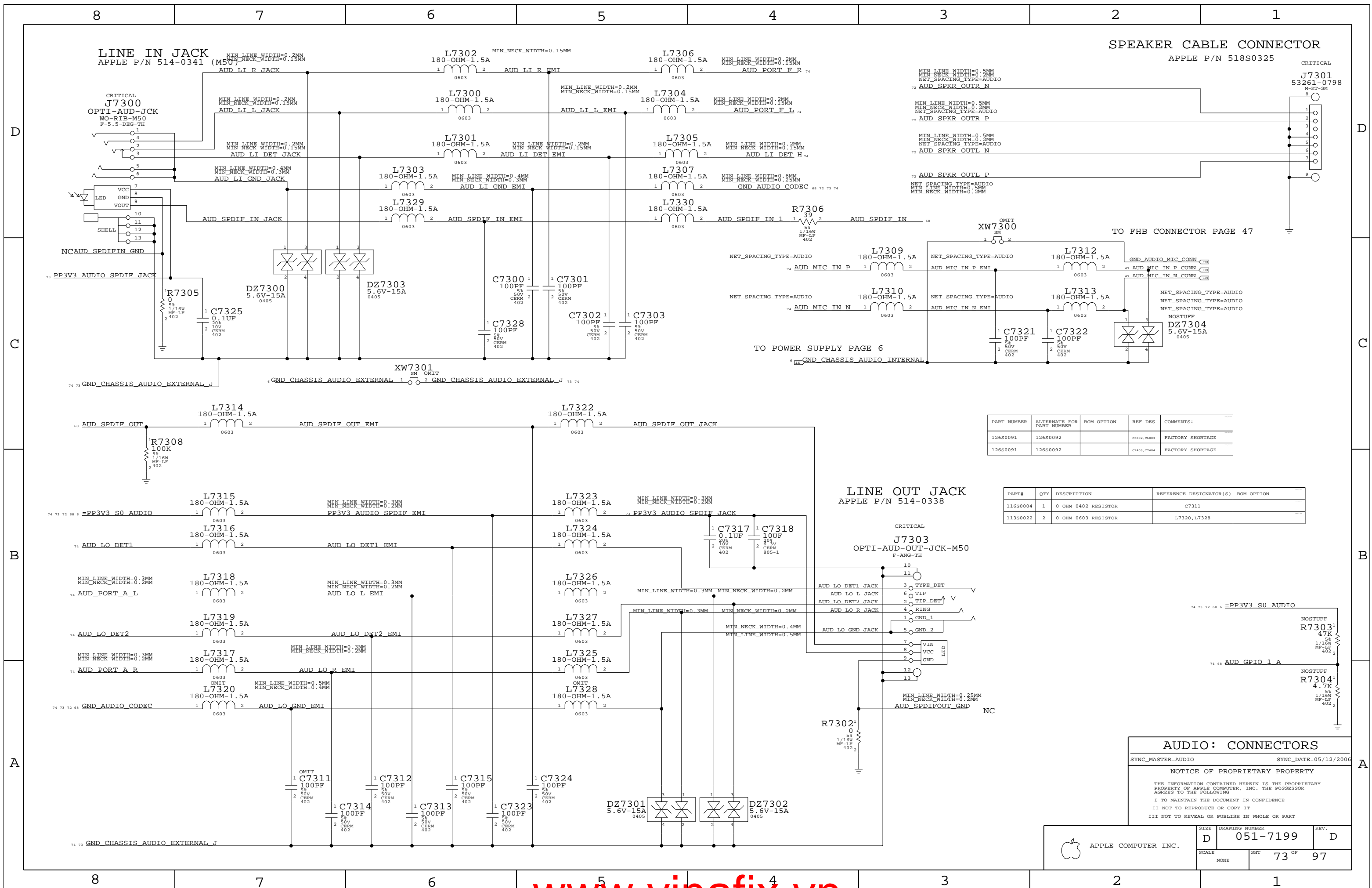
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	D
SCALE	SHT	68 OF 97	
NONE			



GAIN SETTINGS: +19DB
 MODULATION SETTING: LOW EMI
 GAIN AND SWITCHING FREQUENCY STUFF OPTIONS

AUDIO: SPEAKER AMP
 SYNC_MASTER=AUDIO SYNC_DATE=05/12/2006
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	D	051-7199	D
SCALE	SHT	72 OF	97
NONE			



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
126S0091	126S0092		C802, C803	FACTORY SHORTAGE
126S0091	126S0092		C743, C744	FACTORY SHORTAGE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S0004	1	0 OHM 0402 RESISTOR	C7311	
113S0022	2	0 OHM 0603 RESISTOR	L7320, L7328	

AUDIO: CONNECTORS

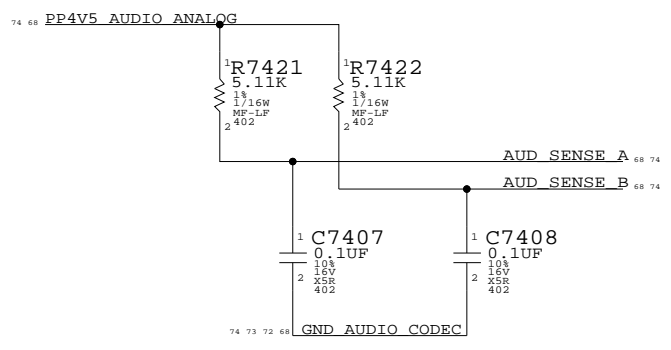
SYNC_MASTER=AUDIO SYNC_DATE=05/12/2006

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	D
SCALE	SHT	73 OF	97
NONE			

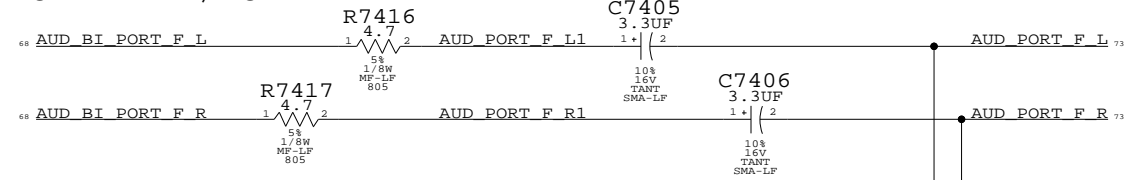
JACK SENSE PULL UPS (PLACE NEXT TO CODEC)



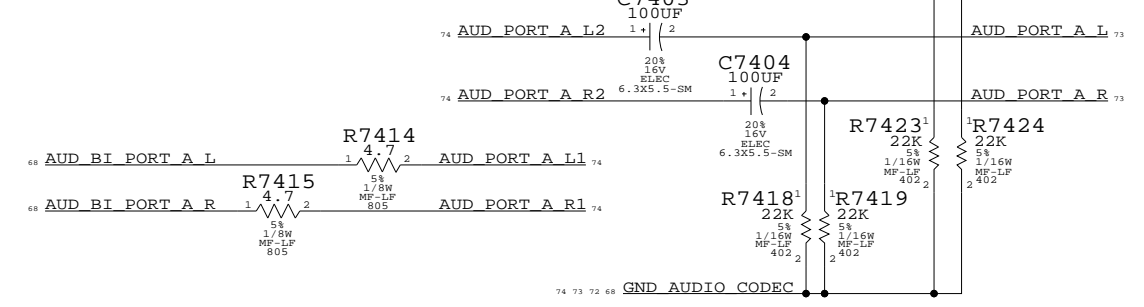
USED PORTS
 PORT A HP/LI
 PORT B MIC IN
 PORT C BI SPEAKERS
 PORT F LI/LO

UNUSED PORTS
 PORT E
 PORT D

PORT F LI/LO

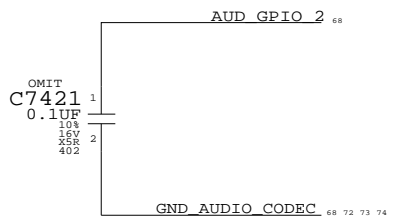


PORT A HP/LI

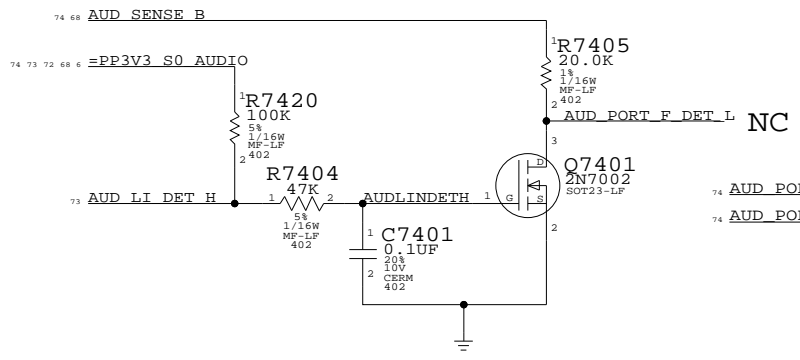


UNUSED PORT TERMINATION

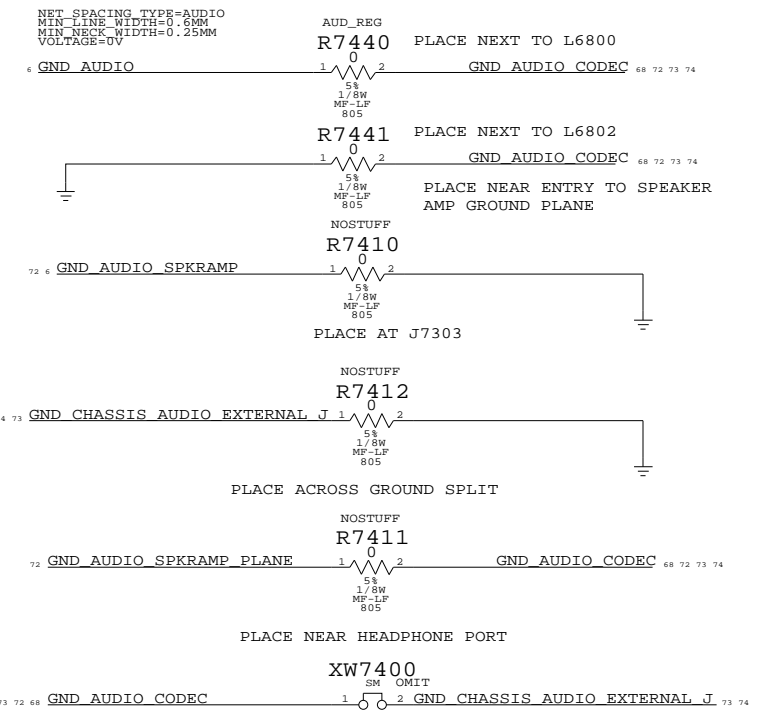
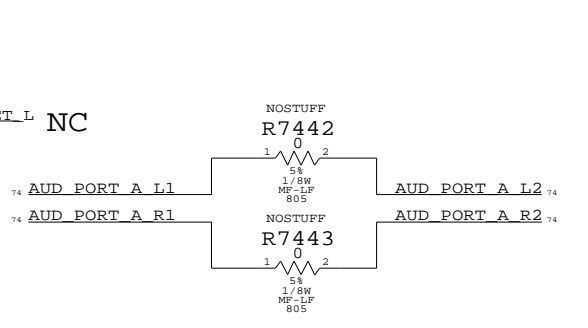
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
132S0099	1	CAPACITOR, .1UF, 0402	C7421	CRITICAL	CAMERA
114S0315	1	RESISTOR, 10K OHM, 0402	C7421	CRITICAL	NOCAMERA



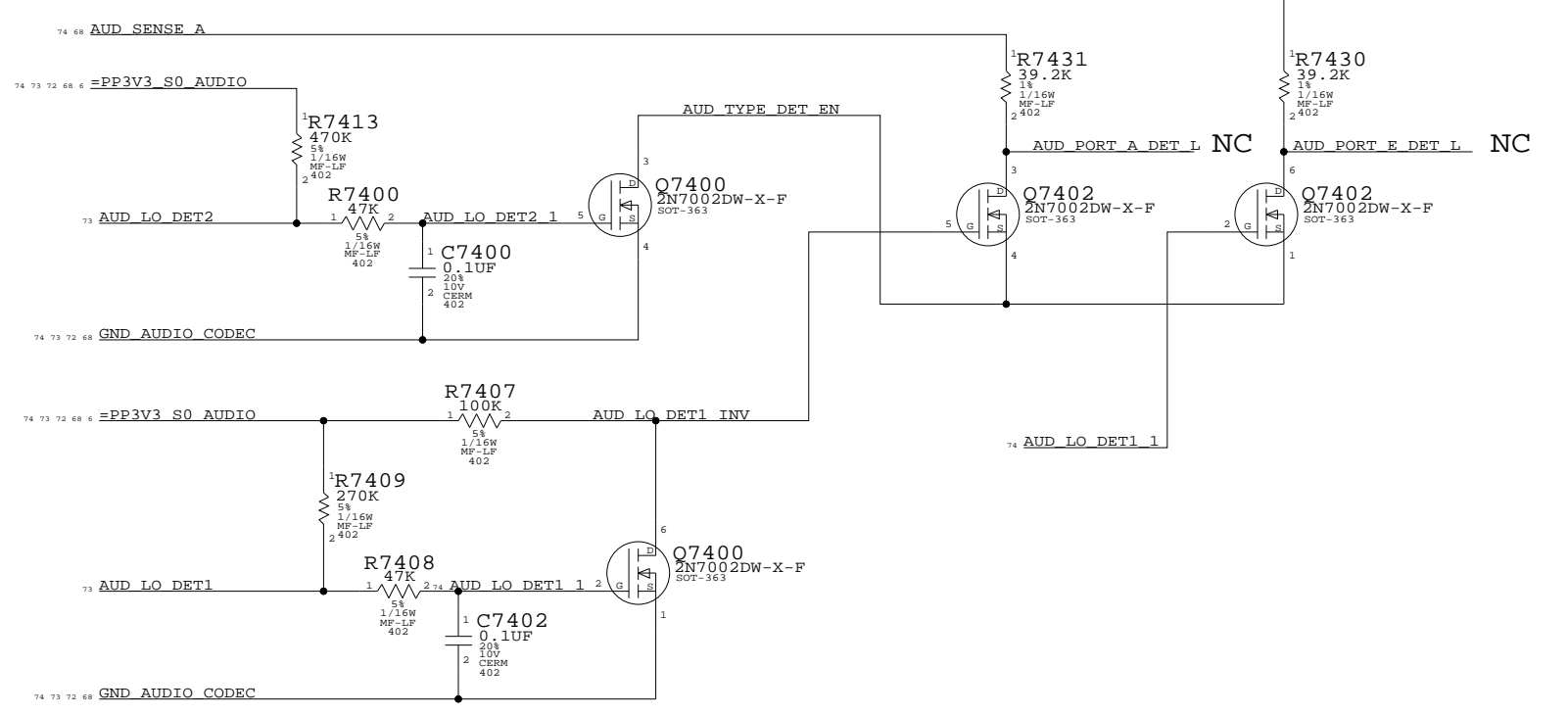
PORT F (LI) PLUG DETECT



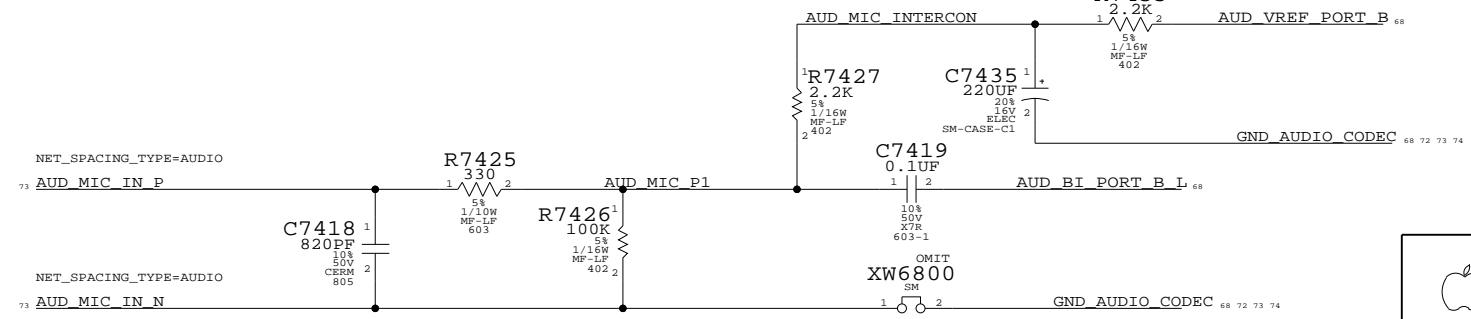
AUDIO GROUND RETURNS



PORT A/H (LO/DIG_OUT) PLUG DETECT (E TELLS H TO COME ON)



MICROPHONE IMPEDANCE MATCHING CIRCUIT



AUDIO: POWER SUPPLIES

SYNC_MASTER=AUDIO SYNC_DATE=05/12/2006

NOTICE OF PROPRIETARY PROPERTY

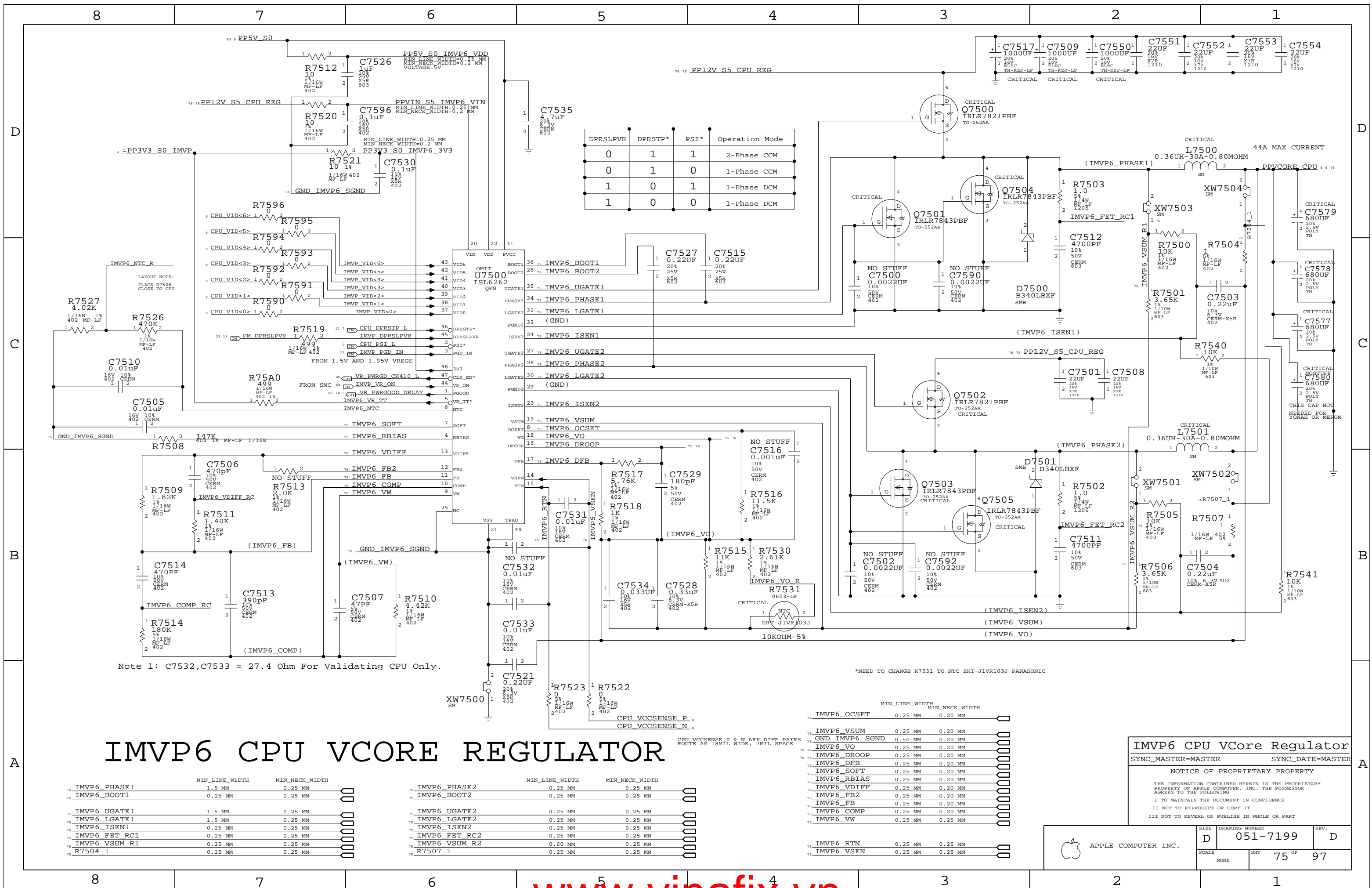
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NONE			



DPRSLPVR	DPRSTP*	PSI*	Operation Mode
0	1	1	2-Phase CCM
0	1	0	1-Phase CCM
1	0	1	1-Phase DCM
1	0	0	1-Phase DCM

Note 1: C7532,C7533 = 27.4 Ohm For Validating CPU Only.

*NEED TO CHANGE R7531 TO NTC ERT-J1VR103J PANASONIC

IMVP6 CPU VCore Regulator

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
75 IMVP6_PHASE1	1.5 MM	0.25 MM
75 IMVP6_BOOT1	0.25 MM	0.25 MM
75 IMVP6_UGATE1	1.5 MM	0.25 MM
75 IMVP6_LGATE1	1.5 MM	0.25 MM
75 IMVP6_ISEN1	0.25 MM	0.25 MM
75 IMVP6_FET_RC1	0.25 MM	0.25 MM
75 IMVP6_VSUM_R1	0.25 MM	0.25 MM
75 R7504_1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
75 IMVP6_PHASE2	0.25 MM	0.25 MM
75 IMVP6_BOOT2	0.25 MM	0.25 MM
75 IMVP6_UGATE2	0.25 MM	0.25 MM
75 IMVP6_LGATE2	0.25 MM	0.25 MM
75 IMVP6_ISEN2	0.25 MM	0.25 MM
75 IMVP6_FET_RC2	0.25 MM	0.25 MM
75 IMVP6_VSUM_R2	0.60 MM	0.25 MM
75 R7507_1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
75 IMVP6_OCSET	0.25 MM	0.20 MM
75 IMVP6_VSUM	0.25 MM	0.20 MM
75 GND_IMVP6_SGND	0.50 MM	0.20 MM
75 IMVP6_VO	0.25 MM	0.20 MM
75 IMVP6_DROOP	0.25 MM	0.20 MM
75 IMVP6_DFB	0.25 MM	0.20 MM
75 IMVP6_SOFT	0.25 MM	0.20 MM
75 IMVP6_RBIAS	0.25 MM	0.20 MM
75 IMVP6_VDIFF	0.25 MM	0.20 MM
75 IMVP6_FB2	0.25 MM	0.20 MM
75 IMVP6_FB	0.25 MM	0.20 MM
75 IMVP6_COMP	0.25 MM	0.20 MM
75 IMVP6_VW	0.25 MM	0.25 MM
75 IMVP6_RTIN	0.25 MM	0.25 MM
75 IMVP6_VSEN	0.25 MM	0.25 MM

IMVP6 CPU VCore Regulator

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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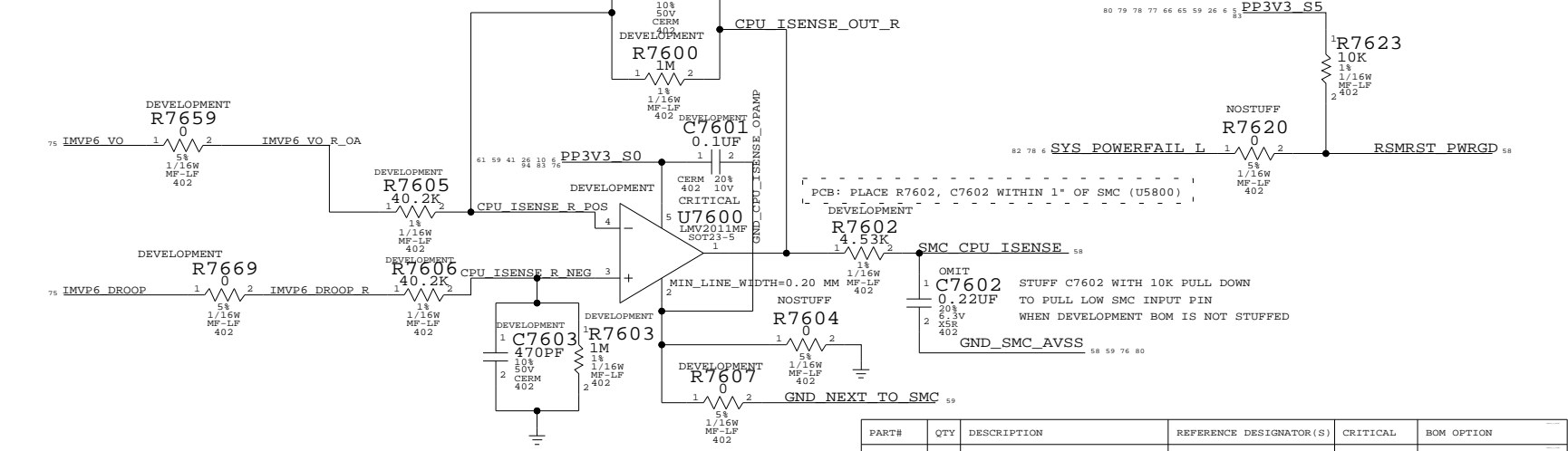
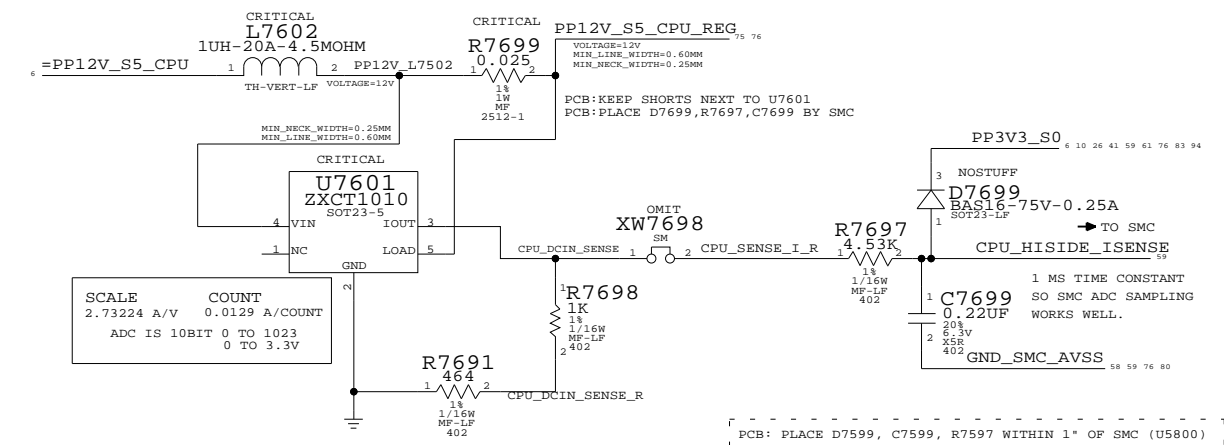
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APPLE COMPUTER INC.	SIZE: D	DRAWING NUMBER: 051-7199	REV.: D
	SCALE: NONE	SHEET: 75 OF 97	

PROCESSOR VCORE CURRENT SENSE
(USING 12V INPUT CURRENT TO DERIVE CPU CURRENT)

PROCESSOR VCORE CURRENT SENSE
(MEASURING DC/DC INDUCTOR DCR TO DERIVE CPU CURRENT)

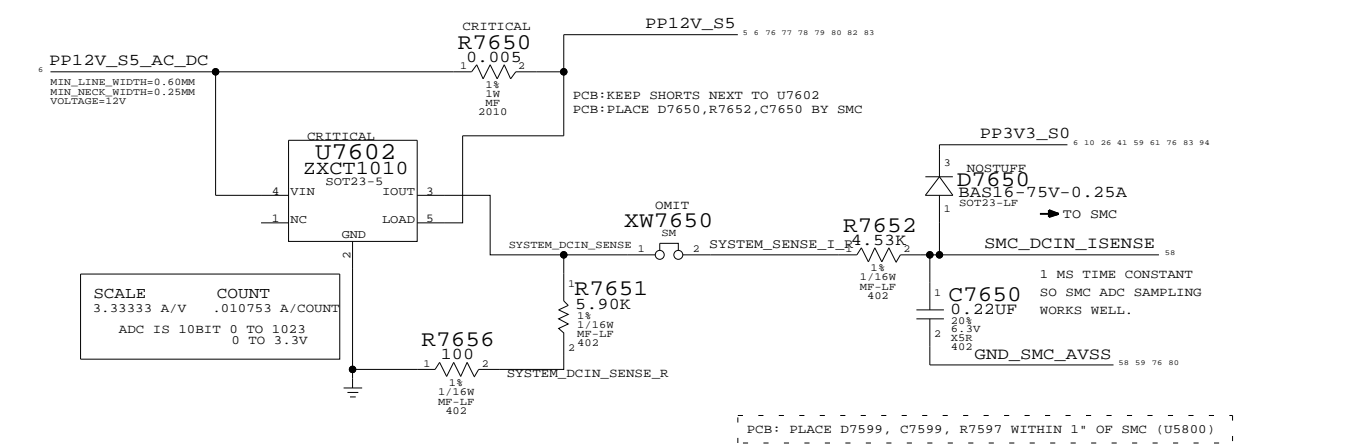
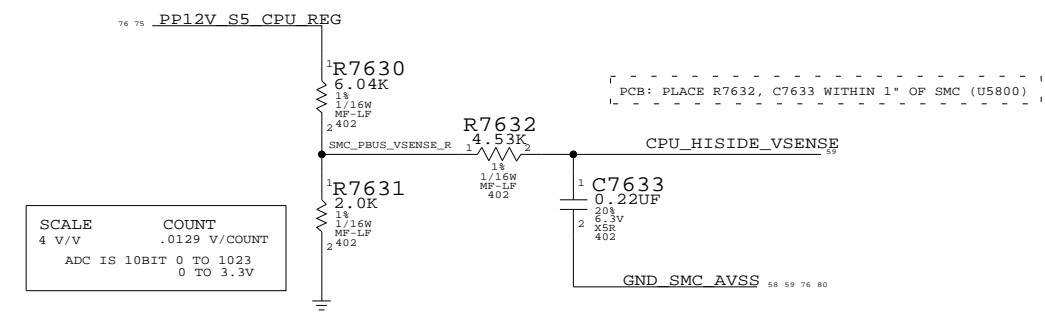
SMC PWRGD PULLUP



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
132S0080	1	CAP, 0.22UF, 6.3V, 20%, 0402	C7602		DEVELOPMENT
116S0090	1	RES, 10K, 5%, 0402	C7602		NOT_DEVELOPMENT

PROCESSOR DCIN VOLTAGE SENSE
(SCALING 12V INPUT VOLTAGE TO SMC)

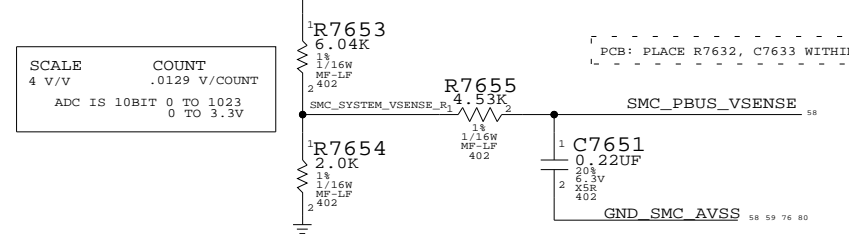
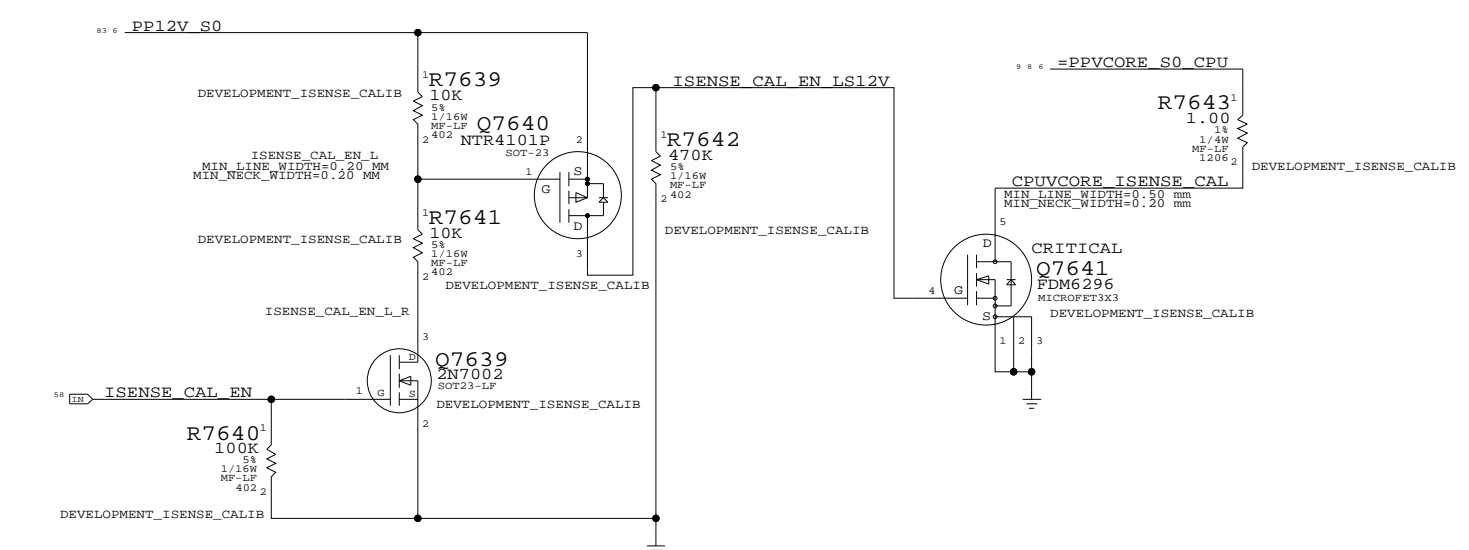
SYSTEM CURRENT SENSE



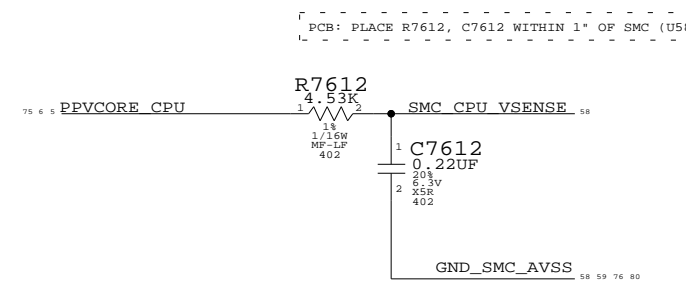
SYSTEM VOLTAGE SENSE
(SCALING 12V INPUT VOLTAGE TO SMC)

Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits



PROCESSOR VCORE SENSE



CPU & SYSTEM SENSE CIRCUITRIES

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

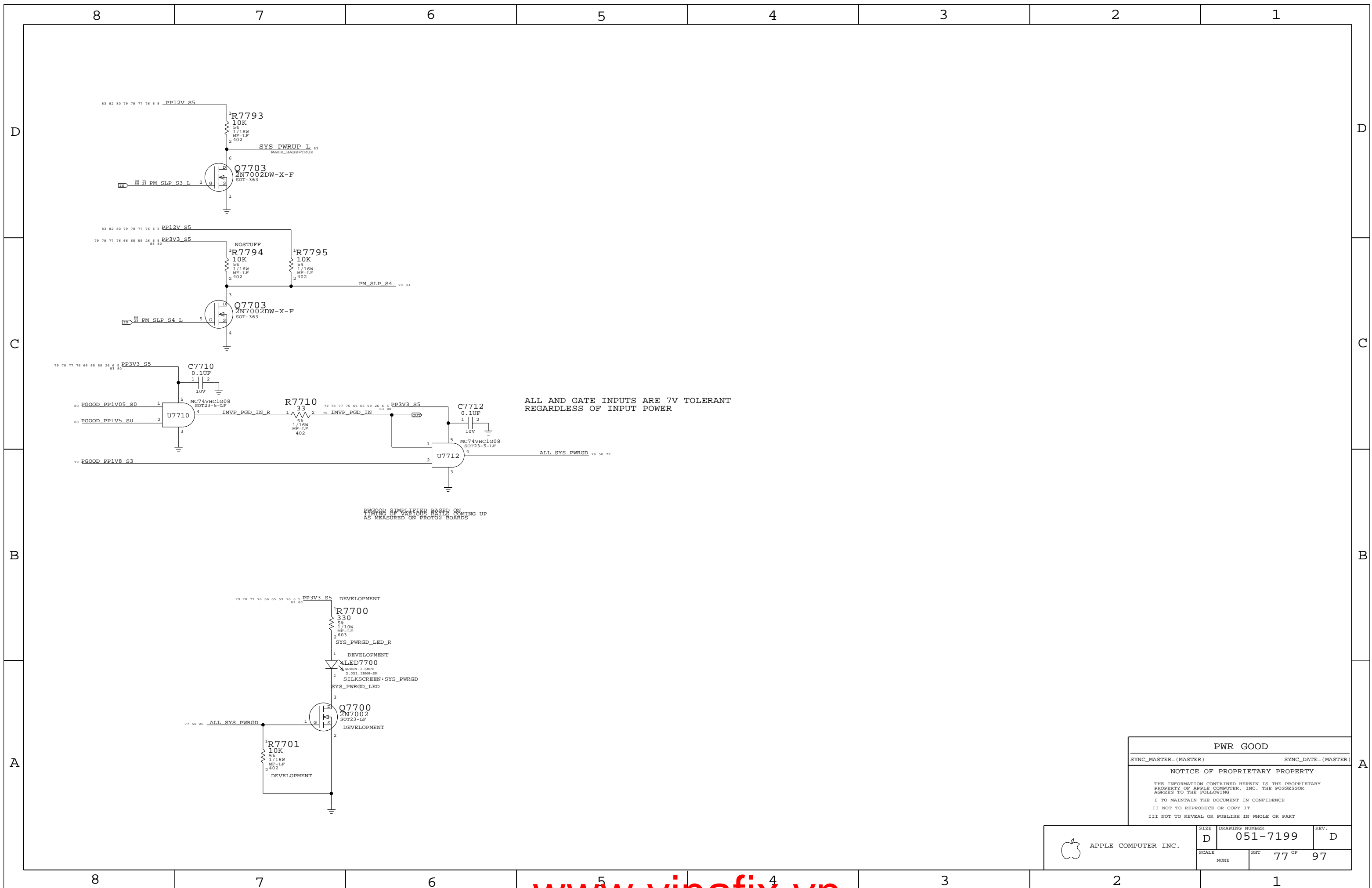
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	D	051-7199	D
SCALE	SHT	76 OF	97
NONE			



PWR GOOD

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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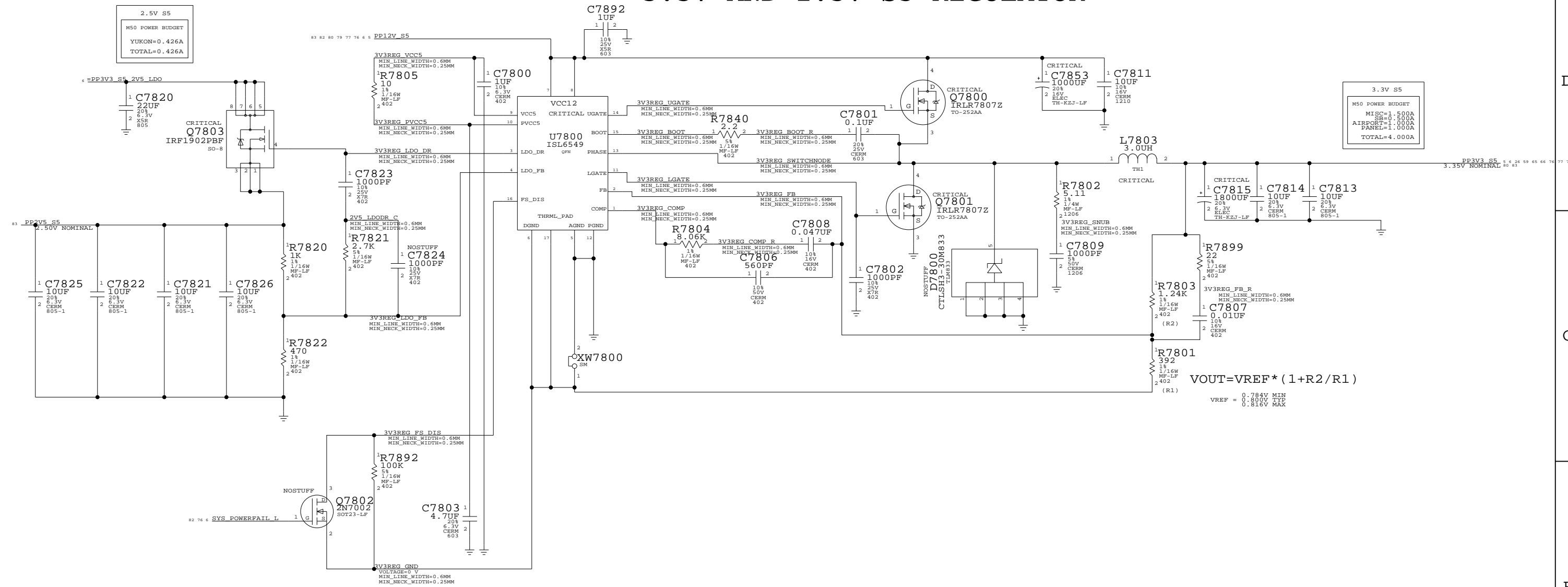
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SCALE	SHT	77 OF 97	
NONE			

3.3V AND 2.5V S5 REGULATOR



3V DC/DC 2.5V

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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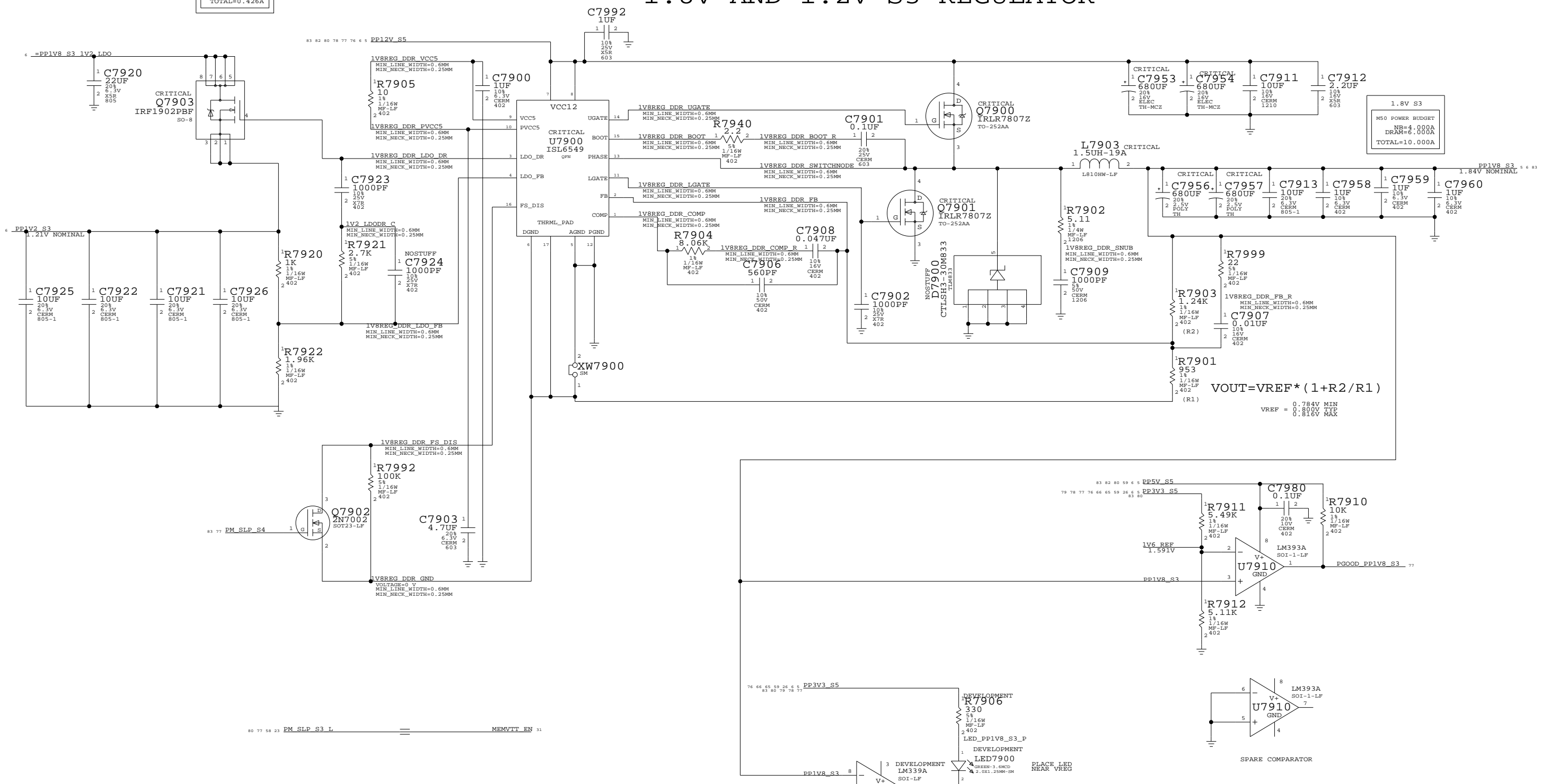
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	D	051-7199	D
SCALE	SHT	78 OF 97	
NONE			

1.8V AND 1.2V S3 REGULATOR

1.2V S3
MS0 POWER BUDGET
YUKON=0.426A
TOTAL=0.426A

1.8V S3
MS0 POWER BUDGET
NB=4.000A
DRAM=6.000A
TOTAL=10.000A

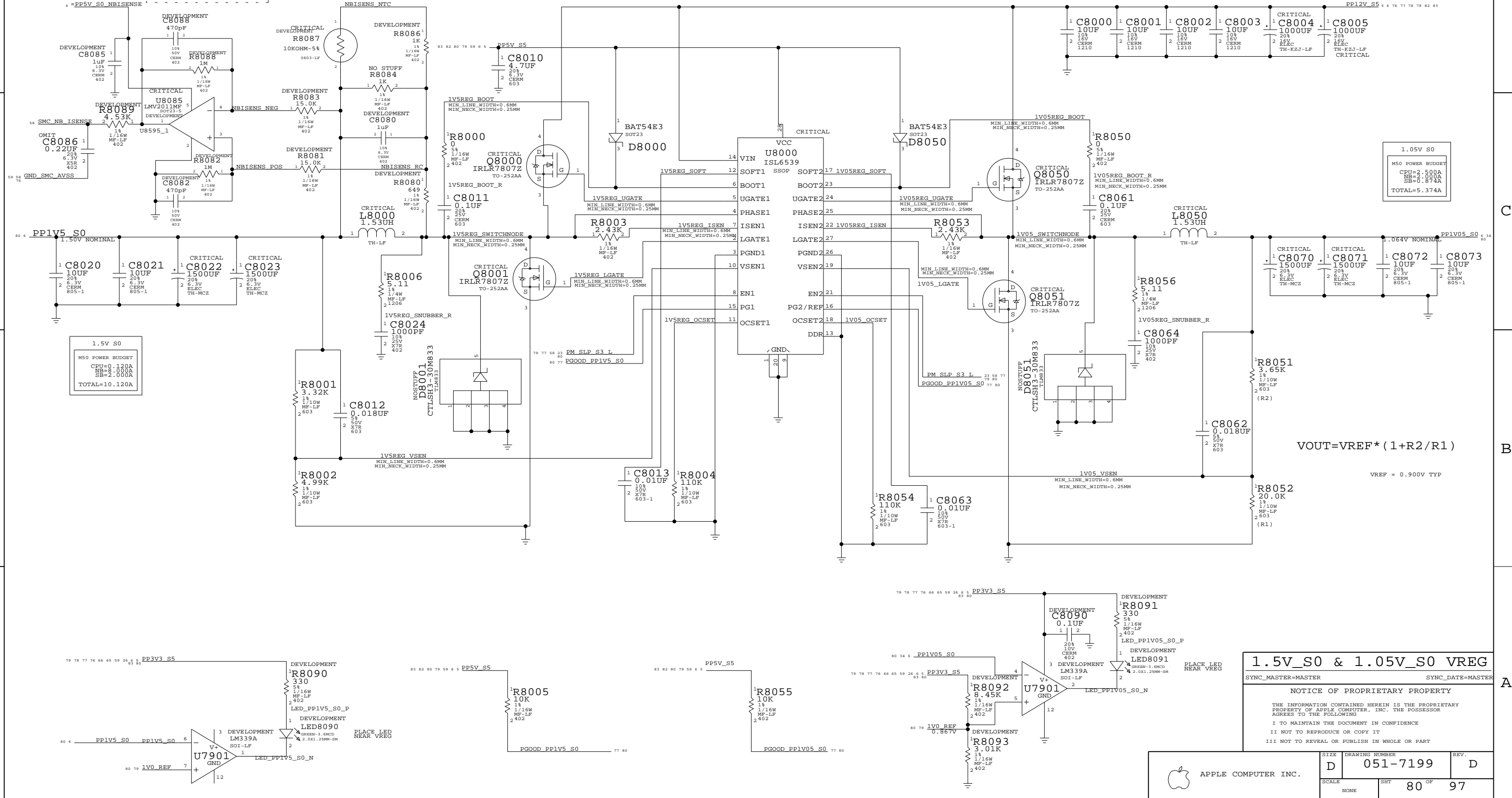


1.8V & 1.2V VREG		
SYNC_MASTER=MASTER	SYNC_DATE=MASTER	
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7199
SCALE NONE	SHT 79	OF 97

1.5V S0 AND 1.05V S0 RAILS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
13280080	1	CAP,0.22UF,6.3V,20%,0402	C8086		DEVELOPMENT
11650090	1	RES,10K,5%,0402	C8086		NOT_DEVELOPMENT

Placement Note:
KEEP C8080, R8080,
R8084 AND R8087
close to inductor



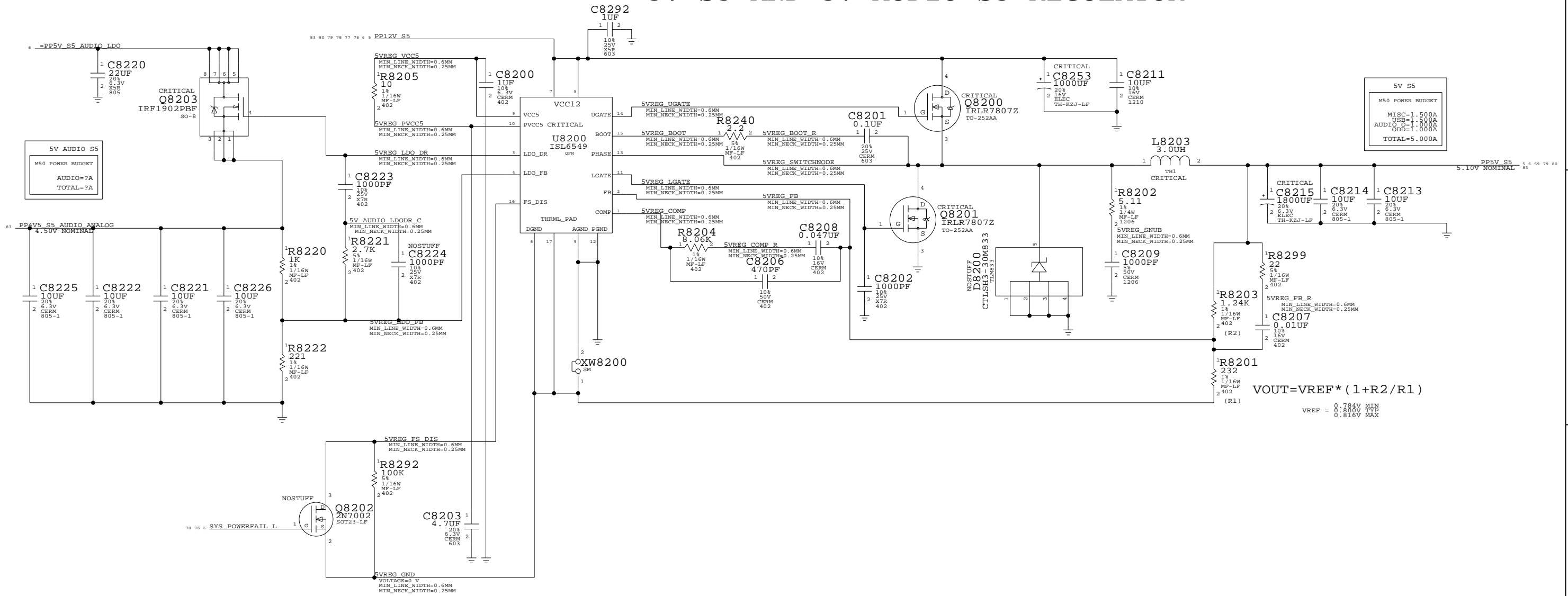
1.5V_S0 & 1.05V_S0 VREG

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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	D	051-7199	D
SCALE	SHT	80 OF	97
NONE			

5V S5 AND 5V AUDIO S5 REGULATOR



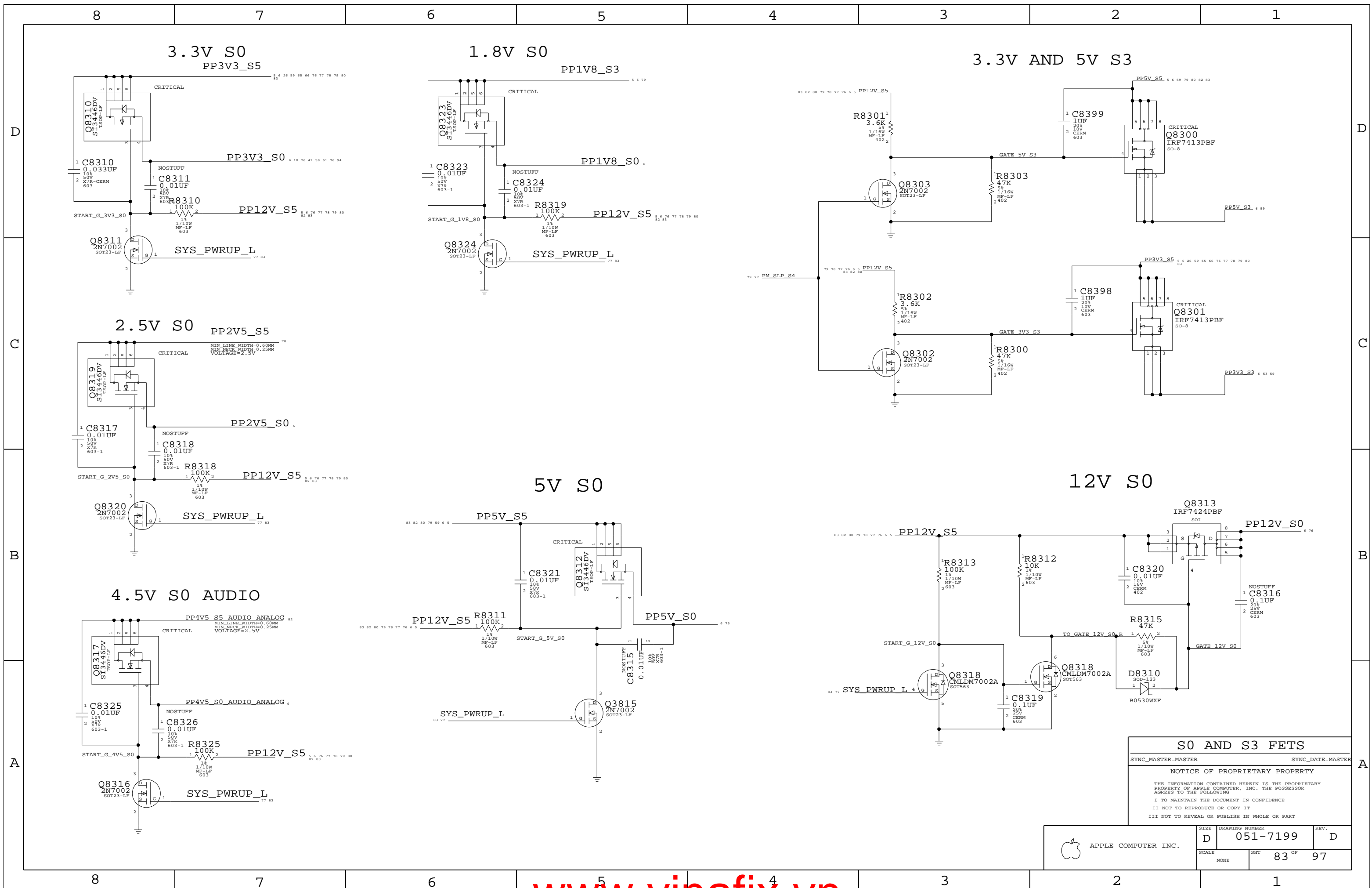
$V_{OUT} = V_{REF} * (1 + R2/R1)$

$V_{REF} = 0.784V \text{ MIN}$
 $0.800V \text{ TYP}$
 $0.816V \text{ MAX}$

POWER SUPPLY 3.3V/5V MAIN SWITCH

5V DC/DC	
SYNC_MASTER=MASTER	SYNC_DATE=MASTER
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	D	051-7199	D
SCALE	SHT	82 OF	97
NONE			



S0 AND S3 FETS

SYNC_MASTER=MASTER SYNC_DATE=MASTER


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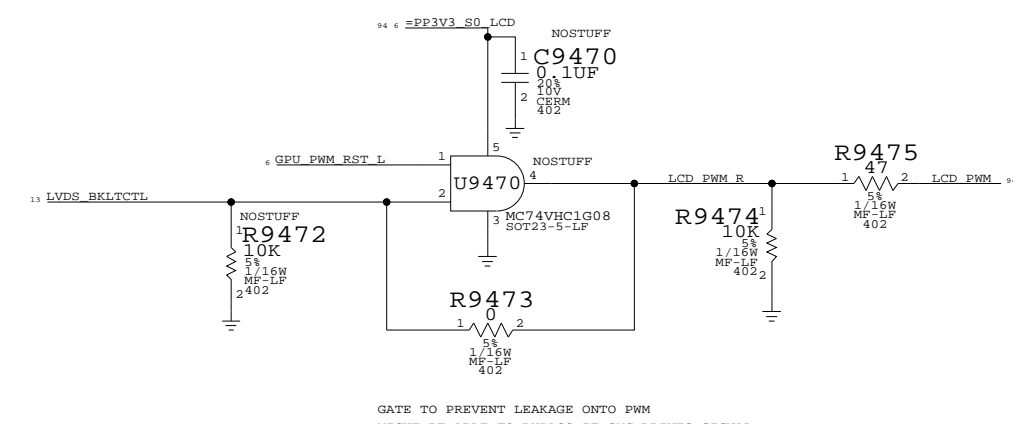
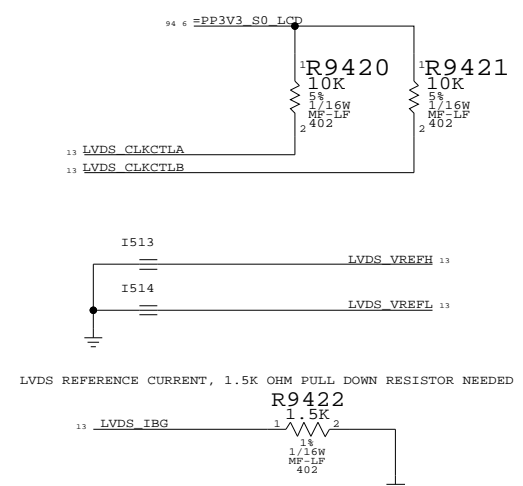
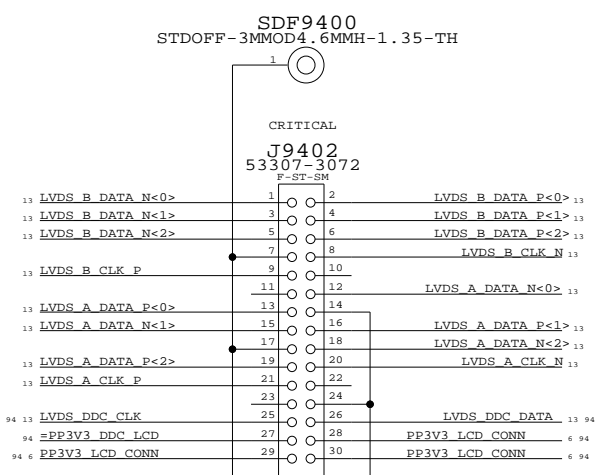
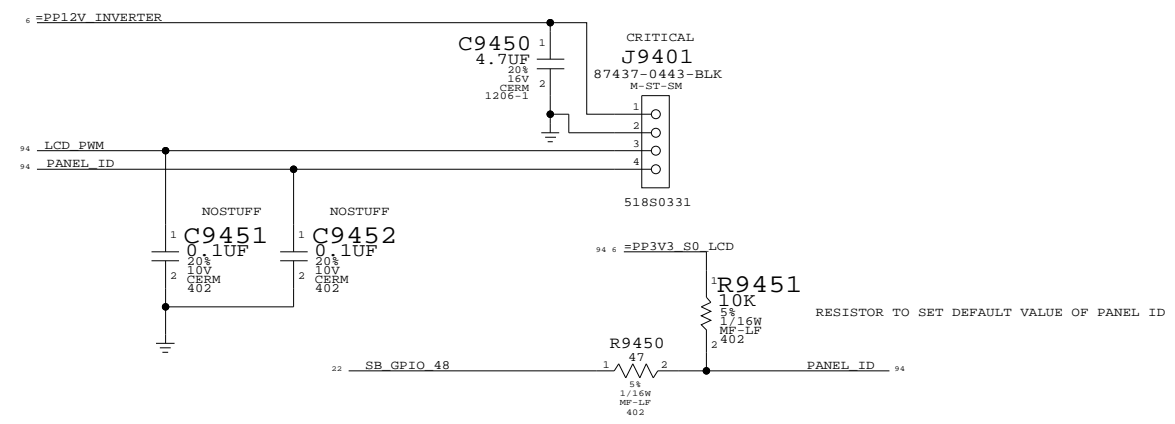
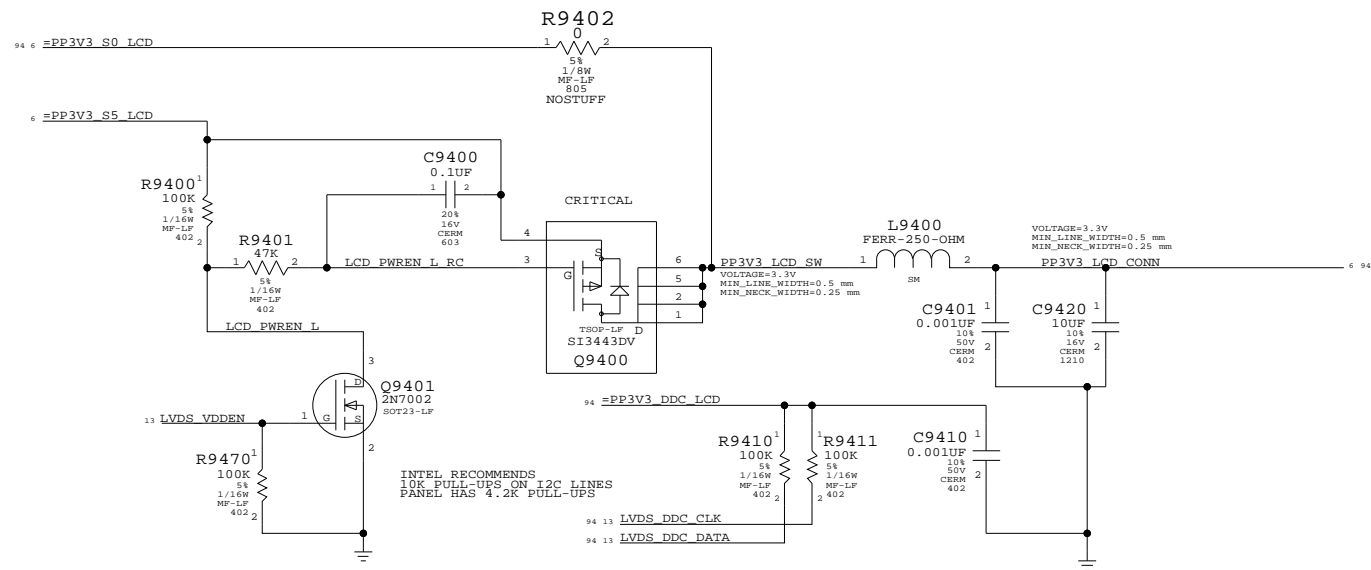
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SCALE	SHT	83 OF	97
NONE			

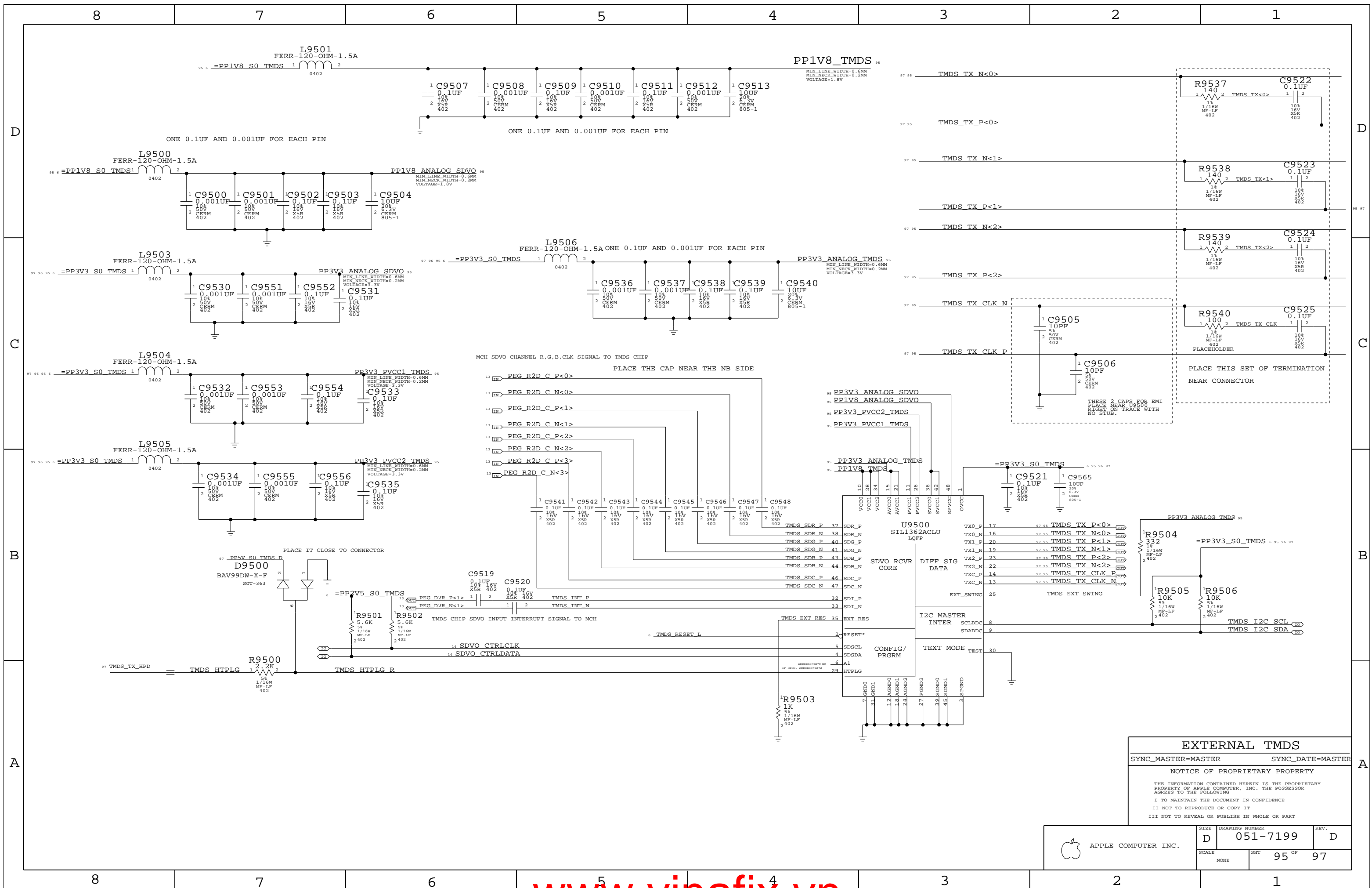
LCD (LVDS) INTERFACE

INVERTER INTERFACE



Internal Display Conns
 SYNC_MASTER=MASTER SYNC_DATE=MASTER
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SCALE	SHT	94 OF	97
NONE			



EXTERNAL TMSD
 SYNC_MASTER=MASTER SYNC_DATA=MASTER

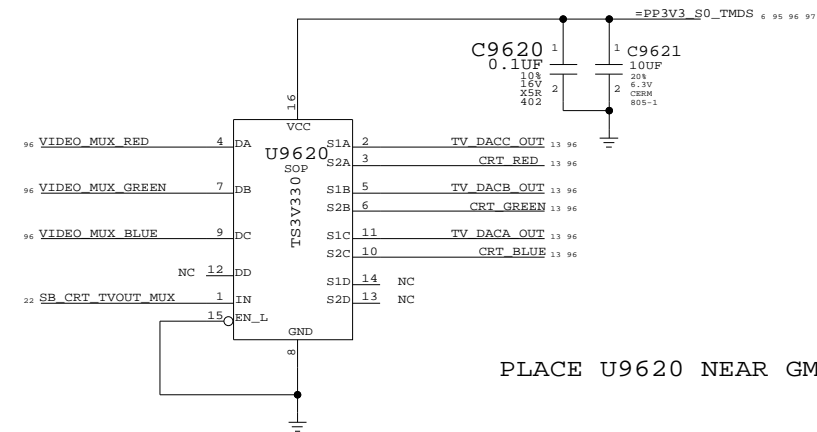
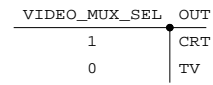
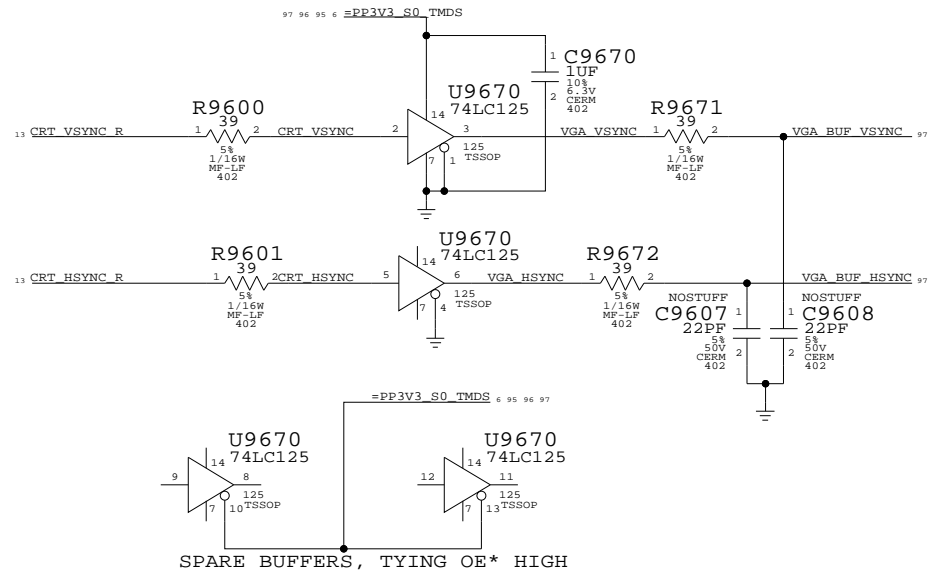
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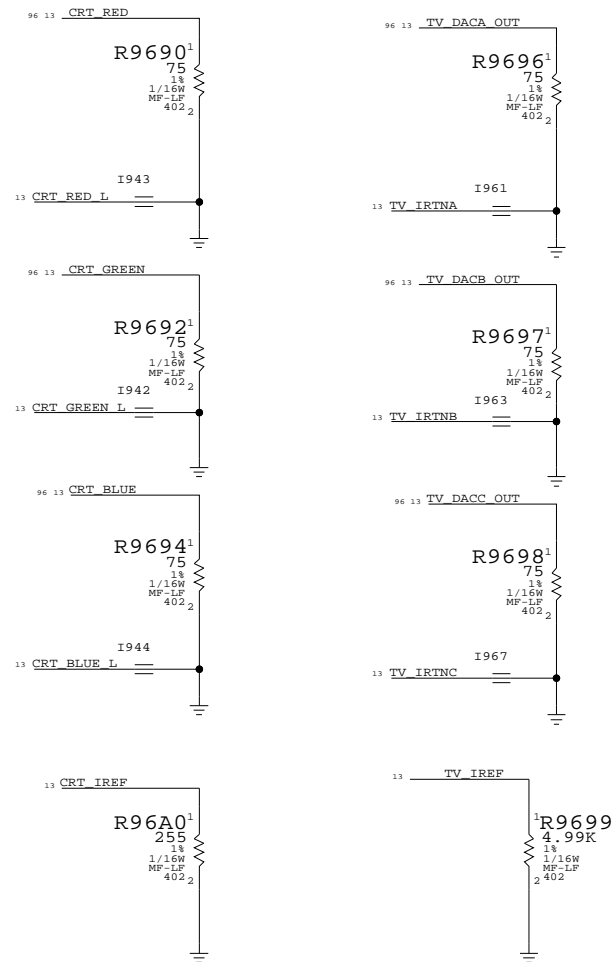
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	SCALE NONE	SHEET 95 OF 97	

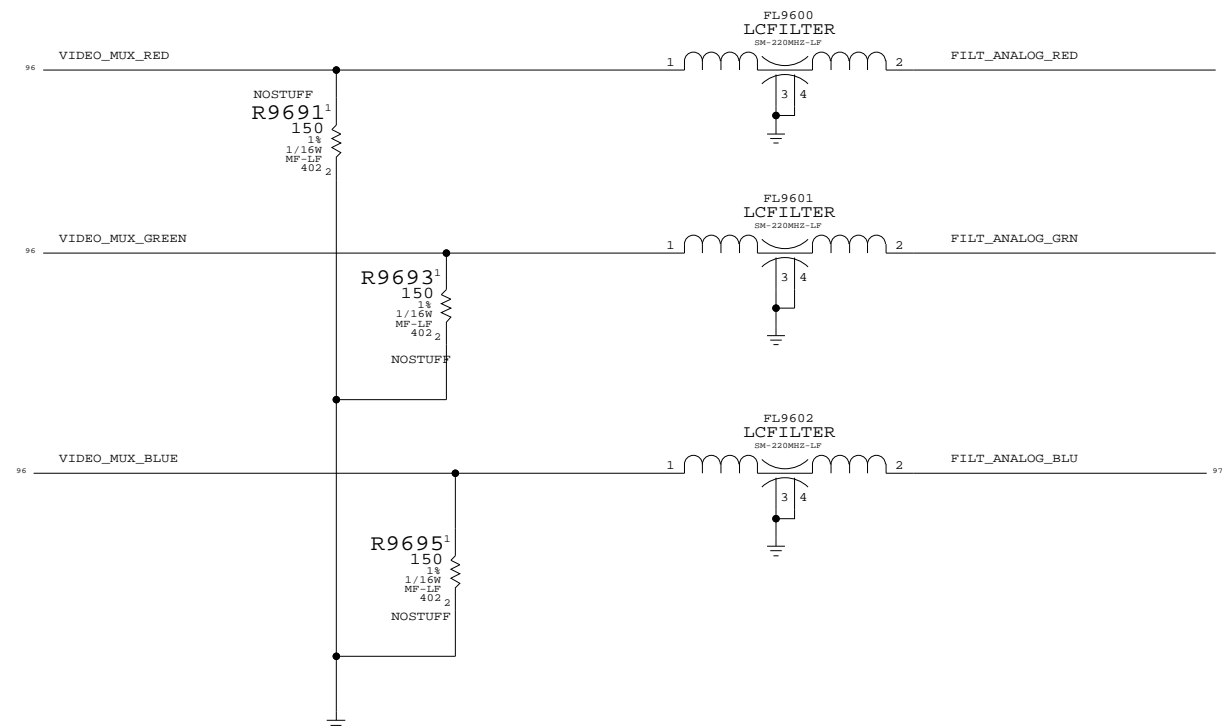
VGA SYNC BUFFERS



PLACE RESISTORS AT NORTHBRIDGE

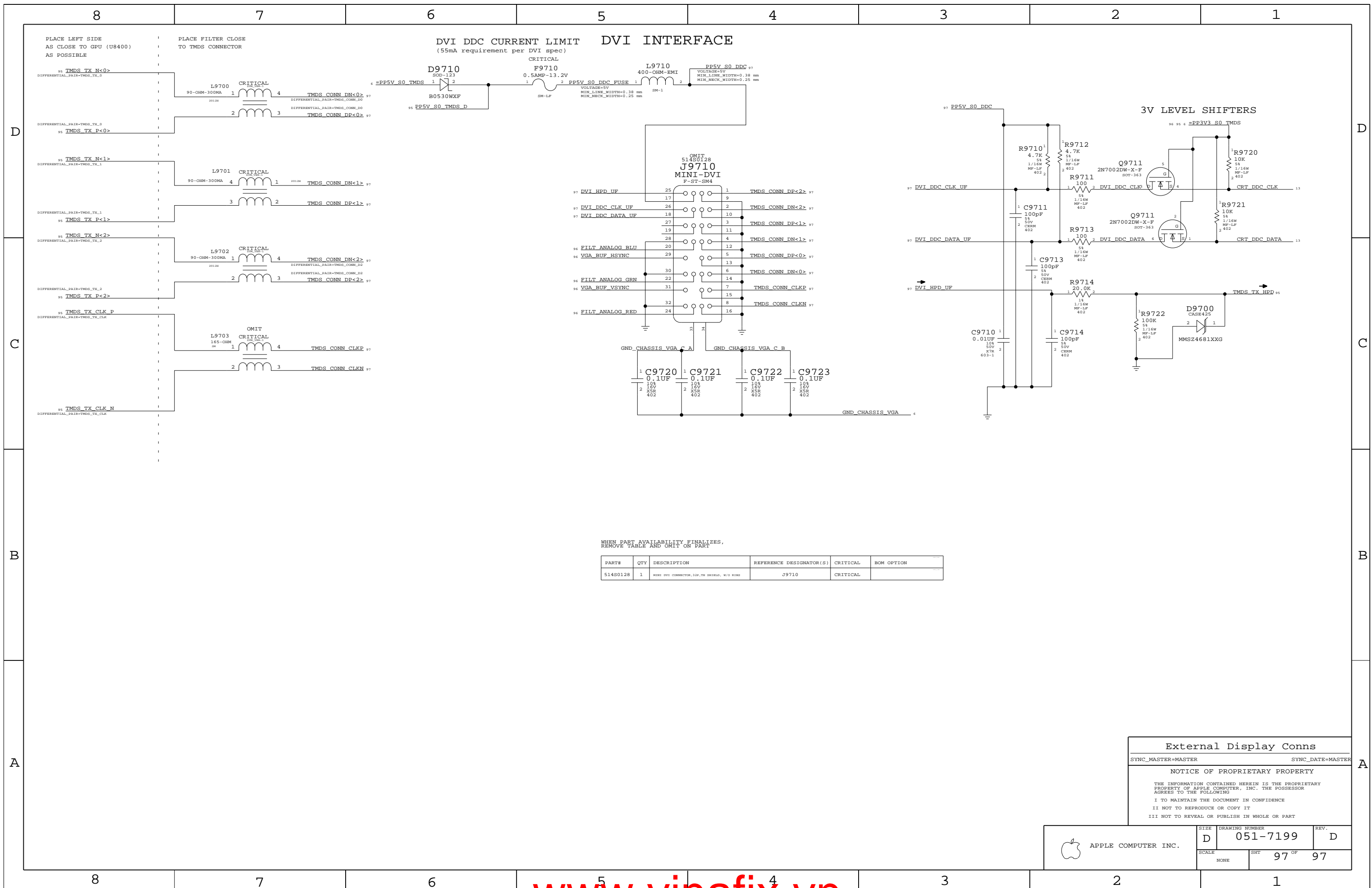


ANALOG FILTERING PLACE BY CONNECTOR



TMDS/Inverter/ExtVGA
 SYNC_MASTER=MASTER SYNC_DATE=MASTER
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SCALE	SHT	96 OF	97
NONE			



DVI DDC CURRENT LIMIT DVI INTERFACE

(55mA requirement per DVI spec)

DVI INTERFACE

CRITICAL

PP5V_S0 DDC 97
VOLTAGE=5V
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm

PP5V_S0 TMS D 95

PP5V_S0 TMS D 95

PP5V_S0 TMS D 95

PP5V_S0 TMS D 95

PP5V_S0 TMS D 95

PP5V_S0 TMS D 95

PP5V_S0 TMS D 95

PP5V_S0 TMS D 95

PP5V_S0 TMS D 95

PP5V_S0 TMS D 95

PP5V_S0 TMS D 95

PP5V_S0 TMS D 95

PP5V_S0 TMS D 95

PP5V_S0 TMS D 95

PP5V_S0 TMS D 95

PP5V_S0 TMS D 95

PP5V_S0 TMS D 95

PP5V_S0 TMS D 95

PP5V_S0 TMS D 95

PP5V_S0 TMS D 95

PP5V_S0 TMS D 95

PP5V_S0 TMS D 95

PP5V_S0 TMS D 95

PP5V_S0 TMS D 95

PP5V_S0 TMS D 95

PP5V_S0 TMS D 95

PP5V_S0 TMS D 95

PP5V_S0 TMS D 95

PP5V_S0 TMS D 95

PP5V_S0 TMS D 95

PP5V_S0 TMS D 95

PP5V_S0 TMS D 95

PP5V_S0 TMS D 95

PP5V_S0 TMS D 95

PP5V_S0 TMS D 95

WHEN PART AVAILABILITY FINALIZES,
REMOVE TABLE AND OMIT ON PART

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514S0128	1	MINI DVI CONNECTOR, 3P, TH SHIELD, W/O RING	J9710	CRITICAL	

External Display Conns

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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SCALE	SHT	97 OF	97
NONE			