### BOARD STACK-UP AND CONSTRUCTION

<table>
<thead>
<tr>
<th>Top</th>
<th>SIGNAL</th>
<th>MLB STACKUP</th>
<th>LAYER</th>
<th>THICKNESS (MM)</th>
<th>TRACK WIDTH (MM)</th>
</tr>
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<tbody>
<tr>
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<tr>
<td>2</td>
<td>GROUND</td>
<td></td>
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<tr>
<td>3</td>
<td>SIGNAL(High Speed)</td>
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<tr>
<td>4</td>
<td>SIGNAL(High Speed)</td>
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<tr>
<td>5</td>
<td>POWER</td>
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<tr>
<td>6</td>
<td>POWER</td>
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<tr>
<td>7</td>
<td>GROUND</td>
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<tr>
<td>8</td>
<td>SIGNAL(High Speed)</td>
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<tr>
<td>10</td>
<td>SIGNAL(High Speed)</td>
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</tr>
<tr>
<td>11</td>
<td>GROUND</td>
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<tr>
<td>BOTTOM</td>
<td>SIGNAL</td>
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</tbody>
</table>

### MLB STACKUP

- **CONFORMAL_COAT**: 0.018
- **L1 SIGNAL**: 0.076
- **L2 SIGNAL**: 0.076
- **L3 SIGNAL**: 0.156
- **L4 SIGNAL**: 0.076
- **L5 GND**: 0.076
- **L6 POWER**: 0.076
- **L7 GND**: 0.076
- **L8 GROUND**: 0.156
- **L9 L10**: 0.076
- **L11 SIGNAL**: 0.076
- **L12 SIGNAL**: 0.076
- **TOTAL**: 1.276

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**CONFIGURATION OPTIONS**

- **SYNC_DATE**: 07/18/2005
- **SYNC_MASTER**: INC

---

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### LVDS Aliases

- **C0608**

### NB CFG Aliases

- **C0610**

### PCI_Express Graphics Aliases

- **C0611**

### SATA Aliases

- **C0612**

### PCI_EXP Aliases

- **C0613**

### Clock Aliases

- **C0614**

### SB Aliases

- **C0615**

### So_DIMM Aliases

- **C0616**

### Ethernet Aliases

- **C0617**

### Signal Alias /Sheet
VCCA DECOUPLING
(CPU INTERNAL PLL POWER 1.5V)

VCCP CORE DECOUPLING
(CPU 10 POWER 1.05V)

VCC CORE DECOUPLING
(CPU CORE POWER)

CPU CORE VID<> SETTINGS

CPU DECAPS & VID<>
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CPU ZONE THERMAL SENSOR

LAYOUT NOTE:
- ADD GND GUARD TRACE FOR CPU_THERMD_P AND LAYOUT NOTE:
- CPU ZONE THERMAL SENSOR

PLACE CPU_THERMD_P NEAR THE CPU_INTERNAL_THERMAL_DIODE

PLACEHOLDER ADT7461A

PLACE U1001 NEAR THE U1200

CRITICAL

www.vinafix.vn
CPU ITP700FLEX DEBUG SUPPORT

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1. CONNECTOR'S FBO PIN: (AND WITH RESET BUTTON)

2. ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU's TCK PIN AND THEN FUSE BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX CONNECTOR'S PRO TCK PIN.

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**DRAWING NUMBER**

**SHEET OF**

**SIZE**

---

**APPEND 004**

**REV.**

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**SYNC_DATE=5/23/05**

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**SYNC_MASTER=MASTER**

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BOM OPTION shown at the top of each group applies to every part below it.

One cap for each side of every RPAK, one cap for every two discrete resistors.

LAYOUT NOTE: PLACE ONE CAP CLOSE TO EVERY TWO PULLUP RESISTORS TERMINATED TO P3/VCC, GND, TERM.

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Value</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>C3000</td>
<td>0.1μF</td>
<td>10V, CERM, 20%</td>
</tr>
<tr>
<td>C3001</td>
<td>0.1μF</td>
<td>10V, CERM, 20%</td>
</tr>
<tr>
<td>C3002</td>
<td>0.1μF</td>
<td>10V, CERM, 20%</td>
</tr>
<tr>
<td>C3003</td>
<td>0.1μF</td>
<td>10V, CERM, 20%</td>
</tr>
<tr>
<td>C3004</td>
<td>0.1μF</td>
<td>10V, CERM, 20%</td>
</tr>
<tr>
<td>C3005</td>
<td>0.1μF</td>
<td>10V, CERM, 20%</td>
</tr>
<tr>
<td>C3006</td>
<td>0.1μF</td>
<td>10V, CERM, 20%</td>
</tr>
<tr>
<td>C3007</td>
<td>0.1μF</td>
<td>10V, CERM, 20%</td>
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<tr>
<td>C3008</td>
<td>0.1μF</td>
<td>10V, CERM, 20%</td>
</tr>
<tr>
<td>C3009</td>
<td>0.1μF</td>
<td>10V, CERM, 20%</td>
</tr>
<tr>
<td>C3010</td>
<td>0.1μF</td>
<td>10V, CERM, 20%</td>
</tr>
<tr>
<td>C3011</td>
<td>0.1μF</td>
<td>10V, CERM, 20%</td>
</tr>
<tr>
<td>C3012</td>
<td>0.1μF</td>
<td>10V, CERM, 20%</td>
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<tr>
<td>C3013</td>
<td>0.1μF</td>
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<tr>
<td>C3014</td>
<td>0.1μF</td>
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<tr>
<td>C3015</td>
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<tr>
<td>C3016</td>
<td>0.1μF</td>
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<tr>
<td>C3017</td>
<td>0.1μF</td>
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<tr>
<td>C3018</td>
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<tr>
<td>C3019</td>
<td>0.1μF</td>
<td>10V, CERM, 20%</td>
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</tbody>
</table>

Memory Active Termination

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If power inputs are not S0, MEMVTT can be used to enable MEMVTT in sleep.

DDR2 Vtt Regulator

Memory Vtt Supply

Synch Date = (MASTER) Sync Master = (MASTER)
CROSS-OVERS ARE IN SCHEMATIC TO EASE ROUTING
PORT POWER CLASS

Enable Port power whenever machine AC Adapter is plugged or system is on state with battery only.

"Snapback" and "Late VG" Protection

LATE-VG PROTECTION POWER

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<table>
<thead>
<tr>
<th>PART#</th>
<th>DESCRIPTION</th>
<th>QTY</th>
<th>REFERENCE DESIGNATOR(S)</th>
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</thead>
<tbody>
<tr>
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</tbody>
</table>

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**BLUETOOTH INTERFACE**

- NOSTUFF 2
- 0.1UF 402 20%
- 10V CERM
- 90-OHM
- 603 6.3V
- 120-OHM-0.3A-EMI 0402-LF 21
- CRITICAL M42B518S0486 1

**USB2_BT_F**

- VOLTAGE=3.3V
- MIN_NECK_WIDTH=0.2MM
- MIN_LINE_WIDTH=0.2MM

- PP3V3_S3_BT_F
- USB2_BT_F_N
- GND_BT_F
- USB2_BT_F_P
- USB2_BT_P
- USB2_BT_N

- =USB2_BT_F_N
- =USB2_BT_F_P
- =USB2_BT_P
- =USB2_BT_N
- =PP3V3_S3_BT

**www.vinafix.vn**
Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits

PLACE RC FILTER CLOSE TO SMC
NOTE: REPLACE J6250 AND J6251 FROM 518S0332 TO 518S0487
AFTER THIS CHANGE, THE PCB WILL USE 518S0332 LANDPATTERN, BUT BOM WILL STUFF 518S0487 PART

DIMM0 TEMPERATURE ZONE

NOTE: REPLACE J6250 AND J6251 FROM 518S0332 TO 518S0487
AFTER THIS CHANGE, THE PCB WILL USE 518S0332 LANDPATTERN, BUT BOM WILL STUFF 518S0487 PART

DIMM1 TEMPERATURE ZONE
R6309 is not needed when sharing SPI flash with ICH7M and Tekoa (LAN chip).

R6307 and R6306 should be placed less than 100 mils from ICH7M.

R6303 should be placed less than 100 mils from flash ROM.
OUT STUFFING OPTIONS FOR ALC882 CODEC

4.5V POWER SUPPLY FOR CODEC

MIN_LINE_WIDTH=0.2MM
MIN_LINE_WIDTH=0.2MM
MIN_LINE_WIDTH=0.2MM
VOLTAGE=4.5V

MIN_NECK_WIDTH=0.2MM
MIN_NECK_WIDTH=0.2MM
MIN_NECK_WIDTH=0.2MM

VOLTAGE=3.3V
MIN_LINE_WIDTH=0.30MM

MIN_LINE_WIDTH=0.2MM
MIN_LINE_WIDTH=0.2MM
MIN_LINE_WIDTH=0.2MM

VOLTAGE=0V
MIN_NECK_WIDTH=0.20MM

VOLTAGE=5V
MIN_LINE_WIDTH=0.60 MM

CASE-B3-SM

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2.5V REGULATORS

1.2V REGULATOR

Vout = 0.5V * (1 + Ra / Rb)

YUKON POWER CONTROL
1.5V/1.05V POWER SUPPLY