POST-PVT RJ45 EB W/ LOCKED BOOTROM

EE DRIS:
RX-RAYMOND XU
DK-DINESH KUMAR
RC-RAY CHANG
MK-MARC KLINGELHOFER
LT-LAWRENCE TAN
LD-LINDA DUNN

Apple Computer Inc.

SCHEM,MLB NO_LDO,M42B
051-7374 C
06/13/07

www.vinafix.vn
### BOARD STACK-UP AND CONSTRUCTION

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<tr>
<th>Layer</th>
<th>Signal</th>
<th>MLB Stackup</th>
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**TOTAL LAYER THICKNESS**

**MLB STACKUP**

**TRACE WIDTH**

---

**CONFIGURATION OPTIONS**

- **COMBINED**
- **BETTER**
- **GOOD**
- **BEST**
- **ACCEL**
- **FET**
- **STANDOFF**
- **NORMAL**
- **FANCY**
- **3V3_IND_3MM**
- **3V3_IND_2MM8**
- **ONEWIRE_ALWAYSON**
- **ONEWIRE_PWRCTL**
- **ONEWIRE_PULLUP**
- **ONEWIRE_PULLUP_OLD**
- **USB_E_OC_PU**
- **USB_D_OC_PU**
- **USB_C_OC_PU**
- **NO_REBOOT_MODE**
- **NBCFG_SDVO_AND_PCIE**
- **NBCFG_PEG_REVERSE**
- **NBCFG_DYN_ODT_DISABLE**
- **NBCFG_DMI_X2**
- **NBCFG_DMI_REVERSE**
- **MEMVTT_EN_PU**
- **LEMENU**
- **ITP**
- **INVERTER_UNBUF**
- **INVERTER_BUF**
- **POST-RAMP-DIMM35**
- **PVT-DIMM**
- **TPM**
- **BEST-ST**
- **GOOD-KIONIX**
- **BETTER-ST**
- **ST MICRO**
- **BEST-KIONIX**
- **KIONIX**
- **APPLE COMPUTER INC.**

---

**Page Notes**

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**www.vinafix.vn**
### Power Supply NO_TESTS

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### Other Func Test Points

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### LVDS B_DATA_P1_SPN

TRUE LVDS B_DATA_P1_SPN
TRUE LVDS B_DATA_N2_SPN
TRUE LVDS B_CLK_P_SPN
TRUE LVDS B_CLK_N_SPN

### LVDS B_DATA_N1_SPN

TRUE LVDS B_DATA_N1_SPN

### CK410_SRC8_P

TRUE CK410_SRC8_P
TRUE CK410_SRC8_N
TRUE CK410_SRC7_P_SPN
TRUE CK410_SRC7_N_SPN
TRUE CK410_SRC6_P
TRUE CK410_SRC5_P_SPN
TRUE CK410_SRC5_N_TRUE
TRUE CK410_SRC4_N
TRUE CK410_SRC2_P
TRUE CK410_SRC1_P_SPN

### 3V3S5_COMP

3V3S5_COMP
CK410_SRC6_N
CK410_SRC5_N
CK410_SRC4_N
CK410_SRC2_P
CK410_SRC1_N_SPN

### 3V3S5_FSET

3V3S5_FSET

### 5VS5_RUNSS

5VS5_RUNSS

### IMVP6_COMP

IMVP6_COMP

### SMC_FAN_3_TACH

SMC_FAN_3_TACH

### ENET_MDI_TRAN_P<3>

ENET_MDI_TRAN_P<3>
ENET_MDI_TRAN_P<2>

### 1V05S0_FSET

1V05S0_FSET

###苹le COMPUTER INC.

APPLE COMPUTER INC.
CPU CORE VID<> SETTINGS

CPU DECAPS & VID<>

VCCA DECOUPLING
(CPU INTERNAL PLL POWER 1.5V)

VCCP CORE DECOUPLING
(CPU IO POWER 1.05V)

VCC CORE DECOUPLING
(CPU CORE POWER)

IF WE USE LOW ESL CAP, THEN WE CAN USE 20PCS 22UF CAP

CPU_VID<3>
CPU_VID<5>
CPU_VID<1>
CPU_VID<2>
CPU_VID<4>

R0921~R0927 FOR CPU VOLTAGE MANUAL SETTING

UNIT: V

DUAL CORE
SV CPU
VCCFM 1.1625
VCCFM TBD
TBD

SINGLE CORE
SV CPU
VCCFM 1.1625
VCCFM TBD
TBD

DUAL CORE
LV CPU
VCCFM 1.0
VCCFM 1.1625
TBD

ULV CPU
VCCFM TBD
VCCFM TBD
TBD

MIN
TYP
MAX

0
1.1625
1.30

TBD
TBD
TBD

TYP

VCCHFM
VCCLFM
VCCHFM
VCCLFM

CPU DECAPS & VID<>

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CPU ITP700FLEX DEBUG SUPPORT

ITP TCK SIGNAL LAYOUT NOTE:
ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S TCK PIN AND THEN FUSE BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX CONNECTOR'S PROG PIN.

(AND WITH RESET BUTTON)
Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie VSSA_CRTDAC and VCC_SYNC to GND. Tie HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core rail, tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and TV-Out Disable filter components. Unused DAC outputs must remain powered, but can omit Component: DACA, DACB & DACC

S-Video: DACB & DACC only

Composite: DACA only

TV-Out Signal Usage:
- VCCD_LVDS must remain powered with proper decoupling.
- Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used, connect SDVO voluntarily.

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SYNC_MASTER=NB SYNC_DATE=07/25/2005
Layout Note:
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PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR

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Internal pull-up
Internal pull-up
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Lane Reversal
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PROBABLY NOT NEEDED
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PCIE Graphics
PCIE Graphics
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PCIE Graphics
PCIE Graphics
PCIE Graphics
PCIE Graphics

Low = Normal
Low = Reversed
Low = Reversed
Low = Reversed
Low = Reversed
Low = Reversed
Low = Reversed
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Low = Reversed
Low = Reversed
Low = Reversed
Low = Reversed
Low = Reversed

Intel pull-ups
Intel pull-ups
Intel pull-ups
Intel pull-ups
Intel pull-ups
Intel pull-ups
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Intel pull-ups
Intel pull-ups
Intel pull-ups
Intel pull-ups
Intel pull-ups

11 = Normal Operation
10 = All-Z Mode Enabled
01 = XOR Mode Enabled
00 = Partial Clock Gating Disable

CONF_DATE=06/28/2005
CONF_MASTER=NB

www.vinafix.vn
Page Notes

- DDR2 VRef
  Over 0.2uf per connector.

- Yellow uses 10K divider and TLV2463 to drive MCH and DIMM connectors.
  Use suppliers listed on page 45.

- DDR2 Bypass Caps
  (For return current.)

- The 4.7uF and 1.0uF caps can be changed to 2.2uF caps when they get cheaper.

- DDR2 SO-DIMM Connector A
  Vertical orientation.

- Notice of Proprietary Property
  The design of this product was inspired by the X270-A40, but was independently created.

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LAYOUT NOTE: PLACE ONE CAP CLOSE TO EVERY TWO PULLUP RESISTOR TERMINATED TO PPDEN_S0_MEM_TERM.
Memory Vtt Supply

- Power aliases required by this page:
  - (NONE)

- Signal aliases required by this page:
  - (NONE)

- Power aliases required by this page:
  - (NONE)

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**MEMVTT_EN** can be used to disable MEMVTT in sleep.

**DDR2 Vtt Regulator**

- If power inputs are not S0, disable MEMVTT in sleep.

- **C3101**
  - 10uF
  - 20%
  - X5R
  - 6.3V

- **U3100**
  - BD3533FVM
  - MSOP-8

- **R3100**
  - 1K
  - MF-LF
  - 1/16W
  - 5%

- **C3102**
  - 10uF
  - 20%
  - X5R
  - 6.3V

- **C3103**
  - 0.1uF
  - 16V
  - 10%
  - X5R

- **C3104**
  - 2.2uF
  - 20%
  - X5R
  - 6.3V

- **C3105**
  - 150UF
  - POLY
  - 6.3V

- **C3100**
  - 1uF
  - 6.3V
  - 10%
  - CERM

- **R3104**
  - 220
  - 1/16W
  - MF-LF
  - 5%

- **C3106**
  - 402
  - 1uF
  - 6.3V
  - 10%
  - CERM

- **C3107**
  - 1/16W
  - 402
  - 16V
  - 10%
  - X5R

- **VOLTAGE=1.8V**

- **MIN_NECK_WIDTH=0.2 mm**

- **MIN_LINE_WIDTH=0.2 mm**

- **PP0V9_S0_MEM_REG**

- **PP1V8_S3_MEMVTT**

- **PP5V_S0_MEMVTT**

- **SYNC_DATE=(MASTER)**

- **SYNC_MASTER=(MASTER)**

- www.vinafix.vn
OCD detect need less than 100ms include OS latency

www.vinafix.vn
PAGE NOTES
7/26/2005 - CONNECTED PIN E10 TO GND
6/22/2005 - REMOVED CONSTRAINT SETS AS THEY WILL BE MANAGED ON BOARD SIDE
6/22/2005 - CHANGED CLK, PME, DIFF PAIR NAMES TO BE RE-USE COMPLIANT
6/21/2005 - CHANGED PCI_ID TO AD19 (PER ARCHITECTURAL DEFINITION)
5/19/2005 - FIRST REVISION OF PAGE

PCI_PME_FW_L - DEDICATED PME FOR FIREWIRE (SB GPIO1)

OUTPUT
FW_B_TPA_P/N, FW_B_TPB_P/N, FW_B_TPBIAS - PORT 1 FIREWIRE DIFF PAIRS

INPUT/OUTPUT
PCI_CLK_FW - NEED TO REFERENCE TO ALIAS PAGE
PCI_GNT3_L - PCI GRANT FROM SB
=PP3V3_S0_PCI - 3.3V POWER FOR PCI FIREWIRE (MOBILE: OFF DURING SLEEP)

THIS IS FROM ICH-7M
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Sync master = NB
Sync date = 06/30/2005

LPC+ Debug Connector

GPIO15 516S002

CRITICAL
J6000 F-ST-5047

8 7 6 5 4 3 2 1

SM1

NOSTUFF

B A C D

D C B A
Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits
NOTE: REPLACE J6250 AND J6251 FROM 518S0332 TO 518S0452 AND THEN 518S0487 AFTER THIS CHANGE, THE SCHEMATIC DOES NOT MATCH THE PCB ON THESE TWO LOCATIONS.

NOTE: REPLACE J6250 AND J6251 FROM 518S0332 TO 518S0452 AND 518S0487 AFTER THIS CHANGE, THE SCHEMATIC DOES NOT MATCH THE PCB ON THESE TWO LOCATIONS.
R6309 IS NOT NEEDED WHEN SHARING SPI FLASH WITH ICH7M AND TEKOA (LAN CHIP)

R6307 AND R6306 SHOULD BE PLACED LESS THAN 100 MILS FORM ICH7M

R6303 SHOULD BE PLACED LESS THAN 100 MILS FORM FLASH ROM
YUKON POWER CONTROL

2.5V REGULATORS

1.2V REGULATOR
1.8V POWER SUPPLY
PBUS SUPPLY / BATTERY CHARGER
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