1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

M42B MLB SCHEMATIC

10/2/2007

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
C		536501	PRODUCTION RELEASED	10/02/07	?

Schematic / PCB #'s

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-7370	1	SCHEM,M42B,MLB	SCH	
820-2213	1	PCBF,M42B,MLB	PCB	

EE DRIS:

RX-RAYMOND XU
DK-DINESH KUMAR
RC-RAY CHANG
MK-MARC KLINGELHOFER
LT-LAWRENCE TAN
LD-LINDA DUNN

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES °
DO NOT SCALE DRAWING
THIRD ANGLE PROJECTION

METRIC

DRAFTER | DESIGN CK | ENG APPD | MFG APPD | QA APPD | DESIGNER | RELEASE | SCALE NONE

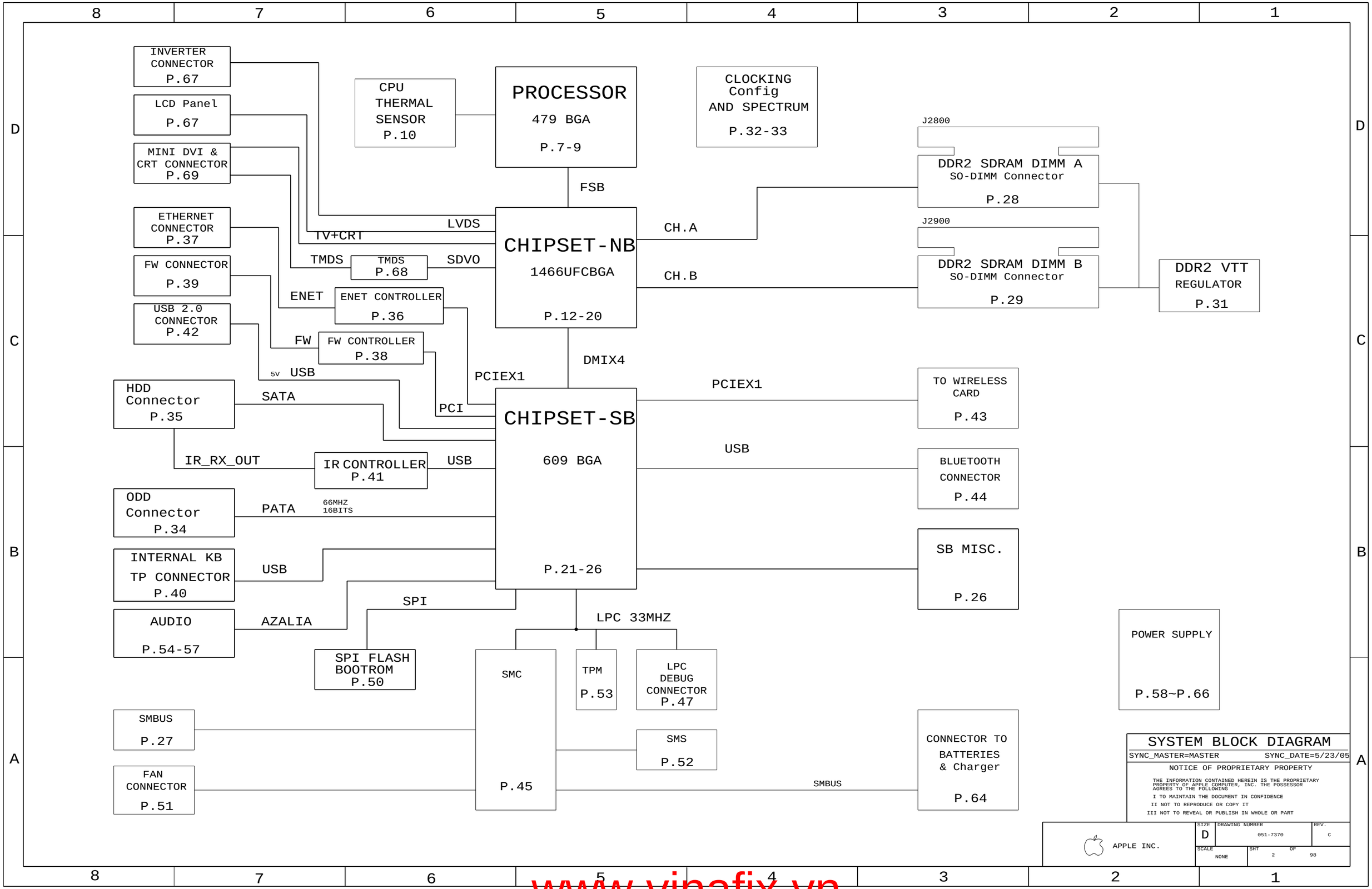
MATERIAL/FINISH NOTED AS APPLICABLE | SIZE D

APPLE INC.

TITLE: SCHEM,MLB,M42B

DRAWING NUMBER 051-7370 | REV. C

SHT 1 OF 98



SYSTEM BLOCK DIAGRAM

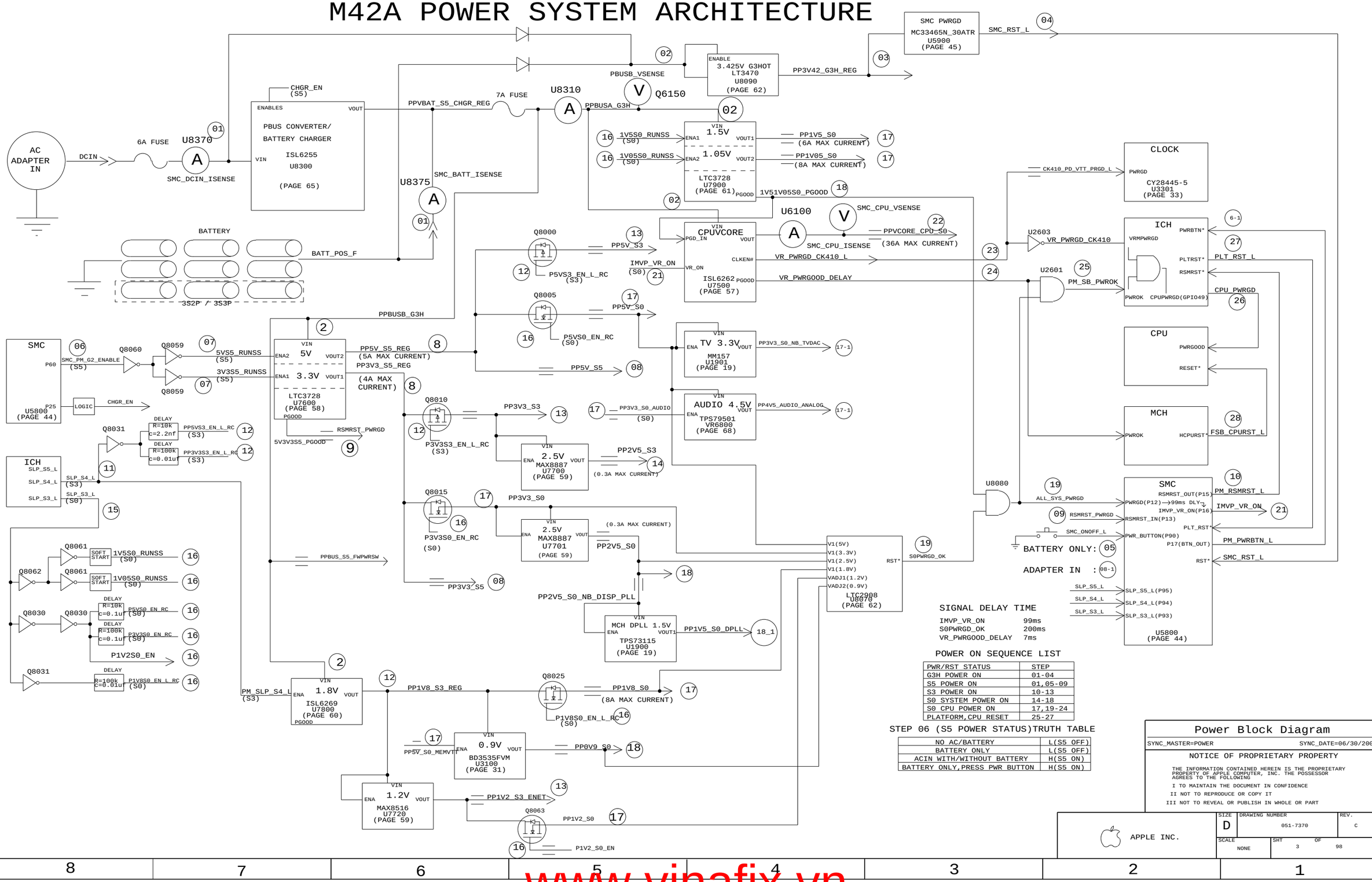
SYNC_MASTER=MASTER SYNC_DATE=5/23/05

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C

SCALE NONE SHT 2 OF 98

M42A POWER SYSTEM ARCHITECTURE



Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

BOM OPTION

BOMOPTION	M42A GOOD ST MICRO 630-7795 EVT	M42A BETTER ST MICRO 630-7796 EVT	M42A BEST KIONIX 630-7799 EVT	M42A GOOD KIONIX 630-7798 EVT	M42A BETTER KIONIX 630-7736 EVT	M42A BEST ST MICRO 630-7797 EVT
1V51V05S0_CONT						
1V51V05S0_SKIP	V	V	V	V	V	V
5V3V3S3_CONT						
5V3V3S3_SKIP	V	V	V	V	V	V
ACCEL_KIONIX			V	V	V	
ACCEL_ST	V	V				V
INVERTER_BUF	V	V	V	V	V	V
INVERTER_UNBUF						
ITP						
LEMENU	V	V	V	V	V	V
MEMVTT_EN_PU	V	V	V	V	V	V
NBCFG_DMI_REVERSE						
NBCFG_DMI_X2						
NBCFG_DYN_ODT_DISABLE						
NBCFG_PEG_REVERSE						
NBCFG_SDVO_AND_PCIE						
NBCFG_VCC_1V5						
NO_REBOOT_MODE						
USB_C_OC_PU	V	V	V	V	V	V
USB_D_OC_PU	V	V	V	V	V	V
USB_E_OC_PU	V	V	V	V	V	V
GOOD	V			V		
BETTER		V			V	
BEST			V			V
M42A_PGM	V	V	V	V	V	V
ONEWIRE_PULLUP	V	V	V	V	V	V
ONEWIRE_PULLUP_OLD						
ONEWIRE_PU_PROT	V	V	V	V	V	V
ONEWIRE_PU_ACOK						
ONEWIRE_PWRCTL	V	V	V	V	V	V
ONEWIRE_ALWAYSON						
3V3_IND_2MM8	V	V	V	V	V	V
3V3_IND_3MM						
NORMAL	V	V		V	V	
FANCY			V			V
STANDOFF	V	V	V	V	V	V
FET_FDN6296	V	V	V	V	V	V
FET_STL8NH3LL						
GOOD-ST	V					
BETTER-ST		V				
BEST-KIONIX			V			
GOOD-KIONIX				V		
BETTER-KIONIX					V	
BEST-ST						V
TPM						
PVT-DIMM						
POST-RAMP-DIMM35	V	V	V	V	V	V
M42A	V	V	V	V	V	V
M42B	V	V	V	V	V	V

BOARD STACK-UP AND CONSTRUCTION

Top		SIGNAL
2		GROUND
3		SIGNAL(High Speed)
4		SIGNAL(High Speed)
5		GROUND
6		POWER
7		POWER
8		GROUND
9		SIGNAL(High Speed)
10		SIGNAL(High Speed)
11		GROUND
BOTTOM		SIGNAL

MLB STACKUP

LAYER	THICKNESS (MM)	TRACE WIDTH (MM)
CONFORMAL_COAT	0.018	
L1 SIGNAL(TOP)	0.047	0.1
L1-L2	0.07	
L2 GROUND	0.014	---
L2-L3	0.076	
L3 SIGNAL	0.014	0.079
L3-L4	0.156	
L4 SIGNAL	0.014	0.079
L4-L5	0.076	
L5 GND	0.014	---
L5-L6	0.07	
L6 POWER	0.031	---
L6-L7	0.076	
L7 POWER	0.031	---
L7-L8	0.07	
L8 GROUND	0.014	---
L8-L9	0.076	
L9 SIGNAL	0.014	0.1
L9-L10	0.156	
L10 SIGNAL	0.014	0.1
L10-L11	0.076	
L11 GROUND	0.014	0.1
L11-L12	0.07	
L12 SIGNAL(BOTTOM)	0.047	0.1
CONFORMAL_COAT	0.018	
TOTAL	1.276	---

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
337S3389	1	IC,MEROM,CPU 2.0GHZ,479 PGA	U0700	GOOD
337S3391	1	IC,MEROM,CPU 2.16GHZ,479 PGA	U0700	BETTER
337S3391	1	IC,MEROM,CPU 2.16GHZ,479 PGA	U0700	BEST

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
338S0268	1	IC,FW32306,1394A LINK,BGA,129P	U4400	LEMENU
338S0270	1	IC,88E8053,GIGABIT ENET XCVR,64P QFN, NO	U4101	LEMENU
359S0109	1	IC,SLG8LP436,CLOCK GEN,68PIN QFN	U3301	LEMENU

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
341S2132	1	IC, 16MBIT 8-PIN SPI SERIAL FLASH,SOIC8	U6301	M42A_PGM
341S1797	1	IC,EEPROM,SERIAL IIC,8KBIT,SO8	U4102	M42A_PGM
341S2133	1	IC,SMC,176P BGA,HS8/2116	U5800	M42A_PGM
341S1890	1	IC,PSOC+W/USB,56P,MLF,CY8C24794	U5100	M42A_PGM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MMX6MM	EEE:YCN	CRITICAL	BEST-KIONIX
826-4393	1	LBL,P/N LABEL,PCB,28MMX6MM	EEE:YCM	CRITICAL	BETTER-KIONIX
826-4393	1	LBL,P/N LABEL,PCB,28MMX6MM	EEE:YCL	CRITICAL	GOOD-KIONIX

CONFIGURATION OPTIONS

SYNC_MASTER=SMC SYNC_DATE=07/18/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 4 OF 98	

Functional Test Points

Power Supply NO_TESTs

NO_TEST

I93		IMVP6_RBIAS	58A4 58B7
I94		IMVP6_COMP	58A4 58B7
I95		5VS5_RUNSS	59B4 63C7
I96		1V5S0_RUNSS	62B5 63B7
I101		1V8S3_COMP	61B6
I102		1V8S3_FSET	61C6
I103	TRUE	3V3S5_COMP	
I104	TRUE	3V3S5_FSET	
I106	TRUE	1V05S0_COMP	
I105	TRUE	1V05S0_FSET	
I107	TRUE	P3V42G3H_FB	63D2

CLOCK NO_TESTS

NO_TEST

I111	TRUE	CK410_CPU0_N	32C4 33D5
I112	TRUE	CK410_CPU0_P	32C4 33D5
I113	TRUE	CK410_CPU1_N	32C4 33D5
I114	TRUE	CK410_CPU1_P	32C4 33D5
I115	TRUE	CK410_CPU2_ITP_SRC10_N	32C4 33D5
I116	TRUE	CK410_CPU2_ITP_SRC10_P	32C4 33D5
I117	TRUE	CK410_DOT96_27M_N	32A4 33B5
I118	TRUE	CK410_DOT96_27M_P	32A4 33B5
I119	TRUE	CK410_LVDS_N	32B4 33A5
I120	TRUE	CK410_LVDS_P	32B4 33A5
I122	TRUE	CK410_PCI4_CLK_SPN	
I122	TRUE	CK410_PCIF1_CLK	32B6 33D8
I123	TRUE	CK410_SRC1_N_SPN	6B3
I122	TRUE	CK410_SRC1_P_SPN	6B3
I123	TRUE	CK410_SRC2_N	32B4 33C5
I183	TRUE	CK410_SRC2_P	32B4 33C5
I184	TRUE	CK410_SRC3_N_SPN	6B3
I185	TRUE	CK410_SRC3_P_SPN	6B3
I186	TRUE	CK410_SRC4_N	32B4 33B5
I187	TRUE	CK410_SRC4_P	32B4 33B5
I188	TRUE	CK410_SRC5_N	32B4 33C5
I189	TRUE	CK410_SRC5_P	32B4 33C5
I190	TRUE	CK410_SRC6_N	32B4 33C5
I191	TRUE	CK410_SRC6_P	32B4 33D5
I192	TRUE	CK410_SRC7_N_SPN	6B3
I193	TRUE	CK410_SRC7_P_SPN	6B3
I194	TRUE	CK410_SRC8_N	32A4 33C5
I195	TRUE	CK410_SRC8_P	32A4 33C5
I196	TRUE	CK410_SRC_CLKREQ1_L_SPN	6B3
I197	TRUE	CK410_SRC_CLKREQ3_L_SPN	6B3
I198	TRUE	CK410_SRC_CLKREQ8_L	32A4 33A5

FIREWARE NO_TESTS

NO_TEST

I199	TRUE	FW_B_TPA_N_SPN	6D1
I200	TRUE	FW_B_TPA_P_SPN	6D1
I201	TRUE	FW_B_TPBIAS_SPN	6D1
I202	TRUE	FW_B_TPB_N_SPN	6D1
I203	TRUE	FW_B_TPB_P_SPN	6D1
I204	TRUE	FW_C_TPA_N_SPN	6D1
I205	TRUE	FW_C_TPA_P_SPN	6D1
I206	TRUE	FW_C_TPBIAS_SPN	6D1
I207	TRUE	FW_C_TPB_N_SPN	6D1
I208	TRUE	FW_C_TPB_P_SPN	6D1

LVDS NO_TESTS

NO_TEST

I209	TRUE	LVDS_B_CLK_N_SPN	6D5
I210	TRUE	LVDS_B_CLK_P_SPN	6D5
I211	TRUE	LVDS_B_DATA_N0_SPN	6D5
I212	TRUE	LVDS_B_DATA_N1_SPN	6D5
I213	TRUE	LVDS_B_DATA_N2_SPN	6D5
I214	TRUE	LVDS_B_DATA_P1_SPN	6D5
I215	TRUE	LVDS_B_DATA_P2_SPN	6D5

ETHERNET NO_TESTS

NO_TEST

I216	TRUE	ENET_MDI_TRAN_P<2>	37B5
I217	TRUE	ENET_MDI_TRAN_N<2>	37B5
I218	TRUE	ENET_MDI_TRAN_P<3>	37B5

NO_TEST

I219	TRUE	SMC_FAN_3_TACH	45B8 46C3
I220	TRUE	ALS_LEFT	45A8 46C3

Fan Connectors

FUNC_TEST

I12	TRUE	=PP5V_S0_FAN_RT	51C4 64D3
I15	TRUE	FAN_RT_PWM	51B3
I16	TRUE	FAN_RT_TACH	51C3
I17	TRUE	=PP3V3_S0_FAN_RT	51C4 64A6
I150	TRUE	SMC_FAN_1_CTL	45B8 51B4
I149	TRUE	SMC_FAN_1_TACH	45B8 51C4

LPC+ Debug Connector

FUNC_TEST

I20	TRUE	=PP3V42_G3H_LPCPLUS	47C6 64D1
I19	TRUE	=PP5V_S0_LPCPLUS	47C6 64D3
I18	TRUE	LPC_AD<0>	21D4 45D8 47C6 53C6
I17	TRUE	LPC_AD<1>	21D4 45D8 47C6 53C6
I71	TRUE	LPC_FRAME_L	21C5 45C8 47C6 53C6
I72	TRUE	PM_CLKRUN_L	23C8 38A5 45D5 47C6 53C6
I73	TRUE	BOOT_LPC_SPI_L	22B3 45C8 47C6
I74	TRUE	SMC_TMS	45B5 46C6 47C6
I75	TRUE	DEBUG_RST_L	26B1 47C6
I76	TRUE	SMC_TRST_L	45C1 47C6
I77	TRUE	SMC_TDO	45C5 46C6 47B6
I78	TRUE	SMC_MD1	45C2 47B6
I79	TRUE	SMC_TX_L	45C8 46B2 46D6 47B6
I80	TRUE	FWH_INIT_L	6B2 21C4 47C5
I81	TRUE	PCI_CLK_PORT80_LPC	33D6 47C5
I82	TRUE	LPC_AD<2>	21D4 45D8 47C5 53C6
I83	TRUE	LPC_AD<3>	21D4 45D8 47C5 53C6
I84	TRUE	INT_SERIRQ	23C8 45C8 47C5 53C6
I85	TRUE	PM_SUS_STAT_L	23C5 45D5 46D3 47C5 53C6
I86	TRUE	SMC_TDI	45C5 46C6 47C5
I87	TRUE	SMC_TCK	45C5 46C6 47C5
I88	TRUE	SMC_RST_L	45C3 46D7 47C5
I89	TRUE	SMC_NMI	45C1 47B5
I91	TRUE	SMC_RX_L	45C8 46B2 46D6 47B5
I90	TRUE	SV_SET_UP	23B6 23C3 47B5

Other Func Test Points

FUNC_TEST

I62	TRUE	=PP1V05_S0_REG	62B1 64D8

SMBus FUNC_TEST

I182

	TRUE	SMBUS_SMC_MLB_SCL	27C5
I183	TRUE	SMBUS_SMC_MLB_SDA	27B5

FIREWIRE FUNC_TEST

I152	TRUE	PPFW_SWITCH	39D4

SLEEP LED FUNC_TEST

I155	TRUE	SYS_LED_ANODE	35C5 46A3

SMC FUNC_TEST

I145	TRUE	SMC_LID	40C4 45B5 46C6 65A8
I146	TRUE	SMC_MANUAL_RST_L	46D8
I156	TRUE	SMC_CPU_VSENSE	45D5 48B1

Power Supply FUNC_TEST

I160	TRUE	ALL_SYS_PWRGD	26A5 45D8 63B1
I161	TRUE	PPVCORE_CPU_S0	64D7
I162	TRUE	PP1V05_S0	64D7
I140	TRUE	PP1V5_S0	64C7
I163	TRUE	PP1V8_S0	64C7
I165	TRUE	PP2V5_S0	64B7
I166	TRUE	PP3V3_S0	64B7
I168	TRUE	PP5V_S0	64D4
I167	TRUE	PP1V2_S3	64C4
I169	TRUE	PP1V8_S3	64C4
I170	TRUE	PP2V5_S3	64C4
I172	TRUE	PP3V3_S3	64B4
I171	TRUE	PP5V_S3	64B4
I177	TRUE	PP3V3_S5	64A4
I178	TRUE	PP5V_S5	64A4
I176	TRUE	PP3V42_G3H	64D1
I174	TRUE	PPBUSA_G3H	
I175	TRUE	PPBUSB_G3H	64C1
I179	TRUE	PP18V5_G3H	64C1
I181	TRUE	PP0V9_S0	64D7

Battery Digital Connector

FUNC_TEST

I1	TRUE	SMC_BS_ALRT_L	45C5 46C6 65A2
I3	TRUE	SMBUS_BATT_SCL_F	65B6
I4	TRUE	SMBUS_BATT_SDA_F	65A6
I2	TRUE	BATT_IN	
I177	TRUE	BATT_POS	65A6
I160	TRUE	BATT_NEG	65A6

Audio FUNC_TEST

I9	TRUE	PP5V_S0_AUDIO_PWR	
I11	TRUE	PP5V_S0_AUDIO	
I10	TRUE	GND_AUDIO_PWR	64B2
I21	TRUE	GND_AUDIO_CODEC	64B2
I22	TRUE	ACZ_SDATAIN<0>	21C7 54D7
I24	TRUE	ACZ_SDATAOUT	21C7 54D7
I23	TRUE	ACZ_BITCLK	21C7 54D7
I25	TRUE	ACZ_RST_L	21C7 54C7 57C3
I45	TRUE	ACZ_SYNC	21C7 54D7

Battery FUNC_TEST

I29	TRUE	SMC_BATT_ISET	45B5 66B7
I32	TRUE	SMC_BATT_CHG_EN	45D8 46B6 66A4
I31	TRUE	SMC_BC_ACOK	45C5 46B6 65C3 65C7 66A5
I33	TRUE	SMC_PS_ON	39C6 45D5 46B3 65C3
I36	TRUE	SMC_BATT_TRICKLE_EN_L	45D8 46B6 66A3
I38	TRUE	SYS_ONEWIRE	45B8 46D6 65C8

USB FUNC_TEST

I44	TRUE	TP_USBP_E	6C2
I47	TRUE	TP_USBN_E	6C2
I46	TRUE	TP_USBP_F	
I48	TRUE	TP_USBN_F	

DC-JACK FUNC_TEST

I57	TRUE	ACIN_ENABLE_GATE	65C3

Battery charger FUNC_TEST

I58	TRUE	PPVBAT_G3H_CHGR_OUT	66B5 66C2

INVERTER CONNECTOR FUNC_TEST

I60	TRUE	PPBUS_ALL_INV_CONN	67D3
I59	TRUE	INV_GND	67D2
I61	TRUE	PP5V_INV_F	67D3
I63	TRUE	INV_BKLIGHT_PWM_L	67D2

FUNC TEST 1 OF 2

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C

SCALE	SHT	OF
NONE	5	98

(EMI PAD FOR INVERTER GONNECTOR)

67C2 INVT_CHGND — 1 ZS0620 EMI-SPRING CLIP-SM-M42

NC — 1 ZS0621 SM (SPKR-MIC-CLIP-M42)

CHASSIS GND

BATTERY,AUDIO,DIP DIMM CONNECTOR CHASSIS GND

GND_CHASSIS_IO 6C7 — 1 OMIT Z0606 5R2P3-7SQB

65A6 =GND_BATT_CHGND
56B8 =GND_CHASSIS_AUDIO_JACK
=GND_CHASSIS_AUDIO_SPKRCONN
57A6 =GND_CHASSIS_AUDIO_MIC
=GND_CHASSIS_AUDIO_SHIELD1
=GND_CHASSIS_AUDIO_SHIELD2
=GND_CHASSIS_AUDIO_SHIELD3
28A5 =GND_CHASSIS_DIPDIMM_LEFT

SATA,LVDS CONNECTOR CHASSIS GND

GND_CHASSIS_SATA 35C8 — 1 OMIT Z0607 6P5R2P6-5P5B
VOLTAGE=0V MAKE_BASE=TRUE

67B2 67A2 =GND_CHASSIS_LVDS

C0607 0.1UF 10% 16V X5R 402
C0608 0.01UF 10% 16V CERM 402

DCIN CONNECTOR CHASSIS GND

GND_CHASSIS_DCIN — 1 OMIT Z0602 5R2P3-7SQB
VOLTAGE=0V MAKE_BASE=TRUE

65C8 =GND_DCIN_CHGND
37A4 =GND_CHASSIS_RJ45
69C3 69A4 =GND_CHASSIS_TMDS_UPPER

C0630 0.1UF 10% 16V X5R 402

I/O CONNECTOR CHASSIS GND

GND_CHASSIS_IO 6D7 — 1 OMIT Z0608 5P0R2P3-7BLB
VOLTAGE=0V MAKE_BASE=TRUE

39A1 =GND_CHASSIS_FW_DOWN
42C4 42C2 42A4 42A2 =GND_CHASSIS_USB

C0610 0.1UF 10% 16V X5R 402
C0611 0.01UF 10% 16V CERM 402

DIP DIMM CONNECTOR CHASSIS GND

GND_CHASSIS_CENTER — 1 OMIT Z0610 5R2P3-7SQB
VOLTAGE=0V MAKE_BASE=TRUE

29A5 28D5 =GND_CHASSIS_DIPDIMM_CENTER

C0616 0.1UF 10% 16V X5R 402
C0617 0.01UF 10% 16V CERM 402

DIP DIMM CONNECTOR CHASSIS GND

GND_CHASSIS_RIGHT — 1 OMIT Z0609 5R2P3-7SQB
VOLTAGE=0V MAKE_BASE=TRUE

29D4 =GND_CHASSIS_DIPDIMM_RIGHT

C0614 0.1UF 10% 16V X5R 402
C0615 0.01UF 10% 16V CERM 402

GND_CHASSIS_CPU — 1 OMIT Z0601 5R2P3-7SQB

C0612 0.1UF 10% 16V X5R 402
C0613 0.01UF 10% 16V CERM 402

GND_CHASSIS_FANSCREW — 1 OMIT Z0611 5R2P3-7B

C0618 0.1UF 10% 16V X5R 402
C0619 0.01UF 10% 16V CERM 402

DIGITAL GND SCREW HOLE OMIT

NB_RIGHT_DOWN_SCREW — 1 OMIT Z0603 STDOFF-4.5OD3.95H-1.1-3.7-TH1

R0612 0 5% 1/16W MF-LF 402

CPU_THERMAL_SCREW_UP — 1 OMIT Z0604 STDOFF-4.5OD3.95H-1.1-3.7-TH1

R0610 0 5% 1/16W MF-LF 402

CPU_THERMAL_SCREW_DOWN — 1 OMIT Z0605 STDOFF-4.5OD3.95H-1.1-3.7-TH1

R0611 0 5% 1/16W MF-LF 402

CPU_THERMAL_SCREW_RIGHT — 1 OMIT Z0621 STDOFF-4.5OD3.95H-1.1-3.7-TH1

R0621 0 5% 1/16W MF-LF 402

LVDS ALIASES

NO-CONNECT UNUSED LVDS INTERFACE PORTS

13C5	LVDS_B_CLK_N	LVDS_B_CLK_N_SPN	5A7
13C5	LVDS_B_CLK_P	LVDS_B_CLK_P_SPN	MAKE_BASE=TRUE 5A7
13C5	LVDS_B_DATA_N<0>	LVDS_B_DATA_N0_SPN	MAKE_BASE=TRUE 5A7
13C5	LVDS_B_DATA_N<1>	LVDS_B_DATA_N1_SPN	MAKE_BASE=TRUE 5A7
13C5	LVDS_B_DATA_N<2>	LVDS_B_DATA_N2_SPN	MAKE_BASE=TRUE 5A7
13C5	LVDS_B_DATA_P<0>	LVDS_B_DATA_P0_SPN	MAKE_BASE=TRUE 5A7
13C5	LVDS_B_DATA_P<1>	LVDS_B_DATA_P1_SPN	MAKE_BASE=TRUE 5A7
13C5	LVDS_B_DATA_P<2>	LVDS_B_DATA_P2_SPN	MAKE_BASE=TRUE 5A7 MAKE_BASE=TRUE

PCI_EXPRESS GRAPHICS ALIASES

NO-CONNECT UNUSED SDVO INTERFACE PORTS

13D3	PEG_D2R_N<0>	PEG_D2R_N0_SPN	MAKE_BASE=TRUE
13D3	PEG_D2R_N<2>	PEG_D2R_N2_SPN	MAKE_BASE=TRUE
13D3	PEG_D2R_N<3>	PEG_D2R_N3_SPN	MAKE_BASE=TRUE
13D3	PEG_D2R_N<4>	PEG_D2R_N4_SPN	MAKE_BASE=TRUE
13D3	PEG_D2R_N<5>	PEG_D2R_N5_SPN	MAKE_BASE=TRUE
13D3	PEG_D2R_N<6>	PEG_D2R_N6_SPN	MAKE_BASE=TRUE
13D3	PEG_D2R_N<7>	PEG_D2R_N7_SPN	MAKE_BASE=TRUE
13D3	PEG_D2R_N<8>	PEG_D2R_N8_SPN	MAKE_BASE=TRUE
13D3	PEG_D2R_N<9>	PEG_D2R_N9_SPN	MAKE_BASE=TRUE
13C3	PEG_D2R_N<10>	PEG_D2R_N10_SPN	MAKE_BASE=TRUE
13C3	PEG_D2R_N<11>	PEG_D2R_N11_SPN	MAKE_BASE=TRUE
13C3	PEG_D2R_N<12>	PEG_D2R_N12_SPN	MAKE_BASE=TRUE
13C3	PEG_D2R_N<13>	PEG_D2R_N13_SPN	MAKE_BASE=TRUE
13C3	PEG_D2R_N<14>	PEG_D2R_N14_SPN	MAKE_BASE=TRUE
13C3	PEG_D2R_N<15>	PEG_D2R_N15_SPN	MAKE_BASE=TRUE
13C3	PEG_D2R_P<0>	PEG_D2R_P0_SPN	MAKE_BASE=TRUE
13C3	PEG_D2R_P<2>	PEG_D2R_P2_SPN	MAKE_BASE=TRUE
13C3	PEG_D2R_P<3>	PEG_D2R_P3_SPN	MAKE_BASE=TRUE
13C3	PEG_D2R_P<4>	PEG_D2R_P4_SPN	MAKE_BASE=TRUE
13C3	PEG_D2R_P<5>	PEG_D2R_P5_SPN	MAKE_BASE=TRUE
13C3	PEG_D2R_P<6>	PEG_D2R_P6_SPN	MAKE_BASE=TRUE
13C3	PEG_D2R_P<7>	PEG_D2R_P7_SPN	MAKE_BASE=TRUE
13C3	PEG_D2R_P<8>	PEG_D2R_P8_SPN	MAKE_BASE=TRUE
13C3	PEG_D2R_P<9>	PEG_D2R_P9_SPN	MAKE_BASE=TRUE
13C3	PEG_D2R_P<10>	PEG_D2R_P10_SPN	MAKE_BASE=TRUE
13C3	PEG_D2R_P<11>	PEG_D2R_P11_SPN	MAKE_BASE=TRUE
13C3	PEG_D2R_P<12>	PEG_D2R_P12_SPN	MAKE_BASE=TRUE
13C3	PEG_D2R_P<13>	PEG_D2R_P13_SPN	MAKE_BASE=TRUE
13C3	PEG_D2R_P<14>	PEG_D2R_P14_SPN	MAKE_BASE=TRUE
13C3	PEG_D2R_P<15>	PEG_D2R_P15_SPN	MAKE_BASE=TRUE
13B3	PEG_R2D_C_N<4>	PEG_R2D_C_N4_SPN	MAKE_BASE=TRUE
13B3	PEG_R2D_C_N<5>	PEG_R2D_C_N5_SPN	MAKE_BASE=TRUE
13B3	PEG_R2D_C_N<6>	PEG_R2D_C_N6_SPN	MAKE_BASE=TRUE
13B3	PEG_R2D_C_N<7>	PEG_R2D_C_N7_SPN	MAKE_BASE=TRUE
13B3	PEG_R2D_C_N<8>	PEG_R2D_C_N8_SPN	MAKE_BASE=TRUE
13B3	PEG_R2D_C_N<9>	PEG_R2D_C_N9_SPN	MAKE_BASE=TRUE
13B3	PEG_R2D_C_N<10>	PEG_R2D_C_N10_SPN	MAKE_BASE=TRUE
13B3	PEG_R2D_C_N<11>	PEG_R2D_C_N11_SPN	MAKE_BASE=TRUE
13B3	PEG_R2D_C_N<12>	PEG_R2D_C_N12_SPN	MAKE_BASE=TRUE
13B3	PEG_R2D_C_N<13>	PEG_R2D_C_N13_SPN	MAKE_BASE=TRUE
13B3	PEG_R2D_C_N<14>	PEG_R2D_C_N14_SPN	MAKE_BASE=TRUE
13B3	PEG_R2D_C_N<15>	PEG_R2D_C_N15_SPN	MAKE_BASE=TRUE
13B3	PEG_R2D_C_P<4>	PEG_R2D_C_P4_SPN	MAKE_BASE=TRUE
13B3	PEG_R2D_C_P<5>	PEG_R2D_C_P5_SPN	MAKE_BASE=TRUE
13B3	PEG_R2D_C_P<6>	PEG_R2D_C_P6_SPN	MAKE_BASE=TRUE
13B3	PEG_R2D_C_P<7>	PEG_R2D_C_P7_SPN	MAKE_BASE=TRUE
13B3	PEG_R2D_C_P<8>	PEG_R2D_C_P8_SPN	MAKE_BASE=TRUE
13B3	PEG_R2D_C_P<9>	PEG_R2D_C_P9_SPN	MAKE_BASE=TRUE
13B3	PEG_R2D_C_P<10>	PEG_R2D_C_P10_SPN	MAKE_BASE=TRUE
13B3	PEG_R2D_C_P<11>	PEG_R2D_C_P11_SPN	MAKE_BASE=TRUE
13A3	PEG_R2D_C_P<12>	PEG_R2D_C_P12_SPN	MAKE_BASE=TRUE
13A3	PEG_R2D_C_P<13>	PEG_R2D_C_P13_SPN	MAKE_BASE=TRUE
13A3	PEG_R2D_C_P<14>	PEG_R2D_C_P14_SPN	MAKE_BASE=TRUE
13A3	PEG_R2D_C_P<15>	PEG_R2D_C_P15_SPN	MAKE_BASE=TRUE

69A3 =GND_CHASSIS_TMDS_DOWN
39A1 =GND_CHASSIS_FW_UPPER
I393
GND_CHASSIS_IO1 — VOLTAGE=0V MAKE_BASE=TRUE

OMIT Z0612 STDOFF-4.2OD2.15H-1.2-TH — NC 1

OMIT Z0613 STDOFF-4.2OD2.15H-1.2-TH — NC 1

NB CFG ALIASES

NO-CONNECT UNUSED CFG INTERFACE PORTS

14C6	NB_CFG<3>	TP_NB_CFG3	
14C6	NB_CFG<4>	TP_NB_CFG4	MAKE_BASE=TRUE
14C6	NB_CFG<6>	TP_NB_CFG6	MAKE_BASE=TRUE
14C6	NB_CFG<8>	TP_NB_CFG8	MAKE_BASE=TRUE
14C6	NB_CFG<10>	TP_NB_CFG10	MAKE_BASE=TRUE
14C6	NB_CFG<11>	TP_NB_CFG11	MAKE_BASE=TRUE
14C6	NB_CFG<12>	TP_NB_CFG12	MAKE_BASE=TRUE
14C6	NB_CFG<13>	TP_NB_CFG13	MAKE_BASE=TRUE
14C6	NB_CFG<14>	TP_NB_CFG14	MAKE_BASE=TRUE
14C6	NB_CFG<15>	TP_NB_CFG15	MAKE_BASE=TRUE
14C6	NB_CFG<17>	TP_NB_CFG17	MAKE_BASE=TRUE MAKE_BASE=TRUE

SATA ALIASES

NO-CONNECT UNUSED SATA INTERFACE PORTS

21B6	SATA_A_D2R_N	SATA_A_D2R_N_SPN	
21B6	SATA_A_D2R_P	SATA_A_D2R_P_SPN	MAKE_BASE=TRUE
21B6	SATA_A_R2D_C_N	SATA_A_R2D_C_N_SPN	MAKE_BASE=TRUE
21B6	SATA_A_R2D_C_P	SATA_A_R2D_C_P_SPN	MAKE_BASE=TRUE MAKE_BASE=TRUE

PCI_EXP ALIASES

NO-CONNECT UNUSED PCI_EXP INTERFACE PORTS

22D4	PCIE_C_D2R_N	PCIE_C_D2R_N_SPN	
22D4	PCIE_C_D2R_P	PCIE_C_D2R_P_SPN	MAKE_BASE=TRUE
22D4	PCIE_C_R2D_C_N	PCIE_C_R2D_C_N_SPN	MAKE_BASE=TRUE
22D4	PCIE_C_R2D_C_P	PCIE_C_R2D_C_P_SPN	MAKE_BASE=TRUE
22D4	PCIE_D_D2R_N	PCIE_D_D2R_N_SPN	MAKE_BASE=TRUE
22D4	PCIE_D_D2R_P	PCIE_D_D2R_P_SPN	MAKE_BASE=TRUE
22D4	PCIE_D_R2D_C_N	PCIE_D_R2D_C_N_SPN	MAKE_BASE=TRUE
22D4	PCIE_D_R2D_C_P	PCIE_D_R2D_C_P_SPN	MAKE_BASE=TRUE
22C4	PCIE_E_D2R_N	PCIE_E_D2R_N_SPN	MAKE_BASE=TRUE
22C4	PCIE_E_D2R_P	PCIE_E_D2R_P_SPN	MAKE_BASE=TRUE
22C4	PCIE_E_R2D_C_N	PCIE_E_R2D_C_N_SPN	MAKE_BASE=TRUE
22C4	PCIE_E_R2D_C_P	PCIE_E_R2D_C_P_SPN	MAKE_BASE=TRUE
22C4	PCIE_F_D2R_N	PCIE_F_D2R_N_SPN	MAKE_BASE=TRUE
22C4	PCIE_F_D2R_P	PCIE_F_D2R_P_SPN	MAKE_BASE=TRUE
22C4	PCIE_F_R2D_C_N	PCIE_F_R2D_C_N_SPN	MAKE_BASE=TRUE
22C4	PCIE_F_R2D_C_P	PCIE_F_R2D_C_P_SPN	MAKE_BASE=TRUE MAKE_BASE=TRUE

CLOCK ALIASES

NO-CONNECT UNUSED CLOCK INTERFACE PORTS

32B4	CK410_SRC1_N	CK410_SRC1_N_SPN	5C7
32B4	CK410_SRC1_P	CK410_SRC1_P_SPN	MAKE_BASE=TRUE 5C7
32B4	CK410_SRC3_N	CK410_SRC3_N_SPN	MAKE_BASE=TRUE 5C7
32B4	CK410_SRC3_P	CK410_SRC3_P_SPN	MAKE_BASE=TRUE 5C7
32B4	CK410_SRC7_N	CK410_SRC7_N_SPN	MAKE_BASE=TRUE 5C7
32B4	CK410_SRC7_P	CK410_SRC7_P_SPN	MAKE_BASE=TRUE 5C7
32B4	CK410_SRC_CLKREQ1_L	CK410_SRC_CLKREQ1_L_SPN	MAKE_BASE=TRUE 5B7
32B4	CK410_SRC_CLKREQ3_L	CK410_SRC_CLKREQ3_L_SPN	MAKE_BASE=TRUE 5B7 MAKE_BASE=TRUE

SB ALIASES

NO-CONNECT UNUSED CLOCK INTERFACE PORTS

23C3	SUS_CLK_SB	SUS_CLK_SB_SPN	MAKE_BASE=TRUE

SO-DIMM ALIASES

NO-CONNECT UNUSED ADDRESS INTERFACE PORTS

28C4	MEM_A_A<15>	MEM_A_A15_SPN	
28C4	MEM_A_A<14>	MEM_A_A14_SPN	MAKE_BASE=TRUE
29C4	MEM_B_A<15>	MEM_B_A15_SPN	MAKE_BASE=TRUE
29C4	MEM_B_A<14>	MEM_B_A14_SPN	MAKE_BASE=TRUE MAKE_BASE=TRUE

Ethernet ALIASES

36C8	ENET_CTRL12	ENET_CTRL12_SPN	
36C8	ENET_CTRL25	ENET_CTRL25_SPN	MAKE_BASE=TRUE MAKE_BASE=TRUE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
860-0722	4	THERMAL STANDOFF	Z0603,Z0604,Z0605,Z0621	STANDOFF
860-0723	1	STANDOFF WIRELESS	Z0612	STANDOFF
860-0749	1	STANDOFF W/THRU HOLES,WIRELESS	Z0613	STANDOFF

FIREWIRE ALIASES

NO-CONNECT UNUSED FIREWIRE INTERFACE PORTS

38B3	FW_B_TPBIAS	FW_B_TPBIAS_SPN	5B7
38B3	FW_B_TPA_P	FW_B_TPA_P_SPN	MAKE_BASE=TRUE 5B7
38B3	FW_B_TPA_N	FW_B_TPA_N_SPN	MAKE_BASE=TRUE 5B7
38B3	FW_B_TPB_P	FW_B_TPB_P_SPN	MAKE_BASE=TRUE 5B7
38B3	FW_B_TPB_N	FW_B_TPB_N_SPN	MAKE_BASE=TRUE 5B7
38B3	FW_C_TPBIAS	FW_C_TPBIAS_SPN	MAKE_BASE=TRUE 5B7
38B3	FW_C_TPA_P	FW_C_TPA_P_SPN	MAKE_BASE=TRUE 5B7
38B3	FW_C_TPA_N	FW_C_TPA_N_SPN	MAKE_BASE=TRUE 5B7
38B3	FW_C_TPB_P	FW_C_TPB_P_SPN	MAKE_BASE=TRUE 5B7
38B3	FW_C_TPB_N	FW_C_TPB_N_SPN	MAKE_BASE=TRUE 5B7 MAKE_BASE=TRUE

39C6 =FWPWR_PWRON — NC_FWPWR_PWRON
NO_TEST=TRUE MAKE_BASE=TRUE

USB PORT A = External USB2.0 Port

42C5	=USB2_EXTA_P	USB2_EXTA_P	USB_A_P	22C2
42C5	=USB2_EXTA_N	MAKE_BASE=TRUE USB2_EXTA_N	MAKE_BASE=TRUE USB_A_N	22C2
42C8	=EXTAUSB_OC_L	MAKE_BASE=TRUE EXTAUSB_OC_L	MAKE_BASE=TRUE USB_A_OC_L	22C4 22D8

USB PORT B = Trackpad(Geyser)

40C7	=USB2_GEYSER_P	USB2_GEYSER_P	USB_B_P	22C2
40C7	=USB2_GEYSER_N	MAKE_BASE=TRUE USB2_GEYSER_N	MAKE_BASE=TRUE USB_B_N	22C2

USB PORT C = External USB2.0 Port B

42B5	=USB2_EXTB_P	USB2_EXTB_P	USB_C_P	22C2
42B5	=USB2_EXTB_N	MAKE_BASE=TRUE USB2_EXTB_N	MAKE_BASE=TRUE USB_C_N	22C2
42C8	=EXTBUSB_OC_L	MAKE_BASE=TRUE EXTBUSB_OC_L	MAKE_BASE=TRUE USB_C_OC_L	22C4 22D8

USB PORT D = CAMERA

67B4	=USB2_CAMERA_P	USB2_CAMERA_P	USB_D_P	22C2
67A4	=USB2_CAMERA_N	MAKE_BASE=TRUE USB2_CAMERA_N	MAKE_BASE=TRUE USB_D_N	22C2

USB PORT "E" = Unused

5C1	TP_USBP_E		USB_E_P	22C2
5C1	TP_USBN_E	MAKE_BASE=TRUE	USB_E_N	22C2

USB PORT "F" = IR CONTROLLER

41C6	=USB2_IR_P	USB_IR_P	USB_F_P	22C2
41C6	=USB2_IR_N	USB_IR_N	MAKE_BASE=TRUE USB_F_N	22C2

MAKE_BASE=TRUE

USB PORT "G" = BLUETOOTH

44C6	=USB2_BT_P	USB_BT_P	USB_G_P	22C2
44C6	=USB2_BT_N	MAKE_BASE=TRUE USB_BT_N	MAKE_BASE=TRUE USB_G_N	22C2

MAKE_BASE=TRUE

USB PORT "H" = PCI-E Mini Card

43B4	=USB2_AIRPORT_P	USB2_AIRPORT_P	USB_H_P	22C2
43B4	=USB2_AIRPORT_N	MAKE_BASE=TRUE USB2_AIRPORT_N	MAKE_BASE=TRUE USB_H_N	22C2

MAKE_BASE=TRUE

ANALOG SWITCH GPIO

69A6 =SB_GPIO22 — SB_GPIO22 — MAKE_BASE=TRUE — TP_SB_GPIO22 22B6

45B8 14B7 PM_EXTTS_L<0> — MAKE_BASE=TRUE — DIMM_OVERTEMP_L 28C4 29C4

47C5 21C4 5C2 FWH_INIT_L — MAKE_BASE=TRUE — SMC_CPU_INIT_3_3_L 45D5

SIGNAL ALIAS /RESET

SYNC_MASTER=ENET SYNC_DATE=08/19/2005

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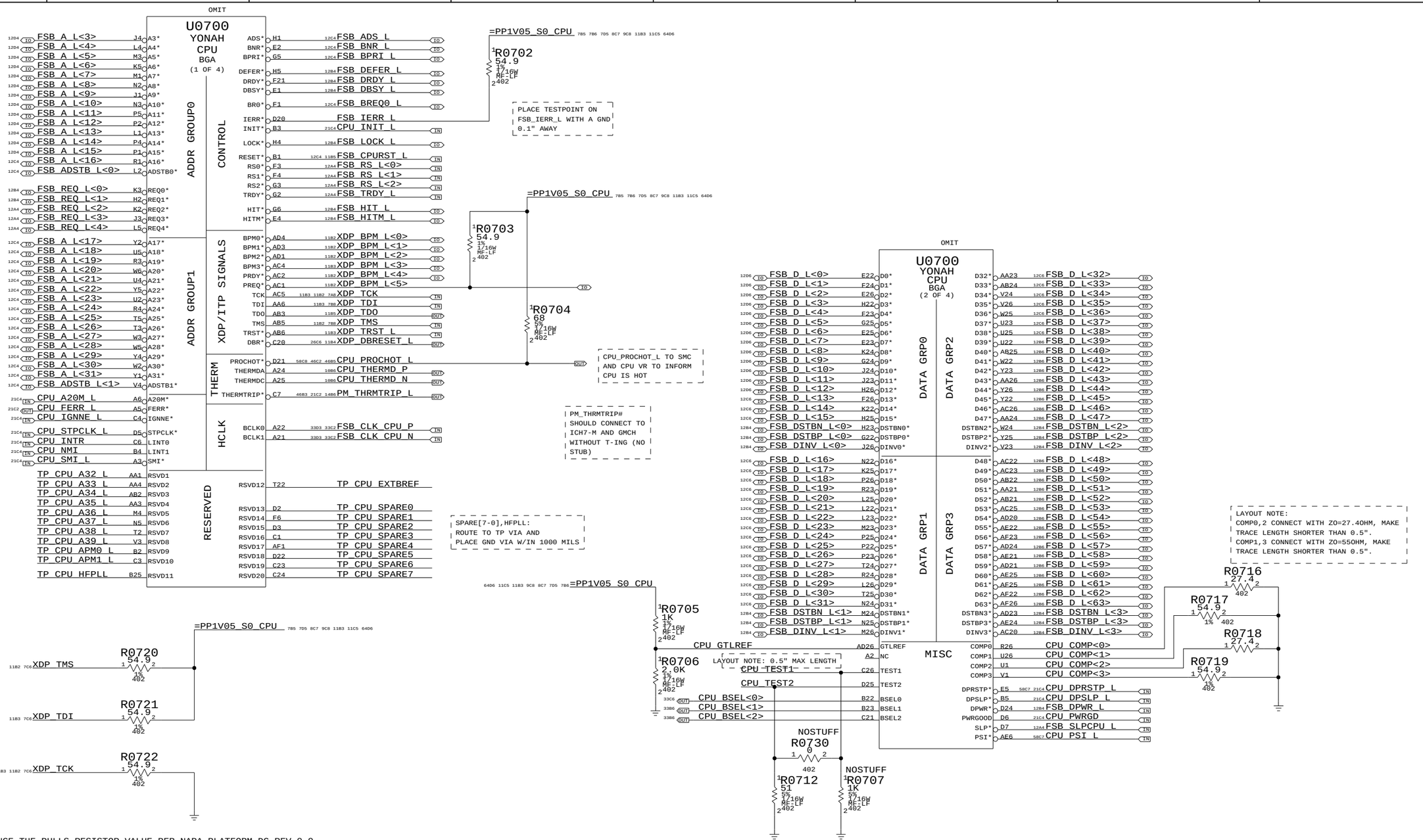
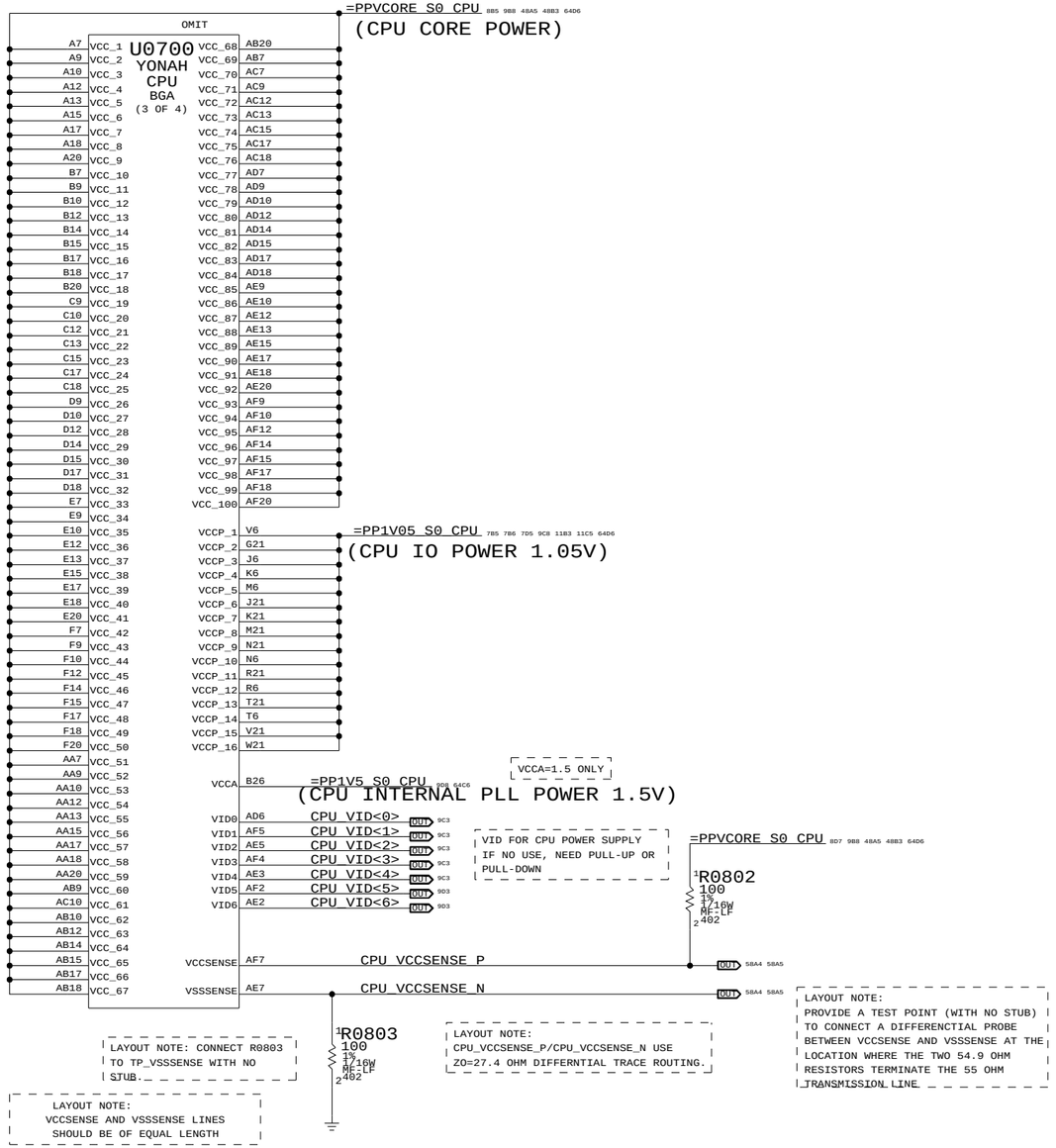
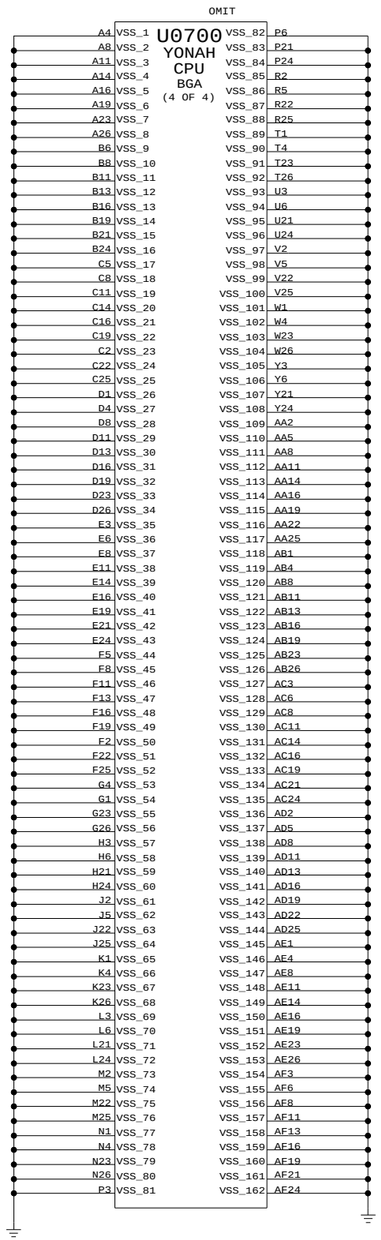
SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 6 OF 98	







CPU 2 OF 2-PWR/GND

SYNC_MASTER=MASTER SYNC_DATE=05/03/2005

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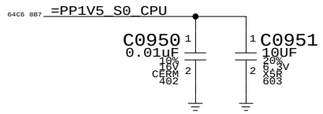
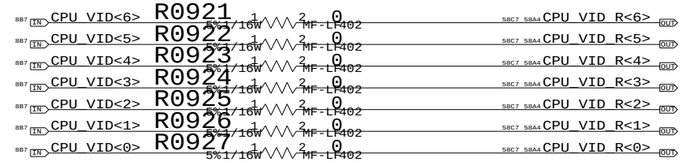
SCALE	SHT	OF
NONE	8	98

VCCA DECOUPLING
(CPU INTERNAL PLL POWER 1.5V)



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0603	138S0602	?	ALL	USE SAMSUNG AND MURATA ONLY
138S0606	138S0602	?	ALL	USE TAIYO

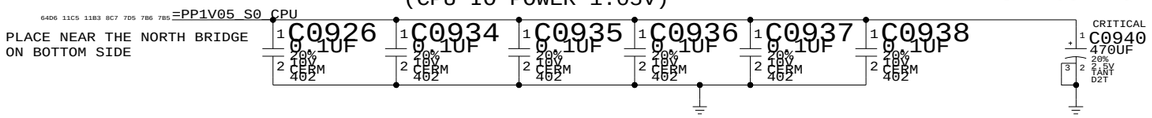
CPU CORE VID<> SETTINGS



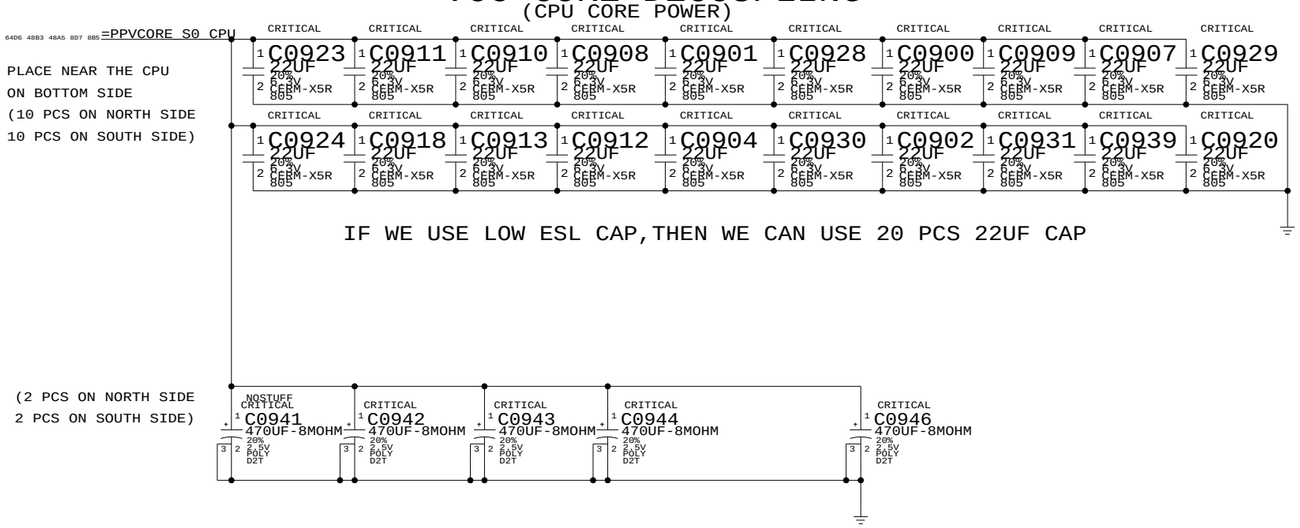
R0921~R0927 FOR CPU VOLTAGE MANUAL SETTING

VCCP CORE DECOUPLING
(CPU IO POWER 1.05V)

THIS 470UF FOR CPU,GMCH FSB BUS 1.05V



VCC CORE DECOUPLING
(CPU CORE POWER)



		MIN	TYP	MAX
DUAL CORE SV CPU	VCCHFM	1.1625		1.30
	VCCLFM	TBD		TBD
SINGLE CORE SV CPU	VCCHFM	1.1625		1.30
	VCCLFM		TBD	
DUAL CORE LV CPU	VCCHFM	1.0		1.1625
	VCCLFM		TBD	
ULV CPU	VCCHFM	TBD		TBD
	VCCLFM		TBD	

UNIT: V

ALL PROCESSOR DEFAULT VCORE FOR INITIAL POWER UP IS 1.2V
TWO PROCESSORS AT THE SAME FREQUENCY MAY HAVE DIFFERENT SETTING WITH THE VID RANGE(VCORE VOLTAGE)!
REFER TO YONAH PROCESSOR EMTS REV 1.0
VCCHFM: VCORE AT HIGHEST FREQUENCY MODE
VCCLFM: VCORE AT LOWEST FREQUENCY MODE

CPU DECAPS & VID<>

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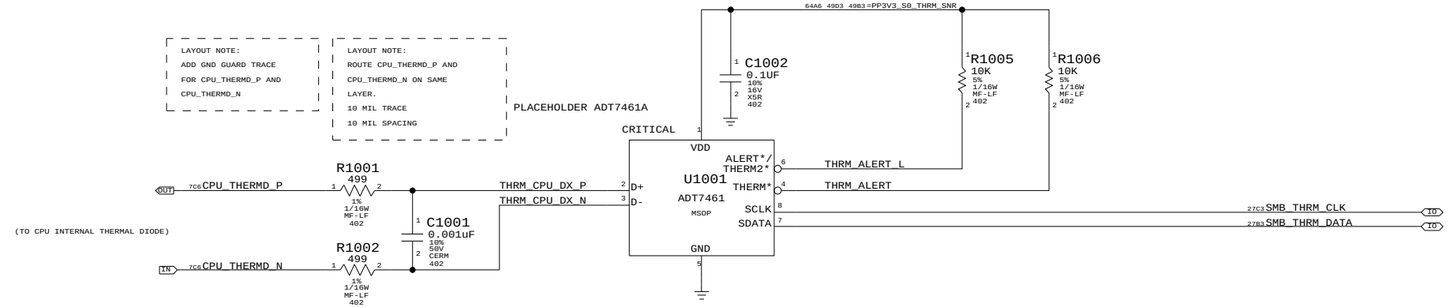
SCALE: NONE	SHT 9 OF 98	

CPU ZONE THERMAL SENSOR



PLACE U1001 NEAR THE U1200

CPU MISC1-TEMP SENSOR

SYNC_MASTER=ENET SYNC_DATE=08/19/2005

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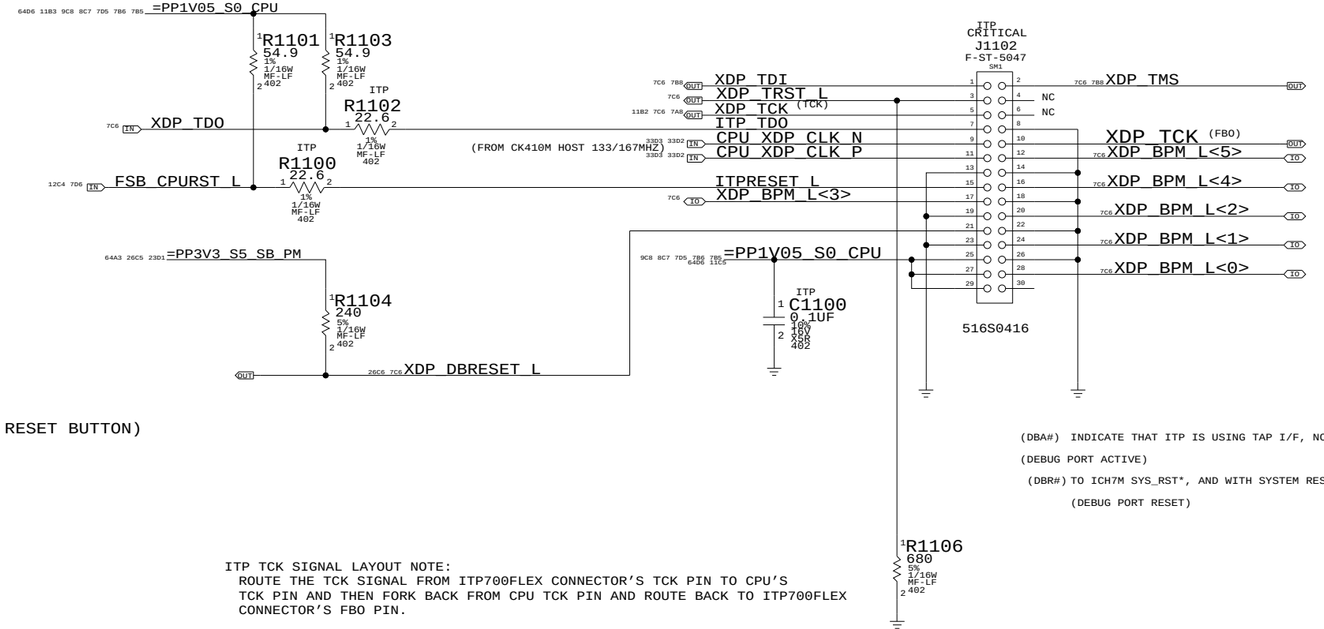
SCALE: NONE	SHT 10 OF 98	

CPU ITP700FLEX DEBUG SUPPORT



(DBA#) INDICATE THAT ITP IS USING TAP I/F, NC IN 945GM CHIPSET SYSTEM.

(DEBUG PORT ACTIVE)

(DBR#) TO ICH7M SYS_RST*, AND WITH SYSTEM RESET LOGIC

(DEBUG PORT RESET)

ITP TCK SIGNAL LAYOUT NOTE:
ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX CONNECTOR'S FBO PIN.

CPU ITP700FLEX DEBUG

SYNC_MASTER=MASTER SYNC_DATE=5/23/05

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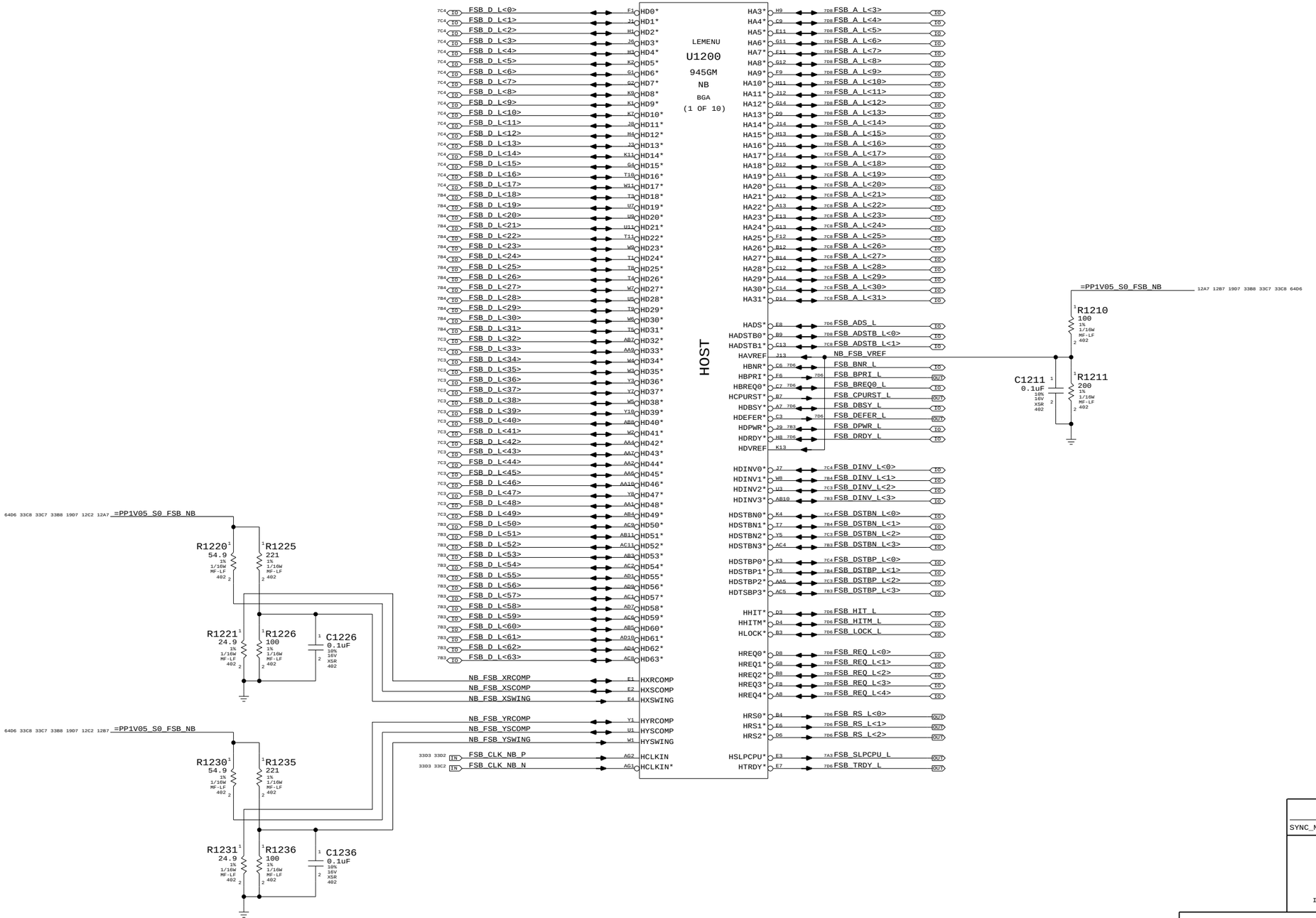

NB CPU Interface

SYNC_MASTER=NB SYNC_DATE=07/25/2005

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SCALE: NONE	SHT 12 OF 98	

LVDS Disable

Can leave all signals NC if LVDS is not implemented
Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
VCCD_LVDS must remain powered with proper decoupling.
Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

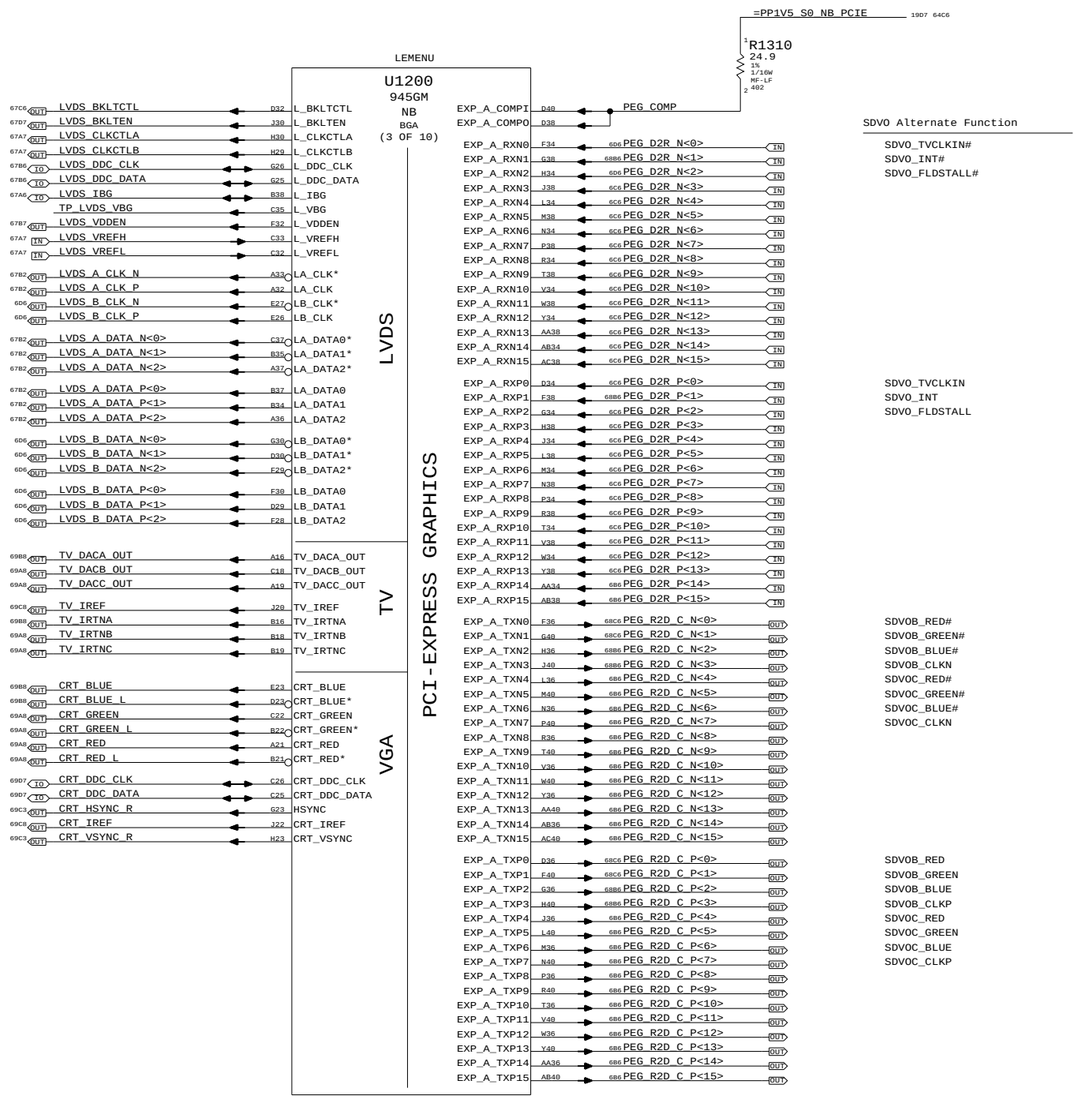
Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable

Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail.
Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and
VCCA_TVBG to 1.5V power rail. Tie VSSA_TVBG to GND.

CRT Disable

Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie
HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core
rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.



NB PEG / Video Interfaces

SYNC_MASTER=NB SYNC_DATE=07/25/2005

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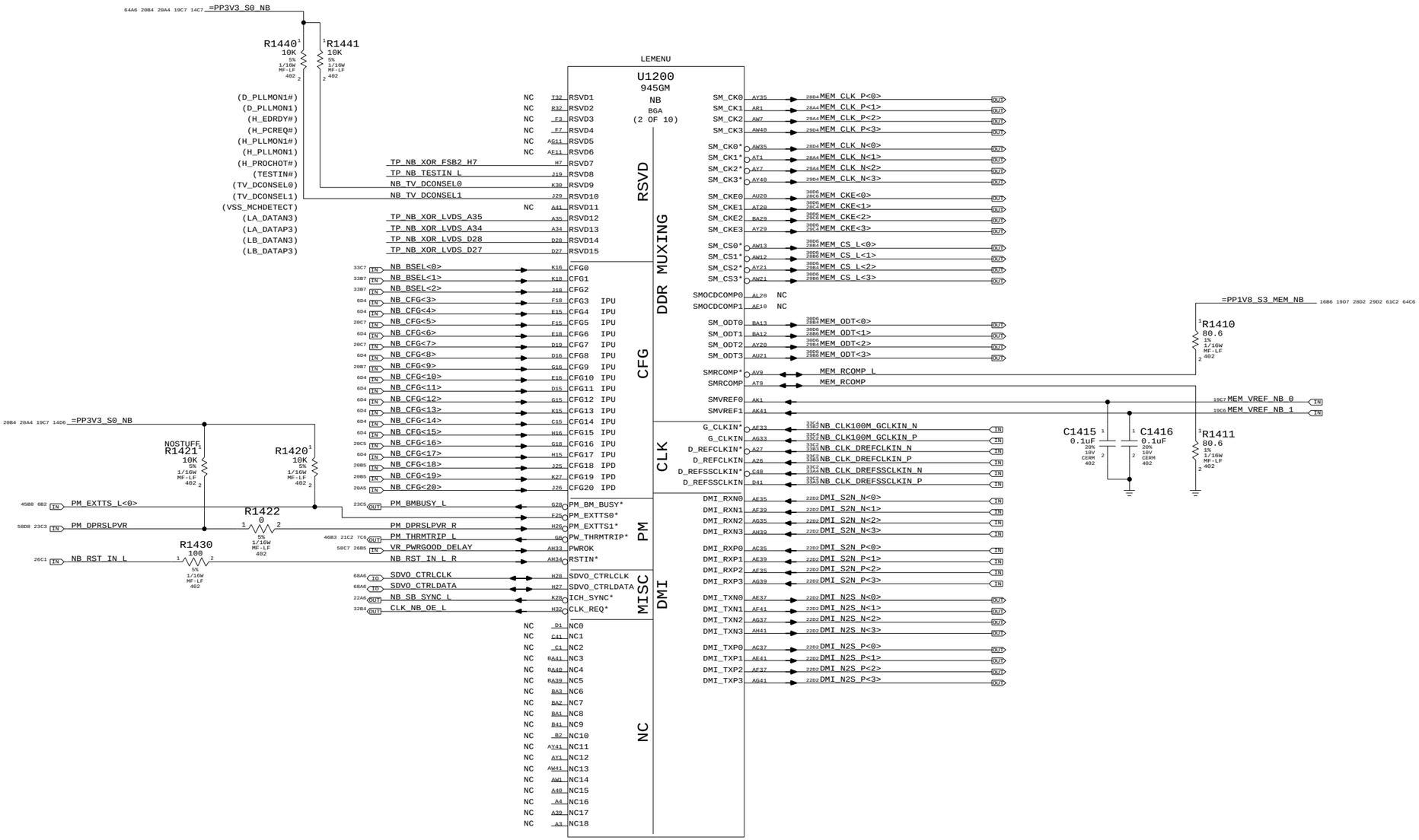

NB Misc Interfaces

SYNC_MASTER=NB SYNC_DATE=08/15/2005

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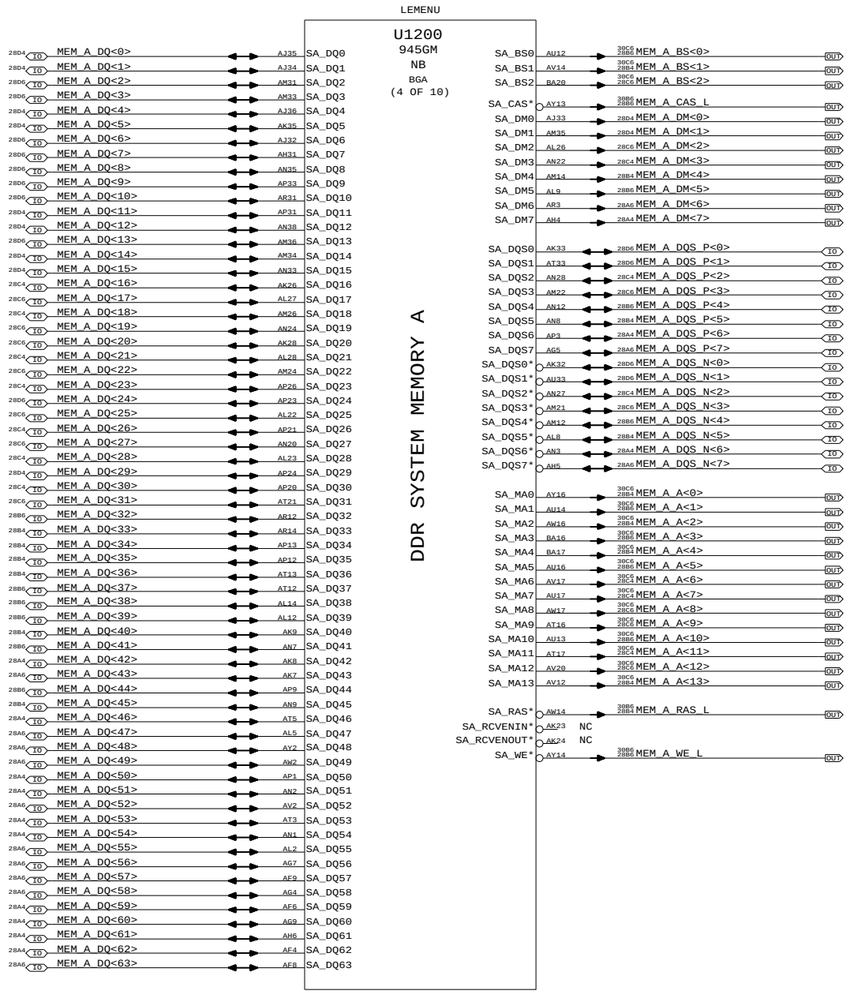
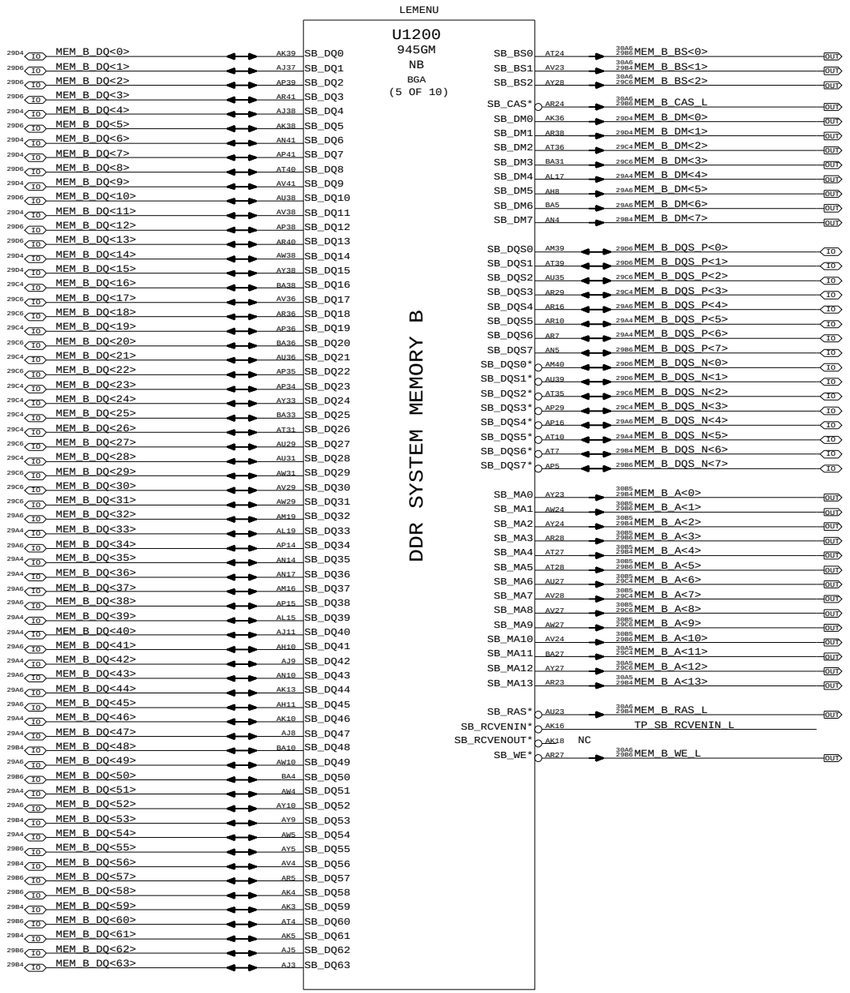
D	051-7370	C
SCALE: NONE	SHT 14 OF 98	





NB DDR2 Interfaces

SYNC_MASTER=NB SYNC_DATE=07/25/2005

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SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 15 OF 98	

NCTF balls are Not Critical To Function

These connections can break without impacting part performance.

=PPVCORE_S0_NB 64D6 19D7 19C8 16C8

LEMENU

U1200 945GM NB BGA (7 OF 10) NCTF

VCC_NCTF0	AD27	VSS_NCTF0	AE27
VCC_NCTF1	AC27	VSS_NCTF1	AE26
VCC_NCTF2	AB27	VSS_NCTF2	AE25
VCC_NCTF3	AA27	VSS_NCTF3	AE24
VCC_NCTF4	Y27	VSS_NCTF4	AE23
VCC_NCTF5	W27	VSS_NCTF5	AE22
VCC_NCTF6	V27	VSS_NCTF6	AE21
VCC_NCTF7	U27	VSS_NCTF7	AE20
VCC_NCTF8	T27	VSS_NCTF8	AE19
VCC_NCTF9	R27	VSS_NCTF9	AE18
VCC_NCTF10	AD26	VSS_NCTF10	AC17
VCC_NCTF11	AC26	VSS_NCTF11	Y17
VCC_NCTF12	AB26	VSS_NCTF12	U17
VCC_NCTF13	AA26		
VCC_NCTF14	Y26		
VCC_NCTF15	W26		
VCC_NCTF16	V26		
VCC_NCTF17	U26		
VCC_NCTF18	T26		
VCC_NCTF19	R26		
VCC_NCTF20	AD25		
VCC_NCTF21	AC25		
VCC_NCTF22	AB25		
VCC_NCTF23	AA25		
VCC_NCTF24	Y25		
VCC_NCTF25	W25		
VCC_NCTF26	V25		
VCC_NCTF27	U25		
VCC_NCTF28	T25		
VCC_NCTF29	R25		
VCC_NCTF30	AD24		
VCC_NCTF31	AC24		
VCC_NCTF32	AB24		
VCC_NCTF33	AA24		
VCC_NCTF34	Y24		
VCC_NCTF35	W24		
VCC_NCTF36	V24		
VCC_NCTF37	U24		
VCC_NCTF38	T24		
VCC_NCTF39	R24		
VCC_NCTF40	AD23		
VCC_NCTF41	U23		
VCC_NCTF42	T23		
VCC_NCTF43	R23		
VCC_NCTF44	AD22		
VCC_NCTF45	V22		
VCC_NCTF46	U22		
VCC_NCTF47	T22		
VCC_NCTF48	R22		
VCC_NCTF49	AD21		
VCC_NCTF50	V21		
VCC_NCTF51	U21		
VCC_NCTF52	T21		
VCC_NCTF53	R21		
VCC_NCTF54	AD20		
VCC_NCTF55	V20		
VCC_NCTF56	U20		
VCC_NCTF57	T20		
VCC_NCTF58	R20		
VCC_NCTF59	AD19		
VCC_NCTF60	V19		
VCC_NCTF61	U19		
VCC_NCTF62	T19		
VCC_NCTF63	AD18		
VCC_NCTF64	AC18		
VCC_NCTF65	AB18		
VCC_NCTF66	AA18		
VCC_NCTF67	Y18		
VCC_NCTF68	W18		
VCC_NCTF69	V18		
VCC_NCTF70	U18		
VCC_NCTF71	T18		
VCC_NCTF72			

=PP1V5_S0_NB_VCCAUX 17B5 19B6 19D7 64C6

VCCAUX_NCTF0	AG27	VCCAUX_NCTF25	AD17
VCCAUX_NCTF1	AF27	VCCAUX_NCTF26	AB17
VCCAUX_NCTF2	AG26	VCCAUX_NCTF27	AA17
VCCAUX_NCTF3	AF26	VCCAUX_NCTF28	W17
VCCAUX_NCTF4	AG25	VCCAUX_NCTF29	V17
VCCAUX_NCTF5	AF25	VCCAUX_NCTF30	T17
VCCAUX_NCTF6	AG24	VCCAUX_NCTF31	R17
VCCAUX_NCTF7	AF24	VCCAUX_NCTF32	AG16
VCCAUX_NCTF8	AG23	VCCAUX_NCTF33	AF16
VCCAUX_NCTF9	AF23	VCCAUX_NCTF34	AE16
VCCAUX_NCTF10	AG22	VCCAUX_NCTF35	AD16
VCCAUX_NCTF11	AF22	VCCAUX_NCTF36	AC16
VCCAUX_NCTF12	AG21	VCCAUX_NCTF37	AB16
VCCAUX_NCTF13	AF21	VCCAUX_NCTF38	AA16
VCCAUX_NCTF14	AG20	VCCAUX_NCTF39	Y16
VCCAUX_NCTF15	AF20	VCCAUX_NCTF40	W16
VCCAUX_NCTF16	AG19	VCCAUX_NCTF41	V16
VCCAUX_NCTF17	AF19	VCCAUX_NCTF42	U16
VCCAUX_NCTF18	R19	VCCAUX_NCTF43	T16
VCCAUX_NCTF19	AG18	VCCAUX_NCTF44	R16
VCCAUX_NCTF20	AF18	VCCAUX_NCTF45	AG15
VCCAUX_NCTF21	R18	VCCAUX_NCTF46	AF15
VCCAUX_NCTF22	AG17	VCCAUX_NCTF47	AE15
VCCAUX_NCTF23	AF17	VCCAUX_NCTF48	AD15
VCCAUX_NCTF24	AE17	VCCAUX_NCTF49	AC15
VCCAUX_NCTF25	AD17	VCCAUX_NCTF50	AB15
VCCAUX_NCTF26	AB17	VCCAUX_NCTF51	AA15
VCCAUX_NCTF27	AA17	VCCAUX_NCTF52	Y15
VCCAUX_NCTF28	W17	VCCAUX_NCTF53	W15
VCCAUX_NCTF29	V17	VCCAUX_NCTF54	V15
VCCAUX_NCTF30	T17	VCCAUX_NCTF55	U15
VCCAUX_NCTF31	R17	VCCAUX_NCTF56	T15
VCCAUX_NCTF32	AG16	VCCAUX_NCTF57	R15
VCCAUX_NCTF33	AF16		
VCCAUX_NCTF34	AE16		
VCCAUX_NCTF35	AD16		
VCCAUX_NCTF36	AC16		
VCCAUX_NCTF37	AB16		
VCCAUX_NCTF38	AA16		
VCCAUX_NCTF39	Y16		
VCCAUX_NCTF40	W16		
VCCAUX_NCTF41	V16		
VCCAUX_NCTF42	U16		
VCCAUX_NCTF43	T16		
VCCAUX_NCTF44	R16		
VCCAUX_NCTF45	AG15		
VCCAUX_NCTF46	AF15		
VCCAUX_NCTF47	AE15		
VCCAUX_NCTF48	AD15		
VCCAUX_NCTF49	AC15		
VCCAUX_NCTF50	AB15		
VCCAUX_NCTF51	AA15		
VCCAUX_NCTF52	Y15		
VCCAUX_NCTF53	W15		
VCCAUX_NCTF54	V15		
VCCAUX_NCTF55	U15		
VCCAUX_NCTF56	T15		
VCCAUX_NCTF57	R15		

=PPVCORE_S0_NB 16D3 19C8 19D7 64D6

1.05V or 1.5V

U1200 945GM NB BGA (6 OF 10) VCC

LEMENU

VCC_0	AA33	VCC_55	P27
VCC_1	AA3	VCC_56	N27
VCC_2	P33	VCC_57	L27
VCC_3	N33	VCC_58	P26
VCC_4	L33	VCC_59	N26
VCC_5	J33	VCC_60	L26
VCC_6	AA32	VCC_61	N25
VCC_7	Y32	VCC_62	L25
VCC_8	W32	VCC_63	P24
VCC_9	V32	VCC_64	N24
VCC_10	P32	VCC_65	M24
VCC_11	N32	VCC_66	L24
VCC_12	M32	VCC_67	AB23
VCC_13	L32	VCC_68	AA23
VCC_14	J32	VCC_69	Y23
VCC_15	AA31	VCC_70	P23
VCC_16	W31	VCC_71	N23
VCC_17	V31	VCC_72	M23
VCC_18	T31	VCC_73	L23
VCC_19	R31	VCC_74	AC22
VCC_20	P31	VCC_75	AB22
VCC_21	N31	VCC_76	Y22
VCC_22	M31	VCC_77	W22
VCC_23	AA30	VCC_78	P22
VCC_24	W30	VCC_79	N22
VCC_25	V30	VCC_80	M22
VCC_26	U30	VCC_81	L22
VCC_27	T30	VCC_82	AC21
VCC_28	R30	VCC_83	AA21
VCC_29	P30	VCC_84	W21
VCC_30	N30	VCC_85	V21
VCC_31	M30	VCC_86	N21
VCC_32	L30	VCC_87	L21
VCC_33	AA29	VCC_88	AC20
VCC_34	W29	VCC_89	AB20
VCC_35	V29	VCC_90	W20
VCC_36	P29	VCC_91	P20
VCC_37	U29	VCC_92	M20
VCC_38	T29	VCC_93	K20
VCC_39	R29	VCC_94	J20
VCC_40	P29	VCC_95	L20
VCC_41	M29	VCC_96	AB19
VCC_42	L29	VCC_97	Y19
VCC_43	AB28	VCC_98	T19
VCC_44	AA28	VCC_99	R19
VCC_45	Y28	VCC_100	M19
VCC_46	V28	VCC_101	L19
VCC_47	U28	VCC_102	N18
VCC_48	T28	VCC_103	L18
VCC_49	R28	VCC_104	P17
VCC_50	P28	VCC_105	N17
VCC_51	N28	VCC_106	M17
VCC_52	M28	VCC_107	N16
VCC_53	L28	VCC_108	M16
VCC_54	P27	VCC_109	L16
		VCC_110	

VCC_SM0	AU41	VCC_SM55	AK20
VCC_SM1	AT41	VCC_SM56	AJ20
VCC_SM2	AM41	VCC_SM57	AH20
VCC_SM3	AU40	VCC_SM58	AT19
VCC_SM4	BA34	VCC_SM59	AR19
VCC_SM5	AT34	VCC_SM60	AP19
VCC_SM6	AM34	VCC_SM61	AN19
VCC_SM7	AV34	VCC_SM62	AM19
VCC_SM8	AU34	VCC_SM63	AU19
VCC_SM9	AT34	VCC_SM64	AR18
VCC_SM10	AR34	VCC_SM65	AP18
VCC_SM11	BA30	VCC_SM66	AJ18
VCC_SM12	AY30	VCC_SM67	AH18
VCC_SM13	AW30	VCC_SM68	AJ17
VCC_SM14	AV30	VCC_SM69	AH17
VCC_SM15	AU30	VCC_SM70	AJ16
VCC_SM16	AT30	VCC_SM71	AH16
VCC_SM17	AR30	VCC_SM72	BA15
VCC_SM18	AP30	VCC_SM73	AY15
VCC_SM19	AN30	VCC_SM74	AW15
VCC_SM20	AM30	VCC_SM75	AV15
VCC_SM21	AM29	VCC_SM76	AU15
VCC_SM22	AL29	VCC_SM77	AT15
VCC_SM23	AK29	VCC_SM78	AR15
VCC_SM24	AJ29	VCC_SM79	AJ15
VCC_SM25	AH29	VCC_SM80	AJ14
VCC_SM26	AJ28	VCC_SM81	AJ13
VCC_SM27	AH28	VCC_SM82	AH13
VCC_SM28	AJ27	VCC_SM83	AK12
VCC_SM29	AH27	VCC_SM84	AJ12
VCC_SM30	BA26	VCC_SM85	AH12
VCC_SM31	AY26	VCC_SM86	AG12
VCC_SM32	AW26	VCC_SM87	AK11
VCC_SM33	AV26	VCC_SM88	BA9
VCC_SM34	AU26	VCC_SM89	AY9
VCC_SM35	AT26	VCC_SM90	AW9
VCC_SM36	AR26	VCC_SM91	AV9
VCC_SM37	AJ26	VCC_SM92	AU9
VCC_SM38	AH26	VCC_SM93	AT9
VCC_SM39	AJ25	VCC_SM94	AR9
VCC_SM40	AH25	VCC_SM95	AP9
VCC_SM41	AJ24	VCC_SM96	AN9
VCC_SM42	AH24	VCC_SM97	AM9
VCC_SM43	BA23	VCC_SM98	AV6
VCC_SM44	AJ23	VCC_SM99	AT6
VCC_SM45	BA22	VCC_SM100	AM6
VCC_SM46	AY22	VCC_SM101	AP6
VCC_SM47	AM22	VCC_SM102	AN6
VCC_SM48	AV22	VCC_SM103	AL6
VCC_SM49	AU22	VCC_SM104	AK6
VCC_SM50	AT22	VCC_SM105	AJ6
VCC_SM51	AR22	VCC_SM106	AV1
VCC_SM52	AP22	VCC_SM107	AJ1
VCC_SM53	AK22		
VCC_SM54	AJ22		

NB_VCCSM_LF4

NB_VCCSM_LF5

C1614 0.47UF 10% 6.3V CERM-X5R 402

C1613 0.47UF 10% 6.3V CERM-X5R 402

C1615 0.47UF 10% 6.3V CERM-X5R 402 — 28D2 19D7 14C2 64C6 61C2 29D2 =PP1V8_S3_MEM_NB

Layout Note:
Place near pin BA23

C1620 10uF 20% 6.3V X5R 603

C1621 10uF 20% 6.3V X5R 603

C1610 0.47UF 10% 6.3V CERM-X5R 402

Layout Note:
Place in cavity
(Need to better define cavity)

Layout Note:
Place near pin BA15

NB_VCCSM_LF2

NB_VCCSM_LF1

C1612 0.47UF 10% 6.3V CERM-X5R 402

C1611 0.47UF 10% 6.3V CERM-X5R 402

NB Power 1

SYNC_MASTER=NB SYNC_DATE=07/25/2005

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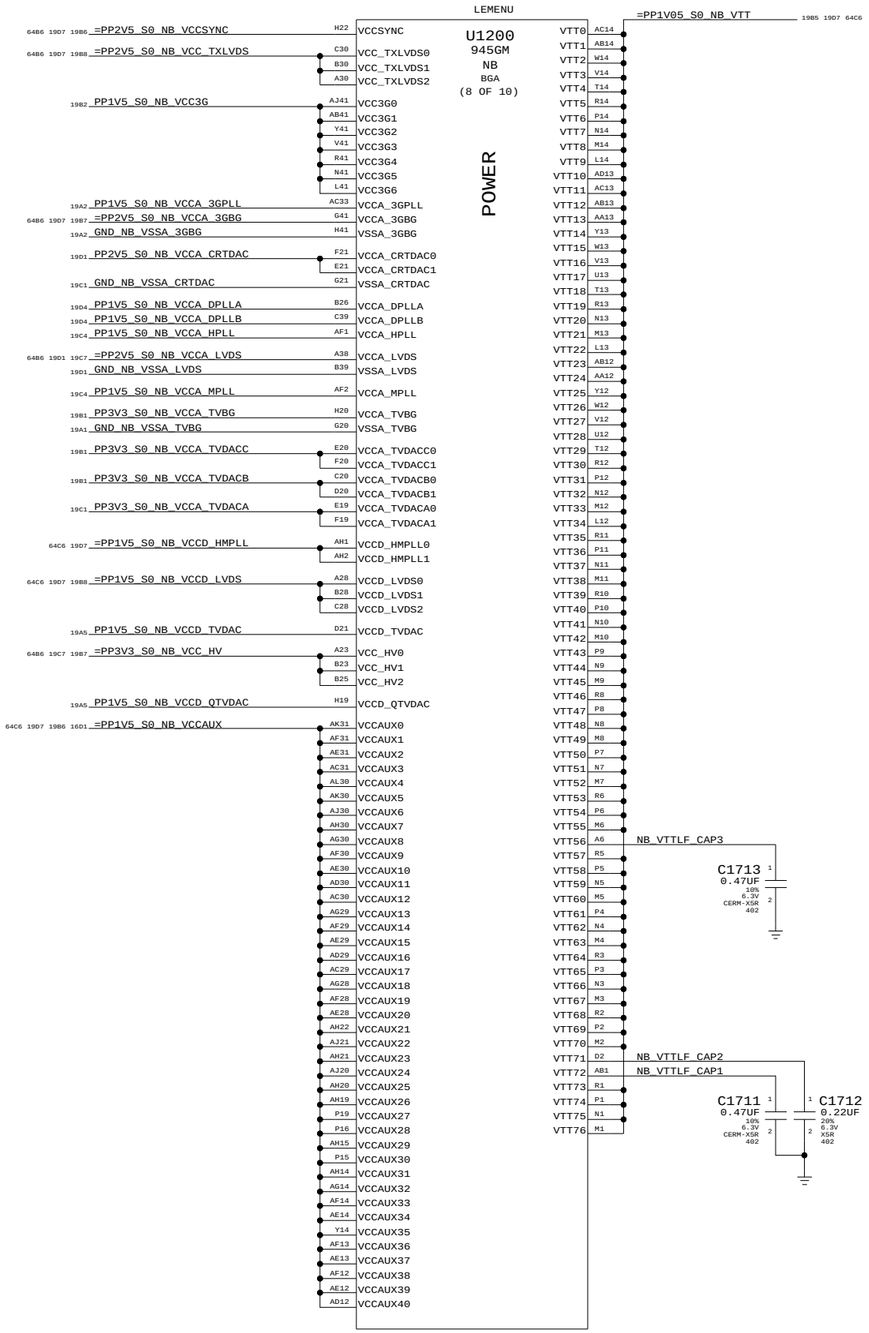
SIZE	DRAWING NUMBER	REV.
D	051-7370	C

SCALE	SHT	OF
NONE	16	98



NB Power 2

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 17 OF 98	

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U1200
945GM
NB
BGA
(9 OF 10)

VSS

AC41	VSS_0	VSS_97	AK34
AA41	VSS_1	VSS_98	AG34
W41	VSS_2	VSS_99	AF34
T41	VSS_3	VSS_100	AE34
P41	VSS_4	VSS_101	AC34
M41	VSS_5	VSS_102	C34
J41	VSS_6	VSS_103	AW33
F41	VSS_7	VSS_104	AV33
AV40	VSS_8	VSS_105	AR33
AP40	VSS_9	VSS_106	AE33
AN40	VSS_10	VSS_107	AB33
AK40	VSS_11	VSS_108	Y33
AJ40	VSS_12	VSS_109	V33
AH40	VSS_13	VSS_110	T33
AG40	VSS_14	VSS_111	R33
AF40	VSS_15	VSS_112	M33
AE40	VSS_16	VSS_113	H33
B40	VSS_17	VSS_114	G33
AY39	VSS_18	VSS_115	F33
AW39	VSS_19	VSS_116	D33
AV39	VSS_20	VSS_117	B33
AR39	VSS_21	VSS_118	AH32
AN39	VSS_22	VSS_119	AG32
AJ39	VSS_23	VSS_120	AF32
AC39	VSS_24	VSS_121	AE32
AB39	VSS_25	VSS_122	AC32
AA39	VSS_26	VSS_123	AB32
Y39	VSS_27	VSS_124	G32
W39	VSS_28	VSS_125	B32
V39	VSS_29	VSS_126	AY31
T39	VSS_30	VSS_127	AV31
R39	VSS_31	VSS_128	AN31
P39	VSS_32	VSS_129	AJ31
N39	VSS_33	VSS_130	AG31
M39	VSS_34	VSS_131	AB31
L39	VSS_35	VSS_132	Y31
J39	VSS_36	VSS_133	AB30
H39	VSS_37	VSS_134	E30
G39	VSS_38	VSS_135	AT29
F39	VSS_39	VSS_136	AN29
D39	VSS_40	VSS_137	AB29
AT38	VSS_41	VSS_138	T29
AM38	VSS_42	VSS_139	N29
AH38	VSS_43	VSS_140	K29
AG38	VSS_44	VSS_141	G29
AF38	VSS_45	VSS_142	E29
AE38	VSS_46	VSS_143	C29
C38	VSS_47	VSS_144	B29
AK37	VSS_48	VSS_145	A29
AH37	VSS_49	VSS_146	BA28
AB37	VSS_50	VSS_147	AW28
AA37	VSS_51	VSS_148	AU28
Y37	VSS_52	VSS_149	AP28
W37	VSS_53	VSS_150	AM28
V37	VSS_54	VSS_151	AD28
T37	VSS_55	VSS_152	AC28
R37	VSS_56	VSS_153	W28
P37	VSS_57	VSS_154	J28
N37	VSS_58	VSS_155	E28
M37	VSS_59	VSS_156	AP27
L37	VSS_60	VSS_157	AM27
J37	VSS_61	VSS_158	AK27
H37	VSS_62	VSS_159	J27
G37	VSS_63	VSS_160	G27
F37	VSS_64	VSS_161	F27
D37	VSS_65	VSS_162	C27
AY36	VSS_66	VSS_163	B27
AW36	VSS_67	VSS_164	AN26
AN36	VSS_68	VSS_165	M26
AH36	VSS_69	VSS_166	K26
AG36	VSS_70	VSS_167	F26
AF36	VSS_71	VSS_168	D26
AE36	VSS_72	VSS_169	AK25
AC36	VSS_73	VSS_170	P25
C36	VSS_74	VSS_171	K25
B36	VSS_75	VSS_172	H25
BA35	VSS_76	VSS_173	E25
AV35	VSS_77	VSS_174	D25
AR35	VSS_78	VSS_175	A25
AH35	VSS_79	VSS_176	BA24
AB35	VSS_80	VSS_177	AU24
AA35	VSS_81	VSS_178	AL24
Y35	VSS_82	VSS_179	AW23
W35	VSS_83		
V35	VSS_84		
T35	VSS_85		
R35	VSS_86		
P35	VSS_87		
N35	VSS_88		
M35	VSS_89		
L35	VSS_90		
J35	VSS_91		
H35	VSS_92		
G35	VSS_93		
F35	VSS_94		
D35	VSS_95		
AN34	VSS_96		

LEMENU

U1200
945GM
NB
BGA
(10 OF 10)

VSS

AT23	VSS_180	VSS_273	J11
AN23	VSS_181	VSS_274	D11
AM23	VSS_182	VSS_275	B11
AH23	VSS_183	VSS_276	AV10
AC23	VSS_184	VSS_277	AP10
W23	VSS_185	VSS_278	AL10
K23	VSS_186	VSS_279	AJ10
J23	VSS_187	VSS_280	AG10
F23	VSS_188	VSS_281	AC10
C23	VSS_189	VSS_282	W10
AA22	VSS_190	VSS_283	U10
K22	VSS_191	VSS_284	BA9
G22	VSS_192	VSS_285	AW9
F22	VSS_193	VSS_286	AR9
E22	VSS_194	VSS_287	AH9
D22	VSS_195	VSS_288	AB9
A22	VSS_196	VSS_289	Y9
BA21	VSS_197	VSS_290	R9
AV21	VSS_198	VSS_291	G9
AR21	VSS_199	VSS_292	E9
AN21	VSS_200	VSS_293	A9
AL21	VSS_201	VSS_294	AG8
AB21	VSS_202	VSS_295	AD8
Y21	VSS_203	VSS_296	AA8
P21	VSS_204	VSS_297	U8
K21	VSS_205	VSS_298	K8
J21	VSS_206	VSS_299	C8
H21	VSS_207	VSS_300	BA7
C21	VSS_208	VSS_301	AV7
AW20	VSS_209	VSS_302	AP7
AR20	VSS_210	VSS_303	AL7
AM20	VSS_211	VSS_304	AJ7
AA20	VSS_212	VSS_305	AH7
K20	VSS_213	VSS_306	AF7
B20	VSS_214	VSS_307	AC7
A20	VSS_215	VSS_308	R7
AN19	VSS_216	VSS_309	G7
AC19	VSS_217	VSS_310	D7
W19	VSS_218	VSS_311	AG6
K19	VSS_219	VSS_312	AD6
G19	VSS_220	VSS_313	AB6
C19	VSS_221	VSS_314	Y6
AH18	VSS_222	VSS_315	U6
P18	VSS_223	VSS_316	N6
H18	VSS_224	VSS_317	K6
D18	VSS_225	VSS_318	H6
A18	VSS_226	VSS_319	B6
AY17	VSS_227	VSS_320	AV5
AR17	VSS_228	VSS_321	AF5
AP17	VSS_229	VSS_322	AD5
AM17	VSS_230	VSS_323	AY4
AK17	VSS_231	VSS_324	AR4
AV16	VSS_232	VSS_325	AP4
AN16	VSS_233	VSS_326	AL4
AL16	VSS_234	VSS_327	AJ4
J16	VSS_235	VSS_328	Y4
F16	VSS_236	VSS_329	U4
C16	VSS_237	VSS_330	R4
AN15	VSS_238	VSS_331	J4
AM15	VSS_239	VSS_332	F4
AK15	VSS_240	VSS_333	C4
N15	VSS_241	VSS_334	AY3
M15	VSS_242	VSS_335	AW3
L15	VSS_243	VSS_336	AV3
B15	VSS_244	VSS_337	AL3
A15	VSS_245	VSS_338	AH3
BA14	VSS_246	VSS_339	AG3
AT14	VSS_247	VSS_340	AF3
AK14	VSS_248	VSS_341	AD3
AD14	VSS_249	VSS_342	AC3
AA14	VSS_250	VSS_343	AA3
U14	VSS_251	VSS_344	G3
K14	VSS_252	VSS_345	AT2
H14	VSS_253	VSS_346	AR2
E14	VSS_254	VSS_347	AP2
AV13	VSS_255	VSS_348	AK2
AR13	VSS_256	VSS_349	AJ2
AN13	VSS_257	VSS_350	AD2
AM13	VSS_258	VSS_351	AB2
AL13	VSS_259	VSS_352	Y2
AG13	VSS_260	VSS_353	U2
P13	VSS_261	VSS_354	T2
F13	VSS_262	VSS_355	N2
D13	VSS_263	VSS_356	J2
B13	VSS_264	VSS_357	H2
AY12	VSS_265	VSS_358	F2
AC12	VSS_266	VSS_359	C2
K12	VSS_267	VSS_360	AL1
H12	VSS_268		
E12	VSS_269		
AD11	VSS_270		
AA11	VSS_271		
Y11	VSS_272		

NB Grounds

SYNC_MASTER=NB SYNC_DATE=07/25/2005

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SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 18 OF 98	

Power Interface

These are the power signals that leave the NB "block"

IN	=PP1V05_S0_FSB_NB	12A7 12B7 12C2 33B8 33C7 33C8 64D6
IN	=PPVCORE_S0_NB	16C8 16D3 19C8 64D6
IN	=PP1V05_S0_NB	19D1 64C6
IN	=PP1V05_S0_NB_VTT	17D3 19B5 64C6
IN	=PP1V5_S0_NB	19C1 64C6
IN	=PP1V5_S0_NB_PCIE	13D2 64C6
IN	=PP1V5_S0_NB_PLL	19C6 64C6
IN	=PP1V5_S0_NB_TVDAC	19A8 64C6
IN	=PP1V5_S0_NB_VCCD_HMPLL	17C6 64C6
IN	=PP1V5_S0_NB_VCCD_LVDS	17C6 19B8 64C6
IN	=PP1V5_S0_NB_VCCAUX	16D1 17B6 19B6 64C6
IN	=PP1V8_S3_MEM_NB	14C2 16B6 28D2 29D2 61C2 64C6
IN	=PP2V5_S0_NB_CRTDAC	19D4 64B6
IN	=PP2V5_S0_NB_VCCSYNC	17D6 19B6 64B6
IN	=PP2V5_S0_NB_VCC_TXLVDS	17D6 19B8 64B6
IN	=PP2V5_S0_NB_VCCA_3GBG	17D6 19B7 64B6
IN	=PP2V5_S0_NB_VCCA_LVDS	17C6 19D1 64B6
IN	=PP3V3_S0_NB	14C7 14D6 28A4 28B4 64A6
IN	=PP3V3_S0_NB_VCC_HV	17C6 19B7 64B6
IN	=PP5V_S0_NB_TVDAC	19C4 64D3

MCH DISPLAY PLL POWER LDO

CRITICAL
U1900
TPS73115
SOT23-5
IN OUT
EN NR/FB
GND

64B6 =PP2V5_S0_NB_DISP_PLL
C1950 1UF 10% 6.3V CERM 402
C1951 0.01uF 10% 16V CERM 402
C1952 10uF 20% 6.3V X5R 603
PP1V5_S0_DPLL
TPS73115_NR

R1950 0 5% 1/16W MF-LF 402
PP1V5_S0_NB_VCCA_DPLLA
VOLTAGE=1.5V
MIN_LINE_WIDTH=1.0 mm
MIN_NECK_WIDTH=1.0 mm
17C6
C1953 0.1uF 20% 10V CERM 402

MCH VCCA_DPLLA FILTER
(MCH DISPLAY A PLL 1.5V PWR)

R1951 0 5% 1/16W MF-LF 402
PP1V5_S0_NB_VCCA_DPLLB
VOLTAGE=1.5V
MIN_LINE_WIDTH=1.0 mm
MIN_NECK_WIDTH=1.0 mm
17C6
C1954 0.1uF 20% 10V CERM 402

GMCH VCCA_DPLL_B FILTER
(MCH DISPLAY B PLL 1.5V PWR)

Layout Note:
THESE 4 0.1UF CAPS SHOULD
be within 5 mm of NB edge

MCH VCCA_LVDS FILTER

(MCH LVDS ANALOG 2.5V PWR)
=PP2V5_S0_NB_VCCA_LVDS 17C6 19C7 64B6

C1980 0.1uF 20% 10V CERM 402
C1981 0.01uF 10% 16V CERM 402
GND_NB_VSSA_LVDS 17C6

Layout Note:
This 0.1uF cap should
be within 5 mm of NB edge

Layout Note: Route to caps, then GND

64B6 19D7 =PP2V5_S0_NB_CRTDAC
R1985 10 1% 1/16W MF-LF 402
PP2V5_S0_NB_CRTDAC_FOLLOW
VOLTAGE=2.5V
MIN_LINE_WIDTH=1.0 mm
MIN_NECK_WIDTH=1.0 mm
D1986 BAT54DW SOT-363
=PP1V05_S0_NB 19D7 64C6

L1985 180-OHM-1.5A 0603
PP2V5_S0_NB_CRTDAC_F

MCH VCCA_CRTDAC BYPASS
(MCH CRTDAC ANALOG 2.5V PWR)

C1986 22000pF-1000mA 16V NFM18
PP2V5_S0_NB_VCCA_CRTDAC
VOLTAGE=2.5V
MIN_LINE_WIDTH=1.0 mm
MIN_NECK_WIDTH=1.0 mm
17D6

C1985 0.1uF 20% 10V CERM 402

Layout Note:
These 2 caps should be
within 6.35 mm of NB edge

GND_NB_VSSA_CRTDAC 17D6

Layout Note: Route to caps, then GND

GMCH VCCA_HPLL FILTER

(HOST PLL 1.5V PWR)

64C6 19D7 =PP1V5_S0_NB_PLL
L1934 FERR-120-OHM-0.2A 0603
PP1V5_S0_NB_VCCA_HPLL
VOLTAGE=1.5V
MIN_LINE_WIDTH=1.0 mm
MIN_NECK_WIDTH=1.0 mm
17C6
C1934 22UF 20% 6.3V CERM-X5R 805 CRITICAL
C1935 0.1uF 20% 10V CERM 402

GMCH VCCA_MPLL FILTER
(MCH MEMORY PLL 1.5V PWR)

L1936 FERR-120-OHM-0.2A 0603
PP1V5_S0_NB_VCCA_MPLL
VOLTAGE=1.5V
MIN_LINE_WIDTH=1.0 mm
MIN_NECK_WIDTH=1.0 mm
17C6
C1936 22UF 20% 6.3V CERM-X5R 805 CRITICAL
C1937 0.1uF 20% 10V CERM 402

64C3 29D6 29D4 29B2 28D6 28D4 28B2 19C8 =PP1V8_S3_MEM
64C3 29D6 29D4 29B2 28D6 28D4 28B2 19C8 =PP1V8_S3_MEM

PLACE THOSE COMPONENT
CLOSE TO GMCH

R1988 1K 1% 1/16W MF-LF 402
MEM_VREF_NB_0 14C2
VOLTAGE=0.9V
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
R1989 1K 1% 1/16W MF-LF 402

R1986 1K 1% 1/16W MF-LF 402
MEM_VREF_NB_1 14C2
VOLTAGE=0.9V
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
R1987 1K 1% 1/16W MF-LF 402

GMCH CORE PWR 1.05V BYPASS
THIS 470UF FOR GMCH CORE 1.05V

19D7 16D3 16C8 64D6 =PPVCORE_S0_NB
CRITICAL
C1900 470UF 20% 2.5V TANT D2T
C1902 10uF 20% 6.3V X5R 603
C1903 10uF 20% 6.3V X5R 603
C1904 1UF 10% 6.3V CERM 402
C1905 0.22uF 20% 6.3V X5R 402
C1906 0.22uF 20% 6.3V X5R 402
C1907 0.22uF 20% 6.3V X5R 402

GMCH VCCD_LVDS BYPASS
(MCH LVDS DIGITAL 1.5V PWR)

64C6 19D7 17C6 =PP1V5_S0_NB_VCCD_LVDS
C1910 10uF 20% 6.3V X5R 603
C1911 0.1uF 20% 10V CERM 402

945 EDS: 5 mOhm, 1nH (1210?)

GMCH VCCTX_LVDS BYPASS
(MCH LVDS DATA/CLK TX 2.5V PWR)

64B6 19D7 17D6 =PP2V5_S0_NB_VCC_TXLVDS
C1912 4.7uF 20% 6.3V CERM 603
C1913 0.1uF 20% 10V CERM 402

945 EDS: 1210?

MCH VCC_HV BYPASS
(MCH HV BUFFER 3.3V PWR)

64B6 19C7 17C6 =PP3V3_S0_NB_VCC_HV
C1914 10uF 20% 6.3V X5R 603
C1915 0.1uF 20% 10V CERM 402

MCH VCCSYNC BYPASS
(MCH H/V SYNC 2.5V PWR)

19D7 17D6 64B6 =PP2V5_S0_NB_VCCSYNC
C1917 0.1uF 20% 10V CERM 402

MCH VCCA_3GBG BYPASS
(MCH PCIE/DMI BAND GAP 2.5V PWR)

64B6 19D7 17D6 =PP2V5_S0_NB_VCCA_3GBG
C1916 0.1uF 20% 10V CERM 402

GMCH VCCAUX FILTER
(MCH DDR DLL&IO, FSB HSIO&IO PWR 1.5V)

64C6 19D7 17B6 16D1 =PP1V5_S0_NB_VCCAUX
C1918 0.1uF 20% 10V CERM 402

MCH VTT BYPASS
(MCH FSB 1.05V PWR) (SHARE C0940 470UF)

64C6 19D7 17D3 =PP1V05_S0_NB_VTT
C1965 4.7uF 20% 6.3V CERM 603
C1966 2.2uF 20% 6.3V CERM1 603
Layout Note:
Place in cavity
C1967 0.22uF 20% 6.3V X5R 402
Layout Note:
Place on the edge

GMCH VCC3G FILTER
(PCI-E/DMI ANALOG 1.5V PWR)

91nH, 20%, 20MOHM, 1.5A (1210 TYP)
CRITICAL
L1970 91nH 1210
64C6 =PP1V5_S0_NB_3G
C1970 220UF 20% 2.5V POLY CASE-B2
Layout Note:
Place L and C
close to MCH
C1971 10uF 20% 6.3V X5R 603
C1972 10uF 20% 6.3V X5R 603
PP1V5_S0_NB_VCC3G
VOLTAGE=1.5V
MIN_LINE_WIDTH=1.0 mm
MIN_NECK_WIDTH=1.0 mm
17D6
Layout Note:
10uF caps should
be close to MCH
on opposite side.

CRITICAL
U1901
MM157
SOT23-5-LF
64D3 19C7 =PP5V_S0_NB_TVDAC
VIN VOUT
CONT NOISE
GND
PP3V3_S0_NB_TVDAC
MM1573DN_NR
C1940 1UF 10% 6.3V CERM 402
C1941 0.01uF 10% 16V CERM 402
C1942 1UF 10% 6.3V CERM 402

R1990 10 1% 1/16W MF-LF 402
PP3V3_S0_NB_TVDAC_FOLLOW
VOLTAGE=3.3V
MIN_LINE_WIDTH=1.0 mm
MIN_NECK_WIDTH=1.0 mm
D1986 BAT54DW SOT-363
=PP1V5_S0_NB 19D7 64C6

L1990 180-OHM-1.5A 0603
PP3V3_S0_NB_TVDAC_F

MCH VCCA_TVDACC FILTER
(MCH TV OUT CHANNEL A 3.3V PWR)

C1992 22000pF-1000mA 16V NFM18
PP3V3_S0_NB_VCCA_TVDACA
VOLTAGE=3.3V
MIN_LINE_WIDTH=1.0 mm
MIN_NECK_WIDTH=1.0 mm
17C6
C1990 10uF 20% 6.3V X5R 603
C1991 0.1uF 20% 10V CERM 402

MCH VCCA_TVDACC FILTER
(MCH TV OUT CHANNEL B 3.3V PWR)

C1994 22000pF-1000mA 16V NFM18
PP3V3_S0_NB_VCCA_TVDACB
VOLTAGE=3.3V
MIN_LINE_WIDTH=1.0 mm
MIN_NECK_WIDTH=1.0 mm
17C6
C1993 0.1uF 20% 10V CERM 402

Layout Note:
These 8 caps should be
within 6.35 mm of NB edge

MCH VCCA_TVDACC FILTER
(MCH TV OUT CHANNEL C 3.3V PWR)

C1996 22000pF-1000mA 16V NFM18
PP3V3_S0_NB_VCCA_TVDACC
VOLTAGE=3.3V
MIN_LINE_WIDTH=1.0 mm
MIN_NECK_WIDTH=1.0 mm
17C6
C1995 0.1uF 20% 10V CERM 402

MCH VCCA_TVBG FILTER
(MCH TV DAC BAND GAP 3.3V PWR)

C1998 22000pF-1000mA 16V NFM18
PP3V3_S0_NB_VCCA_TVBG
VOLTAGE=3.3V
MIN_LINE_WIDTH=1.0 mm
MIN_NECK_WIDTH=1.0 mm
17C6
C1997 0.1uF 20% 10V CERM 402

GND_NB_VSSA_TVBG 17C6

Layout Note: Route to caps, then GND

GMCH VCCD_TVDAC FILTER
(MCH TVDAC DEDICATED PWR 1.5V)

64C6 19D7 =PP1V5_S0_NB_TVDAC
C1921 22000pF-1000mA 16V NFM18
PP1V5_S0_NB_VCCD_TVDAC
VOLTAGE=1.5V
MIN_LINE_WIDTH=1.0 mm
MIN_NECK_WIDTH=1.0 mm
17C6
C1920 0.1uF 20% 10V CERM 402

Layout Note:
These 4 caps should be
within 6.35 mm of NB edge

GMCH VCCD_QTVDAC FILTER
(MCH TVDAC DIGITAL QUIET 1.5V PWR)

L1922 180-OHM-1.5A 0603
PP1V5_S0_NB_QTVDAC
C1923 22000pF-1000mA 16V NFM18
PP1V5_S0_NB_VCCD_QTVDAC
VOLTAGE=1.5V
MIN_LINE_WIDTH=1.0 mm
MIN_NECK_WIDTH=1.0 mm
17B6
C1922 0.1uF 20% 10V CERM 402

GMCH VCCA_3GPLL FILTER
(3GIO PLL 1.5V PWR)

1uH, 20%
L1975 1.0UH-220MA-0.12-OHM 0805
64C6 =PP1V5_S0_NB_3GPLL
PP1V5_S0_NB_3GPLL_F
VOLTAGE=1.5V
MIN_LINE_WIDTH=1.0 mm
MIN_NECK_WIDTH=1.0 mm
R1975 0.51 1% 1/16W MF-LF 402
PP1V5_S0_NB_VCCA_3GPLL
VOLTAGE=1.5V
MIN_LINE_WIDTH=1.0 mm
MIN_NECK_WIDTH=1.0 mm
17D6
C1975 10uF 20% 6.3V X5M 603
C1976 0.1uF 20% 10V CERM 402

Layout Note:
3GPLL 10uF cap should
be placed in cavity

GND_NB_VSSA_3GBG 17D6

Layout Note: Route to caps, then GND

NB (GM) Decoupling

SYNC_MASTER=NB SYNC_DATE=06/22/2005

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SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 19 OF 98	

NB_CFG<3>	RESERVED

NB_CFG<4>	RESERVED

14C6 NB_CFG<5>
Internal pull-up

NB_CFG<5> DMI x2 Select	High = DMIx4 Low = DMIx2

NBCFG_DMI_X2
R2075
2.2K
5%
1/16W
MF-LF
402

PROBABLY NOT NEEDED

NB_CFG<6>	RESERVED

14C6 NB_CFG<7>
Internal pull-up

NB_CFG<7> CPU Strap	High = Mobile CPU Low = RESERVED

NO STUFF
R2077
2.2K
5%
1/16W
MF-LF
402

NB_CFG<8>	RESERVED

14C6 NB_CFG<9>
Internal pull-up

NB_CFG<9> PCIE Graphics Lane Reversal	High = Normal Low = Reversed

NBCFG_PEG_REVERSE
R2079
2.2K
5%
1/16W
MF-LF
402

NB_CFG<10>	RESERVED

NB_CFG<11>	RESERVED

Internal pull-ups

NB_CFG<13:12>	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal Operation

NB_CFG<14>	RESERVED

NB_CFG<15>	RESERVED

14C6 NB_CFG<16>
Internal pull-up

NB_CFG<16> FSB Dynamic ODT	High = Enabled Low = Disabled

NBCFG_DYN_ODT_DISABLE
R2085
2.2K
5%
1/16W
MF-LF
402

NB_CFG<17>	RESERVED

=PP3V3_S0_NB 14C7 14D6 19C7 20A4 20B4 64A6
NBCFG_VCC_1V5
R2058
2.2K
5%
1/16W
MF-LF
402

NB_CFG<18> VCC Select	High = 1.5V Low = 1.05V

14C6 NB_CFG<18>
Internal pull-down

=PP3V3_S0_NB 14C7 14D6 19C7 20A4 20B4 64A6
NBCFG_DMI_REVERSE
R2059
2.2K
5%
1/16W
MF-LF
402

NB_CFG<19> DMI Lane Reversal	High = Reversed Low = Normal

14C6 NB_CFG<19>
Internal pull-down

945 External Design Spec says reserved

=PP3V3_S0_NB 14C7 14D6 19C7 20B4 64A6
NBCFG_SDVO_AND_PCIE
R2060
2.2K
5%
1/16W
MF-LF
402

NB_CFG<20> PCIe Backward Interop. Mode	High = Both active Low = Only SDVO or PCIe x1

14B6 NB_CFG<20>
Internal pull-down

PROBABLY NOT NEEDED

NB Config Straps

SYNC_MASTER=NB SYNC_DATE=06/28/2005

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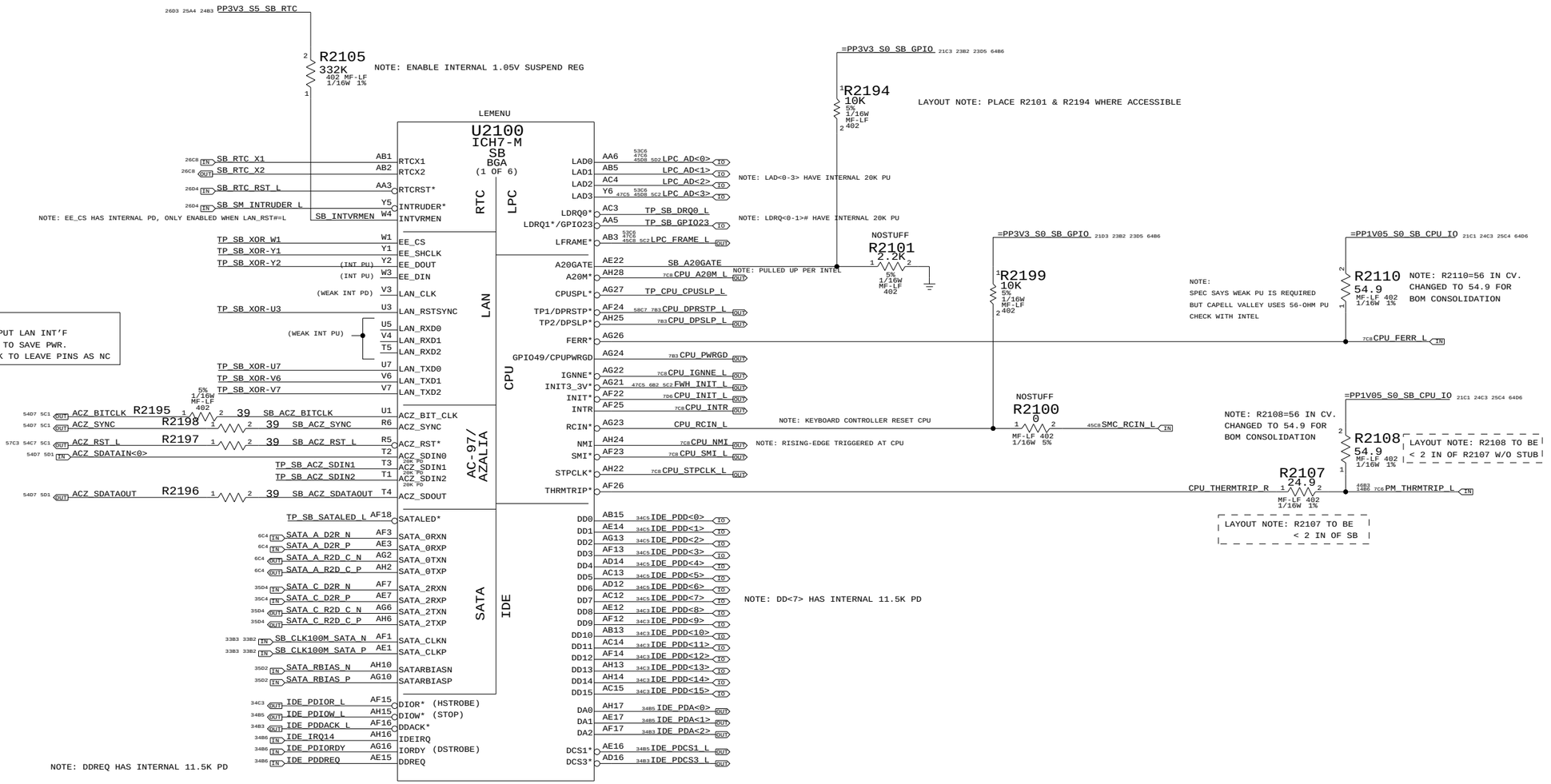
SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 20 OF 98	



	AC '07	INTEL HIGH DEFINITION AUDIO
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	INTERNAL 20K PD ONLY ENABLED IN S3COLD
ACZ_RST#		NONE
ACZ_SDIN[0-2]	INTERNAL 20K PD	INTERNAL 20K PD
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
ACZ_SYNC		INTERNAL 20K PD

SB: 1 OF 4

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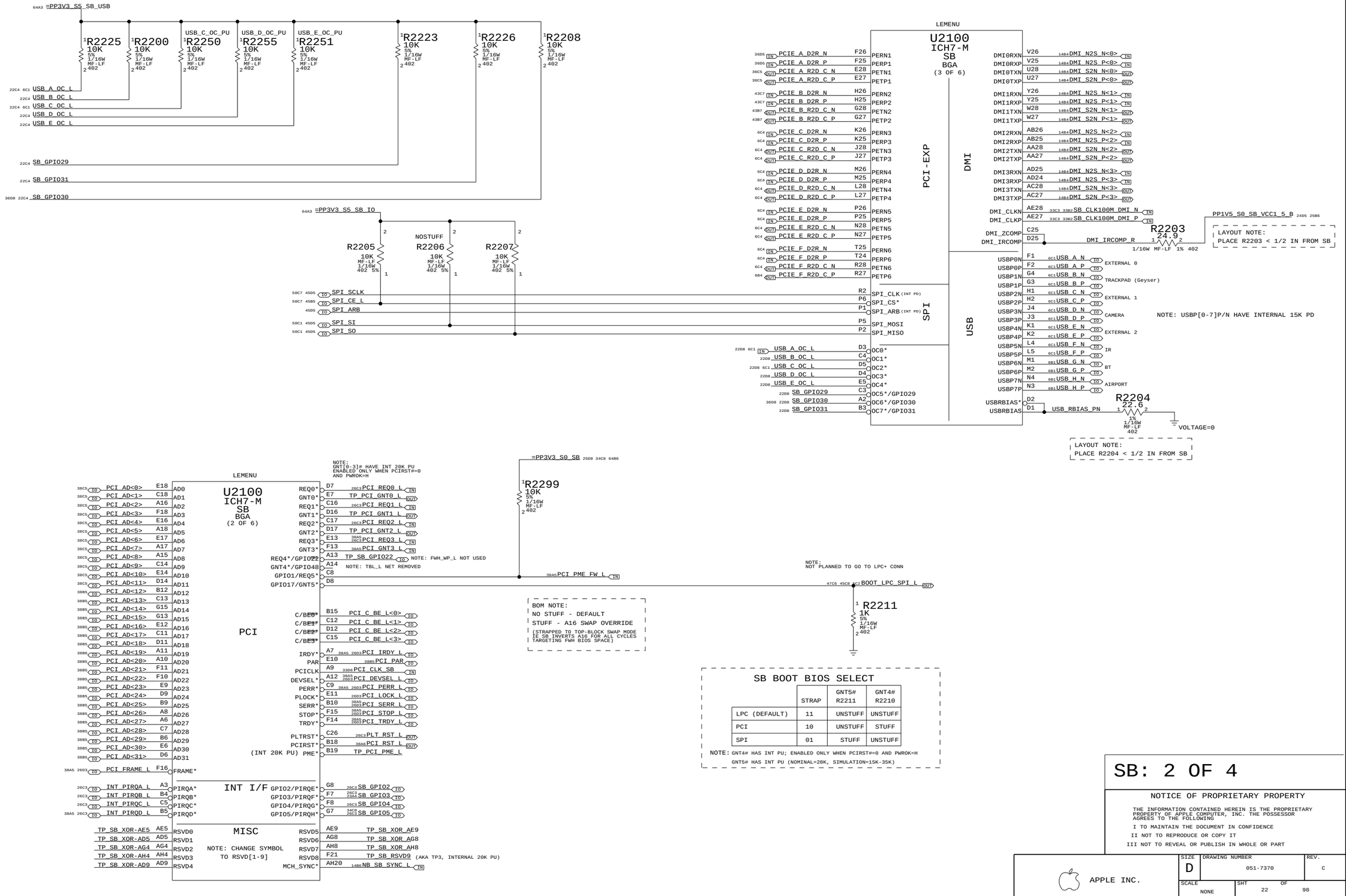
SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 21 OF 98	



NOTE FOR R2323 (DEF=NOSTUFF)
STRAPPING @ PWROK RISING:
SB WILL DISABLE TCO TIMER
SYSTEM REBOOT FEATURE

=PP3V3_S0_SB_GPIO 21C3 21D3 23B2 64B6

=PP3V3_S5_SB 23A7 23B7 23D8 25C8 64A3

64A3 25C8 23D4 23B7 23A7 =PP3V3_S5_SB

R2318 10K 1/16W 402 MF-LF 5%
R2395 8.2K 1/16W 402 MF-LF 5%
R2396 10K 1/16W 402 MF-LF 5%
R2397 8.2K 1/16W 402 MF-LF 5%
R2327 NOSTUFF 10K 1/16W 402 MF-LF 5%
R2326 NOSTUFF 10K 1/16W 402 MF-LF 5%
R2323 NO_REBOOT_MODE 1K 1/16W 402 MF-LF 5%

RP2300 10K 5% 1/16W SM-LF

R2398 1K 1/16W 402 MF-LF 5%
R2320 10K 1/16W 402 MF-LF 5%
R2317 10K 1/16W 402 MF-LF 5%
R2316 10K 1/16W 402 MF-LF 5%

LEMENU

U2100
ICH7-M
SB
BGA
(4 OF 6)

27D8 TO SMB_CLK — C22 SMBCLK
27D8 TO SMB_DATA — B22 SMBDATA
SMB_LINK_ALERT_L — A26 LINKALERT*
SMLINK<0> — B25 SMLINK0
NOT USED — SMLINK<1> — A25 SMLINK1
PM_RI_L — A28 RI*
SB_SPKR — A19 SPKR (INT WEAK PD)
53C6 47C5 46D3 45D5 5C2 OUT PM_SUS_STAT_L — A27 SUS_STAT*
45C8 26C5 IN PM_SYSRST_L — A22 SYS_RST*
14B6 IN PM_BMBUSY_L — AB18 GPIO0/BM_BUSY*
SMB_ALERT_L — B23 GPIO11/SMBALERT*
NOTE: RESERVED FOR FUTURE
32C4 OUT PM_STPPCI_L — AC20 GPIO18/STPPCI*
32C4 OUT PM_STPCPU_L — AF21 GPIO20/STPCPU*
IN SB_GPIO26 — A21 GPIO26
23A6 BIOS_REC — B21 GPIO27
23A6 FWH_MFG_MODE — E23 GPIO28
53C6 47C6 45D5 38A5 5C2 TO PM_CLKRUN_L — AG18 GPIO32/CLKRUN*
RESERVED FOR MOBILE AZALIA DOCKING INT'F
TP_AZ_DOCK_EN_L — AC19 GPIO33/AZ_DOCK_EN*
TP_AZ_DOCK_RST_L — U2 GPIO34/AZ_DOCK_RST*
43C6 36C6 IN PCIE_WAKE_L — F20 WAKE*
53C6 47C5 45C8 5C2 TO INT_SERIRQ — AH21 SERIRQ
45B8 IN PM_THRM_L — AF20 THRM*
26A8 IN VR_PWRGD_CK410 — AD22 VRMPWRGD
TO TP_SB_GPIO6 — AC21 GPIO6
SB_RUNTIME_SCI_L — AC18 GPIO7
E21 GPIO8

SMB

SATA GPIO
GPIO21/SATA0GP — AF19 SB_GPIO21 — 100 — R2302
GPIO19/SATA1GP — AH18 SB_GPIO19 — 100 — R2303
GPIO36/SATA2GP — AH19
GPIO37/SATA3GP — AE19 SB_GPIO37 — 100 — R2305
35D2 SATA_C_DET_L IN

CLKS
CLK14 — AC1 33A6 SB_CLK14P3M_TIMER IN
CLK48 — B2 33C7 SB_CLK48M_USBCTLR IN
SUSCLK — C20 68A4 SUS_CLK_SB OUT

SYS GPIO / PWR MNGT
SLP_S3* — B24 63A7 45C5 63B8 PM_SLP_S3_L OUT
SLP_S4* — D23 63D6 61B8 60C8 45C5 PM_SLP_S4_L OUT
SLP_S5* — F22 46D3 45C5 PM_SLP_S5_L OUT
PWROK — AA4 26A6 PM_SB_PWROK IN
GPIO16/DPRSLPVR — AC22 58D8 14B7 PM_DPRSLPVR OUT
TP0/BATLOW* — C21 NOTE: DPRSLPVR HAS INT 20K PD, ENABLED AT BOOT/RESET FOR STRAPPING FCN
(INT 20K PU) PWRBTN* — C23 45D8 PM_PWRBTN_L IN
LAN_RST* — C19 45D8 PM_LAN_ENABLE IN
RSMRST* — Y4

NOTE:
SMC WILL DRIVE 0-1-0 TO KEEP LAN INT'F
IN RESET STATE TO SAVE PWR

GPIO
GPIO9 — E20 46D6 45B5 SMS_INT_L IN
GPIO10 — A20 45D8 SMC_SB_NMI IN
DEF=GPI GPIO12 — F19 23B3 PATA_PWR_EN_L OUT
GPIO13 — E19
DEF=GPI GPIO14 — R4 23A4 SB_GPIO14 OUT
GPIO15 — E22 SV_SET_UP 5C2 23B6 47B5
GPIO24 — R3 CRB_SV_DET 23B6
GPIO25 — D20 TP_SB_GPIO25_DO_NOT_USE
OD GPIO35 — AD21 32B4 SB_CLK100M_SATA_OE_L OUT
GPIO38 — AD20 TP_SB_GPIO38 TO
DEF=GPI GPIO39 — AE20 23A3 SATA_C_PWR_EN_L OUT

NOTE: PATA_DET IS ACTUALLY CABLE TYPE DETECT

NOTE FOR GPIO25:
- HAS INTERNAL 20K PU, ENABLED DURING RSMRST# AND DISABLED WITHIN 100MS AFTER RSMRST# DEASSERTS
- CAN NOT BE LOW FOR 35US AFTER RSMRST# ON BOOT (DMI AC COUPLING MODE STRAP)

=PP3V3_S5_SB_PM 11B5 26C5 64A3

R2319 10K 1/16W 402 MF-LF 5%
R2343 8.2K 5% 1/16W 402 MF-LF

45B8 PM_BATLOW_L IN
45D8 PM_RSMRST_L IN
R2399 100K 5% 1/16W 402 MF-LF
45D5 SMC_WAKE_SCI_L IN

R2300 0
45B8 IN SMC_RUNTIME_SCI_L
45B8 IN SMC_EXTSMI_L

64A3 25C8 23D8 23D4 23A7 =PP3V3_S5_SB

R2306 NOSTUFF 10K 1/16W 402 MF-LF 5%
R2308 10K 1/16W 402 MF-LF 5%
R2307 10K 1/16W 402 MF-LF 5%
R2309 NOSTUFF 0 1/16W 402 MF-LF 5%

SV_SET_UP 5C2 23C3 47B5
CRB_SV_DET 23C3

NOTE:
SV_SET_UP IS LINDACARD DETECT
HI = PRESENT
LO = NOT PRESENT

LAYOUT NOTE:
PLACE R2306-14 WHERE PHYSICALLY ACCESSIBLE

64A3 25C8 23D8 23D4 23B7 =PP3V3_S5_SB

R2313 10K 1/16W 402 MF-LF 5%
R2310 10K 1/16W 402 MF-LF 5%
R2314 NOSTUFF 0 1/16W 402 MF-LF 5%
R2311 NOSTUFF 10K 1/16W 402 MF-LF 5%

FWH_MFG_MODE 23C5
BIOS_REC 23C5

=PP3V3_S0_SB_GPIO 21C3 21D3 23D5 64B6

R2390 10K 5% 1/16W MF-LF 402
R2388 10K 5% 1/16W MF-LF 402

23C3 PATA_PWR_EN_L
23B3 SATA_C_PWR_EN_L

NOSTUFF
R2312 0 5% 1/16W MF-LF 402
26C3 22A6 SB_GPIO3

IDE_RESET_L 34C5

R2315 0 5% 1/16W MF-LF 402
23C3 SB_GPIO14

R2389 15K 5% 1/10W MF-LF 402

R2312,R2315 and R2389 close to SB

SB: 3 OF 4

NOTICE OF PROPRIETARY PROPERTY

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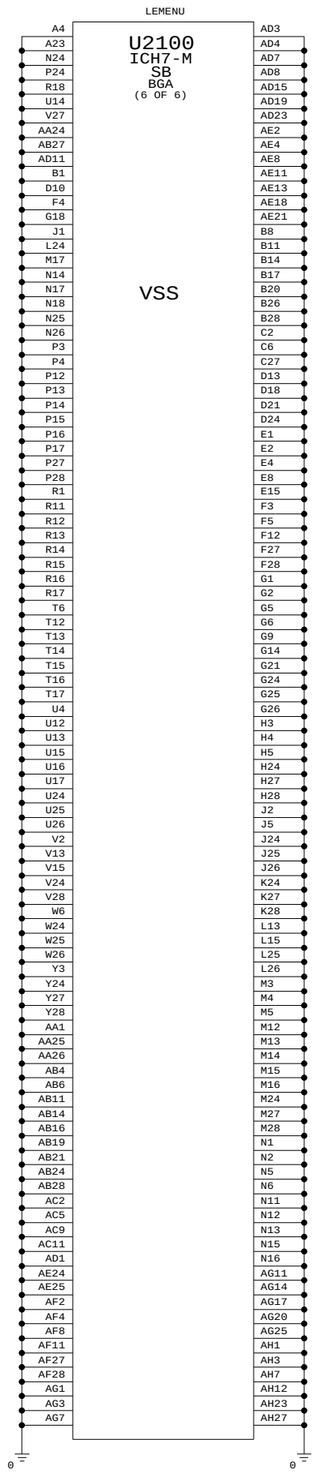
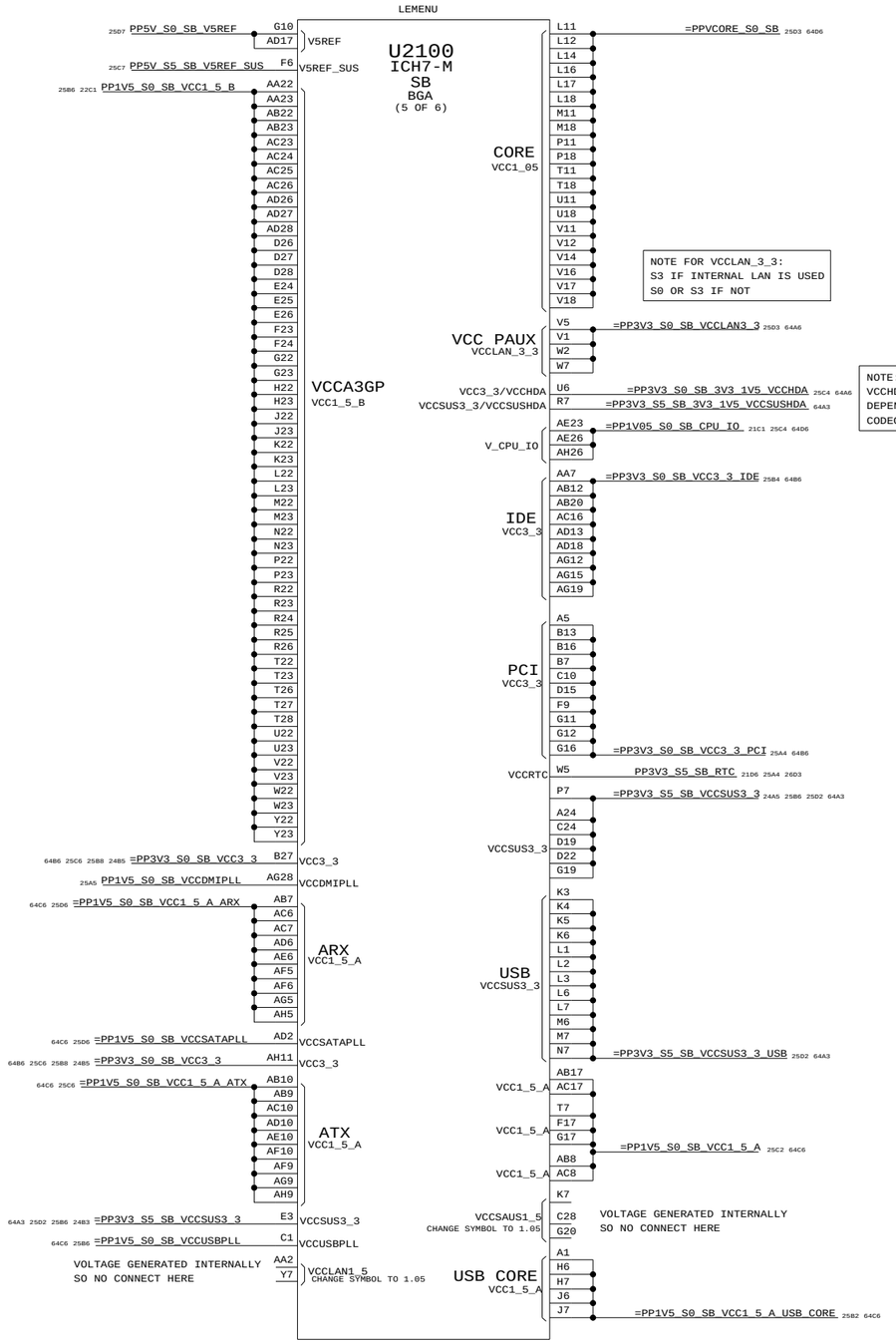
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 23 OF 98	





SB: 4 OF 4

NOTICE OF PROPRIETARY PROPERTY

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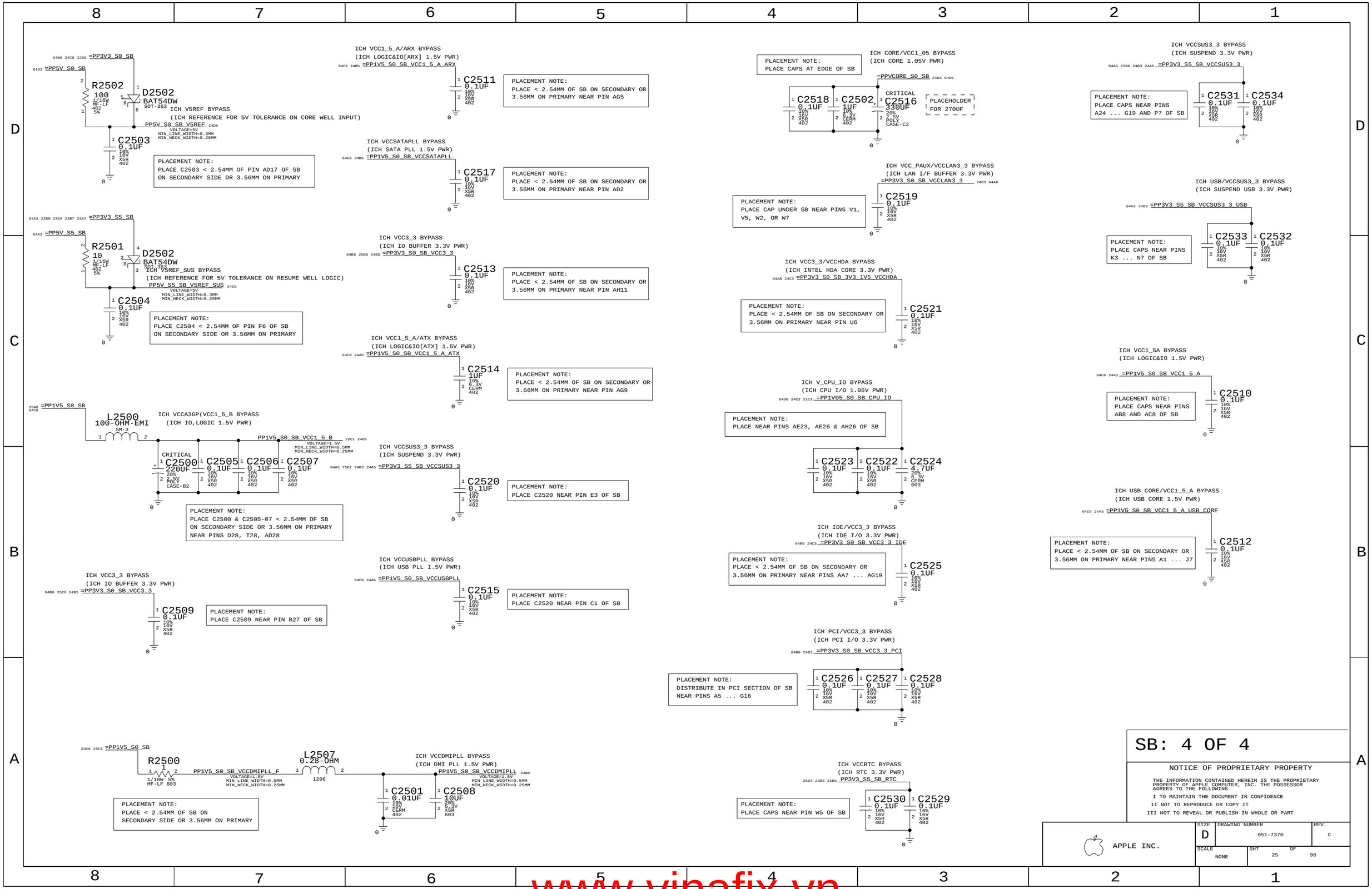
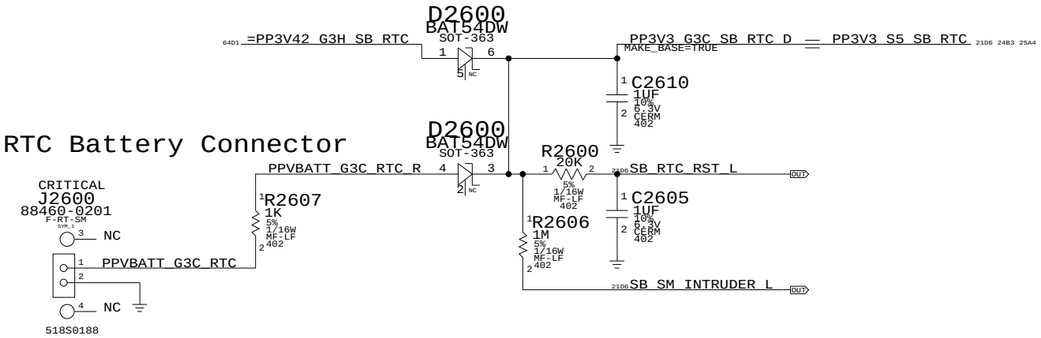
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

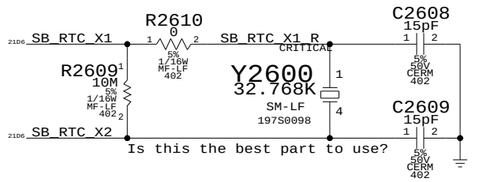
SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 24 OF 98	

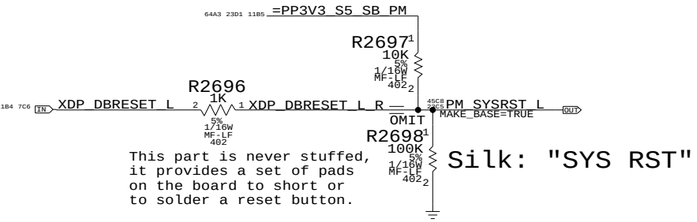


RTC Battery Connector

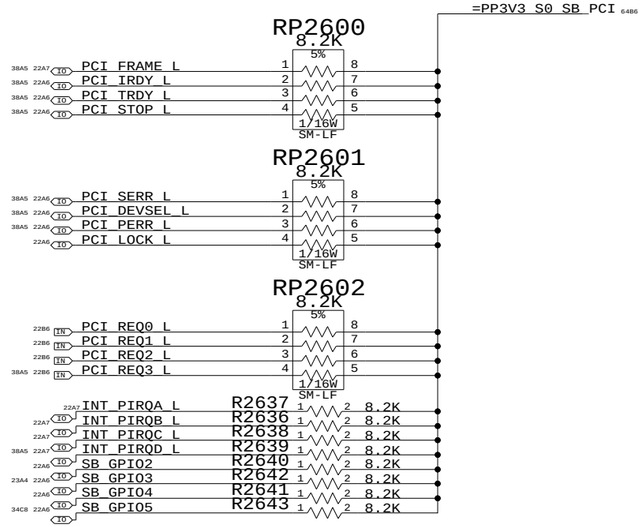


SB RTC Crystal Circuit



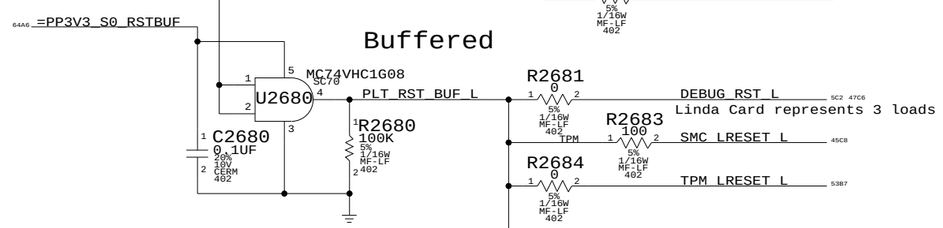


Platform Reset Connections

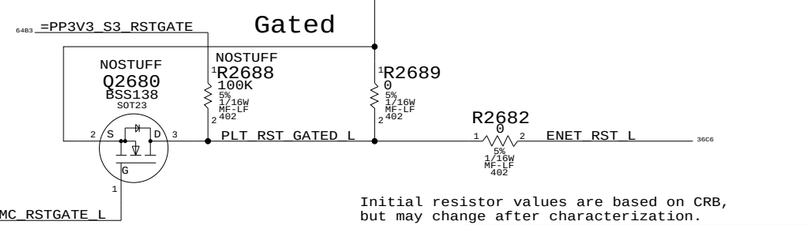


Unbuffered

Buffered

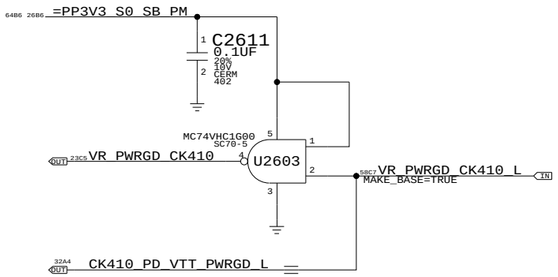


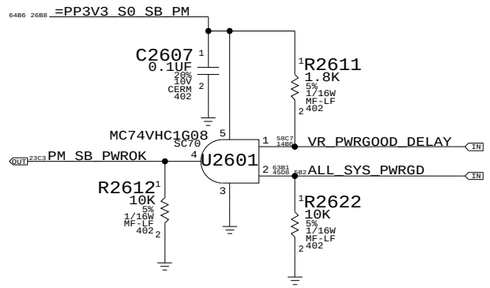
Gated



Initial resistor values are based on CRB,
but may change after characterization.

SB PM





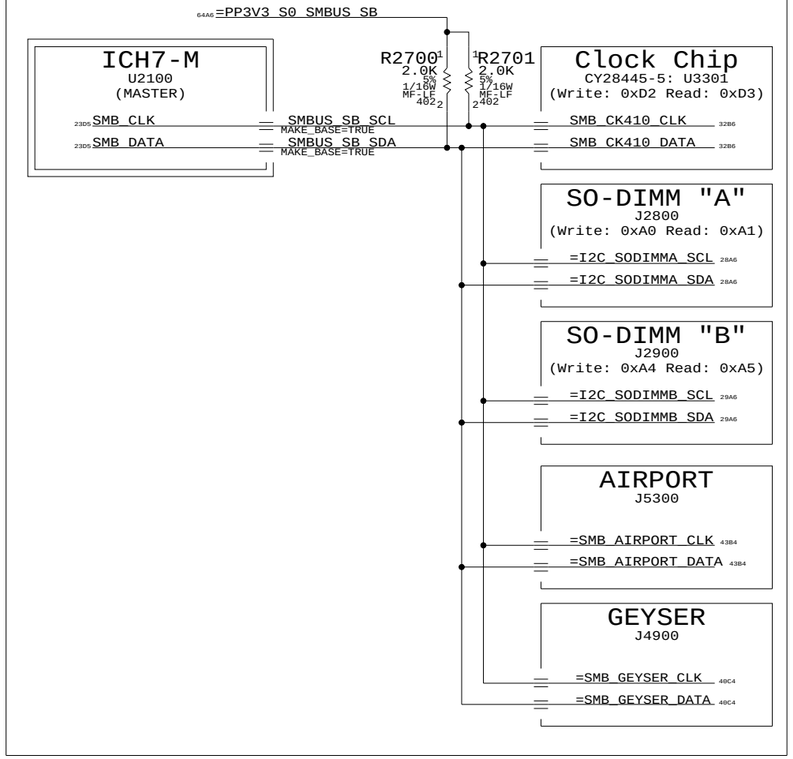
SB Misc

SYNC_MASTER=NB SYNC_DATE=07/26/2005

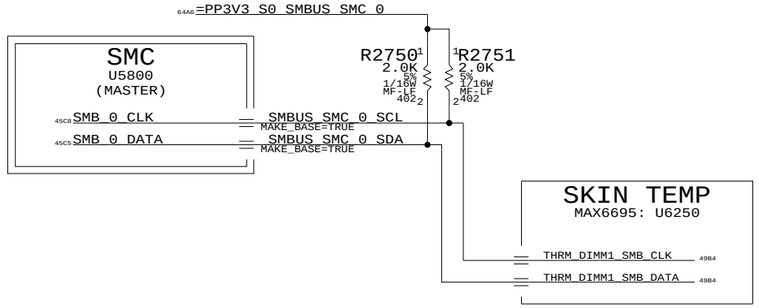
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 26 OF 98	

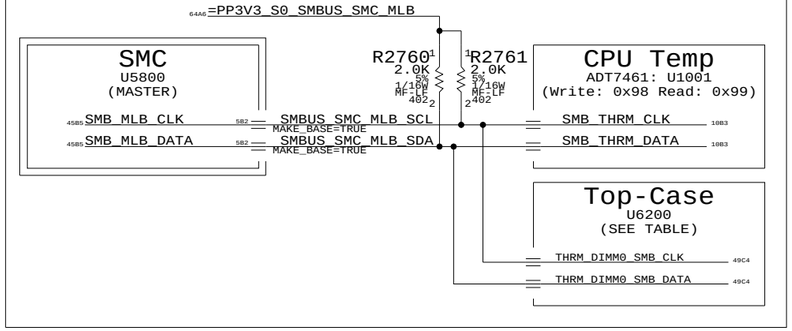
ICH7-M SMBus Connections



SMC "0" SMBus Connections

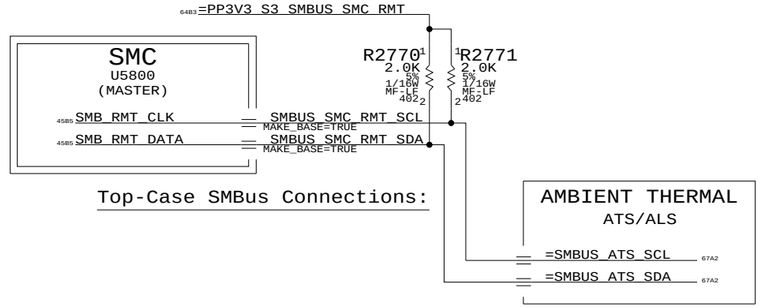


SMC "MLB" SMBus Connections

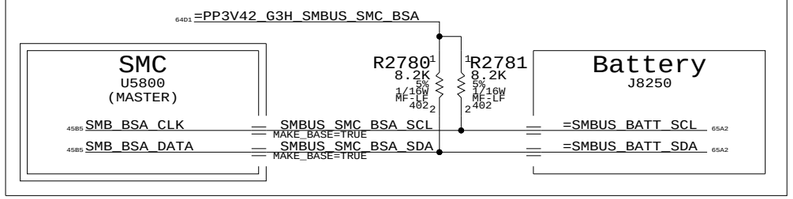


SMC "RMT" SMBus Connections

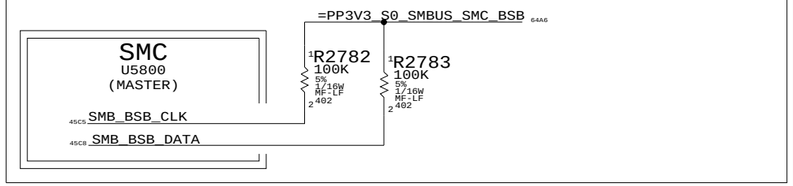
NOTE: SMC RMT bus remains powered and may be active in S3 state



SMC "Battery A" SMBus Connections



SMC "Battery B" SMBus Connections

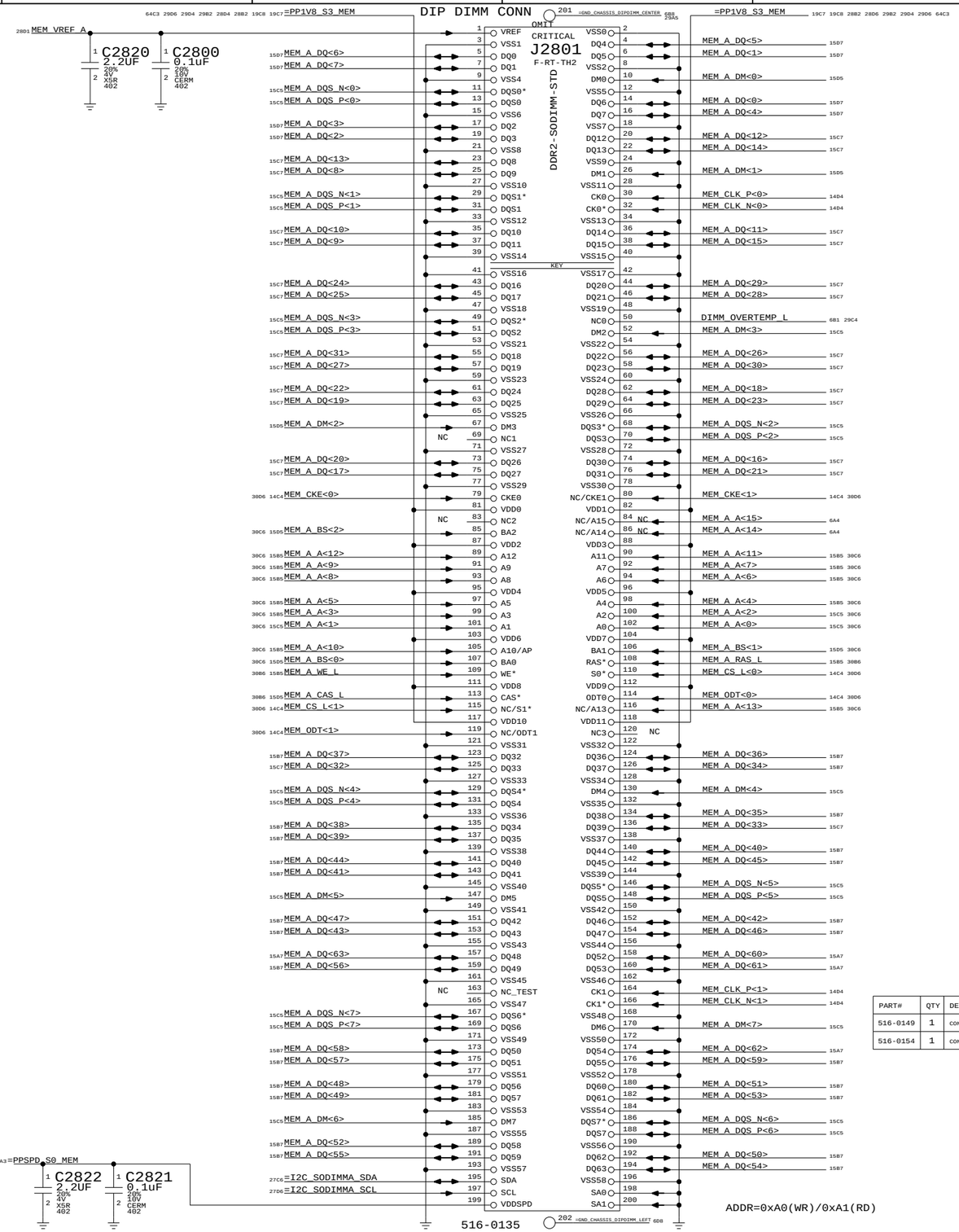


M42 SMBUS CONNECTIONS

SYNC_MASTER=ENET SYNC_DATE=08/30/2005

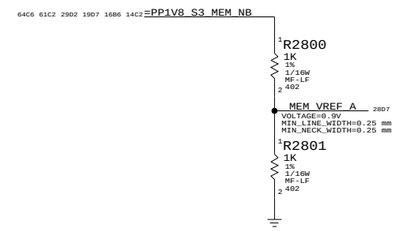
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 27 OF 98	



DDR2 VRef

One 0.1uF per connector



Yellow uses 10K divider and TLV2463
to drive MCH and DIMM connectors.
(See Capell Valley pg 47)

Page Notes

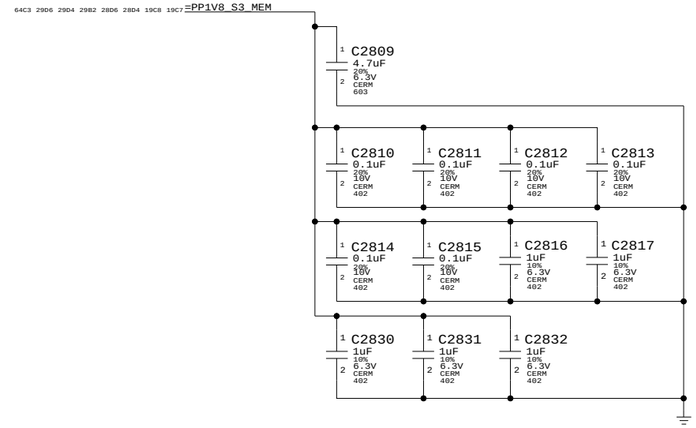
Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_MEM_SCL
- =I2C_MEM_SDA

BOM options provided by this page:
(NONE)

DDR2 Bypass Caps

(For return current)



The 4.7uF and 1.0uF caps can be changed to 5x 2.2uF caps,
when they get cheaper.

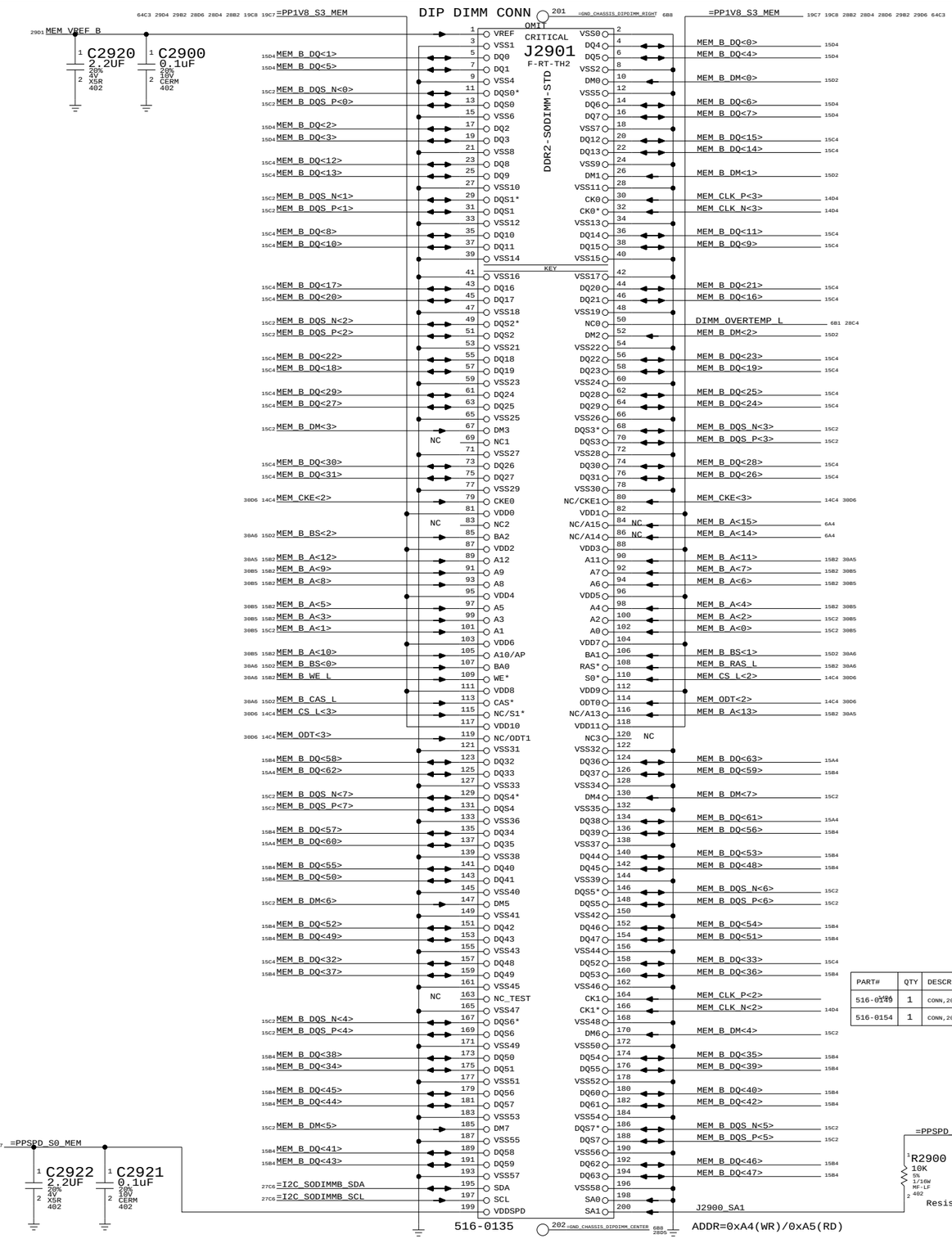
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
516-0149	1	CONN,200P STD SODIMM OLD REV	J2801	CRITICAL	PVT-DIMM
516-0154	1	CONN,200P STD SODIMM NEW REV 3.5	J2801	CRITICAL	POST-RAMP-DIMM35

DDR2 SO-DIMM Connector A

SYNC_MASTER=MEMORY SYNC_DATE=06/20/2005

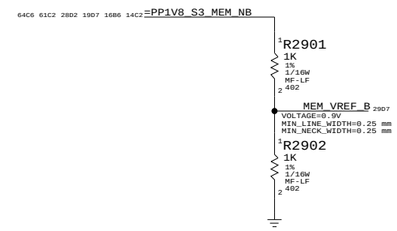
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 28 OF 98	



DDR2 VREF (FOR CONNECTOR B)

One 0.1uF per connector



Yellow uses 10K divider and TLV2463
to drive MCH and DIMM connectors.
(See Capell Valley pg 47)

Page Notes

Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

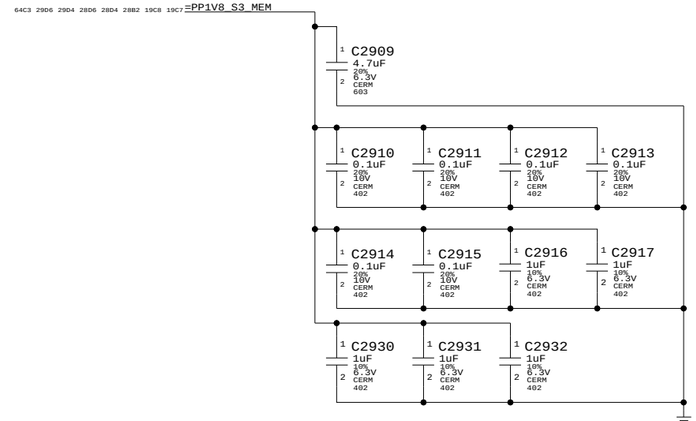
Signal aliases required by this page:
- =I2C_MEM_SCL
- =I2C_MEM_SDA

BOM options provided by this page:
(NONE)

NOTE: This page does not supply VREF.
The reference voltage must be provided
by another page.

DDR2 Bypass Caps

(For return current)



The 4.7uF and 1.0uF caps can be changed to 5x 2.2uF caps,
when they get cheaper.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
516-0149	1	CONN,200P STD SODIMM OLD REV	J2901	CRITICAL	PVT-DIMM
516-0154	1	CONN,200P STD SODIMM NEW REV 3.5	J2901	CRITICAL	POST-RAMP-DIMM35

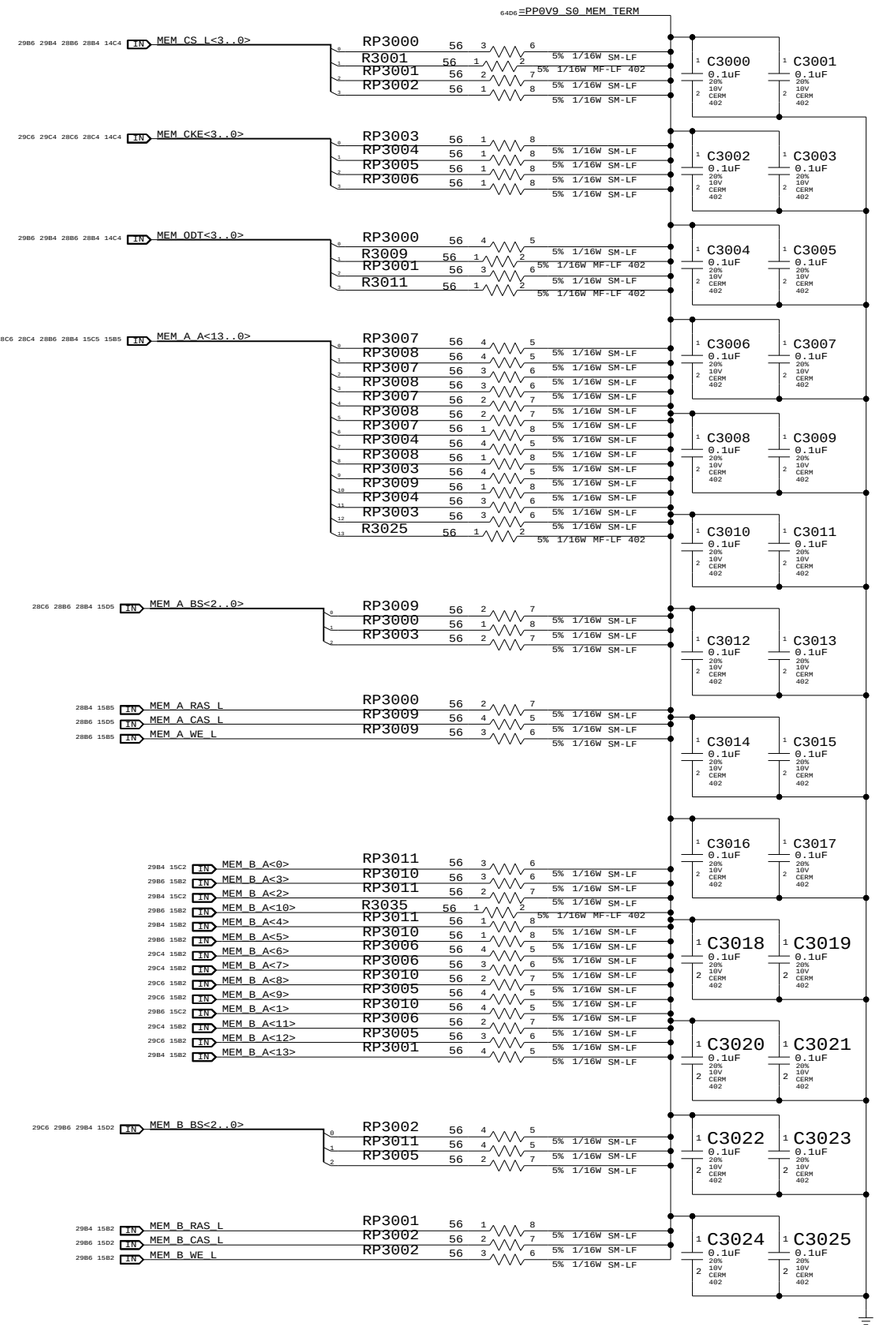
DDR2 SO-DIMM Connector B

SYNC_MASTER=MEMORY SYNC_DATE=06/20/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE	SHT	OF
NONE	29	98

One cap for each side of every RPAK, one cap for every two discrete resistors
BOMOPTION shown at the top of each group applies to every part below it



LAYOUT NOTE:PLACE ONE CAP CLOSE TO EVERY TWO PULLUP RESISTORS TERMINATED TO PP0V9_S0_MEM_TERM

Memory Active Termination

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE	SHT	OF
NONE	30	98

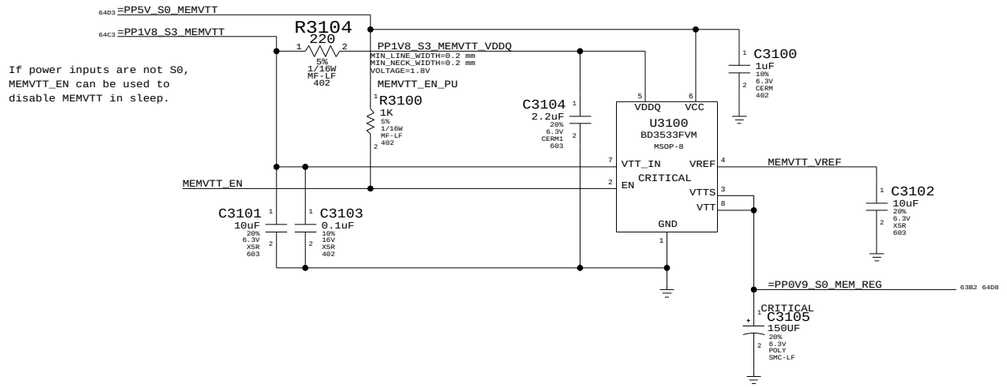
Page Notes

Power aliases required by this page:
- =PP5V_S0_MEMVTT
- =PP1V8_S0_MEMVTT
- =PP0V9_S0_MEMVTT_LDO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

DDR2 Vtt Regulator



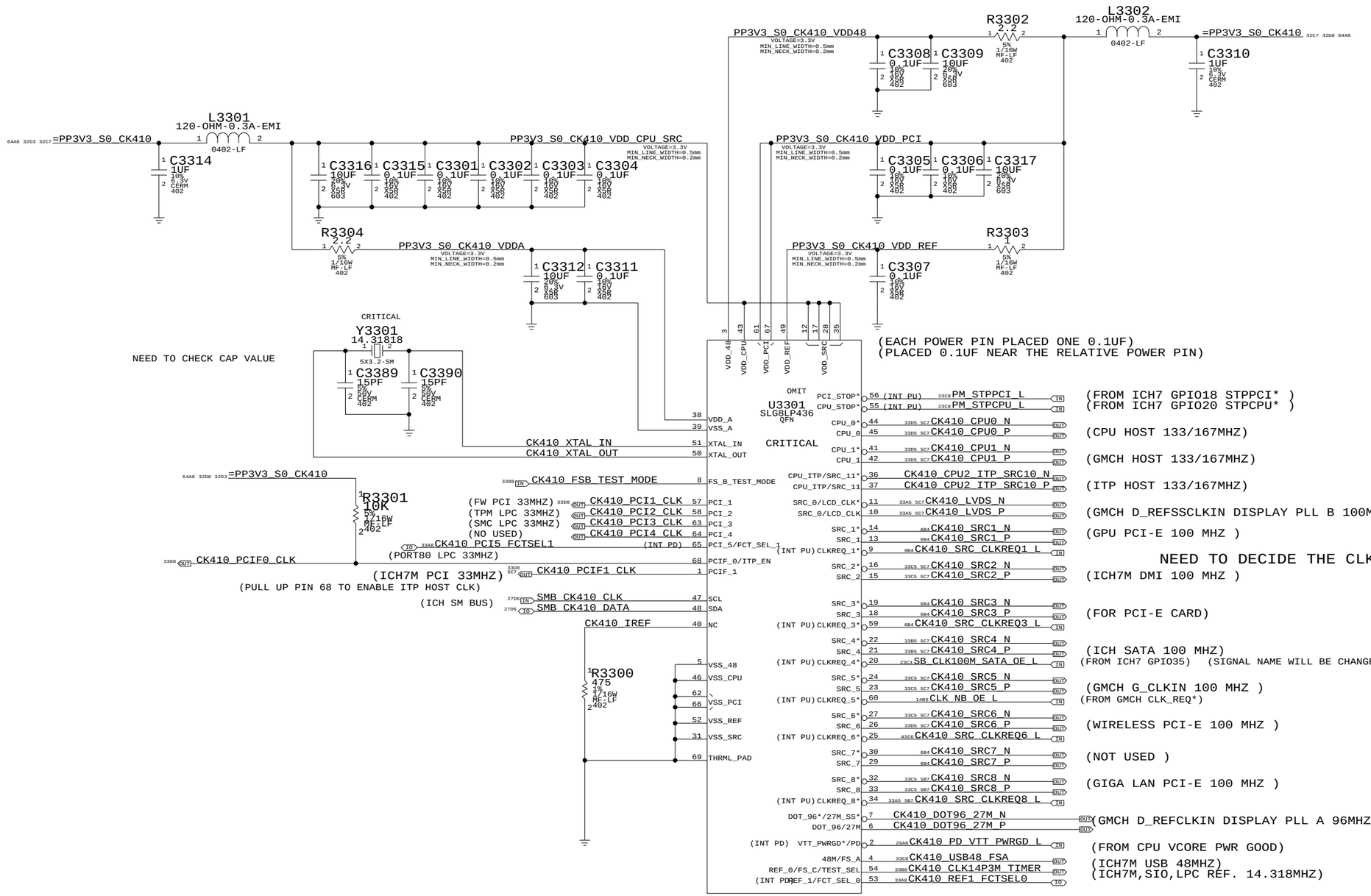
Memory Vtt Supply

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C

SCALE: NONE SHT 31 OF 98



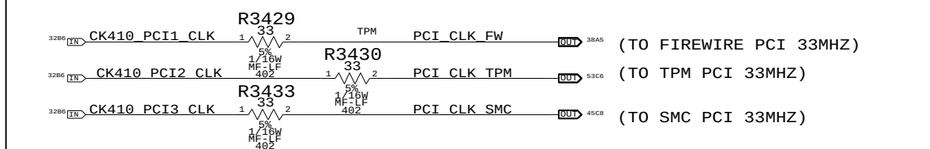
FCTSEL1	FCTSEL0	PIN 6	PIN 7	PIN 10	PIN 11	
0	0	DOT96T	DOT96C	100MT_SST	100MC_SST	* FOR INT. GRAPHIC SYSTEM
0	1	DOT96T	DOT96C	SRCT0	SRCC0	
1	0	27M NON SPREAD	27M SPREAD	SRCT0	SRCC0	* FOR EXT. GRAPHIC SYSTEM
1	1	OFF LOW	TBD	SRCT0	SRCC0	

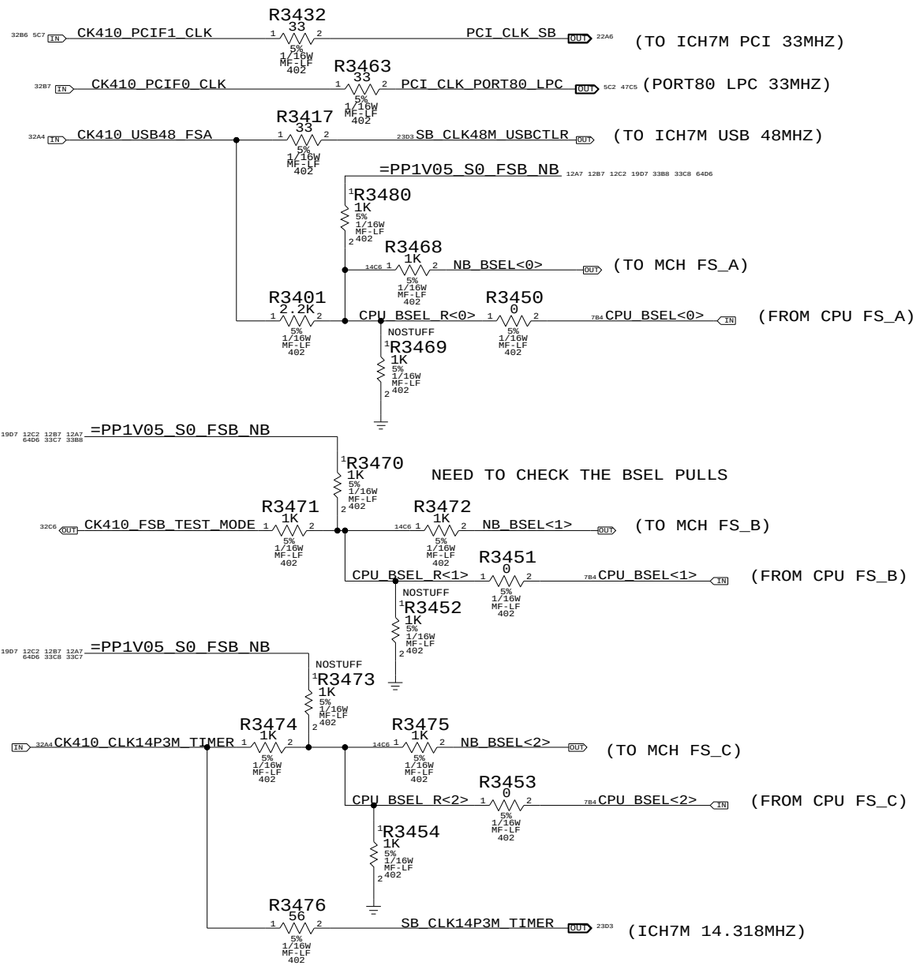
CLOCKS

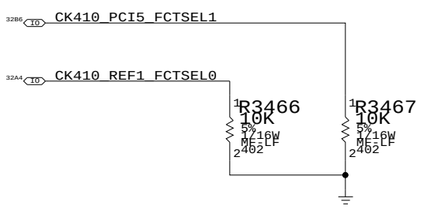
SYNC_MASTER=CLOCK SYNC_DATE=06/03/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 33 OF 98	





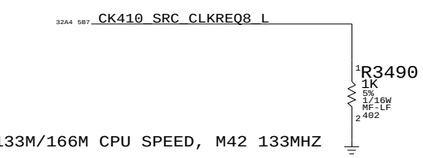


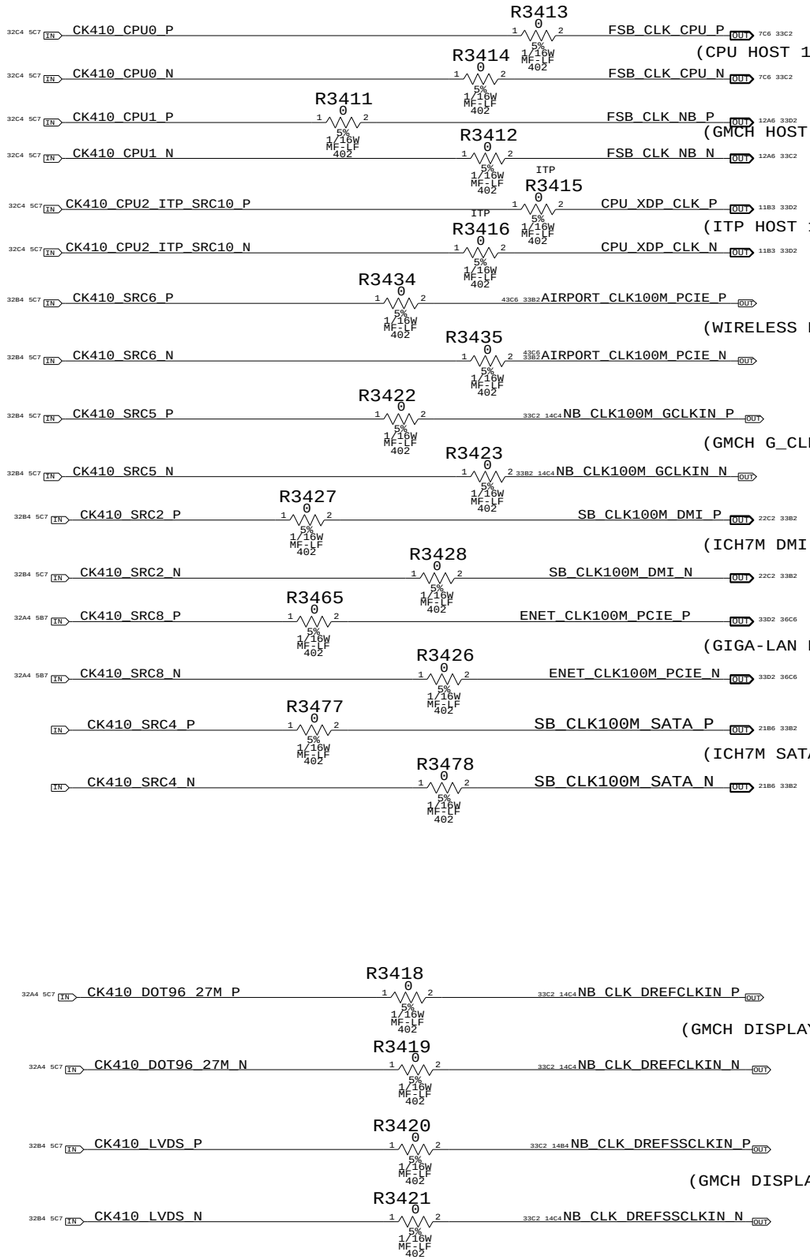
SET FCTSEL0,FCTSEL1 TO 00
EVEN THESE TWO PINS INTERNAL PULL DOWN,
CYPRESS RECOMMAND TO ADD EXTERNAL PULLS,

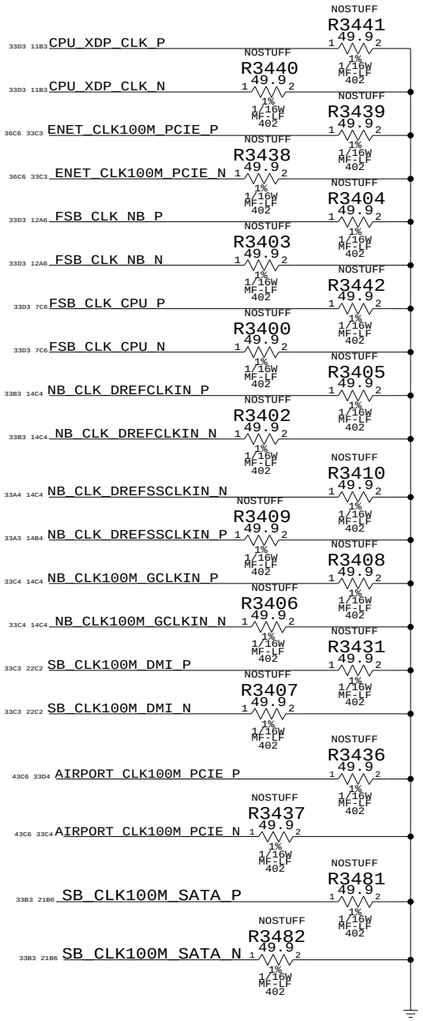
NOSTUFF R3450,R3451,R3453 FOR MANUAL CPU FREQUENCY

	FS_C	FS_B	FS_A	CPU
	1	0	1	100M
	0	0	1	133M
#	0	1	1	166M
	0	1	0	200M

NAPA PLATFORM ONLY SUPPORT 133M/166M CPU SPEED, M42 133MHZ







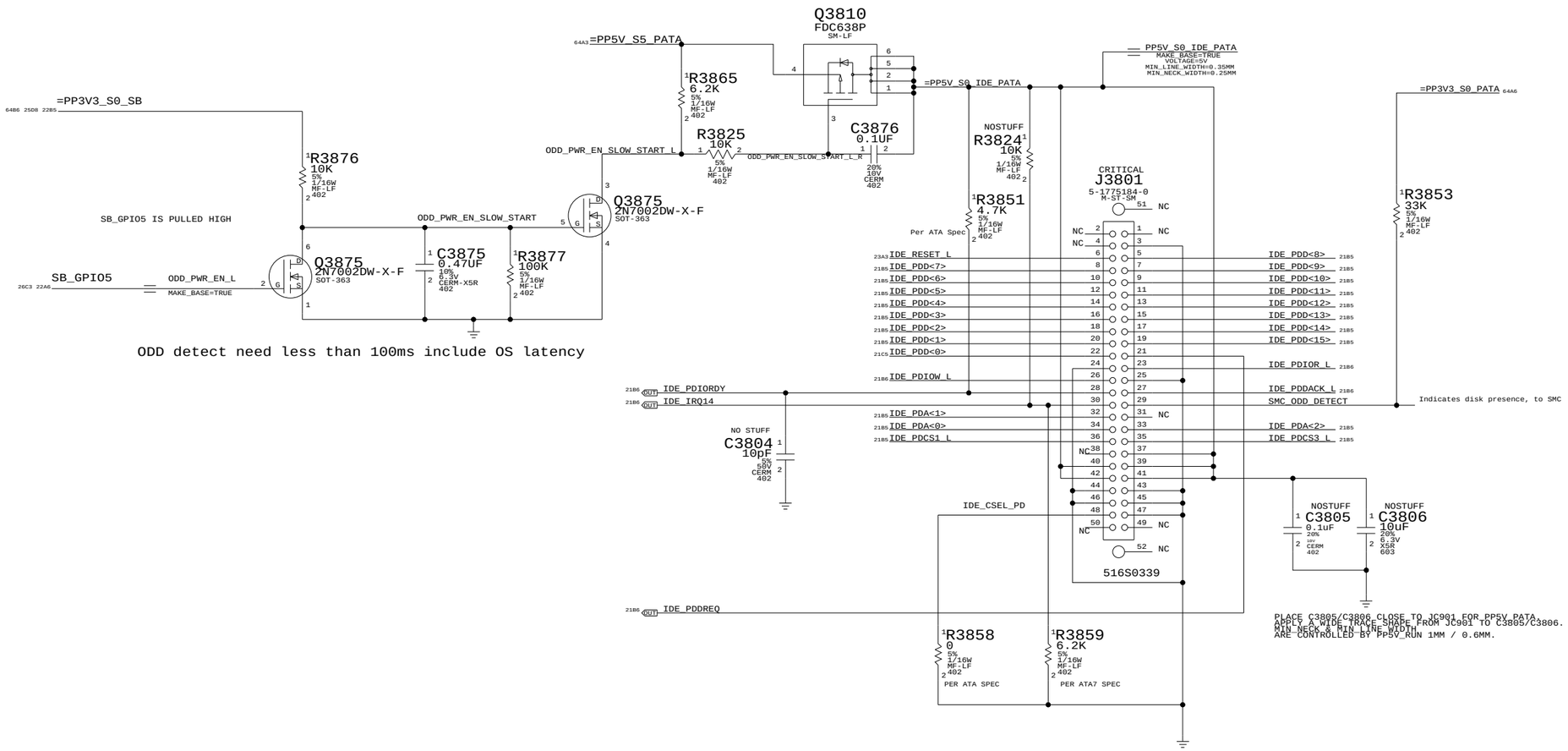
CLOCK TERMINATION

SYNC_MASTER=CLOCK SYNC_DATE=06/06/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C

SCALE: NONE SHT 34 OF 98



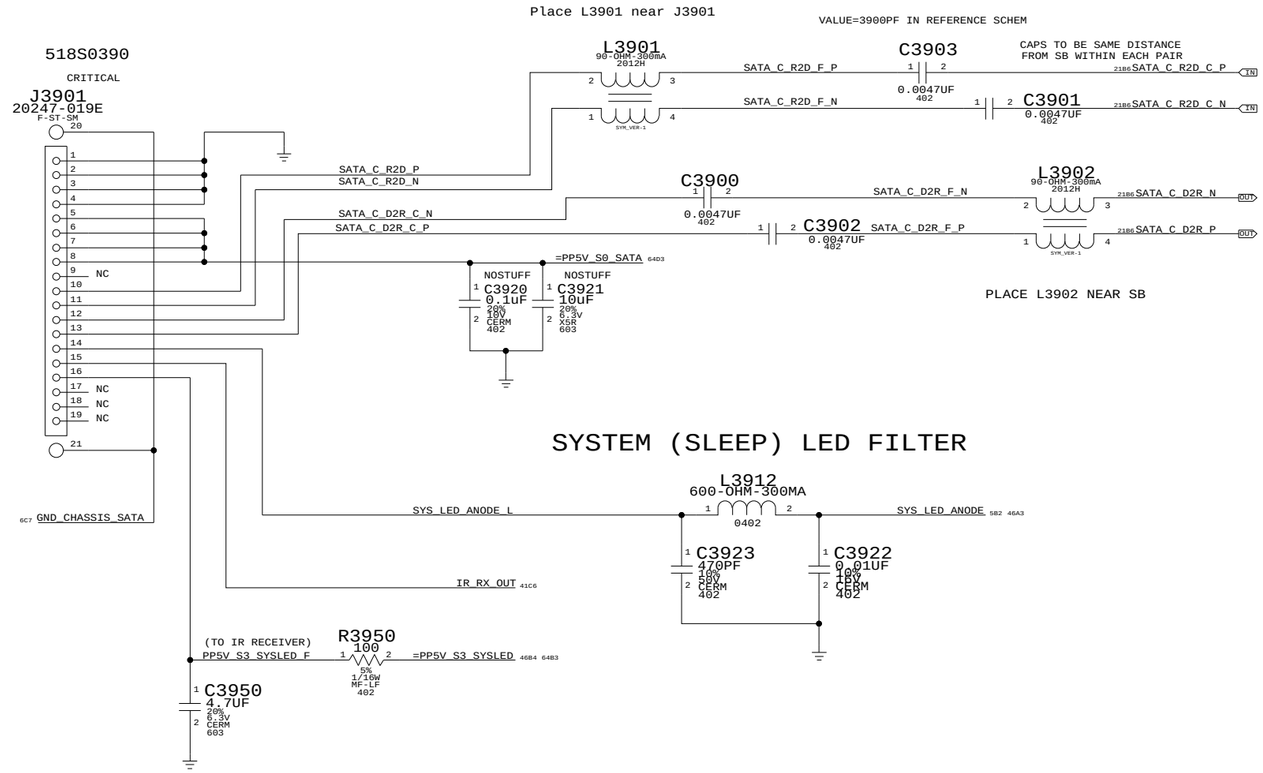
ODD detect need less than 100ms include OS latency

PATA CONNECTOR

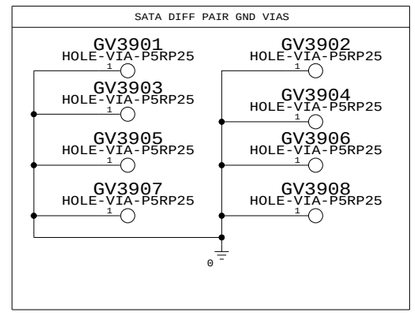
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 38 OF 98	

SATA CONNECTOR



SYSTEM (SLEEP) LED FILTER



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0227	155S0164	?	L3901,L3902	KEEP MAG.LAYER IN BOM

SATA CONNECTOR

NOTICE OF PROPRIETARY PROPERTY

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 39 OF 98	

PLACE C4100-C4106 NEAR PINS AVDLL0-AVDLL6.
SCHEME MATCHES DOC MVL100258-01

MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.22MM
VOLTAGE=2.5V

37D8 =PP2V5_S3_ENET

C4100 1UF 10% 6.3V CERM 402
C4101 0.1UF 10% 16V X5R 402
C4102 0.1UF 10% 16V X5R 402
C4103 0.1UF 10% 16V X5R 402
C4104 0.1UF 10% 16V X5R 402
C4105 0.001UF 10% 50V CERM 402
C4106 0.001UF 10% 50V CERM 402
C4107 0.1UF 10% 16V X5R 402

L4100 FERR-120-OHM-1.5A 0402-LF

=PP2V5_S3_ENET 64C3

PLACE C4107 NEAR U4101 AVDD

36C8 36B5 36B4 36A5 64B3 36D6 =PP3V3_S3_ENET

R4101 4.7K 5% 1/16W MF-LF 402

=PP1V2_S3_ENET 36A8 64C3

=PP3V3_S3_ENET 36D8 64B3 36A5 36B4 36B5 36C8

NOSTUFF
R4107 0 5% 1/16W MF-LF 402

22C4 22D8 SB_GPIO30

ENET_LOM_DIS_L

PLACE C4110 AND C4111 WITHIN
12 MIL OF U4101 PIN 49 AND 50

C4110 0.1UF 10% 16V X5R 402

PCIE_A_D2R_C_P 1 2 22D4 PCIE_A_D2R_P OUT
PCIE_A_D2R_C_N 1 2 22D4 PCIE_A_D2R_N OUT

C4111 0.1UF 10% 16V X5R 402

C4112 0.1UF X5R 10% 16V 402

PCIE_A_R2D_P
PCIE_A_R2D_N

PCIE_A_R2D_C_P 1 2 22D4 PCIE_A_R2D_C_P IN
PCIE_A_R2D_C_N 1 2 22D4 PCIE_A_R2D_C_N IN

C4113 0.1UF 402 X5R 16V 10%

PLACE C4113 AND C4112 WITHIN
12 MIL OF U2100 E27 AND E28

36B5 36B4 36A5 36D6 =PP3V3_S3_ENET
64A6 =PP3V3_S0_ENET

OMIT
CRITICAL
U4101
88E8053
QFN

		10	LOM_DISABLE*	
		12	VAUX_AVLBL	
		47	VMAIN_AVLBL	
	NC	11	SWITCH_VCC	
	NC	9	SWITCH_VAUX	
	NC	24	HSDACP	ANALOG
	NC	25	HSDACN	
OPTIONAL EXTERNAL LDO	OUT 6A4 ENET_CTRL25	4	CTRL25	
	OUT 6A4 ENET_CTRL12	3	CTRL12	
	ENET_RSET	16	RSET	
NO PULL-UP NEEDED	NC	59	LED_ACT*	LED
	NC	60	LED_LINK10/100*	
	NC	62	LED_LINK1000*	
	NC	63	LINK*	
		29	TSTPT	TEST
		46	TESTMODE	

R4102 4.75K 1% 1/16W MF-LF 402

PCI EXPRESS	TX_P	49	
	TX_N	50	
	RX_P	54	
	RX_N	53	
	REFCLKP	55	33D2 33C3 ENET_CLK100M_PCIE_P IN
	REFCLKN	56	33D2 33C3 ENET_CLK100M_PCIE_N IN
	WAKE*	6	43C6 23C8 PCIE_WAKE_L OUT
	PERST*	5	26A1 ENET_RST_L IN
MEDIA	MDIP0	17	ENET_MDI_P<0> IO
	MDIN0	18	ENET_MDI_N<0> IO
	MDIP1	20	ENET_MDI_P<1> IO
	MDIN1	21	ENET_MDI_N<1> IO
	MDIP2	26	ENET_MDI_P<2> IO
	MDIN2	27	ENET_MDI_N<2> IO
	MDIP3	30	ENET_MDI_P<3> IO
	MDIN3	31	ENET_MDI_N<3> IO
TWSI	VPD_CLK	38	ENET_VPD_CLK 36A2
	VPD_DATA	41	ENET_VPD_DATA 36A2
TEST	PU_VDDO_TTL0	42	ENET_PU_VDD_TTL0 36A6
	PU_VDDO_TTL1	43	ENET_PU_VDD_TTL1 36A6
SPI	SPI_DI	35	NC
	SPI_DO	34	NC
	SPI_CLK	37	NC
	SPI_CS	36	NC
MAIN CLK	XTALI	15	ENET_XTALI
	XTALO	14	ENET_XTALO

ASF IS UNAVAILABLE ON 80S3

INTERNAL PULL-UP

CRITICAL

Y4101 25.0000M SM-3.2X2.5MM

C4150 15PF 5% 50V CERM 402
C4151 15PF 5% 50V CERM 402

1. KEEP ENET_XTALI AND ENET_XTALO TRACE LENGTH <12MIL
2. DO NOT ROUTE UNDER CRYSTAL

THRML_PAD

R4106 49.9 1% 1/16W MF-LF 402 ENET_MDI0
R4105 49.9 1% 1/16W MF-LF 402
R4104 49.9 1% 1/16W MF-LF 402 ENET_MDI1
R4103 49.9 1% 1/16W MF-LF 402
R4120 49.9 1% 1/16W MF-LF 402 ENET_MDI2
R4119 49.9 1% 1/16W MF-LF 402
R4118 49.9 1% 1/16W MF-LF 402 ENET_MDI3
R4117 49.9 1% 1/16W MF-LF 402

C4116 0.001UF 10% 50V CERM 402
C4115 0.001UF 10% 50V CERM 402
C4117 0.001UF 10% 50V CERM 402
C4118 0.001UF 10% 50V CERM 402

PLACE RESISTORS CLOSE TO U4101

=PP3V3_S3_ENET 36A5 36B4 36C8 36D6 36D8 64B3

R4130 4.7K 5% 1/16W MF-LF 402
R4131 4.7K 5% 1/16W MF-LF 402

36C6 ENET_PU_VDD_TTL0
36B6 ENET_PU_VDD_TTL1

64B3 36D8 36D6 36C8 36B5 36A5 =PP3V3_S3_ENET

PLACE C4140 NEAR U4102 VCC

C4140 0.1UF 10% 16V X5R 402

OMIT
CRITICAL
U4102
M24C08
SO8

3	E2	
2	NC1	
1	NC0	
7	WC*	
8	VCC	
5	SDA	ENET_VPD_DATA 36C6
6	SCL	ENET_VPD_CLK 36C6
4	VSS	

R4122 4.7K 5% 1/16W MF-LF 402
R4123 4.7K 5% 1/16W MF-LF 402

NOSTUFF
R4124 0 5% 1/16W MF-LF 402

PLACE C4127-C4134 NEAR PINS VDD0-VDD7 ON U4101
SCHEME MATCHES DOC MVL100258-01

64C3 36D7 =PP1V2_S3_ENET

C4126 0.1UF 10% 16V X5R 402
C4127 0.1UF 10% 16V X5R 402
C4128 0.1UF 10% 16V X5R 402
C4129 0.1UF 10% 16V X5R 402
C4130 0.1UF 10% 16V X5R 402
C4131 0.001UF 10% 50V CERM 402
C4132 0.001UF 10% 50V CERM 402
C4133 0.001UF 10% 50V CERM 402
C4134 0.001UF 10% 50V CERM 402

PLACE C4135-C4139 NEAR VDDO_TTL0-VDD_TTL4 ON U4101
SCHEME MATCHES DOC MVL100258-01

64B3 36D8 36D6 36C8 36B5 36B4 =PP3V3_S3_ENET

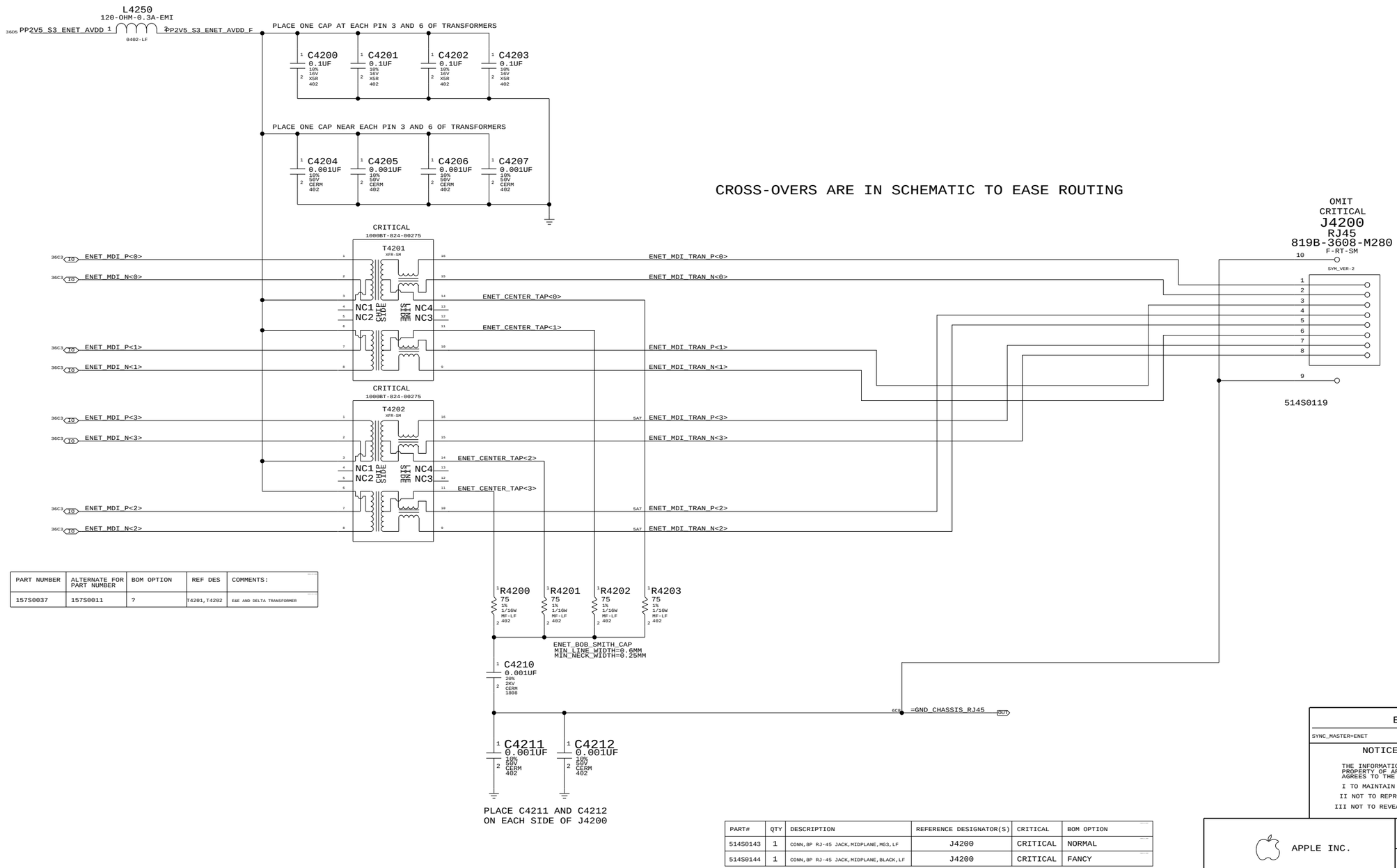
C4135 0.1UF 10% 16V X5R 402
C4136 0.1UF 10% 16V X5R 402
C4137 0.1UF 10% 16V X5R 402
C4138 0.001UF 10% 50V CERM 402
C4139 0.001UF 10% 50V CERM 402

ETHERNET CONTROLLER

SYNC_MASTER=ENET
SYNC_DATE=12/06/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 41 OF 98	



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
157S0037	157S0011	?	T4201,T4202	E&E AND DELTA TRANSFORMER

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514S0143	1	CONN,8P RJ-45 JACK,MIDPLANE,MG3,LF	J4200	CRITICAL	NORMAL
514S0144	1	CONN,8P RJ-45 JACK,MIDPLANE,BLACK,LF	J4200	CRITICAL	FANCY

ETHERNET CONNECTOR

SYNC_MASTER=ENET SYNC_DATE=11/14/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 42 OF 98	

PAGE NOTES

INPUT

=PP3V3_S0_FW - 3.3V POWER FOR FIREWIRE (MOBILE: OFF DURING SLEEP)
=PP3V3_S0_PCI - 3.3V POWER FOR PCI FIREWIRE (MOBILE: OFF DURING SLEEP)
PCI_GNT3_L - PCI GRANT FROM SB
PCI_CLK_FW - NEED TO REFERENCE TO ALIAS PAGE
PCI_RST_L - PCI RESET FROM SB
FW_PC0 - FIREWIRE POWER CLASS IDENTIFIER

INPUT/OUTPUT

PCI_AD<0..31>,PCI_C_BE_L<0..3>,PCI_FRAME_L,PCI_IRDY_L,PCI_TRDY_L,
PCI_DEVSEL_L, PCI_STOP_L, PCI_PAR, PCI_PERR_L, PCI_SERR_L
FW_A_TPA_P/N, FW_A_TPB_P/N, FW_A_TPBIAS - PORT 0 FIREWIRE DIFF PAIRS
FW_B_TPA_P/N, FW_B_TPB_P/N, FW_B_TPBIAS - PORT 1 FIREWIRE DIFF PAIRS
FW_C_TPA_P/N, FW_C_TPB_P/N, FW_C_TPBIAS - PORT 2 FIREWIRE DIFF PAIRS

OUTPUT

PCI_REQ3_L - PCI REQUEST TO SB
PM_CLKRUN_L - CLOCK-RUN PCI PROTOCOL
INT_PIRQD_L - INTERRUPT TO SB
PCI_PME_FW_L - DEDICATED PME FOR FIREWIRE (SB GPIO1)

PAGE HISTORY

5/19/2005 - FIRST REVISION OF PAGE
6/20/2005 - BGA VERSION OF FW323-06 ADDED
6/21/2005 - CHANGED INT* TO INT_PIRQD_L (PER ARCHITECTURAL DEFINITION)
6/21/2005 - CHANGED PCI_ID TO AD19 (PER ARCHITECTURAL DEFINITION)
6/21/2005 - CHANGED REQ/GNT TO REQ3/GNT3 (PER ARCHITECTURAL DEFINITION)
6/22/2005 - ADDED 510R PULL-DOWN ON RST* AND REMOVED CONNECTION TO PLT_RST_L
6/22/2005 - CHANGED CLK_PME_DIFF_PAIR NAMES TO BE RE-USE COMPLIANT
6/22/2005 - REMOVED CONSTRAINT SETS AS THEY WILL BE MANAGED ON BOARD SIDE
6/22/2005 - REMOVED C4421 - REDUNDANT
6/22/2005 - BRING OUT PCB CONNECTION TO BE CONNECTED ON PORT PAGE
7/26/2005 - CONNECTED PIN E10 TO GND

MOBILE TURNS OFF CONTROLLER POWER DURING SLEEP
0.001A DURING SLEEP

64B3 =PP3V3_S3_FW

PLACE ONE CAP PER TWO PINS STARTING WITH C4424 ON VDD0

C4424 10UF 20% 6.3V X5R 603
C4418 0.1UF 10% 10V X5R 402
C4422 0.1UF 10% 10V CERM 402
C4426 0.1UF 10% 10V CERM 402
C4428 0.1UF 10% 10V CERM 402
C4430 0.1UF 10% 10V CERM 402
C4432 0.1UF 10% 10V CERM 402

L4400 600-OHM-300MA 0402

PLACE ONE CAP PER TWO PINS STARTING WITH C4416 ON VDDA0

PP3V3_S3_FW_AVDD
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM

C4416 10UF 20% 6.3V X5R 603
C4417 0.1UF 10% 10V X5R 402
C4429 0.1UF 10% 10V X5R 402
C4425 0.1UF 10% 10V X5R 402

64B3 =PP3V3_S3_PCI

VDD0 G4, VDD1 M1, VDD2 M2, VDD3 K5, VDD4 K7, VDD5 L13, VDD6 H13, VDD7 H1, VDD9 A2
VDDA0 D10, VDDA1 A13, VDDA2 B13, VDDA3 A7, VDDA4 A8, VDDA5 D6

CONNECT TO VDD FOR 3.3V OPERATION

PCI_VIOS G13

PCI_AD<0> F10 PCI_AD0
PCI_AD<1> G10 PCI_AD1
PCI_AD<2> H10 PCI_AD2
PCI_AD<3> H12 PCI_AD3
PCI_AD<4> J13 PCI_AD4
PCI_AD<5> J12 PCI_AD5
PCI_AD<6> K13 PCI_AD6
PCI_AD<7> K10 PCI_AD7
PCI_AD<8> L12 PCI_AD8
PCI_AD<9> M13 PCI_AD9
PCI_AD<10> L11 PCI_AD10
PCI_AD<11> M12 PCI_AD11
PCI_AD<12> M11 PCI_AD12
PCI_AD<13> N12 PCI_AD13
PCI_AD<14> M10 PCI_AD14
PCI_AD<15> N11 PCI_AD15
PCI_AD<16> M4 PCI_AD16
PCI_AD<17> N5 PCI_AD17
PCI_AD<18> N4 PCI_AD18
PCI_AD<19> M3 PCI_AD19
PCI_AD<20> M2 PCI_AD20
PCI_AD<21> N3 PCI_AD21
PCI_AD<22> K4 PCI_AD22
PCI_AD<23> M1 PCI_AD23
PCI_AD<24> K2 PCI_AD24
PCI_AD<25> J4 PCI_AD25
PCI_AD<26> K1 PCI_AD26
PCI_AD<27> J2 PCI_AD27
PCI_AD<28> J1 PCI_AD28
PCI_AD<29> H2 PCI_AD29
PCI_AD<30> H4 PCI_AD30
PCI_AD<31> H1 PCI_AD31

PCI_C_BE_L<0> K12 PCI_CBE0*
PCI_C_BE_L<1> M9 PCI_CBE1*
PCI_C_BE_L<2> L3 PCI_CBE2*
PCI_C_BE_L<3> L1 PCI_CBE3*

PCI_PAR N10 PCI_PAR
PCI_FRAME_L N6 PCI_FRAME*
PCI_IRDY_L M6 PCI_IRDY*
PCI_TRDY_L N7 PCI_TRDY*
PCI_DEVSEL_L N8 PCI_DEVSEL*
PCI_STOP_L M7 PCI_STOP*
FW_PCI_IDSEL L2 PCI_IDSEL

PCI_REQ3_L E2 PCI_REQ*
PCI_GNT3_L E1 PCI_GNT*
PCI_PERR_L M8 PCI_PERR*
PCI_SERR_L N9 PCI_SERR*

PCI_CLK_FW G2 PCI_CLK
PM_CLKRUN_L D1 CLKRUN*
FW_PCI_RST_L F1 PCI_RST*
INT_PIRQD_L D2 PCI_INTA*
PCI_PME_FW_L F2 PCI_PME*

R4431 22 5% 1/16W MF-LF 402

R4432 100 1% 1/16W MF-LF 402

THIS IS FROM ICH-7M

PLACE R4432 VERY CLOSE TO PIN B18 OF U2100

OMIT
CRITICAL
U4400
FW32306
BGA

XI A5 FW_XI
XO B5 FW_XO
RESET* B4 FW_PWRON_RST_L
R1 A6 FW_R1
R0 B7 FW_R0

197S0030 3.2MMX2.5MM
CRITICAL
Y4403
SM-3.2X2.5MM
24.576MHZ

R4400 390 5% 1/16W MF-LF 402
C4411 15PF 5% 50V CERM 402
C4412 15PF 5% 50V CERM 402

NEED TO CHECK CRYSTAL LOAD CAPACITANCE

R4452 2.1K 1% 1/16W MF-LF 402
C4420 0.1UF 10% 10V X5R 402
R4420 510K 5% 1/10W MF-LF 402

SPEC RECOMMENDS 2.49K

TPBIAS0 B8 39B4 FW_A_TPBIAS
TPA0_P A9 39B4 FW_A_TPA_P
TPA0_N B9 39B4 FW_A_TPA_N
TPB0_P B10 39B4 FW_A_TPB_P
TPB0_N A10 39B4 FW_A_TPB_N
TPBIAS1 D8 6D2 FW_B_TPBIAS
TPA1_P A11 6D2 FW_B_TPA_P
TPA1_N B11 6D2 FW_B_TPA_N
TPB1_P B12 6D2 FW_B_TPB_P
TPB1_N A12 6D2 FW_B_TPB_N
TPBIAS2 C13 6D2 FW_C_TPBIAS
TPA2_P C11 6D2 FW_C_TPA_P
TPA2_N C12 6D2 FW_C_TPA_N
TPB2_P D13 6D2 FW_C_TPB_P
TPB2_N D12 6D2 FW_C_TPB_N

MODE_420 M5
MODE_A B6
MODE FOR EXTERNAL LINK

PC0 E12 39C8 FW_PC0
PC1 F13
PC2 F12
CONTENDER G12 LOW = NOT BUS MANAGER
CARDBUSN B1 LOW = PCI OPERATION
MPCI_ACTN_323 E10

DUAL PORT DEVICES ARE POWER CLASS 4 (’100’)
SINGLE PORT DEVICES ARE POWER CLASS 0 (’000’)

TEST0 C2
TEST1 C1
PTEST A4
SE A3
SM B3
MANUFACTURING TEST PINS

VSS0 A1, VSS1 B2, VSS2 C3, VSS3 D4, VSS4 E4, VSS5 E5, VSS6 F4, VSS7 F6, VSS8 F7, VSS9 F8, VSS10 G1, VSS11 G6, VSS12 G7, VSS13 G8, VSS14 H6, VSS15 H7, VSS16 H8, VSS17 J5, VSS18 J9, VSS19 J10, VSS20 K8, VSS21 K9, VSS22 N13
VSSA0 E13, VSSA1 E9, VSSA2 D9, VSSA3 D7, VSSA4 D5

FIREWIRE CONTROLLER

SYNC_MASTER=ENET SYNC_DATE=08/30/2005

NOTICE OF PROPRIETARY PROPERTY

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 44 OF 98	

Page Notes

INPUT:

=PPBUS_FW - PORT POWER

=PP3V3_S5_FW - DIGITAL POWER

=GND_CHASSIS_FW_PORT0 - CHASSIS GROUND

=FWPWR_PWRON - ADDITIONAL POWER CONTROL

INPUT/OUTPUT:

FW_TPA0_P/N,FW_TPB0_P/N,FW_TPBIAS0 - FIREWIRE DIFF PAIRS

OUTPUT:

FW_PC0 - POWER CLASS IDENTIFIER (SINGLE PORT - TIE LOW)

PAGE HISTORY

5/19/05 - INITIAL REVISION
6/22/05 - CHANGED DIFF PAIR NAMES TO MATCH REUSE
6/22/05 - REMOVED CONSTRAINTS BECAUSE USING ALLEGRO CONST MANAGER
6/22/05 - CONNECTED FW_PC0 FOR SINGLE PORT
7/26/05 - UPDATED LATE-VG POWER RAIL CIRCUIT FROM M1
7/26/05 - CHANGED CONNECTOR PORT NAMING TO PORT0
7/26/05 - SWITCHED TO 514-0124 FOR PRE-PROTO CONNECTOR
7/26/05 - REMOVED R4520 - IT HASN'T BEEN STUFFED FOR MANY PRODUCTS
7/26/05 - CHANGED FL4590 TO 1.1A VERSION
7/26/05 - REMOVED ETHERNET LOW-POWER MODE CIRCUIT
7/26/05 - UPDATED SIGNAL NAMES FOR FW PORT POWER ENABLE

1394b implementation based on Apple
FireWire Design Guide (FWDG 0.6, 5/14/03)

PORT POWER CLASS

0 FOR SINGLE PORT
1 FOR DUAL PORT

38A3 OUT FW_PC0

IF =FWPWR_PWRON IS NC:
ENABLES PORT POWER WHEN MACHINE IS RUNNING OR ON AC
IF =FWPWR_PWRON LOW WHEN OFF:
ENABLES PORT POWER WHEN MACHINE IS RUNNING OR ON AC AND NOT SHUTDOWN

PPBUS_S5_FWPWRSW_F
VOLTAGE=18.5V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM

64C1 =PPBUS_S5_FWPWRSW
FL4590
1.1A-24V
MINISMDC

Q4590
FDC638P
SM-LF

PPFW_SWITCH 58Z
VOLTAGE=18V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM

D4590
SMB
B340LBXF

64A6 =PP3V3_S0_FW
R4590 470K 5% 1/16W MF-LF 402
C4590 0.01uF 10% 16V CERM 402
FWPWR_EN_L_DIV
MIN_LINE_WIDTH=0.05MM
MIN_NECK_WIDTH=0.05MM
R4593 100K 5% 1/16W MF-LF 402
R4591 330K 5% 1/16W MF-LF 402
D4591 BAS16TW-X-F SOT-363
FWPWR_RUN
FWPWR_EN_L 60C8
MIN_LINE_WIDTH=0.05MM
MIN_NECK_WIDTH=0.05MM
6D2 =FWPWR_PWRON
Q4591 2N7002 SOT23-LF
FWPWR_EN
R4594 10K 5% 1/16W MF-LF 402
65C3 46B3 45D5 5C1 SMC_PS_ON
FWPWR_ACIN
R4595 470K 5% 1/16W MF-LF 402

Enables port power whenever
machine AC Adapter is plugged
or system at run state with battery only

Cable Power

PPFW_PORT0_VP_F
VOLTAGE=16.5V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
L4510 FERR-250-OHM SM
PPFW_PORT0_VP
VOLTAGE=16.5V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
C4510 0.001uF 10% 50V CERM 402

"Snapback" & "Late VG" Protection

[LATE VG NOTES]
CURRENT THROUGH THE BIAS RESISTOR SHOULD BE 5MA FOR A VOLTAGE DROP TO 2.2V
IT IS 2.2V INSTEAD OF 2.7V BECAUSE THE SNAPBACK ESD DIODES HAVE A 0.5V DROP

39A6 PP3V3_S5_FWLATEVG
C4520 0.01UF 10% 16V CERM 402
D4520 BAV99DW-X-F SOT-363
C4521 0.01UF 10% 16V CERM 402
D4520 BAV99DW-X-F SOT-363

3883 FW_A_TPBIAS
R4500 56.2 1% 1/16W MF-LF 402
R4501 56.2 1% 1/16W MF-LF 402
C4500 0.33UF 10% 6.3V CERM-X5R 402

3883 FW_A_TPA_P
3883 FW_A_TPA_N
3883 FW_A_TPB_P
3883 FW_A_TPB_N

FW_PORT0_TPA_P
FW_PORT0_TPA_N
FW_PORT0_TPB_P
FW_PORT0_TPB_N

120-OHM 2012 SYM_VER-2
FL4520
120-OHM 2012 SYM_VER-2
FL4521

FW_PORT0_TPA_P_FL
FW_PORT0_TPA_N_FL
FW_PORT0_TPB_P_FL
FW_PORT0_TPB_N_FL
(PPFW_PORT0_VP)
(GND_FW_PORT0_VGND)

PORT 0
1394A
OMIT
CRITICAL
J4500
1394A
F-RT-TH1

TPO (TPA+)
TPO# (TPA-)
TPI (TPB+)
TPI# (TPB-)
VP
VGND
=GND_CHASSIS_FW_UPPER 6A6
Plexi: 514-0124
Enclosure: 514-0289
=GND_CHASSIS_FW_DOWN 6C8

R4502 56.2 1% 1/16W MF-LF 402
R4503 56.2 1% 1/16W MF-LF 402
FW_PORT0_TPB
C4501 220PF 5% 25V CERM 402
R4504 4.99K 1% 1/16W MF-LF 402

D4521 BAV99DW-X-F SOT-363
C4522 0.01UF 10% 16V CERM 402
D4521 BAV99DW-X-F SOT-363
C4523 0.01UF 10% 16V CERM 402

C4524 0.01uF 10% 50V X7R 603-1
C4525 0.01uF 10% 16V CERM 402

LATE-VG PROTECTION POWER

64A3 =PP3V3_S5_FWLATEVG
R4550 330 5% 1/16W MF-LF 402
PP3V3_S5_FWLATEVG_F
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.35MM
MIN_NECK_WIDTH=0.25MM
L4550 400-OHM-EMI SM-1
NO STUFF C4551 0.1uF 20% 16V CERM 402
NO STUFF C4552 0.001uF 10% 50V CERM 402
D4550 SOT23 MMBZ5227B
PP3V3_S5_FWLATEVG
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.35MM
MIN_NECK_WIDTH=0.25MM
39B5

CAPS MAY NOT BE NECESSARY.
NO STUFF FOR NOW THOUGH

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0359	1	CONN,6P 1394A RCPT,MIDPLANE,MG3,LF	J4500	CRITICAL	NORMAL
514-0316	1	CONN,6P 1394A RCPT,MIDPLANE,BLACK,LF	J4500	CRITICAL	FANCY

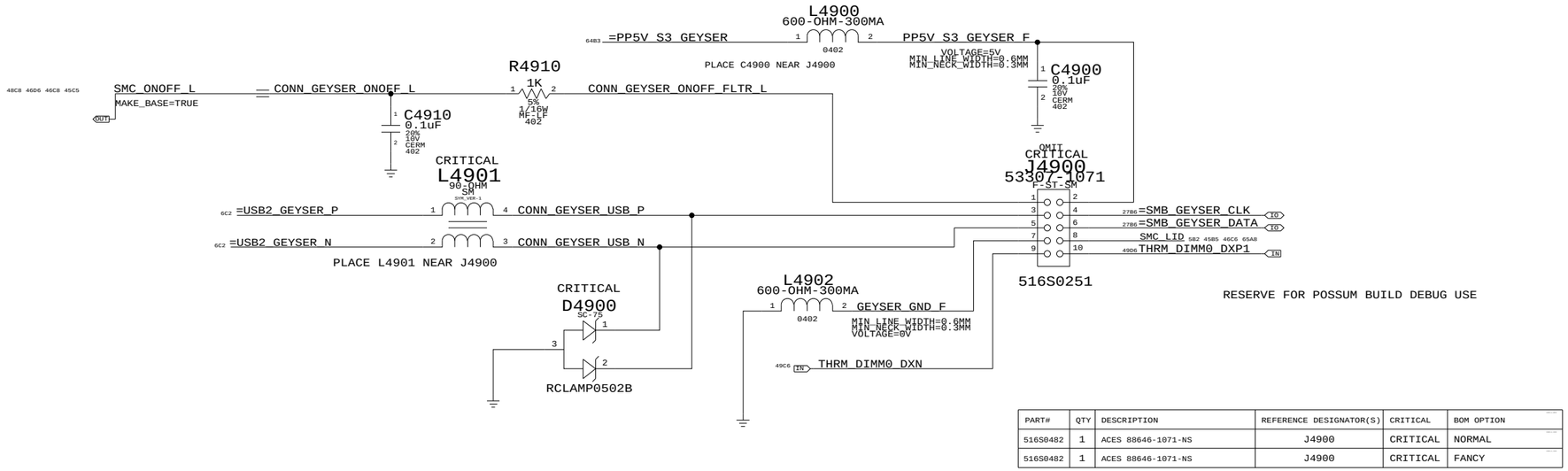
FIREWIRE PORT

SYNC_MASTER=ENET
SYNC_DATE=11/16/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 45 OF 98	

GEYSER AND DIMM0 REMOTE TEMP SENSORS



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
516S0482	1	ACES 88646-1071-NS	J4900	CRITICAL	NORMAL
516S0482	1	ACES 88646-1071-NS	J4900	CRITICAL	FANCY

CONNECTOR MISC

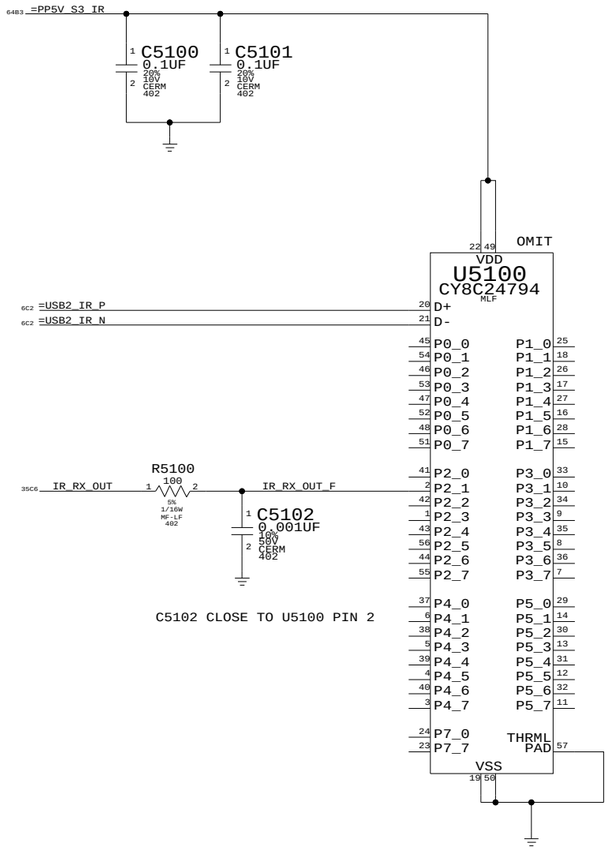
SYNC_MASTER=ENET SYNC_DATE=11/16/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C

SCALE	SHT	OF
NONE	49	98

PLACE C5100 AND C5101
NEAR U5100 PIN 22 AND 49



C5102 CLOSE TO U5100 PIN 2

IR CONTROLLER

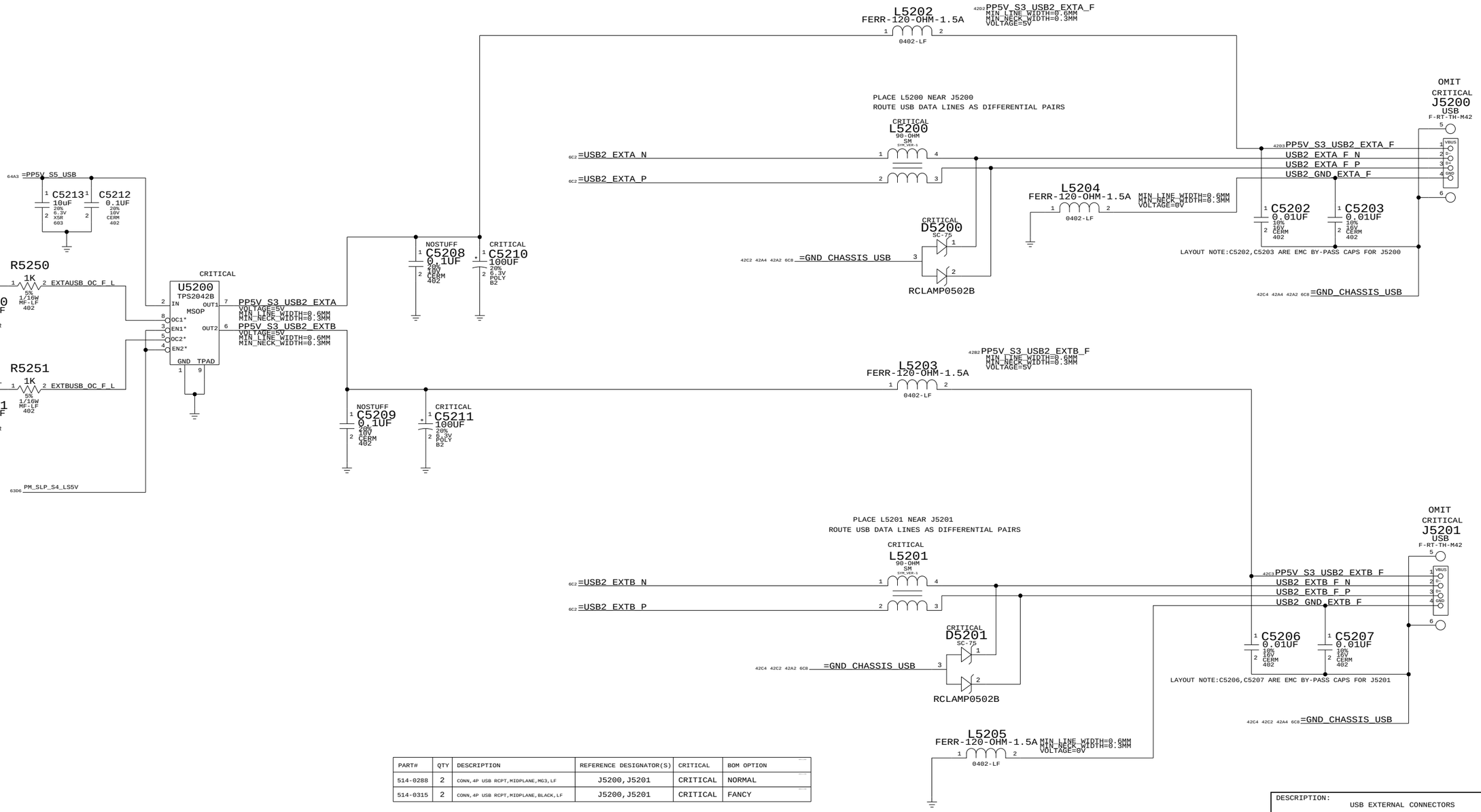
SYNC_MASTER=ENET SYNC_DATE=11/09/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C

SCALE	SHT	OF
NONE	51	98

USB 2.0 CONNECTORS

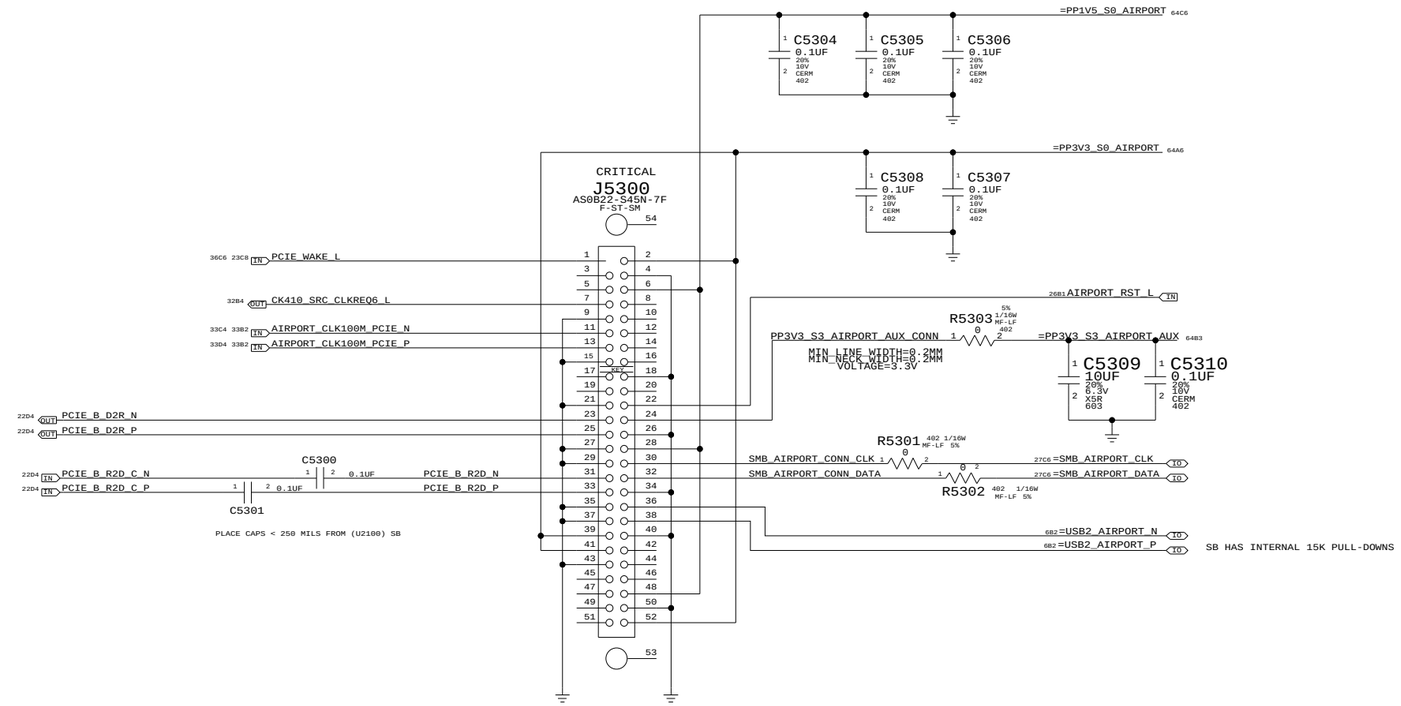


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0288	2	CONN,4P USB RCPT,MIDPLANE,MG3,LF	J5200,J5201	CRITICAL	NORMAL
514-0315	2	CONN,4P USB RCPT,MIDPLANE,BLACK,LF	J5200,J5201	CRITICAL	FANCY

DESCRIPTION:
USB EXTERNAL CONNECTORS

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 52 OF 98	



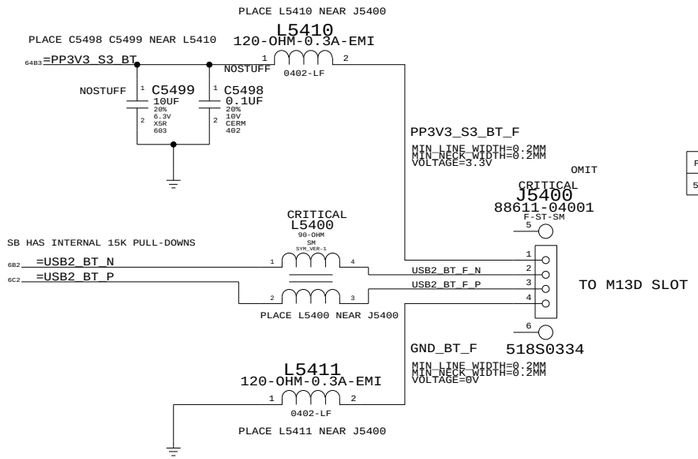
CONNECT TO M35 MODULE

Plexi: 516S0363
* Enclosure: 516S0406

AIRPORT CONN

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 53 OF 98	



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
518S0486	1	IMPROVED ACES CONNECTOR	J5400	CRITICAL	M42B

BLUETOOTH INTERFACE

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 54 OF 98	

OMIT

U5800
SMC_H8S2116
BGA
(1 OF 4)

23C3	PM_LAN_ENABLE	B12	P10	P60/KIN0*	L13	63C8	SMC_PM_G2_EN
26A3	SMC_RSTGATE_L	C13	P11	P61/KIN1*	L14	65C3 46B3 39C6 5C1	SMC_PS_ON (Enable AC adapter PWR)
63B1 26A5 5B2	ALL_SYS_PWRGD	A15	P12	P62/KIN2*	L15	22C6	SPI_ARB
59A1 46D6	RSMRST_PWRGD	B14	P13	P63/KIN3*	K12	50C7 22C6	SPI_SCLK
23C3	SMC_SB_NMI	B15	P14	P64/KIN4*	K13	50C1 22C6	SPI_SI
23C1	PM_RSMRST_L	C14	P15	P65/KIN5*	K14	50C1 22C6	SPI_SO
58C7	IMVP_VR_ON	D12	P16	P66/IRQ6*/KIN6*	J12	46C1	SMC_PROCHOT_3_3_L
23C3	PM_PWRBTN_L	C15	P17	P67/IRQ7*/KIN7*	J13	6B1	SMC_CPU_INIT_3_3_L
46C6	SMC_P20	D13	P20	P70/AN0	N12	48C1	SMC_CPU_ISENSE
46C6	SMC_P21	D14	P21	P71/AN1	R13	48B1 5B2	SMC_CPU_VSENSE
46C6	SMC_P22	D15	P22	P72/AN2	P13	46C6	SMC_GPU_ISENSE
46C6	SMC_P23	E12	P23	P73/AN3	R14	46C6	SMC_GPU_VSENSE
66A3 46B6 5C1	SMC_BATT_TRICKLE_EN_L	E14	P24	P74/AN4	P14	66C2	SMC_DCIN_ISENSE
66A4 46B6 5C1	SMC_BATT_CHG_EN	E15	P25	P75/AN5	R15	48C1	SMC_PBUS_VSENSE
46C6	SMC_P26	E13	P26	P76/AN6	N13	66B1	SMC_BATT_ISENSE
46C6	SMC_P27	F14	P27	P77/AN7	P15	46B1	SMC_FWIRE_ISENSE
53C6 47C6 21D4 5D2	LPC_AD<0>	D9	P30/LAD0	P80/PME*	C7	23C1	SMC_WAKE_SCI_L
53C6 47C6 21D4 5D2	LPC_AD<1>	C9	P31/LAD1	P81/GA20	A7	46B2	SMC_TPM_GPIO
53C6 47C5 21D4 5C2	LPC_AD<2>	A9	P32/LAD2	P82/CLKRUN*	B7	47C6 38A5 53C6 23C8 5C2	PM_CLKRUN_L
53C6 47C5 21D4 5C2	LPC_AD<3>	B9	P33/LAD3	P83/LPCPD*	D6	47C5 46D3 53C6 23C5 5C2	PM_SUS_STAT_L
53C6 47C6 21C5 5C2	LPC_FRAME_L	D8	P34/LFRAME*	P84/IRQ3*/TXD1	C6	46B1	SC_TX_L (Serial Port Transmit)
26B1	SMC_LRESET_L	C8	P35/LRESET*	P85/IRQ4*/RXD1	A6	46B1	SC_RX_L (Serial Port Receive)
33D6	PCI_CLK_SMC	A8	P36/LCLK	P86/IRQ5*/SCK1/SCL1	B6	27B3	SMB_BSB_CLK (BAT B SMBUS CLK)
53C6 47C5 23C8 5C2	INT_SERIRQ	D7	P37/SERIRQ	P90/IRQ2*	K4	48C8 46D6 46C8 40C8	SMC_ONOFF_L
	SMC_DISPLAY_ENABLE	A5	P40/TMI0	P91/IRQ1*	J2	65C7 65C3 46B6 5C1	SMC_BC_ACOK (AC I/P detect)
46A4	SMC_SYS_LED_16B	B5	P41/TMO0	P92/IRQ0*	J1	65A2 46C6 5D1	SMC_BS_ALRT_L
27B3	SMB_BSB_DATA (BAT B SMBUS DATA)	D5	P42/SDA1	P93/IRQ12*	J3	63B8 63A7 23C3	PM_SLP_S3_L
53C7	SMC_TPM_PP (TPM physical presence)	C3	P43/TMI1/EXSCK1	P94/IRQ13*	J4	63D6 61B8 60C8 23C3	PM_SLP_S4_L
46C6	SMC_P44	B1	P44/TMO1	P95/IRQ14*	H2	46D3 23C3	PM_SLP_S5_L
	SMC_BKLIGHT_ENABLE	C2	P45	P96/EXCL	H1	46A6	SMC_SUS_CLK
46C6	SMC_P46	D3	P46/PWX0/PWM0	P97/IRQ15*/SDA0	G2	27D6	SMB_0_DATA
46C6	SMC_SYS_KBDLED	C1	P47/PWX1/PWM1				
47B6 46D6 46B2 5C2	SMC_TX_L (Debug feature,16550 Transmit)	G1	P50				
47B5 46D6 46B2 5C2	SMC_RX_L (Debug feature,16550 Receive)	G4	P51				
27D6	SMB_0_CLK	F2	P52/SCL0				

OMIT

U5800
SMC_H8S2116
BGA
(2 OF 4)

21C3	SMC_RCIN_L	R3	PA0/KIN8*/PA2DC	PE0	M3		SMC_CASE_OPEN (CASE OPEN/CLOSE DETECT) 46B3
47C6 22B3 5C2	BOOT_LPC_SPI_L	P3	PA1/KIN9*/PA2DD	PE1*/ETCK	M2	47C5 46C6 5C2	SMC_TCK
26C5 23C5	PM_SYSRST_L	R2	PA2/KIN10*/PS2AC	PE2*/ETDI	M1	47C5 46C6 5C2	SMC_TDI
53B7 46D6	SMC_TPM_RESET_L	N3	PA3/KIN11*/PS2AD	PE3*/ETDO	L4	47B6 46C6 5C2	SMC_TDO
14B7 6B2	PM_EXTTS_L<0>	R1	PA4/KIN12*/PS2BC	PE4*/ETMS	L2	47C6 46C6 5C2	SMC_TMS
23C8	PM_THRM_L	N2	PA5/KIN13*/PS2BD	PF0/IRQ8*/PWM2	M7		SMC_DISP_BKLT_B 46C3
65C8 46D6 5C1	SYS_ONEWIRE	M4	PA6/KIN14*/PS2CC	PF1/IRQ9*/PWM3	P6		SMC_DISP_BKLT_A
23C1	PM_BATLOW_L	N1	PA7/KIN15*/PS2CD	PF2/IRQ10*/TMOY	R6	65A8 46C6 40C4 5B2	SMC_LID (LID OPEN/CLOSE SW)
23B8	SMC_EXTSMI_L	B10	PB0/LSMI*	PF3/IRQ11*/TMOX	N6	46C1	SMC_CPU_RESET_3_3_L
23C8	SMC_RUNTIME_SCI_L	A10	PB1/LSCI	PF4/PWM4	M6	66B7 5C1	SMC_BATT_ISET
34B3	SMC_ODD_DETECT (Optical Disk Insert detect)	D10	PB2	PF5/PWM5	R5		SMC_BATT_VSET 46C3
48A8	ISENSE_CAL_EN	A11	PB3	PF6/PWM6	P5	66D7	SMC_SYS_ISET
46C3	SMC_EXCARD_CP	B11	PB4	PF7/PWM7	N5		SMC_SYS_VSET 46C3
46C3	SMC_EXCARD_PWR_EN	C11	PB5				
46D3	SMC_EXCARD_PWR_OC_L	A12	PB6	PG0/EXIRQ8*/TMIX	P9	58C7 22C6	SPI_CE_L
45B3	SMC_PB7	D11	PB7	PG1/EXIRQ9*/TMIY	R9		SMC_PG1
46C3	SMC_FAN_0_CTL	G14	PC0/TIOCA0/WUE8*	PG2/EXIRQ10*/SDA2	N9	27C3	SMB_BSA_DATA
51B4 5D2	SMC_FAN_1_CTL	G15	PC1/TIOCB0/WUE9*	PG3/EXIRQ11*/SCL2	P8	27C3	SMB_BSA_CLK
46C3	SMC_FAN_2_CTL	G13	PC2/TIOCC0/TCLKA/WUE10*	PG4/EXIRQ12*/EXSDAA	R8	27D3	SMB_RMT_DATA
46C3	SMC_FAN_3_CTL	G12	PC3/TIOCD0/TCLKB/WUE11*	PG5/EXIRQ13*/EXSCLA	M8	27D3	SMB_RMT_CLK
46C3	SMC_FAN_0_TACH	H14	PC4/TIOCA1/WUE12*	PG6/EXIRQ14*/EXSDAB	P7	27B6	SMB_MLB_DATA
51C4 5D2	SMC_FAN_1_TACH	H15	PC5/TIOCB1/TCLKC/WUE13*	PG7/EXIRQ15*/EXSCLB	R7	27C6	SMB_MLB_CLK
46C3	SMC_FAN_2_TACH	H13	PC6/TIOCA2/WUE14*	PH0/EXIRQ6*	E1	46B6	SMC_PROCHOT
46C3 5A7	SMC_FAN_3_TACH	H12	PC7/TIOCB2/TCLKD/WUE15*	PH1/EXIRQ7*	F3	46B5	SMC_THRMTRIP
52C2	SMS_X_AXIS	M11	PD0/AN8	PH2/FWE	K2		SMC_FWE 46C6
52C2	SMS_Y_AXIS	P11	PD1/AN9	PH3/EXEXCL	C4		ALS_GAIN 46C6
52C2	SMS_Z_AXIS	R11	PD2/AN10	PH4	D4	46D6 23C3	SMS_INT_L
46C3	SMC_PD3 (ANALOG_ID)	N11	PD3/AN11	PH5	B3	52C7	SMC_ONOFF_L
62A5 46B3	SMC_NB_ISENSE	P10	PD4/AN12				
61C1 46B3	SMC_MEM_ISENSE	R10	PD5/AN13				
46C3 5A7	ALS_LEFT	N10	PD6/AN14				
46C3	ALS_RIGHT	M10	PD7/AN15				

OMIT

U5800
SMC_H8S2116
BGA
(4 OF 4)

NC	G3	NC0	NC12	F15	NC
NC	H3	NC1	NC13	A14	NC
NC	K3	NC2	NC14	C12	NC
NC	L3	NC3	NC15	C10	NC
NC	N4	NC4	NC16	C5	NC
NC	M5	NC5	NC17	A3	NC
NC	N7	NC6	NC18	B8	NC
NC	M12	NC7	NC19	E4	NC
NC	M13	NC8	NC20	H4	NC
NC	L12	NC9	NC21	M9	NC
NC	K15	NC10	NC22	N8	NC
NC	J14	NC11			

64D1 48C8 46D8 46D5 46D1 45D3 45D2 =PP3V42_G3H_SMC

CRITICAL
C5802 22UF 20% 6.3V CERM-X5R 805
C5803 0.1UF 20% 10V CERM 402
C5804 0.1UF 20% 10V CERM 402
C5805 0.1UF 20% 10V CERM 402
C5806 0.1UF 20% 10V CERM 402

LAYOUT NOTE:
PLACE R5899, C5820 NEAR SMC PIN N14, N15

(VCL IS INTERNAL RAIL)
SMC_VCL

64D1 48C8 46D8 46D5 46D1 45D3 45D2 =PP3V42_G3H_SMC

R5899 4.7 5% 1/16W MF-LF 402

C5807 0.47UF 10% 6.3V CERM-X5R 402

LAYOUT NOTE:
PLACE C5807 NEAR PIN F1

R5809 10K 5% 1/16W MF-LF 402

R5801 10K 5% 1/16W MF-LF 402

PP3V3_AVREF_SMC 46C6

SMC_AVCC_RC

C5820 0.1UF 10% 16V CERM 402

66C2 66B1 62A5 61C1 48C1 48B5 48A1 46B6 45C2 GND_SMC_AVSS

47B6 5C2 SMC_MD1 (Should PD) (To debug card for mode select)
KBC_MDE (Should PU)

R5802 10K 5% 1/16W MF-LF 402

R5803 0 5% 1/16W MF-LF 402

NOSTUFF

OMIT
U5800
SMC_H8S2116
BGA
(3 OF 4)

AVCC N14, N15
VCC P2, P1, J15, A1, F1, VCL
AVREF M14, M15

47C5 46D7 5C2 SMC_RST_L → E3 RES*
46C7 SMC_XTAL → A2 XTAL
46C7 SMC_EXTAL → B2 EXTAL
MD1 E2
MD2 K1
NMI F4 (Should PD) (To debug card for mode select) 47B5 5C2 SMC_NMI
ETRST* L1 47C6 5C2 SMC_TRST_L
AVSS P12, R12
VSS D1, F4, R4, F12, F13, B13, A13, A4, B4, D2

R5898 10K 5% 1/16W MF-LF 402

XW5800 SM 1 2

45C4 46B6 48A1 48B5 48C1 61C1 62A5 66B1 66C2 GND_SMC_AVSS

45B8 SMC_PB7 = MAKE_BASE=TRUE SMC_ENRGYSTR_LDO_EN 46C6 66D2

45B5 SMC_PG1 = MAKE_BASE=TRUE SMC_ENRGYSTR_LDO_PGOOD 46C6 66C1

SMC

SYNC_MASTER=SMC SYNC_DATE=08/18/2005

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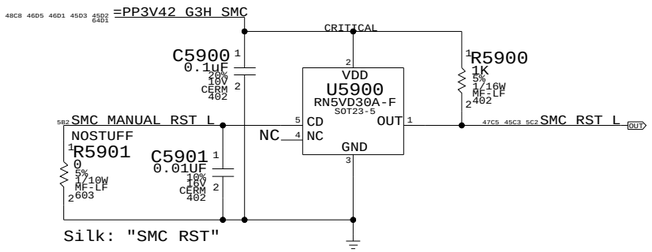
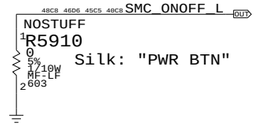
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 58 OF 98	

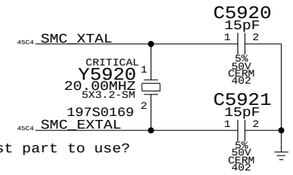
SMC Reset Button / Brownout Detect



Debug Power Button

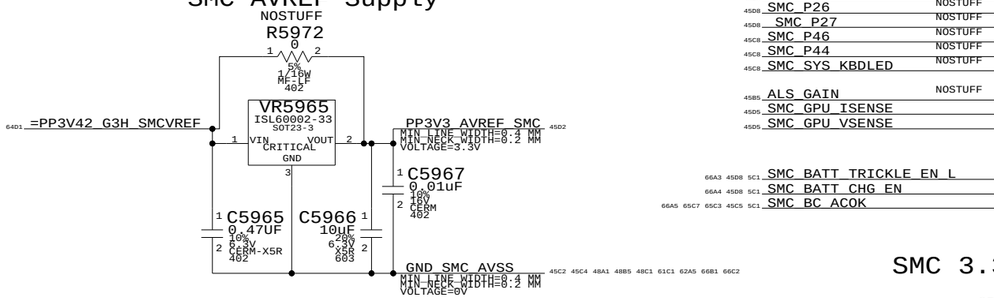


SMC Crystal Circuit



Is this the best part to use?

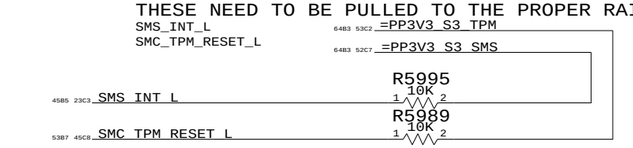
SMC AVREF Supply

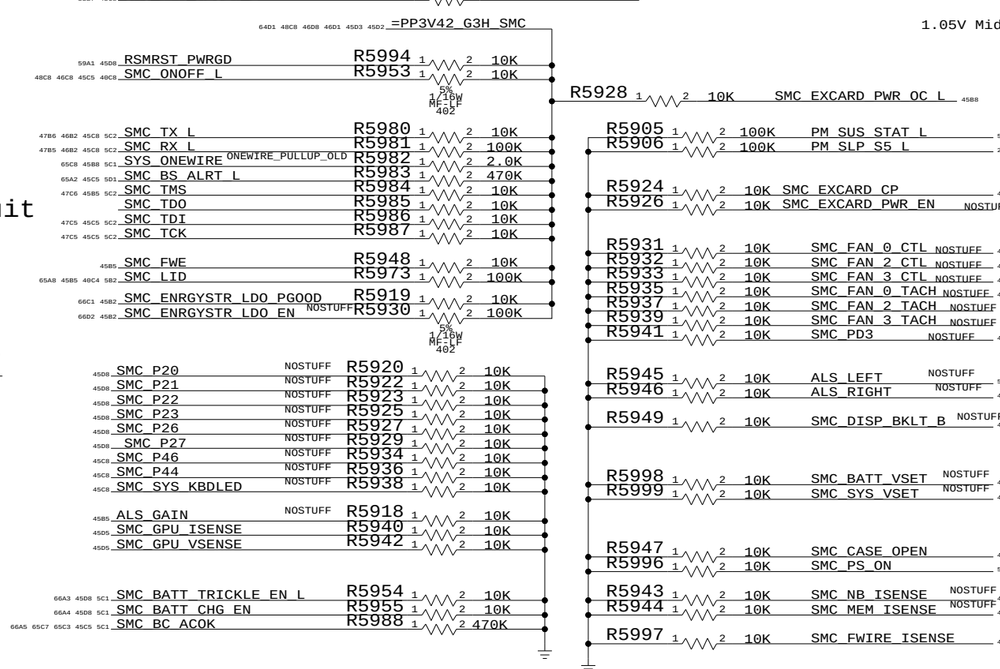


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1278	353S1381	?	VR5965	TI REF3133

THESE NEED TO BE PULLED TO THE PROPER RAIL:

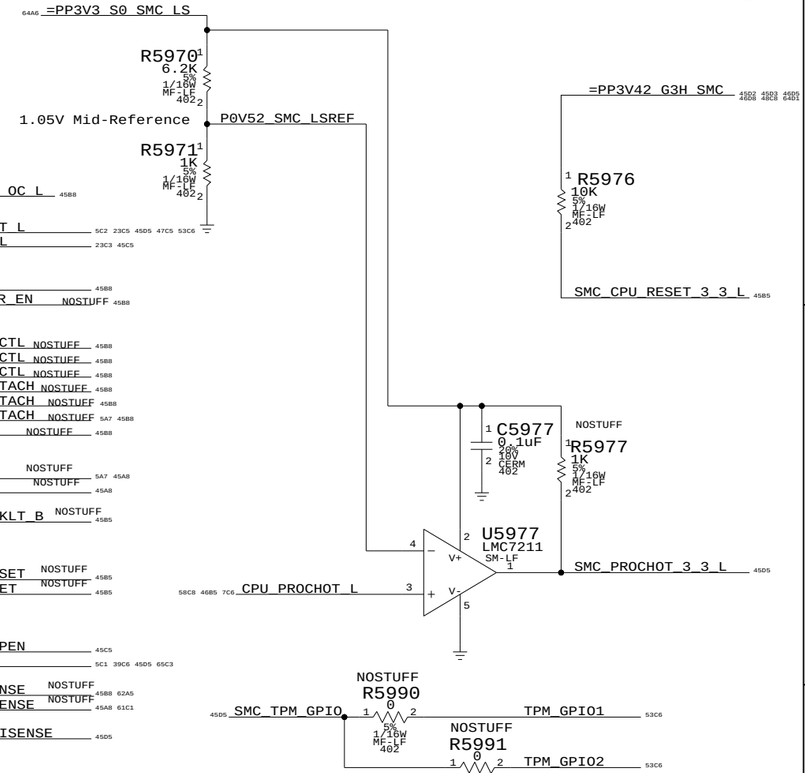
SMS_INT_L
SMC_TPM_RESET_L

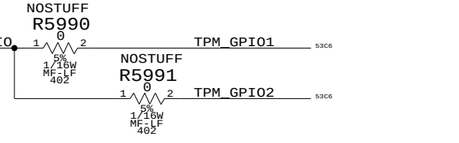


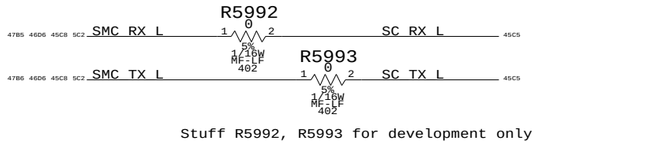


SMC 3.3V to 1.05V Level Shifting

SMC 1.05V to 3.3V Level Shifting

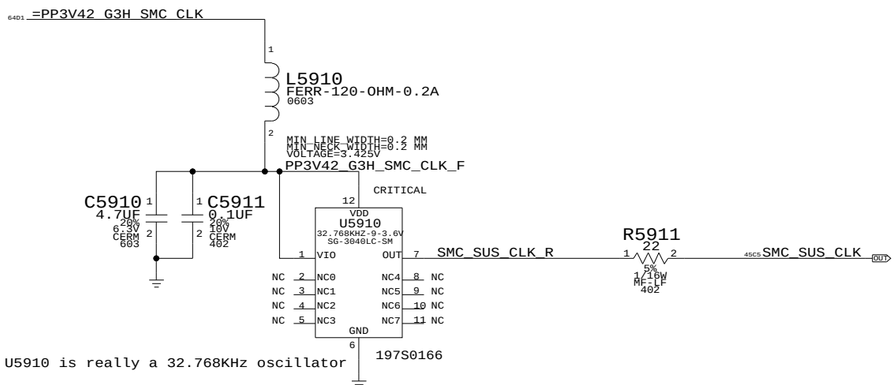




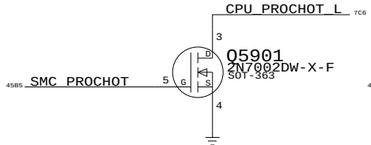


Stuff R5992, R5993 for development only

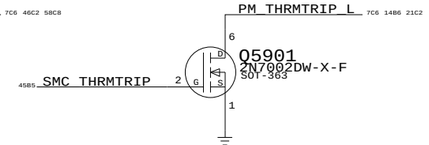
SMC G3HOT OSCILLATOR



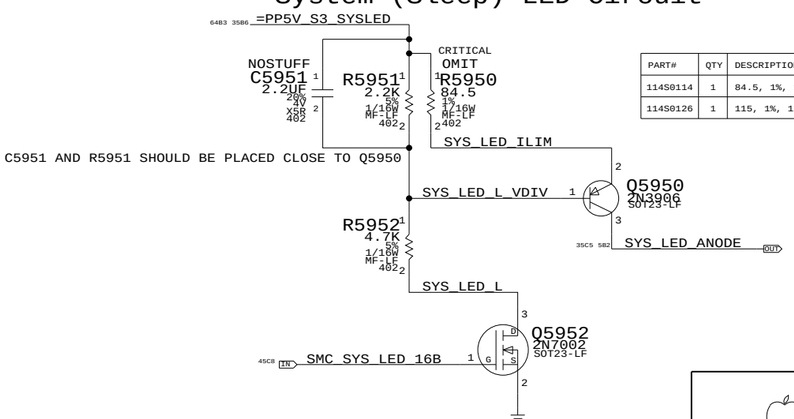
SMC_PROCHOT



SMC_THRMTRIP



System (Sleep) LED Circuit



C5951 AND R5951 SHOULD BE PLACED CLOSE TO Q5950

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S0114	1	84.5, 1%, 1/16W, MF-LF, 402	R5950	NORMAL
114S0126	1	115, 1%, 1/16W, MF-LF, 402	R5950	FANCY

SMC SUPPORT

SYNC_MASTER=SMC SYNC_DATE=08/23/2005

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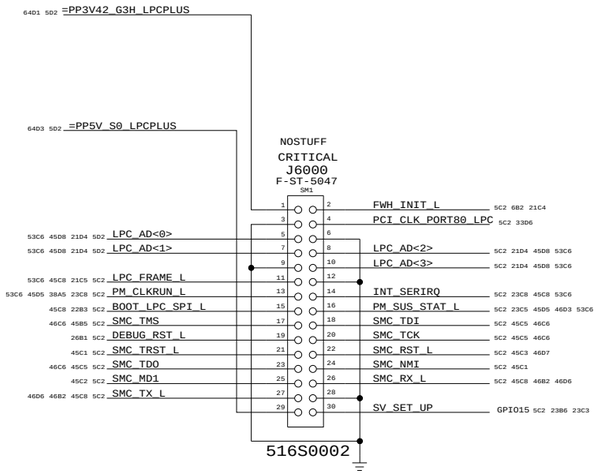
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 59 OF 98	



LPC+ Debug Connector

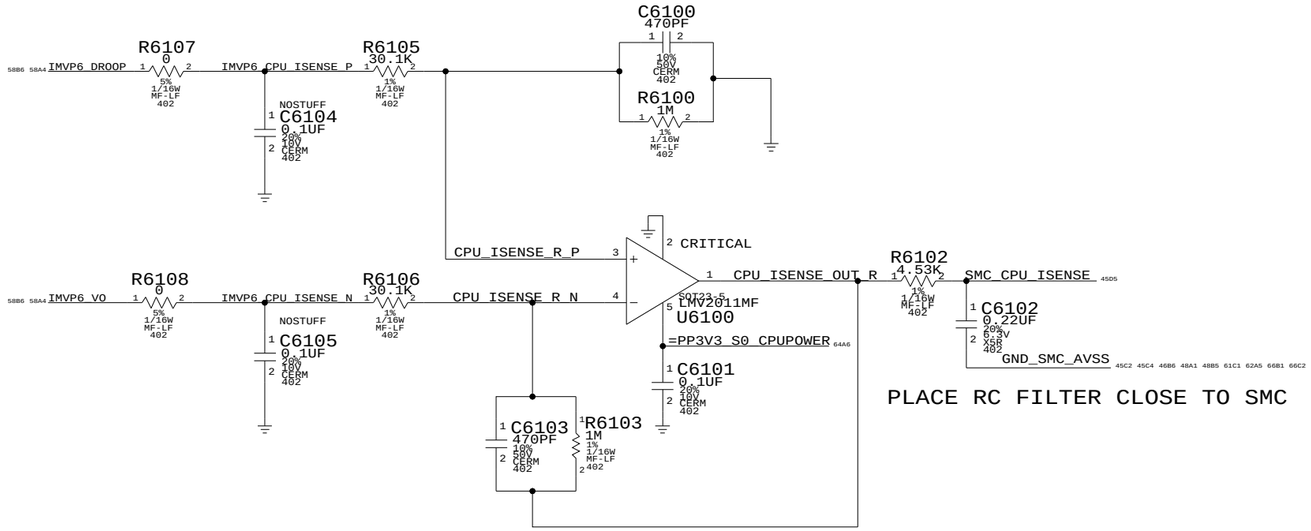
SYNC_MASTER=NB SYNC_DATE=06/30/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C

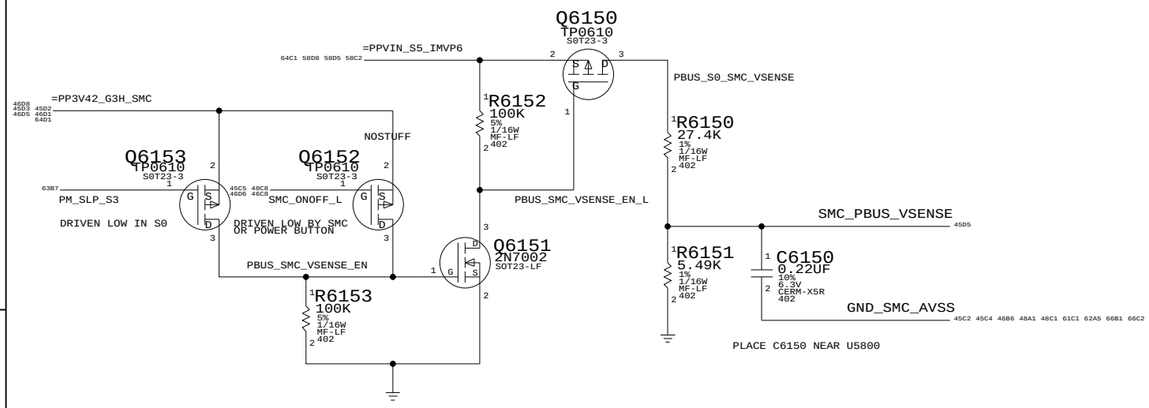
SCALE	SHT	OF
NONE	60	98

CPU CURRENT SENSE



PLACE RC FILTER CLOSE TO SMC

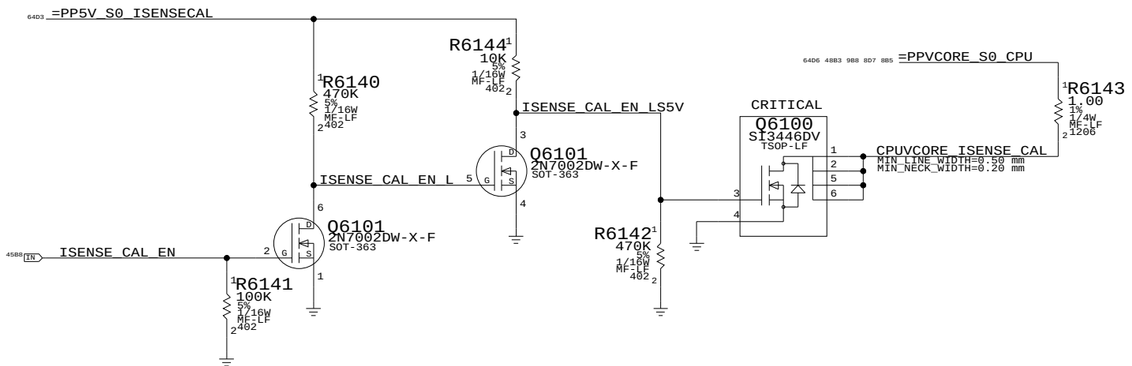
PROCESSOR DCIN VOLTAGE SENSE



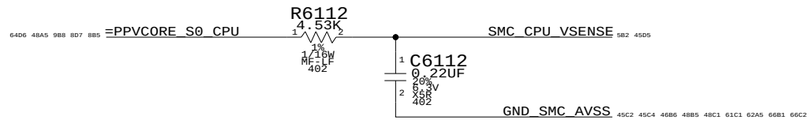
PLACE C6150 NEAR U5800

Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits



CPU VOLTAGE SENSE



PLACE RC FILTER CLOSE TO SMC

CPU Current & Voltage Sense

SYNC_MASTER=ENET SYNC_DATE=08/30/2005

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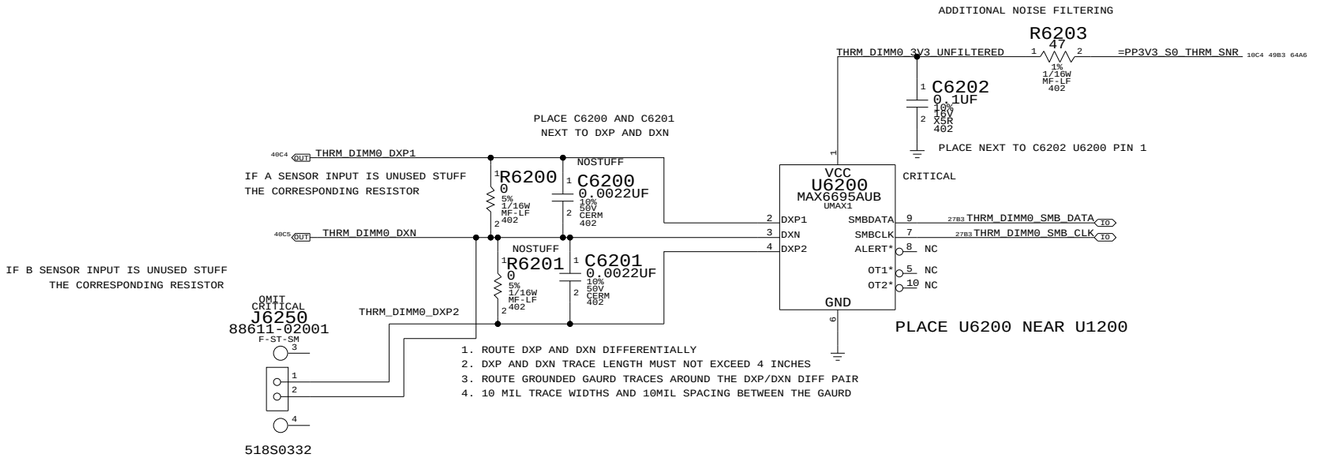
APPLE INC.

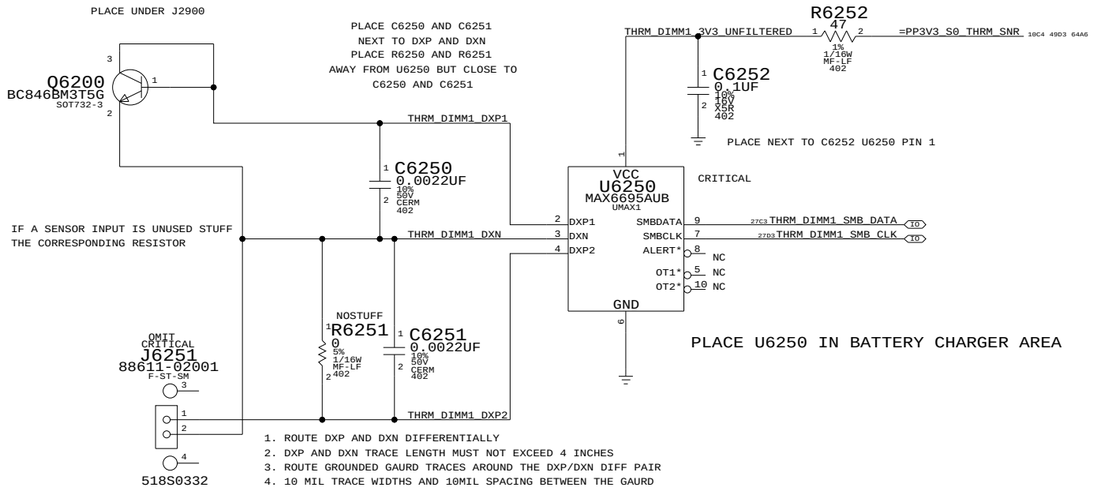
SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 61 OF 98	

DIMM0 TEMPERATURE ZONE



NOTE: REPLACE J6250 AND J6251 FROM 518S0332 TO 518S0487
AFTER THIS CHANGE, THE PCB WILL USE 518S0332 LANDPATTERN, BUT BOM WILL STUFF 518S0487 PART

DIMM1 TEMPERATURE ZONE



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
518S0487	2	JST 2-PIN CONNECTOR	J6250,J6251	M42B

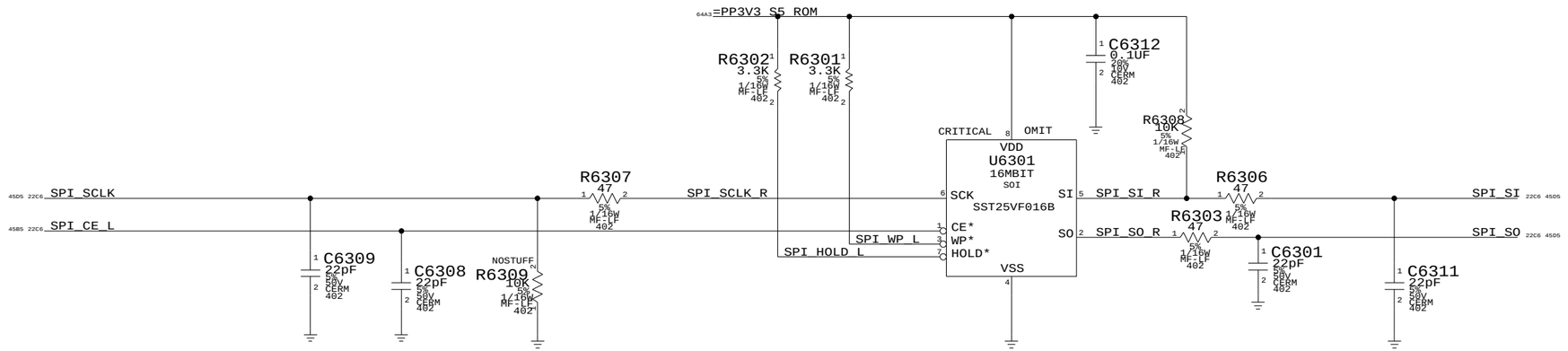
NOTE: REPLACE J6250 AND J6251 FROM 518S0332 TO 518S0487
AFTER THIS CHANGE, THE PCB WILL USE 518S0332 LANDPATTERN, BUT BOM WILL STUFF 518S0487 PART

TEMPERATURE SENSE

SYNC_MASTER=ENET SYNC_DATE=11/09/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 62 OF 98	



R6309 IS NOT NEEDED WHEN SHARING SPI FLASH WITH ICH7M AND TEKOA(LAN CHIP)

R6307 AND R6306 SHOULD BE PLACED LESS THAN 100 MILS FORM ICH7M

R6303 SHOULD BE PLACED LESS THAN 100 MILS FORM FLASH ROM

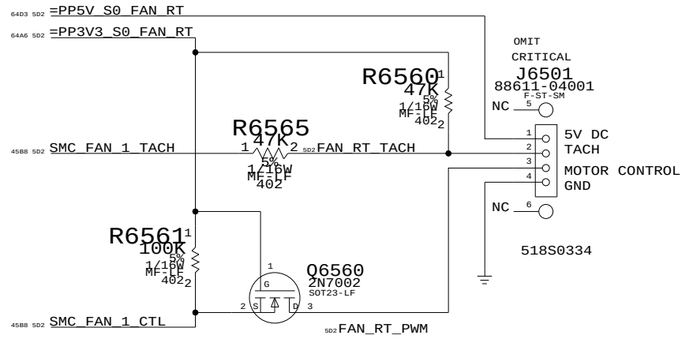
SPI BOOTROM

SYNC_MASTER=MASTER SYNC_DATE=5/23/05

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C

SCALE	SHT	OF
NONE	63	98



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
518S0486	1	IMPROVED ACES CONNECTOR	J6501	CRITICAL	M42B

Fan

SYNC_MASTER=ENET SYNC_DATE=11/10/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C

SCALE	SHT	OF
NONE	65	98

PAGE NOTES

INPUT

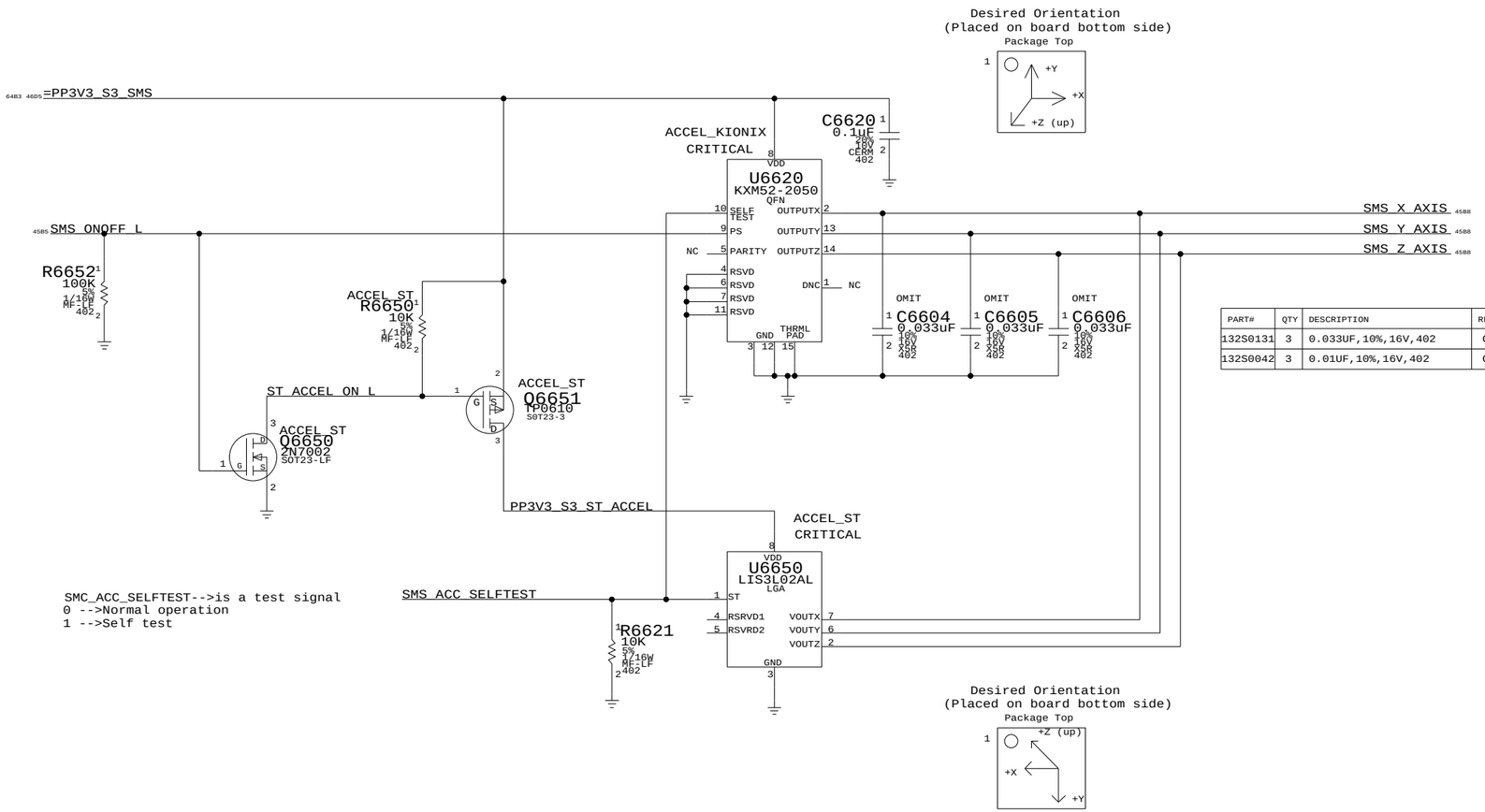
=PP3V3_S3_SMS - 3.3V POWER FOR SMS (STAYS ALIVE IN SLEEP)
SMS_ONOFF_L - CONNECT TO SMC TO BE ABLE TO PUT SMS INTO LOW-POWER MODE

OUTPUT

SMS_ACC_*_AXIS - ACCELEROMETER OUTPUT TO SCU

PAGE HISTORY

5/19/2005 - FIRST REVISION OF PAGE
7/26/2005 - REMOVED BOM TABLE AND UPDATED SYMBOL TO KXM52-2050
7/26/2005 - CONNECTED PD PIN TO SMC'S SMS_ONOFF_L
7/26/2005 -



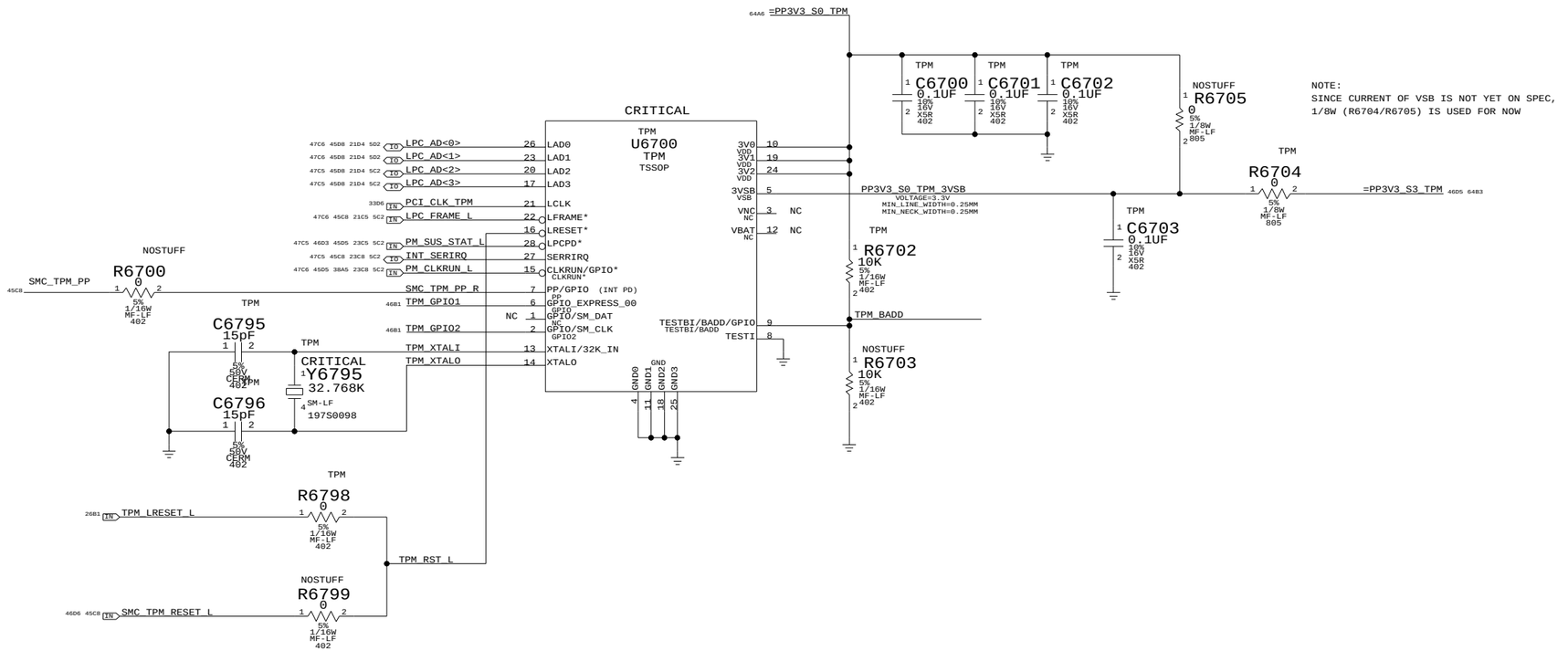
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
132S0131	3	0.033UF,10%,16V,402	C6604,C6605,C6606		ACCEL_KIONIX
132S0042	3	0.01UF,10%,16V,402	C6604,C6605,C6606		ACCEL_ST

SMS

SYNC_MASTER=SMC SYNC_DATE=08/23/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 66 OF 98	



TPM

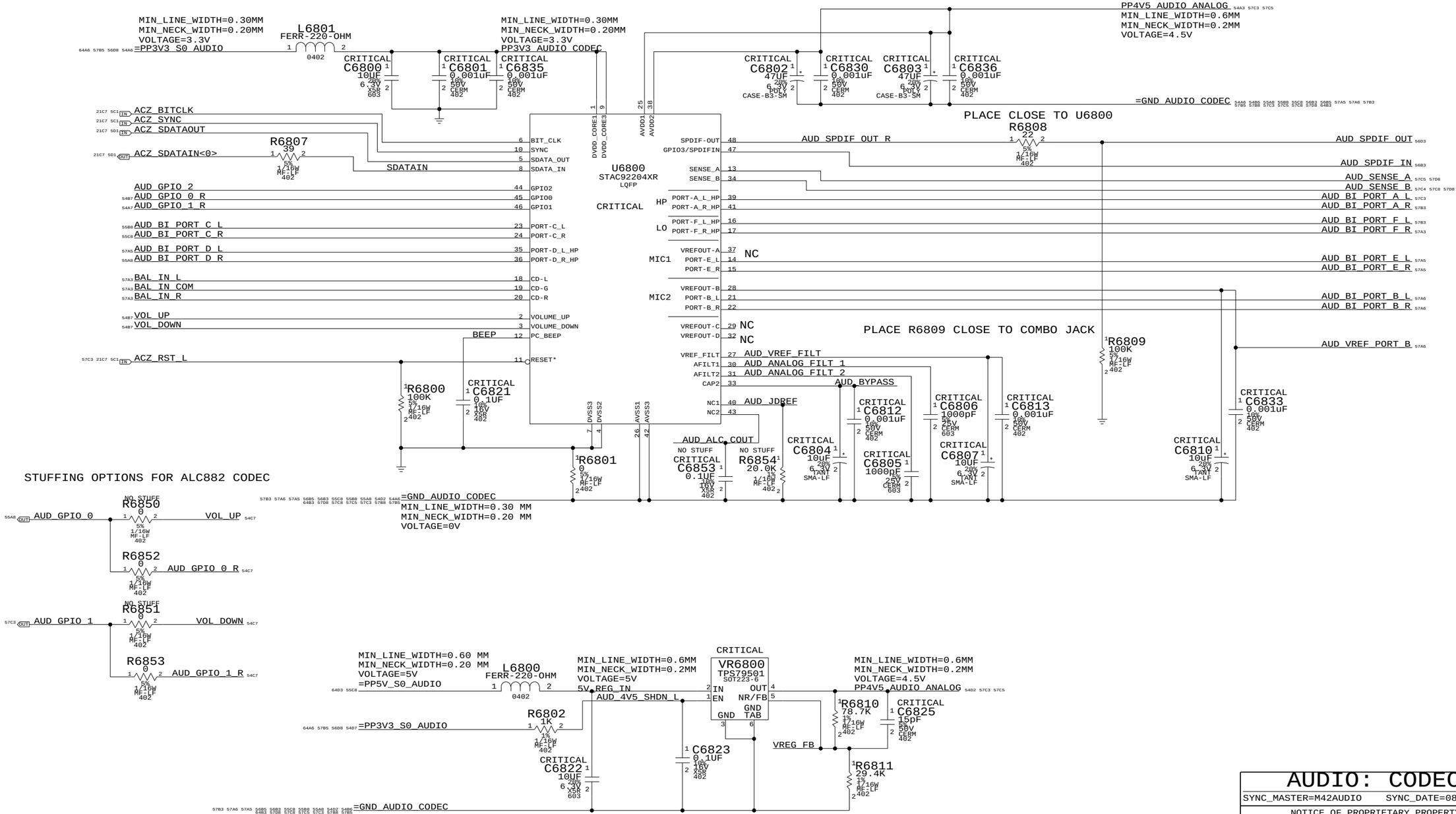
SYNC_MASTER=SMC SYNC_DATE=07/18/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 67 OF 98	

AUDIO CODEC

APPLE P/N 353S1458



AUDIO: CODEC

SYNC_MASTER=M42AUDIO SYNC_DATE=08/05/2006

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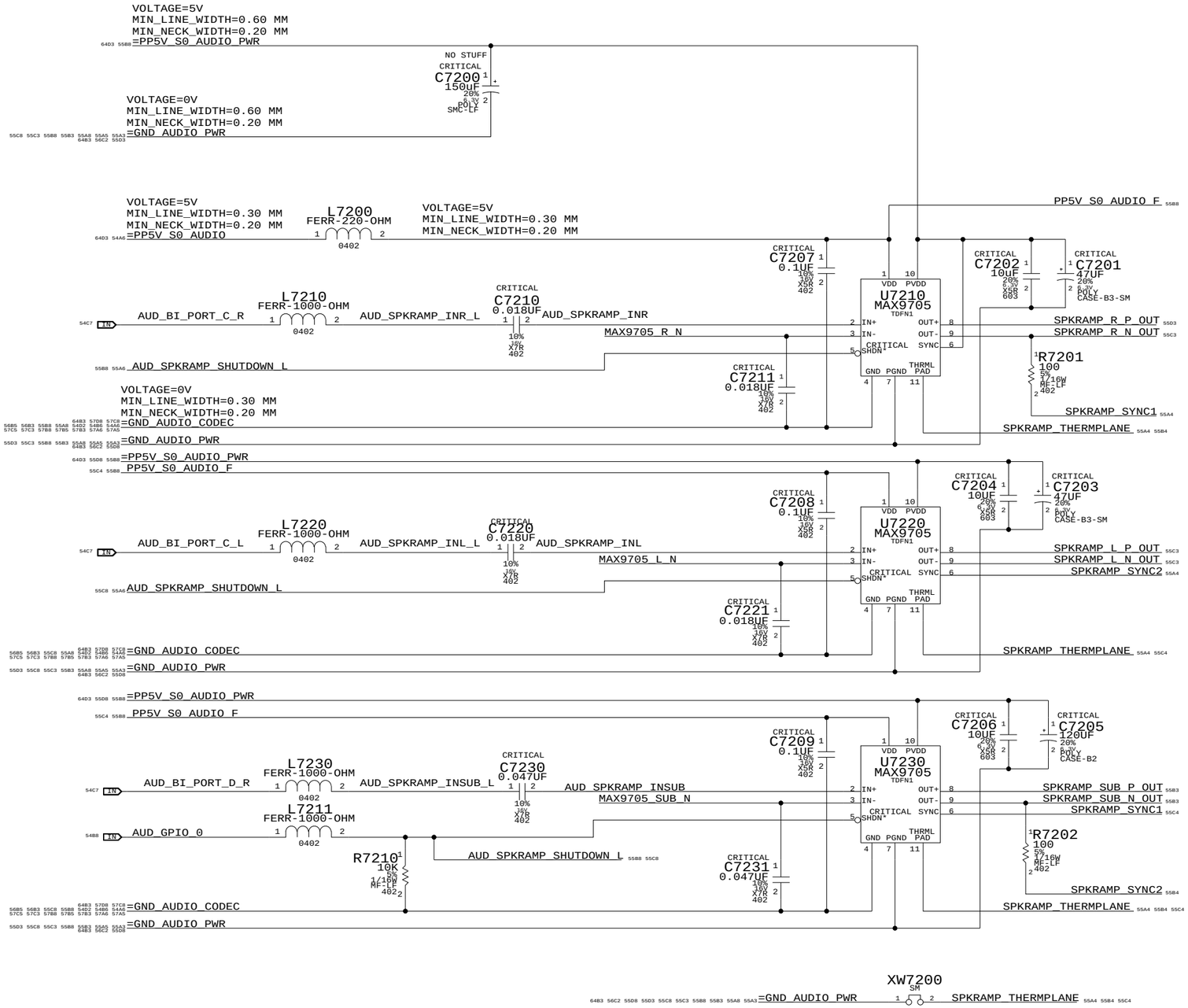
D	051-7370	C

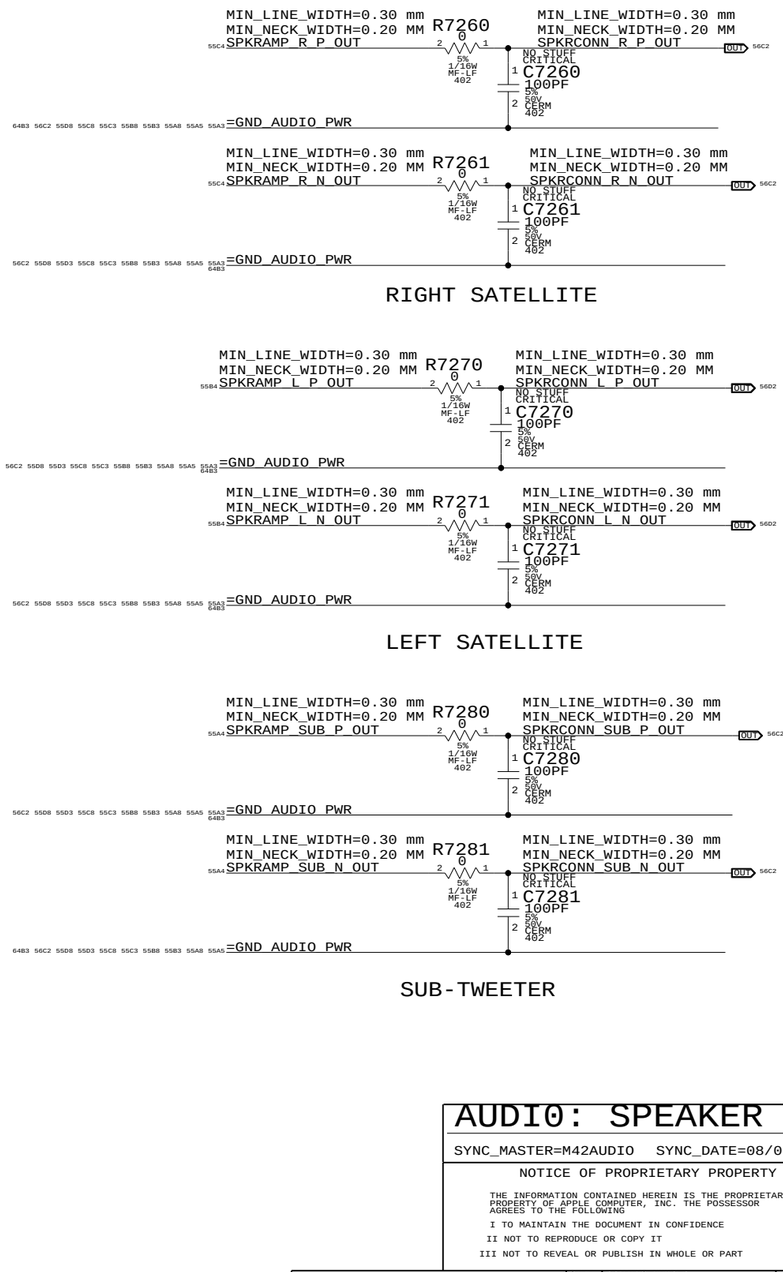
SCALE	SHT	OF
NONE	68	98

SATELLITE & SUB TWEETER AMPLIFIER APN:353S1595

SATELLITE 442 Hz < FC < 736 Hz
SUB 169 Hz < FC < 282 Hz



SPEAKER OUTPUT EMI FILTERS



AUDIO: SPEAKER AMP

SYNC_MASTER=M42AUDIO SYNC_DATE=08/05/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 72 OF 98	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
518S0491	518S0332	?	J7302	IMPROVED TWO PIN CONNECTOR

AUDIO JACK 1: LO/HP CONNECTOR, SPDIF TX

L7390 FERR-220-OHM 0402 =PP3V3_S0_AUDIO

PP3V3_S0_AUDIO_SPDIF

APN:514-0290
APN:514-0317
OMIT
CRITICAL
J7300 AUDIO-OUT F-RT-TH

VCC GND VIN

SHLD_PIN SHLD_PIN

NO STUFF C7306 100PF 5% 50V CERM 402

C7300 1UF 10% 6.3V CERM 402

GND_AUDIO_SPDIF_DGND

R7391 0 5% 1/16W MF-LF 402

CHASSIS_AUDIO_JACK_ISOL

XW7305 SM =GND_CHASSIS_AUDIO_JACK CHASSIS_AUDIO_JACK_ISOL

AUD_CONNJ1_SLEEVE
NO STUFF R7321 0 5% 1/16W MF-LF 402
AUD_CONNJ1_TIPDET
AUD_CONNJ1_RING
AUD_CONNJ1_TIP
AUD_CONNJ1_SLEEVEDET

C7307 0.047uF 10% 10V X7R 402
C7308 0.047uF 10% 10V X7R 402

CRITICAL DZ7300 5.6V-15A 0405

CRITICAL DZ7301 5.6V-15A 0405

L7300 FERR-120-OHM-1.5A 0402-LF
L7301 FERR-120-OHM-1.5A 0402-LF
L7302 FERR-1000-OHM 0402
L7303 FERR-1000-OHM 0402
L7304 FERR-1000-OHM 0402
L7305 FERR-1000-OHM 0402
L7306 FERR-1000-OHM 0402
L7307 FERR-1000-OHM 0402

AUD_CONNJ1_SLEEVE_F
AUD_CONNJ1_TIPDET_F
AUD_CONNJ1_RING_F
AUD_CONNJ1_TIP_F
AUD_CONNJ1_SLEEVEDET_F

AUD_SPDIF_OUT
AUD_PORTA_R
AUD_PORTA_L
AUD_J1_SLEEVEDET_R
AUD_J1_TIPDET_R

R7300 10K 5% 1/16W MF-LF 402
R7301 4.7 5% 1/16W MF-LF 402

C7302 100PF 5% 50V CERM 402
C7303 0.001uF 10% 50V CERM 402
C7304 100PF 5% 50V CERM 402
C7305 100PF 5% 50V CERM 402
C7301 100PF 5% 50V CERM 402

XW7300 SM AUD_J1_COM
XW7301 SM AUD_J2_COM =GND_AUDIO_CODEC

NO STUFF R7320 0 5% 1/16W MF-LF 402
CHASSIS_AUDIO_JACK_ISOL =GND_AUDIO_CODEC

MIC CONNECTOR

APN:514S0392

CRITICAL J7301 48227-0301 M-RT-SM1

MIC_LO_CONN
MIC_HI_CONN
MIC_SHLD_CONN

SPEAKER CONNECTOR

APN:518S0332

CRITICAL J7302 88611-02001 F-ST-SM

SPKRCONN_L_P_OUT
SPKRCONN_L_N_OUT

NO STUFF R7380 0 5% 1/16W MF-LF 402
=GND_AUDIO_PWR SPKR_SHIELD

OMIT
CRITICAL J7303 88611-04001 F-ST-SM

SPKRCONN_SUB_P_OUT
SPKRCONN_SUB_N_OUT
SPKRCONN_R_P_OUT
SPKRCONN_R_N_OUT

APN:518S0334

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
518S0486	1	IMPROVED ACES CONNECTOR	J7303	CRITICAL	M42B

AUDIO SHIELD FILL

AUDIO_SHIELD_PLANE

XW7302 SM CHASSIS_AUDIO_JACK_ISOL
XW7303 SM CHASSIS_AUDIO_JACK_ISOL
XW7304 SM CHASSIS_AUDIO_JACK_ISOL
NO STUFF R7382 0 5% 1/16W MF-LF 402 CHASSIS_AUDIO_JACK_ISOL

MIC EMI FILTER

L7370 FERR-1000-OHM 0402 MIC_LO MIC_LO_F
L7371 FERR-1000-OHM 0402 MIC_LO_F MIC_LO_CONN
L7372 FERR-1000-OHM 0402 MIC_HI MIC_HI_F
L7373 FERR-1000-OHM 0402 MIC_HI_F MIC_HI_CONN
L7374 FERR-1000-OHM 0402 MIC_SHIELD MIC_SHIELD_F
L7375 FERR-1000-OHM 0402 MIC_SHIELD_F MIC_SHLD_CONN

C7370 100PF 5% 50V CERM 402
C7371 100PF 5% 50V CERM 402
C7372 100PF 5% 50V CERM 402

CHASSIS_AUDIO_JACK_ISOL

AUDIO JACK 2: LINE IN CONNECTOR, SPDIF RX

PP3V3_S0_AUDIO_SPDIF

APN:514-0291
APN:514-0318
OMIT
CRITICAL
J7350 AUDIO-IN F-RT-TH

VCC GND VOUT

SHLD_PIN SHLD_PIN

NO STUFF C7357 100PF 5% 50V CERM 402

C7350 1UF 10% 6.3V CERM 402
C7351 10uF 20% 6.3V X5R 603

GND_AUDIO_SPDIF_DGND

CHASSIS_AUDIO_JACK_ISOL

R7349 10 5% 1/16W MF-LF 402 AUD_J2_OPT_OUT

AUD_CONNJ2_SLEEVE
NO STUFF R7322 0 5% 1/16W MF-LF 402
AUD_CONNJ2_TIP
AUD_CONNJ2_TIPDET
AUD_CONNJ2_RING
AUD_CONNJ2_SLEEVEDET

CRITICAL DZ7350 5.6V-15A 0405

CRITICAL DZ7351 5.6V-15A 0405

L7350 FERR-220-OHM 0402
L7351 FERR-220-OHM 0402
L7352 FERR-1000-OHM 0402
L7353 FERR-1000-OHM 0402
L7354 FERR-1000-OHM 0402
L7355 FERR-1000-OHM 0402
L7356 FERR-1000-OHM 0402
L7357 FERR-1000-OHM 0402

AUD_CONNJ2_SLEEVE_F
AUD_CONNJ2_TIPDET_F
AUD_CONNJ2_RING_F
AUD_CONNJ2_TIP_F
AUD_CONNJ2_SLEEVEDET_F

AUD_SPDIF_IN
AUD_PORTF_R
AUD_PORTF_L
AUD_J2_SLEEVEDET_R
AUD_J2_TIPDET_R

R7350 10K 5% 1/16W MF-LF 402
R7351 4.7 5% 1/16W MF-LF 402

C7353 100PF 5% 50V CERM 402
C7355 100PF 5% 50V CERM 402
C7352 100PF 5% 50V CERM 402
C7354 0.001uF 10% 50V CERM 402
C7356 100PF 5% 50V CERM 402

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0409	1	CONN,3.5MM COMBO AUDIO OUT,RA,MG3,LF	J7300	CRITICAL	NORMAL
514-0408	1	CONN,3.5MM COMBO AUDIO IN,RA,MG3,LF	J7350	CRITICAL	NORMAL
514-0411	1	CONN,3.5MM COMBO AUDIO OUT,RA,BLACK,LF	J7300	CRITICAL	FANCY
514-0410	1	CONN,3.5MM COMBO AUDIO IN,RA,BLACK,LF	J7350	CRITICAL	FANCY

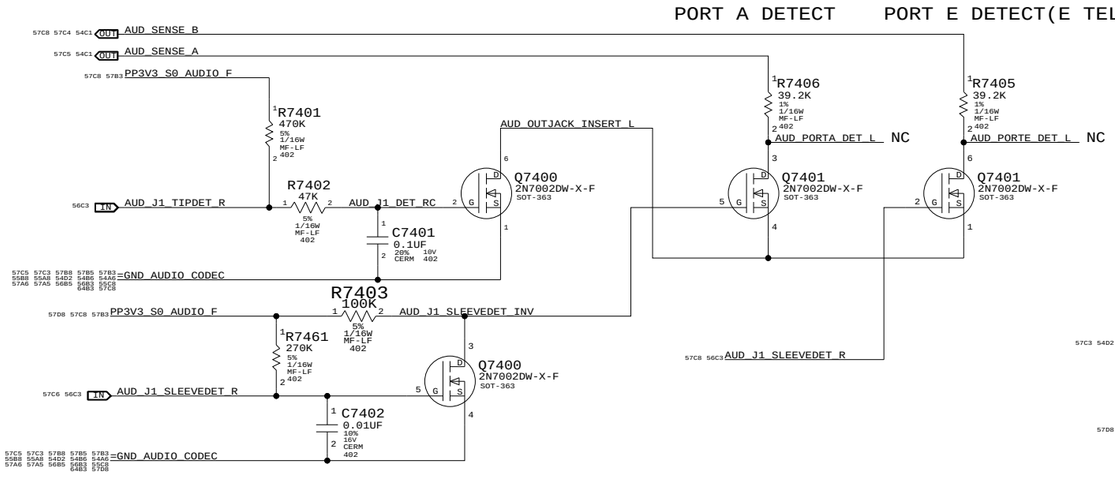
AUDIO: JACK

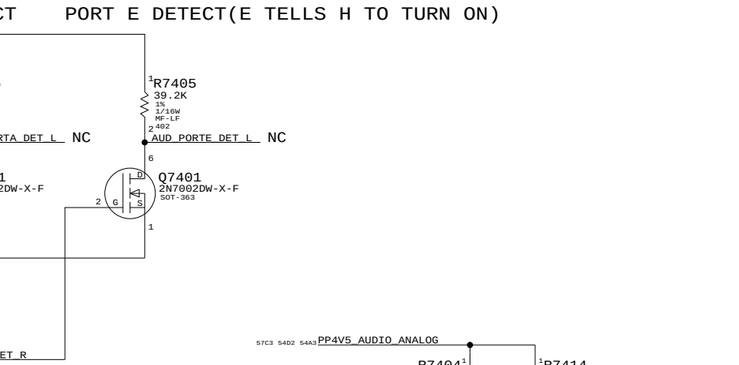
SYNC_MASTER=M42AUDIO SYNC_DATE=08/05/2006

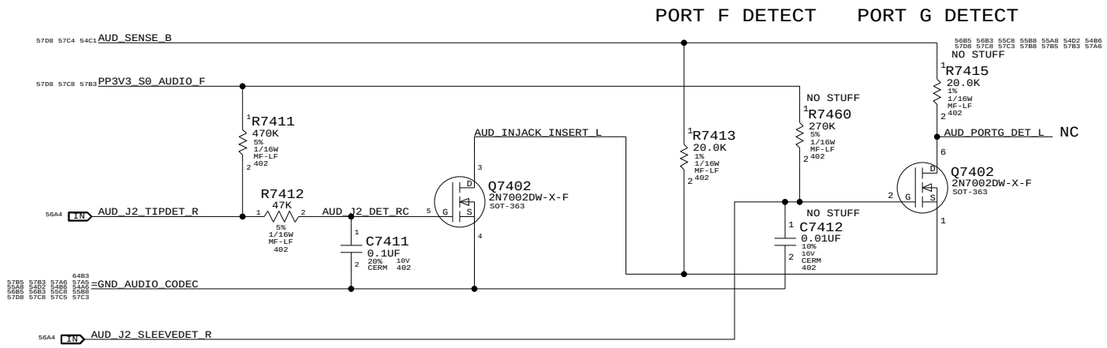
APPLE INC.

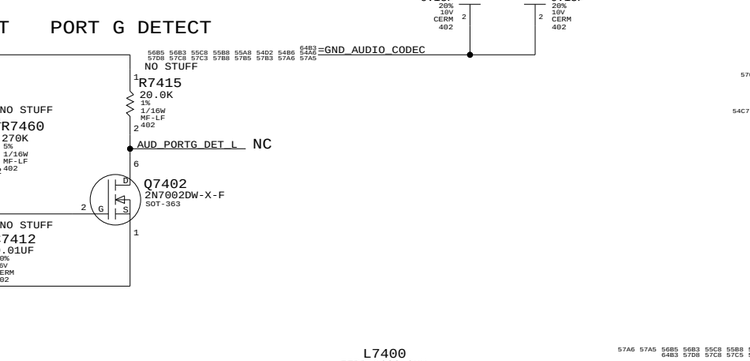
SIZE	DRAWING NUMBER	REV.
D	051-7370	C

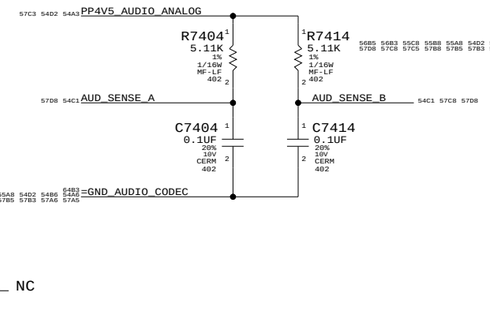
SCALE: NONE SHT 73 OF 98





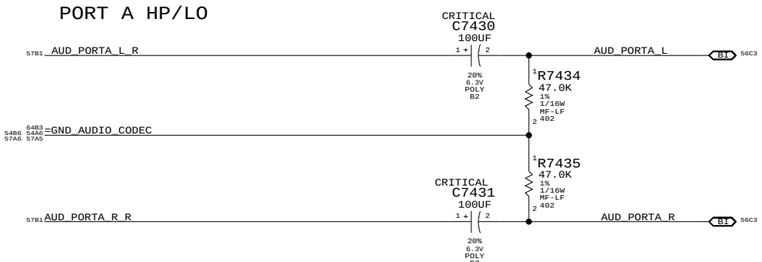


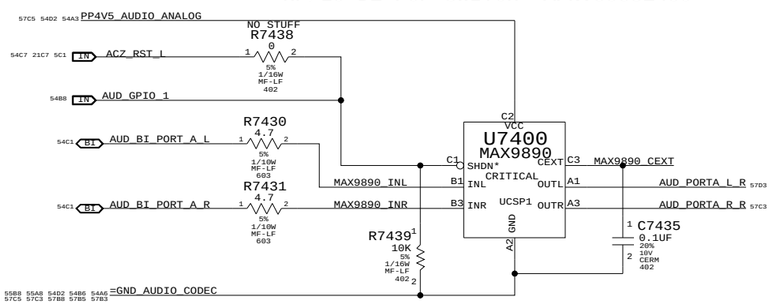


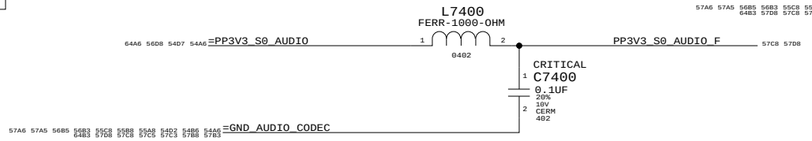


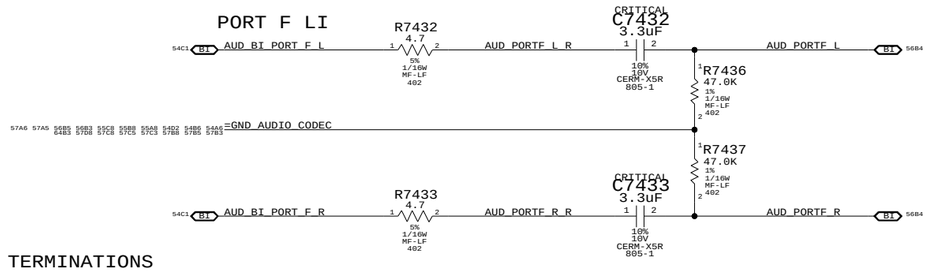
CODEC PORT ASSIGNMENTS

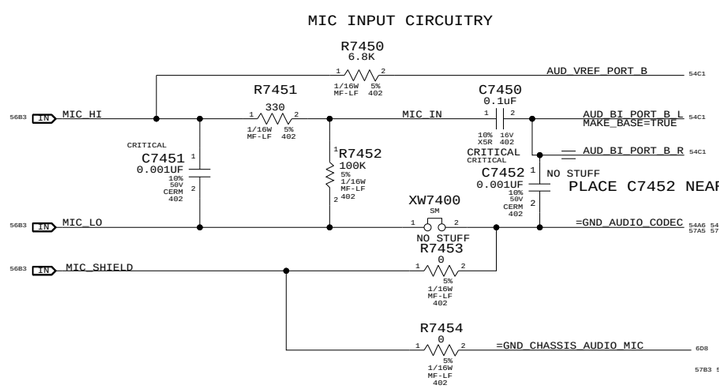
PORT A :HEADPHONE/LINE OUT
PORT B :MICROPHONE ON BOTH CH (ADC 0)
PORT C :SPEAKER AMP
PORT D :UNUSED
PORT E :SW USES TO TRIGGER DIGITAL OUT
PORT F :LINE IN (ADC 1)
CD INPUT :UNUSED

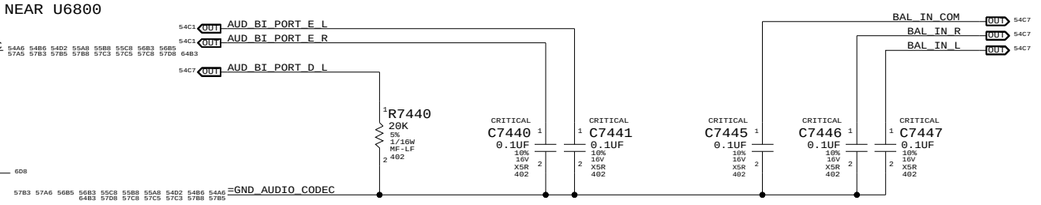












AUDIO: JACK TRANSLATORS

SYNC_MASTER=M42AUDIO SYNC_DATE=08/05/2006

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SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE	SHT	OF
NONE	74	98

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0093	128S0092	?	C7501,C7508	KEMET T520V336M016ATE045?650
128S0093	128S0092	?	C7509,C7517	KEMET T520V336M016ATE045?650

DPRSLPVR	DPRSTP*	PSI*	Operation Mode
0	1	1	2-Phase CCM
0	1	0	1-Phase CCM
1	0	1	1-Phase DCM
1	0	0	1-Phase DCM

Note 1: C7532,C7533 = 27.4 Ohm For Validating CPU Only.

R0802/R0803 **on the CPU page** protect the IMVP6 if the CPU is not installed

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S1465	1	ISL6262	U7500		M42
353S1461	1	ISL9504	U7500		M42A

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE1	1.5 MM	0.25 MM
IMVP6_BOOT1	0.25 MM	0.25 MM
IMVP6_UGATE1	1.5 MM	0.25 MM
IMVP6_LGATE1	1.5 MM	0.25 MM
IMVP6_ISEN1	0.25 MM	0.25 MM
IMVP6_FET_RC1	0.25 MM	0.25 MM
IMVP6_VSUM_R1	0.25 MM	0.25 MM
IMVP6_VO_R1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE2	0.25 MM	0.25 MM
IMVP6_BOOT2	0.25 MM	0.25 MM
IMVP6_UGATE2	0.25 MM	0.25 MM
IMVP6_LGATE2	0.25 MM	0.25 MM
IMVP6_ISEN2	0.25 MM	0.25 MM
IMVP6_FET_RC2	0.25 MM	0.25 MM
IMVP6_VSUM_R2	0.25 MM	0.25 MM
IMVP6_VO_R2	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_OCSET	0.25 MM	0.20 MM
CPU_VID_R<0..6>	0.25 MM	0.20 MM
IMVP6_VSUM	0.25 MM	0.20 MM
GND_IMVP6_SGND	0.50 MM	0.20 MM
IMVP6_VO	0.25 MM	0.20 MM
IMVP6_DROOP	0.25 MM	0.20 MM
IMVP6_DFB	0.25 MM	0.20 MM
IMVP6_SOFT	0.25 MM	0.20 MM
IMVP6_RBIAS	0.25 MM	0.20 MM
IMVP6_VDIFF	0.25 MM	0.20 MM
IMVP6_FB2	0.25 MM	0.20 MM
IMVP6_FB	0.25 MM	0.20 MM
IMVP6_COMP	0.25 MM	0.20 MM
IMVP6_VW	0.25 MM	0.25 MM
CPU_VCCSENSE_P	0.25 MM	0.25 MM
CPU_VCCSENSE_N	0.25 MM	0.25 MM
IMVP6_RTN	0.25 MM	0.25 MM
IMVP6_VSEN	0.25 MM	0.25 MM

IMVP6 CPU VCORE REGULATOR

IMVP6 CPU VCore Regulator

SYNC_MASTER=POWER SYNC_DATE=07/13/2005

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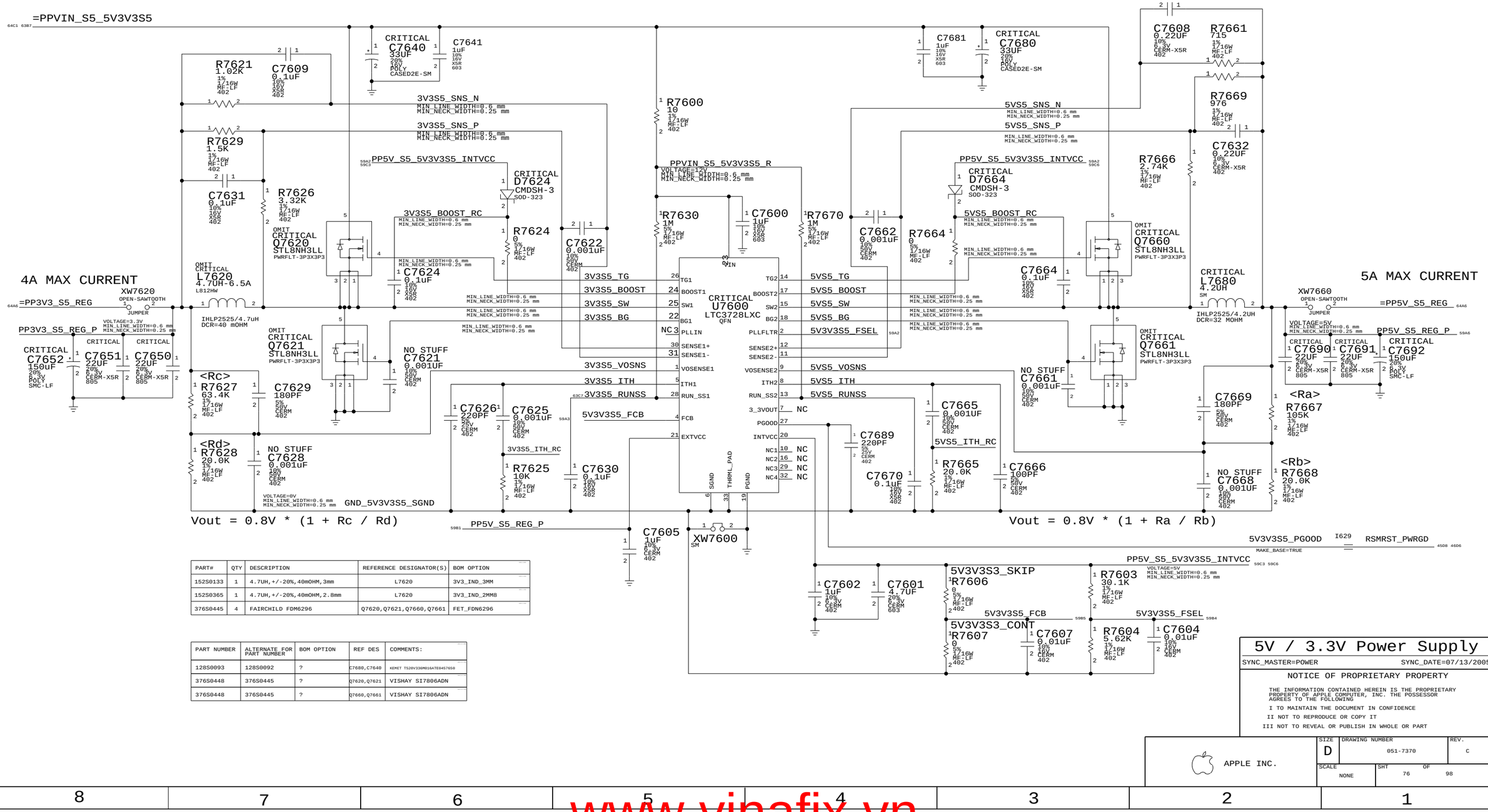
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 75 OF 98	

5V/3.3V POWER SUPPLY



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
152S0133	1	4.7UH,+/-20%,40mOHM,3mm	L7620	3V3_IND_3MM
152S0365	1	4.7UH,+/-20%,40mOHM,2.8mm	L7620	3V3_IND_2MM8
376S0445	4	FAIRCHILD FDM6296	Q7620,Q7621,Q7660,Q7661	FET_FDN6296

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0093	128S0092	?	C7680,C7640	KEMET T520V336M016ATE0457650
376S0448	376S0445	?	Q7620,Q7621	VISHAY SI7806ADN
376S0448	376S0445	?	Q7660,Q7661	VISHAY SI7806ADN

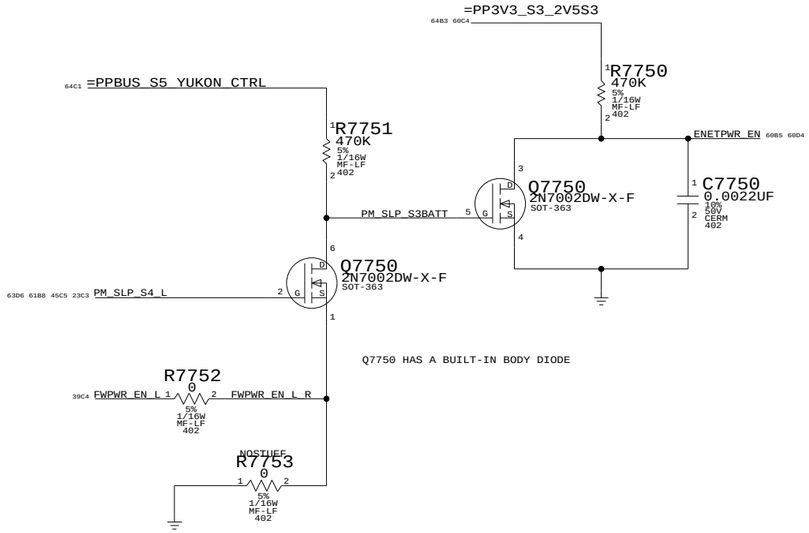
5V / 3.3V Power Supply

SYNC_MASTER=POWER SYNC_DATE=07/13/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 76 OF 98	

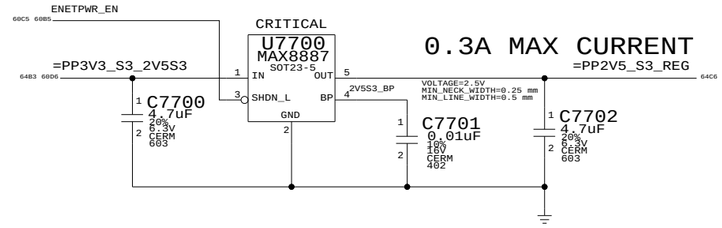
YUKON POWER CONTROL

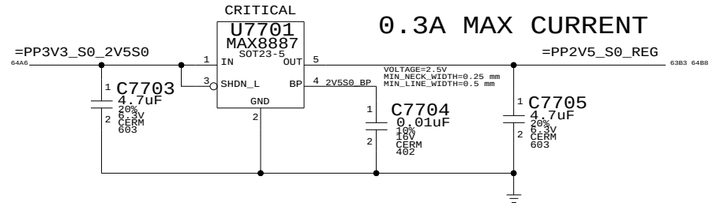


NAME	PM_SLP_S4_L	FWPWR_EN_L	PM_SLP_S3BATT	ENETPWR_EN
LOGIC	S3 | S0	~S0 | ~SMC_PS_ON		POWER YUKON
S3 ON BATTERY	TRUE (3.3V)	TRUE (PBUS 12.6V)	TRUE (PBUS 12.6V)	FALSE (0V)
S0 OR S3 ON AC	TRUE (3.3V)	FALSE (0V)	FALSE (0V)	TRUE (3.3V)
S5 ON AC	FALSE (0V)	TRUE (PBUS 12.6V)	TRUE (PBUS 12.6V)	FALSE (0V)
S5 ON BATT	FALSE (0V)	FALSE (0V)	TRUE (PBUS 12.6V)	FALSE (0V)

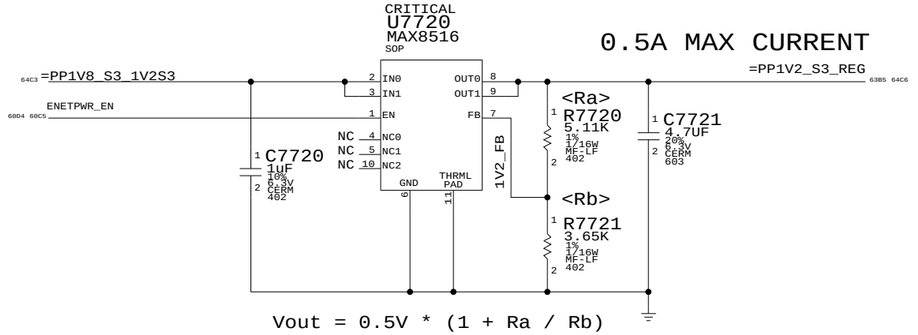
NOTE: IF CHANGE TO STUFFING R7753 THEN ENETPWR_EN IS BUFFERED PM_SLP_S4_L

2.5V REGULATORS





1.2V REGULATOR



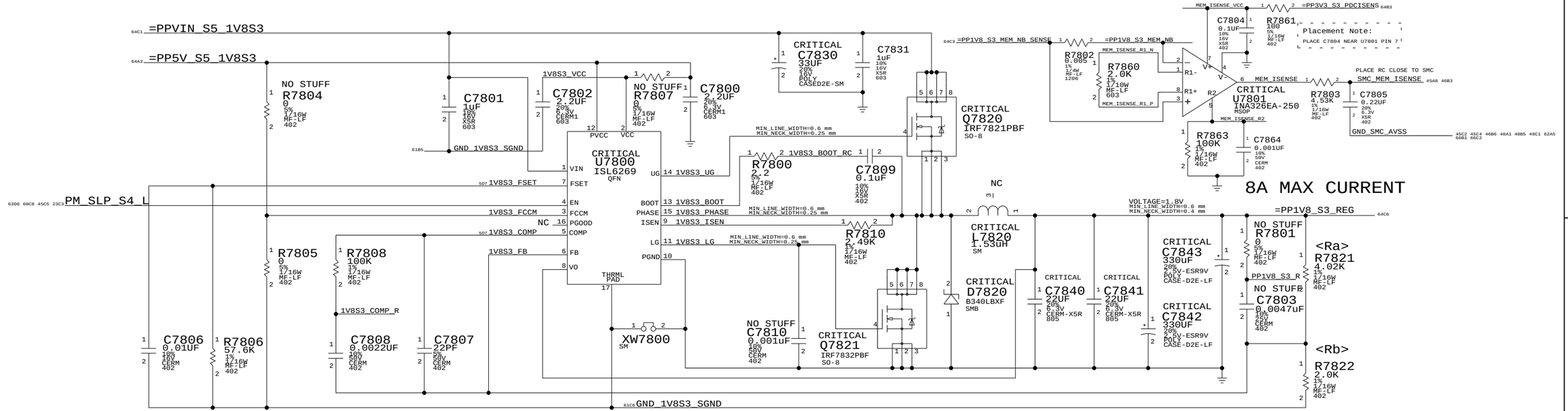
Vout = 0.5V * (1 + Ra / Rb)

2.5V/1.2V Regulator	
SYNC_MASTER=ENET	SYNC_DATE=12/06/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 77 OF 98	

1.8V POWER SUPPLY



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0093	128S0092	?	C7830	KEMET T520V336M016ATE045760

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0094	128S0060	?	C7842,C7843	PANASONIC EEFSX0D331ER
128S0095	128S0060	?	C7842,C7843	PANASONIC EEFSX0D331XE

1.8V Supply

SYNC_MASTER=POWER SYNC_DATE=07/13/2005

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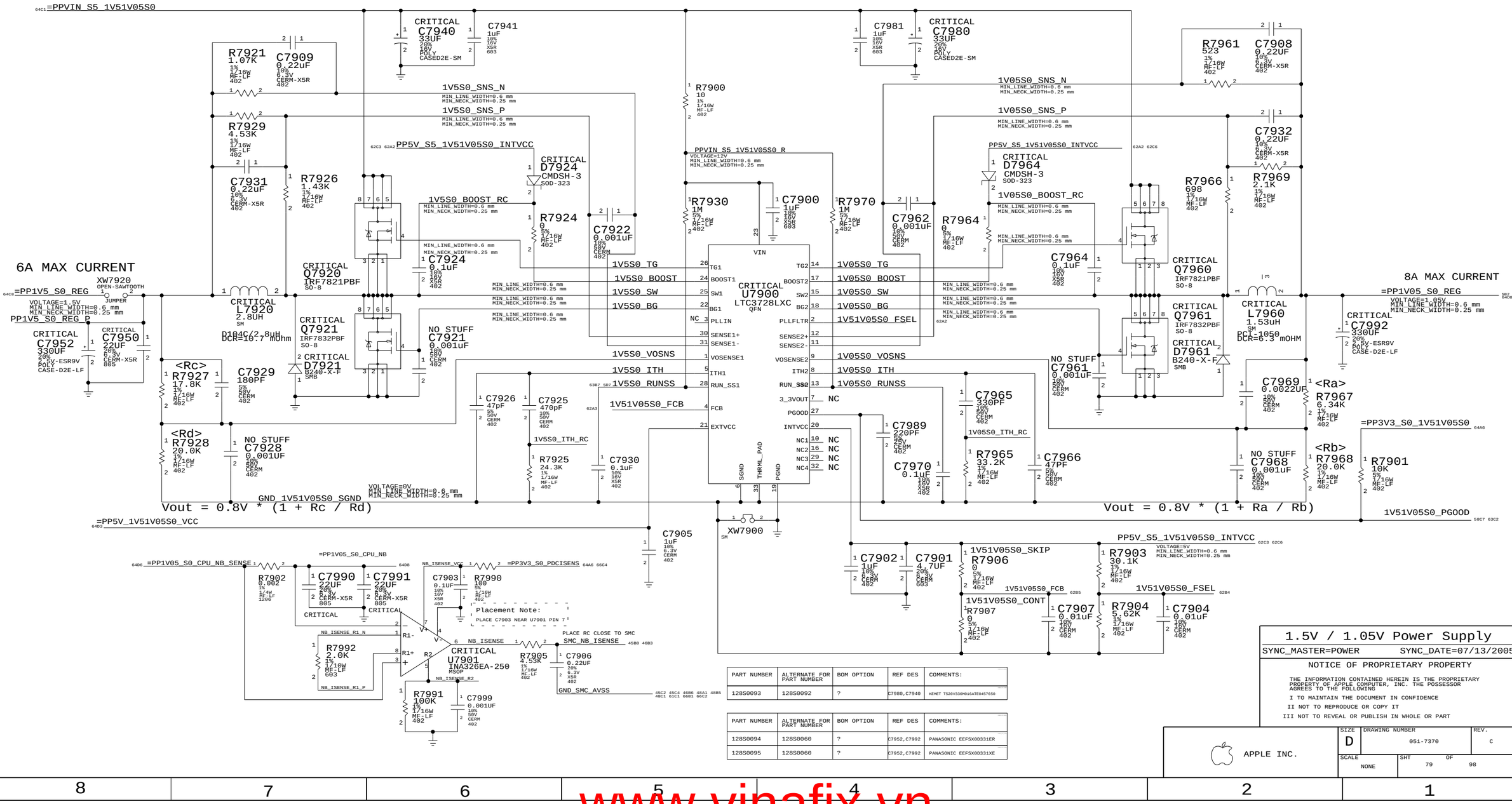
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 78 OF 98	

1.5V/1.05V POWER SUPPLY

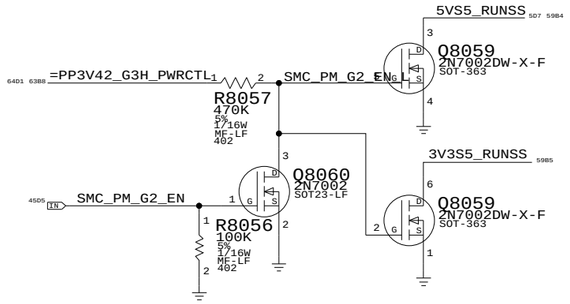


POWER CONTROL SIGNALS

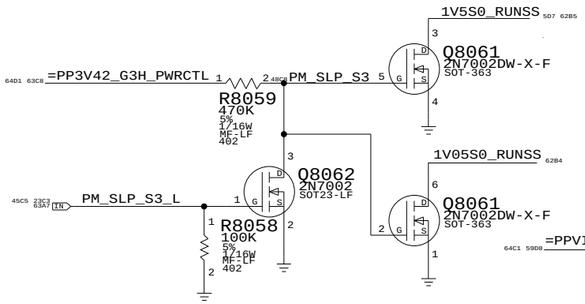
These rails are monitored by LTC2908

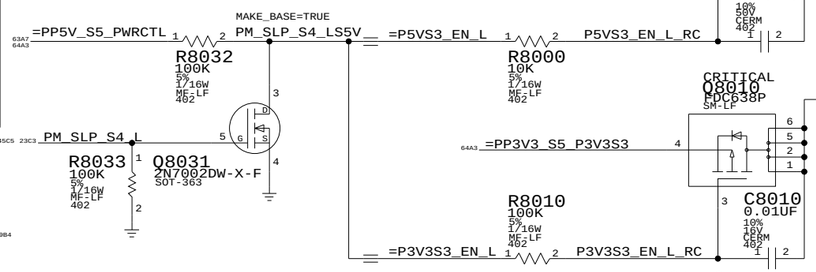
State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

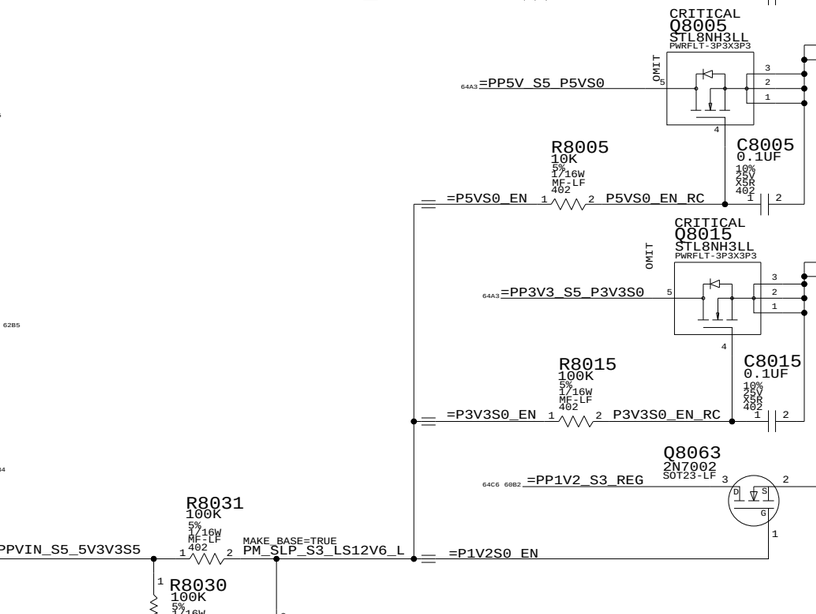
5V/3.3V S5 RUN/SS CONTROL



1.5V/1.05V S0 RUN/SS CONTROL







5V S3 FET

MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	48 mOhm @4.5V
LOADING	100 mA

3.3V S3 FET

MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	65 mOhm @2.5V
LOADING	1 A

5V S0 FET

MOSFET	STL8NH3LL
CHANNEL	N-TYPE
RDS(ON)	15 mOhm @10V
LOADING	3 A

3.3V S0 FET

MOSFET	STL8NH3LL
CHANNEL	N-TYPE
RDS(ON)	15 mOhm @10V
LOADING	2 A

1.2V S0 FET

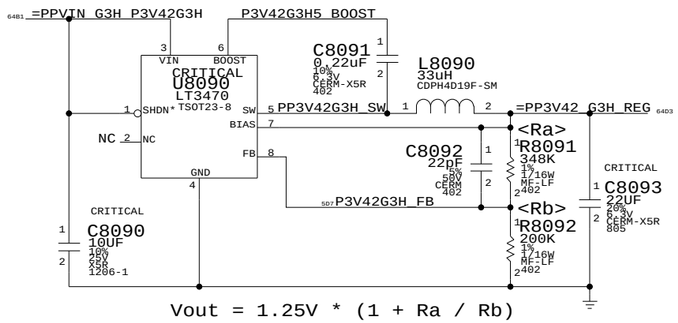
MOSFET	2N7002
CHANNEL	N-TYPE
RDS(ON)	13.5 Ohm
LOADING	Nothing

1.8V S0 FET

MOSFET	SI3447BDV
CHANNEL	P-TYPE
RDS(ON)	72 mOhm @1.8V
LOADING	320 mA

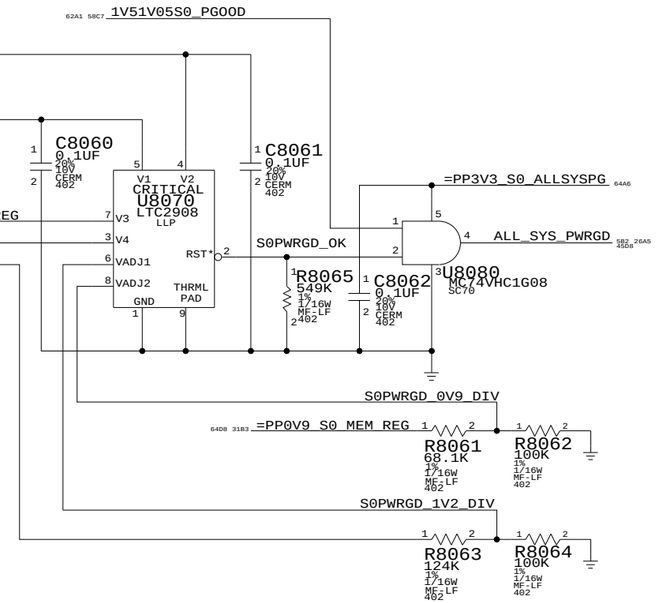
3.425V "G3Hot" SUPPLY

Supply needs to guarantee 3.31V delivered to SMC VRef generator



Vout = 1.25V * (1 + Ra / Rb)

ALL SYSTEM PWRGD CIRCUIT



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
376S0445	2	FAIRCHILD FDM6296	Q8005,Q8015	FET_FDN6296

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0448	376S0445	?	Q8005,Q8015	VISHAY SI7806ADN

S3/S0 FETS, G3H SUPPLY

SYNC_MASTER=ENET SYNC_DATE=08/30/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C

SCALE: NONE SHT 80 OF 98

"S0" RAILS ONLY ON IN RUN

PPVCORE_CPU_S0
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.4MM
VOLTAGE=0.9V

(REGULATOR OUTPUT CPU VCORE PWR) =PPVOUT_S0_IMVP6_REG (58D1)
(CPU VCORE PWR) =PPVCORE_S0_CPU — 8B5 8D7 9B8 48A5 48B3

PP0V9_S0
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.4MM
VOLTAGE=0.9V

(LDO OUTPUT 0.9V PWR) =PP0V9_S0_MEM_REG (63B2 31B3)
(DDR2 TERMINATION 0.9V PWR) =PP0V9_S0_MEM_TERM — 30D4

PP1V05_S0
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.05V

(REGULATOR OUTPUT 1.05V PWR) =PP1V05_S0_REG (62B1 5B2)
(ICH CPU I/O 1.05V PWR) =PP1V05_S0_SB_CPU_IO — 21C1 24C3 25C4
(ICH VCORE 1.05V PWR) =PPVCORE_S0_SB — 24D3 25D3
=PP1V05_S0_CPU_NB_SENSE — 62A8

PP1V05_S0_CPU_NB
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.4MM
VOLTAGE=1.05V

=PP1V05_S0_CPU_NB (62A6)
(MCH CORE 1.05V PWR) =PPVCORE_S0_NB — 16C8 16D3 19C8 19D7
(CPU FSB 1.05V PWR) =PP1V05_S0_CPU — 7B5 7B6 7D5 8C7 9C8 11B3 11C5
(MCH FSB 1.05V PWR) =PP1V05_S0_FSB_NB — 12A7 12B7 12C2 19D7 33B8 33C7 33C8
=PP1V05_S0_NB_VTT — 17D3 19B5 19D7
(MCH FSB 1.05V PWR) =PP1V05_S0_NB — 19D1 19D7

PP1V5_S0
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.4MM
VOLTAGE=1.5V

(REGULATOR OUTPUT 1.5V PWR) =PP1V5_S0_REG (62B8)
(CPU AVDD 1.5V PWR) =PP1V5_S0_CPU — 8B7 9D8
(MCH PCIE GRAPHICS O/P COMPENSATION 1.5V PWR) =PP1V5_S0_NB_PCIE — 13D2 19D7
(MCH DDR DLL&IO, FSB HSIO&IO PWR 1.5V) =PP1V5_S0_NB_VCCAUX — 16D1 17B6 19B6 19D7
(MCH DIGITAL DIVIDER IN HMPLL 1.5V PWR) =PP1V5_S0_NB_VCCD_HMPLL — 17C6 19D7
(MCH LVDS DIGITAL 1.5V PWR) =PP1V5_S0_NB_VCCD_LVDS — 17C6 19B8 19D7
(HOST/MEMORY PLL 1.5V PWR) =PP1V5_S0_NB_PLL — 19C6 19D7
=PP1V5_S0_NB — 19C1 19D7
(MCH TVDAC DEDICATED/QUIET PWR 1.5V) =PP1V5_S0_NB_TVDAC — 19A8 19D7
(MCH 3GIO[PCIE/DMI] 1.5V PWR) =PP1V5_S0_NB_3G — 19B5
(MCH 3GIO PLL 1.5V PWR) =PP1V5_S0_NB_3GPLL — 19A5
(ICH LOGIC&IO[ARX] 1.5V PWR) =PP1V5_S0_SB_VCC1_5_A_ARX — 24B5 25D6
(ICH SATA PLL 1.5V PWR) =PP1V5_S0_SB_VCCSATAPLL — 24B5 25D6
(ICH LOGIC&IO[ATX] 1.5V PWR) =PP1V5_S0_SB_VCC1_5_A_ATX — 24A5 25C6
(ICH USB PLL 1.5V PWR) =PP1V5_S0_SB_VCCUSBPLL — 24A5 25B6
(ICH USB CORE 1.5V PWR) =PP1V5_S0_SB_VCC1_5_A_USB_CORE — 24A3 25B2
(ICH LOGIC&IO 1.5V PWR) =PP1V5_S0_SB_VCC1_5_A — 24A3 25C2
=PP1V5_S0_SB — 25A8 25C8
(WIRELESS CARD 1.5V PWR) =PP1V5_S0_AIRPORT — 43D3

PP1V8_S0
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.4MM
VOLTAGE=1.8V

(COME FROM S3 TO S0 MOSFET) =PP1V8_S0_FET (63B3)
(DDR2 TERMINATION REGULATOR 1.8V SWITCH PWR) =PP1V8_S0_TMDS — 68D6

PP2V5_S0
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=2.5V

(COME FROM S3 TO S0 MOSFET) =PP2V5_S0_REG (63B3 60C2)
(MCH H/V SYNC 2.5V PWR) =PP2V5_S0_NB_VCCSYNC — 17D6 19B6 19D7
(MCH LVDS DATA/CLK TX 2.5V PWR) =PP2V5_S0_NB_VCC_TXLVDS — 17D6 19B8 19D7
(MCH PCIE/DMI BAND GAP 2.5V PWR) =PP2V5_S0_NB_VCCA_3GBG — 17D6 19B7 19D7
(MCH LVDS ANALOG 2.5V PWR) =PP2V5_S0_NB_VCCA_LVDS — 17C6 19C7 19D1
(MCH CRTDAC ANALOG 2.5V PWR) =PP2V5_S0_NB_CRTDAC — 19D4 19D7
(TMDS 2.5V PWR) =PP2V5_S0_TMDS — 68B7
=PP2V5_S0_NB_DISP_PLL — 19D6

PP3V3_S0
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.30MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V

(COME FROM S5 TO S0 MOSFET) =PP3V3_S0_FET (63C3)
(MCH HV BUFFER 3.3V PWR) =PP3V3_S0_NB_VCC_HV — 17C6 19B7 19C7
=PP3V3_S0_SB — 22B5 25D8 34C8
(ICH GPIO PULLS 3.3V PWR) =PP3V3_S0_SB_GPIO — 21C3 21D3 23B2 23D5
(ICH IO BUFFER 3.3V PWR) =PP3V3_S0_SB_VCC3_3 — 24B5 25B8 25C6
(ICH PCI I/O 3.3V PWR) =PP3V3_S0_SB_VCC3_3_PCI — 24B3 25A4
(ICH IDE I/O 3.3V PWR) =PP3V3_S0_SB_VCC3_3_IDE — 24C3 25B4
(ICH PCI PULLS 3.3V PWR) =PP3V3_S0_SB_PCI — 26D1
(ICH PM PULLS 3.3V PWR) =PP3V3_S0_SB_PM — 26B6 26B8
(PATA PULLS 3.3V PWR) =PP3V3_S0_PATA — 34C2
(SATA 3.3V PWR) =PP3V3_S0_SMC_LS — 46D3
(MCH PULLS 3.3V PWR) =PP3V3_S0_NB — 14C7 14D6 19C7 20A4 20B4
(ICH LAN I/F 3.3V PWR, NEED TO CHECK INTEL) =PP3V3_S0_SB_VCCLAN3_3 — 24D3 25D3
(ICH INTEL HDA CORE 3.3V PWR) =PP3V3_S0_SB_3V3_1V5_VCCHDA — 24C3 25C4
(DIMM SPD 3.3V PWR) =PPSPD_S0_MEM — 28A7 29A3 29A7
(CLOCK GENERATOR 3.3V PWR) =PP3V3_S0_CK410 — 32C7 32D3 32D8
(WIRELESS CARD 3.3V PWR) =PP3V3_S0_AIRPORT — 43C3
(TPM 3.3V PWR) =PP3V3_S0_TPM — 53D4
(AUDIO 3.3V PWR) =PP3V3_S0_AUDIO — 54A6 54D7 56D8 57B5
(TMDS 3.3V PWR) =PP3V3_S0_TMDS — 68B1 68B2 68C8 68D8 69B7 69D1 69D5
(CPU THERMAL SENSOR 3.3V PWR) =PP3V3_S0_THRM_SNR — 10C4 49B3 49D3
(ISL6262 3V3) =PP3V3_S0_IMVP6 — 58D8
=PP3V3_S0_RSTBUF — 26B4
=PP3V3_S0_SMBUS_SB — 27D8
=PP3V3_S0_SMBUS_SMC_0 — 27D5
=PP3V3_S0_SMBUS_SMC_MLB — 27C5
=PP3V3_S0_ALLSYSPG — 63B1
=PP3V3_S0_FAN_RT — 5D2 51C4
=PP3V3_S0_LCD — 67B5 67B7 67C6
=PP3V3_S0_PBATTISENS — 66B3
=PP3V3_S0_PDCISENS — 62A5 66C4
=PP3V3_S0_CPUPOWER — 48C2
=PP3V3_S0_SMBUS_SMC_BSB — 27B1
=PP3V3_S0_1V51V05S0 — 62B1
=PP3V3_S0_2V5S0 — 60C4
(FIREWIRE DIGITAL 3.3V PWR) =PP3V3_S0_FW — 39C6
=PP3V3_S0_ENET — 36C8

PP5V_S0
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.30 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=5V

(COME FROM S5 TO S0 MOSFET) =PP5V_S0_FET (63C3)
=PP5V_S0_SB — 25D8
(SATA 5V PWR) =PP5V_S0_SATA — 35C6
(DDR2 TERMINATION) =PP5V_S0_MEMVTT — 31C6
(AUDIO 5V PWR) =PP5V_S0_AUDIO — 54A6 55C8
(AUDIO SPEAKER 5V PWR) =PP5V_S0_AUDIO_PWR — 55B8 55D8
(LPC DEBUG BOARD 5V PWR) =PP5V_S0_LPCPLUS — 5D2 47C6
(MCH TV 3.3V LDO) =PP5V_S0_NB_TVDAC — 19C4 19C7
(ISL6262 VDD) =PP5V_S0_IMVP6 — 58D8
(LTC3728LXC EXTVCC) =PP5V_1V51V05S0_VCC — 62A8
(TMDS 5V PWR) =PP5V_S0_TMDS — 68B7 69C6
=PP5V_S0_FAN_RT — 5D2 51C4
=PP5V_S0_LCD — 67D7
=PP5V_S0_ISENSECAL — 48A8

"S3" RAILS
ON IN RUN AND SLEEP

PP1V2_S3
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.32MM
VOLTAGE=1.2V

(LDO OUTPUT 1.2V PWR) =PP1V2_S3_REG (63B5 60B2)
(ENET 1.2V PWR) =PP1V2_S3_ENET — 36A8 36D7

PP1V8_S3
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=1.8V

(REGULATOR OUTPUT 1.8V PWR) =PP1V8_S3_REG (61B1)
(DDR2 DIMM 1.8V PWR) =PP1V8_S3_MEM — 19C7 19C8 28B2 28D4 28D6 29B2 29D4 29D6
=PP1V8_S3_P1V8S0 — 63A5
=PP1V8_S3_MEMVTT — 31C6
=PP1V8_S3_MEM_NB_SENSE — 61C4
=PP1V8_S3_1V2S3 — 60B5

PP1V8_S3_MEM_NB
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.4MM
VOLTAGE=1.8V

=PP1V8_S3_MEM_NB (61C2 29D2 28D2 19D7 16B6 14C2)
(MCH DDR2 1.8V PWR)

PP2V5_S3
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=2.5V

(REGULATOR OUTPUT 2.5V PWR) =PP2V5_S3_REG (60C2)
(ENET 2.5V PWR) =PP2V5_S3_ENET — 36D3

PP3V3_S3
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.16 MM
VOLTAGE=3.3V

(COME FROM S5 TO S3 MOSFET) =PP3V3_S3_FET (63D3)
=PP3V3_S3_SMBUS_SMC_RMT — 27D3
(ETHERNET 3.3V PWR) =PP3V3_S3_ENET — 36A5 36B4 36B5 36C8 36D6 36D8
(BLUETOOTH 3.3V PWR) =PP3V3_S3_BT — 44C6
(ACCELEROMETER 3.3V PWR) =PP3V3_S3_SMS — 46D5 52C7
(TPM 3.3V SUSPEND PWR) =PP3V3_S3_TPM — 46D5 53C2
(TPS62050 VIN) =PP3V3_S3_2V5S3 — 60C4 60D6
(FIREWIRE CHIP PCI SIGNAL INDICATOR) =PP3V3_S3_PCI — 38C5
=PP3V3_S3_RSTGATE — 26B3
=PP3V3_S3_AIRPORT_AUX — 43C3
=PP3V3_S3_FW — 38D5
=PP3V3_S3_PDCISENS — 61C1

PP5V_S3
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.3MM
VOLTAGE=5V

(COME FROM S5 TO S3 MOSFET) =PP5V_S3_FET (63D3)
(ISL6269 PVCC)
=PP5V_S3_SYSLED — 35B6 46B4
(SYSTEM LED PWR) =PP5V_S3_CAMERA — 67A5
(USB IO PORT 5V PWR) =PP5V_S3_IR — 41D6
(USB IR CONTROLLER 5V PWR) =PP5V_S3_GEYSER — 40D6

"S5" RAILS
ALWAYS ON WHEN UNIT HAS AC POWER (TRICKLE)

PP3V3_S5
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.3MM
VOLTAGE=3.3V

(REGULATOR OUTPUT 3.3V PWR) =PP3V3_S5_REG (59B8)
=PP3V3_S5_SB — 23A7 23B7 23D4 23D8 25C8
(ICH USB CTL PULLS 3.3V PWR) =PP3V3_S5_SB_USB — 22D8
(ICH PM 3.3V PWR) =PP3V3_S5_SB_PM — 11B5 23D1 26C5
(ICH SUSPEND 3.3V PWR) =PP3V3_S5_SB_VCCSUS3_3 — 24A5 24B3 25B6 25D2
(ICH SUSPEND USB 3.3V PWR) =PP3V3_S5_SB_VCCSUS3_3_USB — 24B3 25D2
(ICH SUSPEND PULLS 3.3V PWR) =PP3V3_S5_SB_IO — 22C6
(ICH INTEL HDA SUSPEND 3.3V PWR) =PP3V3_S5_SB_3V3_1V5_VCCSUSHDA — 24C3
(SPI BOOTROM PWR) =PP3V3_S5_ROM — 50D4
=PP3V3_S5_P3V3S3 — 63D5
=PP3V3_S5_P3V3S0 — 63C5
=PP3V3_S5_FWLATEVG — 39A8
=PP3V3_S5_LCD — 67C7

PP5V_S5
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.3MM
VOLTAGE=5V

(REGULATOR OUTPUT 5 PWR) =PP5V_S5_REG (59B1)
=PP5V_S5_SB — 25C8
=PP5V_S5_P5VS3 — 63D5
=PP5V_S5_PWRCTL — 63A7 63D6
=PP5V_S5_P5VS0 — 63C5
=PP5V_S5_USB — 42C8
=PP5V_S5_PATA (PATA 5V PWR) — 34D6
=PP5V_S5_1V8S3 — 61C7

G3 HOT

PP3V42_G3H
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=3.425V

=PP3V42_G3H_REG (63D1)
=PP3V42_G3H_SMCVREF — 46C8
=PP3V42_G3H_SMBUS_SMC_BSA — 27C3
=PP3V42_G3H_PWRCTL — 63B8 63C8
=PP3V42_G3H_LIDSWITCH — 65A8
(LPC DEBUG BOARD) =PP3V42_G3H_LPCPLUS — 5D2 47C6
=PP3V42_G3H_SB_RTC — 26D6
=PP3V42_G3H_ACIN — 65C4 65C8 66A5
(SMC 32.768KHz OSC) =PP3V42_G3H_SMC_CLK — 46A8
(SMC 3.3V PWR) =PP3V42_G3H_SMC — 45D2 45D3 46D1 46D5 46D8 48C8

PBUS HOT

PPBUSB_G3H
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.3MM
VOLTAGE=12.6V

=PPBUSA_G3H (66C2)
(INVERTER PBUS PWR)
(ISL6262 VIN)
(LTC3728 VIN) =PPBUS_S5_INV — 67D4
=PPVIN_S5_IMVP6 — 48C7 58C2 58D5 58D8
=PPVIN_S5_1V51V05S0 — 62D8

=PPBUSB_G3H (66C2)
(LTC3728 VIN) =PPVIN_S5_5V3V3S5 — 59D8 63B7
(ISL6269 VIN) =PPVIN_S5_1V8S3 — 61C7
(FIREWIRE PORT PBUS PWR) =PPBUS_S5_FWPWRSW — 39D6
(YUKON POWER CONTROL) =PPBUS_S5_YUKON_CTRL — 60C8

PP18V5_G3H
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=18.5V

=PP18V5_G3H_INRUSH (65D1)
(DC-IN OUTPUT 18.5V PWR)
(CHARGER INPUT 18.5V PWR)
(SMC INPUT 18.5V PWR) =PP18V5_G3H_CHGR — 66D8

DCIN G3HOT

PPDCIN_G3H
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.3MM
VOLTAGE=18.5V

=PPDCIN_G3H (65D3)
=PPVBATT_G3H (66B2)
=PPVIN_G3H_P3V42G3H — 63D3

GND RAILS

XW8101 SM
XW8102 SM

=GND_AUDIO_CODEC (5D1) — GND_AUDIO_CODEC — MAKE_BASE=TRUE
=GND_AUDIO_PWR (5D1) — GND_AUDIO_PWR — MAKE_BASE=TRUE

57A6 57A5 56B5 56B3 55C8 55B8 55A8 54D2 54B6 54A5 57D8 57C8 57C5 57C3 57B8 57B5 57B3 — 56C2 55D8 55D3 55C8 55C3 55B8 55B3 55A8 55A5 55A3

Power Conn / Alias

SYNC_MASTER=ENET SYNC_DATE=11/16/2005

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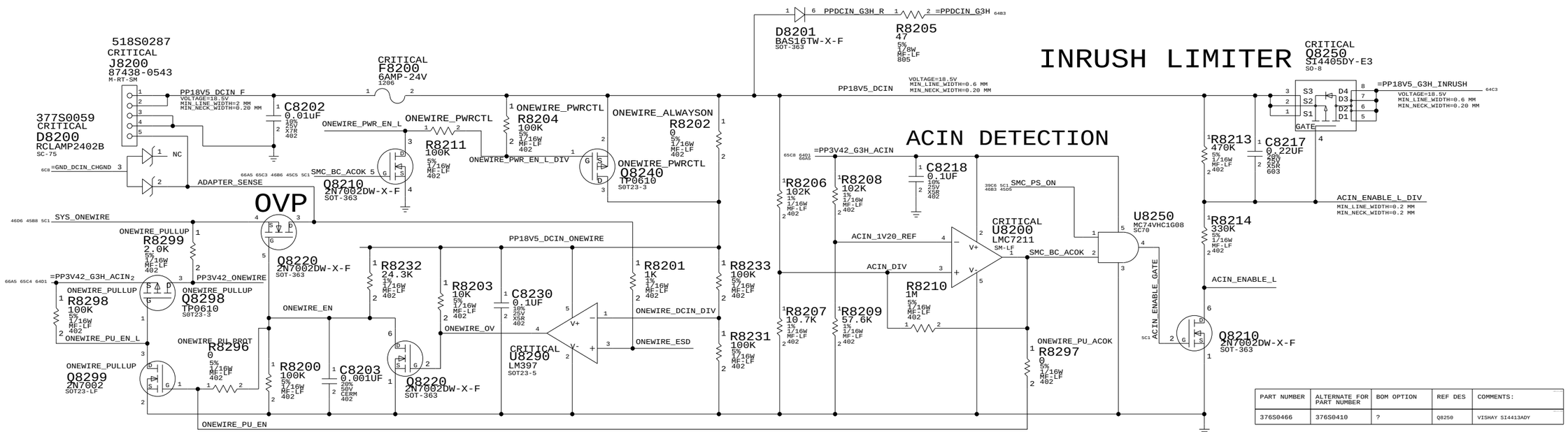
APPLE INC.

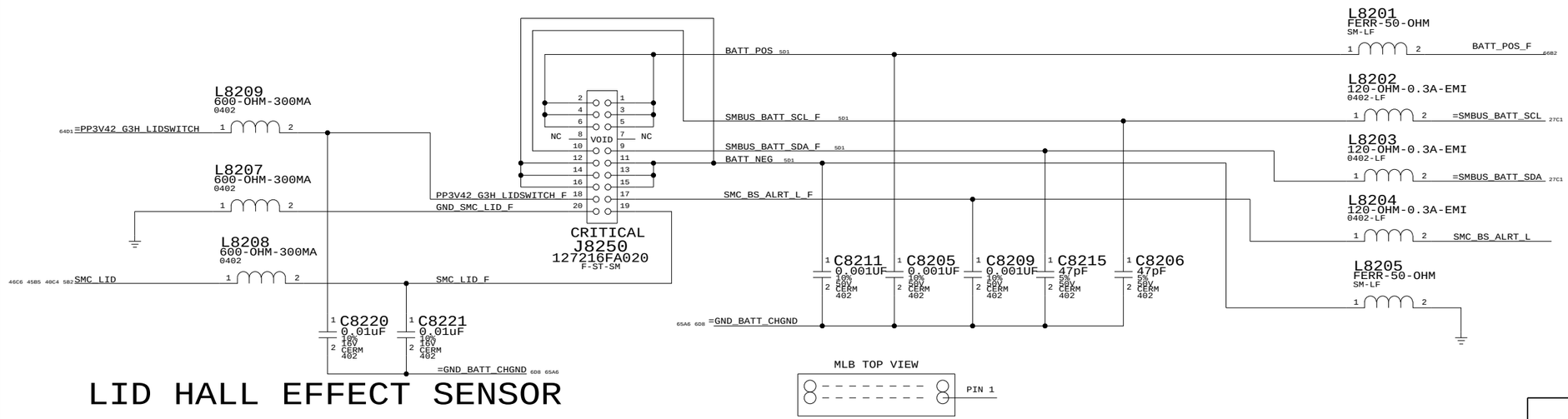
SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 81 OF 98	

DC-JACK INTERFACE



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0466	376S0410	?	Q8250	VISHAY SI4413ADY

BATTERY INTERFACE



LID HALL EFFECT SENSOR

DC-In & Battery Connectors

SYNC_MASTER=POWER SYNC_DATE=07/13/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C

SCALE	SHT	OF
NONE	82	98

PBUS SUPPLY / BATTERY CHARGER

CHLIM circuit (R8362, R8363, C8328) subject to change pending M1 resolution (100mV offset, radar 4221420)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0093	128S0092	?	C8308,C8310	KEMET T520V336M016ATE0457650
376S0466	376S0410	?	Q8300,Q8320	VISHAY SI4413ADY
376S0466	376S0410	?	Q8321	VISHAY SI4413ADY

PBUS Supply/Battery Charger

SYNC_MASTER=SMC SYNC_DATE=08/19/2005

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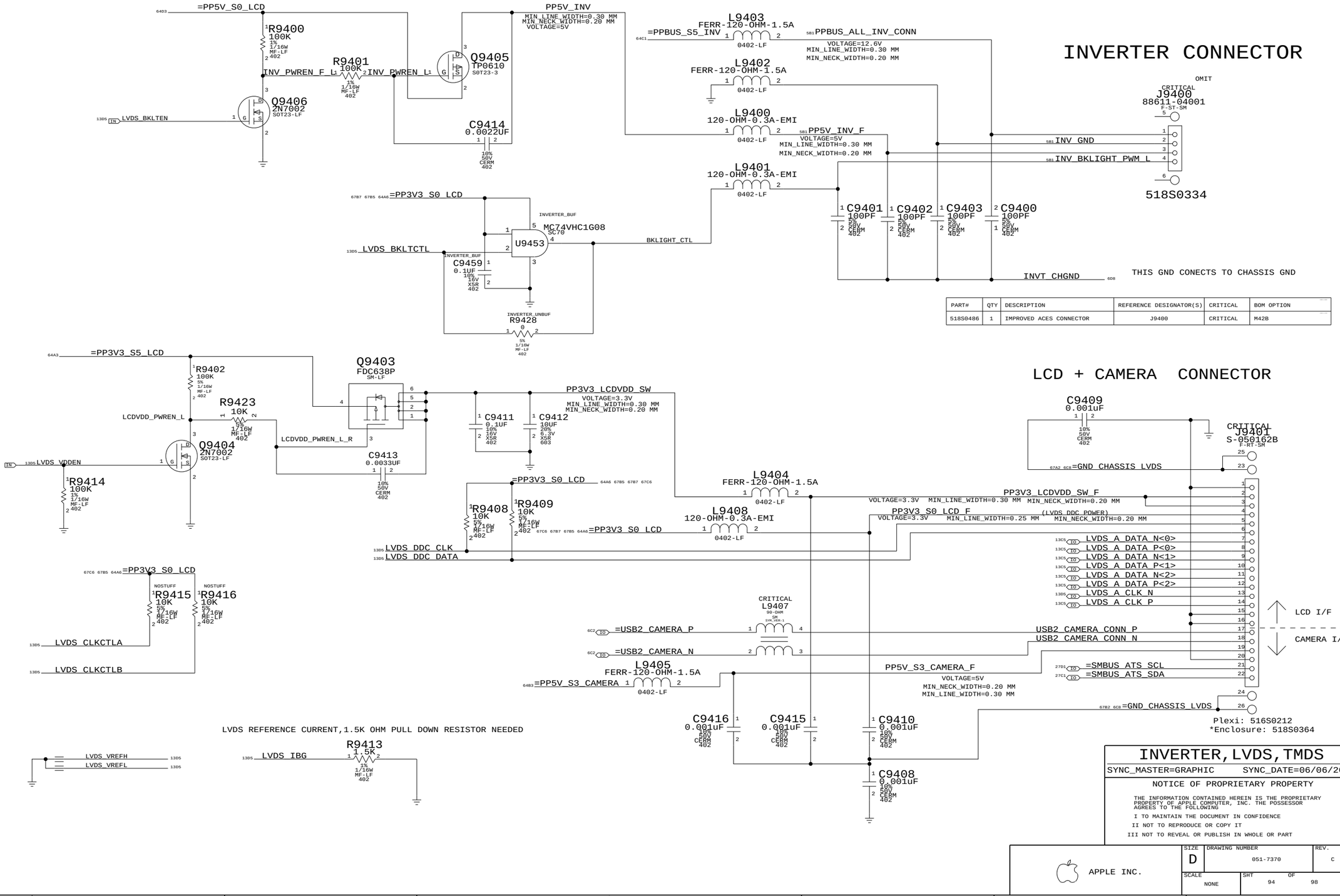
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 83 OF 98	



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
518S0486	1	IMPROVED ACES CONNECTOR	J9400	CRITICAL	M42B

INVERTER, LVDS, TMDS

SYNC_MASTER=GRAPHIC SYNC_DATE=06/06/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 94 OF 98	

L9506
120-OHM-0.3A-EMI
=PP3V3_S0_TMDS
0402-LF
PP3V3_S0_ANALOG_TMDS_F
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
C9536 0.001UF 10% 50V CERM 402
C9537 0.001UF 10% 50V CERM 402
C9538 0.1UF 10% 16V X5R 402
C9539 0.1UF 10% 16V X5R 402
C9540 10UF 20% 6.3V X5R 603
ONE 0.1UF AND 0.001UF FOR EACH PIN

L9501
120-OHM-0.3A-EMI
=PP1V8_S0_TMDS
0402-LF
PP1V8_S0_TMDS_F
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
C9507 0.1UF 10% 16V X5R 402
C9508 0.001UF 10% 50V CERM 402
C9509 0.1UF 10% 16V X5R 402
C9510 0.001UF 10% 50V CERM 402
C9511 0.1UF 10% 16V X5R 402
C9512 0.001UF 10% 50V CERM 402
C9513 10UF 20% 6.3V X5R 603
ONE 0.1UF AND 0.001UF FOR EACH PIN

L9503
120-OHM-0.3A-EMI
=PP3V3_S0_TMDS
0402-LF
PP3V3_S0_ANALOG_SDVO_F
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.25MM
C9530 0.001UF 10% 50V CERM 402
C9531 0.1UF 10% 16V X5R 402
C9514 0.1UF 10% 16V X5R 402

L9500
120-OHM-0.3A-EMI
=PP1V8_S0_TMDS
0402-LF
PP1V8_S0_ANALOG_SDVO_F
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
C9500 0.001UF 10% 50V CERM 402
C9501 0.001UF 10% 50V CERM 402
C9502 0.1UF 10% 16V X5R 402
C9503 0.1UF 10% 16V X5R 402
C9504 10UF 20% 6.3V X5R 603
ONE 0.1UF AND 0.001UF FOR EACH PIN

L9504
120-OHM-0.3A-EMI
=PP3V3_S0_TMDS
0402-LF
PP3V3_S0_PVCC1_TMDS_F
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.25MM
C9532 0.001UF 10% 50V CERM 402
C9533 0.1UF 10% 16V X5R 402
C9506 0.1UF 10% 16V X5R 402

L9505
120-OHM-0.3A-EMI
=PP3V3_S0_TMDS
0402-LF
PP3V3_S0_PVCC2_TMDS_F
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.25MM
C9534 0.001UF 10% 50V CERM 402
C9535 0.1UF 10% 16V X5R 402

R9507 49.9 1% 1/10W MF-LF 402
R9537 49.9 1% 1/10W MF-LF 402
TMDS_TX_P<0> TMDS_TX<0> TMDS_TX_N<0>
C9522 0.001UF 10% 50V CERM 402

R9508 49.9 1% 1/10W MF-LF 402
R9538 49.9 1% 1/10W MF-LF 402
TMDS_TX_P<1> TMDS_TX<1> TMDS_TX_N<1>
C9523 0.001UF 10% 50V CERM 402

R9509 49.9 1% 1/10W MF-LF 402
R9539 49.9 1% 1/10W MF-LF 402
TMDS_TX_P<2> TMDS_TX<2> TMDS_TX_N<2>
C9524 0.001UF 10% 50V CERM 402

R9510 49.9 1% 1/10W MF-LF 402
R9540 49.9 1% 1/10W MF-LF 402
TMDS_TX_CLK_P TMDS_TX_CLK TMDS_TX_CLK_N
NOSTUFF
C9526 10pF 5% 50V CERM 402
C9525 0.001UF 10% 50V CERM 402
NOSTUFF
C9527 10pF 5% 50V CERM 402

C9526,C9527 close to CHIP

MCH SDVO CHANNEL R,G,B,CLK SIGNAL TO TMDS CHIP
PLACE THE CAP NEAR THE NB SIDE

PEG_R2D_C_P<0>
PEG_R2D_C_N<0>
PEG_R2D_C_P<1>
PEG_R2D_C_N<1>
PEG_R2D_C_P<2>
PEG_R2D_C_N<2>
PEG_R2D_C_P<3>
PEG_R2D_C_N<3>

C9541 0.1UF 10% 16V X5R 402
C9542 0.1UF 10% 16V X5R 402
C9543 0.1UF 10% 16V X5R 402
C9544 0.1UF 10% 16V X5R 402
C9545 0.1UF 10% 16V X5R 402
C9546 0.1UF 10% 16V X5R 402
C9547 0.1UF 10% 16V X5R 402
C9548 0.1UF 10% 16V X5R 402

PP3V3_S0_ANALOG_SDVO_F
PP1V8_S0_ANALOG_SDVO_F
PP3V3_S0_PVCC2_TMDS_F
PP3V3_S0_PVCC1_TMDS_F
PP3V3_S0_ANALOG_TMDS_F
PP1V8_S0_TMDS_F

=PP3V3_S0_TMDS
C9521 0.1UF 10% 16V X5R 402
C9505 10UF 20% 6.3V X5R 603

CRITICAL
U9500
SIL1362ACLU
LQFP

TMDS_SDR_P TMDS_SDR_N TMDS_SDG_P TMDS_SDG_N TMDS_SDB_P TMDS_SDB_N TMDS_SDC_P TMDS_SDC_N
SDVO RCVR CORE
DIFF SIG DATA
TX0_P TX0_N TX1_P TX1_N TX2_P TX2_N TXC_P TXC_N
TMDS_TX_P<0> TMDS_TX_N<0> TMDS_TX_P<1> TMDS_TX_N<1> TMDS_TX_P<2> TMDS_TX_N<2> TMDS_TX_CLK_P TMDS_TX_CLK_N
EXT_SWING
TMDS_EXT_SWING
PP3V3_S0_ANALOG_TMDS_F
R9504 249 1% 1/16W MF-LF 402

PLACE IT CLOSE TO CONNECTOR
=PP5V_S0_TMDS
D9500 BAV99DW-X-F SOT-363
=PP2V5_S0_TMDS
R9501 3.3K 5% 1/16W MF-LF 402
R9502 3.3K 5% 1/16W MF-LF 402
C9519 0.1UF 10% 16V X5R 402
C9520 0.1UF 10% 16V X5R 402
PEG_D2R_P<1>
PEG_D2R_N<1>
TMDS_INT_P
TMDS_INT_N
TMDS CHIP SDVO INPUT INTERRUPT SIGNAL TO MCH
TMDS_EXT_RES
TMDS_RST_L
SDVO_CTRLCLK
SDVO_CTRLDATA
R9500 2.2K 5% 1/16W MF-LF 402
TMDS_HTPLG
TMDS_HTPLG_R
R9503 1K 5% 1/16W MF-LF 402
I2C MASTER INTER
CONFIG/ PRGRM
TEXT MODE
TMDS_I2C_SCL
TMDS_I2C_SDA
R9505 10K 5% 1/16W MF-LF 402
R9506 10K 5% 1/16W MF-LF 402
=PP3V3_S0_TMDS
TMDS_I2C_SCL AND TMDS_I2C_SDA DON'T NEED TO CONNECT

NC
D9500 BAV99DW-X-F SOT-363
PP5V_S0_DVIPORT
PP5V_S0_DVIPORT_D

EXTERNAL TMDS

SYNC_MASTER=GRAPHIC SYNC_DATE=06/06/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 95 OF 98	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0227	155S0164	?	L9805,L9806,L9807	KEEP MAG.LAYER IN BOM

Video Connectors

EXTERNAL VIDEO (VGA) INTERFACE

Isolation required for DVI power switch

TMDS(MINI DVI) INTERFACE

PLACE THE RESISTOR CLOSE TO GMCH AND THE CAP NEAR CONNECTOR

A 255 OHM 1% RESISTOR IS REQUIRED BETWEEN CRT_IREF AND GROUND

TV REFERENCE CURRENT,USES AN EXTERNAL RESISTOR OF 5K OHM 1% TO SET INTERNAL VOLTAGE LEVELS

DVI power DIODE on page 95 (D9500)

PLACE THE RESISTOR CLOSE TO GMCH

PLACE THE RESISTOR CLOSE TO GMCH AND THE CAP NEAR THE CONNECTOR

PLACE THE RESISTOR CLOSE TO GMCH

PLACE THE RESISTOR CLOSE TO GMCH

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0292	1	CONN,32P MINI-DVI RCPT,RA,MG3,LF	J9801	CRITICAL	NORMAL
514-0319	1	CONN,32P MINI-DVI RCPT,RA,BLACK,LF	J9801	CRITICAL	FANCY

MINI-DVI CONNECTOR

SYNC_MASTER=EUGENE SYNC_DATE=05/21/05

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SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 98 OF 98	