1. ALL RESISTANCE VALUES ARE IN OHM, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.
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CPU THERMAL SENSOR

NOTE: SYMBOL SHOULD BE ADT7461A

NOTE: CPU THERMAL SENSOR TEMPORARILY REMOVED BOMOPTION=CPU_TSENS_EXT

ROUTE ON SAME LAYER WITH 0.254MM TRACE WIDTH & SPACING.
ADD GND GUARD TRACES FOR CPU_THERMD_P/N

THERM_DX_P = SMB_THRM_DATA
THERM_DX_N = SMB_THRM_CLK
THRM_ALERT_L = PM_THRM_L
THRM_THM = THERM_DX_P
THRM_DX_N

LAYOUT NOTE:
PLACE R1017 AND R1019 SUCH THAT THEY SHARE ONE PAD
PLACE R1002 AND R1018 SUCH THAT THEY SHARE ONE PAD

TEMPERATURE SENSORS MONITORCPU_TSENS_Int

ADD 1/16W 10K MF-LF 5%

CPU_TEMP SENSOR

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CPU ITP700FLEX DEBUG SUPPORT

ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S TCK PIN AND THEN FUSE BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX CONNECTOR'S FBO PIN.
NCTF balls are Not Critical To Function
These connections can break without affecting part performance. Only

Layout Note:
C1613 0.47uF
402 20%

Layout Note:
VCC_NCTF70
VCC_NCTF69
VCC_NCTF65
VCC_NCTF62
VCC_NCTF61
VCC_NCTF58
VCC_NCTF56
VCC_NCTF54
VCC_NCTF51
VCC_NCTF49
VCC_NCTF48
VCC_NCTF47
VCC_NCTF45
VCC_NCTF44
VCC_NCTF40
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VCC_NCTF10
VCC_NCTF9
VCC_NCTF8
VCC_NCTF6
VCC_NCTF5
VCC_NCTF3
VCC_NCTF2
VCC_NCTF1
VSS_NCTF11
VSS_NCTF8
VSS_NCTF7
VSS_NCTF1
VSS_NCTF0

SCALE

NB Power 1

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DRAWING NUMBER
SYNC_DATE=MASTER
- BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
- LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR
- INTERNAL 20K PD

NOTE: EE_CS HAS INTERNAL PD, ONLY ENABLED WHEN LAN_RST#=L

NOTE: ALL IDE PINS HAVE INTERNAL 33-OHM SERIES R'S

NOTE: ENABLE INTERNAL 1.05V SUSPEND REG

NOTE: KEYBOARD CONTROLLER RESET CPU

NOTE: DD<7> HAS INTERNAL 11.5K PD

NOTE: RISING-EDGE TRIGGERED AT CPU

NOTE: CPU_PWRGD

NOTE: PULLED UP PER INTEL

NOTE: LDRQ<0-1># HAVE INTERNAL 20K PU

NOTE: DD<7> HAS INTERNAL 11.5K PD

NOTE: NOSTUFF

NOTE: SCALE

NOTE: BOM CONSOLIDATION

NOTE: CHANGED TO 54.9 FOR R2107 TO BE CHANGED TO 54.9 FOR

NOTE: KEYBOARD CONTROLLER RESET CPU

NOTE: EE_CS HAS INTERNAL 1.05V SUSPEND REG

NOTE: INTERNAL 20K PD

NOTE: DD<7> HAS INTERNAL 11.5K PD

NOTE: SCALE

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SB I2C BUSSES

PCI CONTROL

SB: SMB HUB AND ALIAS

R2729

R2728

R2729

R2728

TP_PCI_GNT3_L

PCI_GNT3_L

PCI_GNT1_L

PCI_REQ3_L

CHIPSEL

R2719

R2718

R2719

R2718

PCI_GNT1_L

MAKE_BASE=TRUE

PCI_FW_GNT_L

NO_TEST=TRUE

PCI_FW_REQ_L

MAKE_BASE=TRUE

PCI_REQ1_L

MAKE_BASE=TRUE

SMB_CLK

SMB_DATA

=PP3V3_S0_SB_GPIO

=PP3V3_S5_SB_IO

SMB_CLK

SMB_DATA

=SMB_AIRPORT_DATA

=SMB_AIRPORT_CLK

SMB_CK410_DATA

SMB_CK410_CLK

27 23

27 23

29 28

29 28

53

53

33

33

22

22

26 22

44

44

27 23

27 23

26

22

480x8 www.vinafix.vn
Use a cap for each side of every NPN, one cap for every two discrete resistors.

Memorial shown at the top of each group applies to every part below it.
Can 5V be S0 if 1V8 is S3?

If power inputs are not S0, MEMVTT_EN can be used to disable MEMVTT in sleep.

- =PP0V9_S0_MEMVTT_LDO
- =PP1V8_S0_MEMVTT
- =PP5V_S0_MEMVTT

BOM options provided by this page:
- (NONE)

Power aliases required by this page:
- (NONE)

Signal aliases required by this page:
- (NONE)

APPENDIX

SYNC_DATE=MASTER
SYNC_MASTER=MASTER

Apple Computer Inc.

051-7032  77

D  31°  97

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REV.

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FAN 2

HD TEMP SENSOR

ODD TEMP SENSOR

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