1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

M50 - DVT

04/05/06

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
13		405954	ENGINEERING RELEASED	10/18/05	06/22/04

PDF	CSA	CONTENTS	SYNC MASTER	DATE
2	2	System Block Diagram	MASTER	MASTER
3	3	Power Block Diagram	MASTER	MASTER
4	4	Table Items	MASTER	MASTER
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6	6	Power Conn / Alias	MASTER	MASTER
7	7	CPU 1 OF 2-FSB	MASTER	MASTER
8	8	CPU 2 OF 2-PWR/GND	MASTER	MASTER
9	9	CPU DECAPS & VID<>	MASTER	MASTER
10	10	CPU TEMP SENSOR	MASTER	MASTER
11	11	CPU ITP700FLEX DEBUG	M38	01/05/2006
12	12	NB CPU Interface	M1	01/05/2006
13	13	NB PEG / Video Interfaces	M1	01/05/2006
14	14	NB Misc Interfaces	MASTER	MASTER
15	15	NB DDR2 Interfaces	M1	01/05/2006
16	16	NB Power 1	MASTER	MASTER
17	17	NB Power 2	M40	01/05/2006
18	18	NB Grounds	M1	01/05/2006
19	19	NB (GM) Decoupling	(MASTER)	(MASTER)
20	20	NB Config Straps	M1	01/05/2006
21	21	SB: 1 OF 4	M38	01/05/2006
22	22	SB: 2 OF 4	MASTER	MASTER
23	23	SB: 3 OF 4	MASTER	MASTER
24	24	SB: 4 OF 4	M38	01/05/2006
25	25	SB:DECOUPLING	MASTER	MASTER
26	26	SB: MISC	MASTER	MASTER
27	27	SB: SMB HUB AND ALIAS	MASTER	MASTER
28	28	DDR2 SO-DIMM Connector A	MASTER	MASTER
29	29	DDR2 SO-DIMM Connector B	MASTER	MASTER
30	30	Memory Active Termination	MASTER	MASTER
31	31	Memory Vtt Supply	MASTER	MASTER
32	33	CLOCKS	MASTER	MASTER
33	34	CLOCKS: TERMINATIONS	MASTER	MASTER
34	38	Disk Connectors	MASTER	MASTER
35	41	ETHERNET CONTROLLER	MASTER	MASTER
36	42	ETHERNET MISC	MASTER	MASTER
37	43	ETHERNET CONNECTOR	MASTER	MASTER

PDF	CSA	CONTENTS	SYNC MASTER	DATE
38	44	FW: FW323-06	MASTER	MASTER
39	45	FW: DECAPS	MASTER	MASTER
40	46	FIREWIRE CONNECTORS	MASTER	MASTER
41	47	USB Device Interfaces	MASTER	MASTER
42	53	AIRPORT CONN	MASTER	MASTER
43	54	PCIE PORT ALIASES	MASTER	MASTER
44	58	SMC	M1	01/05/2006
45	59	SMC & TPM SUPPORT	(MASTER)	(MASTER)
46	60	LPC+ CONN	M38	12/09/2005
47	61	NB THERMAL	MASTER	MASTER
48	63	SPI BOOTROM	M38	01/05/2006
49	65	Fan 0, 1 & System Temp	MASTER	MASTER
50	66	Fan 2 & HD Temp	MASTER	MASTER
51	67	TPM	M38	01/05/2006
52	68	AUDIO: CODEC	AUDIO	03/30/2006
53	72	AUDIO: SPEAKER AMP	AUDIO	03/30/2006
54	73	AUDIO: CONNECTORS	AUDIO	03/30/2006
55	74	AUDIO: POWER SUPPLIES	AUDIO	03/30/2006
56	75	IMVP6 CPU VCore Regulator	MASTER	MASTER
57	76	CPU & SYSTEM SENSE CIRCUITRY	(MASTER)	(MASTER)
58	77	PWR GOOD	(MASTER)	(MASTER)
59	78	3V DC/DC 2.5V	(MASTER)	(MASTER)
60	79	1.8V & 1.2V VREG	MASTER	MASTER
61	80	1.5V_S0 & 1.05V_S0 VREG	MASTER	MASTER
62	82	5V DC/DC	MASTER	MASTER
63	83	S0 AND S3 FETS	MASTER	MASTER
64	94	Internal Display Conns	MASTER	MASTER
65	95	EXTERNAL TMDS	MASTER	MASTER
66	96	TMDS/Inverter/ExtVGA	MASTER	MASTER
67	97	External Display Conns	MASTER	MASTER

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING
THIRD ANGLE PROJECTION

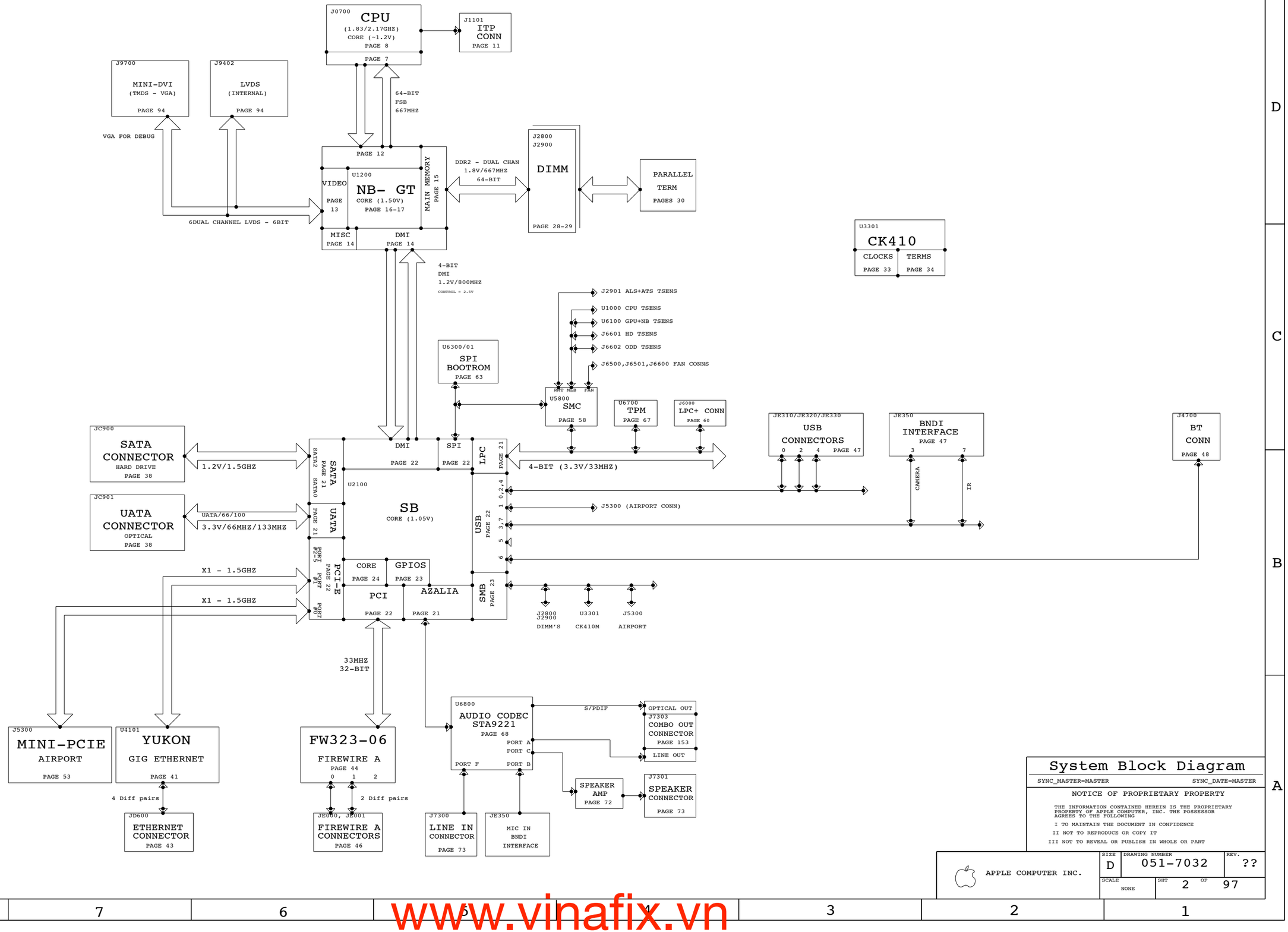
METRIC

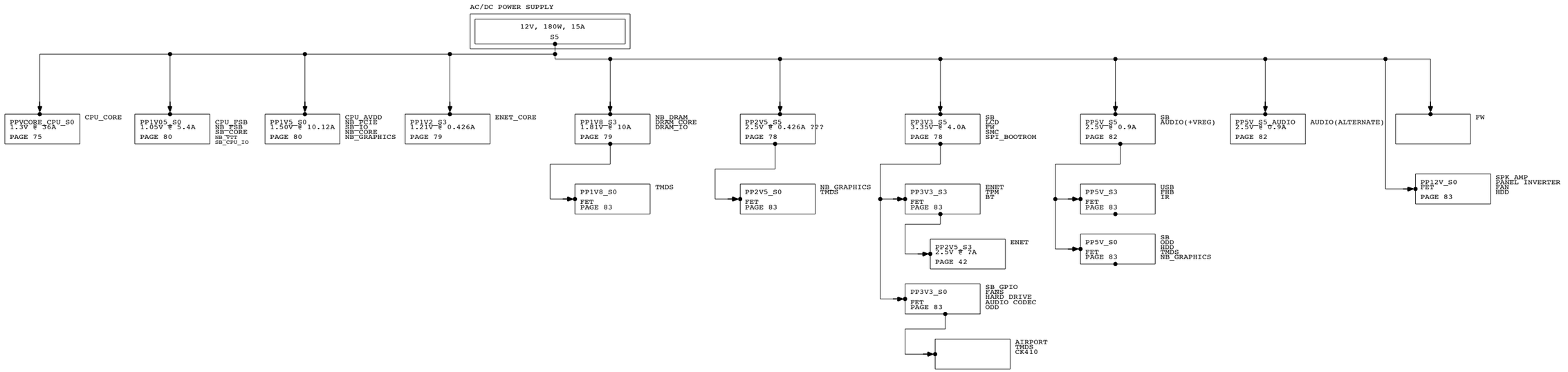
DRAFTER / DESIGN CK
ENG APPD / MFG APPD
QA APPD / DESIGNER
RELEASE / SCALE NONE
MATERIAL/FINISH NOTED AS APPLICABLE
SIZE D

Apple Computer Inc.

TITLE
SCHEM VALLCO

DRAWING NUMBER 051-7032 REV. ??
SHT 1 OF 97





Power Block Diagram

SYNC_MASTER=MASTER SYNC_DATE=MASTER

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7032	??

SCALE	SHT	OF
NONE	3	97

COMMON

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
	511S0025	1	IC,CPU-SKT,479BGA	J0700	CRITICAL	
	338S0298	1	IC,945GT,NORTHBRIDGE	U1200	CRITICAL	
	343S0385	1	IC,SB,652BGA	U2100	CRITICAL	
	742-0048	1	BAT,COIN,3V,220MAH,CR2032	BT2600	CRITICAL	
	359S0101	1	IC,CY28445-5,CLK GEN,68PIN QFN	U3301	CRITICAL	
	338S0270	1	IC,88E8053,GIGABIT ENET XCVR,64P QFN,NO	U4101	CRITICAL	
(335S0382)	341S1797	1	IC,ENET LAN ROM	U4102	CRITICAL	
	338S0279	1	IC,FW32306,1394A LINK,TQFP	U4400	CRITICAL	
338S0274	341T0022	1	IC,SMC,M50	U5800	CRITICAL	
	341S1789	1	IC,TPM,TSSOP,28P	U6700	CRITICAL	LEMENU
	353S1235	1	IC,CPU VREG,IMVP,TWO PHASE	U7500	CRITICAL	

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
	051-7032	1	PCB,SCHEM,MLB,M50	SCH1		
	820-1960	1	PCB,FAB,MLB,M50	MLB1		
(335S0384)	341T0021	1	EFI ROM,M50	U6301	CRITICAL	
	337S3244	1	M50 1.66G CPU (C0)	CPU	CRITICAL	YONAH
	337S3242	1	M38 CPU (C0)	CPU	CRITICAL	MEROM

341S1859 IC EFI BOOTROM DEV M50
337S3242 M38 CPU(C0)
337S3280 M50 1.83G LOW SPEED CPU (D0)

OPS REQUESTED QUAL PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
155S0295	1	CHOKE,COMMON_MODE,165OHM,4PIN	L9703	CRITICAL	
124-0359	3	PCAP,120UF,16V,20%,ELEC	C6505,C6504,C6602	CRITICAL	

ALTERNATE PARTS

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
126S0091	126S0092		C625	FACTORY SHORTAGE
353S1381	353S1278		U5940	SMC VREF
378S0140	378S0141		LED401,LED402,LED403	

MECHANICAL PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
603-9187	1	SUBASSY, M50 NB HEATSINK	HS2	CRITICAL	
603-9186	1	SUBASSY, M50 CPU HEATSINK	HS1	CRITICAL	
725-0668	1	MYLAR WASHER	WASH1	CRITICAL	
725-0720	1	MYLAR BLACK LED CVR, M50	CVR1	CRITICAL	
825-6447	1	BARCODE LABEL, M50	[EEE:V3M]	CRITICAL	

Table Items

SYNC_MASTER=MASTER SYNC_DATE=MASTER

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7032	??

SCALE NONE SHT 4 OF 97

LAYOUT NOTE: PLACE NEAR J0700

12 7 5	FSB_A_L<6>	PP600	OMIT P4MM
12 7 5	FSB_ADSTB_L<0>	PP601	OMIT P4MM
12 7 5	FSB_A_L<27>	PP602	OMIT P4MM
12 7 5	FSB_ADSTB_L<1>	PP603	OMIT P4MM
12 7 5	FSB_D_L<0>	PP604	OMIT P4MM
12 7 5	FSB_DSTBN_L<0>	PP605	OMIT P4MM
12 7 5	FSB_DSTBP_L<0>	PP606	OMIT P4MM
12 7 5	FSB_DINV_L<0>	PP607	OMIT P4MM
12 7 5	FSB_D_L<16>	PP608	OMIT P4MM
12 7 5	FSB_DSTBN_L<1>	PP609	OMIT P4MM
12 7 5	FSB_DSTBP_L<1>	PP610	OMIT P4MM
12 7 5	FSB_DINV_L<1>	PP611	OMIT P4MM
12 7 5	FSB_D_L<41>	PP612	OMIT P4MM
12 7 5	FSB_DSTBN_L<2>	PP613	OMIT P4MM
12 7 5	FSB_DSTBP_L<2>	PP614	OMIT P4MM
12 7 5	FSB_DINV_L<2>	PP615	OMIT P4MM
12 7 5	FSB_D_L<59>	PP616	OMIT P4MM
12 7 5	FSB_DSTBN_L<3>	PP617	OMIT P4MM
12 7 5	FSB_DSTBP_L<3>	PP618	OMIT P4MM
12 7 5	FSB_DINV_L<3>	PP619	OMIT P4MM
12 7 5	FSB_LOCK_L	PP620	OMIT P4MM
12 11 7	FSB_CPURST_L	PP621	OMIT P4MM
21 7	CPU_INIT_L	PP622	OMIT P4MM
21 7	CPU_A20M_L	PP623	OMIT P4MM
21 7	CPU_IGNNE_L	PP624	OMIT P4MM
21 7	CPU_STPCLK_L	PP625	OMIT P4MM
21 7	CPU_INTR	PP626	OMIT P4MM
21 7	CPU_NMI	PP627	OMIT P4MM
21 7	CPU_SMI_L	PP628	OMIT P4MM
34 7	FSB_CLK_CPU_P	PP629	OMIT P4MM
34 7	FSB_CLK_CPU_N	PP630	OMIT P4MM

LAYOUT NOTE: PLACE NEAR U2100

34 21	SB_CLK100M_SATA_P	PP6C4	OMIT P4MM
34 21	SB_CLK100M_SATA_N	PP6C5	OMIT P4MM
38 21	IDE_PDIOR_L	PP6C6	OMIT P4MM
38 21	IDE_PDIORDY	PP6C7	OMIT P4MM
38 21	IDE_PDD<9>	PP6C8	OMIT P4MM
34 22	PCI_CLK_SB	PP6D0	OMIT P4MM
54 22	PCIE_A_D2R_P	PP6D1	OMIT P4MM
54 22	PCIE_A_D2R_N	PP6D2	OMIT P4MM
54 22	PCIE_B_D2R_P	PP5E1	OMIT P4MM
54 22	PCIE_B_D2R_N	PP5E2	OMIT P4MM
22 14	DMI_N2S_P<0>	PP6D3	OMIT P4MM
22 14	DMI_N2S_N<0>	PP6D4	OMIT P4MM
34 22	SB_CLK100M_DMI_P	PP6D5	OMIT P4MM
34 22	SB_CLK100M_DMI_N	PP6D6	OMIT P4MM
58 26 23	PM_SYSRST_L	PP6D7	OMIT P4MM
58 44 23 47 60	PM_CLKRUN_L	PP6D8	OMIT P4MM
34 23	SB_CLK14P3M_TIMER	PP6D9	OMIT P4MM
34 23	SB_CLK48M_USBCTLR	PP6E0	OMIT P4MM

LAYOUT NOTE: PLACE NEAR U1200

12 7 5	FSB_A_L<6>	PP631	OMIT P4MM
12 7 5	FSB_ADSTB_L<0>	PP632	OMIT P4MM
12 7 5	FSB_A_L<27>	PP633	OMIT P4MM
12 7 5	FSB_ADSTB_L<1>	PP634	OMIT P4MM
12 7 5	FSB_D_L<0>	PP635	OMIT P4MM
12 7 5	FSB_DSTBN_L<0>	PP636	OMIT P4MM
12 7 5	FSB_DSTBP_L<0>	PP637	OMIT P4MM
12 7 5	FSB_DINV_L<0>	PP638	OMIT P4MM
12 7 5	FSB_D_L<16>	PP639	OMIT P4MM
12 7 5	FSB_DSTBN_L<1>	PP640	OMIT P4MM
12 7 5	FSB_DSTBP_L<1>	PP641	OMIT P4MM
12 7 5	FSB_DINV_L<1>	PP642	OMIT P4MM
12 7 5	FSB_D_L<41>	PP643	OMIT P4MM
12 7 5	FSB_DSTBN_L<2>	PP644	OMIT P4MM
12 7 5	FSB_DSTBP_L<2>	PP645	OMIT P4MM
12 7 5	FSB_DINV_L<2>	PP646	OMIT P4MM
12 7 5	FSB_D_L<59>	PP647	OMIT P4MM
12 7 5	FSB_DSTBN_L<3>	PP648	OMIT P4MM
12 7 5	FSB_DSTBP_L<3>	PP649	OMIT P4MM
12 7 5	FSB_DINV_L<3>	PP650	OMIT P4MM
12 7 5	FSB_LOCK_L	PP651	OMIT P4MM
12 7	FSB_HIT_L	PP652	OMIT P4MM
12 7	FSB_HITM_L	PP653	OMIT P4MM
12 7	FSB_BNR_L	PP654	OMIT P4MM
12 7	FSB_BREQ0_L	PP655	OMIT P4MM
12 7	FSB_DBSY_L	PP656	OMIT P4MM
12 7	FSB_DPWR_L	PP657	OMIT P4MM
12 7	FSB_REQ_L<0>	PP658	OMIT P4MM
12 7	FSB_REQ_L<1>	PP659	OMIT P4MM
12 7	FSB_REQ_L<2>	PP660	OMIT P4MM
12 7	FSB_REQ_L<3>	PP661	OMIT P4MM
12 7	FSB_REQ_L<4>	PP662	OMIT P4MM
34 12	FSB_CLK_NB_P	PP663	OMIT P4MM
34 12	FSB_CLK_NB_N	PP664	OMIT P4MM
75 26 14	VR_PWRGOOD_DELAY	PP665	OMIT P4MM
14	NB_RST_IN_L_R	PP666	OMIT P4MM
34 14	NB_CLK100M_GCLKIN_P	PP667	OMIT P4MM
34 14	NB_CLK100M_GCLKIN_N	PP668	OMIT P4MM
34 14	NB_CLK_DREFSSCLKIN_P	PP669	OMIT P4MM
34 14	NB_CLK_DREFSSCLKIN_N	PP670	OMIT P4MM
34 14	NB_CLK_DREFCLKIN_P	PP671	OMIT P4MM
34 14	NB_CLK_DREFCLKIN_N	PP672	OMIT P4MM
22 14	DMI_S2N_N<0>	PP673	OMIT P4MM
22 14	DMI_S2N_P<0>	PP674	OMIT P4MM
19 14	MEM_VREF_NB_0	PP6E1	OMIT P4MM
19 14	MEM_VREF_NB_1	PP675	OMIT P4MM
28 15	MEM_A_DQ<7>	PP676	OMIT P4MM
28 15	MEM_A_DQ<14>	PP677	OMIT P4MM
28 15	MEM_A_DQ<16>	PP678	OMIT P4MM
28 15	MEM_A_DQ<25>	PP679	OMIT P4MM
28 15	MEM_A_DQ<39>	PP680	OMIT P4MM
28 15	MEM_A_DQ<47>	PP681	OMIT P4MM
28 15	MEM_A_DQ<54>	PP682	OMIT P4MM
28 15	MEM_A_DQ<59>	PP683	OMIT P4MM
28 15	MEM_A_DQS_P<0>	PP684	OMIT P4MM
28 15	MEM_A_DQS_N<0>	PP685	OMIT P4MM
28 15	MEM_A_DQS_P<1>	PP686	OMIT P4MM
28 15	MEM_A_DQS_N<1>	PP687	OMIT P4MM
28 15	MEM_A_DQS_P<2>	PP688	OMIT P4MM
28 15	MEM_A_DQS_N<2>	PP689	OMIT P4MM
28 15	MEM_A_DQS_P<3>	PP690	OMIT P4MM
28 15	MEM_A_DQS_N<3>	PP691	OMIT P4MM
28 15	MEM_A_DQS_P<4>	PP692	OMIT P4MM
28 15	MEM_A_DQS_N<4>	PP693	OMIT P4MM
28 15	MEM_A_DQS_P<5>	PP694	OMIT P4MM
28 15	MEM_A_DQS_N<5>	PP695	OMIT P4MM
28 15	MEM_A_DQS_P<6>	PP696	OMIT P4MM
28 15	MEM_A_DQS_N<6>	PP697	OMIT P4MM
28 15	MEM_A_DQS_P<7>	PP698	OMIT P4MM
28 15	MEM_A_DQS_N<7>	PP699	OMIT P4MM
29 15	MEM_B_DQ<6>	PP6A0	OMIT P4MM
29 15	MEM_B_DQ<8>	PP6A1	OMIT P4MM
29 15	MEM_B_DQ<23>	PP6A2	OMIT P4MM
29 15	MEM_B_DQ<25>	PP6A3	OMIT P4MM
29 15	MEM_B_DQ<38>	PP6A4	OMIT P4MM
29 15	MEM_B_DQ<44>	PP6A5	OMIT P4MM
29 15	MEM_B_DQ<48>	PP6A6	OMIT P4MM
29 15	MEM_B_DQ<62>	PP6A7	OMIT P4MM
29 15	MEM_B_DQS_P<0>	PP6A8	OMIT P4MM
29 15	MEM_B_DQS_N<0>	PP6A9	OMIT P4MM
29 15	MEM_B_DQS_P<1>	PP6B0	OMIT P4MM
29 15	MEM_B_DQS_N<1>	PP6B1	OMIT P4MM
29 15	MEM_B_DQS_P<2>	PP6B2	OMIT P4MM
29 15	MEM_B_DQS_N<2>	PP6B3	OMIT P4MM
29 15	MEM_B_DQS_P<3>	PP6B4	OMIT P4MM
29 15	MEM_B_DQS_N<3>	PP6B5	OMIT P4MM
29 15	MEM_B_DQS_P<4>	PP6B6	OMIT P4MM
29 15	MEM_B_DQS_N<4>	PP6B7	OMIT P4MM
29 15	MEM_B_DQS_P<5>	PP6B8	OMIT P4MM
29 15	MEM_B_DQS_N<5>	PP6B9	OMIT P4MM
29 15	MEM_B_DQS_P<6>	PP6C0	OMIT P4MM
29 15	MEM_B_DQS_N<6>	PP6C1	OMIT P4MM
29 15	MEM_B_DQS_P<7>	PP6C2	OMIT P4MM
29 15	MEM_B_DQS_N<7>	PP6C3	OMIT P4MM

LAYOUT NOTE: PLACE NEAR U4101

41 34	ENET_CLK100M_PCIE_P	PP4100	OMIT P4MM
41 34	ENET_CLK100M_PCIE_N	PP4101	OMIT P4MM

13	PEG_R2D_C_N<4>	NC_PEG_R2D_C_N<4>	NO_TEST=TRUE
13	PEG_R2D_C_N<5>	NC_PEG_R2D_C_N<5>	NO_TEST=TRUE
13	PEG_R2D_C_N<6>	NC_PEG_R2D_C_N<6>	NO_TEST=TRUE
13	PEG_R2D_C_N<7>	NC_PEG_R2D_C_N<7>	NO_TEST=TRUE
13	PEG_R2D_C_N<8>	NC_PEG_R2D_C_N<8>	NO_TEST=TRUE
13	PEG_R2D_C_N<9>	NC_PEG_R2D_C_N<9>	NO_TEST=TRUE
13	PEG_R2D_C_N<10>	NC_PEG_R2D_C_N<10>	NO_TEST=TRUE
13	PEG_R2D_C_N<11>	NC_PEG_R2D_C_N<11>	NO_TEST=TRUE
13	PEG_R2D_C_N<12>	NC_PEG_R2D_C_N<12>	NO_TEST=TRUE
13	PEG_R2D_C_N<13>	NC_PEG_R2D_C_N<13>	NO_TEST=TRUE
13	PEG_R2D_C_N<14>	NC_PEG_R2D_C_N<14>	NO_TEST=TRUE
13	PEG_R2D_C_N<15>	NC_PEG_R2D_C_N<15>	NO_TEST=TRUE
13	PEG_D2R_N<3>	NC_PEG_D2R_N<3>	NO_TEST=TRUE
13	PEG_D2R_N<4>	NC_PEG_D2R_N<4>	NO_TEST=TRUE
13	PEG_D2R_N<5>	NC_PEG_D2R_N<5>	NO_TEST=TRUE
13	PEG_D2R_N<6>	NC_PEG_D2R_N<6>	NO_TEST=TRUE
13	PEG_D2R_N<7>	NC_PEG_D2R_N<7>	NO_TEST=TRUE
13	PEG_D2R_N<8>	NC_PEG_D2R_N<8>	NO_TEST=TRUE
13	PEG_D2R_N<9>	NC_PEG_D2R_N<9>	NO_TEST=TRUE
13	PEG_D2R_N<10>	NC_PEG_D2R_N<10>	NO_TEST=TRUE
13	PEG_D2R_N<11>	NC_PEG_D2R_N<11>	NO_TEST=TRUE
13	PEG_D2R_N<12>	NC_PEG_D2R_N<12>	NO_TEST=TRUE
13	PEG_D2R_N<13>	NC_PEG_D2R_N<13>	NO_TEST=TRUE
13	PEG_D2R_N<14>	NC_PEG_D2R_N<14>	NO_TEST=TRUE
13	PEG_D2R_N<15>	NC_PEG_D2R_N<15>	NO_TEST=TRUE

SPARE USB PORT

22	USB_F_N	TP_USB_F_N	MAKE_BASE=TRUE
22	USB_F_P	TP_USB_F_P	MAKE_BASE=TRUE

INVERTER DOES NOT USE THIS SIGNAL

13	LVDS_BKLTEN	TP_LVDS_BKLTEN	MAKE_BASE=TRUE

PLACE NEAR R1210 AND R1211

12	NB_FSB_VREF	PP1200	SM-TP50-TOP
19 12 6	=PP1V05_S0_FSB_NB	PP1201	SM-TP50-TOP
		PP1202	SM-TP50-TOP

PLACE NEAR R0705 AND R0706

11 9 8 7 6	=PP1V05_S0_CPU	PP700	SM-TP50-TOP
		PP702	SM-TP50-TOP

PLACE NEAR R2800 AND R2801

29 28 6	=PP1V8_S3_MEM	PP2800	SM-TP50-TOP
29 28	MEM_VREF	PP2801	SM-TP50-TOP
		PP2802	SM-TP50-TOP

58 22	IN	SPI_ARB	NO_TEST=TRUE
34	IN	TP_PCI_CLK_SPARE	NO_TEST=TRUE
29	IN	TP_MEM_B_A<14>	NO_TEST=TRUE
29	IN	TP_MEM_B_A<15>	NO_TEST=TRUE

78 77 76 66 65 59 26 6	IN	PP3V3_S5	FUNC_TEST=TRUE
83 82 80 79 59 6	IN	PP5V_S5	FUNC_TEST=TRUE
83 82 80 79 78 77 76 6	IN	PP12V_S5	FUNC_TEST=TRUE
83 79 6	IN	PP1V8_S3	FUNC_TEST=TRUE
76 75 6	IN	PPVCORE_CPU	FUNC_TEST=TRUE
26 25 24 21	IN	PP3V3_S5_SB_RTC	FUNC_TEST=TRUE
		8 TESTPOINTS	
	IN		FUNC_TEST=TRUE

60 59 58	IN	SMC_TCK	FUNC_TEST=TRUE
60 59 58	IN	SMC_TDI	FUNC_TEST=TRUE
60 59 58	IN	SMC_TDO	FUNC_TEST=TRUE
60 59 58	IN	SMC_TMS	FUNC_TEST=TRUE
60 58	IN	SMC_TRST_L	FUNC_TEST=TRUE
60 59 58	IN	SMC_TX_L	FUNC_TEST=TRUE
60 59 58	IN	SMC_RX_L	FUNC_TEST=TRUE
59	IN	SMC_MANUAL_RST_L	FUNC_TEST=TRUE
11 7	IN	XDP_TCK	FUNC_TEST=TRUE
11 7	IN	XDP_TDI	FUNC_TEST=TRUE
11 7	IN	XDP_TDO	FUNC_TEST=TRUE
11 7	IN	XDP_TMS	FUNC_TEST=TRUE
11 7	IN	XDP_TRST_L	FUNC_TEST=TRUE
59	IN	POWER_BUTTON_L	FUNC_TEST=TRUE
26	IN	SW_RST_BTN_L	FUNC_TEST=TRUE

MISC GROUND VIAS

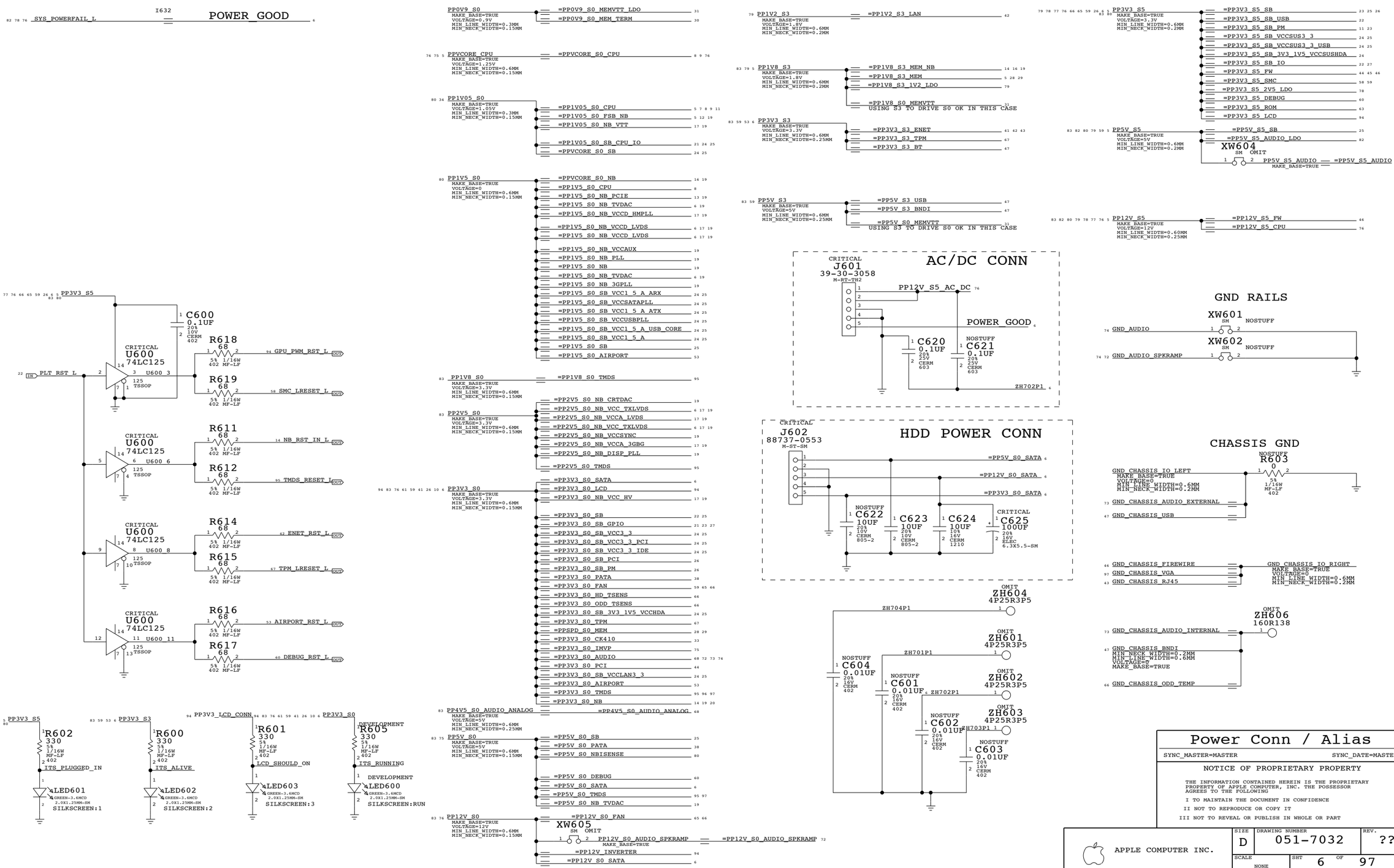
ZH500 HOLE-VIA	ZH510 HOLE-VIA	ZH520 HOLE-VIA
ZH501 HOLE-VIA	ZH511 HOLE-VIA	ZH521 HOLE-VIA
ZH502 HOLE-VIA	ZH512 HOLE-VIA	ZH522 HOLE-VIA
ZH503 HOLE-VIA	ZH513 HOLE-VIA	ZH523 HOLE-VIA
ZH504 HOLE-VIA	ZH514 HOLE-VIA	ZH524 HOLE-VIA
ZH505 HOLE-VIA	ZH515 HOLE-VIA	ZH525 HOLE-VIA
ZH506 HOLE-VIA	ZH516 HOLE-VIA	ZH526 HOLE-VIA
ZH507 HOLE-VIA	ZH517 HOLE-VIA	ZH527 HOLE-VIA
ZH508 HOLE-VIA	ZH518 HOLE-VIA	ZH528 HOLE-VIA
ZH509 HOLE-VIA	ZH519 HOLE-VIA	ZH529 HOLE-VIA

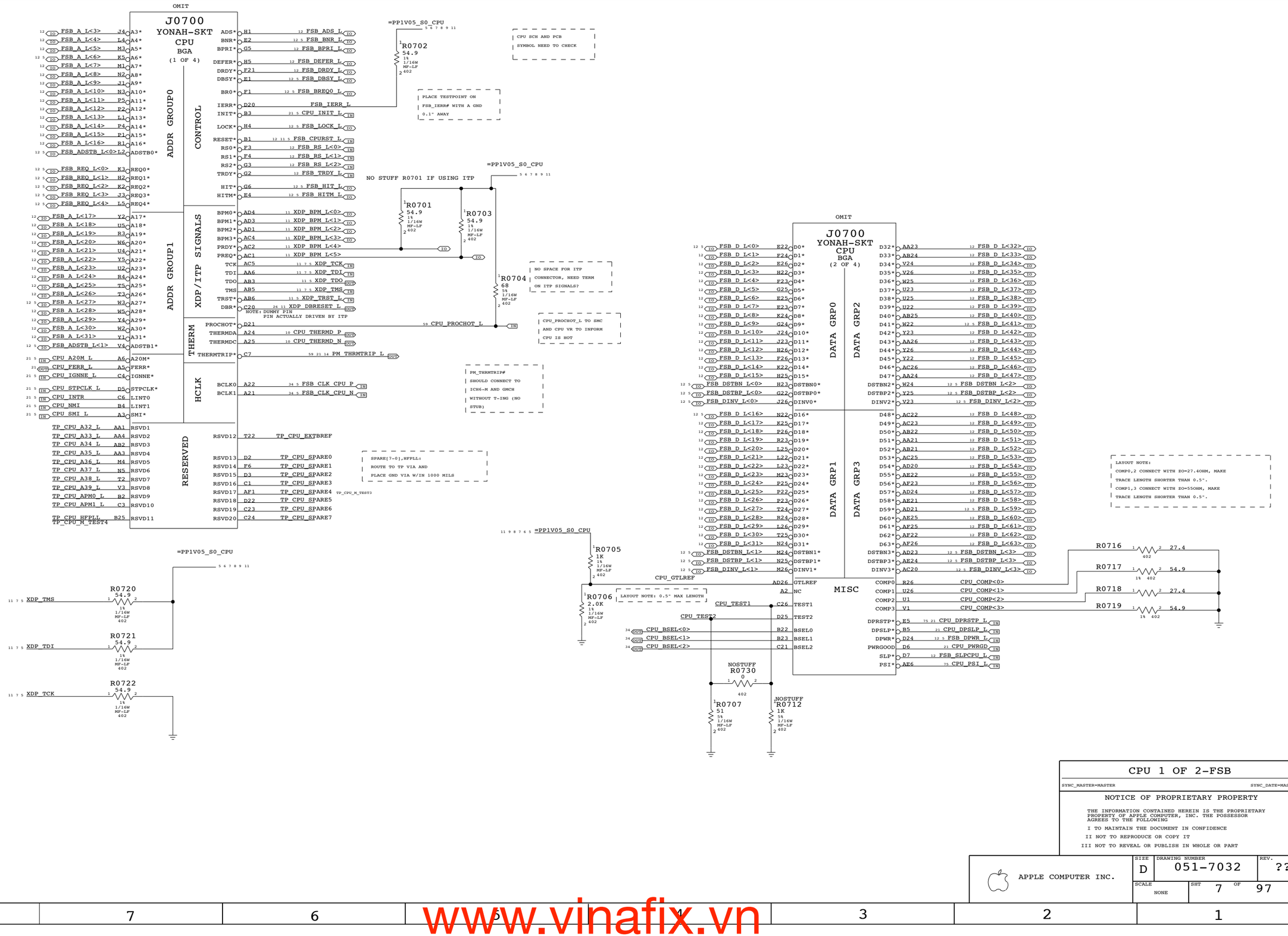
FUNC TEST 1 OF 2

SYNC_MASTER=MASTER SYNC_DATE=MASTER

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7032	??
SCALE: NONE	SHT 5 OF 97	





CPU 1 OF 2-FSB

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7032	??
SCALE: NONE	SHT 7 OF 97	

=PPVCORE_S0_CPU 6 8 9 76

OMIT

J0700
YONAH-SKT
CPU
BGA
(3 OF 4)

A7	VCC_1	VCC_68	AB20
A9	VCC_2	VCC_69	AB7
A10	VCC_3	VCC_70	AC7
A12	VCC_4	VCC_71	AC9
A13	VCC_5	VCC_72	AC12
A15	VCC_6	VCC_73	AC13
A17	VCC_7	VCC_74	AC15
A18	VCC_8	VCC_75	AC17
A20	VCC_9	VCC_76	AC18
B7	VCC_10	VCC_77	AD7
B9	VCC_11	VCC_78	AD9
B10	VCC_12	VCC_79	AD10
B12	VCC_13	VCC_80	AD12
B14	VCC_14	VCC_81	AD14
B15	VCC_15	VCC_82	AD15
B17	VCC_16	VCC_83	AD17
B18	VCC_17	VCC_84	AD18
B20	VCC_18	VCC_85	AE9
C9	VCC_19	VCC_86	AE10
C10	VCC_20	VCC_87	AE12
C12	VCC_21	VCC_88	AE13
C13	VCC_22	VCC_89	AE15
C15	VCC_23	VCC_90	AE17
C17	VCC_24	VCC_91	AE18
C18	VCC_25	VCC_92	AE20
D9	VCC_26	VCC_93	AF9
D10	VCC_27	VCC_94	AF10
D12	VCC_28	VCC_95	AF12
D14	VCC_29	VCC_96	AF14
D15	VCC_30	VCC_97	AF15
D17	VCC_31	VCC_98	AF17
D18	VCC_32	VCC_99	AF18
E7	VCC_33	VCC_100	AF20
E9	VCC_34		
E10	VCC_35	VCCP_1	V6
E12	VCC_36	VCCP_2	G21
E13	VCC_37	VCCP_3	J6
E15	VCC_38	VCCP_4	K6
E17	VCC_39	VCCP_5	M6
E18	VCC_40	VCCP_6	J21
E20	VCC_41	VCCP_7	K21
F7	VCC_42	VCCP_8	M21
F9	VCC_43	VCCP_9	N21
F10	VCC_44	VCCP_10	N6
F12	VCC_45	VCCP_11	R21
F14	VCC_46	VCCP_12	R6
F15	VCC_47	VCCP_13	T21
F17	VCC_48	VCCP_14	T6
F18	VCC_49	VCCP_15	V21
F20	VCC_50	VCCP_16	W21
AA7	VCC_51		
AA9	VCC_52		
AA10	VCC_53		
AA12	VCC_54		
AA13	VCC_55		
AA15	VCC_56		
AA17	VCC_57		
AA18	VCC_58		
AA20	VCC_59		
AB9	VCC_60		
AC10	VCC_61		
AB10	VCC_62		
AB12	VCC_63		
AB14	VCC_64		
AB15	VCC_65	VCCSENSE	AF7
AB17	VCC_66	VSSSENSE	AE7
AB18	VCC_67		

=PPVCORE_S0_CPU 6 8 9 76

=PP1V05_S0_CPU 5 6 7 9 11

=PP1V5_S0_CPU 6 8

VCCA=1.5 ONLY

VCCA	B26	
VID0	AD6	75 CPU_VID<0> OUT
VID1	AF5	75 CPU_VID<1> OUT
VID2	AE5	75 CPU_VID<2> OUT
VID3	AF4	75 CPU_VID<3> OUT
VID4	AE3	75 CPU_VID<4> OUT
VID5	AF2	75 CPU_VID<5> OUT
VID6	AE2	75 CPU_VID<6> OUT

=PPVCORE_S0_CPU 6 8 9 76

R0802
100
1%
1/16W
MF-LF
402

75 CPU_VCCSENSE_P OUT

75 CPU_VCCSENSE_N OUT

R0803
100
1%
1/16W
MF-LF
402

LAYOUT NOTE: CONNECT R0802-03 TO VCCSENSE_P/N WITH NO STUB

=PP1V5_S0_CPU 6 8

C0800
0.01UF
20%
16V
CERM
402

C0801
10UF
20%
6.3V
CERM
805-1

LAYOUT NOTE:
PROVIDE A TEST POINT (WITH NO STUB) TO CONNECT A DIFFERENCTIAL PROBE BETWEEN VCCSENSE AND VSSSENSE AT THE LOCATION WHERE THE TWO 54.9 OHM RESISTORS TERMINATE THE 55 OHM TRANSMISSION LINE

OMIT

J0700
YONAH-SKT
CPU
BGA
(4 OF 4)

A4	VSS_1	VSS_82	P6
A8	VSS_2	VSS_83	P21
A11	VSS_3	VSS_84	P24
A14	VSS_4	VSS_85	R2
A16	VSS_5	VSS_86	R5
A19	VSS_6	VSS_87	R22
A23	VSS_7	VSS_88	R25
A26	VSS_8	VSS_89	T1
B6	VSS_9	VSS_90	T4
B8	VSS_10	VSS_91	T23
B11	VSS_11	VSS_92	T26
B13	VSS_12	VSS_93	U3
B16	VSS_13	VSS_94	U6
B19	VSS_14	VSS_95	U21
B21	VSS_15	VSS_96	U24
B24	VSS_16	VSS_97	V2
C5	VSS_17	VSS_98	V5
C8	VSS_18	VSS_99	V22
C11	VSS_19	VSS_100	V25
C14	VSS_20	VSS_101	W1
C16	VSS_21	VSS_102	W4
C19	VSS_22	VSS_103	W23
C2	VSS_23	VSS_104	W26
C22	VSS_24	VSS_105	Y3
C25	VSS_25	VSS_106	Y6
D1	VSS_26	VSS_107	Y21
D4	VSS_27	VSS_108	Y24
D8	VSS_28	VSS_109	AA2
D11	VSS_29	VSS_110	AA5
D13	VSS_30	VSS_111	AA8
D16	VSS_31	VSS_112	AA11
D19	VSS_32	VSS_113	AA14
D23	VSS_33	VSS_114	AA16
D26	VSS_34	VSS_115	AA19
E3	VSS_35	VSS_116	AA22
E6	VSS_36	VSS_117	AA25
E8	VSS_37	VSS_118	AB1
E11	VSS_38	VSS_119	AB4
E14	VSS_39	VSS_120	AB8
E16	VSS_40	VSS_121	AB11
E19	VSS_41	VSS_122	AB13
E21	VSS_42	VSS_123	AB16
E24	VSS_43	VSS_124	AB19
F5	VSS_44	VSS_125	AB23
F8	VSS_45	VSS_126	AB26
F11	VSS_46	VSS_127	AC3
F13	VSS_47	VSS_128	AC6
F16	VSS_48	VSS_129	AC8
F19	VSS_49	VSS_130	AC11
F2	VSS_50	VSS_131	AC14
F22	VSS_51	VSS_132	AC16
F25	VSS_52	VSS_133	AC19
G4	VSS_53	VSS_134	AC21
G1	VSS_54	VSS_135	AC24
G23	VSS_55	VSS_136	AD2
G26	VSS_56	VSS_137	AD5
H3	VSS_57	VSS_138	AD8
H6	VSS_58	VSS_139	AD11
H21	VSS_59	VSS_140	AD13
H24	VSS_60	VSS_141	AD16
J2	VSS_61	VSS_142	AD19
J5	VSS_62	VSS_143	AD22
J22	VSS_63	VSS_144	AD25
J25	VSS_64	VSS_145	AE1
K1	VSS_65	VSS_146	AE4
K4	VSS_66	VSS_147	AE8
K23	VSS_67	VSS_148	AE11
K26	VSS_68	VSS_149	AE14
L3	VSS_69	VSS_150	AE16
L6	VSS_70	VSS_151	AE19
L21	VSS_71	VSS_152	AE23
L24	VSS_72	VSS_153	AE26
M2	VSS_73	VSS_154	AF3
M5	VSS_74	VSS_155	AF6
M22	VSS_75	VSS_156	AF8
M25	VSS_76	VSS_157	AF11
N1	VSS_77	VSS_158	AF13
N4	VSS_78	VSS_159	AF16
N23	VSS_79	VSS_160	AF19
N26	VSS_80	VSS_161	AF21
P3	VSS_81	VSS_162	AF24

CPU 2 OF 2-PWR/GND

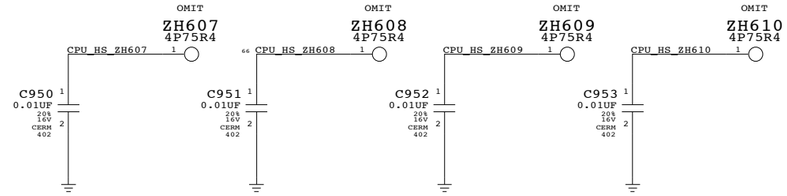
SYNC_MASTER=MASTER SYNC_DATE=MASTER

APPLE COMPUTER INC.

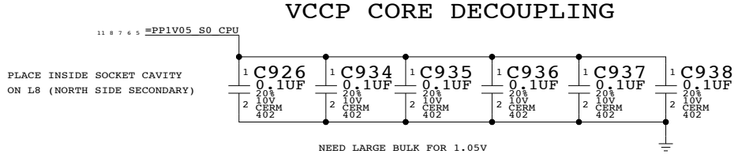
SIZE	DRAWING NUMBER	REV.
D	051-7032	??
SCALE: NONE	SHT 8 OF 97	

WE HAD A 330UF ELEC CAP HERE FOR 1.05V RAIL - CHECK WE CAN REMOVE

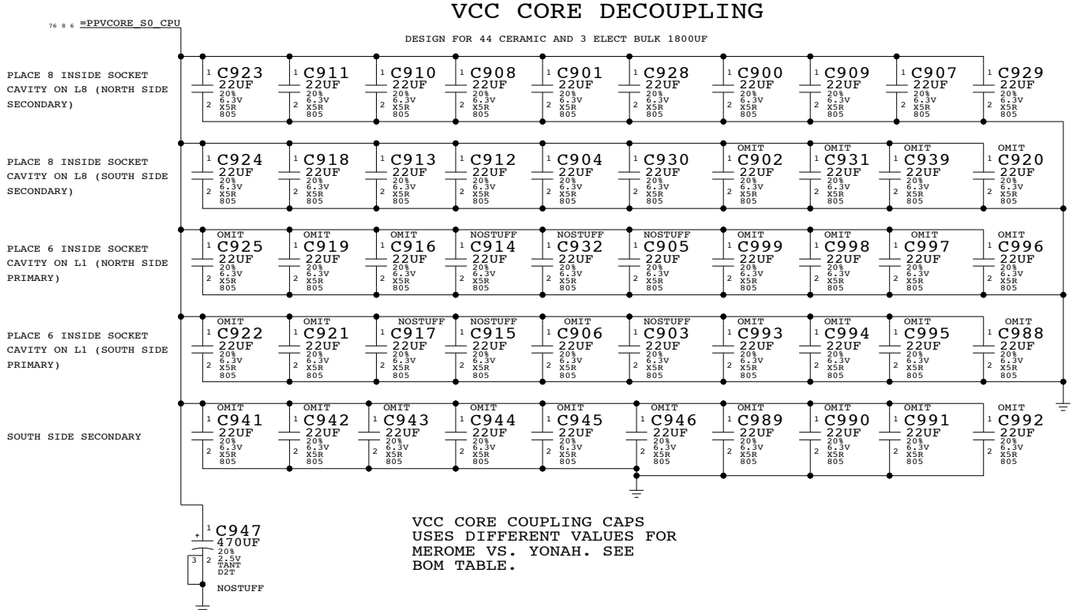
CPU HEATSINK MOUNTING HOLES



VCCP CORE DECOUPLING



VCC CORE DECOUPLING



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
138S0552	28	CAP,22UF,6.3V,20%,X5R,0805	C922,C925,C906,C939,C919,C993,C942,C991,C995,C990,C989,C988,C920,C997,C992,C994,C996,C921,C999,C943,C998,C944,C945,C946,C941,C916,C931,C902		MEROM
138S0558	28	CAP,10UF,6.3V,20%,X5R,0805	C922,C925,C906,C939,C919,C993,C942,C991,C995,C990,C989,C988,C920,C997,C992,C994,C996,C921,C999,C943,C998,C944,C945,C946,C941,C916,C931,C902		YONAH

CPU DECAPS & VID<>

SYNC_MASTER=MASTER SYNC_DATE=MASTER

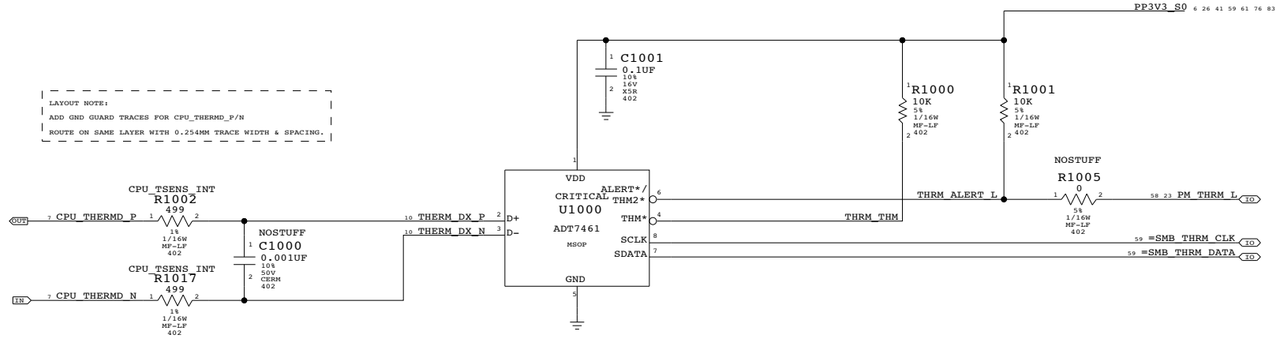
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7032	??
SCALE: NONE	SHT 9 OF 97	

CPU THERMAL SENSOR

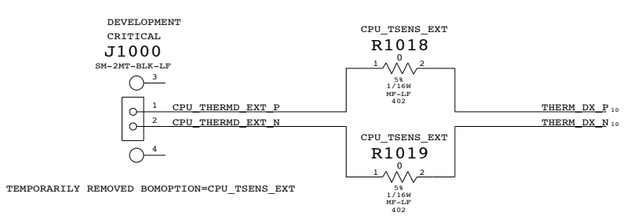
NOTE:
IF CPU T DIODE TO BE READ IN OFF STATE,
THEN THIS SHOULD BE S5

LAYOUT NOTE:
ADD GND GUARD TRACES FOR CPU_THERMD_P/N
ROUTE ON SAME LAYER WITH 0.254MM TRACE WIDTH & SPACING.



NOTE: SYMBOL SHOULD BE SHOWN ADT7461A

LAYOUT NOTE:
PLACE R1002 AND R1018 SUCH THAT THEY SHARE ONE PAD
PLACE R1017 AND R1019 SUCH THAT THEY SHARE ONE PAD



TEMPORARILY REMOVED BOMOPTION=CPU_TSENS_EXT

CPU TEMP SENSOR

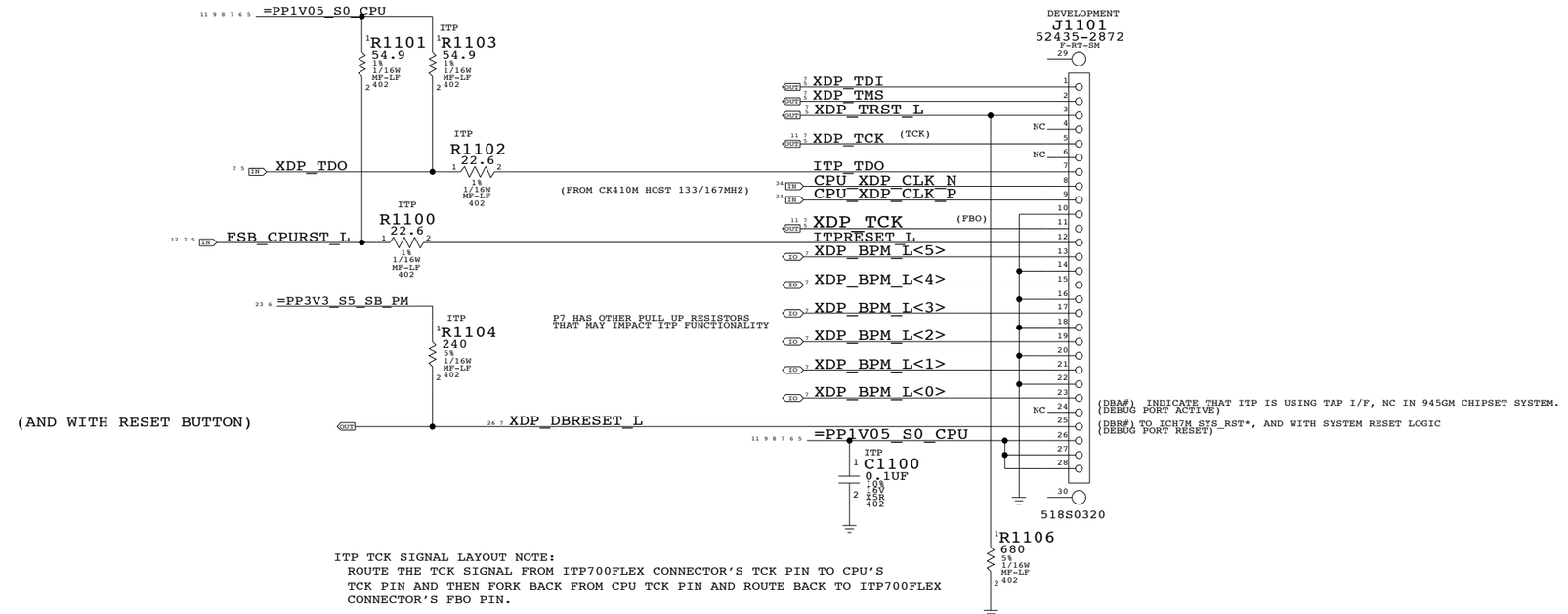
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7032	??

SCALE: NONE

SHT 10 OF 97

CPU ITP700FLEX DEBUG SUPPORT



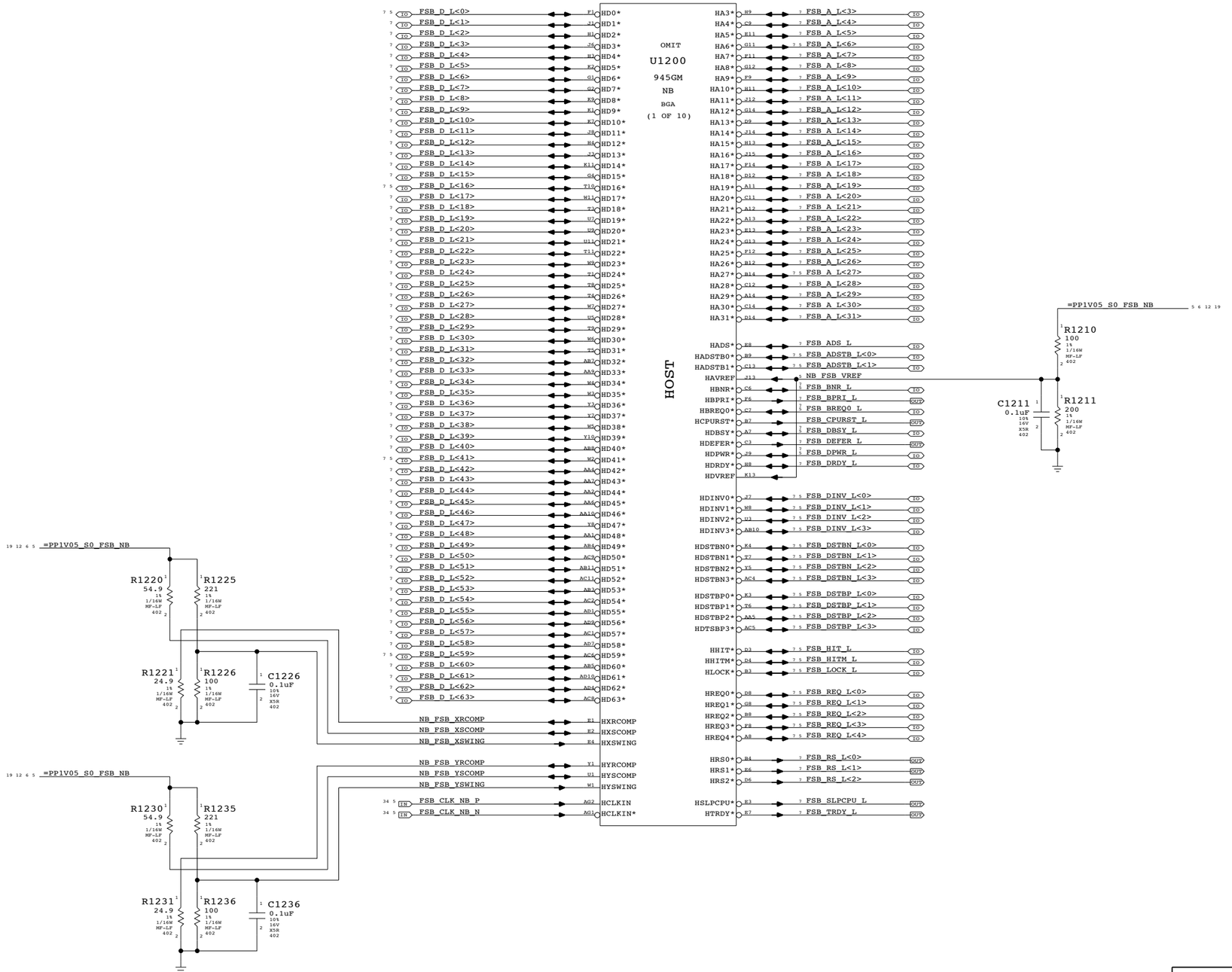
ITP TCK SIGNAL LAYOUT NOTE:
ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX CONNECTOR'S FBO PIN.

CPU ITP700FLEX DEBUG

SYNC_MASTER=M38 SYNC_DATE=01/05/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7032	??
SCALE: NONE	SHT 11 OF 97	



NB CPU Interface

SYNC_MASTER=M1 SYNC_DATE=01/05/2006

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SIZE	DRAWING NUMBER	REV.
D	051-7032	??
SCALE: NONE	SHT 12 OF 97	

LVDS Disable

Can leave all signals NC if LVDS is not implemented
Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
VCCD_LVDS must remain powered with proper decoupling.
Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

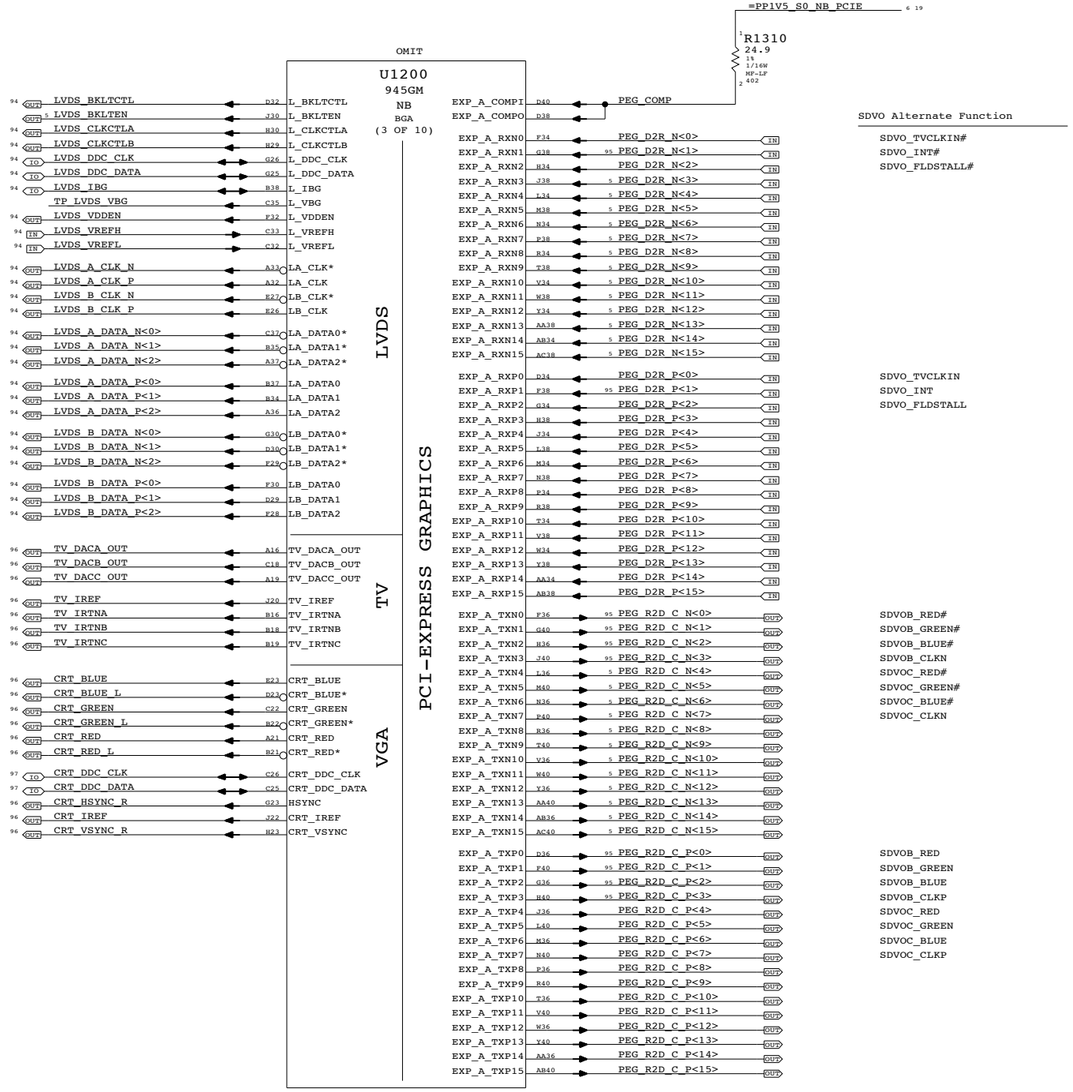
Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable

Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail.
Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and
VCCA_TVBG to 1.5V power rail. Tie VSSA_TVBG to GND.

CRT Disable

Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie
HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core
rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.

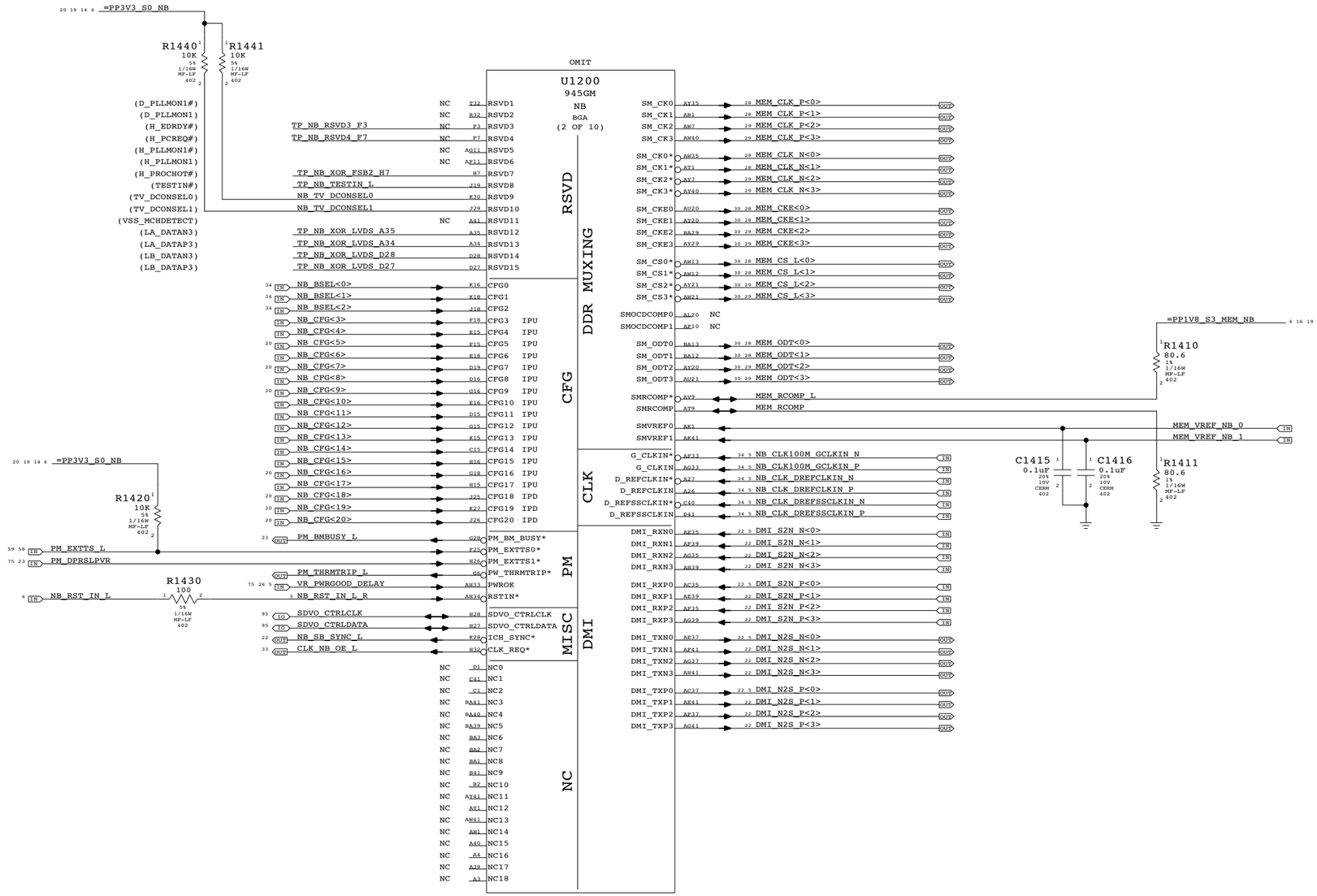


NB PEG / Video Interfaces

SYNC_MASTER=M1 SYNC_DATE=01/05/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7032	??
SCALE: NONE	SHT 13 OF 97	



NB Misc Interfaces

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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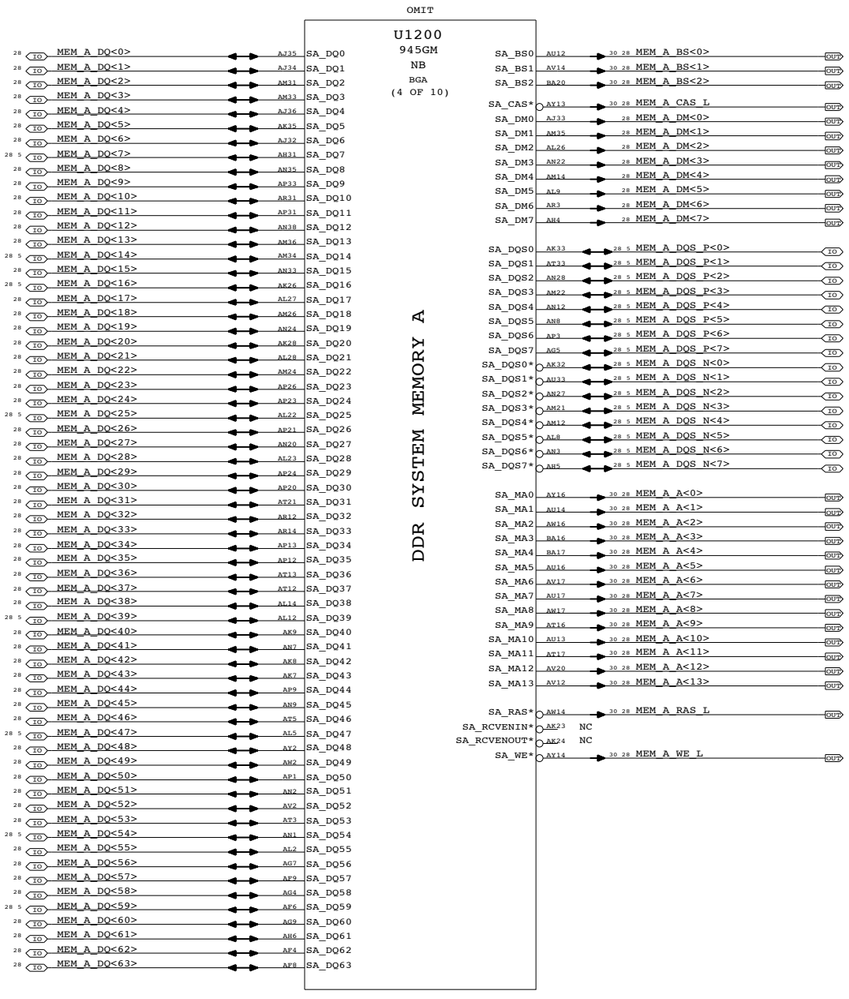
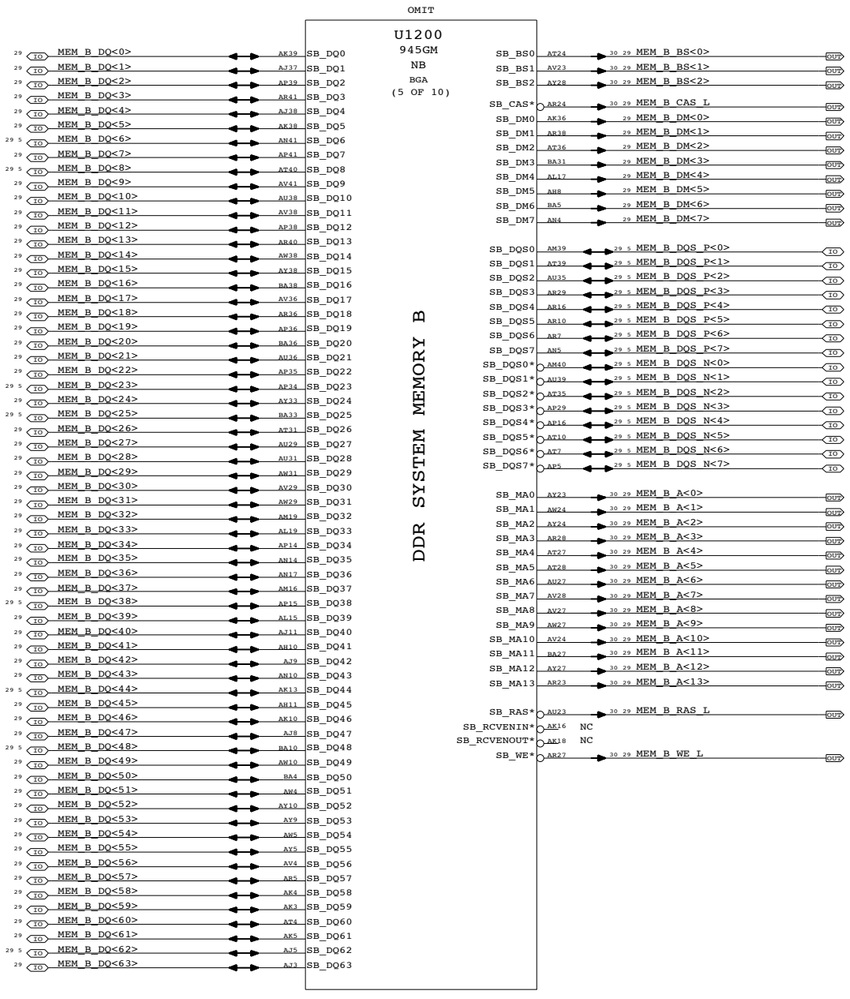
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7032	??

SCALE: NONE SHT 14 OF 97





NB DDR2 Interfaces

SYNC_MASTER=M1 SYNC_DATE=01/05/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7032	??
SCALE: NONE	SHT 15 OF 97	

NCTF balls are Not Critical To Function

These connections can break without impacting part performance.

=PPVCORE_S0_NB 6 16 19

1.05V or 1.5V

U1200 945GM NB BGA (6 OF 10) OMIT VCC

VCC_0	AA33	
VCC_1	R33	
VCC_2	P33	
VCC_3	L33	
VCC_4	J33	
VCC_5	AA32	
VCC_6	T32	
VCC_7	M32	
VCC_8	V32	
VCC_9	P32	
VCC_10	N32	
VCC_11	K32	
VCC_12	H32	
VCC_13	L32	
VCC_14	J32	
VCC_15	AA31	
VCC_16	W31	
VCC_17	V31	
VCC_18	T31	
VCC_19	R31	
VCC_20	P31	
VCC_21	N31	
VCC_22	L31	
VCC_23	AA30	
VCC_24	Y30	
VCC_25	W30	
VCC_26	V30	
VCC_27	U30	
VCC_28	T30	
VCC_29	R30	
VCC_30	P30	
VCC_31	N30	
VCC_32	L30	
VCC_33	AA29	
VCC_34	Y29	
VCC_35	W29	
VCC_36	V29	
VCC_37	U29	
VCC_38	T29	
VCC_39	R29	
VCC_40	P29	
VCC_41	N29	
VCC_42	L29	
VCC_43	AB28	
VCC_44	AA28	
VCC_45	Y28	
VCC_46	V28	
VCC_47	U28	
VCC_48	T28	
VCC_49	R28	
VCC_50	P28	
VCC_51	N28	
VCC_52	M28	
VCC_53	L28	
VCC_54	P27	
VCC_55	N27	
VCC_56	M27	
VCC_57	L27	
VCC_58	P26	
VCC_59	N26	
VCC_60	L26	
VCC_61	M25	
VCC_62	L25	
VCC_63	P24	
VCC_64	N24	
VCC_65	M24	
VCC_66	L24	
VCC_67	AB23	
VCC_68	AA23	
VCC_69	Y23	
VCC_70	W23	
VCC_71	V23	
VCC_72	N23	
VCC_73	L23	
VCC_74	AC22	
VCC_75	AB22	
VCC_76	Y22	
VCC_77	W22	
VCC_78	P22	
VCC_79	N22	
VCC_80	M22	
VCC_81	L22	
VCC_82	AC21	
VCC_83	AA21	
VCC_84	V21	
VCC_85	N21	
VCC_86	M21	
VCC_87	L21	
VCC_88	AC20	
VCC_89	AB20	
VCC_90	Y20	
VCC_91	W20	
VCC_92	P20	
VCC_93	N20	
VCC_94	M20	
VCC_95	L20	
VCC_96	AB19	
VCC_97	AA19	
VCC_98	Y19	
VCC_99	W19	
VCC_100	M19	
VCC_101	L19	
VCC_102	R18	
VCC_103	N18	
VCC_104	L18	
VCC_105	P17	
VCC_106	N17	
VCC_107	M17	
VCC_108	M16	
VCC_109	N16	
VCC_110	L16	
VCC_SM0	AU41	
VCC_SM1	AT41	
VCC_SM2	AM41	
VCC_SM3	AU40	
VCC_SM4	BA34	
VCC_SM5	BA24	
VCC_SM6	AW34	
VCC_SM7	AV34	
VCC_SM8	AU34	
VCC_SM9	AT34	
VCC_SM10	AM34	
VCC_SM11	BA30	
VCC_SM12	AV30	
VCC_SM13	AM30	
VCC_SM14	AV30	
VCC_SM15	AU30	
VCC_SM16	AT30	
VCC_SM17	AM30	
VCC_SM18	AP30	
VCC_SM19	AN30	
VCC_SM20	AM30	
VCC_SM21	AM29	
VCC_SM22	AL29	
VCC_SM23	AK29	
VCC_SM24	AJ29	
VCC_SM25	AM29	
VCC_SM26	AJ28	
VCC_SM27	AH28	
VCC_SM28	AE27	
VCC_SM29	AD27	
VCC_SM30	BA26	
VCC_SM31	AW26	
VCC_SM32	AM26	
VCC_SM33	AV26	
VCC_SM34	AU26	
VCC_SM35	AT26	
VCC_SM36	AR26	
VCC_SM37	AJ26	
VCC_SM38	AH26	
VCC_SM39	AJ25	
VCC_SM40	AM25	
VCC_SM41	AJ24	
VCC_SM42	AH24	
VCC_SM43	AJ23	
VCC_SM44	BA23	
VCC_SM45	AJ22	
VCC_SM46	AV22	
VCC_SM47	AM22	
VCC_SM48	AV22	
VCC_SM49	AU22	
VCC_SM50	AT22	
VCC_SM51	AR22	
VCC_SM52	AP22	
VCC_SM53	AJ22	
VCC_SM54	AH22	
VCC_SM55	AM21	
VCC_SM56	AK20	
VCC_SM57	BA19	
VCC_SM58	AV19	
VCC_SM59	AM19	
VCC_SM60	AV19	
VCC_SM61	AU19	
VCC_SM62	AT19	
VCC_SM63	AJ19	
VCC_SM64	AH19	
VCC_SM65	AM19	
VCC_SM66	AJ19	
VCC_SM67	AJ18	
VCC_SM68	AH18	
VCC_SM69	AJ17	
VCC_SM70	AJ16	
VCC_SM71	BA15	
VCC_SM72	AV15	
VCC_SM73	AM15	
VCC_SM74	AV15	
VCC_SM75	AU15	
VCC_SM76	AT15	
VCC_SM77	AR15	
VCC_SM78	AJ15	
VCC_SM79	AH15	
VCC_SM80	AJ14	
VCC_SM81	AJ13	
VCC_SM82	AH13	
VCC_SM83	AK12	
VCC_SM84	AJ12	
VCC_SM85	AM12	
VCC_SM86	AG12	
VCC_SM87	AK11	
VCC_SM88	BA8	
VCC_SM89	AV8	
VCC_SM90	AM8	
VCC_SM91	AV8	
VCC_SM92	AU8	
VCC_SM93	AT8	
VCC_SM94	AR8	
VCC_SM95	AJ8	
VCC_SM96	AH8	
VCC_SM97	AM6	
VCC_SM98	AV6	
VCC_SM99	AM6	
VCC_SM100	AV6	
VCC_SM101	AU6	
VCC_SM102	AT6	
VCC_SM103	AR6	
VCC_SM104	AJ6	
VCC_SM105	AV1	
VCC_SM106	AM1	
VCC_SM107	AJ1	

NB_VCCSM_LF4

NB_VCCSM_LF5

C1614 1 0.47uF 20% 6.3V CERM-X5R 402 2

C1613 1 0.47uF 20% 6.3V CERM-X5R 402 2

C1615 1 0.47uF 20% 6.3V CERM-X5R 402 2

19 14 6 =PP1V8_S3_MEM_NB

Layout Note: Place near pin BA23

C1620 1 10UF 20% 6.3V CERM 805-1 2

C1621 1 10UF 20% 6.3V CERM 805-1 2

Layout Note: Place in cavity (Need to better define cavity)

C1610 1 0.47uF 20% 6.3V CERM-X5R 402 2

Layout Note: Place near pin BA15

NB_VCCSM_LF2

NB_VCCSM_LF1

C1612 1 0.47uF 20% 6.3V CERM-X5R 402 2

C1611 1 0.47uF 20% 6.3V CERM-X5R 402 2

19 16 6 =PPVCORE_S0_NB

U1200 945GM NB BGA (7 OF 10) OMIT NCTF

VCC_NCTF0	AD27	
VCC_NCTF1	AC27	
VCC_NCTF2	AB27	
VCC_NCTF3	AA27	
VCC_NCTF4	Y27	
VCC_NCTF5	W27	
VCC_NCTF6	V27	
VCC_NCTF7	U27	
VCC_NCTF8	T27	
VCC_NCTF9	R27	
VCC_NCTF10	AD26	
VCC_NCTF11	AC26	
VCC_NCTF12	AB26	
VCC_NCTF13	AA26	
VCC_NCTF14	Y26	
VCC_NCTF15	W26	
VCC_NCTF16	V26	
VCC_NCTF17	U26	
VCC_NCTF18	T26	
VCC_NCTF19	R26	
VCC_NCTF20	AD25	
VCC_NCTF21	AC25	
VCC_NCTF22	AB25	
VCC_NCTF23	AA25	
VCC_NCTF24	Y25	
VCC_NCTF25	W25	
VCC_NCTF26	V25	
VCC_NCTF27	U25	
VCC_NCTF28	T25	
VCC_NCTF29	R25	
VCC_NCTF30	AD24	
VCC_NCTF31	AC24	
VCC_NCTF32	AB24	
VCC_NCTF33	AA24	
VCC_NCTF34	Y24	
VCC_NCTF35	W24	
VCC_NCTF36	V24	
VCC_NCTF37	U24	
VCC_NCTF38	T24	
VCC_NCTF39	R24	
VCC_NCTF40	AD23	
VCC_NCTF41	V23	
VCC_NCTF42	U23	
VCC_NCTF43	T23	
VCC_NCTF44	R23	
VCC_NCTF45	AD22	
VCC_NCTF46	V22	
VCC_NCTF47	U22	
VCC_NCTF48	T22	
VCC_NCTF49	R22	
VCC_NCTF50	AD21	
VCC_NCTF51	V21	
VCC_NCTF52	U21	
VCC_NCTF53	T21	
VCC_NCTF54	R21	
VCC_NCTF55	AD20	
VCC_NCTF56	V20	
VCC_NCTF57	U20	
VCC_NCTF58	T20	
VCC_NCTF59	R20	
VCC_NCTF60	AD19	
VCC_NCTF61	V19	
VCC_NCTF62	U19	
VCC_NCTF63	T19	
VCC_NCTF64	AD18	
VCC_NCTF65	AC18	
VCC_NCTF66	AB18	
VCC_NCTF67	AA18	
VCC_NCTF68	Y18	
VCC_NCTF69	W18	
VCC_NCTF70	V18	
VCC_NCTF71	U18	
VCC_NCTF72	T18	
VSS_NCTF0	AE27	
VSS_NCTF1	AE26	
VSS_NCTF2	AE25	
VSS_NCTF3	AE24	
VSS_NCTF4	AE23	
VSS_NCTF5	AE22	
VSS_NCTF6	AE21	
VSS_NCTF7	AE20	
VSS_NCTF8	AE19	
VSS_NCTF9	AE18	
VSS_NCTF10	AC17	
VSS_NCTF11	Y17	
VSS_NCTF12	U17	

PP1V5_S0_NB_FILT_VCCAUX 17 19

VCCAUX_NCTF0	AG27	
VCCAUX_NCTF1	AF27	
VCCAUX_NCTF2	AG26	
VCCAUX_NCTF3	AF26	
VCCAUX_NCTF4	AG25	
VCCAUX_NCTF5	AF25	
VCCAUX_NCTF6	AG24	
VCCAUX_NCTF7	AF24	
VCCAUX_NCTF8	AG23	
VCCAUX_NCTF9	AF23	
VCCAUX_NCTF10	AG22	
VCCAUX_NCTF11	AF22	
VCCAUX_NCTF12	AG21	
VCCAUX_NCTF13	AF21	
VCCAUX_NCTF14	AG20	
VCCAUX_NCTF15	AF20	
VCCAUX_NCTF16	AG19	
VCCAUX_NCTF17	AF19	
VCCAUX_NCTF18	R19	
VCCAUX_NCTF19	AG18	
VCCAUX_NCTF20	AF18	
VCCAUX_NCTF21	R18	
VCCAUX_NCTF22	AG17	
VCCAUX_NCTF23	AF17	
VCCAUX_NCTF24	AE17	
VCCAUX_NCTF25	AD17	
VCCAUX_NCTF26	AB17	
VCCAUX_NCTF27	AA17	
VCCAUX_NCTF28	W17	
VCCAUX_NCTF29	V17	
VCCAUX_NCTF30	T17	
VCCAUX_NCTF31	R17	
VCCAUX_NCTF32	AG16	
VCCAUX_NCTF33	AF16	
VCCAUX_NCTF34	AE16	
VCCAUX_NCTF35	AD16	
VCCAUX_NCTF36	AC16	
VCCAUX_NCTF37	AB16	
VCCAUX_NCTF38	AA16	
VCCAUX_NCTF39	Y16	
VCCAUX_NCTF40	W16	
VCCAUX_NCTF41	V16	
VCCAUX_NCTF42	U16	
VCCAUX_NCTF43	T16	
VCCAUX_NCTF44	R16	
VCCAUX_NCTF45	AG15	
VCCAUX_NCTF46	AF15	
VCCAUX_NCTF47	AE15	
VCCAUX_NCTF48	AD15	
VCCAUX_NCTF49	AC15	
VCCAUX_NCTF50	AB15	
VCCAUX_NCTF51	AA15	
VCCAUX_NCTF52	Y15	
VCCAUX_NCTF53	W15	
VCCAUX_NCTF54	V15	
VCCAUX_NCTF55	U15	
VCCAUX_NCTF56	T15	
VCCAUX_NCTF57	R15	

NB Power 1

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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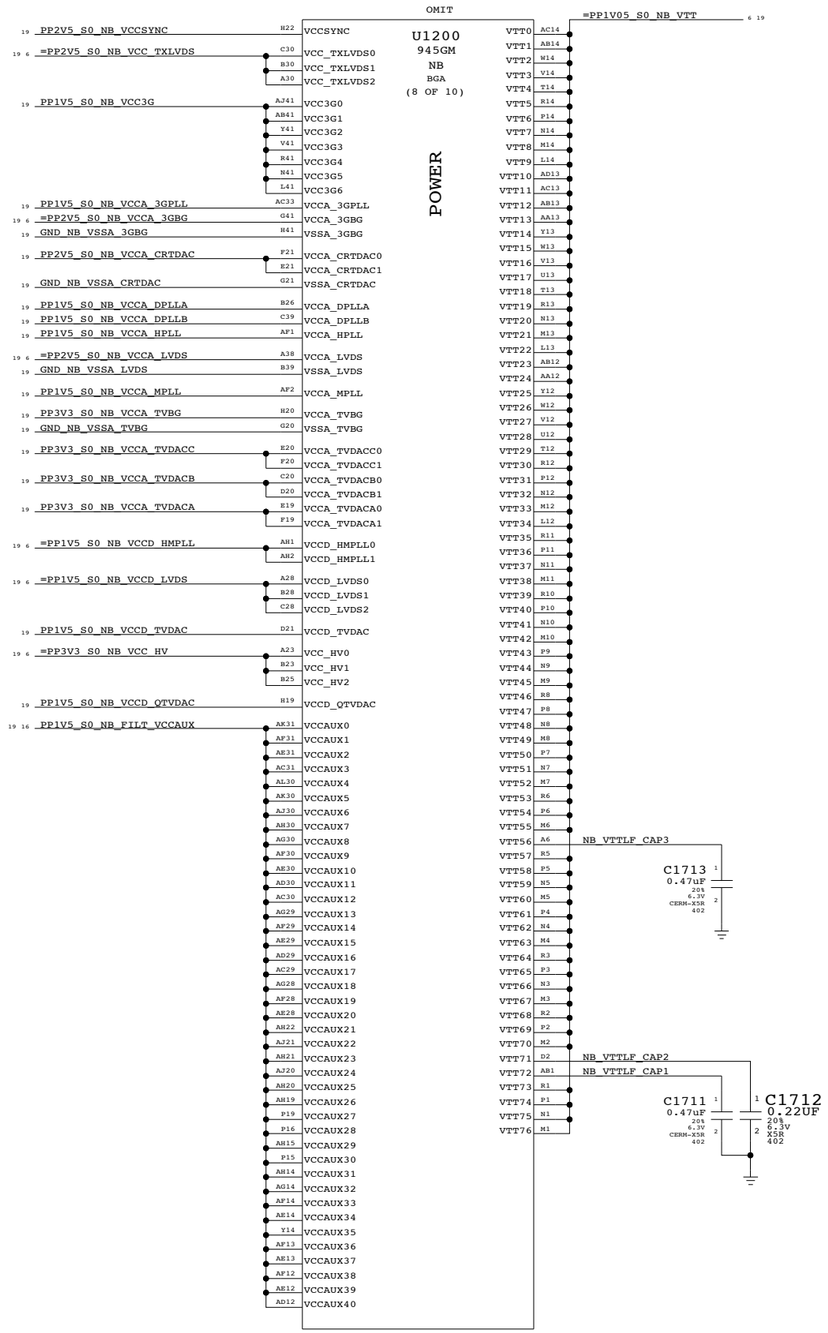
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7032	??

SCALE NONE SHT 16 OF 97

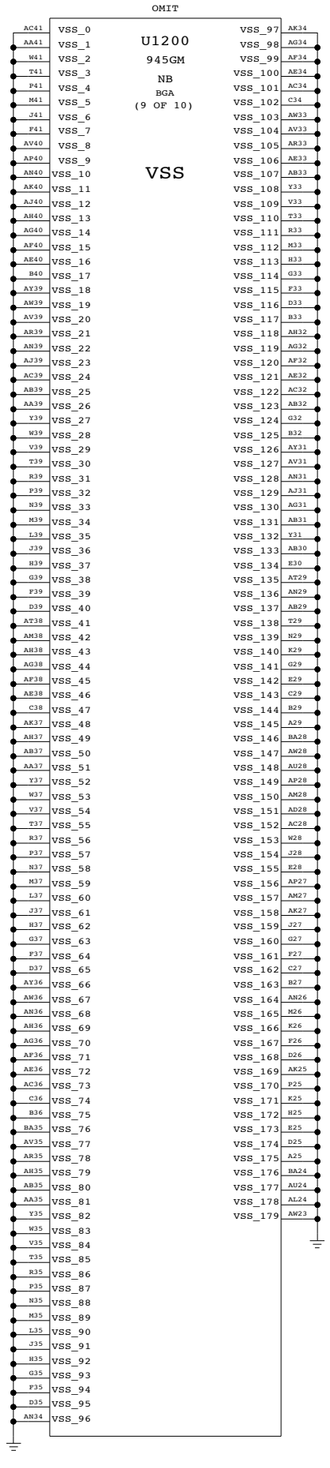


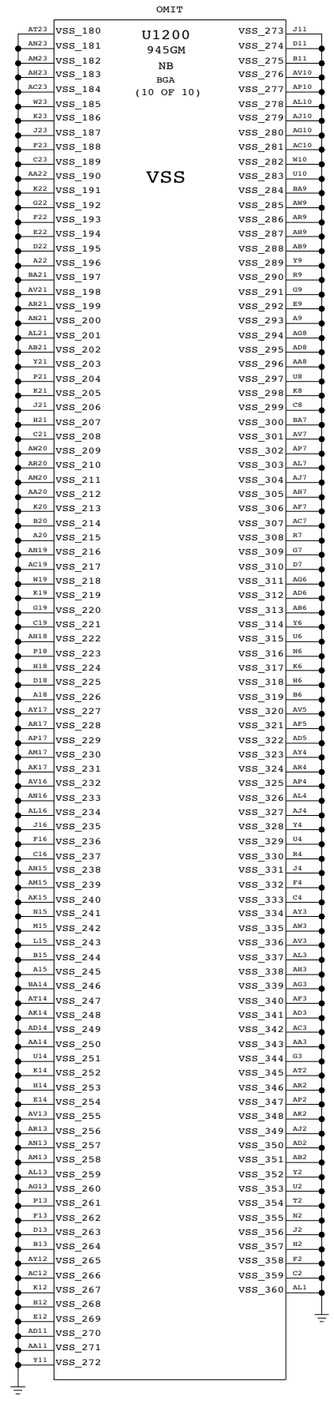
NB Power 2

SYNC_MASTER=M40 SYNC_DATE=01/05/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7032	??
SCALE: NONE	SHT 17 OF 97	





NB Grounds

SYNC_MASTER=M1 SYNC_DATE=01/05/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7032	??

SCALE NONE SHT 18 OF 97

Power Interface

These are the power signals that leave the NB "block"

IN =PP1V05_S0_FSB_NB 5 6 12
IN =PPVCORE_S0_NB 6 16 19
IN =PP1V05_S0_NB_VTT 6 17 19
IN =PP1V5_S0_NB 6 19
IN =PP1V5_S0_NB_PCIE 6 13
IN =PP1V5_S0_NB_PLL 6 19
IN =PP1V5_S0_NB_TVDAC 6 19
IN =PP1V5_S0_NB_VCCD_HMPLL 6 17
IN =PP1V5_S0_NB_VCCD_LVDS 6 17 19
IN =PP1V5_S0_NB_VCCAUX 6 19
IN =PP1V8_S3_MEM_NB 6 14 16 19
IN =PP2V5_S0_NB_VCCSYNC 19 6 — I276 — PP2V5_S0_NB_VCCSYNC 17
IN =PP2V5_S0_NB_VCC_TXLVDS 6 17 19
IN =PP2V5_S0_NB_VCCA_3GBG 6 17 19
IN =PP2V5_S0_NB_VCCA_LVDS 6 17 19
IN =PP3V3_S0_NB 6 14 20
IN =PP3V3_S0_NB_VCC_HV 6 17 19
IN =PP5V_S0_NB_TVDAC 6 19

MCH DISPLAY PLL POWER LDO

6 =PP2V5_S0_NB_DISP_PLL
U1900 TPS73115 SOT23-5
1 IN OUT 5 PP1V5_S0_DPLL
3 EN NR/FB 4 TPS73115_NR
GND 2
VOLTAGE=1.5V MIN_LINE_WIDTH=1.0 mm MIN_NECK_WIDTH=0.35MM
C1950 1UF 10% 6.3V CERM 402
C1951 0.01uF 10% 16V CERM 402
C1952 10UF 20% 6.3V CERM 805-1

R1950 1 5% 1/16W MF-LF 402 — PP1V5_S0_NB_VCCA_DPLLA 17
VOLTAGE=1.5V MIN_LINE_WIDTH=1.0 mm MIN_NECK_WIDTH=0.35MM
C1953 1UF 10% 6.3V CERM 402

MCH VCCA_DPLLA FILTER
(MCH DISPLAY A PLL 1.5V PWR)

R1951 1 5% 1/16W MF-LF 402 — PP1V5_S0_NB_VCCA_DPLLB 17
VOLTAGE=1.5V MIN_LINE_WIDTH=1.0 mm MIN_NECK_WIDTH=0.35MM
C1954 1UF 10% 6.3V CERM 402

GMCH VCCA_DPLL_B FILTER
(MCH DISPLAY B PLL 1.5V PWR)

MCH VCCA_LVDS FILTER

(MCH LVDS ANALOG 2.5V PWR)

=PP2V5_S0_NB_VCCA_LVDS 6 17 19
C1980 0.1uF 10% 16V CERM 402
C1981 0.01uF 10% 16V CERM 402
GND_NB_VSSA_LVDS 17
I243
Layout Note: This 0.1uF cap should be within 5 mm of NB edge
Layout Note: Route to caps, then GND

MCH VCCA_CRTDAC BYPASS

(MCH CRTDAC ANALOG 2.5V PWR)

6 =PP2V5_S0_NB_CRTDAC
R1985 10 1% 1/16W MF-LF 402 — PP2V5_S0_NB_CRTDAC_FOLLOW
VOLTAGE=2.5V MIN_LINE_WIDTH=1.0 mm MIN_NECK_WIDTH=0.35MM
D1986 BAT54DW SOT-363 =PPVCORE_S0_NB 6 16 19
L1985 180-OHM-1.5A 0603 — PP2V5_S0_NB_CRTDAC_F
VOLTAGE=2.5V MIN_LINE_WIDTH=1.0 mm MIN_NECK_WIDTH=0.35MM
C1986 22000pF~1000mA 16V NPM18 — PP2V5_S0_NB_VCCA_CRTDAC 17
VOLTAGE=2.5V MIN_LINE_WIDTH=1.0 mm MIN_NECK_WIDTH=0.35MM
C1985 0.1uF 10% 16V CERM 402
C1987 10UF 20% 6.3V X5R 603
GND_NB_VSSA_CRTDAC 17
Layout Note: These 2 caps should be within 6.35 mm of NB edge
Layout Note: Route to caps, then GND

GMCH VCCD_LVDS BYPASS

(MCH LVDS DIGITAL 1.5V PWR)

19 17 6 =PP1V5_S0_NB_VCCD_LVDS
C1910 10UF 20% 6.3V CERM 805-1
C1911 0.1uF 20% 10V CERM 402
945 EDS: 5 mOhm, 1nH (1210?)

GMCH VCCTX_LVDS BYPASS

(MCH LVDS DATA/CLK TX 2.5V PWR)

19 17 6 =PP2V5_S0_NB_VCC_TXLVDS
C1912 4.7uF 20% 6.3V CERM 603
C1913 0.1uF 20% 10V CERM 402
945 EDS: 1210?

FILTERING REQUIRED FOR INTEGRATED GFX (PG. 333)

L1910 180-OHM-1.5A 0603
19 6 =PP1V5_S0_NB_VCCAUX — PP1V5_S0_NB_FILT_VCCAUX 16 17
VOLTAGE=1.5V MIN_LINE_WIDTH=0.6 MM MIN_NECK_WIDTH=0.2 MM
C1963 220UF 20% 2.5V POLY SMB2
C1964 220UF 20% 2.5V POLY SMB2
C1962 0.1uF 20% 10V CERM 402

L1934 / L1936 — PLL filters

19 6 =PP1V5_S0_NB_PLL
L1934 FERR-120-OHM-0.2A 0603 — PP1V5_S0_NB_VCCA_HPLL 17
VOLTAGE=1.5V MIN_LINE_WIDTH=1.0 mm MIN_NECK_WIDTH=0.2 MM
C1934 22uF 20% 6.3V X5R 805
C1935 0.1uF 20% 10V CERM 402
L1936 FERR-120-OHM-0.2A 0603 — PP1V5_S0_NB_VCCA_MPLL 17
VOLTAGE=1.5V MIN_LINE_WIDTH=1.0 mm MIN_NECK_WIDTH=0.2 MM
C1936 22uF 20% 6.3V X5R 805
C1937 0.1uF 20% 10V CERM 402
Layout Note: These 4 0.1uF caps should be within 5 mm of NB edge

MCH VCCSYNC BYPASS

(MCH H/V SYNC 2.5V PWR)

19 6 =PP2V5_S0_NB_VCCSYNC
C1917 0.1uF 20% 10V CERM 402

19 17 6 =PP1V05_S0_NB_VTT
C1965 4.7uF 20% 6.3V CERM 603
C1966 2.2UF 10% 6.3V CERM1 603
Layout Note: Place in cavity
C1967 0.22uF 20% 6.3V X5R 402
Layout Note: Place on the edge

19 16 14 6 =PP1V8_S3_MEM_NB
R1982 1K 5% 1/16W MF-LF 402 — MEM_VREF_NB_1 5 14
R1983 1K 5% 1/16W MF-LF 402
R1980 1K 5% 1/16W MF-LF 402 — MEM_VREF_NB_0 6 14
R1981 1K 5% 1/16W MF-LF 402

19 16 6 =PPVCORE_S0_NB
WAS A 330UF ELEC - CHECK WE CAN REMOVE
C1902 10UF 20% 6.3V CERM 805-1
C1903 10UF 20% 6.3V CERM 805-1
C1904 1UF 10% 6.3V CERM 402
C1905 0.22uF 20% 6.3V X5R 402
C1906 0.22uF 20% 6.3V X5R 402
C1907 0.22uF 20% 6.3V X5R 402
WAS A 330UF ELEC - CHECK WE CAN REMOVE

19 17 6 =PP2V5_S0_NB_VCCA_3GBG
C1916 0.1uF 20% 10V CERM 402
19 6 =PP1V5_S0_NB_VCCAUX
C1918 0.1uF 20% 10V CERM 402
19 17 6 =PP3V3_S0_NB_VCC_HV
C1914 10UF 20% 6.3V CERM 805-1
C1915 0.1uF 20% 10V CERM 402

U1901 MM157 — PP3V3_S0_NB_TVDAC

19 6 =PP5V_S0_NB_TVDAC
U1901 MM157 SOT23-5-LF
1 VIN VOUT 5 PP3V3_S0_NB_TVDAC VOLTAGE=3.3V
3 CONT NOISE 4 MM157_DN_NR
GND 2
MIN_LINE_WIDTH=1.0 mm MIN_NECK_WIDTH=0.35MM
C1940 1UF 10% 6.3V CERM 402
C1941 0.01uF 10% 16V CERM 402
C1942 1UF 10% 6.3V CERM 402

R1990 10 1% 1/16W MF-LF 402 — PP3V3_S0_NB_TVDAC_FOLLOW
VOLTAGE=3.3V MIN_LINE_WIDTH=1.0 mm MIN_NECK_WIDTH=0.35MM
D1986 BAT54DW SOT-363 =PP1V5_S0_NB 6 19
L1990 180-OHM-1.5A 0603 — PP3V3_S0_NB_TVDAC_F
VOLTAGE=3.3V MIN_LINE_WIDTH=1.0 mm MIN_NECK_WIDTH=0.35MM
C1992 22000pF~1000mA 16V NPM18 — PP3V3_S0_NB_VCCA_TVDACA 17
VOLTAGE=3.3V MIN_LINE_WIDTH=1.0 mm MIN_NECK_WIDTH=0.35MM
C1990 10UF 20% 6.3V CERM 805-1
C1991 0.1uF 20% 10V CERM 402

MCH VCCA_TVDACC FILTER

(MCH TV OUT CHANNEL A 3.3V PWR)

MCH VCCA_TVDACC FILTER

(MCH TV OUT CHANNEL B 3.3V PWR)

C1994 22000pF~1000mA 16V NPM18 — PP3V3_S0_NB_VCCA_TVDACB 17
VOLTAGE=3.3V MIN_LINE_WIDTH=1.0 mm MIN_NECK_WIDTH=0.35MM
C1993 0.1uF 20% 10V CERM 402
Layout Note: These 8 caps should be within 6.35 mm of NB edge

MCH VCCA_TVDACC FILTER

(MCH TV OUT CHANNEL C 3.3V PWR)

C1996 22000pF~1000mA 16V NPM18 — PP3V3_S0_NB_VCCA_TVDACC 17
VOLTAGE=3.3V MIN_LINE_WIDTH=1.0 mm MIN_NECK_WIDTH=0.35MM
C1995 0.1uF 20% 10V CERM 402

MCH VCCA_TVBG FILTER

(MCH TV DAC BAND GAP 3.3V PWR)

C1998 22000pF~1000mA 16V NPM18 — PP3V3_S0_NB_VCCA_TVBG 17
VOLTAGE=3.3V MIN_LINE_WIDTH=1.0 mm MIN_NECK_WIDTH=0.35MM
C1997 0.1uF 20% 10V CERM 402
GND_NB_VSSA_TVBG 17
Layout Note: Route to caps, then GND

L1923 / L1922 — GMCH VCCD_TVDAC / GMCH VCCD_QTVDAC FILTER

L1923 180-OHM-1.5A 0603
19 6 =PP1V5_S0_NB_TVDAC — PP1V5_S0_NB_TVDAC
VOLTAGE=1.5V MIN_LINE_WIDTH=1.0 mm MIN_NECK_WIDTH=0.35MM
C1924 10UF 20% 6.3V X5R 603
C1921 22000pF~1000mA 16V NPM18
GMCH VCCD_TVDAC FILTER (MCH TVDAC DEDICATED PWR 1.5V)
PP1V5_S0_NB_VCCD_TVDAC 17
VOLTAGE=1.5V MIN_LINE_WIDTH=1.0 mm MIN_NECK_WIDTH=0.35MM
C1920 0.1uF 20% 10V CERM 402
Layout Note: PLACE CAPS NEAR NB EDGE ON THESE 2 RAILS

L1922 180-OHM-1.5A 0603
PP1V5_S0_NB_QTVDAC
VOLTAGE=1.5V MIN_LINE_WIDTH=1.0 mm MIN_NECK_WIDTH=0.35MM
C1926 10UF 20% 6.3V X5R 603
C1923 22000pF~1000mA 16V NPM18
GMCH VCCD_QTVDAC FILTER (MCH TVDAC DIGITAL QUIET 1.5V PWR)
PP1V5_S0_NB_VCCD_QTVDAC 17
VOLTAGE=1.5V MIN_LINE_WIDTH=1.0 mm MIN_NECK_WIDTH=0.35MM
C1922 0.1uF 20% 10V CERM 402
C1927 10UF 20% 6.3V X5R 603

L1970 — PP1V5_S0_NB_VCC3G

19 6 =PP1V5_S0_NB_3GPLL
L1970 91NH 1210
Layout Note: Place L and C close to MCH
C1970 220UF 20% 2.5V POLY SMB2
PP1V5_S0_NB_VCC3G 17
VOLTAGE=1.5V MIN_LINE_WIDTH=1.0 mm MIN_NECK_WIDTH=0.2 MM
C1971 10UF 20% 6.3V CERM 805-1
C1972 10UF 20% 6.3V CERM 805-1
Layout Note: 10uF caps should be close to MCH on opposite side.

L1975 — PP1V5_S0_NB_3GPLL_F

1uH, 20%
19 6 =PP1V5_S0_NB_3GPLL
L1975 1.0UH-220MA-0.12-OHM 0805
PP1V5_S0_NB_3GPLL_F
VOLTAGE=1.5V MIN_LINE_WIDTH=1.0 mm MIN_NECK_WIDTH=0.2 MM
Should be 1%
R1975 0.51 1% 1/16W MF-LF 402
PP1V5_S0_NB_VCCA_3GPLL 17
VOLTAGE=1.5V MIN_LINE_WIDTH=1.0 mm MIN_NECK_WIDTH=0.2 MM
C1975 10UF 20% 6.3V CERM 805-1
C1976 0.1uF 20% 10V CERM 402
GND_NB_VSSA_3GBG 17
Layout Note: 3GPLL 10uF cap should be placed in cavity
Layout Note: Route to caps, then GND

NB (GM) Decoupling

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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D	051-7032	??
SCALE: NONE	SHT 19 OF 97	

NB_CFG<3>	RESERVED

NB_CFG<4>	RESERVED

14 NB_CFG<5>
Internal pull-up

NB_CFG<5> DMI x2 Select	High = DMIx4 Low = DMIx2

NBCFG_DMI_X2
R2075
2.2K
5%
1/16W
MF-LF
402

PROBABLY NOT NEEDED

NB_CFG<6>	RESERVED

14 NB_CFG<7>
Internal pull-up

NB_CFG<7> CPU Strap	High = Mobile CPU Low = RESERVED

NO STUFF
R2077
2.2K
5%
1/16W
MF-LF
402

NB_CFG<8>	RESERVED

14 NB_CFG<9>
Internal pull-up

NB_CFG<9> PCIE Graphics Lane Reversal	High = Normal Low = Reversed

NBCFG_PEG_REVERSE
R2079
2.2K
5%
1/16W
MF-LF
402

NB_CFG<10>	RESERVED

NB_CFG<11>	RESERVED

Internal pull-ups

NB_CFG<13:12>	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal Operation

NB_CFG<14>	RESERVED

NB_CFG<15>	RESERVED

14 NB_CFG<16>
Internal pull-up

NB_CFG<16> FSB Dynamic ODT	High = Enabled Low = Disabled

NBCFG_DYN_ODT_DISABLE
R2085
2.2K
5%
1/16W
MF-LF
402

NB_CFG<17>	RESERVED

=PP3V3_S0_NB 6 14 19 20
NBCFG_VCC_1V5
R2058
2.2K
5%
1/16W
MF-LF
402

NB_CFG<18> VCC Select	High = 1.5V Low = 1.05V

14 NB_CFG<18>
Internal pull-down

=PP3V3_S0_NB 6 14 19 20
NBCFG_DMI_REVERSE
R2059
2.2K
5%
1/16W
MF-LF
402

NB_CFG<19> DMI Lane Reversal	High = Reversed Low = Normal

14 NB_CFG<19>
Internal pull-down

945 External Design Spec says reserved

=PP3V3_S0_NB 6 14 19 20
NBCFG_SDVO_AND_PCIE
R2060
2.2K
5%
1/16W
MF-LF
402

NB_CFG<20> PCIe Backward Interop. Mode	High = Both active Low = Only SDVO or PCIe x1

14 NB_CFG<20>
Internal pull-down

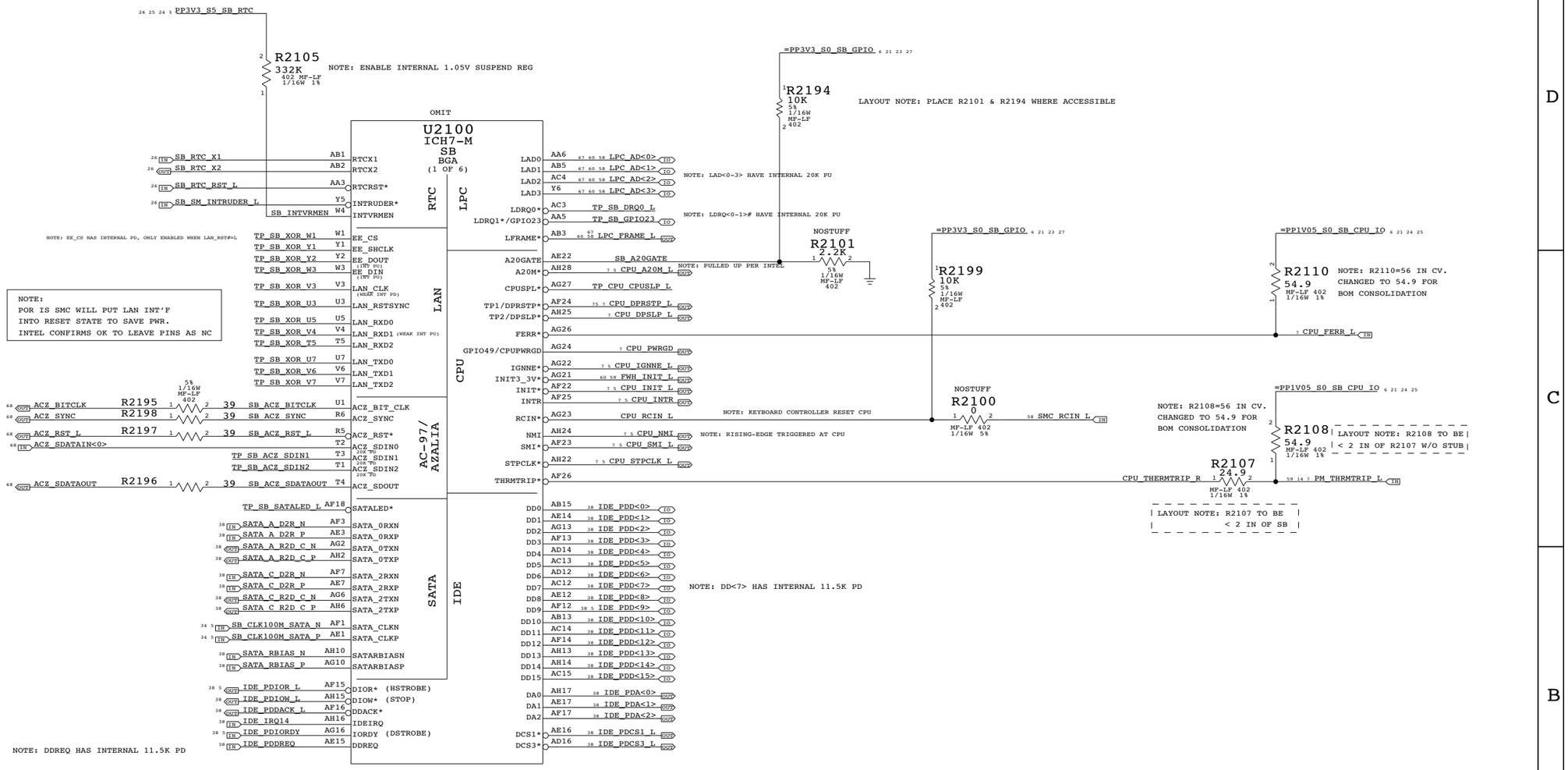
PROBABLY NOT NEEDED

NB Config Straps

SYNC_MASTER=M1 SYNC_DATE=01/05/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7032	??
SCALE: NONE	SHT 20 OF 97	



	AC '07	INTEL HIGH DEFINITION AUDIO
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN	INTERNAL 20K PD ONLY ENABLED IN S3COLD
ACZ_RST#	- LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	NONE
ACZ_SDIN[0-2]	INTERNAL 20K PD	INTERNAL 20K PD
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
ACZ_SYNC		INTERNAL 20K PD

SB: 1 OF 4

SYNC_MASTER=M38 SYNC_DATE=01/05/2006

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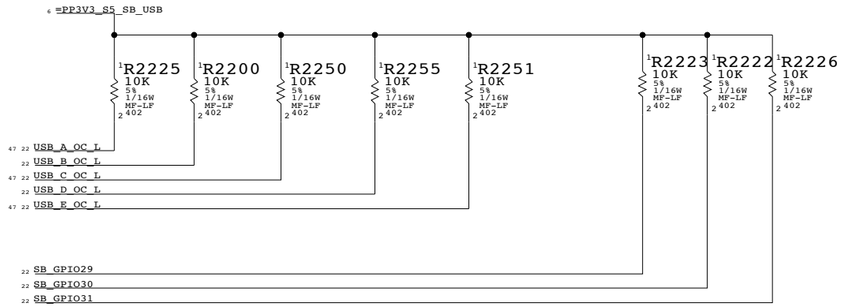
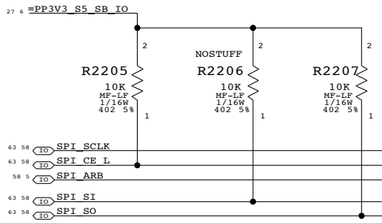
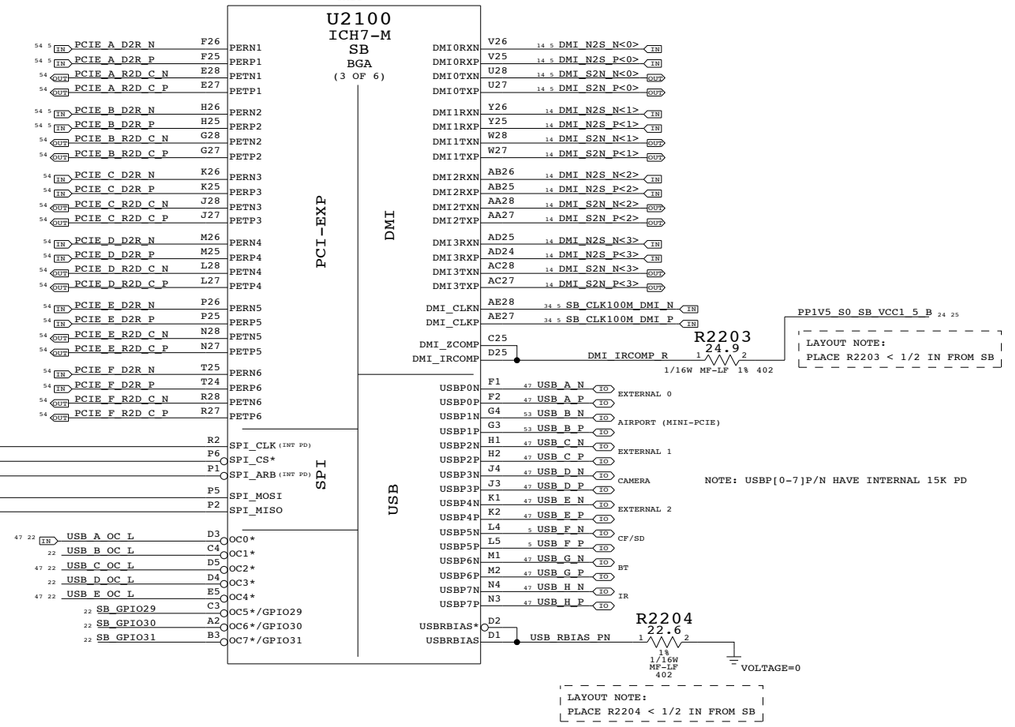
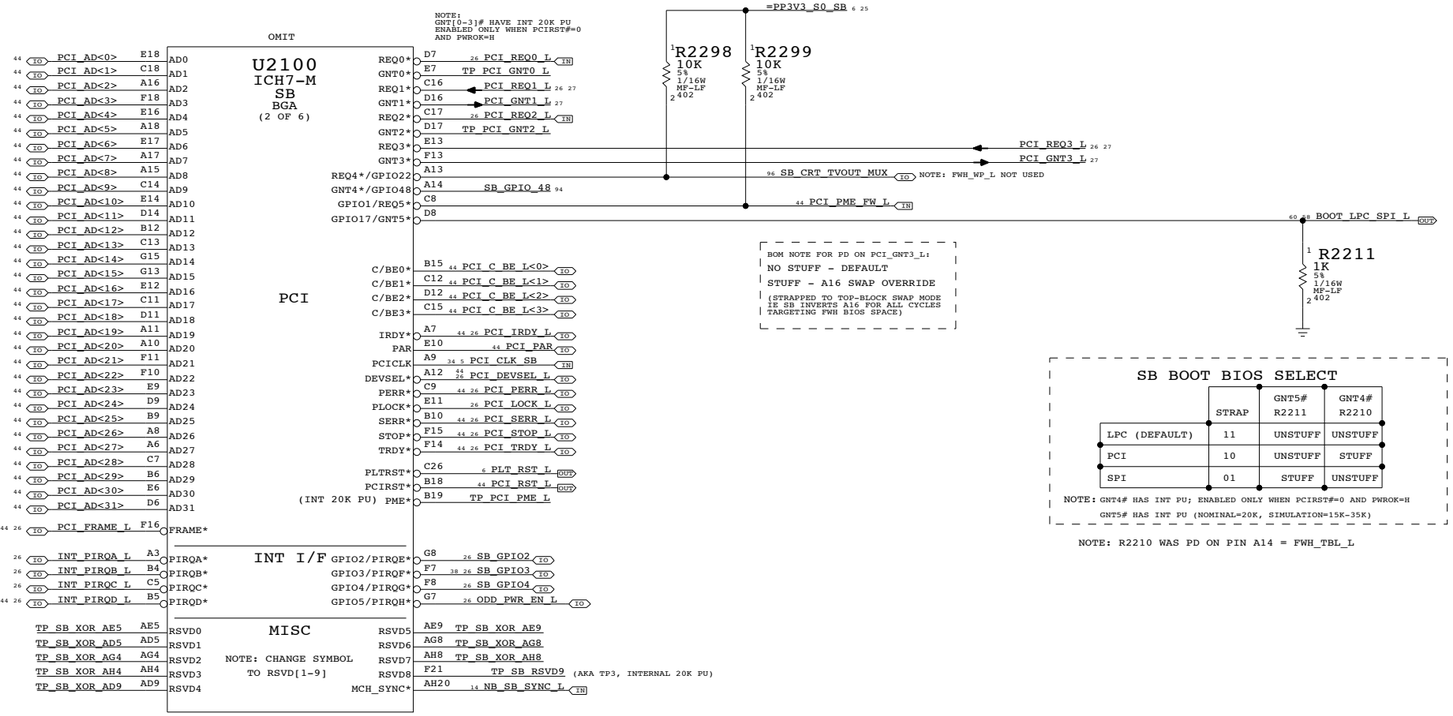
D	051-7032	??
SCALE: NONE	SHT 21 OF 97	









	STRAP	GNT5# R2211	GNT4# R2210
LPC (DEFAULT)	11	UNSTUFF	UNSTUFF
PCI	10	UNSTUFF	STUFF
SPI	01	STUFF	UNSTUFF

SB: 2 OF 4

SYNC_MASTER=MASTER SYNC_DATE=MASTER

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7032	??

SCALE: NONE SHT 22 OF 97

NOTE FOR R2323 (DEF=NOSTUFF)
STRAPPING 8 PWROK RISING:
SB WILL DISABLE TCO TIMER
SYSTEM REBOOT FEATURE

=PP3V3_S0_SB_GPIO 6 21 23 27

=PP3V3_S5_SB 6 23 25 26

26 25 23 6 =PP3V3_S5_SB

R2318 10K 1/16W 402 MF-LF 5%
R2395 8.2K 1/16W 402 MF-LF 5%
R2396 10K 1/16W 402 MF-LF 5%
R2397 8.2K 1/16W 402 MF-LF 5%
R2327 10K 1/16W 402 MF-LF 5% NOSTUFF
R2326 10K 1/16W 402 MF-LF 5% NOSTUFF
R2323 1K 1/16W 402 MF-LF 5% NO_REBOOT_MODE

RP2300 10K 5% 1/16W SM-LF

R2398 1K 1/16W 402 MF-LF 5%
R2320 10K 1/16W 402 MF-LF 5%
R2317 10K 1/16W 402 MF-LF 5%
R2316 10K 1/16W 402 MF-LF 5%

OMIT

U2100
ICH7-M
SB
BGA
(4 OF 6)

SMB

27 TO SMB_CLK — C22 SMBCLK
27 TO SMB_DATA — B22 SMBDATA
SMB_LINK_ALERT_L — A26 LINKALERT*
SMLINK<0> — B25 SMLINK0
NOT USED — SMLINK<1> — A25 SMLINK1

PM_RI_L — A28 RI*
SB_SPKR — A19 SPKR (INT WEAK PD)
67 60 58 OUT PM_SUS_STAT_L — A27 SUS_STAT*
58 26 5 IN PM_SYSRST_L — A22 SYS_RST*
14 IN PM_BMBUSY_L — AB18 GPIO0/BM_BUSY*
SMB_ALERT_L — B23 GPIO11/SMBALERT*
NOTE: RESERVED FOR FUTURE

33 OUT PM_STPPCI_L — AC20 GPIO18/STPPCI*
34 OUT PM_STPCPU_L — AF21 GPIO20/STPCPU*
SB_GPIO26 — A21 GPIO26
23 BIOS_REC — B21 GPIO27
23 FWH_MFG_MODE — E23 GPIO28
67 60 58 44 5 TO PM_CLKRUN_L — AG18 GPIO32/CLKRUN*

RESERVED FOR MOBILE
AZALIA DOCKING INT'F
TP_AZ_DOCK_EN_L — AC19 GPIO33/AZ_DOCK_EN*
TP_AZ_DOCK_RST_L — U2 GPIO34/AZ_DOCK_RST*

53 41 IN PCIE_WAKE_L — F20 WAKE*
67 60 58 TO INT_SERIRQ — AH21 SERIRQ
58 10 IN PM_THRM_L — AF20 THRM*
26 IN VR_PWRGD_CK410 — AD22 VRMPWRGD
TO TP_SB_GPIO6 — AC21 GPIO6
58 IN SMC_RUNTIME_SCI_L — AC18 GPIO7
58 IN SMC_EXTSMI_L — E21 GPIO8

SYS GPIO

PWR MNGT

SATA GPIO
GPIO21/SATA0GP — AF19 SB_GPIO21 — 100 — R2302
GPIO19/SATA1GP — AH18 SB_GPIO19 — 100 — R2303
GPIO36/SATA2GP — AH19
GPIO37/SATA3GP — AE19 SB_GPIO37 — 100 — R2305
38 SATA_C_DET_L IN

CLKS
CLK14 — AC1 — 34 5 SB_CLK14P3M_TIMER IN
CLK48 — B2 — 34 5 SB_CLK48M_USBCTLR IN
SUSCLK — C20 — 58 SUS_CLK_SB OUT

SLP_S3* — B24 — 80 79 77 58 PM_SLP_S3_L OUT
SLP_S4* — D23 — 77 58 PM_SLP_S4_L OUT
SLP_S5* — F22 — 58 PM_SLP_S5_L OUT
PWROK — AA4 — 26 PM_SB_PWROK IN
GPIO16/DPRSLPVR — AC22 — 75 14 PM_DPRSLPVR OUT
TP0/BATLOW* — C21 — NOTE: DPRSLPVR HAS INT 20K PD, ENABLED AT BOOT/RESET FOR STRAPPING FCN
(INT 20K PU) PWRBTN* — C23 — 58 PM_PWRBTN_L IN
LAN_RST* — C19 — 58 PM_LAN_ENABLE IN — NOTE: SMC WILL DRIVE 0-1-0 TO KEEP LAN INT'F IN RESET STATE TO SAVE PWR
RSMRST* — Y4

GPIO9 — E20 — 58 26 SMS_INT_L IN
GPIO10 — A20 — 58 SMC_SB_NMI IN
DEF=GPI GPIO12 — F19 — 23 PATA_PWR_EN_L OUT
GPIO13
DEF=GPI GPIO14 — R4 — 38 IDE_RESET_L OUT
GPIO15 — E22 — SV_SET_UP 23 60
GPIO24 — R3 — CRB_SV_DET 23
GPIO25 — D20 — TP_SB_GPIO25_DO_NOT_USE
OD GPIO35 — AD21 — 23 SB_CLK100M_SATA_OE_L OUT
GPIO38 — AD20 — TP_SB_GPIO38 TO
DEF=GPI GPIO39 — AE20 — 23 SATA_C_PWR_EN_L OUT

GPIO

NOTE FOR GPIO25:
- HAS INTERNAL 20K PU, ENABLED DURING RSMRST# AND DISABLED WITHIN 100MS AFTER RSMRST# DEASSERTS
- CAN NOT BE LOW FOR 350S AFTER RSMRST# ON BOOT (DMI AC COUPLING MODE STRAP)

=PP3V3_S5_SB_PM 6 11

R2387 NOSTUFF 10K 1/16W 402 MF-LF 5%
R2319 10K 1/16W 402 MF-LF 5%
R2343 8.2K 5% 1/16W 402 MF-LF

R2399 100K 5% 1/16W 402 MF-LF

58 PM_BATLOW_L IN
58 PM_RSMRST_L IN
58 SMC_WAKE_SCI_L IN

NOTE:
SV_SET_UP IS LINDACARD DETECT
HI = PRESENT
LO = NOT PRESENT

26 25 23 6 =PP3V3_S5_SB

R2306 NOSTUFF 10K 1/16W 402 MF-LF 5%
R2308 10K 1/16W 402 MF-LF 5%
R2307 10K 1/16W 402 MF-LF 5%
R2309 NOSTUFF 0 1/16W 402 MF-LF 5%

SV_SET_UP 23 60
CRB_SV_DET 23

LAYOUT NOTE:
PLACE R2306-14 WHERE PHYSICALLY ACCESSIBLE

26 25 23 6 =PP3V3_S5_SB

R2313 10K 1/16W 402 MF-LF 5%
R2310 10K 1/16W 402 MF-LF 5%
R2314 NOSTUFF 0 1/16W 402 MF-LF 5%
R2311 NOSTUFF 10K 1/16W 402 MF-LF 5%

FWH_MFG_MODE 23
BIOS_REC 23

=PP3V3_S5_SB 6 23 25 26

R2390 10K 5% 1/16W MF-LF 402
23 PATA_PWR_EN_L

=PP3V3_S0_SB_GPIO 6 21 23 27

R2388 10K 5% 1/16W MF-LF 402
23 SATA_C_PWR_EN_L

SB: 3 OF 4

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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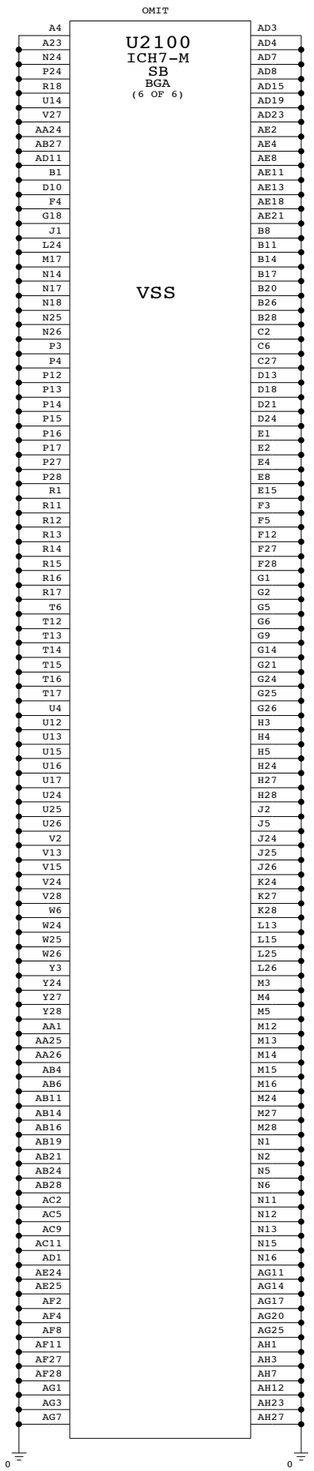

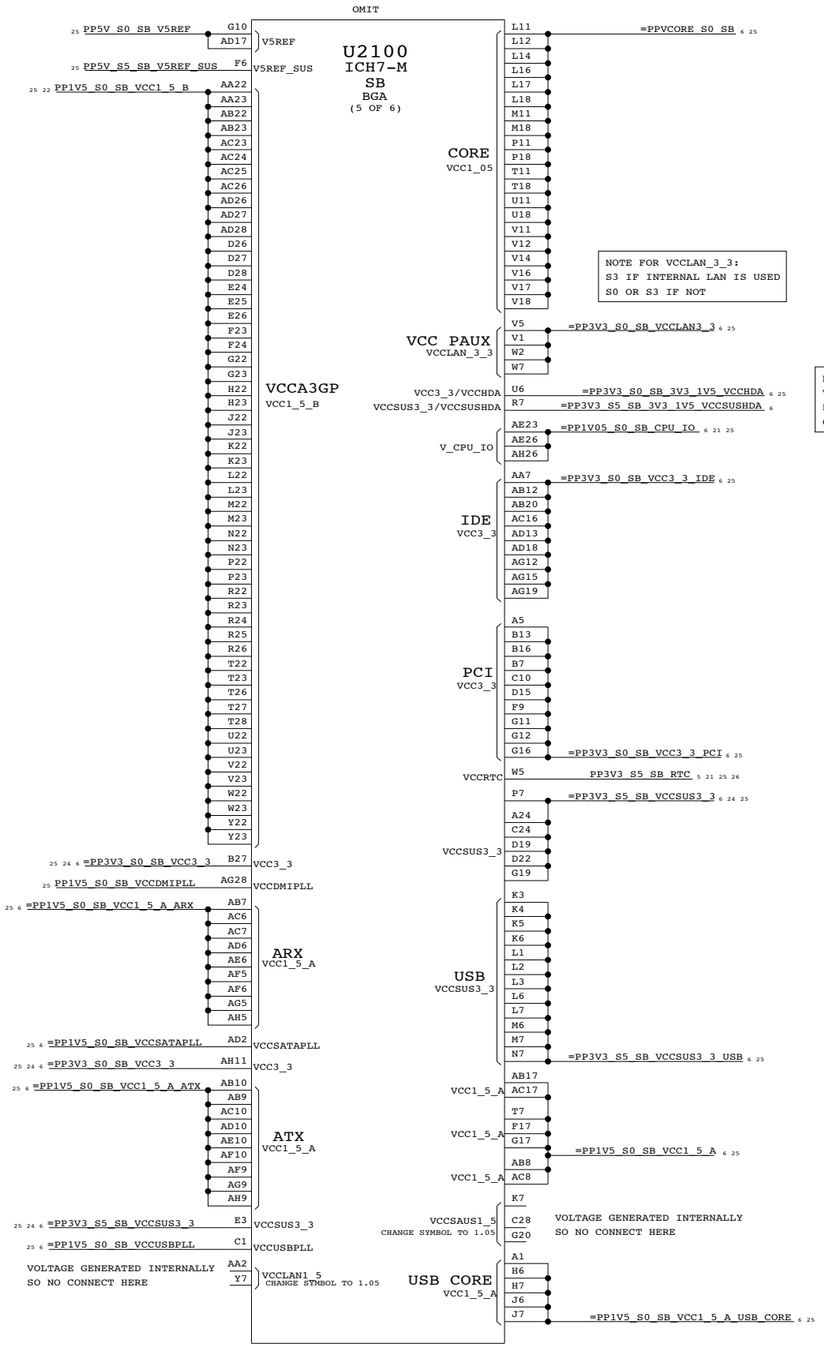

SB: 4 OF 4

SYNC_MASTER=M38 SYNC_DATE=01/05/2006

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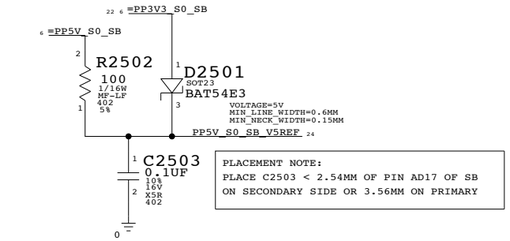
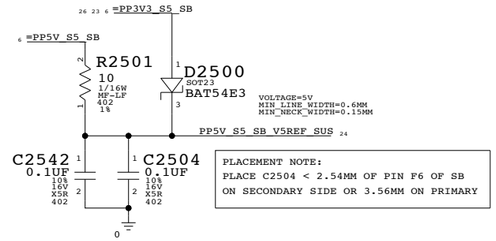
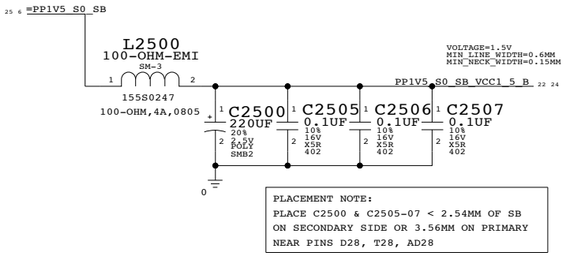
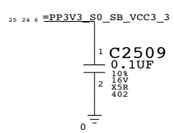
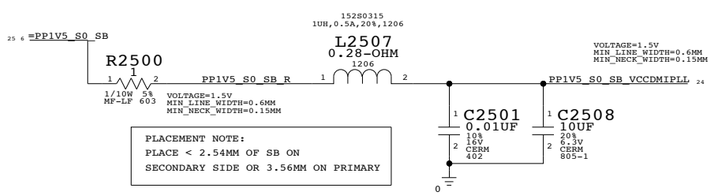
SCALE: NONE	SHT 24 OF 97	

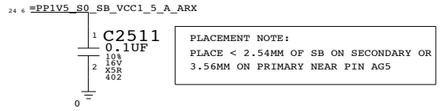


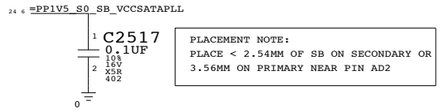


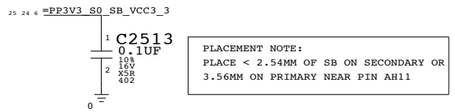


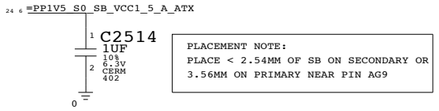


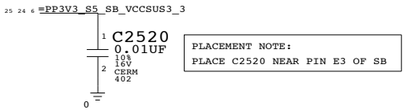


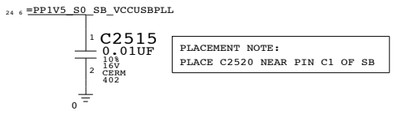


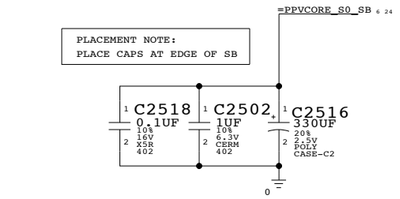


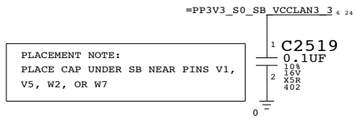


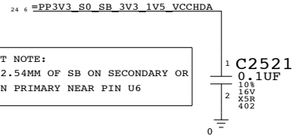


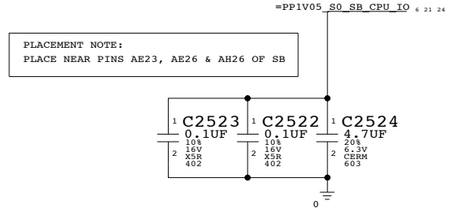


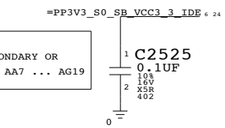


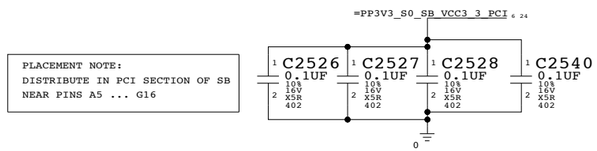


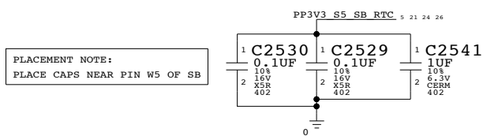


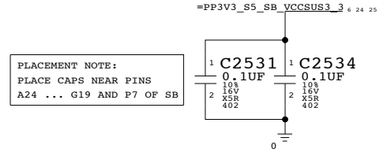


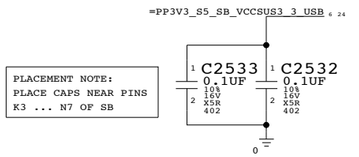


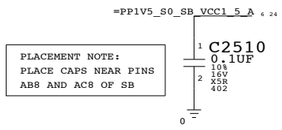


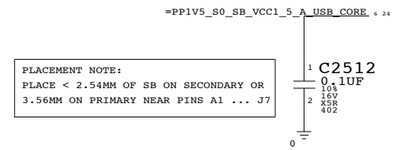












SB:DECOUPLING

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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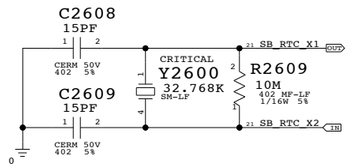
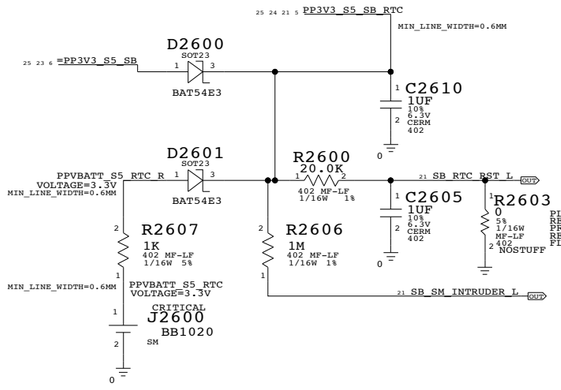
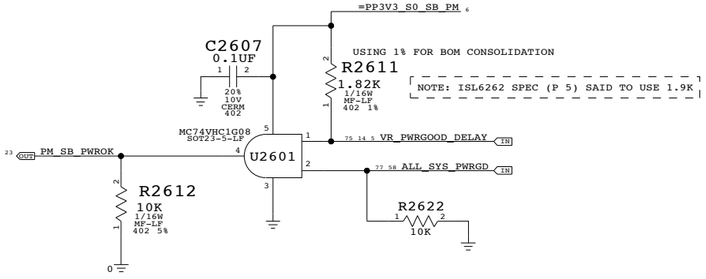
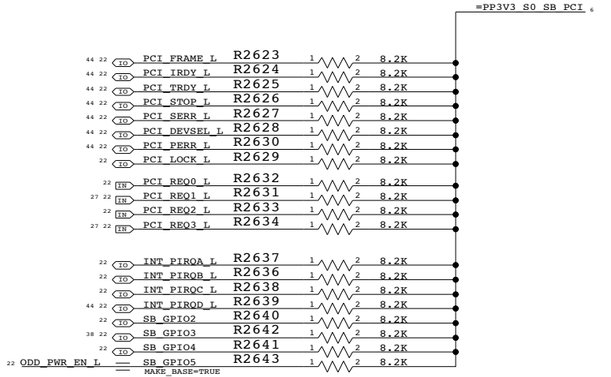
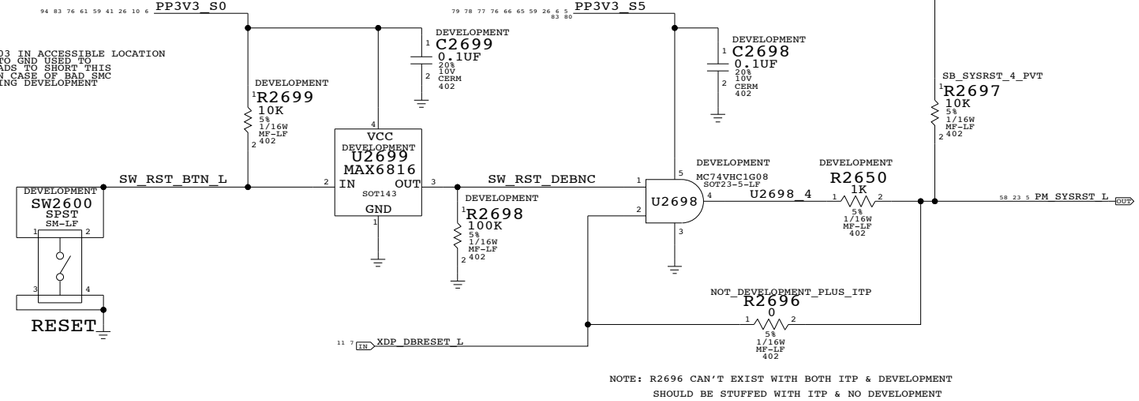
SIZE	DRAWING NUMBER	REV.
D	051-7032	??
SCALE: NONE	SHT 25 OF 97	



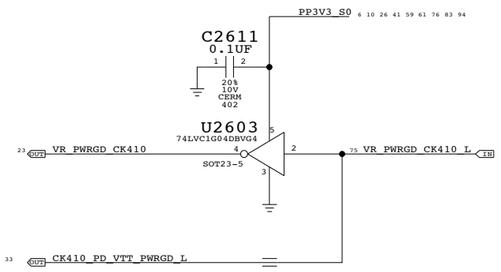








NOTE: R2696 CAN'T EXIST WITH BOTH ITP & DEVELOPMENT
SHOULD BE STUFFED WITH ITP & NO DEVELOPMENT



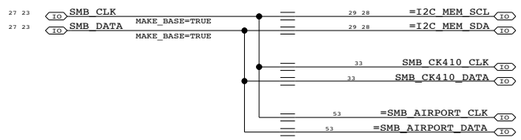
SB: MISC

SYNC_MASTER=MASTER SYNC_DATE=MASTER

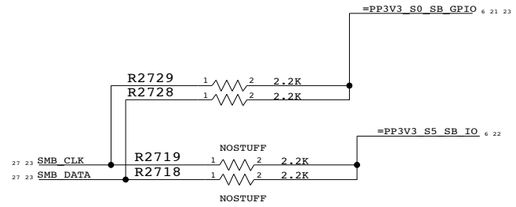
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7032	??
SCALE: NONE	SHT 26 OF 97	

SB I2C BUSSES



PCI CONTROL



SB: SMB HUB AND ALIAS

SYNC_MASTER=MASTER SYNC_DATE=MASTER

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7032	??
SCALE: NONE	SHT 27 OF 97	

Page Notes

Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_MEM_SCL
- =I2C_MEM_SDA

BOM options provided by this page:
(NONE)

DDR2 VRef

One 0.1uF per connector

=PP1V8_S3_MEM

R2800 1K 1% 1/16W MF-LF 402

MEM_VREF (5 28 29)
VOLTAGE=0.9V
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm

R2801 1K 1% 1/16W MF-LF 402

Yellow uses 10K divider and TLV2463
to drive MCH and DIMM connectors.
(See Capell Valley pg 47)

MEM_VREF (29 28 5)

C2850 2.2UF 10% 6.3V CERM1 603

C2800 0.1uF 20% 10V CERM 402

=PP1V8_S3_MEM (29 28 6 5)

CRITICAL
J2800
F-RT-SM1
DDR2-SODIMM-STD

	1	VREF	VSS0	2			
	3	VSS1	DQ4	4	MEM_A_DQ<4>		15
15	MEM_A_DQ<0>	5	DQ0	DQ5	6	MEM_A_DQ<5>	15
15	MEM_A_DQ<1>	7	DQ1	VSS2	8		
	9	VSS4	DM0	10	MEM_A_DM<0>		15
15 5	MEM_A_DQS_N<0>	11	DQS0*	VSS5	12		
15 5	MEM_A_DQS_P<0>	13	DQS0	DQ6	14	MEM_A_DQ<6>	15
	15	VSS6	DQ7	16	MEM_A_DQ<7>		5 15
15	MEM_A_DQ<2>	17	DQ2	VSS7	18		
15	MEM_A_DQ<3>	19	DQ3	DQ12	20	MEM_A_DQ<12>	15
	21	VSS8	DQ13	22	MEM_A_DQ<13>		15
15	MEM_A_DQ<8>	23	DQ8	VSS9	24		
15	MEM_A_DQ<9>	25	DQ9	DM1	26	MEM_A_DM<1>	15
	27	VSS10	VSS11	28			
15 5	MEM_A_DQS_N<1>	29	DQS1*	CK0	30	MEM_CLK_P<0>	14
15 5	MEM_A_DQS_P<1>	31	DQS1	CK0*	32	MEM_CLK_N<0>	14
	33	VSS12	VSS13	34			
15	MEM_A_DQ<10>	35	DQ10	DQ14	36	MEM_A_DQ<14>	5 15
15	MEM_A_DQ<11>	37	DQ11	DQ15	38	MEM_A_DQ<15>	15
	39	VSS14	VSS15	40			
		KEY					
	41	VSS16	VSS17	42			
15 5	MEM_A_DQ<16>	43	DQ16	DQ20	44	MEM_A_DQ<20>	15
15	MEM_A_DQ<17>	45	DQ17	DQ21	46	MEM_A_DQ<21>	15
	47	VSS18	VSS19	48			
15 5	MEM_A_DQS_N<2>	49	DQS2*	NC0	50	DIMM_OVERTEMP_L	29 59
15 5	MEM_A_DQS_P<2>	51	DQS2	DM2	52	MEM_A_DM<2>	15
	53	VSS21	VSS22	54			
15	MEM_A_DQ<18>	55	DQ18	DQ22	56	MEM_A_DQ<22>	15
15	MEM_A_DQ<19>	57	DQ19	DQ23	58	MEM_A_DQ<23>	15
	59	VSS23	VSS24	60			
15	MEM_A_DQ<24>	61	DQ24	DQ28	62	MEM_A_DQ<28>	15
15 5	MEM_A_DQ<25>	63	DQ25	DQ29	64	MEM_A_DQ<29>	15
	65	VSS25	VSS26	66			
15	MEM_A_DM<3>	67	DM3	DQS3*	68	MEM_A_DQS_N<3>	5 15
NC		69	NC1	DQS3	70	MEM_A_DQS_P<3>	5 15
	71	VSS27	VSS28	72			
15	MEM_A_DQ<26>	73	DQ26	DQ30	74	MEM_A_DQ<30>	15
15	MEM_A_DQ<27>	75	DQ27	DQ31	76	MEM_A_DQ<31>	15
	77	VSS29	VSS30	78			
30 14	MEM_CKE<0>	79	CKE0	NC/CKE1	80	MEM_CKE<1>	14 30
	81	VDD0	VDD1	82			
NC		83	NC2	NC/A15	84	TP_MEM_A_A<15>	
30 15	MEM_A_BS<2>	85	BA2	NC/A14	86	TP_MEM_A_A<14>	
	87	VDD2	VDD3	88			
30 15	MEM_A_A<12>	89	A12	A11	90	MEM_A_A<11>	15 30
30 15	MEM_A_A<9>	91	A9	A7	92	MEM_A_A<7>	15 30
30 15	MEM_A_A<8>	93	A8	A6	94	MEM_A_A<6>	15 30
	95	VDD4	VDD5	96			
30 15	MEM_A_A<5>	97	A5	A4	98	MEM_A_A<4>	15 30
30 15	MEM_A_A<3>	99	A3	A2	100	MEM_A_A<2>	15 30
30 15	MEM_A_A<1>	101	A1	A0	102	MEM_A_A<0>	15 30
	103	VDD6	VDD7	104			
30 15	MEM_A_A<10>	105	A10/AP	BA1	106	MEM_A_BS<1>	15 30
30 15	MEM_A_BS<0>	107	BA0	RAS*	108	MEM_A_RAS_L	15 30
30 15	MEM_A_WE_L	109	WE*	S0*	110	MEM_CS_L<0>	14 30
	111	VDD8	VDD9	112			
30 15	MEM_A_CAS_L	113	CAS*	ODT0	114	MEM_ODT<0>	14 30
30 14	MEM_CS_L<1>	115	NC/S1*	NC/A13	116	MEM_A_A<13>	15 30
	117	VDD10	VDD11	118			
30 14	MEM_ODT<1>	119	NC/ODT1	NC3	120	NC	
	121	VSS31	VSS32	122			
15	MEM_A_DQ<32>	123	DQ32	DQ36	124	MEM_A_DQ<36>	15
15	MEM_A_DQ<33>	125	DQ33	DQ37	126	MEM_A_DQ<37>	15
	127	VSS33	VSS34	128			
15 5	MEM_A_DQS_N<4>	129	DQS4*	DM4	130	MEM_A_DM<4>	15
15 5	MEM_A_DQS_P<4>	131	DQS4	VSS35	132		
	133	VSS36	DQ38	134	MEM_A_DQ<38>		15
15	MEM_A_DQ<34>	135	DQ34	DQ39	136	MEM_A_DQ<39>	5 15
15	MEM_A_DQ<35>	137	DQ35	VSS37	138		
	139	VSS38	DQ44	140	MEM_A_DQ<44>		15
15	MEM_A_DQ<40>	141	DQ40	DQ45	142	MEM_A_DQ<45>	15
15	MEM_A_DQ<41>	143	DQ41	VSS39	144		
	145	VSS40	DQS5*	146	MEM_A_DQS_N<5>		5 15
15	MEM_A_DM<5>	147	DM5	DQS5	148	MEM_A_DQS_P<5>	5 15
	149	VSS41	VSS42	150			
15	MEM_A_DQ<42>	151	DQ42	DQ46	152	MEM_A_DQ<46>	15
15	MEM_A_DQ<43>	153	DQ43	DQ47	154	MEM_A_DQ<47>	5 15
	155	VSS43	VSS44	156			
15	MEM_A_DQ<48>	157	DQ48	DQ52	158	MEM_A_DQ<52>	15
15	MEM_A_DQ<49>	159	DQ49	DQ53	160	MEM_A_DQ<53>	15
	161	VSS45	VSS46	162			
NC		163	NC_TEST	CK1	164	MEM_CLK_P<1>	14
	165	VSS47	CK1*	166	MEM_CLK_N<1>		14
15 5	MEM_A_DQS_N<6>	167	DQS6*	VSS48	168		
15 5	MEM_A_DQS_P<6>	169	DQS6	DM6	170	MEM_A_DM<6>	15
	171	VSS49	VSS50	172			
15	MEM_A_DQ<50>	173	DQ50	DQ54	174	MEM_A_DQ<54>	5 15
15	MEM_A_DQ<51>	175	DQ51	DQ55	176	MEM_A_DQ<55>	15
	177	VSS51	VSS52	178			
15	MEM_A_DQ<56>	179	DQ56	DQ60	180	MEM_A_DQ<60>	15
15	MEM_A_DQ<57>	181	DQ57	DQ61	182	MEM_A_DQ<61>	15
	183	VSS53	VSS54	184			
15	MEM_A_DM<7>	185	DM7	DQS7*	186	MEM_A_DQS_N<7>	5 15
	187	VSS55	DQS7	188	MEM_A_DQS_P<7>		5 15
15	MEM_A_DQ<58>	189	DQ58	VSS56	190		
15 5	MEM_A_DQ<59>	191	DQ59	DQ62	192	MEM_A_DQ<62>	15
	193	VSS57	DQ63	194	MEM_A_DQ<63>		15
29 27	=I2C_MEM_SDA	195	SDA	VSS58	196		
29 27	=I2C_MEM_SCL	197	SCL	SA0	198		
	199	VDDSPD	SA1	200	ADDR=0xA0(WR)/0xA1(RD)		
	201	202	203	204	205	GND	

516S0403

ALL NC'S

=PPSPD_S0_MEM (29 6)

C2851 2.2UF 10% 6.3V CERM1 603

C2852 0.1uF 20% 10V CERM 402

DDR2 Bypass Caps

(For return current)

=PP1V8_S3_MEM (29 28 6 5)

C2801 10UF 20% 6.3V X5R 603
C2802 10UF 20% 6.3V X5R 603
C2803 10UF 20% 6.3V X5R 603
C2804 10UF 20% 6.3V X5R 603

C2810 0.1uF 20% 10V CERM 402
C2811 0.1uF 20% 10V CERM 402
C2812 0.1uF 20% 10V CERM 402
C2813 0.1uF 20% 10V CERM 402

C2814 0.1uF 20% 10V CERM 402
C2815 0.1uF 20% 10V CERM 402
C2816 0.1uF 20% 10V CERM 402
C2817 0.1uF 20% 10V CERM 402

C2818 0.1uF 20% 10V CERM 402
C2819 0.1uF 20% 10V CERM 402
C2820 0.1uF 20% 10V CERM 402
C2821 0.1uF 20% 10V CERM 402

=PP1V8_S3_MEM (5 6 28 29)

DDR2 SO-DIMM Connector A

SYNC_MASTER=MASTER SYNC_DATE=MASTER

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7032	??
SCALE: NONE	SHT 28 OF 97	

Page Notes

Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_MEM_SCL
- =I2C_MEM_SDA

BOM options provided by this page:
(NONE)

NOTE: This page does not supply VREF.
The reference voltage must be provided
by another page.

=PP1V8_S3_MEM

MEM_VREF

C2950 2.2UF 10% 6.3V CERM1 603
C2900 0.1uF 20% 10V CERM 402

CRITICAL
J2900
F-RT-SM1
DDR2-SODIMM-REV

1	VREF		VSS0	2			
3	VSS1		DQ4	4	MEM_B_DQ<4>	15	
5	DQ0	MEM_B_DQ<0>	15	DQ5	6	MEM_B_DQ<5>	15
7	DQ1	MEM_B_DQ<1>	15	VSS2	8		
9	VSS4		DM0	10	MEM_B_DM<0>	15	
11	DQS0*	MEM_B_DQS_N<0>	15 5	VSS5	12		
13	DQS0	MEM_B_DQS_P<0>	15 5	DQ6	14	MEM_B_DQ<6>	5 15
15	VSS6		DQ7	16	MEM_B_DQ<7>	15	
17	DQ2	MEM_B_DQ<2>	15	VSS7	18		
19	DQ3	MEM_B_DQ<3>	15	DQ12	20	MEM_B_DQ<12>	15
21	VSS8		DQ13	22	MEM_B_DQ<13>	15	
23	DQ8	MEM_B_DQ<8>	15 5	VSS9	24		
25	DQ9	MEM_B_DQ<9>	15	DM1	26	MEM_B_DM<1>	15
27	VSS10		VSS11	28			
29	DQS1*	MEM_B_DQS_N<1>	15 5	CK0	30	MEM_CLK_P<3>	14
31	DQS1	MEM_B_DQS_P<1>	15 5	CK0*	32	MEM_CLK_N<3>	14
33	VSS12		VSS13	34			
35	DQ10	MEM_B_DQ<10>	15	DQ14	36	MEM_B_DQ<14>	15
37	DQ11	MEM_B_DQ<11>	15	DQ15	38	MEM_B_DQ<15>	15
39	VSS14		VSS15	40			
KEY							
41	VSS16		VSS17	42			
43	DQ16	MEM_B_DQ<16>	15	DQ20	44	MEM_B_DQ<20>	15
45	DQ17	MEM_B_DQ<17>	15	DQ21	46	MEM_B_DQ<21>	15
47	VSS18		VSS19	48			
49	DQS2*	MEM_B_DQS_N<2>	15 5	NC0	50	DIMM_OVERTEMP_L	28 59
51	DQS2	MEM_B_DQS_P<2>	15 5	DM2	52	MEM_B_DM<2>	15
53	VSS21		VSS22	54			
55	DQ18	MEM_B_DQ<18>	15	DQ22	56	MEM_B_DQ<22>	15
57	DQ19	MEM_B_DQ<19>	15	DQ23	58	MEM_B_DQ<23>	5 15
59	VSS23		VSS24	60			
61	DQ24	MEM_B_DQ<24>	15	DQ28	62	MEM_B_DQ<28>	15
63	DQ25	MEM_B_DQ<25>	15 5	DQ29	64	MEM_B_DQ<29>	15
65	VSS25		VSS26	66			
67	DM3	MEM_B_DM<3>	15	DQS3*	68	MEM_B_DQS_N<3>	5 15
69	NC1	NC		DQS3	70	MEM_B_DQS_P<3>	5 15
71	VSS27		VSS28	72			
73	DQ26	MEM_B_DQ<26>	15	DQ30	74	MEM_B_DQ<30>	15
75	DQ27	MEM_B_DQ<27>	15	DQ31	76	MEM_B_DQ<31>	15
77	VSS29		VSS30	78			
79	CKE0	MEM_CKE<2>	30 14	NC/CKE1	80	MEM_CKE<3>	14 30
81	VDD0		VDD1	82			
83	NC2	NC		NC/A15	84	TP_MEM_B_A<15>	5
85	BA2	MEM_B_BS<2>	30 15	NC/A14	86	TP_MEM_B_A<14>	5
87	VDD2		VDD3	88			
89	A12	MEM_B_A<12>	30 15	A11	90	MEM_B_A<11>	15 30
91	A9	MEM_B_A<9>	30 15	A7	92	MEM_B_A<7>	15 30
93	A8	MEM_B_A<8>	30 15	A6	94	MEM_B_A<6>	15 30
95	VDD4		VDD5	96			
97	A5	MEM_B_A<5>	30 15	A4	98	MEM_B_A<4>	15 30
99	A3	MEM_B_A<3>	30 15	A2	100	MEM_B_A<2>	15 30
101	A1	MEM_B_A<1>	30 15	A0	102	MEM_B_A<0>	15 30
103	VDD6		VDD7	104			
105	A10/AP	MEM_B_A<10>	30 15	BA1	106	MEM_B_BS<1>	15 30
107	BA0	MEM_B_BS<0>	30 15	RAS*	108	MEM_B_RAS_L	15 30
109	WE*	MEM_B_WE_L	30 15	S0*	110	MEM_CS_L<2>	14 30
111	VDD8		VDD9	112			
113	CAS*	MEM_B_CAS_L	30 15	ODT0	114	MEM_ODT<2>	14 30
115	NC/S1*	MEM_CS_L<3>	30 14	NC/A13	116	MEM_B_A<13>	15 30
117	VDD10		VDD11	118			
119	NC/ODT1	MEM_ODT<3>	30 14	NC3	120	NC	
121	VSS31		VSS32	122			
123	DQ32	MEM_B_DQ<32>	15	DQ36	124	MEM_B_DQ<36>	15
125	DQ33	MEM_B_DQ<33>	15	DQ37	126	MEM_B_DQ<37>	15
127	VSS33		VSS34	128			
129	DQS4*	MEM_B_DQS_N<4>	15 5	DM4	130	MEM_B_DM<4>	15
131	DQS4	MEM_B_DQS_P<4>	15 5	VSS35	132		
133	VSS36		DQ38	134	MEM_B_DQ<38>	5 15	
135	DQ34	MEM_B_DQ<34>	15	DQ39	136	MEM_B_DQ<39>	15
137	DQ35	MEM_B_DQ<35>	15	VSS37	138		
139	VSS38		DQ44	140	MEM_B_DQ<44>	5 15	
141	DQ40	MEM_B_DQ<40>	15	DQ45	142	MEM_B_DQ<45>	15
143	DQ41	MEM_B_DQ<41>	15	VSS39	144		
145	VSS40		DQS5*	146	MEM_B_DQS_N<5>	5 15	
147	DM5	MEM_B_DM<5>	15	DQS5	148	MEM_B_DQS_P<5>	5 15
149	VSS41		VSS42	150			
151	DQ42	MEM_B_DQ<42>	15	DQ46	152	MEM_B_DQ<46>	15
153	DQ43	MEM_B_DQ<43>	15	DQ47	154	MEM_B_DQ<47>	15
155	VSS43		VSS44	156			
157	DQ48	MEM_B_DQ<48>	15 5	DQ52	158	MEM_B_DQ<52>	15
159	DQ49	MEM_B_DQ<49>	15	DQ53	160	MEM_B_DQ<53>	15
161	VSS45		VSS46	162			
163	NC_TEST	NC		CK1	164	MEM_CLK_P<2>	14
165	VSS47		CK1*	166	MEM_CLK_N<2>	14	
167	DQS6*	MEM_B_DQS_N<6>	15 5	VSS48	168		
169	DQS6	MEM_B_DQS_P<6>	15 5	DM6	170	MEM_B_DM<6>	15
171	VSS49		VSS50	172			
173	DQ50	MEM_B_DQ<50>	15	DQ54	174	MEM_B_DQ<54>	15
175	DQ51	MEM_B_DQ<51>	15	DQ55	176	MEM_B_DQ<55>	15
177	VSS51		VSS52	178			
179	DQ56	MEM_B_DQ<56>	15	DQ60	180	MEM_B_DQ<60>	15
181	DQ57	MEM_B_DQ<57>	15	DQ61	182	MEM_B_DQ<61>	15
183	VSS53		VSS54	184			
185	DM7	MEM_B_DM<7>	15	DQS7*	186	MEM_B_DQS_N<7>	5 15
187	VSS55		DQS7	188	MEM_B_DQS_P<7>	5 15	
189	DQ58	MEM_B_DQ<58>	15	VSS56	190		
191	DQ59	MEM_B_DQ<59>	15	DQ62	192	MEM_B_DQ<62>	5 15
193	VSS57		DQ63	194	MEM_B_DQ<63>	15	
195	SDA	I2C_MEM_SDA	28 27	VSS58	196		
197	SCL	I2C_MEM_SCL	28 27	SA0	198	ADDR=0XA4(WR)/0XA5(RD)	
199	VDDSPD		SA1	200	MEM_B_SPD_SA1		
201	GND		ALL NC'S				
202							
203							
204							
205							

516S0404

=PPSPD_S0_MEM

C2951 2.2UF 10% 6.3V CERM1 603
C2952 0.1uF 20% 10V CERM 402

=PPSPD_S0_MEM

R2900 10K 5% 1/16W MF-LF 402

Resistor prevents pwr-gnd short

DDR2 Bypass Caps

(For return current)

=PP1V8_S3_MEM

C2908 C2909 C2910 C2911
C2912 C2913 C2914 C2915
C2916 C2917 C2918 C2919
C2920 C2921 C2922 C2923

1UF 10% 6.3V CERM 402

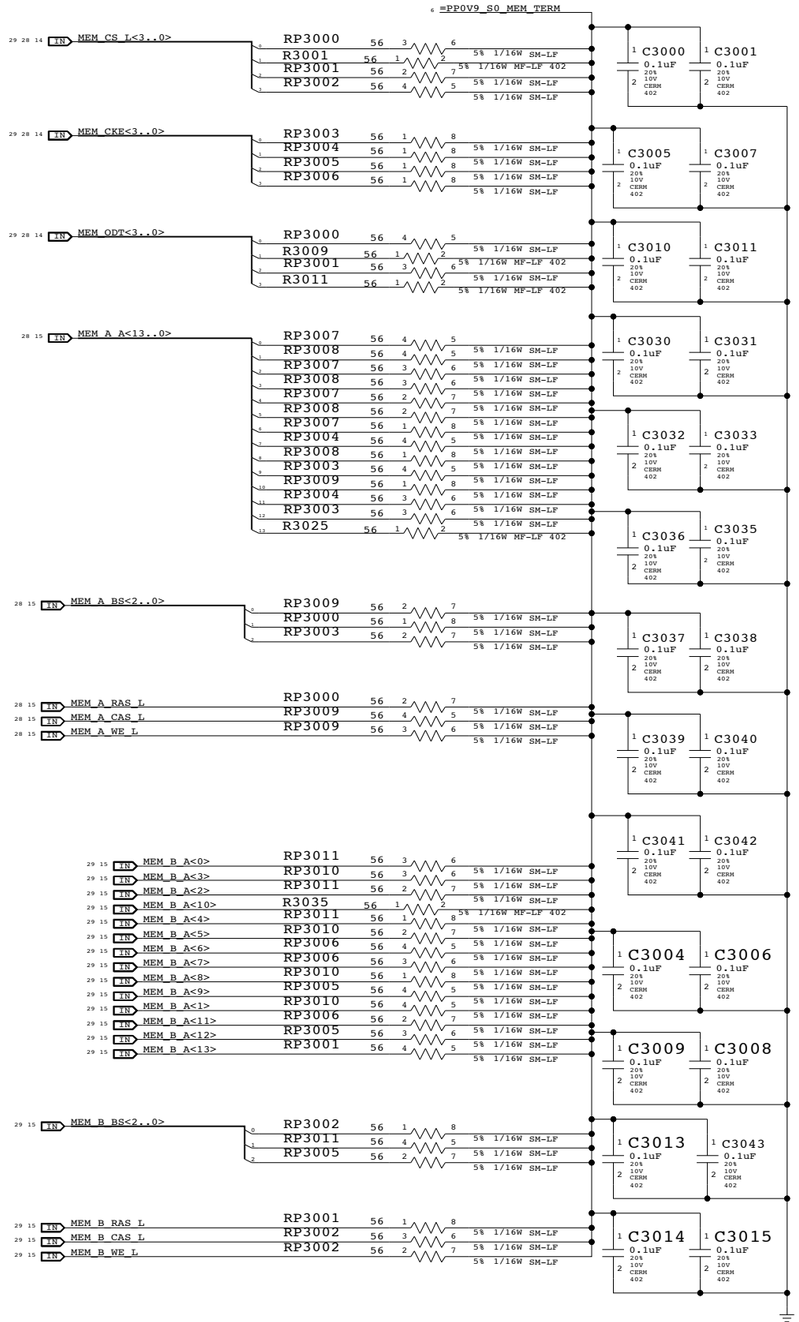
DDR2 SO-DIMM Connector B

SYNC_MASTER=MASTER SYNC_DATE=MASTER

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7032	??
SCALE: NONE	SHT 29 OF 97	

One cap for each side of every RPAK, one cap for every two discrete resistors
BOMOPTION shown at the top of each group applies to every part below it



Memory Active Termination

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7032	??

SCALE: NONE

SHT 30 OF 97

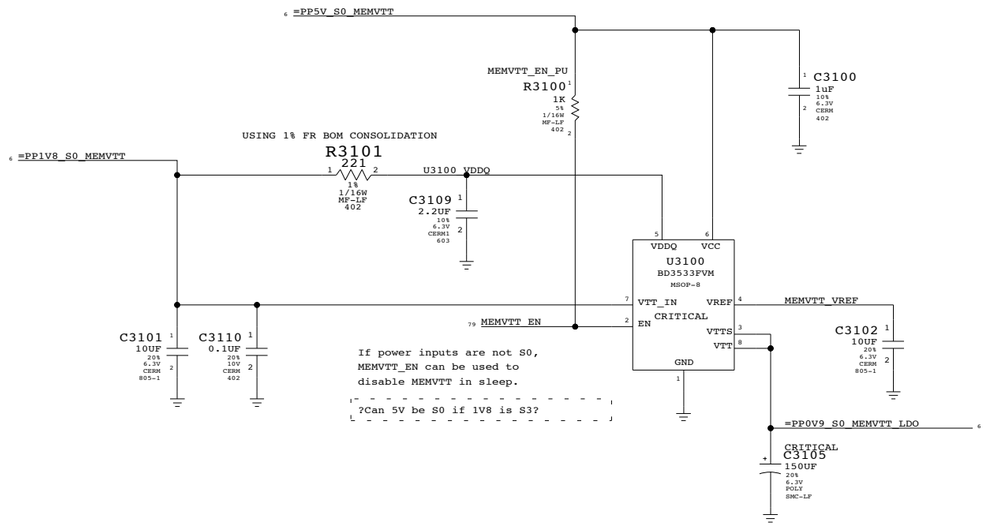
Page Notes

Power aliases required by this page:
- =PP5V_S0_MEMVTT
- =PP1V8_S0_MEMVTT
- =PP0V9_S0_MEMVTT_LDO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

DDR2 Vtt Regulator



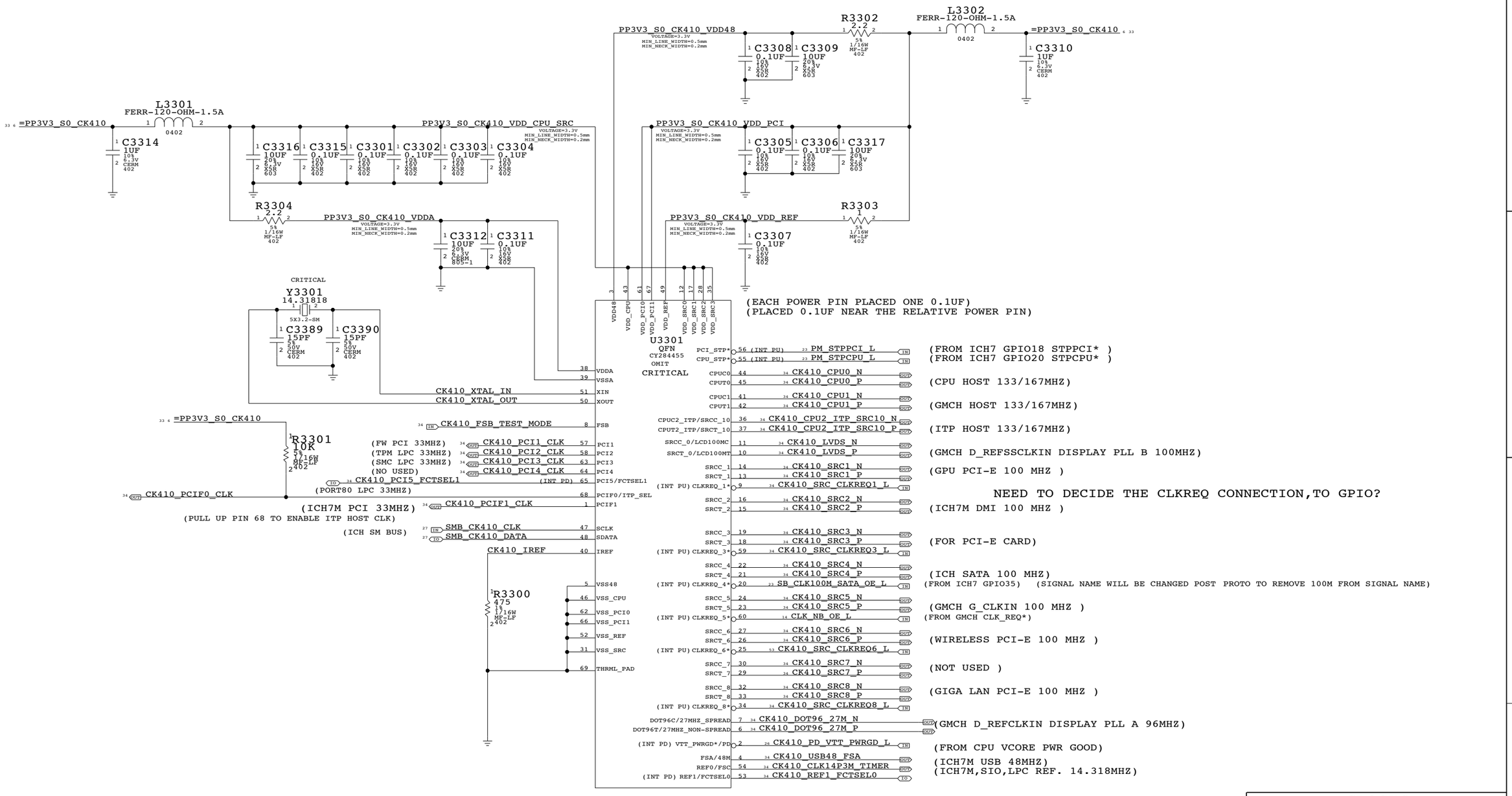
Memory Vtt Supply

SYNC_MASTER=MASTER SYNC_DATE=MASTER

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7032	??

SCALE: NONE SHT 31 OF 97



FCTSEL1	FCTSEL0	PIN 6	PIN 7	PIN 10	PIN 11	
0	0	DOT96T	DOT96C	100MT_SST	100MC_SST	* FOR INT. GRAPHIC SYSTEM
0	1	DOT96T	DOT96C	SRCT0	SRCC0	
1	0	27M NON SPREAD	27M SPREAD	SRCT0	SRCC0	* FOR EXT. GRAPHIC SYSTEM
1	1	OFF LOW	TBD	SRCT0	SRCC0	

CLOCKS

SYNC_MASTER=MASTER SYNC_DATE=MASTER

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7032	??
SCALE: NONE	SHT 33 OF 97	

NOTE: USE THESE PULL-DOWNS IF NOT CONNECTED TO GPIO'S

33 CK410_SRC_CLKREQ1_L (GPU CLK OE*) R3495 1K
33 CK410_SRC_CLKREQ3_L (SPARE CLK OE*) R3494 1K
33 CK410_SRC_CLKREQ8_L (YUKON CLK OE*) R3493 1K

FSB FREQUENCY SELECT:

	STUFF	NO STUFF
CPU DRIVEN	R3454 R3459 R3463	R3452 R3457 R3461
533MHZ (133MHZ CPU CLK)	R3452 R3457 R3461	R3454 R3459 R3463
667MHZ (166MHZ CPU CLK)	R3452 R3461	R3454 R3459 R3463 R3457

80 34 6 PP1V05_S0

R3453 1K 1/16W 5% MF-LF 402
14 NB_BSEL<0>
34 CK410_FSA
R3455 1K 1/16W 5% MF-LF 402
7 CPU_BSEL<0>
NOSTUFF R3452 56 5% 1/16W MF-LF 402
R3454 0 5% 1/16W MF-LF 402

80 34 6 PP1V05_S0

R3458 1K 1/16W 5% MF-LF 402
14 NB_BSEL<1>
33 CK410_FSB_TEST_MODE
7 CPU_BSEL<1>
R3456 1K 5% 1/16W MF-LF 402
NOSTUFF R3457 0 5% 1/16W MF-LF 402
R3459 0 5% 1/16W MF-LF 402

80 34 6 PP1V05_S0

R3462 1K 1/16W 5% MF-LF 402
14 NB_BSEL<2>
34 CK410_FSC
7 CPU_BSEL<2>
R3460 1K 5% 1/16W MF-LF 402
NOSTUFF R3461 0 5% 1/16W MF-LF 402
R3463 0 5% 1/16W MF-LF 402

33 IO CK410_PCI5_FCTSEL1 R3499 1K 1/16W 5% MF-LF 402 TP_CK410_PCI5_FCTSEL1

R3497 2.2K 5% 1/16W MF-LF 402 CK410_FSC 34
33 IN CK410_CLK14P3M_TIMER R3498 33 1/16W 5% MF-LF 402 SB_CLK14P3M_TIMER OUT 5 23
33 IN CK410_REF1_FCTSEL0 R3496 33 TP_CLK14P3M_SPARE OUT

R3451 2.2K 5% 1/16W MF-LF 402 CK410_FSA 34
33 IN CK410_USB48_FSA R3400 33 1/16W 5% MF-LF 402 SB_CLK48M_USBCTLR OUT 5 23
33 IN CK410_PCI4_CLK R3406 33 TP_PCI_CLK_SPARE OUT 5
33 IN CK410_PCI3_CLK R3405 33 PCI_CLK_SMC OUT 58
33 IN CK410_PCI2_CLK R3404 33 PCI_CLK_TPM OUT 67
33 IN CK410_PCI1_CLK R3403 33 PCI_CLK_FW OUT 44
33 IN CK410_PCIF1_CLK R3401 33 PCI_CLK_SB OUT 5 22
33 IN CK410_PCIF0_CLK R3402 33 PCI_CLK_PORT80 OUT 60

33 IN CK410_CPU1_P R3407 33 FSB_CLK_NB_P OUT 5 12 34
33 IN CK410_CPU1_N R3408 33 FSB_CLK_NB_N OUT 5 12 34
33 IN CK410_CPU0_P R3409 33 FSB_CLK_CPU_P OUT 5 7 34
33 IN CK410_CPU0_N R3410 33 FSB_CLK_CPU_N OUT 5 7 34
33 IN CK410_CPU2_ITP_SRC10_P R3411 33 34 FSB_CLK_XDP_P CPU_XDP_CLK_P 11
33 IN CK410_CPU2_ITP_SRC10_N R3412 33 MAKE_BASE=TRUE 34 FSB_CLK_XDP_N CPU_XDP_CLK_N 11
MAKE_BASE=TRUE
33 IN CK410_SRC6_P R3413 33 AIRPORT_CLK100M_PCIE_P OUT 34 53
33 IN CK410_SRC6_N R3414 33 AIRPORT_CLK100M_PCIE_N OUT 34 53
33 IN CK410_SRC5_P R3415 33 NB_CLK100M_GCLKIN_P OUT 5 14 34
33 IN CK410_SRC5_N R3416 33 NB_CLK100M_GCLKIN_N OUT 5 14 34
33 IN CK410_SRC4_P R3417 33 SB_CLK100M_SATA_P OUT 5 21 34
33 IN CK410_SRC4_N R3418 33 SB_CLK100M_SATA_N OUT 5 21 34
33 IN CK410_SRC2_P R3419 33 SB_CLK100M_DMI_P OUT 5 22 34
33 IN CK410_SRC2_N R3420 33 SB_CLK100M_DMI_N OUT 5 22 34
33 IN CK410_SRC8_P R3421 33 ENET_CLK100M_PCIE_P OUT 5 34 41
33 IN CK410_SRC8_N R3422 33 ENET_CLK100M_PCIE_N OUT 5 34 41
33 IN CK410_LVDS_P R3425 33 NB_CLK_DREFSSCLKIN_P OUT 5 14 34
33 IN CK410_LVDS_N R3426 33 NB_CLK_DREFSSCLKIN_N OUT 5 14 34
33 IN CK410_DOT96_27M_P R3471 33 NB_CLK_DREFCLKIN_P OUT 5 14 34
33 IN CK410_DOT96_27M_N R3470 33 NB_CLK_DREFCLKIN_N OUT 5 14 34

33 IN CK410_SRC3_P R3492 33 SPARE_SRC3_P R3488 49.9
33 IN CK410_SRC3_N R3491 33 SPARE_SRC3_N R3487 49.9
33 IN CK410_SRC7_P R3490 33 SPARE_SRC7_P R3486 49.9
33 IN CK410_SRC7_N R3489 33 SPARE_SRC7_N R3485 49.9
MAKE_BASE=TRUE
33 IN CK410_SRC1_P NO_TEST=TRUE NC_CK410_SRC1_P
33 IN CK410_SRC1_N NO_TEST=TRUE NC_CK410_SRC1_N MAKE_BASE=TRUE
NO GPU SO LEAVE THIS CLK NOT CONNECTED AND DISABLE THE OUTPUT IN THE CLOCK CHIP

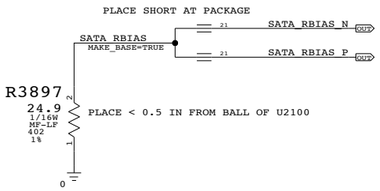
1% 402 1/16W MF-LF
34 12 5 FSB_CLK_NB_P R3429 49.9
34 12 5 FSB_CLK_NB_N R3430 49.9
34 7 5 FSB_CLK_CPU_P R3431 49.9
34 7 5 FSB_CLK_CPU_N R3432 49.9
34 FSB_CLK_XDP_P R3433 49.9
34 FSB_CLK_XDP_N R3434 49.9
53 34 AIRPORT_CLK100M_PCIE_P R3435 49.9
53 34 AIRPORT_CLK100M_PCIE_N R3436 49.9
34 14 5 NB_CLK100M_GCLKIN_P R3438 49.9
34 14 5 NB_CLK100M_GCLKIN_N R3437 49.9
34 21 5 SB_CLK100M_SATA_P R3439 49.9
34 21 5 SB_CLK100M_SATA_N R3440 49.9
34 22 5 SB_CLK100M_DMI_P R3442 49.9
34 22 5 SB_CLK100M_DMI_N R3441 49.9
41 34 5 ENET_CLK100M_PCIE_P R3443 49.9
41 34 5 ENET_CLK100M_PCIE_N R3444 49.9
34 14 5 NB_CLK_DREFSSCLKIN_P R3447 49.9
34 14 5 NB_CLK_DREFSSCLKIN_N R3448 49.9
34 14 5 NB_CLK_DREFCLKIN_P R3449 49.9
34 14 5 NB_CLK_DREFCLKIN_N R3450 49.9

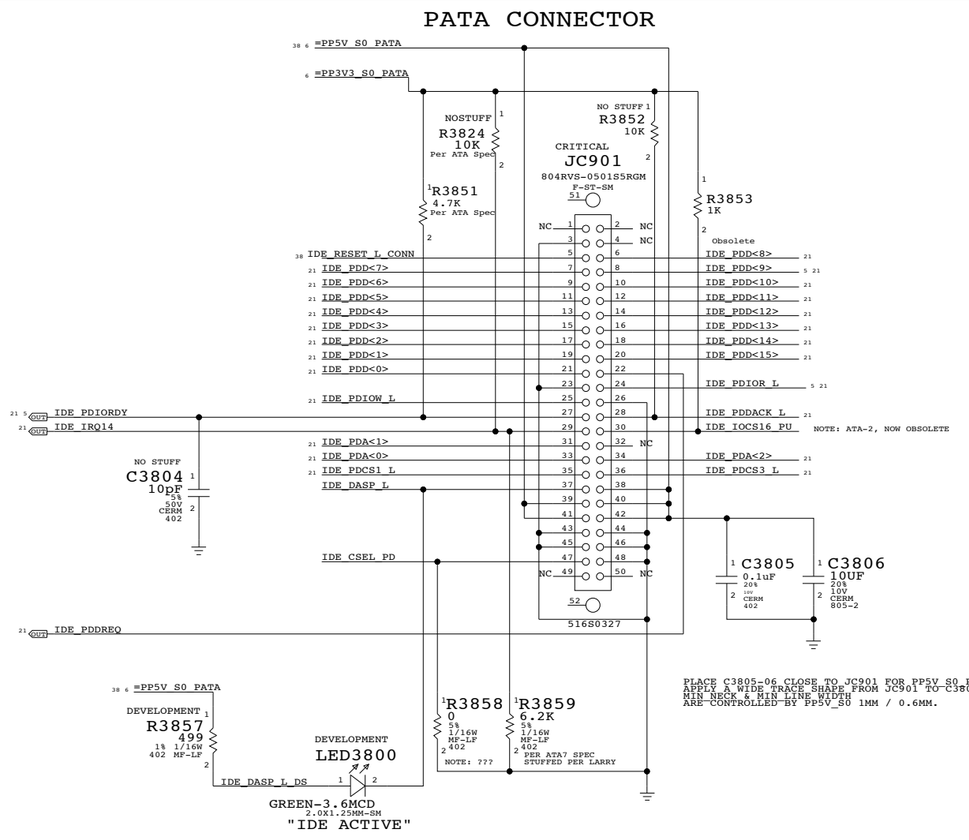
CLOCKS: TERMINATIONS

SYNC_MASTER=MASTER SYNC_DATE=MASTER

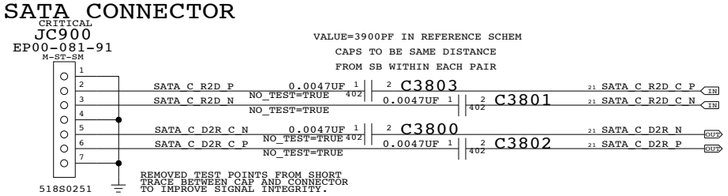
APPLE COMPUTER INC.

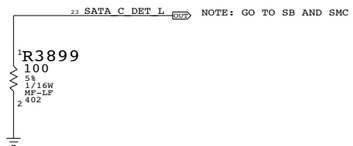
SIZE	DRAWING NUMBER	REV.
D	051-7032	??
SCALE: NONE	SHT 34 OF 97	

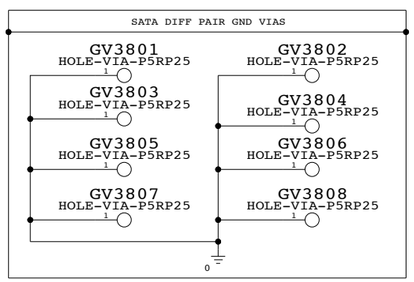




SATA CONNECTOR







SATA PORT 0 IS NOT USED

21 IN SATA_A_R2D_C_P — TP_SATA_A_R2D_P
21 IN SATA_A_R2D_C_N — TP_SATA_A_R2D_N
MAKE_BASE=TRUE

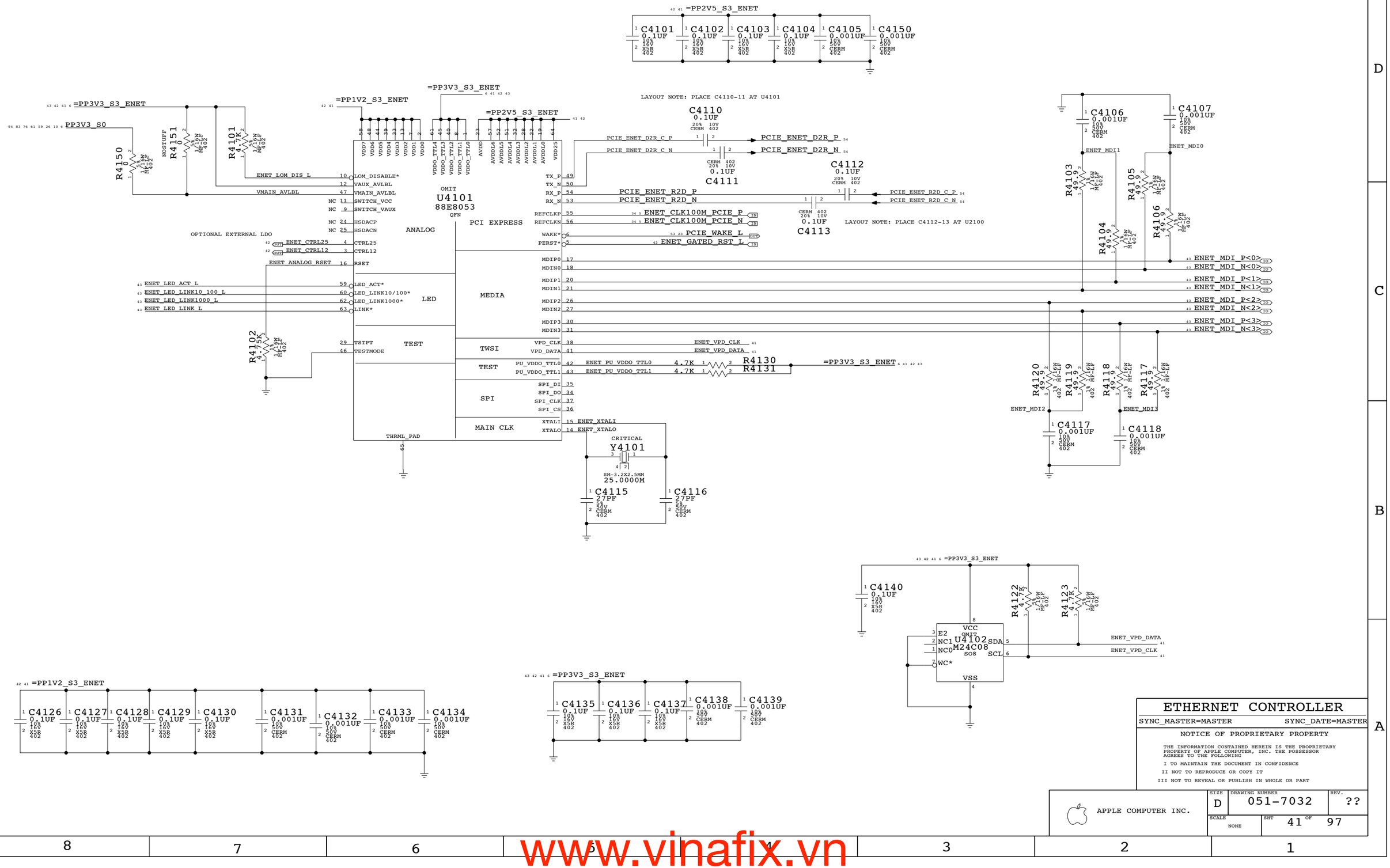
21 OUT SATA_A_D2R_P — TP_SATA_A_D2R_P
21 OUT SATA_A_D2R_N — TP_SATA_A_D2R_N
MAKE_BASE=TRUE

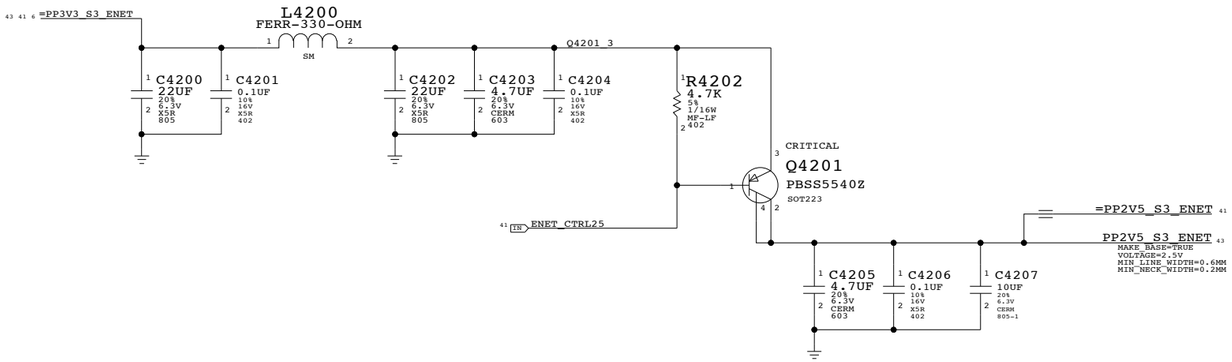
Disk Connectors

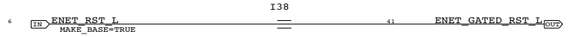
NOTICE OF PROPRIETARY PROPERTY

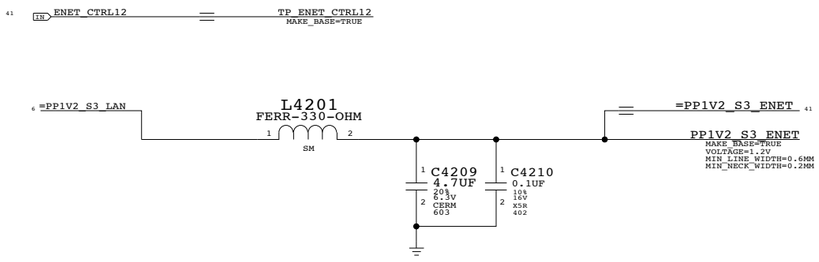
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7032	??
SCALE: NONE	SHT 38 OF 97	





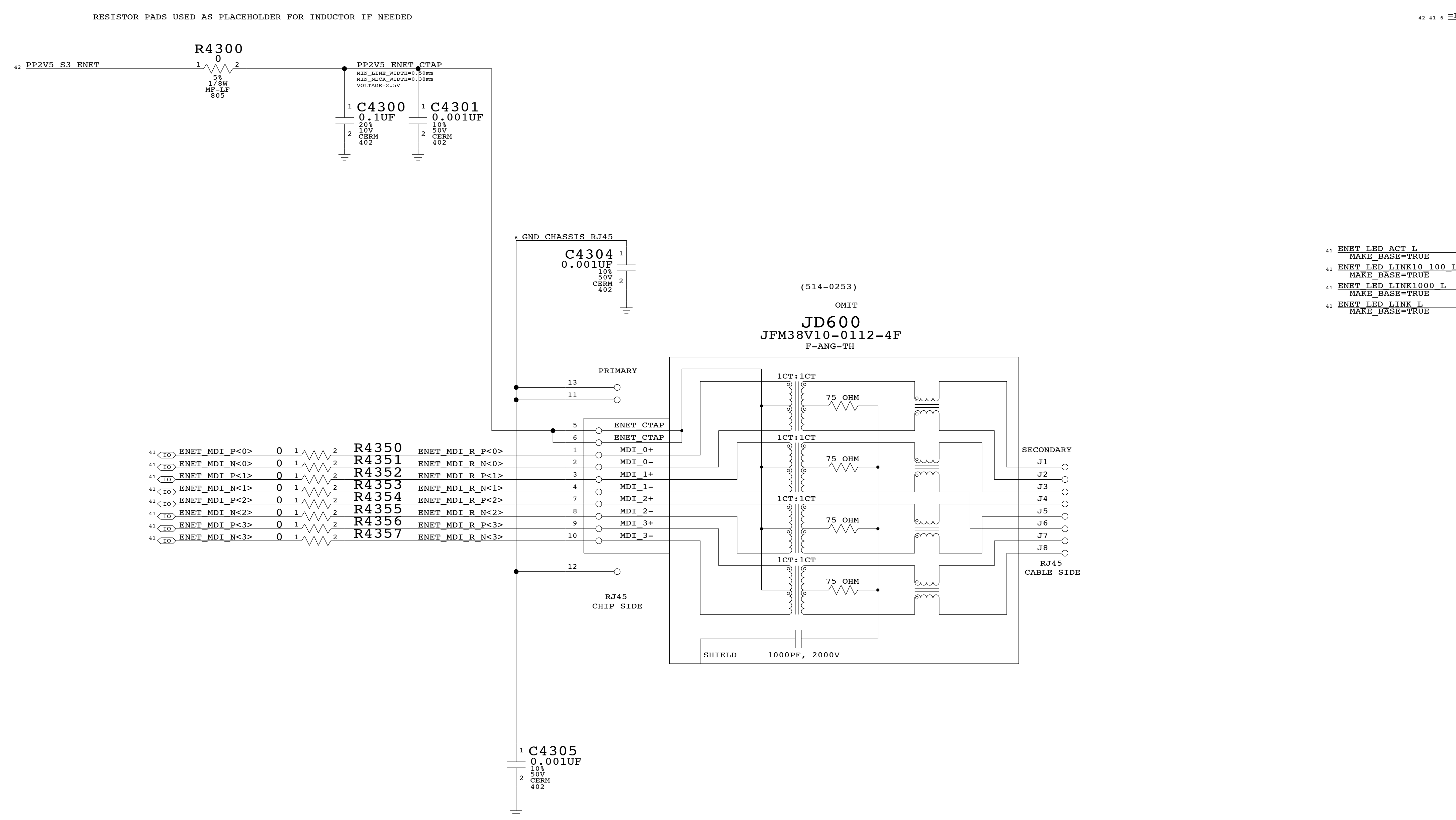




ETHERNET MISC

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7032	??
SCALE: NONE	SHT 42 OF 97	


RESISTOR PADS USED AS PLACEHOLDER FOR INDUCTOR IF NEEDED
PP2V5_S3_ENET
R4300
0
5%
1/8W
MF-LF
805
PP2V5_ENET_CTAP
VOLTAGE=2.5V
C4300
0.1UF
20%
10V
CERM
402
C4301
0.001UF
10%
50V
CERM
402
GND_CHASSIS_RJ45
C4304
0.001UF
10%
50V
CERM
402
(514-0253)
OMIT
JD600
JFM38V10-0112-4F
F-ANG-TH
PRIMARY
ENET_CTAP
MDI_0+
MDI_0-
MDI_1+
MDI_1-
MDI_2+
MDI_2-
MDI_3+
MDI_3-
1CT:1CT
75 OHM
SECONDARY
J1
J2
J3
J4
J5
J6
J7
J8
RJ45
CABLE SIDE
RJ45
CHIP SIDE
SHIELD
1000PF, 2000V
ENET_MDI_P<0>
ENET_MDI_N<0>
ENET_MDI_P<1>
ENET_MDI_N<1>
ENET_MDI_P<2>
ENET_MDI_N<2>
ENET_MDI_P<3>
ENET_MDI_N<3>
R4350
R4351
R4352
R4353
R4354
R4355
R4356
R4357
ENET_MDI_R_P<0>
ENET_MDI_R_N<0>
ENET_MDI_R_P<1>
ENET_MDI_R_N<1>
ENET_MDI_R_P<2>
ENET_MDI_R_N<2>
ENET_MDI_R_P<3>
ENET_MDI_R_N<3>
C4305
0.001UF
10%
50V
CERM
402
=PP3V3_S3_ENET
DEVELOPMENT
R4301
R4302
R4303
R4304
330
5%
1/10W
MF-LF
603
LED4300_1
LED4301_1
LED4302_1
LED4303_1
LED4300
LED4301
LED4302
LED4303
GREEN-3.6MCD
2.0X1.25MM-SM
ENET_LED_ACT_L
MAKE_BASE=TRUE
ENET_LED_LINK10_100_L
MAKE_BASE=TRUE
ENET_LED_LINK1000_L
MAKE_BASE=TRUE
ENET_LED_LINK_L
MAKE_BASE=TRUE

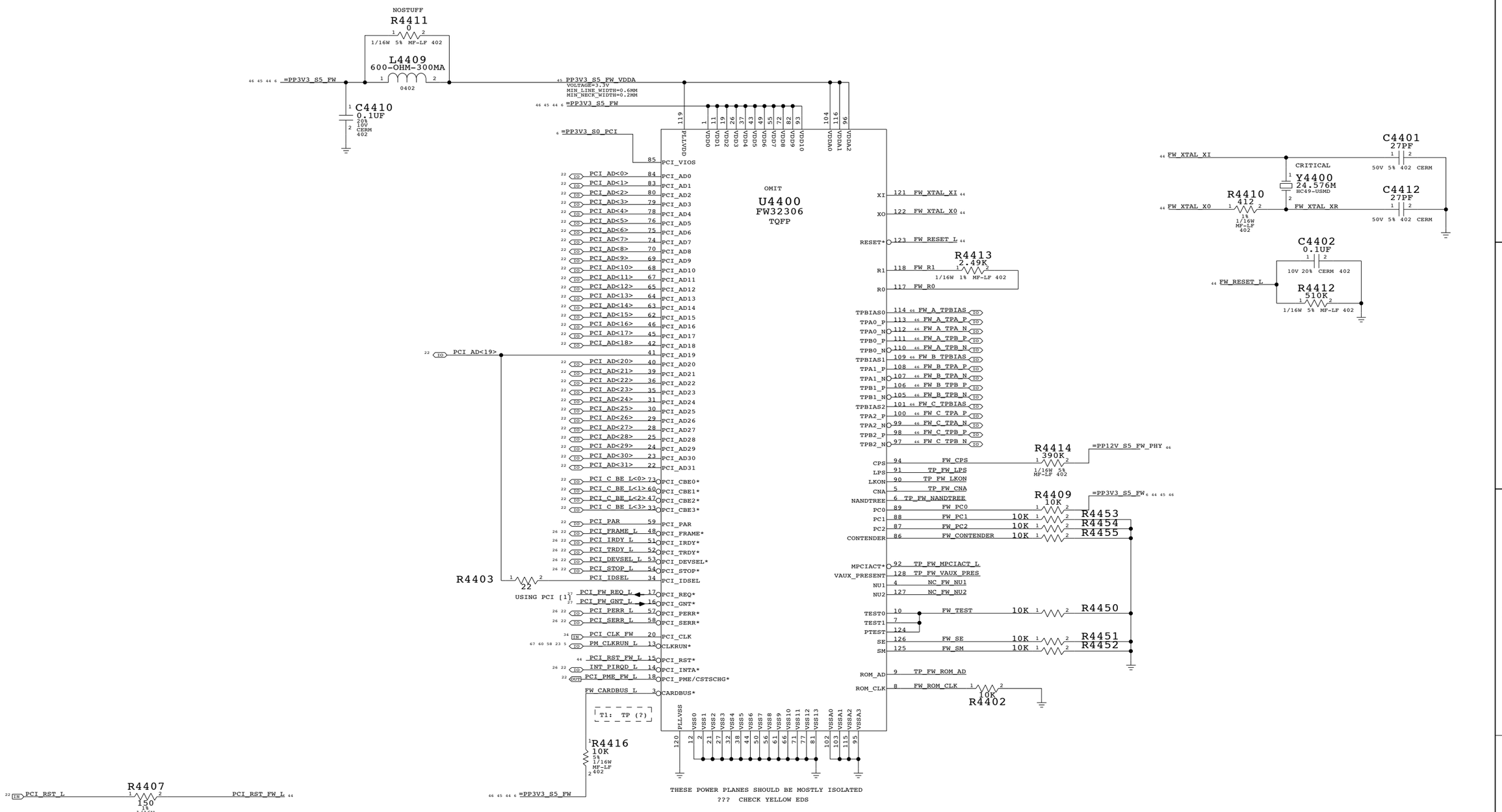
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0340	1	CON,RJ-45 7 DEGRESS, W/O RIBS	JD600	CRITICAL	17_INCH_LCD

ETHERNET CONNECTOR

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-7032 | REV. ??

SCALE NONE | SHT 43 OF 97

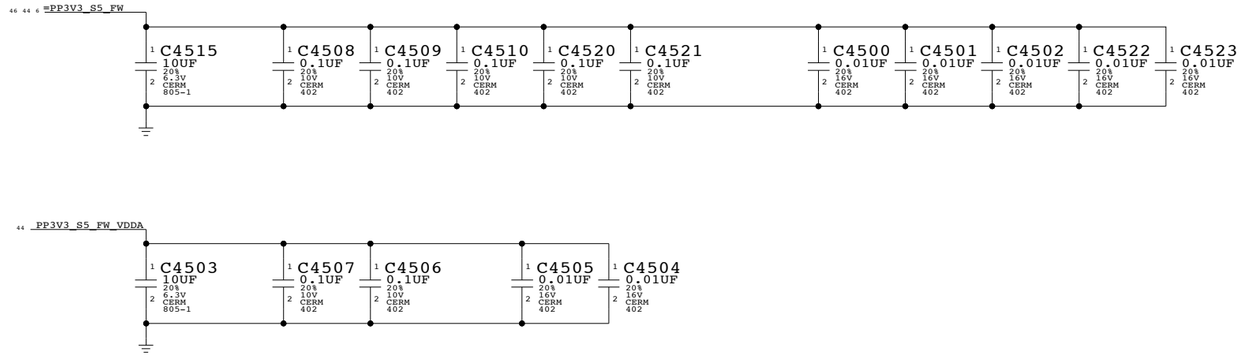


FW: FW323-06

SYNC_MASTER=MASTER SYNC_DATE=MASTER

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7032	??
SCALE: NONE	SHT 44 OF 97	



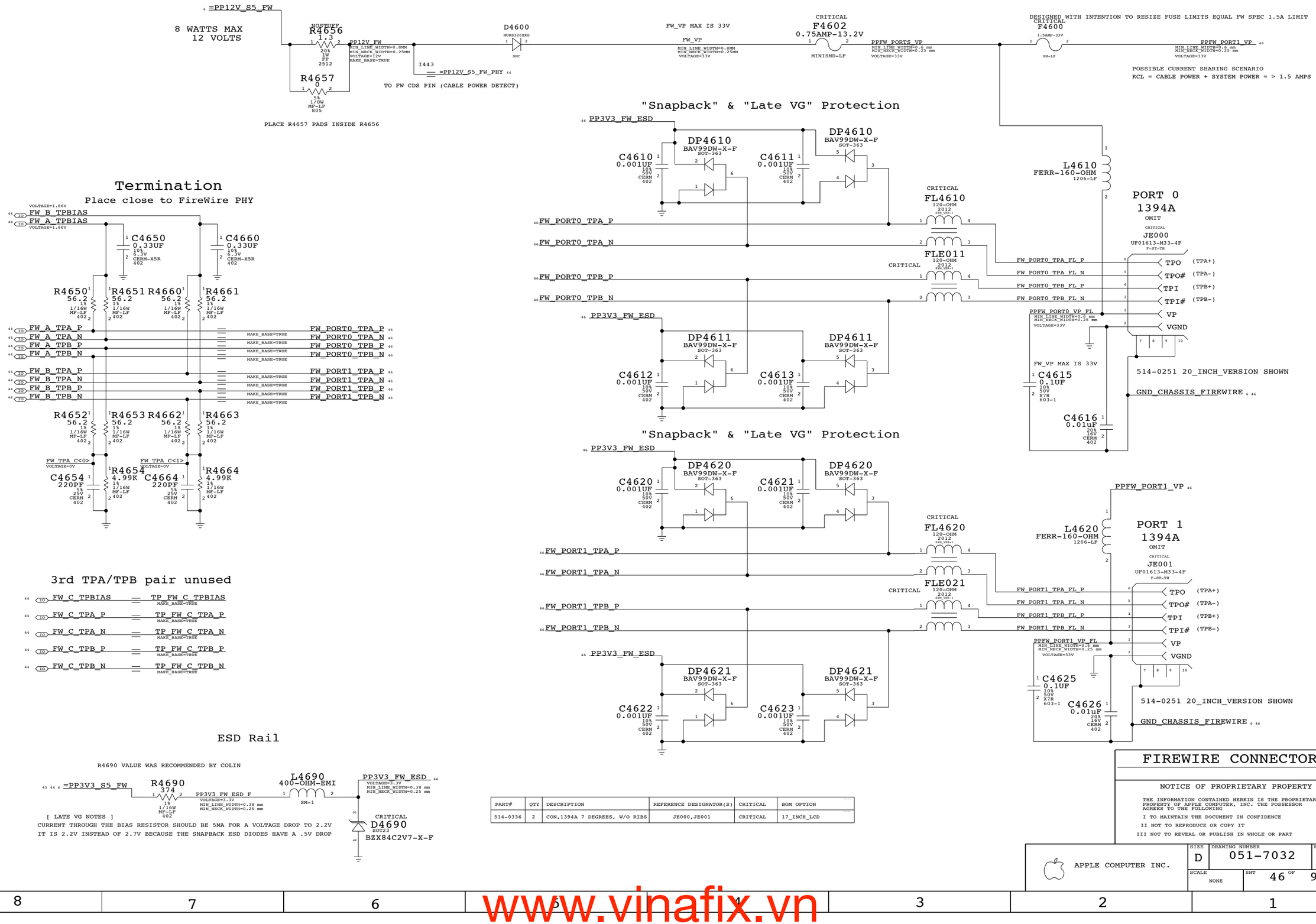
FW: DECAPS

SYNC_MASTER=MASTER SYNC_DATE=MASTER

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7032	??

SCALE	SHT
NONE	45 OF 97



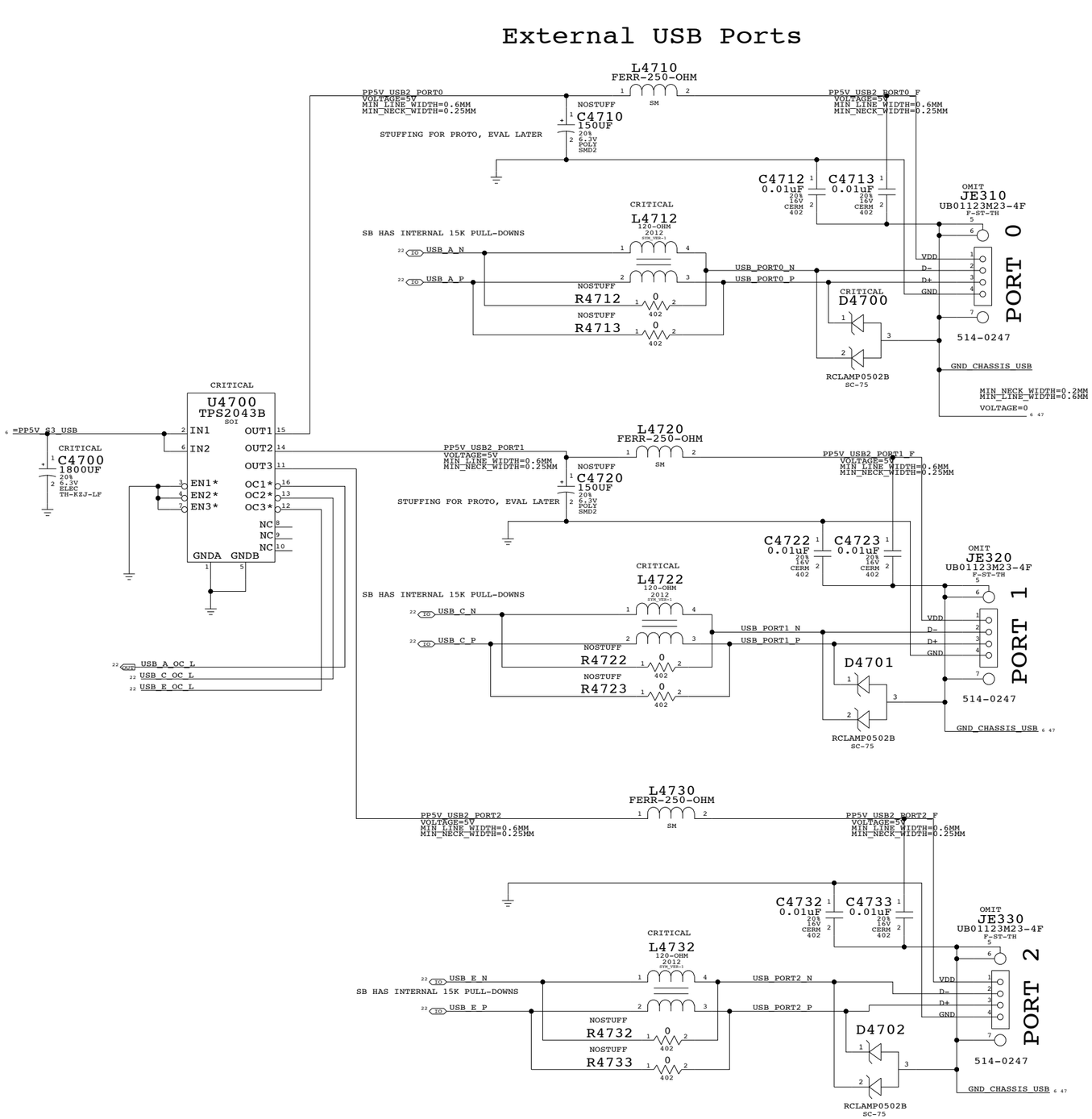
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0336	2	CON,1394A 7 DEGREES, W/O RIBS	JE000,JE001	CRITICAL	17_INCH_LCD

FIREWIRE CONNECTORS

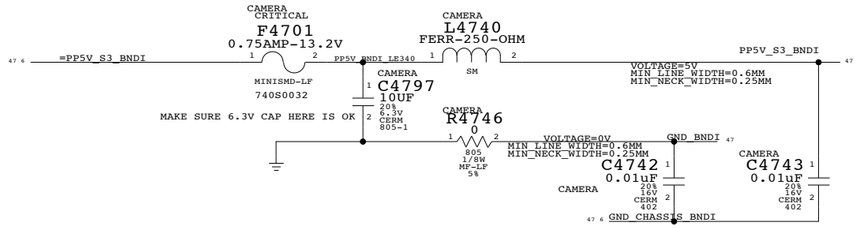
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7032	??
SCALE: NONE	SHT 46 OF 97	

External USB Ports

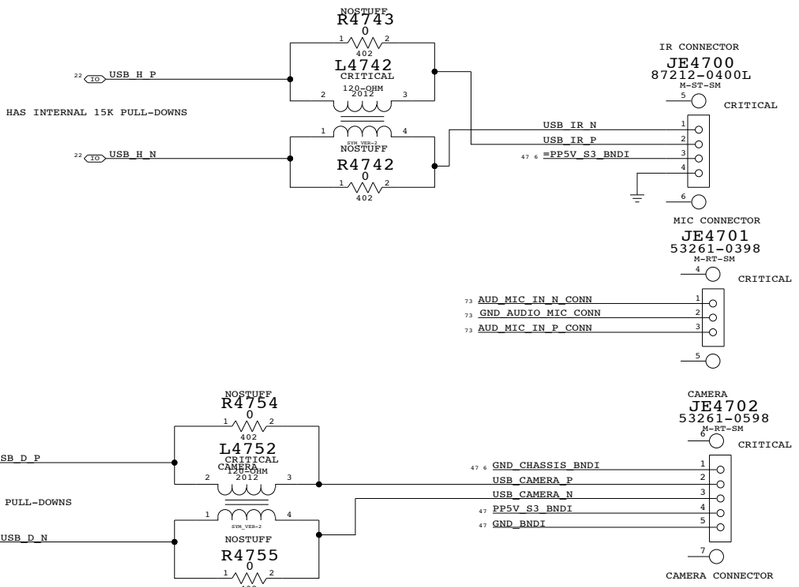


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0339	3	USB RECEPTACLE,4P,UB1123-M50-4F	JE310,JE320,JE330	CRITICAL	17_INCH_LCD

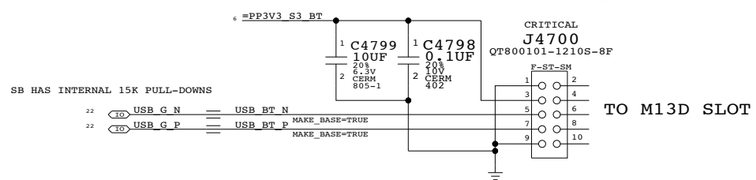


LAYOUT NOTE:
PLACE C4743, C4797 & L4740
NEAR JE4702 PIN 14 IN THE
ORDER LISTED, AND NOT ON
BOTH SIDES OF THE PIN.

PLACE C4742 CLOSED TO JE4702.



BLUETOOTH



NOTE: STANDOFFS FOR J4700

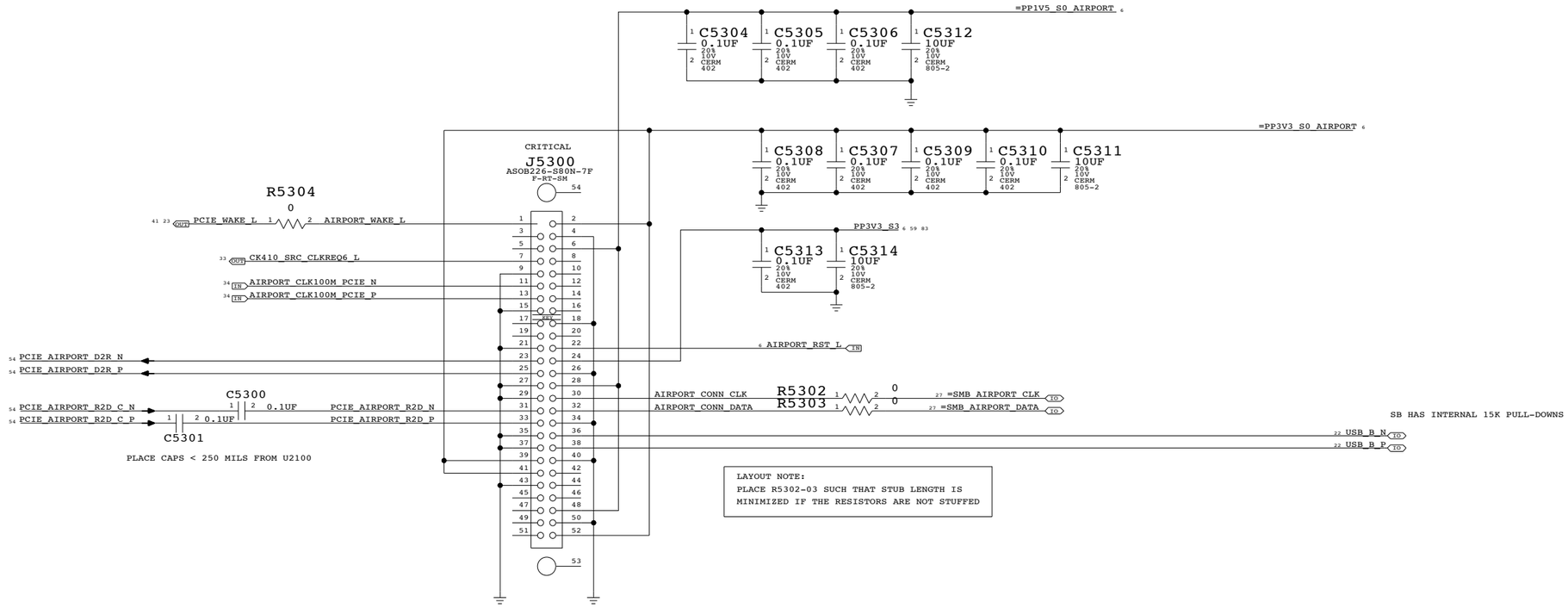
SDF4700
STDOFF-4OD4.5H-1.35-TH

SDF4701
STDOFF-4OD4.5H-1.35-TH

USB Device Interfaces

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7032	??
SCALE: NONE	SHT 47 OF 97	



AIRPORT CONN

SYNC_MASTER=MASTER SYNC_DATE=MASTER

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7032	??
SCALE: NONE	SHT 53 OF 97	

22 IN PCIE_C_R2D_C_N — TP_PCIE_C_R2D_C_N MAKE_BASE=TRUE
22 IN PCIE_C_R2D_C_P — TP_PCIE_C_R2D_C_P MAKE_BASE=TRUE

22 OUT PCIE_C_D2R_N — TP_PCIE_C_D2R_N MAKE_BASE=TRUE
22 OUT PCIE_C_D2R_P — TP_PCIE_C_D2R_P MAKE_BASE=TRUE

22 IN PCIE_D_R2D_C_N — TP_PCIE_D_R2D_C_N MAKE_BASE=TRUE
22 IN PCIE_D_R2D_C_P — TP_PCIE_D_R2D_C_P MAKE_BASE=TRUE

22 OUT PCIE_D_D2R_N — TP_PCIE_D_D2R_N MAKE_BASE=TRUE
22 OUT PCIE_D_D2R_P — TP_PCIE_D_D2R_P MAKE_BASE=TRUE

22 IN PCIE_E_R2D_C_N — TP_PCIE_E_R2D_C_N MAKE_BASE=TRUE
22 IN PCIE_E_R2D_C_P — TP_PCIE_E_R2D_C_P MAKE_BASE=TRUE

22 OUT PCIE_E_D2R_N — TP_PCIE_E_D2R_N MAKE_BASE=TRUE
22 OUT PCIE_E_D2R_P — TP_PCIE_E_D2R_P MAKE_BASE=TRUE

22 IN PCIE_F_R2D_C_N — TP_PCIE_F_R2D_C_N MAKE_BASE=TRUE
22 IN PCIE_F_R2D_C_P — TP_PCIE_F_R2D_C_P MAKE_BASE=TRUE

22 OUT PCIE_F_D2R_N — TP_PCIE_F_D2R_N MAKE_BASE=TRUE
22 OUT PCIE_F_D2R_P — TP_PCIE_F_D2R_P MAKE_BASE=TRUE

USED PCIE PORTS

22 IN PCIE_A_R2D_C_N — PCIE_AIRPORT_R2D_C_N 53
MAKE_BASE=TRUE
22 IN PCIE_A_R2D_C_P — PCIE_AIRPORT_R2D_C_P 53
MAKE_BASE=TRUE

22 5 OUT PCIE_A_D2R_N — PCIE_AIRPORT_D2R_N 53
MAKE_BASE=TRUE
22 5 OUT PCIE_A_D2R_P — PCIE_AIRPORT_D2R_P 53
MAKE_BASE=TRUE

22 IN PCIE_B_R2D_C_N — PCIE_ENET_R2D_C_N 41
MAKE_BASE=TRUE
22 IN PCIE_B_R2D_C_P — PCIE_ENET_R2D_C_P 41
MAKE_BASE=TRUE

22 5 OUT PCIE_B_D2R_N — PCIE_ENET_D2R_N 41
MAKE_BASE=TRUE
22 5 OUT PCIE_B_D2R_P — PCIE_ENET_D2R_P 41
MAKE_BASE=TRUE

PCIE PORT ALIASES

SYNC_MASTER=MASTER SYNC_DATE=MASTER

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7032	??
SCALE: NONE	SHT 54 OF 97	

UNUSED PINS HAVE THE FORMAT
SMC_XXX_WHERE_XXX_IS_THE_PORT_NUMBER.
THEY ARE SET BY SOFTWARE TO BE
DRIVEN OUTPUTS ALWAYS SO THEY
CAN BE LEFT NO-CONNECTED.

OMIT
U5800
SMC_H8S2116
BGA
(1 OF 4)

PM_LAN_ENABLE	B12	P10	P60/KIN0*	L13		SMC_PM_G2_EN	OUT
SMC_RSTGATE_L	C13	P11	P61/KIN1*	L14		SMC_ADAPTER_EN	OUT
ALL_SYS_PWRGD	A15	P12	P62/KIN2*	L15	22 5	SPI_ARB	IN
RSMRST_PWRGD	B14	P13	P63/KIN3*	K12	63 22	SPI_SCLK	IN
SMC_SB_NMI	B15	P14	P64/KIN4*	K13	63 22	SPI_SI	OUT
PM_RSMRST_L	C14	P15	P65/KIN5*	K14	63 22	SPI_SO	IN
IMVP_VR_ON	D12	P16	P66/IRQ6*/KIN6*	J12		SMC_PROCHOT_3_3_L	IN
PM_PWRBTN_L	C15	P17	P67/IRQ7*/KIN7*	J13		SMC_CPU_INIT_3_3_L	IN
SMC_P20	D13	P20	P70/AN0	N12		SMC_CPU_ISENSE	IN
SMC_P21	D14	P21	P71/AN1	R13		SMC_CPU_VSENSE	IN
SMC_P22	D15	P22	P72/AN2	P13		SMC_GPU_ISENSE	IN
SMC_P23	E12	P23	P73/AN3	R14		SMC_GPU_VSENSE	IN
SMC_BATT_TRICKLE_EN_L	E14	P24	P74/AN4	P14		SMC_DCIN_ISENSE	IN
SMC_BATT_CHG_EN	E15	P25	P75/AN5	R15		SMC_PBUS_VSENSE	IN
SMC_P26	E13	P26	P76/AN6	N13		SMC_BATT_ISENSE	IN
SMC_P27	F14	P27	P77/AN7	P15		SMC_FWIRE_ISENSE	IN
LPC_AD<0>	D9	P30/LAD0	P80/PME*	C7		SMC_WAKE_SCI_L	IN
LPC_AD<1>	C9	P31/LAD1	P81/GA20	A7		SMC_TPM_GPIO	OUT
LPC_AD<2>	A9	P32/LAD2	P82/CLKRUN*	B7	67 60 44 23 5	PM_CLKRUN_L	IO
LPC_AD<3>	B9	P33/LAD3	P83/LPCPD*	D6	67 60 23	PM_SUS_STAT_L	IN
LPC_FRAME_L	D8	P34/LFRAME*	P84/IRQ3*/TXD1	C6		SC_TX_L	OUT
SMC_LRESET_L	C8	P35/LRESET*	P85/IRQ4*/RXD1	A6		SC_RX_L	IN
PCI_CLK_SMC	A8	P36/LCLK	P86/IRQ5*/SCK1/SCL1	B6		SMB_BSB_CLK	IO
INT_SERIRQ	D7	P37/SERIRQ	P90/IRQ2*	K4		SMC_ONOFF_L	IN
SMC_XDP_TMS	A5	P40/TMIO	P91/IRQ1*	J2		SMC_BC_ACOK	IN
SMC_SYS_LED_16B	B5	P41/TMO0	P92/IRQ0*	J1		SMC_BS_ALRT_L	IN
SMB_BSB_DATA	D5	P42/SDA1	P93/IRQ12*	J3	80 79 77 23	PM_SLP_S3_L	IN
SMC_TPM_PP	C3	P43/TMI1/EXSCK1	P94/IRQ13*	J4	77 23	PM_SLP_S4_L	IN
SMC_XDP_TRST_L	B1	P44/TMO1	P95/IRQ14*	H2	23	PM_SLP_S5_L	IN
SMC_XDP_TCK	C2	P45	P96/EXCL	H1		SMC_SUS_CLK	IN
SMC_SYS_LED	D3	P46/PWX0/PWM0	P97/IRQ15*/SDA0	G2		SMB_0_S0_DATA	IO
SMC_SYS_KBDLED	C1	P47/PWX1/PWM1					
SMC_TX_L	G1	P50					
SMC_RX_L	G4	P51					
SMB_0_S0_CLK	F2	P52/SCL0					

OMIT
U5800
SMC_H8S2116
BGA
(2 OF 4)

SMC_RCIN_L	R3	PA0/KIN8*/PA2DC	PE0	M3		SMC_CASE_OPEN	IN
BOOT_LPC_SPI_L	P3	PA1/KIN9*/PA2DD	PE1*/ETCK	M2	60 59 5	SMC_TCK	IN
PM_SYSRST_L	R2	PA2/KIN10*/PS2AC	PE2*/ETDI	M1	60 59 5	SMC_TDI	IN
SMC_TPM_RESET_L	N3	PA3/KIN11*/PS2AD	PE3*/ETDO	L4	60 59 5	SMC_TDO	OUT
PM_EXTTS_L	R1	PA4/KIN12*/PS2BC	PE4*/ETMS	L2	60 59 5	SMC_TMS	IN
PM_THRM_L	N2	PA5/KIN13*/PS2BD	PF0/IRQ8*/PWM2	M7		SMC_PF0	59
SYS_ONEWIRE	M4	PA6/KIN14*/PS2CC	PF1/IRQ9*/PWM3	P6		SMC_PF1	59
PM_BATLOW_L	N1	PA7/KIN15*/PS2CD	PF2/IRQ10*/TMOY	R6	59	SMC_LID	IN
SMC_EXTSMI_L	B10	PB0/LSMI*	PF3/IRQ11*/TMOX	N6	59	SMC_CPU_RESET_3_3_L	IN
SMC_RUNTIME_SCI_L	A10	PB1/LSCI	PF4/PWM4	M6	59	SMC_BATT_ISET	OUT
SMC_ODD_DETECT	D10	PB2	PF5/PWM5	R5	59	SMC_BATT_VSET	OUT
ISENSE_CAL_EN	A11	PB3	PF6/PWM6	P5	59	SMC_SYS_ISET	OUT
SMC_EXCARD_CP	B11	PB4	PF7/PWM7	N5	59	SMC_SYS_VSET	OUT
SMC_EXCARD_PWR_EN	C11	PB5	PG0/EXIRQ8*/TMIX	P9	63 22	SPI_CE_L	IO
SMC_EXCARD_OC_L	A12	PB6	PG1/EXIRQ9*/TMIY	R9	59	SMC_XDP_TCK_3_3	IN
SMC_XDP_TDO_3_3	D11	PB7	PG2/EXIRQ10*/SDA2	N9	59	SMB_BSA_DATA	IO
SMC_FAN_0_CTL	G14	PC0/TIOCA0/WUE8*	PG3/EXIRQ11*/SCL2	P8	59	SMB_BSA_CLK	IO
SMC_FAN_1_CTL	G15	PC1/TIOCB0/WUE9*	PG4/EXIRQ12*/EXSDAA	R8	59	SMB_A_S3_DATA	IO
SMC_FAN_2_CTL	G13	PC2/TIOCC0/TCLKA/WUE10*	PG5/EXIRQ13*/EXSCLA	M8	59	SMB_A_S3_CLK	IO
SMC_FAN_3_CTL	G12	PC3/TIOCD0/TCLKB/WUE11*	PG6/EXIRQ14*/EXSDAB	P7	59	SMB_B_S0_DATA	IO
SMC_FAN_0_TACH	H14	PC4/TIOCA1/WUE12*	PG7/EXIRQ15*/EXSCLB	R7	59	SMB_B_S0_CLK	IO
SMC_FAN_1_TACH	H15	PC5/TIOCB1/TCLKC/WUE13*	PH0/EXIRQ6*	E1	59	SMC_PROCHOT	OUT
SMC_FAN_2_TACH	H13	PC6/TIOCA2/WUE14*	PH1/EXIRQ7*	F3	59	SMC_THRMTRIP	OUT
SMC_FAN_3_TACH	H12	PC7/TIOCB2/TCLKD/WUE15*	PH2/FWE	K2	59	SMC_FWE	IN
SMS_X_AXIS	M11	PD0/AN8	PH3/EXEXCL	C4	59	ALS_GAIN	OUT
SMS_Y_AXIS	P11	PD1/AN9	PH4	D4	26 23	SMS_INT_L	OUT
SMS_Z_AXIS	R11	PD2/AN10	PH5	B3	59	SMS_ONOFF_L	OUT
SMC_ANALOG_ID	N11	PD3/AN11					
SMC_NB_ISENSE	P10	PD4/AN12					
SMC_MEM_ISENSE	R10	PD5/AN13					
ALS_LEFT	N10	PD6/AN14					
ALS_RIGHT	M10	PD7/AN15					

OMIT
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SMC_H8S2116
BGA
(4 OF 4)

G3	NC0	NC12	F15
H3	NC1	NC13	A14
K3	NC2	NC14	C12
L3	NC3	NC15	C10
N4	NC4	NC16	C5
M5	NC5	NC17	A3
N7	NC6	NC18	B8
M12	NC7	NC19	E4
M13	NC8	NC20	H4
L12	NC9	NC21	M9
K15	NC10	NC22	N8
J14	NC11		

59 58 6 =PP3V3_S5_SMC

C5802 22UF 20% 6.3V X5R 805
C5803 0.1UF 20% 10V CERM 402
C5804 0.1UF 20% 10V CERM 402
C5805 0.1UF 20% 10V CERM 402
C5806 0.1UF 20% 10V CERM 402

LAYOUT NOTE:
PLACE C5807 NEAR PIN F1

SMC_VCL
C5807 0.47UF 20% 6.3V CERM-X5R 402
VCL IS INTERNAL RAIL

LAYOUT NOTE:
PLACE R5899 AND C5820 NEAR SMC PIN N14,N15

59 58 6 =PP3V3_S5_SMC
R5899 4.7 5% 1/16W MF-LF 402
PP3V3_AVCC_SMC
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.20 MM
C5820 0.1UF 20% 10V CERM 402
80 76 59 58 GND_SMC_AVSS

PP3V3_AVREF_SMC 59
59 58 6 =PP3V3_S5_SMC

OMIT
U5800
SMC_H8S2116
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AVCC	N14		
AVCC	N15		
VCC	P2		
VCC	P1		
VCC	J15		
VCC	A1		
VCL	F1		
AVREF	M14		
AVREF	M15		
60 59 IN SMC_RST_L	E3	RES*	
59 SMC_XTAL	A2	XTAL	
59 SMC_EXTAL	B2	EXTAL	
MD1	E2		SMC_MD1 60
MD2	K1		KBC_MDE
NMI	F4		SMC_NMI 60 IN
ETRST*	L1		SMC_TRST_L IN
AVSS	P12		
AVSS	R12		
VSS	D1		
VSS	F4		
VSS	R4		
VSS	F12		
VSS	F13		
VSS	B13		
VSS	A13		
VSS	A4		
VSS	B4		
VSS	D2		

R5809 10K 5% 1/16W MF-LF 402
R5801 10K 5% 1/16W MF-LF 402
NOSTUFF
R5898 10K 5% 1/16W MF-LF 402
R5803 0 5% 1/16W MF-LF 402
R5802 10K 5% 1/16W MF-LF 402

XW5800 SM
GND_SMC_AVSS 58 59 76 80

SMC

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SIZE	DRAWING NUMBER	REV.
D	051-7032	??
SCALE: NONE	SHT 58 OF 97	

SMC RESET BUTTON

=PP3V3_S5_SMC

C5901 0.1uF 20% 10V CERM 402

C5900 0.01UF 10% 16V CERM 402

DEVELOPMENT SW5900 SPST SM-LF

U5900 RN5VD30A-F SOT23-5 (CRITICAL) VDD CD NC GND OUT

R5900 1K 5% 1/16W MF-LF 402

SMC_MANUAL_RST_L

SMC_RST_L (MAKE_BASE=TRUE)

WHITE SYSLED

LED2901 WHITE-500MCD 3X2MM-SM

PP5V_S3

SYS_LED_DRV_K

MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM

17_INCH_LCD

R5901 56.2 1% 1/16W MF-LF 402

SYS_LED_DRV_C

MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM

Q5900 FDV301N SOT23-LF

SMC_SYS_LED_16B

NOSTUFF R5902 4.7K 5% 1/16W MF-LF 402

AMBIENT LIGHT SENSOR CONNECTOR

(REF DES PRESERVED FOR PLACEMENT PURPOSE)

I2C ADDR:72(1001000)

J2901 53398-0476 F-ST-SM (CRITICAL) 518S0328

PP3V3_S3

I2C_ALS_SDA

I2C_ALS_SCL

SMC 3.3V -> CPU 1.05V SHIFTER

CPU_PROCHOT_L

Q5901 2N7002DW-X-F SOT-363

SMC_PROCHOT

PM_THRMTRIP_L

Q5901 2N7002DW-X-F SOT-363

SMC_THRMTRIP

POWER BUTTON HEADER

(REF DES PRESERVED FOR PLACEMENT PURPOSE)

J2903 53398-0276 M-ST-SM 518S0327

POWER_BUTTON_L

R5907

SYS POWER BUTTON

DEVELOPMENT SW5901 SPST SM-LF

NOSTUFF R5908 1K 5% 1/16W MF-LF 402

PLACE R5908 CLOSE TO SW5901 ONLY USING PADS FOR SWITCH

R5909 1K 5% 1/16W MF-LF 402

SMC_ONOFF_L

GENERATE 0.48V MID-VREF

C5902 0.1uF 20% 10V CERM 402

=PP3V3_S0_FAN

R5930 6.2K 1% 1/16W MF-LF 402

P0V48_SMC_LSREF

R5931 1K 5% 1/16W MF-LF 402

SMC CRYSTAL

LAYOUT NOTE: PLACE CAPACITORS BETWEEN CRYSTAL AND SMC/TPM

C5800 22PF CERM 5% 50V 402

C5801 22PF CERM 5% 50V 402

OMIT Y5800 20.000M SM-3

SMC_XTAL

SMC_EXTAL

TPM CRYSTAL

C6704 15PF 5% 50V CERM 402

C6705 15PF 5% 50V CERM 402

CRITICAL Y6700 32.768K SM-LF

TPM_XTALI

TPM_XTALO

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0165	1	XTAL,20.00,80PPM,HC49,SMD,LF	Y5800	CRITICAL	

CPU 1.05V -> SMC 3.3V SHIFTER

PP3V3_S5

=PP3V3_S0_FAN

C5903 0.1uF 20% 10V CERM 402

U5999 LM393A SOI-1-LF

P0V48_SMC_LSREF

CPU_PROCHOT_L

R5932 1K 5% 1/16W MF-LF 402

R5933 1K 5% 1/16W MF-LF 402

R5934 1K 5% 1/16W MF-LF 402

R5935 1K 5% 1/16W MF-LF 402

SMC_PROCHOT_3_3_L

SMC_CPU_RESET_3_3_L

SMC_XDP_TCK_3_3

SMC_XDP_TDO_3_3

U5999 LM393A SOI-1-LF

SPARE COMPARATOR

PCB: ENSURE FSB_CPURST_L FANS OUT FROM U1200 AND MINIMIZE ROUTE LENGTH TO U5999.

SMC ALIASES, PULLUPS, AND TESTPOINTS

NO-CONNECT UNUSED PINS

SMC_P20	NC_SMC_P20
SMC_P21	NC_SMC_P21
SMC_P22	NC_SMC_P22
SMC_P23	NC_SMC_P23
SMC_P26	NC_SMC_P26
SMC_P27	NC_SMC_P27
SMC_BATT_ISET	NC_SMC_BATT_ISET
SMC_BATT_VSET	NC_SMC_BATT_VSET
SMC_SYS_ISET	NC_SMC_SYS_ISET
SMC_SYS_VSET	NC_SMC_SYS_VSET
SMC_BATT_TRICKLE_EN_L	NC_SMC_BATT_TRICKLE_EN_L
SMC_BATT_CHG_EN	NC_SMC_BATT_CHG_EN
SMC_ANALOG_ID	NC_SMC_ANALOG_ID
ALS_GAIN	NC_ALS_GAIN

DEBUG TESTPOINTS ON SELECTED INPUTS/OUTPUTS

SMC_SYS_KBDLED	TP_SMC_SYS_KBDLED
SMC_PF0	TP_SMC_PF0
SMC_PM_G2_EN	TP_PM_G2_EN
SMC_ADAPTER_EN	TP_SMC_ADAPTER_EN
ALS_LEFT	TP_ALS_LEFT
ALS_RIGHT	TP_ALS_RIGHT
SMC_PF1	TP_SMC_PF1
SMC_XDP_TCK	TP_SMC_XDP_TCK
SMC_XDP_TMS	TP_SMC_XDP_TMS
SMC_XDP_TRST_L	TP_SMC_XDP_TRST_L
SMC_PB7	TP_SMC_PB7
SMC_SYS_LED	TP_SMC_SYS_LED
SMC_RSTGATE_L	TP_SMC_RSTGATE_L
SMC_EXCARD_PWR_EN	TP_SMC_EXCARD_PWR_EN
SMC_PB7	TP_SMC_PB7
SMC_FAN_3_TACH	TP_SMC_FAN_3_TACH
SMC_FAN_3_CTL	TP_SMC_FAN_3_CTL

TPM RESET PULLUP

PP3V3_TPM_3VSB

SMC_TPM_RESET_L — R5827 10K

WIRE-OR DIMM OVERTEMP TO SMC

DIMM_OVERTEMP_L — PM_EXTTS_L

CPU HIGH SIDE IN CURRENT

SMC_GPU_ISENSE — CPU_HISIDE_ISENSE

WIRE SMC TO SB PINS

SMC_CPU_INIT_3_3_L	FWH_INIT_L
SMC_SUS_CLK	SUS_CLK_SB

NC OR PULLDOWN UNUSED ANALOG SENSE PINS

SMS_X_AXIS	NC_SMS_X_AXIS
SMS_Y_AXIS	NC_SMS_Y_AXIS
SMS_Z_AXIS	NC_SMS_Z_AXIS
SMC_MEM_ISENSE	NC_SMC_MEM_ISENSE
SMC_BATT_ISENSE	UNUSED_SMC_SENSE
SMC_FWIRE_ISENSE	UNUSED_SMC_SENSE

UNUSED_SMC_SENSE — 10K R5924

PULLDOWN UNUSED ANALOG SENSE PINS ON PORT 7.

SMC PULL-UPS

=PP3V3_S5_SMC

SMC_ONOFF_L	R5808 10K
SMC_ODD_DETECT	R5829 10K
SMC_EXCARD_CP	R5830 10K
SC_RX_L	R5832 10K (NOT_DEVELOPMENT_SMC)
SC_TX_L	R5833 10K (NOT_DEVELOPMENT_SMC)
SMS_ONOFF_L	R5815 10K
SMC_TX_L	R5817 10K
SMC_RX_L	R5818 100K
SYS_ONEWIRE	R5819 10K
SMC_BS_ALRT_L	R5821 10K
SMC_TMS	R5822 10K
SMC_TDO	R5823 10K
SMC_TDI	R5824 10K
SMC_TCK	R5825 10K
SMC_BC_ACOK	R5826 10K
SMC_FWE	R5828 10K

SENSE GPU VCORE

SMC_GPU_VSENSE — CPU_HISIDE_VSENSE

SELECT TPM GPIO

SMC_TPM_GPIO

SMC_TPM_GPIO1 — R5920 — TPM_GPIO1

SMC_TPM_GPIO2 — R5921 — TPM_GPIO2

SMC_TPM_PP — R5995 0 — TPM_PP

PRECISION 3.3V AVREF FOR SMC

PP5V_S5

Q5910 NTR4101P SOT-23

SMC_REF_GATE2

SMC_REF_GATE1

R5941 10K

Q5911 2N7002 SOT23-LF

C5943 1UF 10% 6.3V CERM 402

SMC_REF_IN

PIN COMPATIBLE WITH TI REF3133 353S1278

NOSTUFF R5940 0

U5940 ISL60002-33 SOT23-3 (CRITICAL)

C5940 0.47uF 20% 6.3V CERM-X5R 402

C5942 10UF 20% 6.3V CERM 805-1

C5941 0.01uF 20% 16V CERM 402

PP3V3_AVREF_SMC

GND_SMC_AVSS

TURN ON 3.3V VREF ONLY AFTER SMC 3.3V RAIL AND AVCC RAIL IS UP.

SMC I2C BUS PULLUPS (INCLUDING UNUSED ONES)

PP3V3_S0

2.2K R5903	SMB_B_S0_CLK
2.2K R5904	SMB_B_S0_DATA

PP3V3_S3

2.2K R5905	SMB_A_S3_CLK
2.2K R5906	SMB_A_S3_DATA

=PP3V3_S5_SMC

10K R5910	SMB_BSB_CLK
10K R5911	SMB_BSB_DATA
10K R5912	SMB_0_S0_CLK (TP_SMB_0_S0_CLK)
10K R5913	SMB_0_S0_DATA (TP_SMB_0_S0_DATA)
10K R5914	SMB_BSA_CLK
10K R5915	SMB_BSA_DATA

PULLUPS FOR SYSTEM STATE PINS

10K R5916 SMC_LID

PULLDOWNS FOR SYSTEM STATE PINS

10K R5917 SMC_CASE_OPEN

ALIAS SENSORS INTO SMC I2C BUSSES

SMB_B_S0_CLK	=I2C_HD_TEMP_SCL
SMB_B_S0_DATA	=I2C_HD_TEMP_SDA
	=I2C_ODD_TEMP_SCL
	=I2C_ODD_TEMP_SDA
	=SMB_THRM_CLK
	=SMB_THRM_DATA
	SMB_GPU_NB_THRM_CLK
	SMB_GPU_NB_THRM_DATA
SMB_A_S3_CLK	I2C_ALS_SCL
SMB_A_S3_DATA	I2C_ALS_SDA

NOSTUFF C5904 100PF 5% 50V CERM 402

TIE ANALOG SENSOR OPAMP GROUNDS TO SMC GROUND

PCB: RUN A TRACE FROM EACH ANALOG OPAMP PSEUDO-DIFFERENTIALLY NEXT TO THIS GND TRACE AND TIE INTO DIGITAL GND VERY CLOSE TO SMC'S XW5800. PLACE XW5900 NEAR XW5800.

XW5900 SM — GND_NEXT_TO_SMC

SMC & TPM SUPPORT

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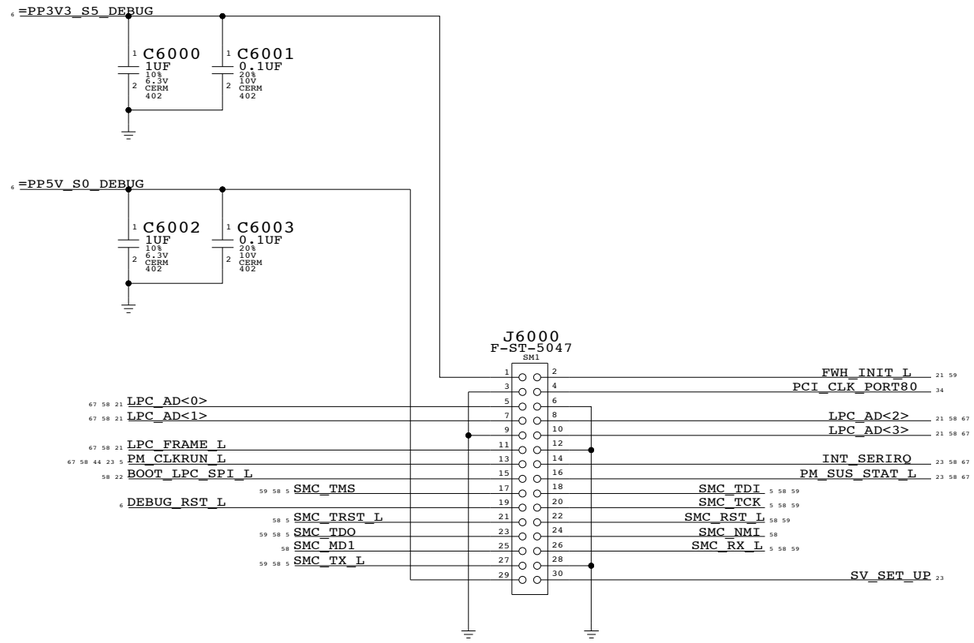
SIZE	DRAWING NUMBER	REV.
D	051-7032	??
SCALE: NONE	SHT 59 OF 97	



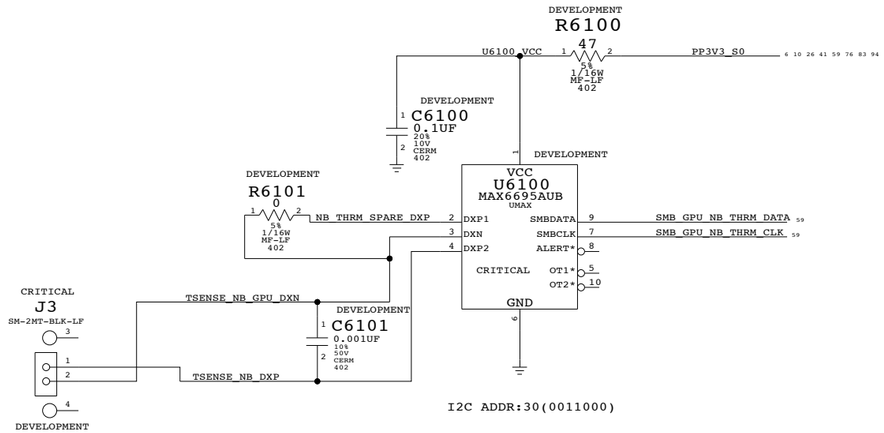
LPC+ CONN

SYNC_MASTER=M38 SYNC_DATE=12/09/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7032	??

SCALE	SHT
NONE	60 OF 97



NB THERMAL

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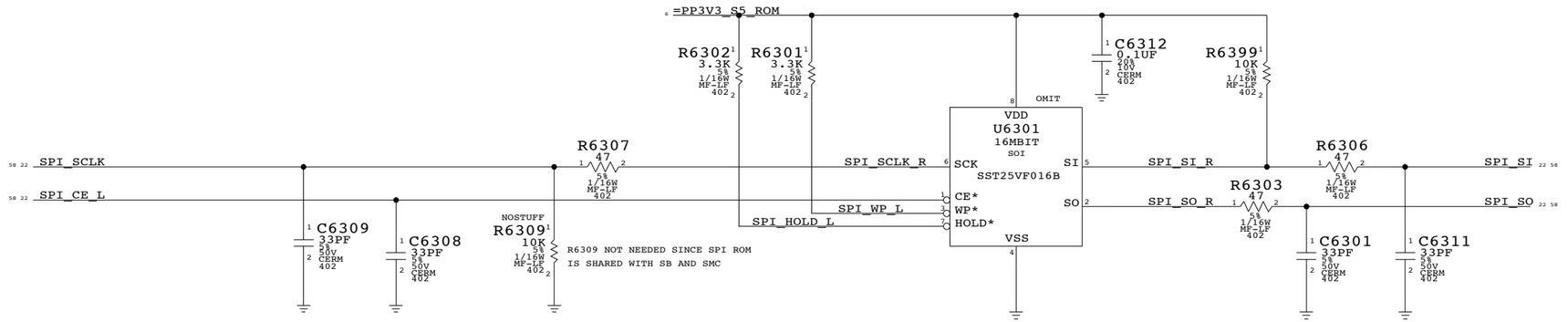
SIZE	DRAWING NUMBER	REV.
D	051-7032	??

SCALE: NONE

SHT 61 OF 97



R6306-07 SHOULD BE PLACED LESS THAN 2.54MM FROM U2100

R6303 SHOULD BE PLACED LESS THAN 2.54MM FROM U6301

SPI BOOTROM

SYNC_MASTER=M38 SYNC_DATE=01/05/2006

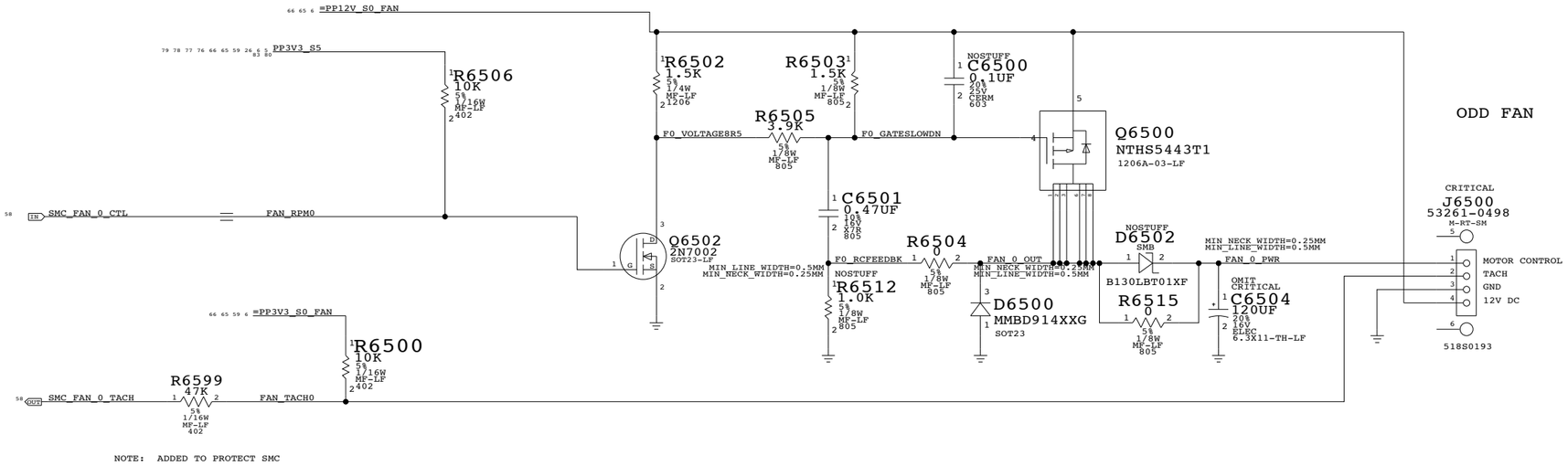
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7032	??

SCALE: NONE

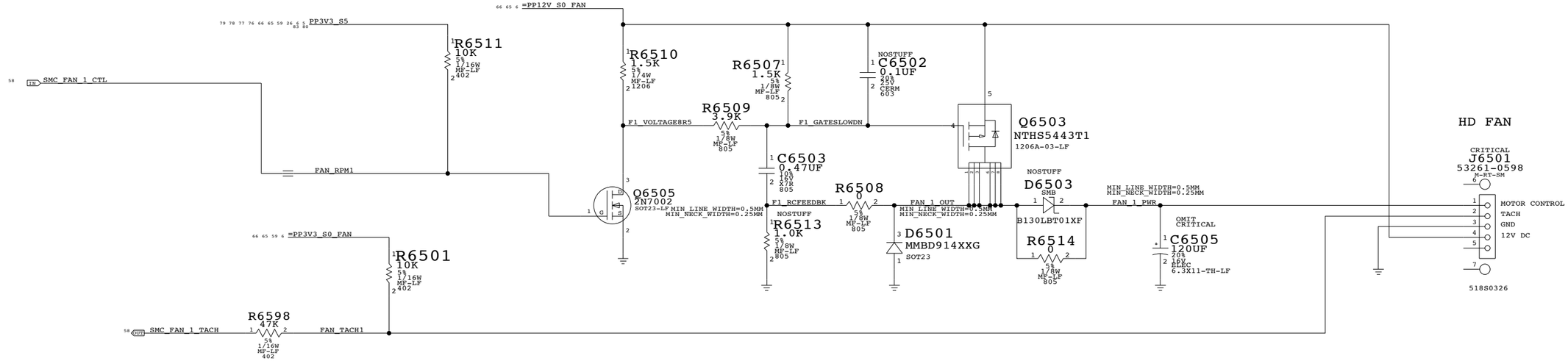
SHT 63 OF 97

FAN 0



NOTE: ADDED TO PROTECT SMC

FAN 1



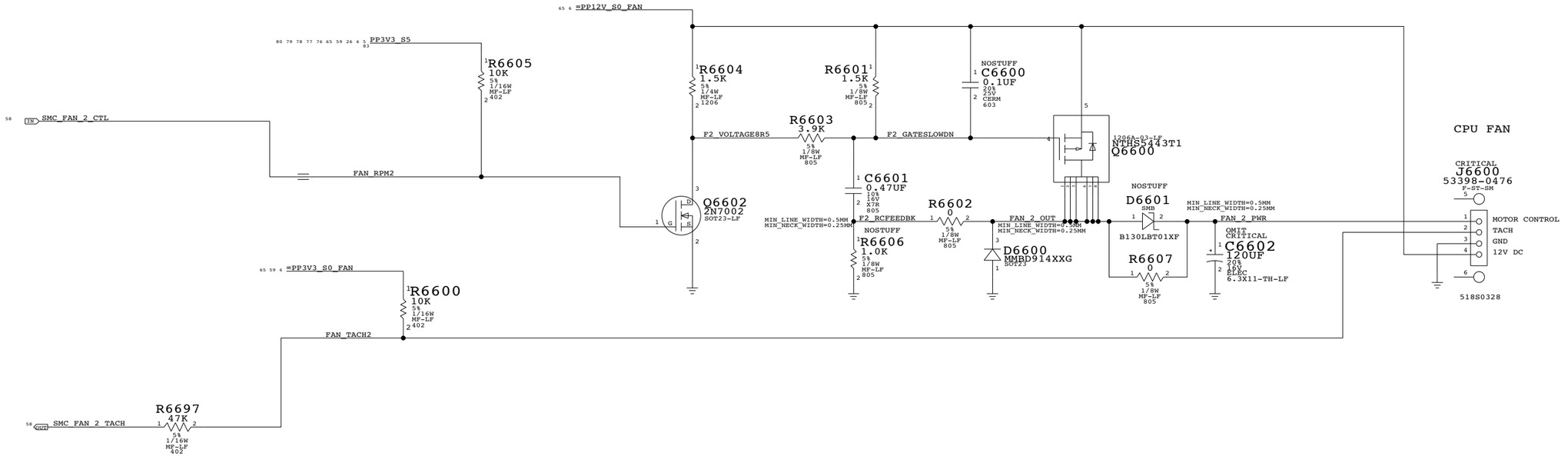
Fan 0, 1 & System Temp

APPLE COMPUTER INC.

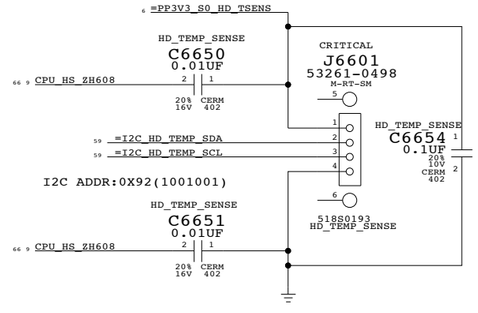
SIZE	DRAWING NUMBER	REV.
D	051-7032	??

SCALE	SHT OF
NONE	65 OF 97

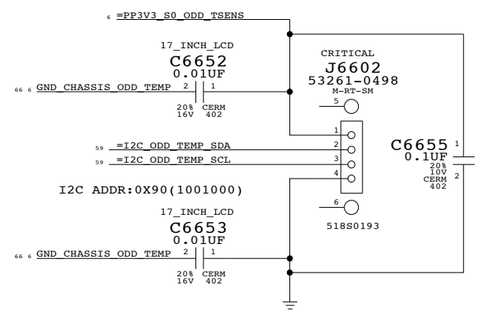
FAN 2



HD TEMP SENSOR



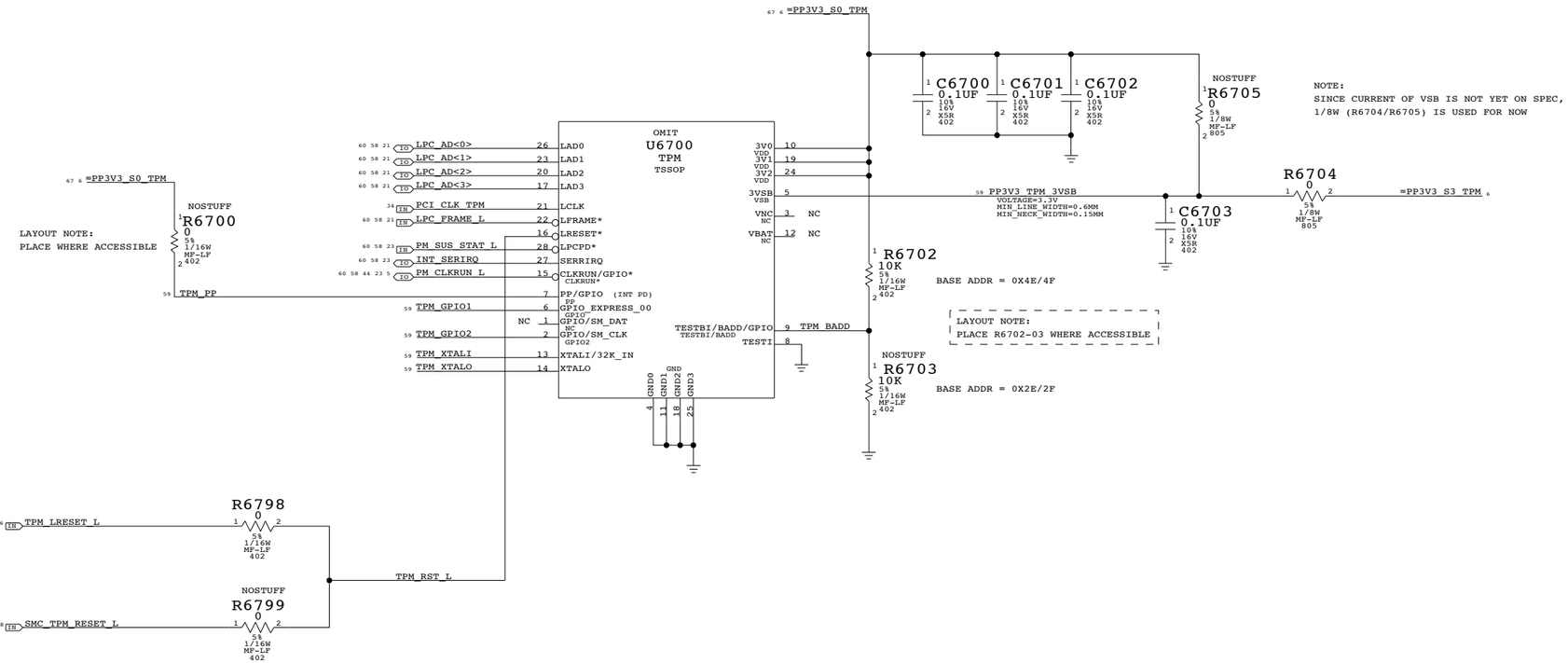
ODD TEMP SENSOR



Fan 2 & HD Temp

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7032	??
SCALE: NONE	SHT 66 OF 97	



TPM

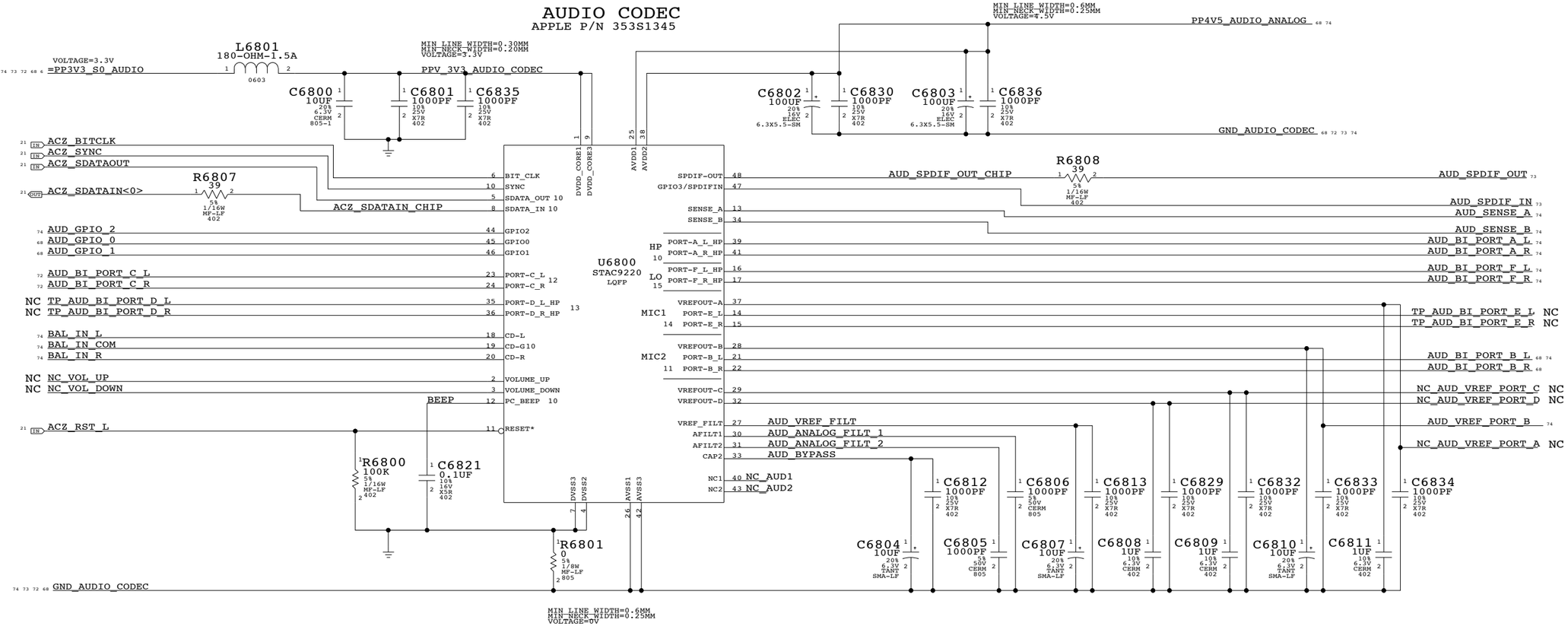
SYNC_MASTER=M38 SYNC_DATE=01/05/2006

NOTICE OF PROPRIETARY PROPERTY

APPLE COMPUTER INC.

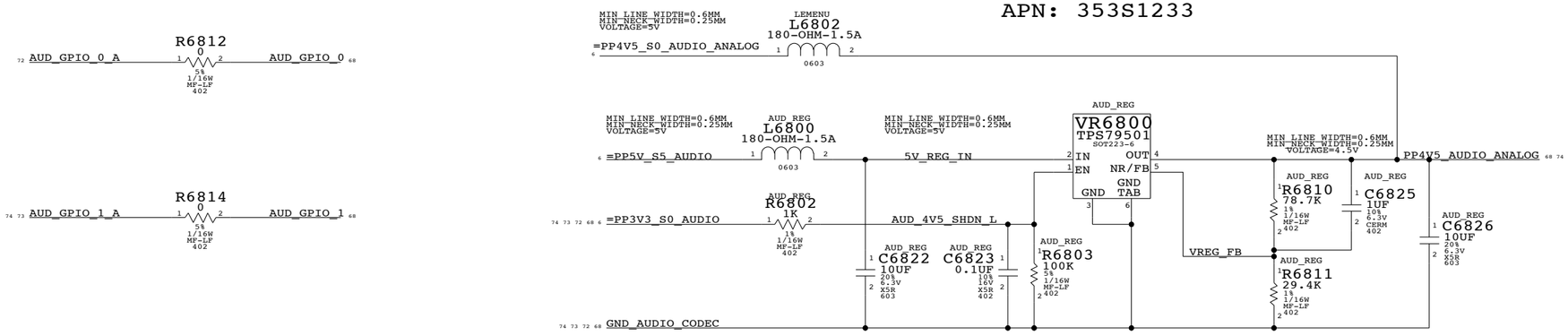
SIZE	DRAWING NUMBER	REV.
D	051-7032	??
SCALE: NONE	SHT 67 OF 97	

AUDIO CODEC
APPLE P/N 353S1345



MIC INPUT TO BOTH L&R

4.5V POWER SUPPLY FOR CODEC AND LINE IN AMP
APN: 353S1233



AUDIO: CODEC

SYNC_MASTER=AUDIO SYNC_DATE=03/30/2006

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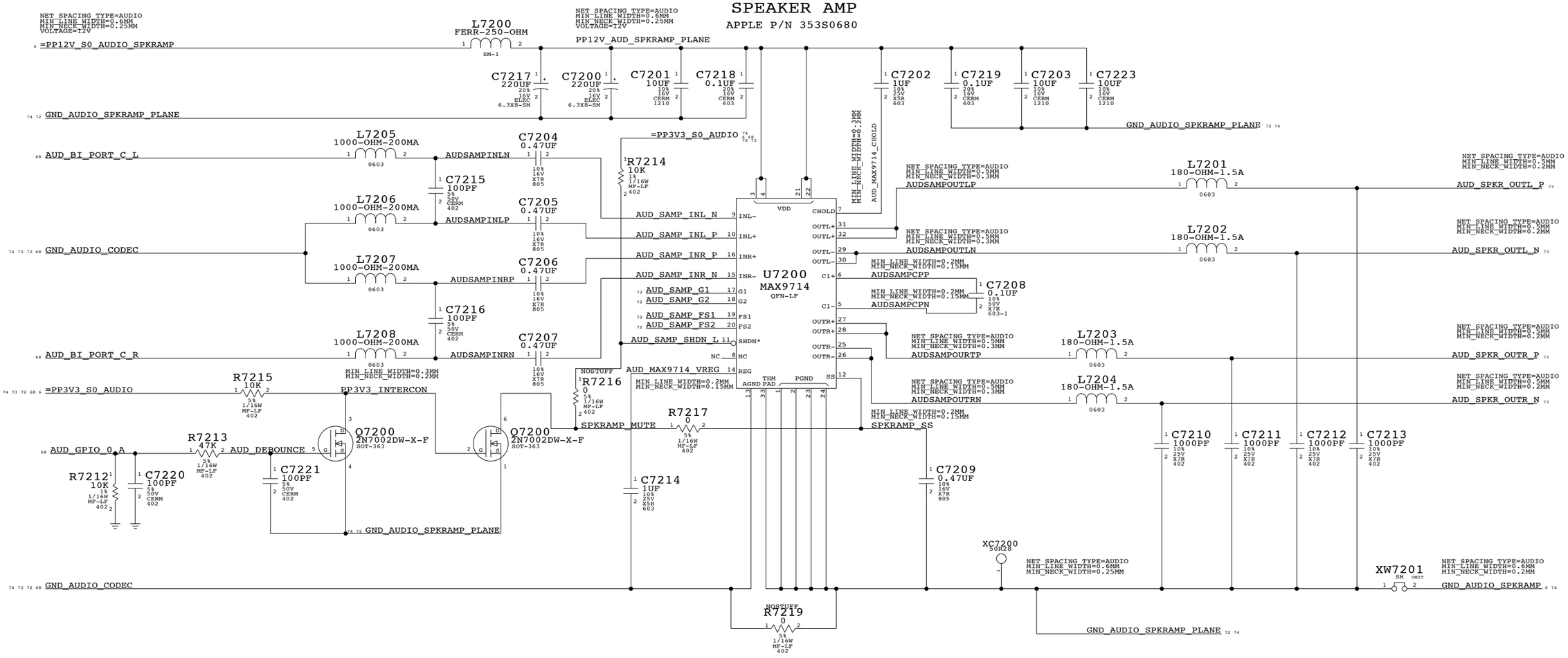
APPLE COMPUTER INC.

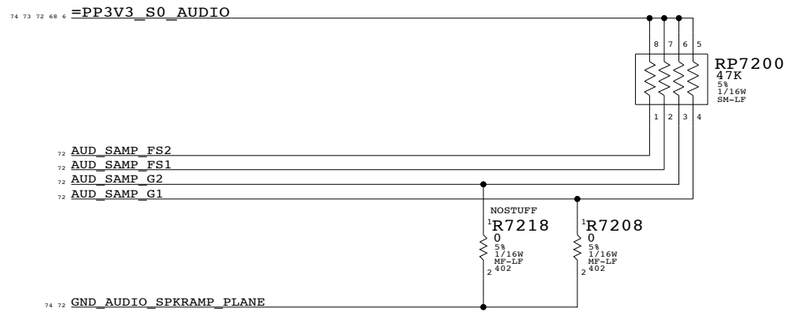
SIZE	DRAWING NUMBER	REV.
D	051-7032	??
SCALE: NONE	SHT 68 OF 97	

SPEAKER AMP

APPLE P/N 353S0680



GAIN SETTINGS: +19DB
MODULATION SETTING: LOW EMI
GAIN AND SWITCHING FREQUENCY STUFF OPTIONS

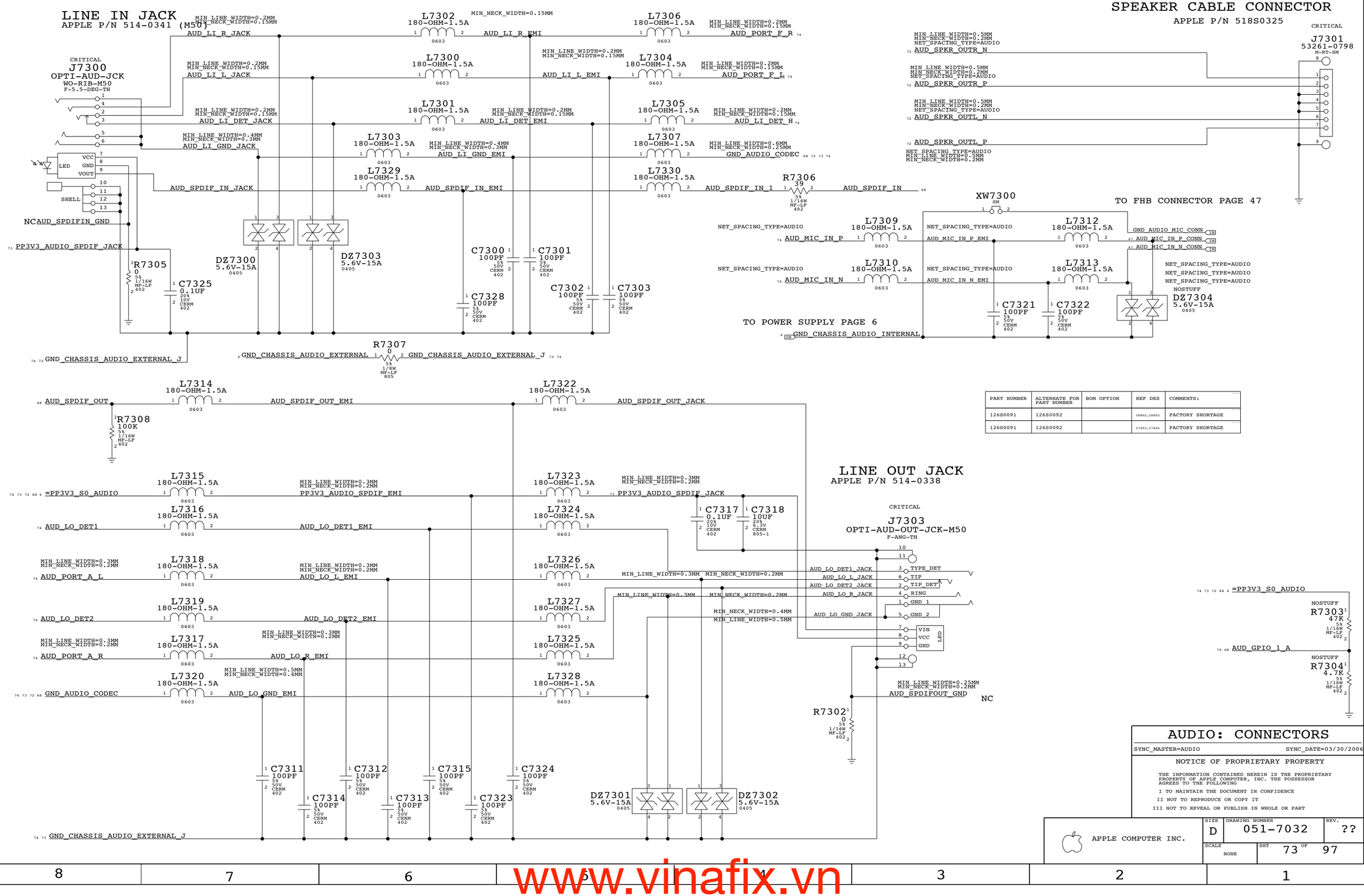


AUDIO: SPEAKER AMP

SYNC_MASTER=AUDIO SYNC_DATE=03/30/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7032	??
SCALE: NONE	SHT 72 OF 97	



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
126S0091	126S0092		C6802,C6803	FACTORY SHORTAGE
126S0091	126S0092		C7403,C7404	FACTORY SHORTAGE

AUDIO: CONNECTORS

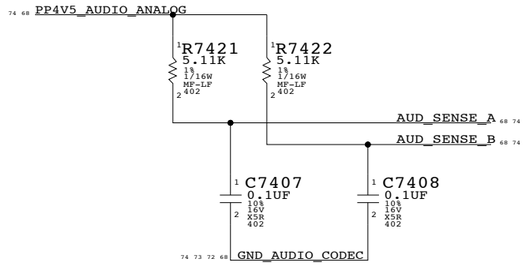
SYNC_MASTER=AUDIO SYNC_DATE=03/30/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7032	??

SCALE: NONE SHT 73 OF 97

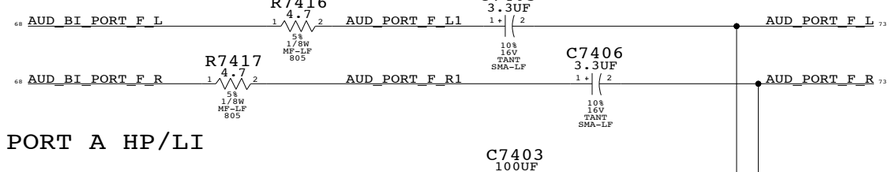
JACK SENSE PULL UPS(PLACE NEXT TO CODEC)



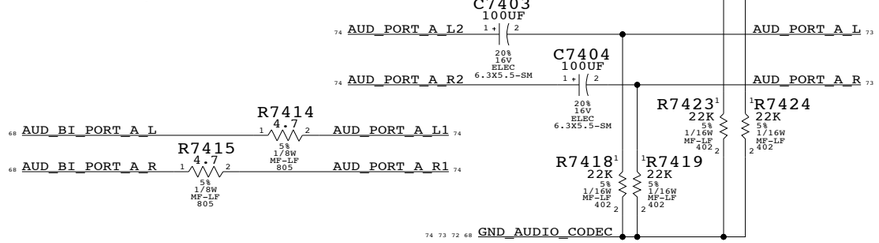
USED PORTS
PORT A HP/LI
PORT B MIC IN
PORT C BI SPEAKERS
PORT F LI/LO

UNUSED PORTS
PORT E
PORT D

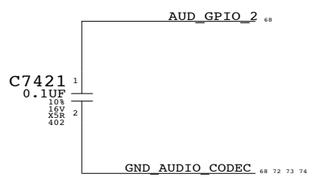
PORT F LI/LO

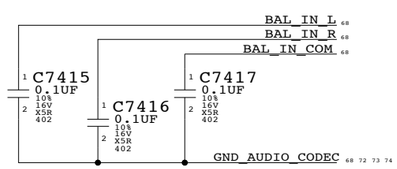


PORT A HP/LI

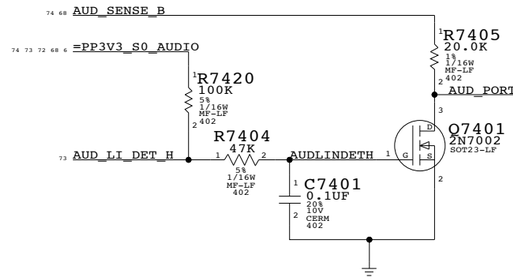


UNUSED PORT TERMINATION

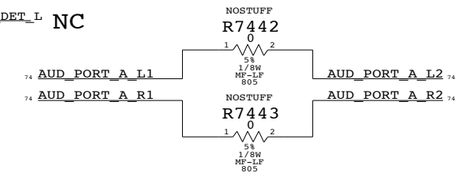


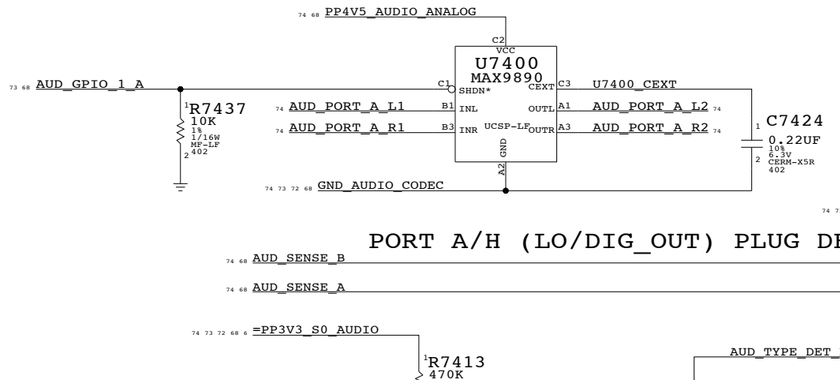


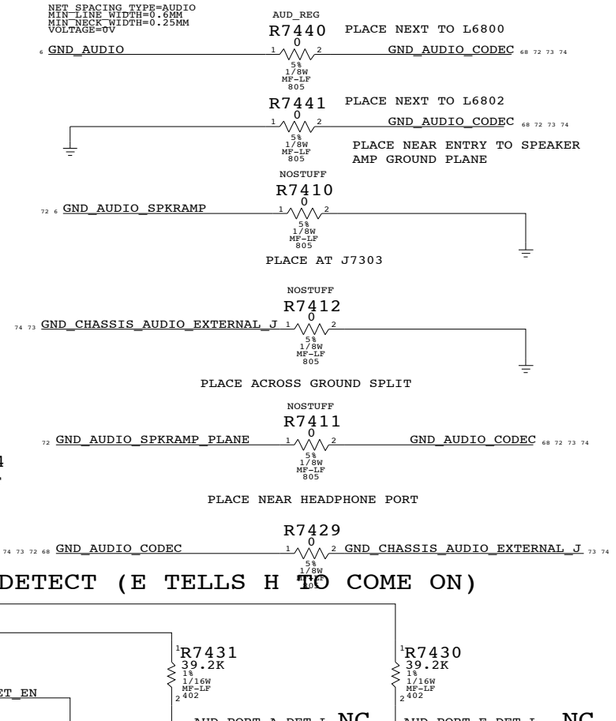
PORT F (LI) PLUG DETECT



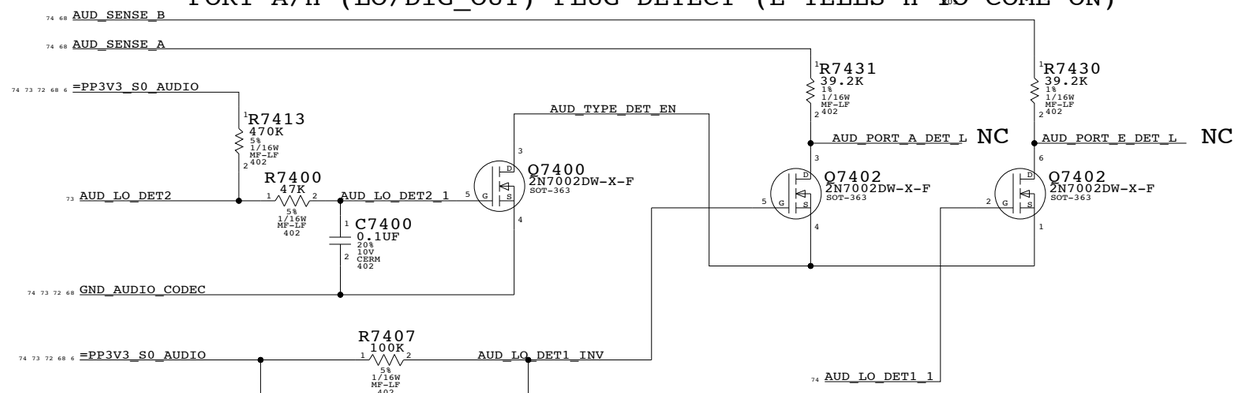
AUDIO GROUND RETURNS



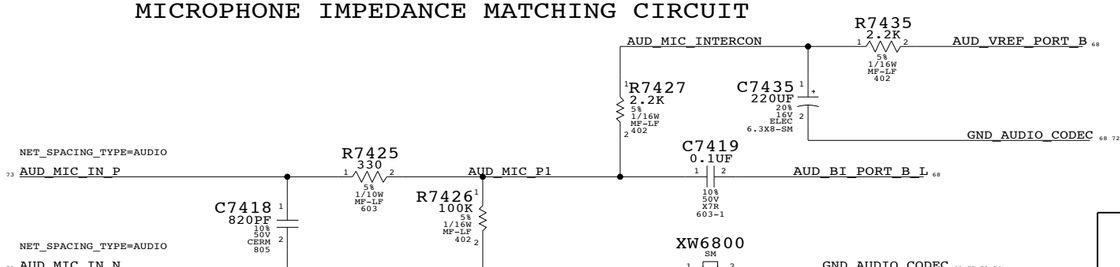




PORT A/H (LO/DIG_OUT) PLUG DETECT (E TELLS H TO COME ON)



MICROPHONE IMPEDANCE MATCHING CIRCUIT



AUDIO: POWER SUPPLIES

SYNC_MASTER=AUDIO
SYNC_DATE=03/30/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7032	??
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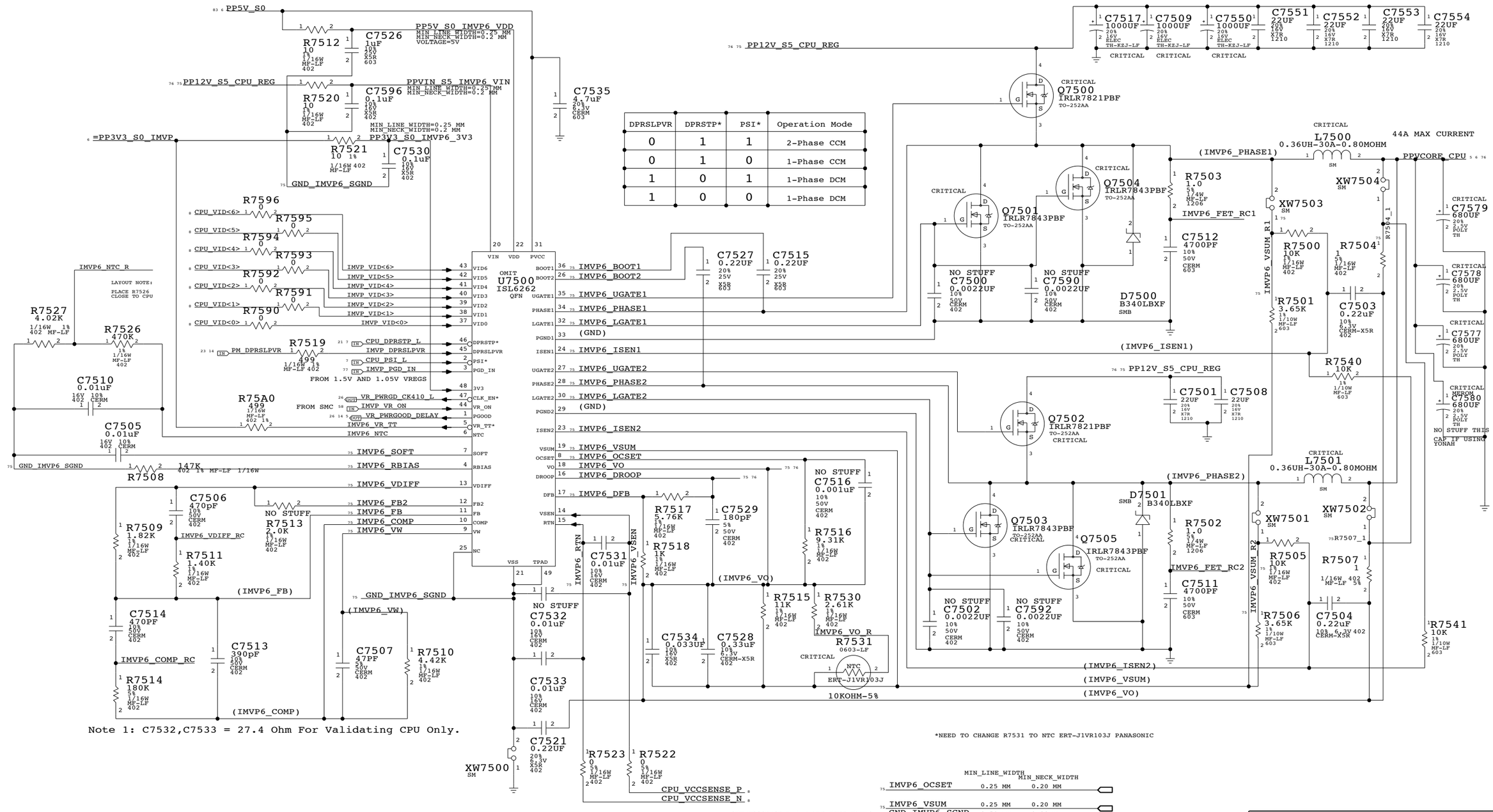

DPRSLPVR	DPRSTP*	PSI*	Operation Mode
0	1	1	2-Phase CCM
0	1	0	1-Phase CCM
1	0	1	1-Phase DCM
1	0	0	1-Phase DCM

*NEED TO CHANGE R7531 TO NTC ERT-J1VR103J PANASONIC

IMVP6 CPU VCORE REGULATOR

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE1	1.5 MM	0.25 MM
IMVP6_BOOT1	0.25 MM	0.25 MM
IMVP6_UGATE1	1.5 MM	0.25 MM
IMVP6_LGATE1	1.5 MM	0.25 MM
IMVP6_ISEN1	0.25 MM	0.25 MM
IMVP6_FET_RC1	0.25 MM	0.25 MM
IMVP6_VSUM_R1	0.25 MM	0.25 MM
R7504_1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE2	0.25 MM	0.25 MM
IMVP6_BOOT2	0.25 MM	0.25 MM
IMVP6_UGATE2	0.25 MM	0.25 MM
IMVP6_LGATE2	0.25 MM	0.25 MM
IMVP6_ISEN2	0.25 MM	0.25 MM
IMVP6_FET_RC2	0.25 MM	0.25 MM
IMVP6_VSUM_R2	0.60 MM	0.25 MM
R7507_1	0.25 MM	0.25 MM

CPU VCCSENSE P & N ARE DIFF PAIRS
ROUTE AS 18MIL WIDE, 7MIL SPACE

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_OCSET	0.25 MM	0.20 MM
IMVP6_VSUM	0.25 MM	0.20 MM
GND_IMVP6_SGND	0.50 MM	0.20 MM
IMVP6_VO	0.25 MM	0.20 MM
IMVP6_DROOP	0.25 MM	0.20 MM
IMVP6_DFB	0.25 MM	0.20 MM
IMVP6_SOFT	0.25 MM	0.20 MM
IMVP6_RBIAS	0.25 MM	0.20 MM
IMVP6_VDIFF	0.25 MM	0.20 MM
IMVP6_FB2	0.25 MM	0.20 MM
IMVP6_FB	0.25 MM	0.20 MM
IMVP6_COMP	0.25 MM	0.20 MM
IMVP6_VW	0.25 MM	0.25 MM
IMVP6_RTN	0.25 MM	0.25 MM
IMVP6_VSEN	0.25 MM	0.25 MM

IMVP6 CPU VCore Regulator

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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APPLE COMPUTER INC.

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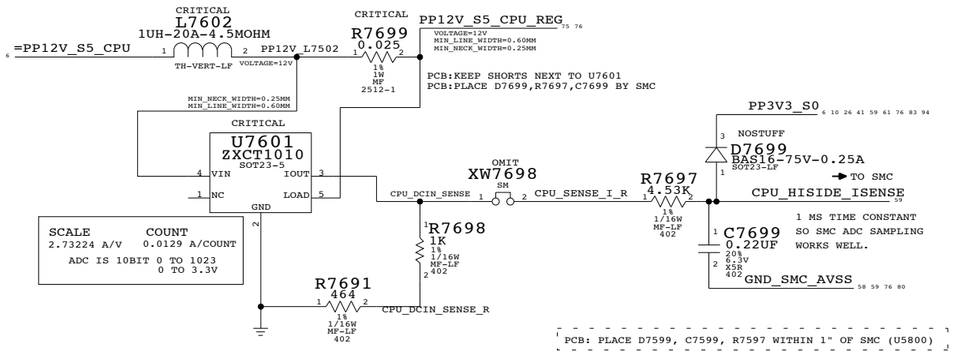
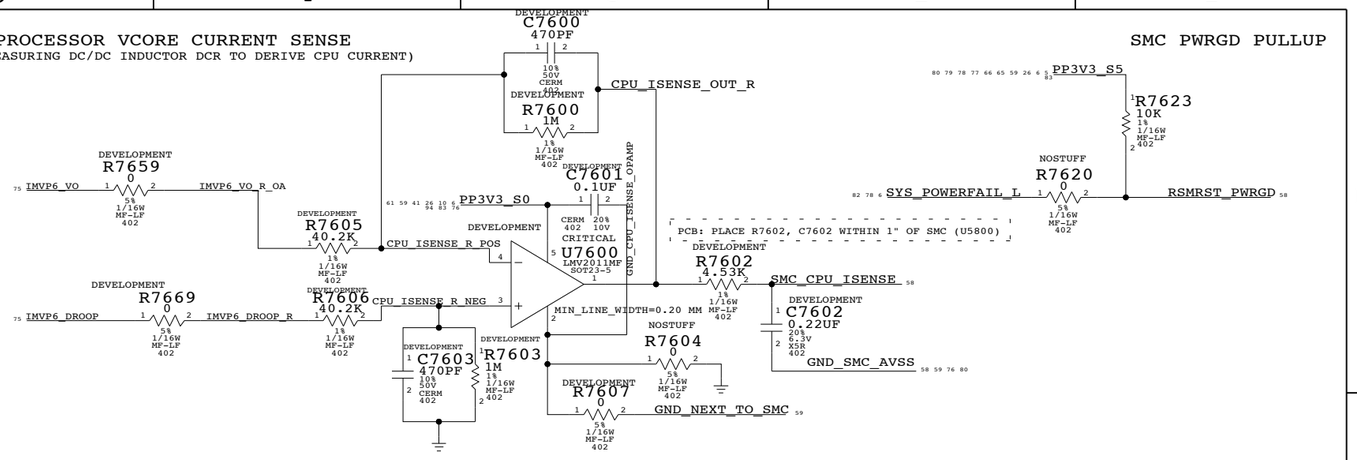
D	051-7032	??
SCALE: NONE	SHT 75 OF 97	

PROCESSOR VCORE CURRENT SENSE
(USING 12V INPUT CURRENT TO DERIVE CPU CURRENT)

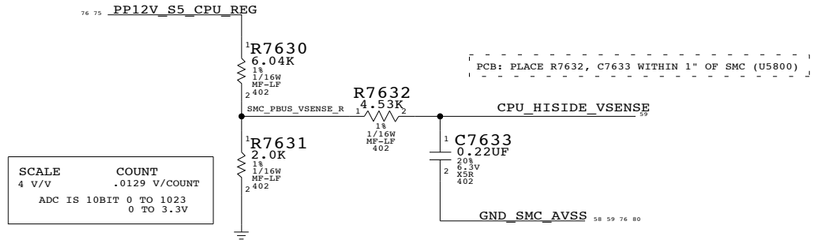


PROCESSOR VCORE CURRENT SENSE
(MEASURING DC/DC INDUCTOR DCR TO DERIVE CPU CURRENT)

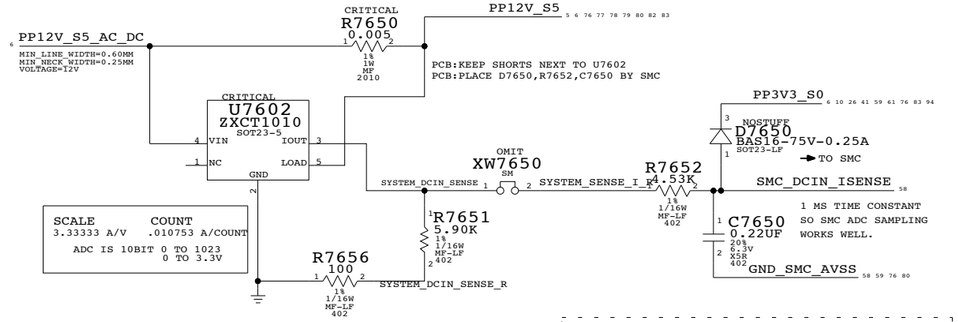


SMC PWRGD PULLUP

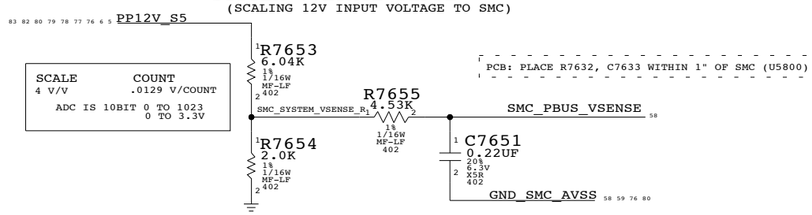
PROCESSOR DCIN VOLTAGE SENSE
(SCALING 12V INPUT VOLTAGE TO SMC)



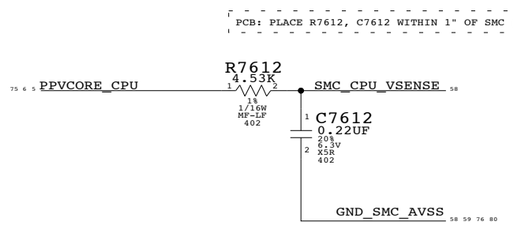
SYSTEM CURRENT SENSE



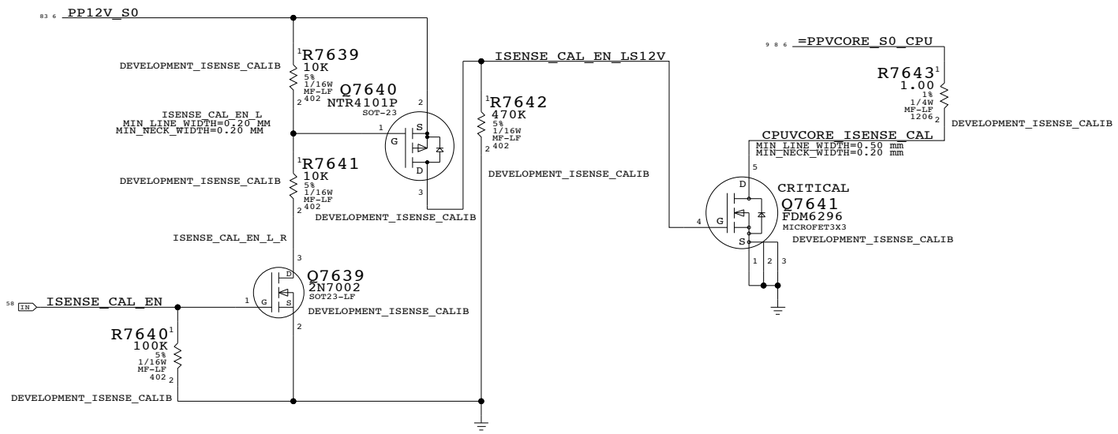
SYSTEM VOLTAGE SENSE
(SCALING 12V INPUT VOLTAGE TO SMC)



PROCESSOR VCORE SENSE

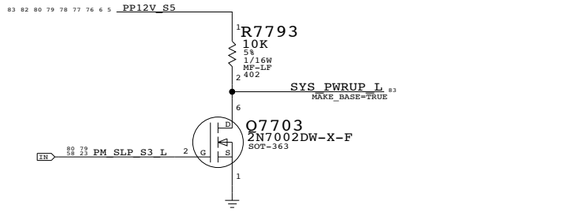


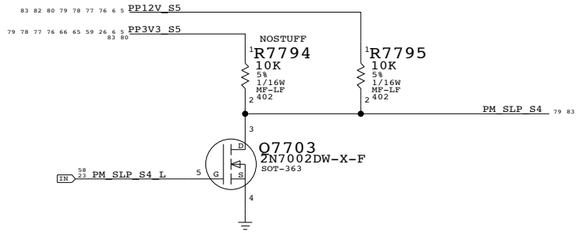
Current Sense Calibration Circuit
Switches in fixed load on power supplies to calibrate current sense circuits

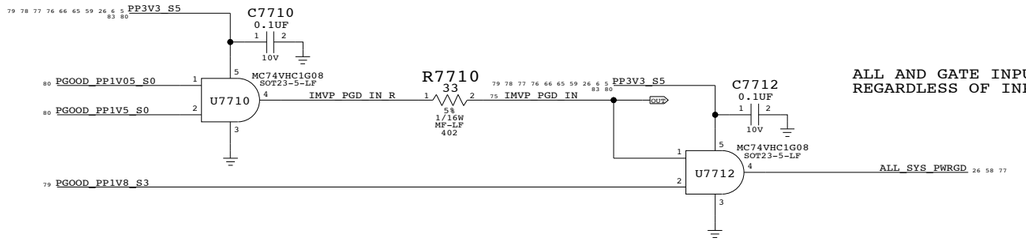


APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7032	??
SCALE: NONE	SHT 76 OF 97	

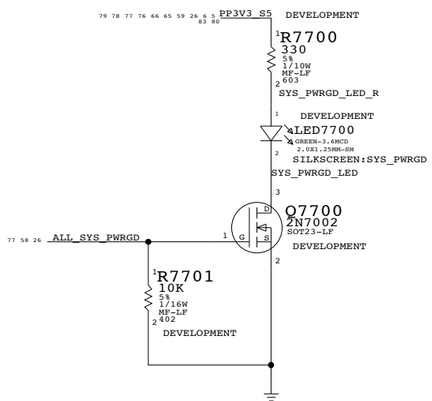






ALL AND GATE INPUTS ARE 7V TOLERANT
REGARDLESS OF INPUT POWER

PWGOOD SIMPLIFIED BASED ON
TIMING OF VARIOUS RAILS COMING UP
AS MEASURED ON PROTO2 BOARDS



PWR GOOD

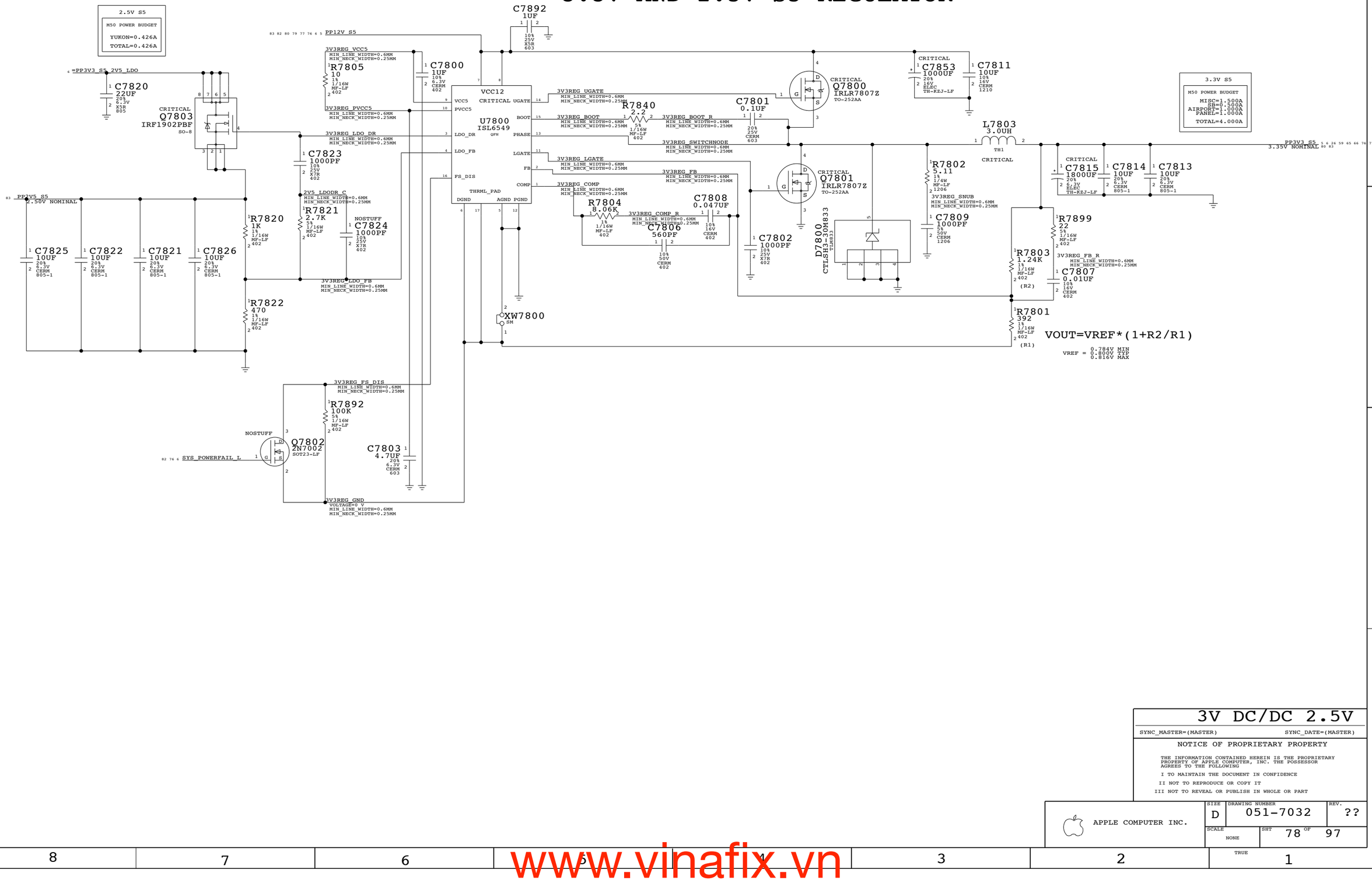
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7032	??

SCALE NONE SHT 77 OF 97

3.3V AND 2.5V S5 REGULATOR



3V DC/DC 2.5V

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

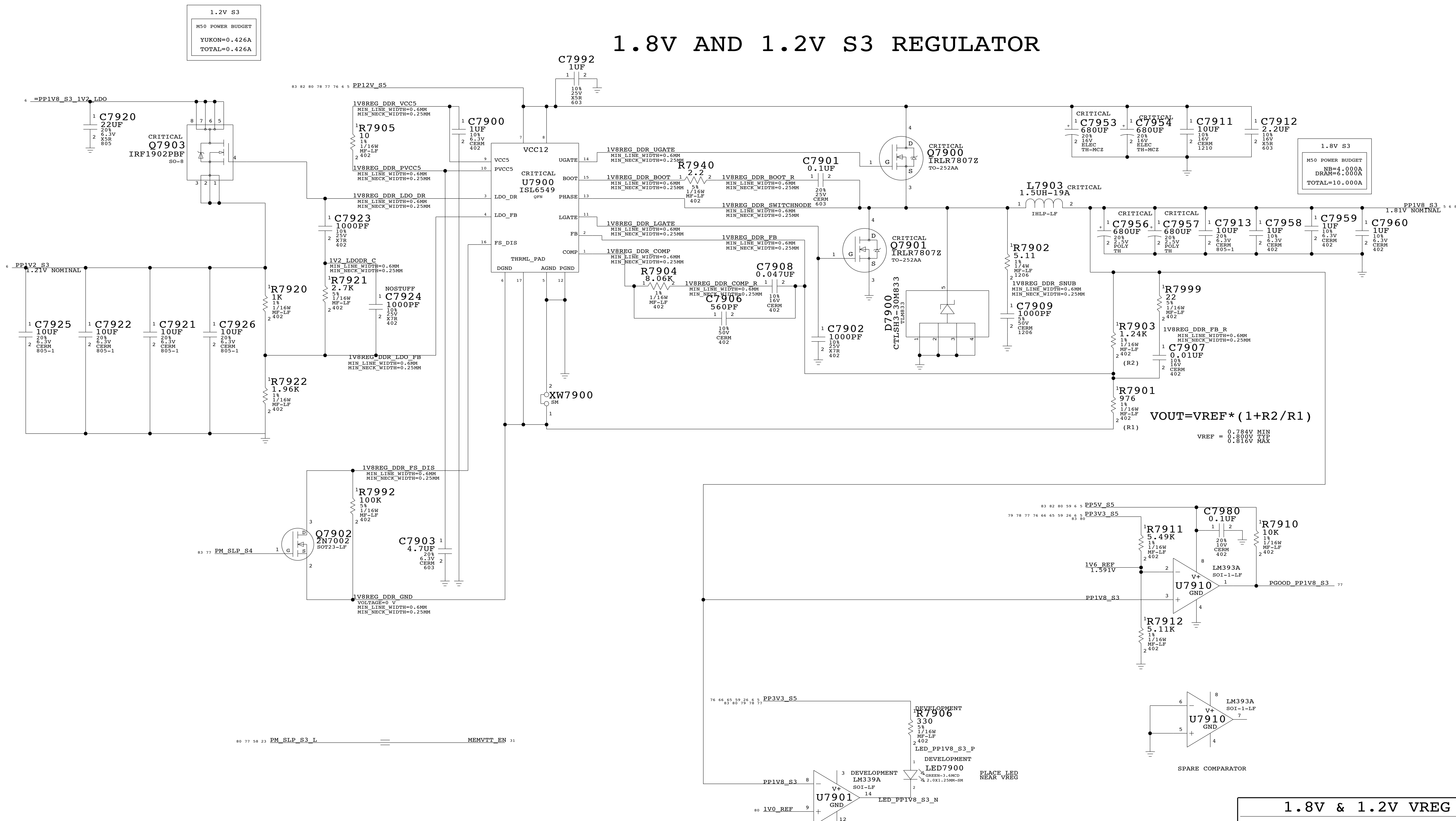
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7032	??

SCALE NONE | SHT 78 OF 97

TRUE

1.8V AND 1.2V S3 REGULATOR


1.2V S3
M50 POWER BUDGET
YUKON=0.426A
TOTAL=0.426A
1.8V S3
M50 POWER BUDGET
NB=4.000A
DRAM=6.000A
TOTAL=10.000A
=PP1V8_S3_1V2_LDO
PP12V_S5
PP1V2_S3
1.21V NOMINAL
PP1V8_S3
1.81V NOMINAL
C7920 22UF
CRITICAL Q7903 IRF1902PBF SO-8
C7992 1UF
C7900 1UF
R7905 10
1V8REG_DDR_VCC5
1V8REG_DDR_PVCC5
1V8REG_DDR_LDO_DR
1V8REG_DDR_LDO_FB
1V2_LDODR_C
C7923 1000PF
R7921 2.7K
NOSTUFF C7924 1000PF
R7920 1K
R7922 1.96K
C7925 10UF
C7922 10UF
C7921 10UF
C7926 10UF
CRITICAL U7900 ISL6549 QFN
VCC12 VCC5 PVCC5 LDO_DR LDO_FB FS_DIS UGATE BOOT PHASE LGATE FB COMP THRML_PAD DGND AGND PGND
1V8REG_DDR_UGATE
1V8REG_DDR_BOOT
1V8REG_DDR_BOOT_R
1V8REG_DDR_SWITCHNODE
1V8REG_DDR_LGATE
1V8REG_DDR_FB
1V8REG_DDR_COMP
1V8REG_DDR_COMP_R
R7940 2.2
C7901 0.1UF
R7904 8.06K
C7908 0.047UF
C7906 560PF
CRITICAL Q7900 IRLR7807Z TO-252AA
CRITICAL Q7901 IRLR7807Z TO-252AA
D7900 CTLSH3-30M833
L7903 1.5UH-19A CRITICAL IHLP-LF
C7902 1000PF
R7902 5.11
C7909 1000PF
1V8REG_DDR_SNUB
CRITICAL C7953 680UF
CRITICAL C7954 680UF
C7911 10UF
C7912 2.2UF
CRITICAL C7956 680UF
CRITICAL C7957 680UF
C7913 10UF
C7958 1UF
C7959 1UF
C7960 1UF
R7999 22
1V8REG_DDR_FB_R
R7903 1.24K (R2)
C7907 0.01UF
R7901 976 (R1)
VOUT=VREF*(1+R2/R1)
VREF = 0.784V MIN 0.800V TYP 0.816V MAX
XW7900 SM
1V8REG_DDR_FS_DIS
R7992 100K
Q7902 2N7002 SOT23-LF
PM_SLP_S4
C7903 4.7UF
1V8REG_DDR_GND VOLTAGE=0 V
PM_SLP_S3_L
MEMVTT_EN
PP5V_S5
PP3V3_S5
C7980 0.1UF
R7911 5.49K
R7910 10K
1V6_REF 1.591V
U7910 LM393A SOI-1-LF
PGOOD_PP1V8_S3
R7912 5.11K
SPARE COMPARATOR
DEVELOPMENT R7906 330
LED_PP1V8_S3_P
DEVELOPMENT LED7900 GREEN-3.6MCD 2.0X1.25MM-SM
PLACE LED NEAR VREG
DEVELOPMENT U7901 LM339A SOI-LF
1V0_REF
LED_PP1V8_S3_N

1.8V & 1.2V VREG			
SYNC_MASTER=MASTER		SYNC_DATE=MASTER	

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7032	REV. ??
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1.5V S0 AND 1.05V S0 RAILS

Placement Note:
KEEP C8080, R8080,
R8084 AND R8087
close to inductor

1.5V S0
M50 POWER BUDGET
CPU=0.120A
NB=8.000A
SB=2.000A
TOTAL=10.120A

1.05V S0
M50 POWER BUDGET
CPU=2.500A
NB=2.000A
SB=0.874A
TOTAL=5.374A

SYNC_MASTER=MASTER	SYNC_DATE=MASTER

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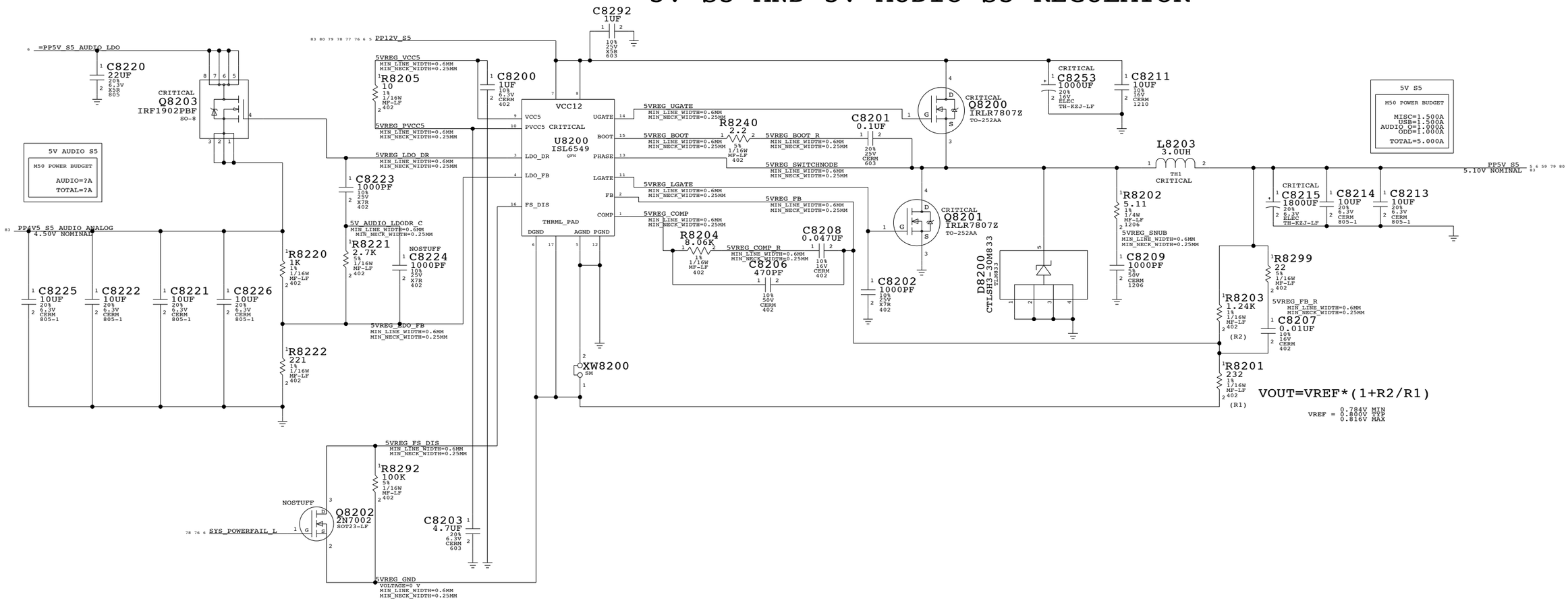
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7032	??
SCALE: NONE	SHT 80 OF 97	

5V S5 AND 5V AUDIO S5 REGULATOR



POWER SUPPLY 3.3V/5V MAIN SWITCH

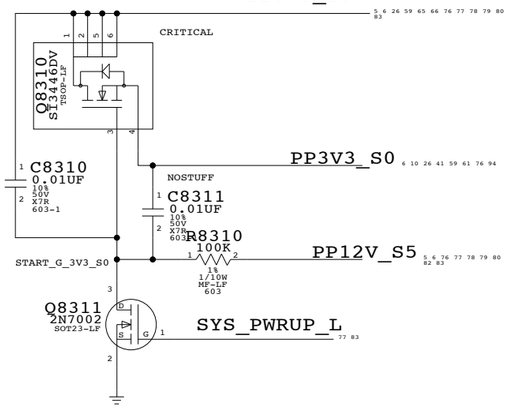
5V DC/DC

SYNC_MASTER=MASTER SYNC_DATE=MASTER

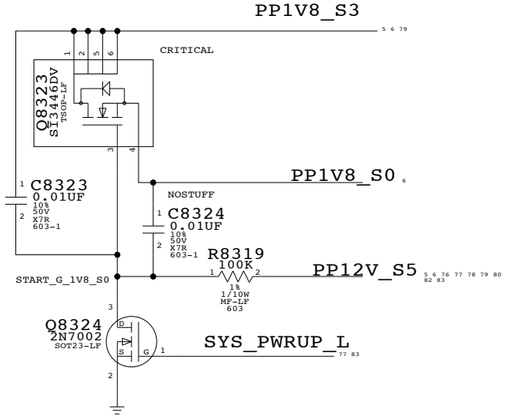
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7032	??
SCALE: NONE	SHT 82 OF 97	

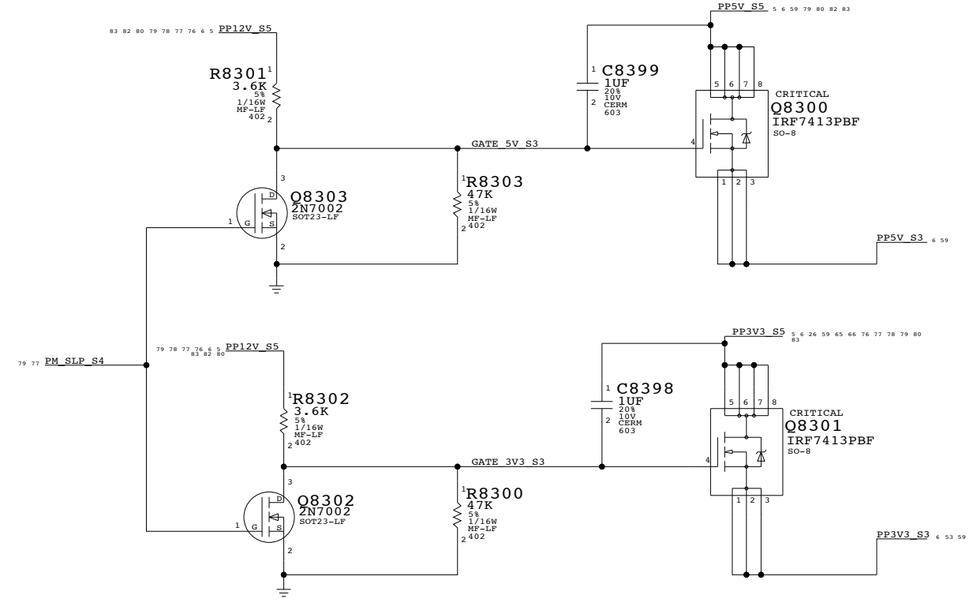
3.3V S0



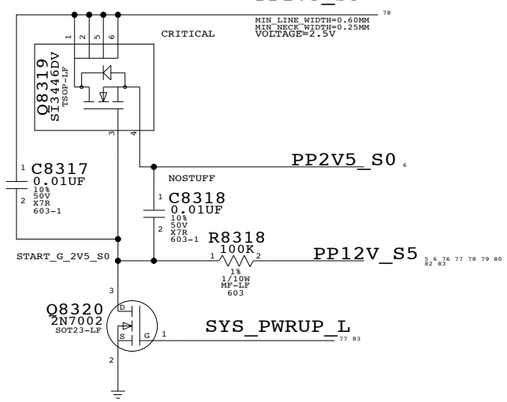
1.8V S0



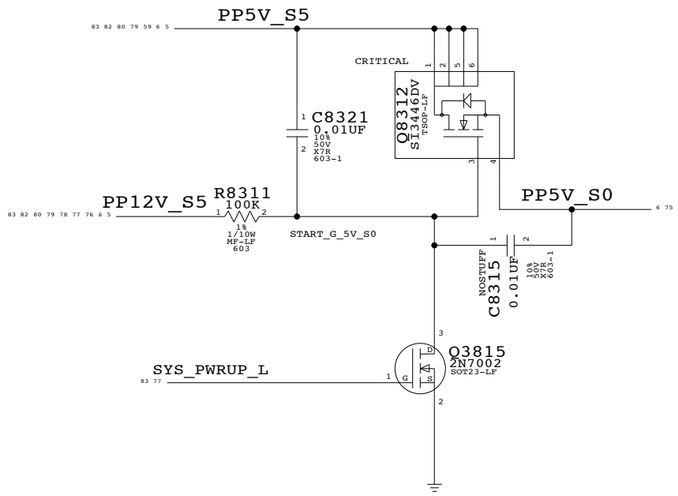
3.3V AND 5V S3



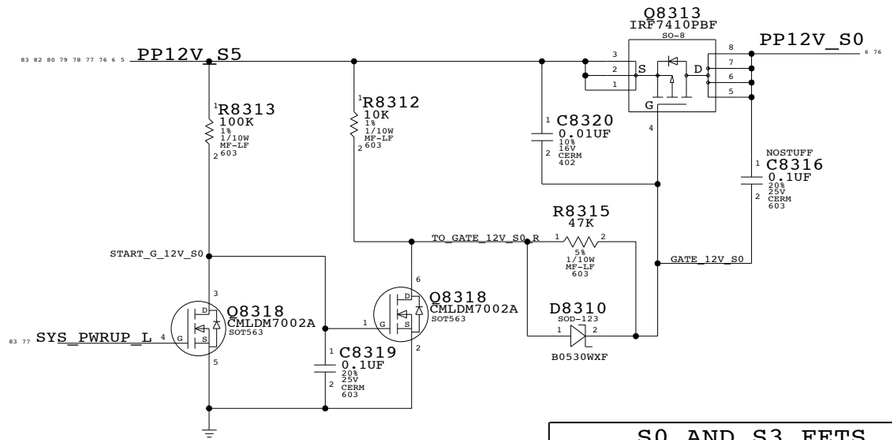
2.5V S0



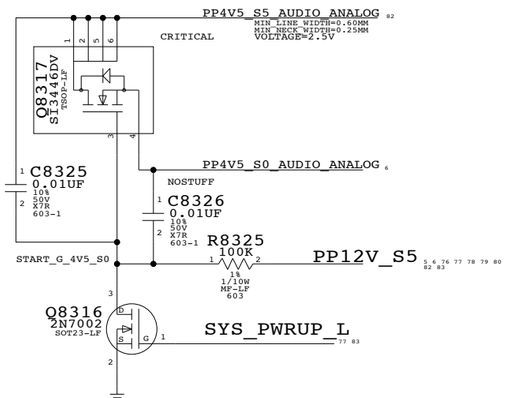
5V S0



12V S0



4.5V S0 AUDIO



S0 AND S3 FETS

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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SIZE	DRAWING NUMBER	REV.
D	051-7032	??
SCALE: NONE	SHT 83 OF 97	

83 76 61 59 41 26 10 6 PP3V3_S0

I512

=PP3V3_DDC_LCD 94

LCD (LVDS) INTERFACE

94 6 =PP3V3_S0_LCD

R9402
0
5%
1/8W
MF-LF
805
NOSTUFF

6 =PP3V3_S5_LCD

C9400
0.1UF
20%
16V
CERM
603

R9400 1
100K
5%
1/16W
MF-LF
402 2

R9401
47K
5%
1/16W
MF-LF
402

LCD_PWREN_L_RC

CRITICAL

Q9400
SI3443DV
TSOP-LF

PP3V3_LCD_SW
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm

L9400
FERR-250-OHM
SM

VOLTAGE=3.3V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
PP3V3_LCD_CONN 6 94

C9401
0.001UF
10%
50V
CERM
402

C9420
10UF
10%
16V
CERM
1210

LCD_PWREN_L

Q9401
2N7002
SOT23-LF

13 LVDS_VDDEN

R9470 1
100K
5%
1/16W
MF-LF
402

INTEL RECOMMENDS
10K PULL-UPS ON I2C LINES
PANEL HAS 4.2K PULL-UPS

94 =PP3V3_DDC_LCD

R9410 1
100K
5%
1/16W
MF-LF
402

R9411 1
100K
5%
1/16W
MF-LF
402

C9410
0.001UF
10%
50V
CERM
402

94 13 LVDS_DDC_CLK

94 13 LVDS_DDC_DATA

INVERTER INTERFACE

6 =PP12V_INVERTER

C9450
4.7UF
20%
16V
CERM
1206-1

CRITICAL

J9401
87437-0443-BLK
M-ST-SM

518S0331

94 LCD_PWM

94 PANEL_ID

94 6 =PP3V3_S0_LCD

R9451 1
10K
5%
1/16W
MF-LF
402

RESISTOR TO SET DEFAULT VALUE OF PANEL ID

22 SB_GPIO_48

R9450
47
5%
1/16W
MF-LF
402

PANEL_ID 94

94 6 =PP3V3_S0_LCD

NOSTUFF
C9470 1
0.1UF
20%
16V
CERM
402 2

NOSTUFF
U9470
MC74VHC1G08
SOT23-5-LF

6 GPU_PWM_RST_L

13 LVDS_BKLTCTL

NOSTUFF
R9472 1
10K
5%
1/16W
MF-LF
402

LCD_PWM_R

R9474 1
10K
5%
1/16W
MF-LF
402

R9475
47
5%
1/16W
MF-LF
402

LCD_PWM 94

R9473
0
5%
1/16W
MF-LF
402

GATE TO PREVENT LEAKAGE ONTO PWM
MIGHT BE ABLE TO BYPASS IF SMC DRIVES SIGNAL

SDF9400
STDOFF-3MMOD4.6MMH-1.35-TH

CRITICAL

J9402
53307-3072
F-ST-SM

13 LVDS_B_DATA_N<0>	1	2	LVDS_B_DATA_P<0> 13
13 LVDS_B_DATA_N<1>	3	4	LVDS_B_DATA_P<1> 13
13 LVDS_B_DATA_N<2>	5	6	LVDS_B_DATA_P<2> 13
	7	8	LVDS_B_CLK_N 13
13 LVDS_B_CLK_P	9	10	
	11	12	LVDS_A_DATA_N<0> 13
13 LVDS_A_DATA_P<0>	13	14	
13 LVDS_A_DATA_N<1>	15	16	LVDS_A_DATA_P<1> 13
	17	18	LVDS_A_DATA_N<2> 13
13 LVDS_A_DATA_P<2>	19	20	LVDS_A_CLK_N 13
13 LVDS_A_CLK_P	21	22	
	23	24	
94 13 LVDS_DDC_CLK	25	26	LVDS_DDC_DATA 13 94
94 =PP3V3_DDC_LCD	27	28	PP3V3_LCD_CONN 6 94
94 6 PP3V3_LCD_CONN	29	30	PP3V3_LCD_CONN 6 94

SDF9401
STDOFF-3MMOD4.6MMH-1.35-TH

94 6 =PP3V3_S0_LCD

R9420 1
10K
5%
1/16W
MF-LF
402

R9421 1
10K
5%
1/16W
MF-LF
402

13 LVDS_CLKCTLA

13 LVDS_CLKCTLB

I513

LVDS_VREFH 13

I514

LVDS_VREFL 13

LVDS REFERENCE CURRENT, 1.5K OHM PULL DOWN RESISTOR NEEDED

R9422
1.5K
1%
1/16W
MF-LF
402

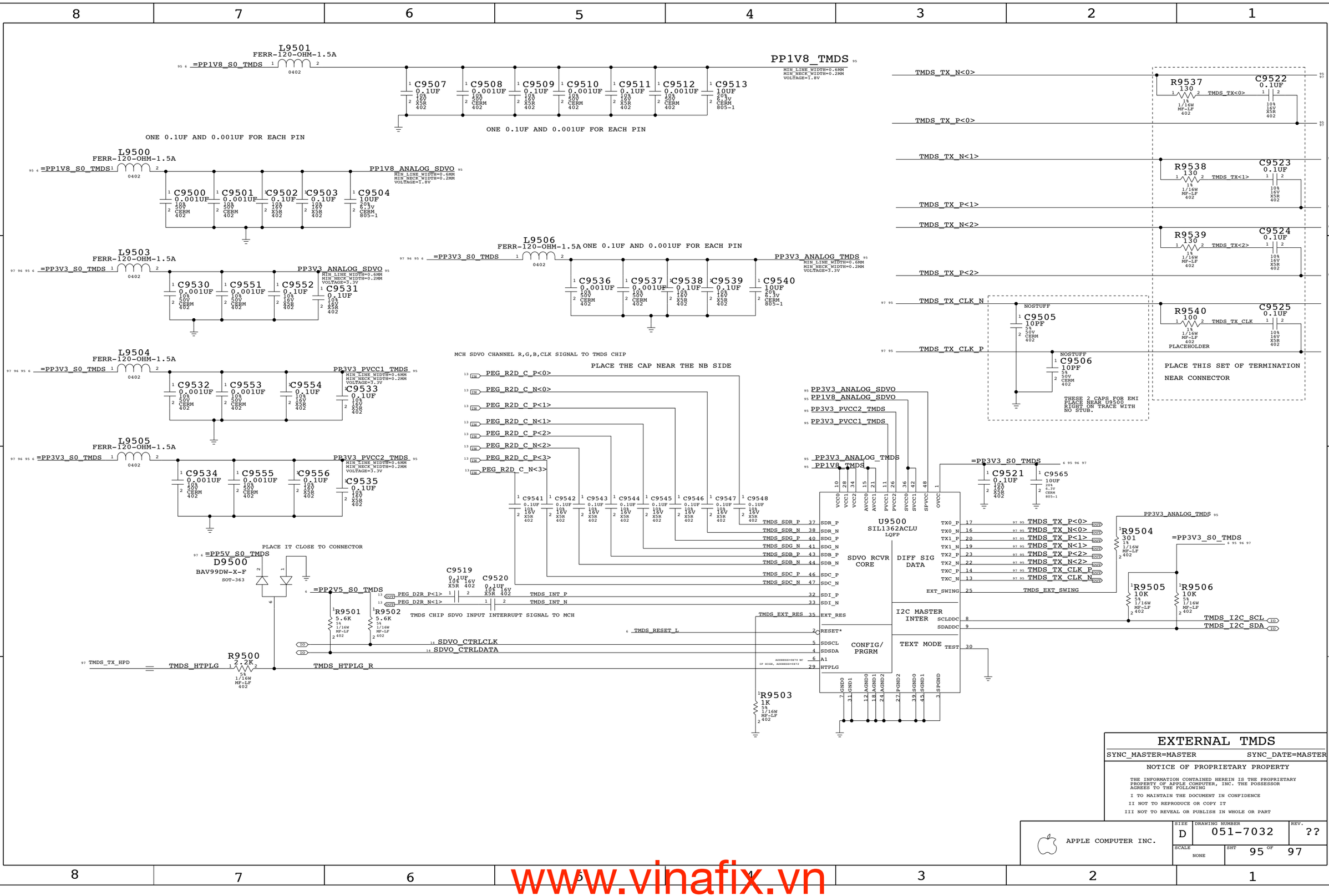
13 LVDS_IBG

Internal Display Conns

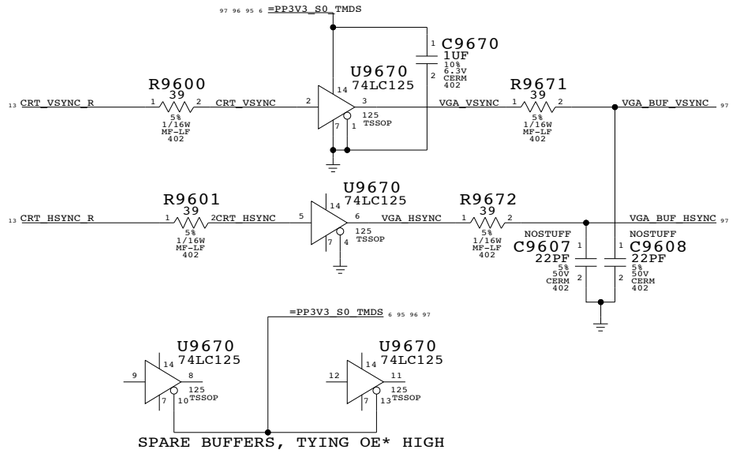
SYNC_MASTER=MASTER SYNC_DATE=MASTER

APPLE COMPUTER INC.

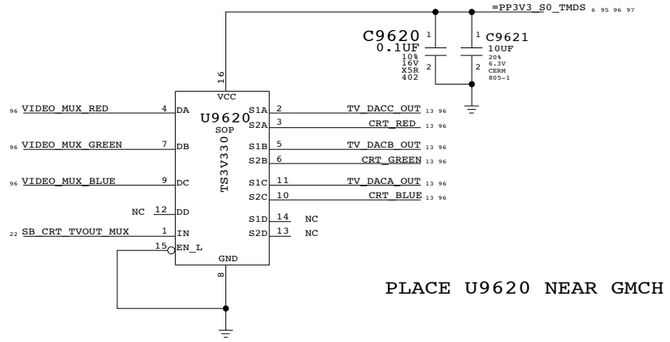
SIZE	DRAWING NUMBER	REV.
D	051-7032	??
SCALE: NONE	SHT 94 OF 97	



VGA SYNC BUFFERS

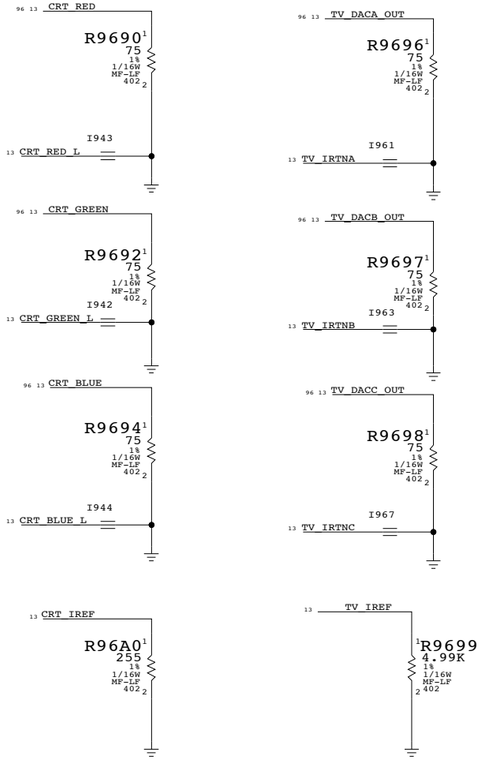


VIDEO_MUX_SEL	OUT
1	CRT
0	TV

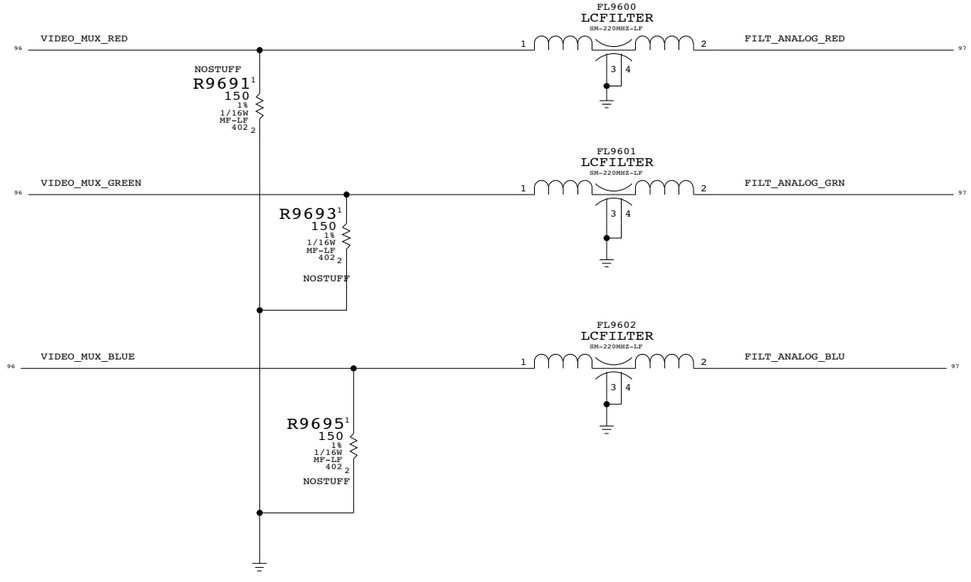


PLACE U9620 NEAR GMCH

PLACE RESISTORS AT NORTHBRIDGE



ANALOG FILTERING
PLACE BY CONNECTOR



TMDS/Inverter/ExtVGA		
SYNC_MASTER=MASTER	SYNC_DATE=MASTER	
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APPLE COMPUTER INC.	SIZE D / DRAWING NUMBER 051-7032 / REV. ??	
	SCALE NONE / SHT 96 OF 97	

PLACE LEFT SIDE
AS CLOSE TO GPU (U8400)
AS POSSIBLE

PLACE FILTER CLOSE
TO TMDS CONNECTOR

DVI INTERFACE

DVI DDC CURRENT LIMIT
(55mA requirement per DVI spec)

CRITICAL

D9710
SOD-123
B0530WXF

F9710
0.5AMP-13.2V
SM-LF

L9710
400-OHM-EMI
SM-1

=PP5V_S0_TMDS → PP5V_S0_TMDS_D → PP5V_S0_DDC_FUSE → PP5V_S0_DDC
VOLTAGE=5V
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm

L9700 CRITICAL
90-OHM-300MA
2012H
TMDS_TX_N<0> → TMDS_CONN_DN<0>
TMDS_TX_P<0> → TMDS_CONN_DP<0>
DIFFERENTIAL_PAIR=TMDS_TX_0
DIFFERENTIAL_PAIR=TMDS_CONN_D0

L9701 CRITICAL
90-OHM-300MA
2012H
TMDS_TX_N<1> → TMDS_CONN_DN<1>
TMDS_TX_P<1> → TMDS_CONN_DP<1>
DIFFERENTIAL_PAIR=TMDS_TX_1

L9702 CRITICAL
90-OHM-300MA
2012H
TMDS_TX_N<2> → TMDS_CONN_DN<2>
TMDS_TX_P<2> → TMDS_CONN_DP<2>
DIFFERENTIAL_PAIR=TMDS_TX_2
DIFFERENTIAL_PAIR=TMDS_CONN_D2

L9703 OMIT CRITICAL
165-OHM
SM
TMDS_TX_CLK_P → TMDS_CONN_CLKP
TMDS_TX_CLK_N → TMDS_CONN_CLKN
DIFFERENTIAL_PAIR=TMDS_TX_CLK

OMIT
514S0128
J9710
MINI-DVI
F-ST-SM4

DVI_HPD_UF	25	TMDS_CONN_DP<2>
	17	
DVI_DDC_CLK_UF	26	TMDS_CONN_DN<2>
DVI_DDC_DATA_UF	18	
	27	TMDS_CONN_DP<1>
	19	
	28	TMDS_CONN_DN<1>
FILT_ANALOG_BLU	20	
VGA_BUF_HSYNC	29	TMDS_CONN_DP<0>
	30	TMDS_CONN_DN<0>
FILT_ANALOG_GRN	22	
VGA_BUF_VSYNC	31	TMDS_CONN_CLKP
	32	TMDS_CONN_CLKN
FILT_ANALOG_RED	24	
	S3	
	S4	

1	9	TMDS_CONN_DP<2>
2	10	TMDS_CONN_DN<2>
3	11	TMDS_CONN_DP<1>
4	12	TMDS_CONN_DN<1>
5	13	TMDS_CONN_DP<0>
6	14	TMDS_CONN_DN<0>
7	15	TMDS_CONN_CLKP
8	16	TMDS_CONN_CLKN

GND_CHASSIS_VGA_C_A
GND_CHASSIS_VGA_C_B
GND_CHASSIS_VGA

C9720 0.1UF 10% 16V X5R 402
C9721 0.1UF 10% 16V X5R 402
C9722 0.1UF 10% 16V X5R 402
C9723 0.1UF 10% 16V X5R 402

3V LEVEL SHIFTERS

PP5V_S0_DDC
=PP3V3_S0_TMDS

R9710 4.7K 5% 1/16W MF-LF 402
R9712 4.7K 5% 1/16W MF-LF 402

Q9711 2N7002DW-X-F SOT-363

R9711 100 5% 1/16W MF-LF 402
DVI_DDC_CLK_UF → DVI_DDC_CLK → CRT_DDC_CLK

R9720 10K 5% 1/16W MF-LF 402

C9711 100pF 5% 50V CERM 402

Q9711 2N7002DW-X-F SOT-363

R9721 10K 5% 1/16W MF-LF 402

R9713 100 5% 1/16W MF-LF 402
DVI_DDC_DATA_UF → DVI_DDC_DATA → CRT_DDC_DATA

C9713 100pF 5% 50V CERM 402

R9714 20.0K 1% 1/16W MF-LF 402
DVI_HPD_UF → TMDS_TX_HPD

R9722 100K 5% 1/16W MF-LF 402

D9700 CASE425 MMSZ4681XXG

C9710 0.01UF 10% 50V X7R 603-1

C9714 100pF 5% 50V CERM 402

WHEN PART AVAILABILITY FINALIZES,
REMOVE TABLE AND OMIT ON PART

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514S0128	1	MINI DVI CONNECTOR,32P,TH SHIELD, W/O RIBS	J9710	CRITICAL	

External Display Conns

SYNC_MASTER=MASTER SYNC_DATE=MASTER

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7032	??
SCALE: NONE	SHT 97 OF 97	