

IM4, 2 - REV A

05/18/06

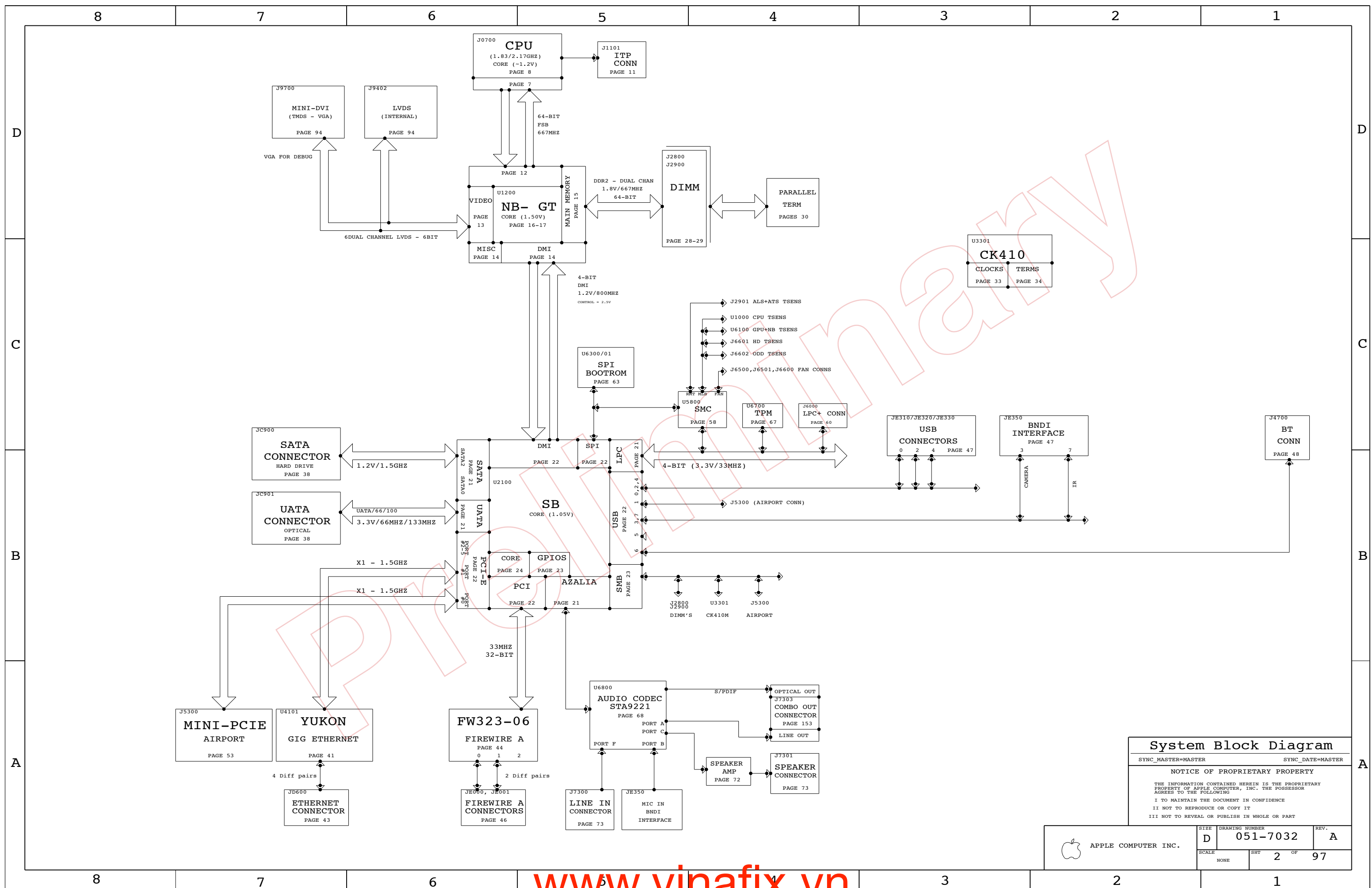
1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
A		440263	PRODUCTION RELEASED	05/18/06	06/22/04

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19	19	NB (GM) Decoupling	(MASTER)	(MASTER)	
20	20	NB Config Straps	M1	01/05/2006	
21	21	SB: 1 OF 4	M38	01/05/2006	
22	22	SB: 2 OF 4	MASTER	MASTER	
23	23	SB: 3 OF 4	MASTER	MASTER	
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25	25	SB: DECOUPLING	MASTER	MASTER	
26	26	SB: MISC	MASTER	MASTER	
27	27	SB: SMB HUB AND ALIAS	MASTER	MASTER	
28	28	DDR2 SO-DIMM Connector A	MASTER	MASTER	
29	29	DDR2 SO-DIMM Connector B	MASTER	MASTER	
30	30	Memory Active Termination	MASTER	MASTER	
31	31	Memory Vtt Supply	MASTER	MASTER	
32	33	CLOCKS	MASTER	MASTER	
33	34	CLOCKS: TERMINATIONS	MASTER	MASTER	
34	38	Disk Connectors	MASTER	MASTER	
35	41	ETHERNET CONTROLLER	MASTER	MASTER	
36	42	ETHERNET MISC	MASTER	MASTER	
37	43	ETHERNET CONNECTOR	MASTER	MASTER	

PDF	CSA	CONTENTS	SYNC	MASTER	DATE
38	44	FW: FW323-06	MASTER	MASTER	
39	45	FW: DECAPS	MASTER	MASTER	
40	46	FIREWIRE CONNECTORS	MASTER	MASTER	
41	47	USB Device Interfaces	MASTER	MASTER	
42	53	AIRPORT CONN	MASTER	MASTER	
43	54	PCIE PORT ALIASES	MASTER	MASTER	
44	58	SMC	M1	01/05/2006	
45	59	SMC & TPM SUPPORT	(MASTER)	(MASTER)	
46	60	LPC+ CONN	M38	12/09/2005	
47	61	NB THERMAL	MASTER	MASTER	
48	63	SPI BOOTROM	M38	01/05/2006	
49	65	Fan 0, 1 & System Temp	MASTER	MASTER	
50	66	Fan 2 & HD Temp	MASTER	MASTER	
51	67	TPM	M38	01/05/2006	
52	68	AUDIO: CODEC	AUDIO	05/12/2006	
53	72	AUDIO: SPEAKER AMP	AUDIO	05/12/2006	
54	73	AUDIO: CONNECTORS	AUDIO	05/12/2006	
55	74	AUDIO: POWER SUPPLIES	AUDIO	05/12/2006	
56	75	IMVP6 CPU VCore Regulator	MASTER	MASTER	
57	76	CPU & SYSTEM SENSE CIRCUITS	(MASTER)	(MASTER)	
58	77	PWR GOOD	(MASTER)	(MASTER)	
59	78	3V DC/DC 2.5V	(MASTER)	(MASTER)	
60	79	1.8V & 1.2V VREG	MASTER	MASTER	
61	80	1.5V_S0 & 1.05V_S0 VREG	MASTER	MASTER	
62	82	5V DC/DC	MASTER	MASTER	
63	83	S0 AND S3 FETS	MASTER	MASTER	
64	94	Internal Display Conns	MASTER	MASTER	
65	95	EXTERNAL TMDS	MASTER	MASTER	
66	96	TMDS/Inverter/ExtVGA	MASTER	MASTER	
67	97	External Display Conns	MASTER	MASTER	

<p style="font-size: small;">DIMENSIONS ARE IN MILLIMETERS</p> <p>XX : _____</p> <p>X.XX : _____</p> <p>X.XXX : _____</p> <p>ANGLES : _____</p> <p style="text-align: center;">DO NOT SCALE DRAWING</p> <p style="text-align: center;"> <small>THIRD ANGLE PROJECTION</small> </p>	<p>METRIC</p>	<p style="text-align: right; font-weight: bold;">Apple Computer Inc.</p> <p style="font-size: x-small; text-align: center;"> NOTICE OF PROPRIETARY PROPERTY THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING: I. TO MAINTAIN THE DOCUMENT IN CONFIDENCE II. NOT TO REPRODUCE OR COPY IT III. NOT TO REVEAL OR PUBLISH IN WHOLE OR PART </p> <p style="text-align: center; font-weight: bold; font-size: large;">SCHEM VALLCO</p> <p style="text-align: right;">DRAWING NUMBER 051-7032 REV. A</p> <p style="text-align: right; font-size: x-small;">SHT 1 OF 97</p>
DRAFTER _____ ENG APPD _____ QA APPD _____ RELEASE _____	DESIGN CK _____ MFG APPD _____ DESIGNER _____ SCALE _____	TITLE _____ SIZE D MATERIAL/FINISH NOTED AS APPLICABLE



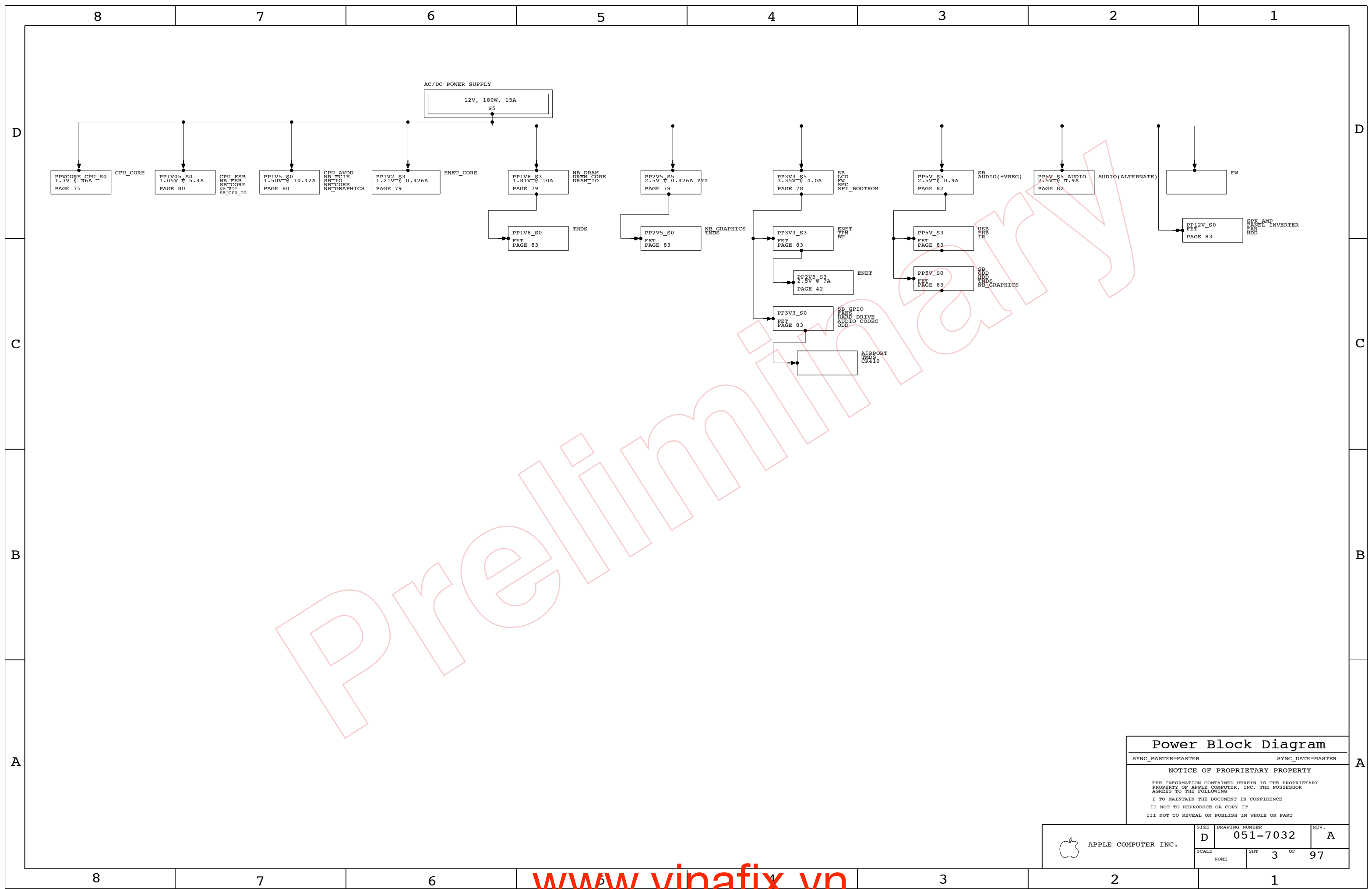
System Block Diagram

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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	D	051-7032	A
SCALE	SHT		OF
NONE	2		97



Preliminary

Power Block Diagram

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COMMON

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
51180025	1	IC,CPU-SKT,479BGA	J0700	CRITICAL	
33880298	1	IC,945GT,NORTHBRIDGE	U1200	CRITICAL	
34380385	1	IC,SB,652BGA	U2100	CRITICAL	
742-0048	1	BAT,COIN,3V,220MAH,CR2032	BT2600	CRITICAL	
35980101	1	IC,CY28445-5,CLK GEN,68PIN QFP	U3301	CRITICAL	
33880270	1	IC,8888053,1GIGABIT ENET XCVR,64P QFN,NO	U4101	CRITICAL	
(33580382) 34181797	1	IC,ENET LAN ROM	U4102	CRITICAL	
33880279	1	IC,FW32306,1394A LINK,TOFP	U4400	CRITICAL	
33880274 34170022	1	IC,SMC,M50	U5800	CRITICAL	
34181789	1	IC,TPM,TSSOP,28P	U6700	CRITICAL	LEMENU
35381465	1	IC,CPU VREG,1MVP,TWO PHASE	U7500	CRITICAL	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-7032	1	PCB,SCHM,MLB,M50	SCH1		
820-1960	1	PCB,FAB,MLB,M50	MLB1		
(33580384) 34170021	1	EFI ROM,M50	U6301	CRITICAL	
33783242	1	M38 CPU (C0)	CPU	CRITICAL	YONAH_1_83

34181859 IC EFI BOOTROM DEV M50
 33783242 M38 CPU(C0)
 33783280 M50 1.83G LOW SPEED CPU (D0)
 USE BOM OPTION MEROM FOR MEROM PROCESSOR

OPS REQUESTED QUAL PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
15580295	1	CHOKE,COMMON_MODE,1650HM,4PIN	L9703	CRITICAL	
124-0359	3	PCAP,120UF,16V,20%,ELEC	C6505,C6504,C6602	CRITICAL	

ALTERNATE PARTS

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
12650091	12650092		C625	FACTORY SHORTAGE
35381278	35381381		U5940	SMC VREF
37880141	37880140		L20601,L20602,L20603	
35381235	35381465		U7500	CPU VREG, NON-SCREENED PART

MECHANICAL PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
603-9187	1	SUBASSY, M50 NB HEATSINK	HS2	CRITICAL	
603-9186	1	SUBASSY, M50 CPU HEATSINK	HS1	CRITICAL	
725-0668	1	MYLAR WASHER	WASH1	CRITICAL	
725-0720	1	MYLAR BLACK LED CVR, M50	CVR1	CRITICAL	
825-6447	1	BARCODE LABEL, M50	[EEE:V3M]	CRITICAL	YONAH_1_83

Table Items

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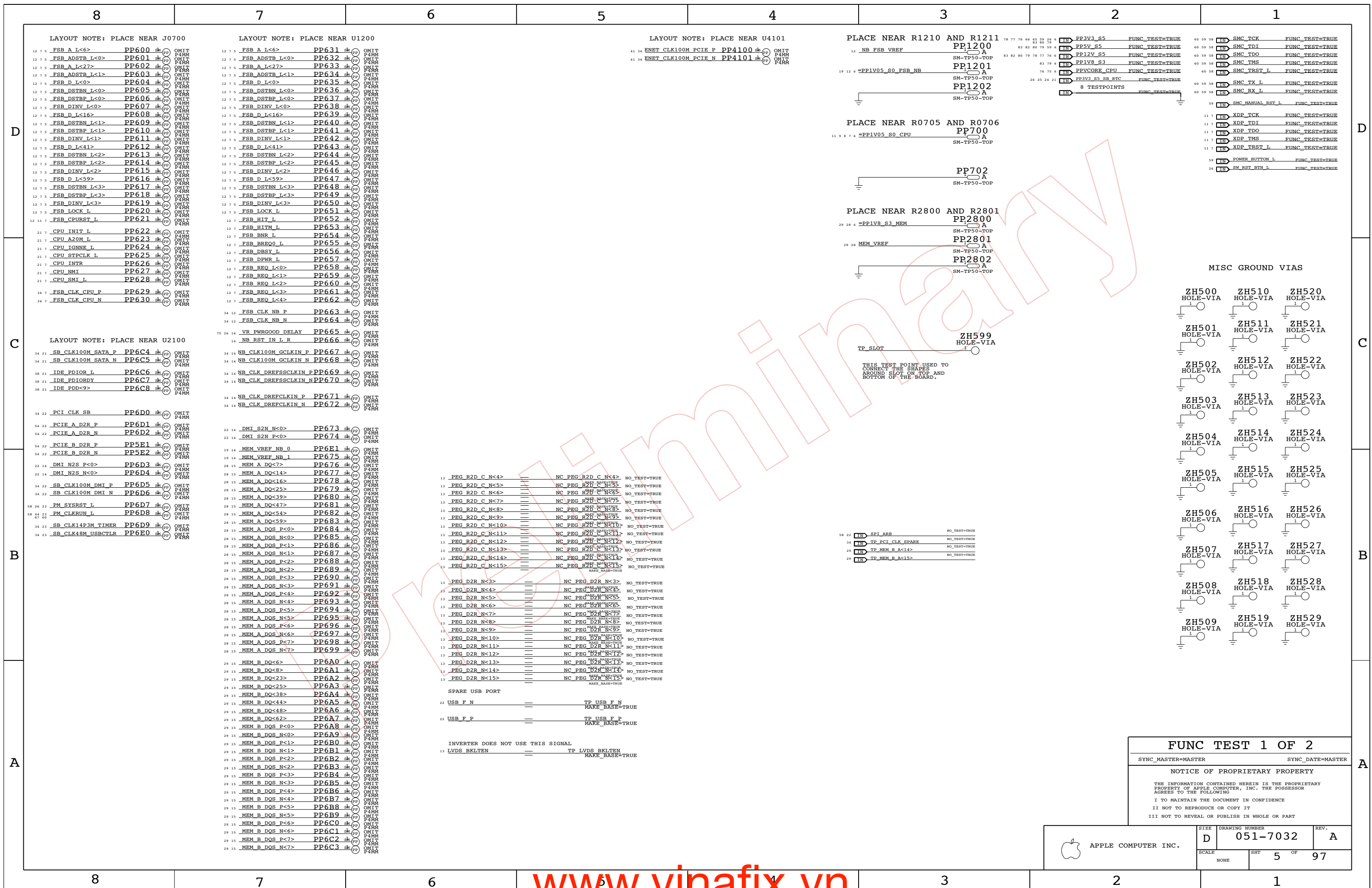
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NONE	4	97



LAYOUT NOTE: PLACE NEAR J0700

LAYOUT NOTE: PLACE NEAR U1200

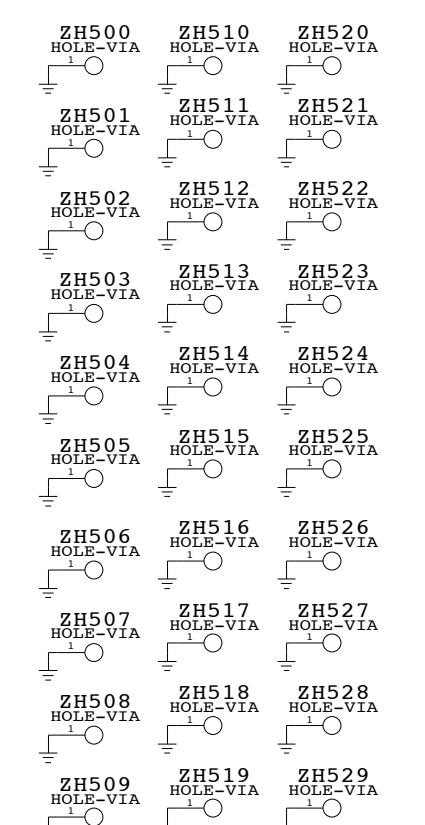
LAYOUT NOTE: PLACE NEAR U4101

PLACE NEAR R1210 AND R1211

PLACE NEAR R0705 AND R0706

PLACE NEAR R2800 AND R2801

MISC GROUND VIAS



THIS TEST POINT USED TO CONNECT THE SHAPES AROUND SLOT ON TOP AND BOTTOM OF THE BOARD.

FUNC TEST 1 OF 2

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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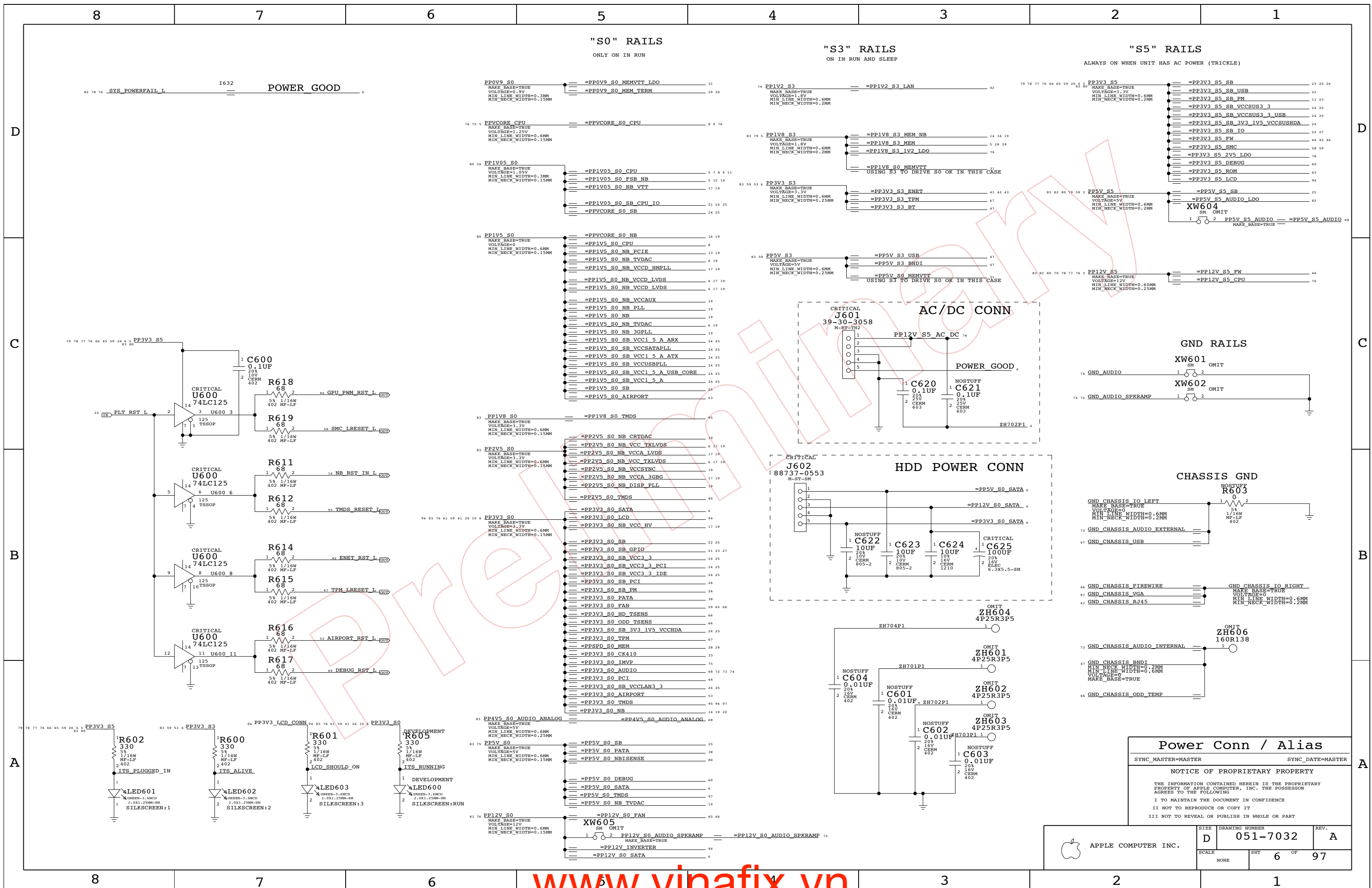
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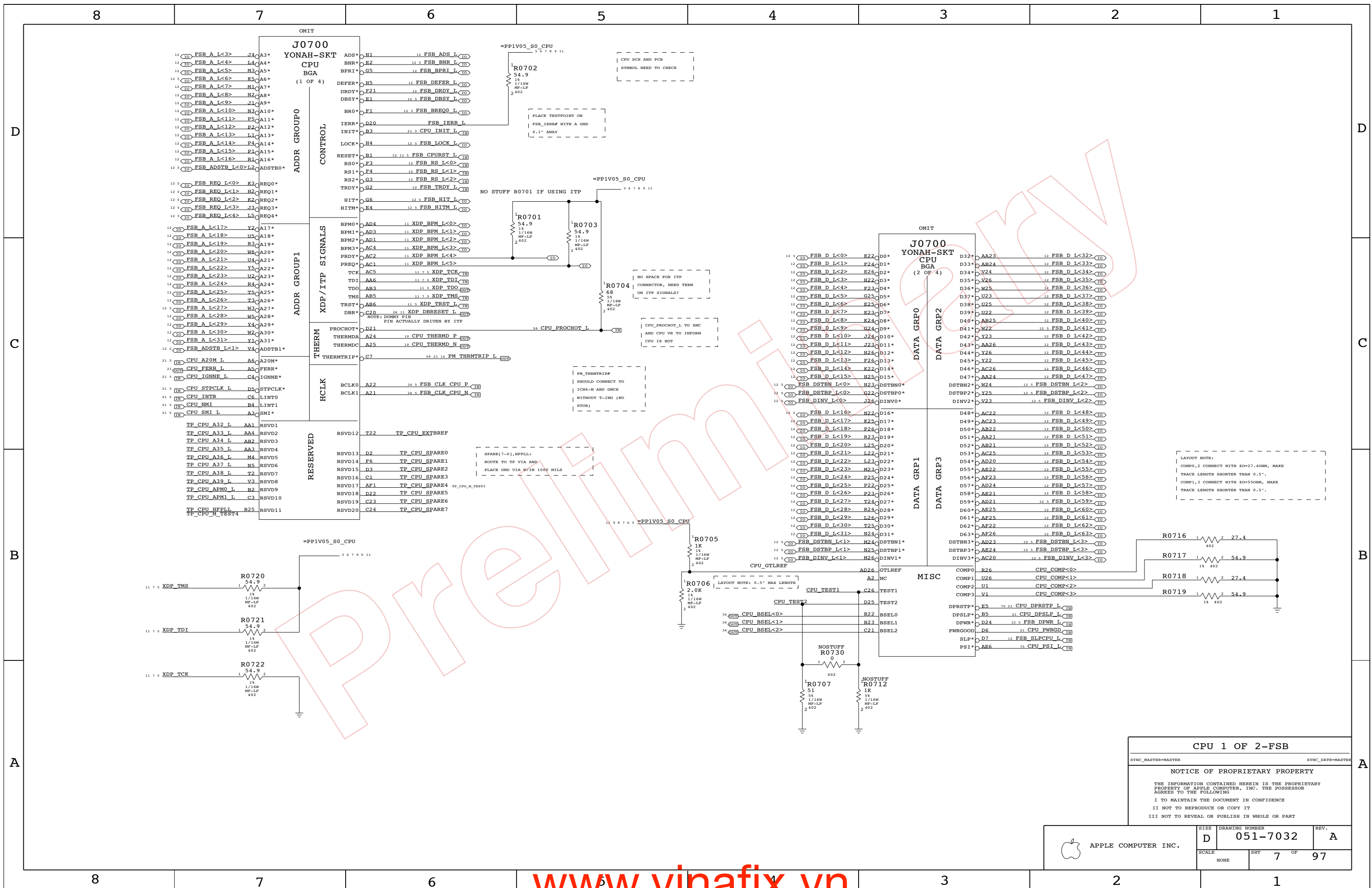
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Power Conn / Alias	
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NONE	6	97	



CPU 1 OF 2-FSB

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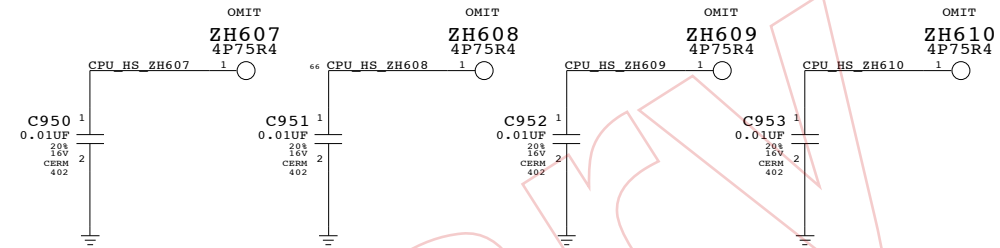
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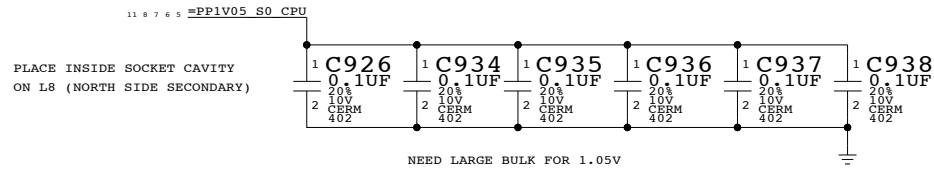
1

CPU HEATSINK MOUNTING HOLES



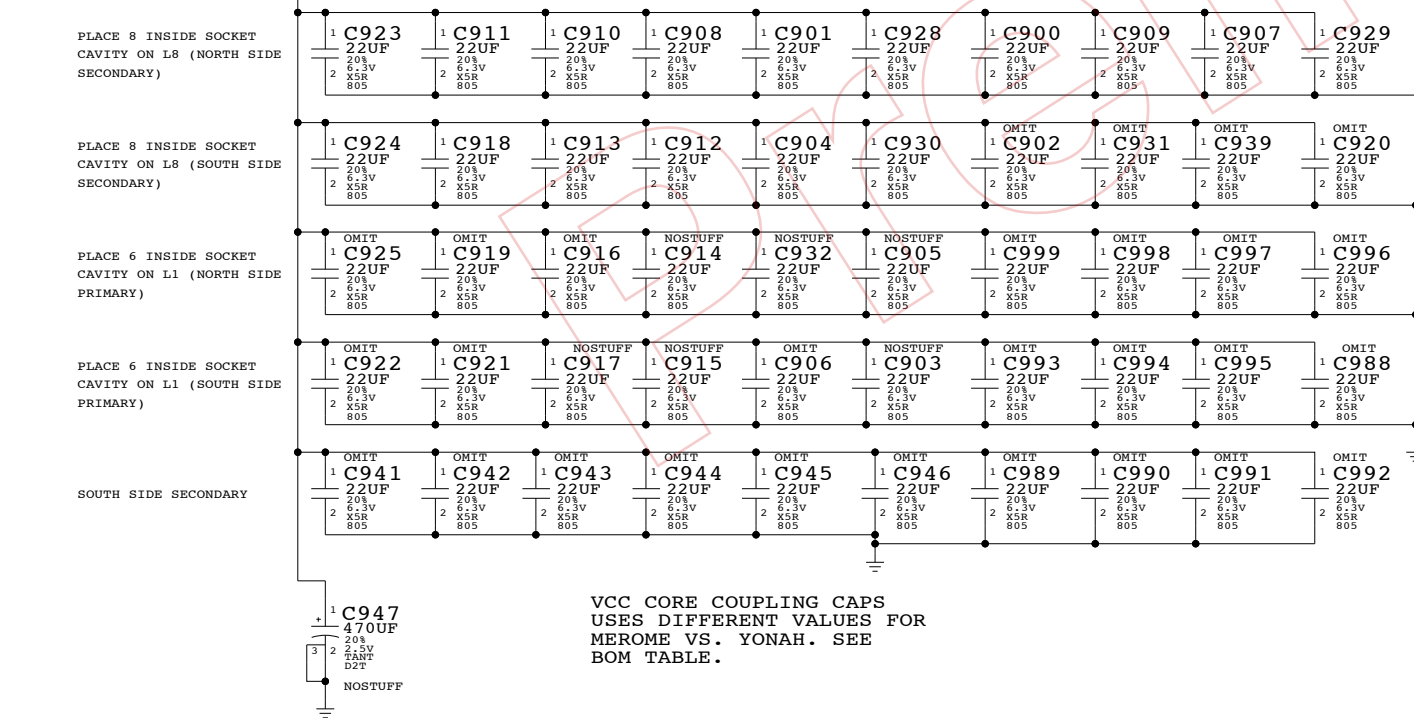
WE HAD A 330UF ELEC CAP HERE FOR 1.05V RAIL - CHECK WE CAN REMOVE

VCCP CORE DECOUPLING



VCC CORE DECOUPLING

DESIGN FOR 44 CERAMIC AND 3 ELECT BULK 1800UF



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
138S0552	28	CAP, 22UF, 6.3V, 20%, X5R, 0805	C922, C925, C906, C939, C919, C993, C942, C991, C995		MEROME C990, C989, C988, C920, C997, C992, C994, C996, C921, C999, C943, C998, C944, C945, C946, C941, C916, C931, C902
138S0558	28	CAP, 10UF, 6.3V, 20%, X5R, 0805	C922, C925, C906, C939, C919, C993, C942, C991, C995		YONAH C990, C989, C988, C920, C997, C992, C994, C996, C921, C999, C943, C998, C944, C945, C946, C941, C916, C931, C902

CPU DECAPS & VID<>

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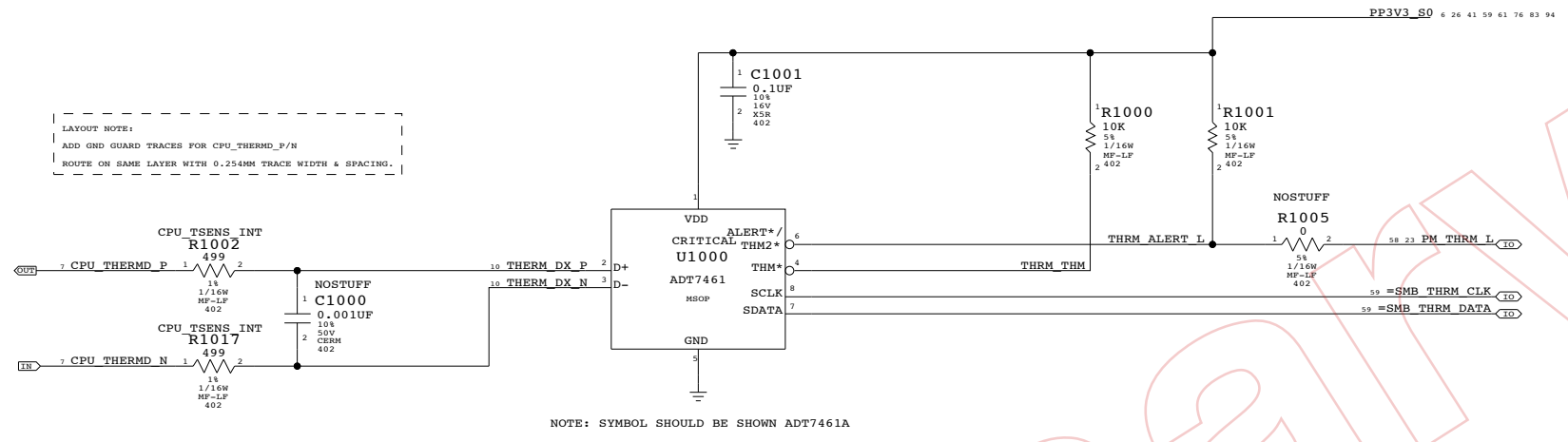
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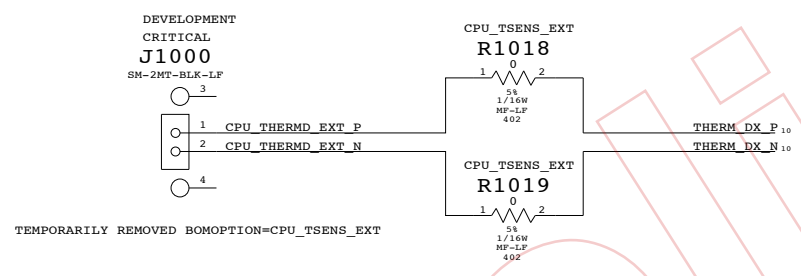
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	A
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NONE			

CPU THERMAL SENSOR

NOTE:
IF CPU T DIODE TO BE READ IN OFF STATE,
THEN THIS SHOULD BE S5



LAYOUT NOTE:
PLACE R1002 AND R1018 SUCH THAT THEY SHARE ONE PAD
PLACE R1017 AND R1019 SUCH THAT THEY SHARE ONE PAD



CPU TEMP SENSOR

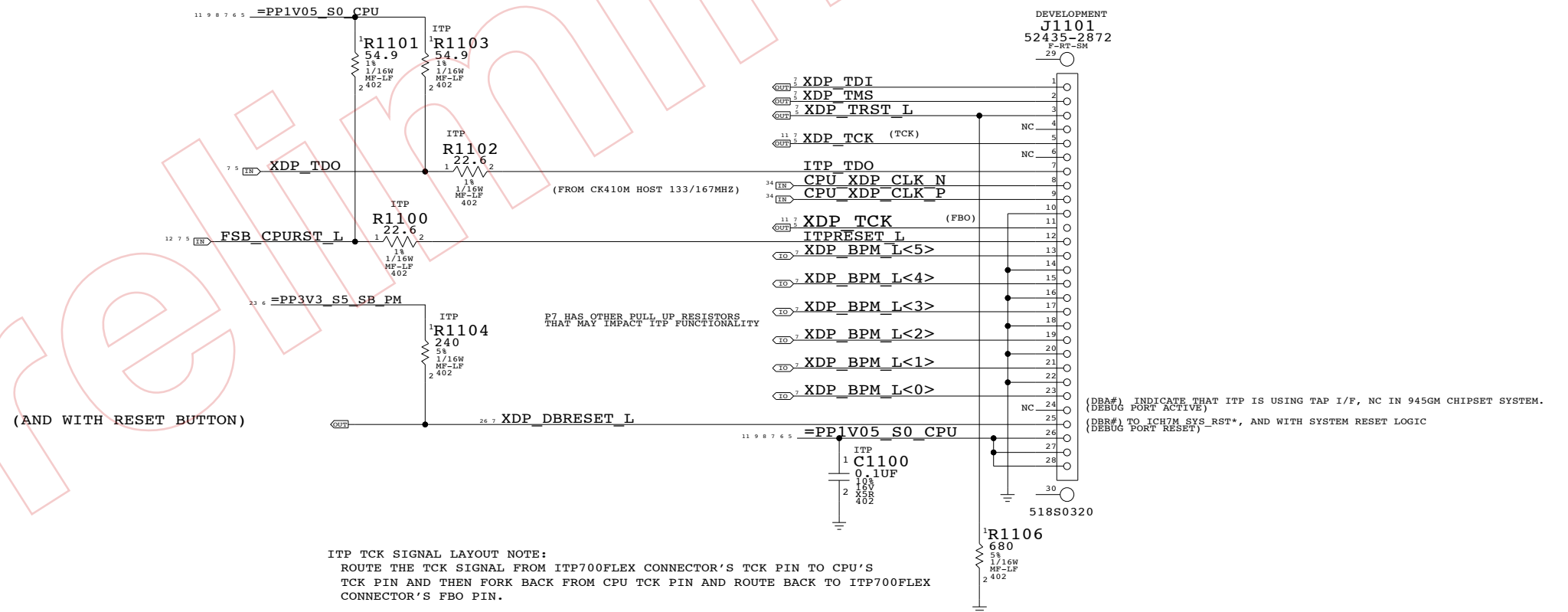
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NONE			

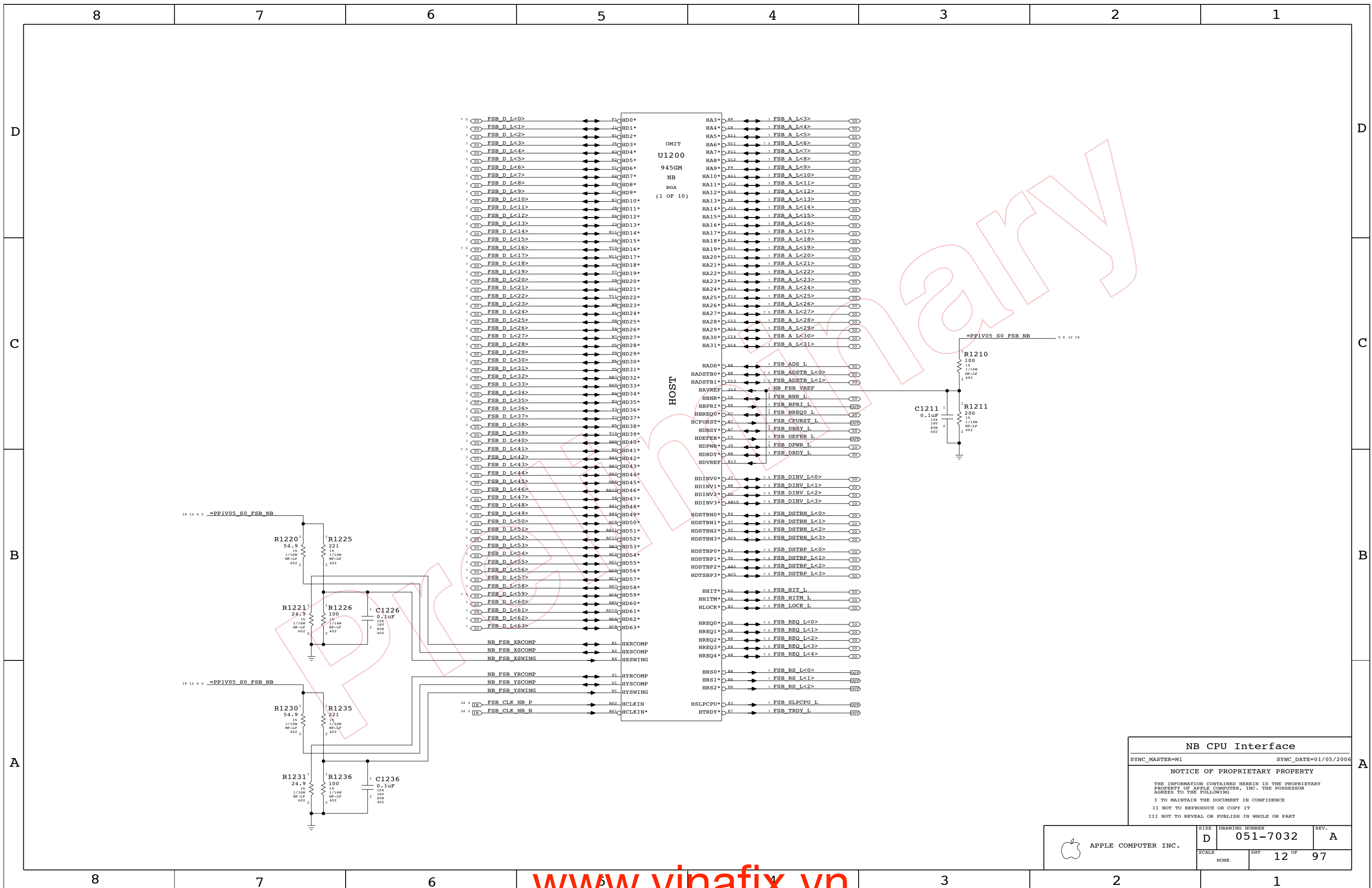
CPU ITP700FLEX DEBUG SUPPORT



CPU ITP700FLEX DEBUG
 SYNC_MASTER=M38 SYNC_DATE=01/05/2006

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NONE			



NB CPU Interface

SYNC_MASTER=M1 SYNC_DATE=01/05/2006

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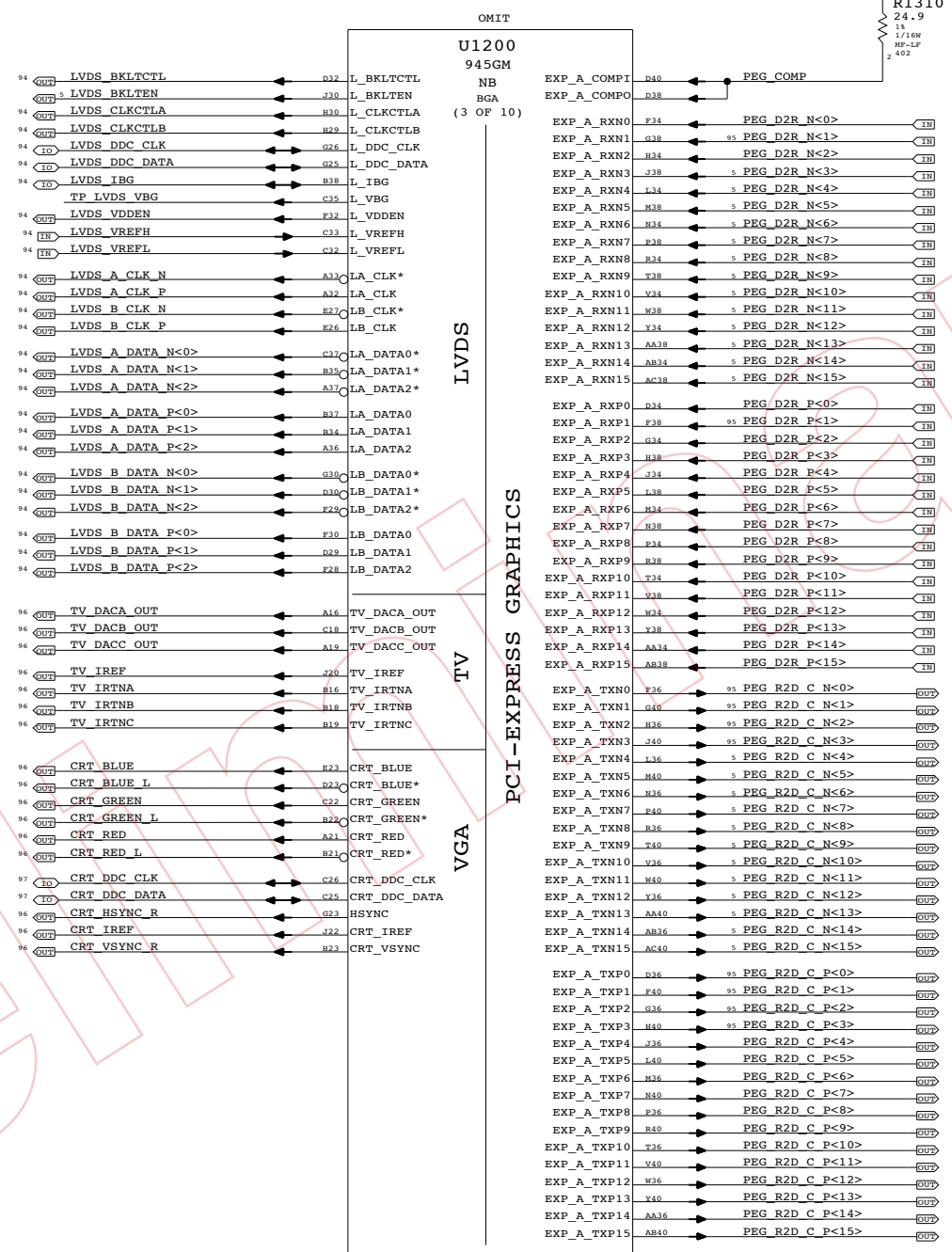
LVDS Disable
 Can leave all signals NC if LVDS is not implemented
 Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
 VCCD_LVDS must remain powered with proper decoupling.
 Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:
 Composite: DACA only
 S-Video: DACB & DACC only
 Component: DACA, DACB & DACC

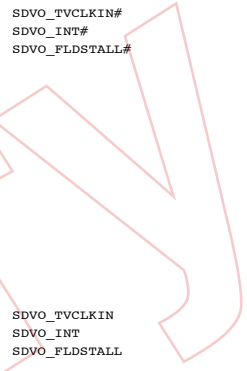
Unused DAC outputs must remain powered, but can omit
 filtering components. Unused DAC outputs should
 connect to GND through 75-ohm resistors.

TV-Out Disable
 Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail.
 Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and
 VCCA_TVVBG to 1.5V power rail. Tie VSSA_TVVBG to GND.

CRT Disable
 Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie
 HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core
 rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.



SDVO Alternate Function



SDVO_TVCLKIN
 SDVO_INT
 SDVO_FLDSTALL

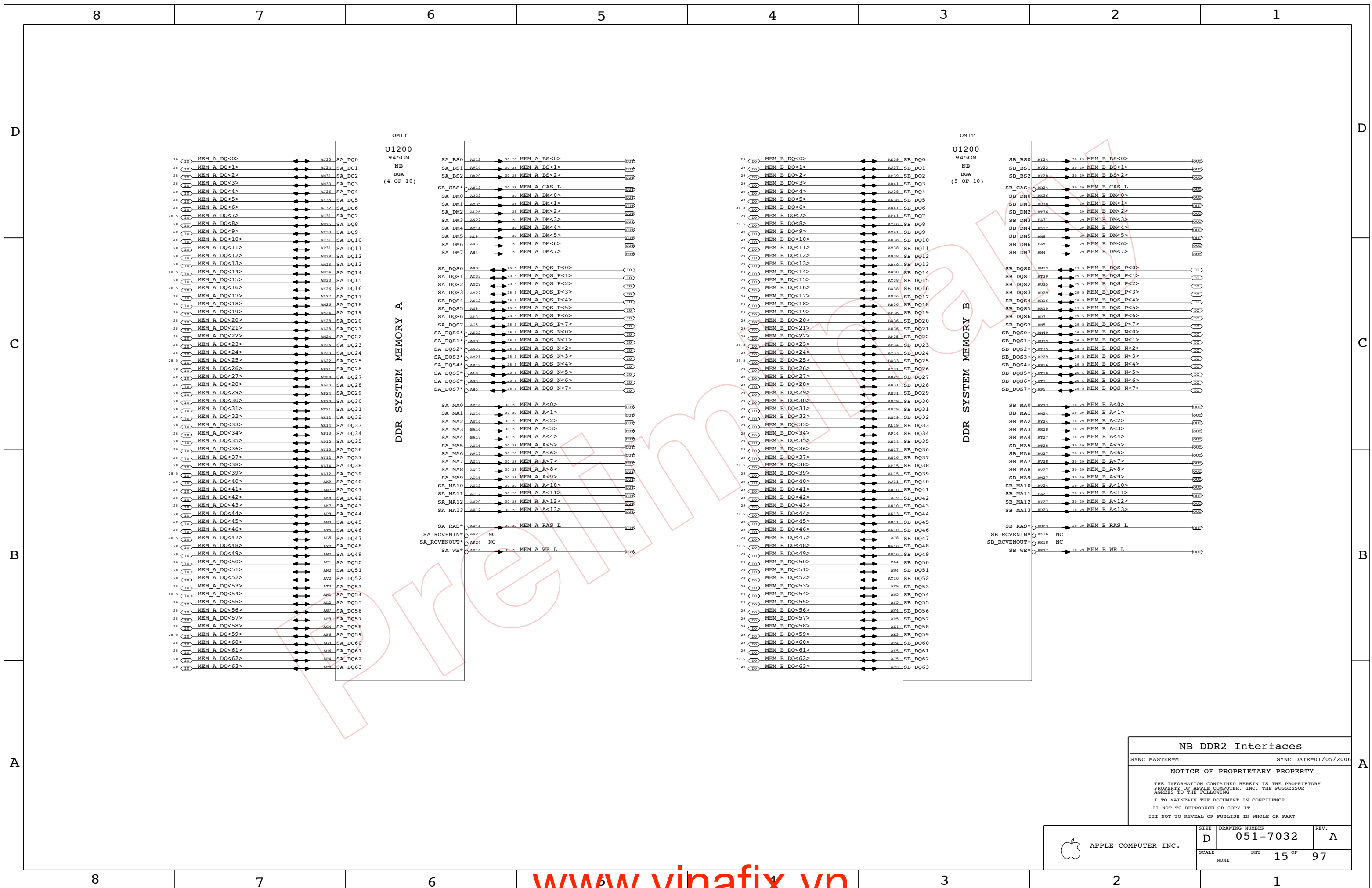
SDVOB_RED#
 SDVOB_GREEN#
 SDVOB_BLUE#
 SDVOB_CLKN
 SDVOC_RED#
 SDVOC_GREEN#
 SDVOC_BLUE#
 SDVOC_CLKN

SDVOB_RED
 SDVOB_GREEN
 SDVOB_BLUE
 SDVOB_CLKP
 SDVOC_RED
 SDVOC_GREEN
 SDVOC_BLUE
 SDVOC_CLKP

Preview

NB PEG / Video Interfaces
 SYNC_MASTER=M1 SYNC_DATE=01/05/2006
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NONE			



NB DDR2 Interfaces

SYNC_MASTER=M1 SYNC_DATE=01/05/2006

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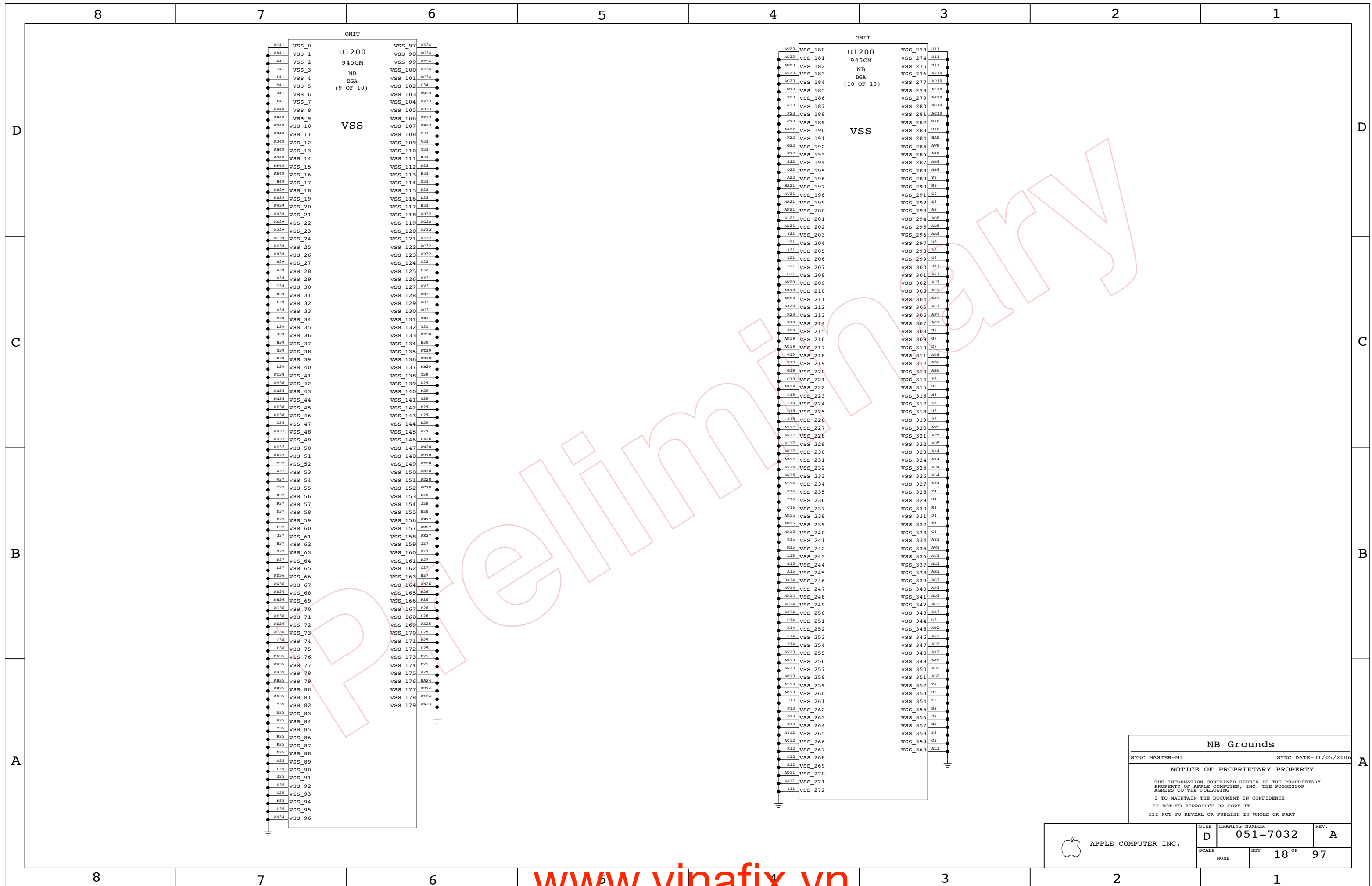
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NONE			



NB Grounds

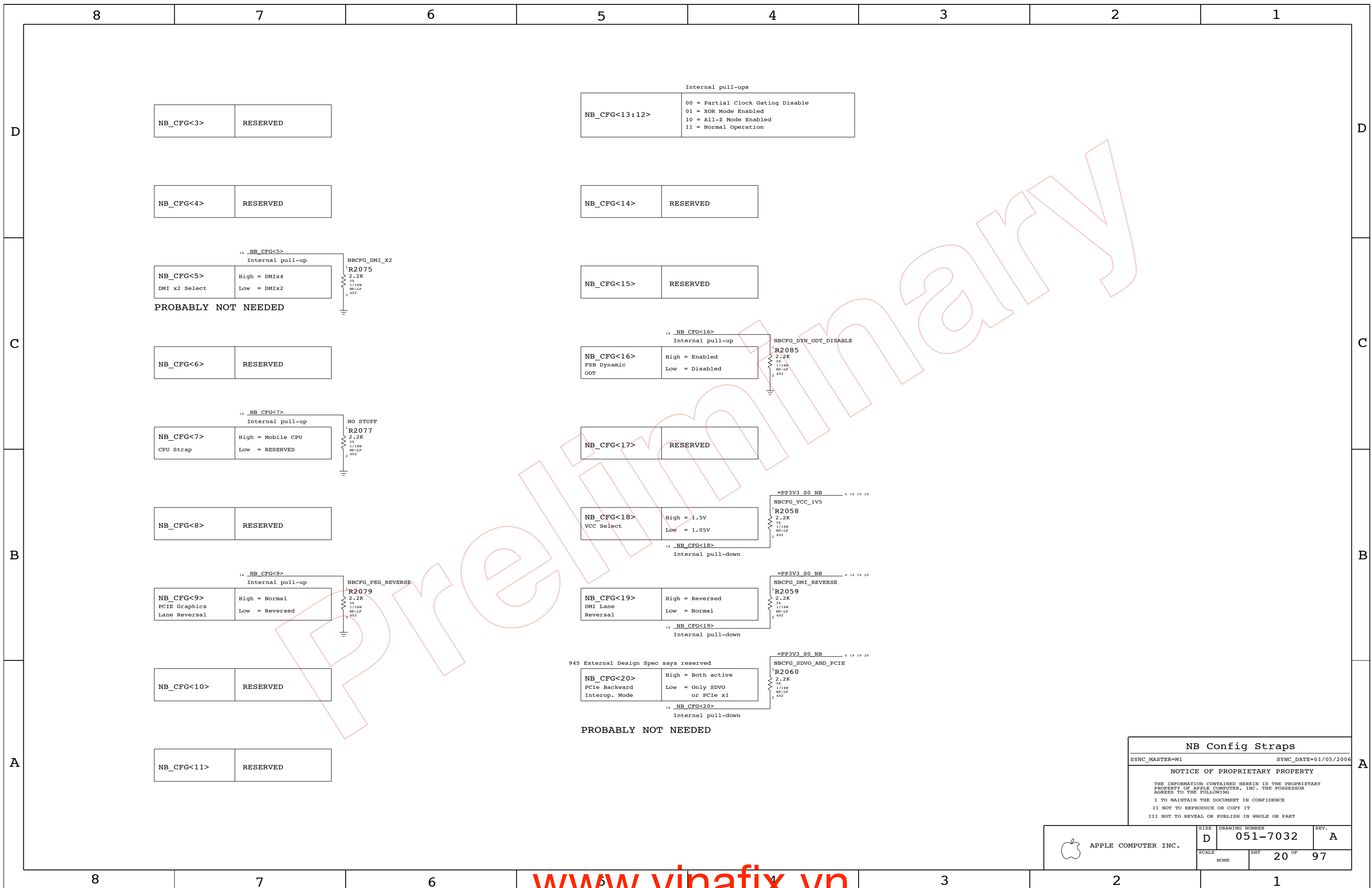
SYNC_MASTER=M1 SYNC_DATE=01/05/2006

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Internal pull-ups

NB_CFG<13:12>	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal Operation
---------------	--

NB_CFG<3>	RESERVED
-----------	----------

NB_CFG<14>	RESERVED
------------	----------

NB_CFG<4>	RESERVED
-----------	----------

14 NB_CFG<5>
Internal pull-up

NB_CFG<5>	High = DMIX4 DMI x2 Select Low = DMIX2
-----------	--

PROBABLY NOT NEEDED

NBCFG_DMI_X2
R2075
2.2K
5%
1/16W
MF-LF
2 402

NB_CFG<15>	RESERVED
------------	----------

NB_CFG<6>	RESERVED
-----------	----------

14 NB_CFG<16>
Internal pull-up

NB_CFG<16>	High = Enabled FSB Dynamic ODT Low = Disabled
------------	--

NBCFG_DYN_ODT_DISABLE
R2085
2.2K
5%
1/16W
MF-LF
2 402

14 NB_CFG<7>
Internal pull-up

NB_CFG<7>	High = Mobile CPU CPU Strap Low = RESERVED
-----------	--

NO STUFF
R2077
2.2K
5%
1/16W
MF-LF
2 402

NB_CFG<17>	RESERVED
------------	----------

NB_CFG<8>	RESERVED
-----------	----------

=PP3V3 S0 NB 6 14 19 20

NB_CFG<18>	High = 1.5V VCC Select Low = 1.05V
------------	--

NBCFG_VCC_1V5
R2058
2.2K
5%
1/16W
MF-LF
2 402

14 NB_CFG<18>
Internal pull-down

14 NB_CFG<9>
Internal pull-up

NB_CFG<9>	High = Normal PCIe Graphics Lane Reversal Low = Reversed
-----------	---

NBCFG_PEG_REVERSE
R2079
2.2K
5%
1/16W
MF-LF
2 402

=PP3V3 S0 NB 6 14 19 20

NB_CFG<19>	High = Reversed DMI Lane Reversal Low = Normal
------------	---

NBCFG_DMI_REVERSE
R2059
2.2K
5%
1/16W
MF-LF
2 402

14 NB_CFG<19>
Internal pull-down

NB_CFG<10>	RESERVED
------------	----------

945 External Design Spec says reserved

NB_CFG<20>	High = Both active PCIe Backward Interop. Mode Low = Only SDVO or PCIe x1
------------	---

NBCFG_SDVO_AND_PCIE
R2060
2.2K
5%
1/16W
MF-LF
2 402

14 NB_CFG<20>
Internal pull-down

PROBABLY NOT NEEDED

NB_CFG<11>	RESERVED
------------	----------

NB Config Straps

SYNC_MASTER=M1 SYNC_DATE=01/05/2006

NOTICE OF PROPRIETARY PROPERTY

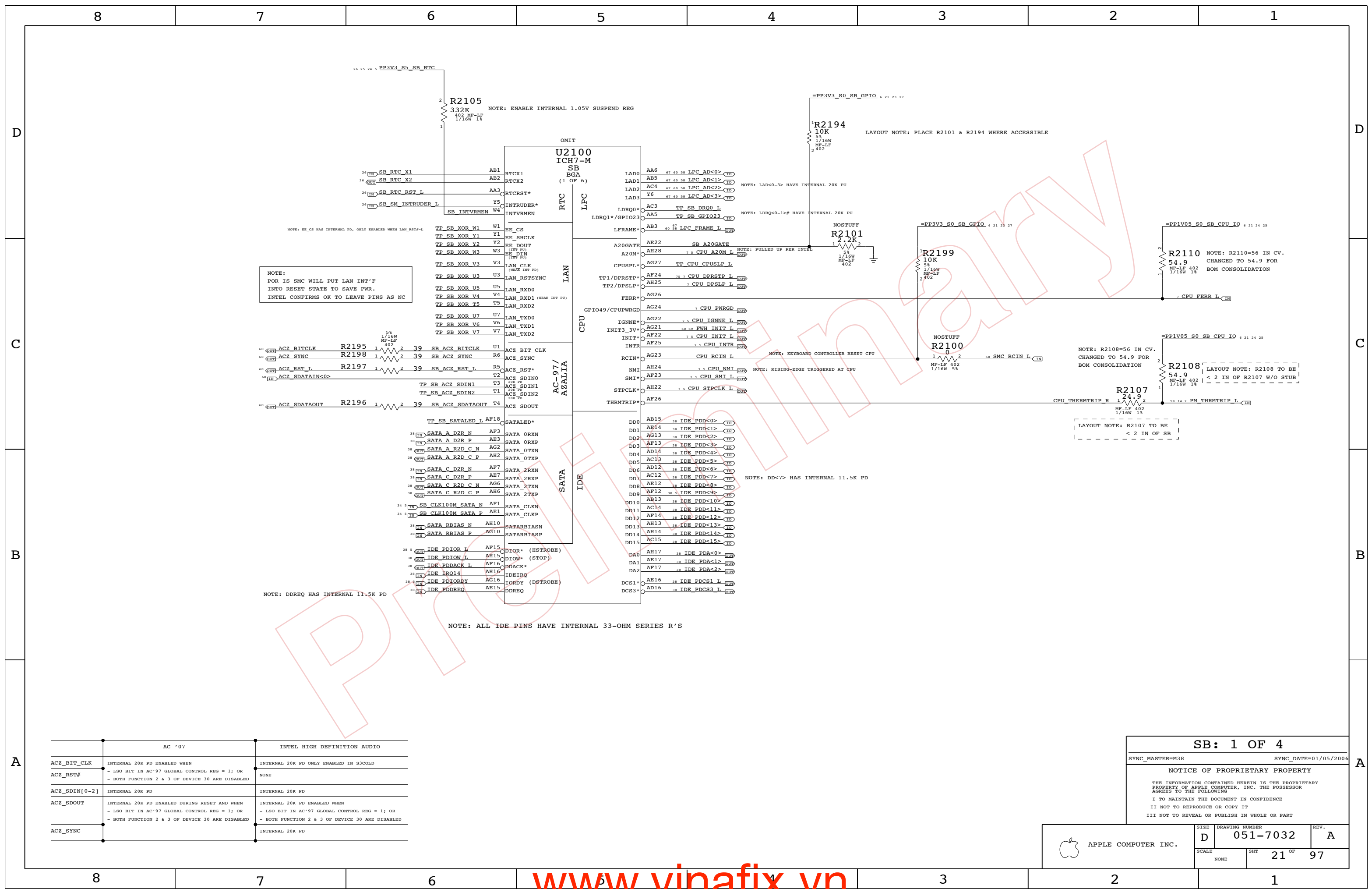
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	D	051-7032	A
SCALE	SHT	20 OF	97
NONE			



NOTE:
 POR IS SMC WILL PUT LAN INT'F
 INTO RESET STATE TO SAVE PWR.
 INTEL CONFIRMS OK TO LEAVE PINS AS NC

NOTE: DDREQ HAS INTERNAL 11.5K PD

NOTE: ALL IDE PINS HAVE INTERNAL 33-OHM SERIES R'S

	AC '07	INTEL HIGH DEFINITION AUDIO
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR	INTERNAL 20K PD ONLY ENABLED IN S3COLD
ACZ_RST#	NONE - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	NONE
ACZ_SDIN[0-2]	INTERNAL 20K PD	INTERNAL 20K PD
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
ACZ_SYNC	INTERNAL 20K PD	INTERNAL 20K PD

SB: 1 OF 4

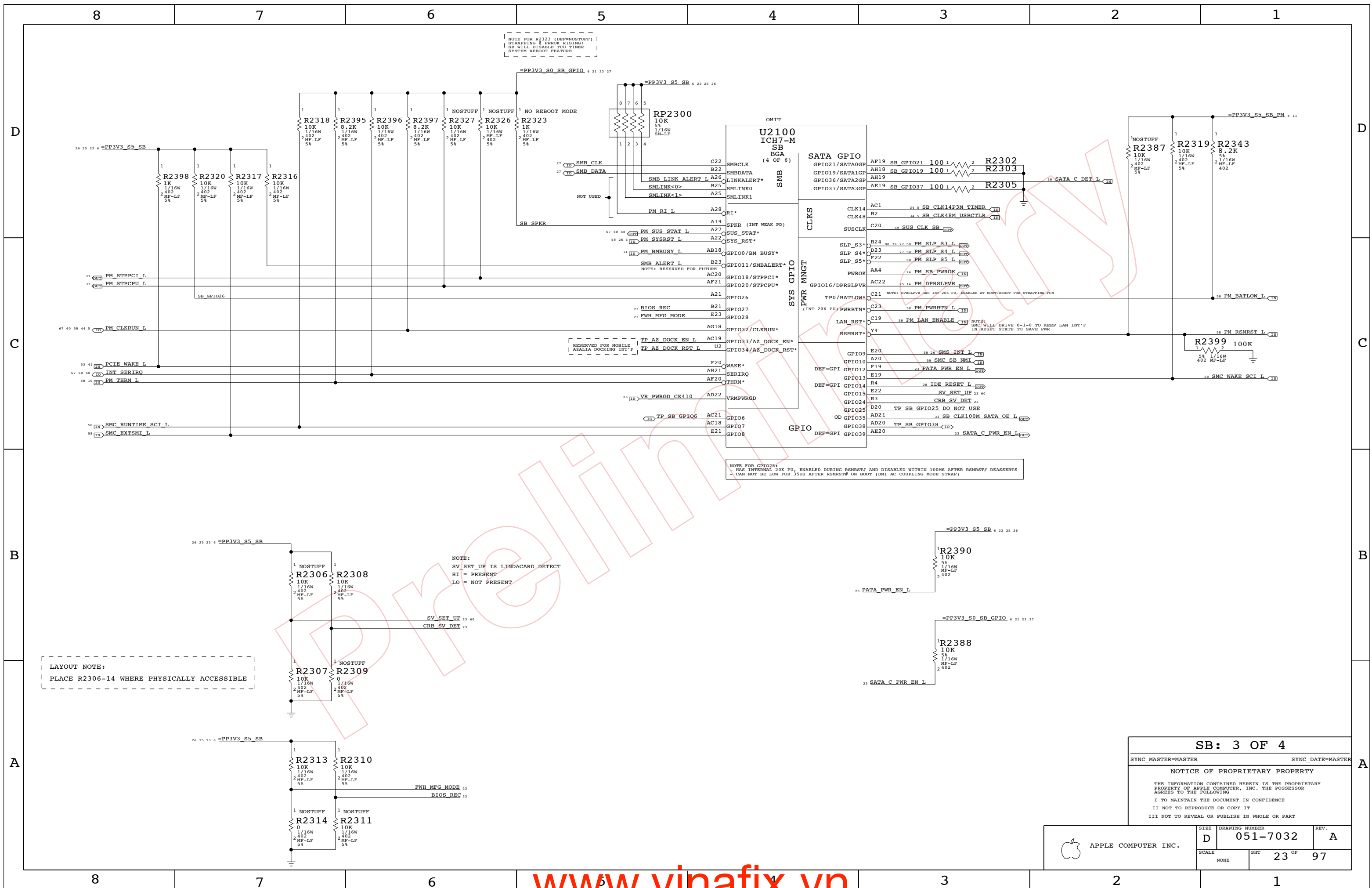
SYNC_MASTER=M38 SYNC_DATE=01/05/2006

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	D	051-7032	A
SCALE	SHT		REV.
NONE	21 OF 97		



NOTE FOR R2323 (DEF=NOSTUFF) | STRAPPING & PWROK RISING: SB WILL DISABLE TOO TIMER SYSTEM REBOOT FEATURE

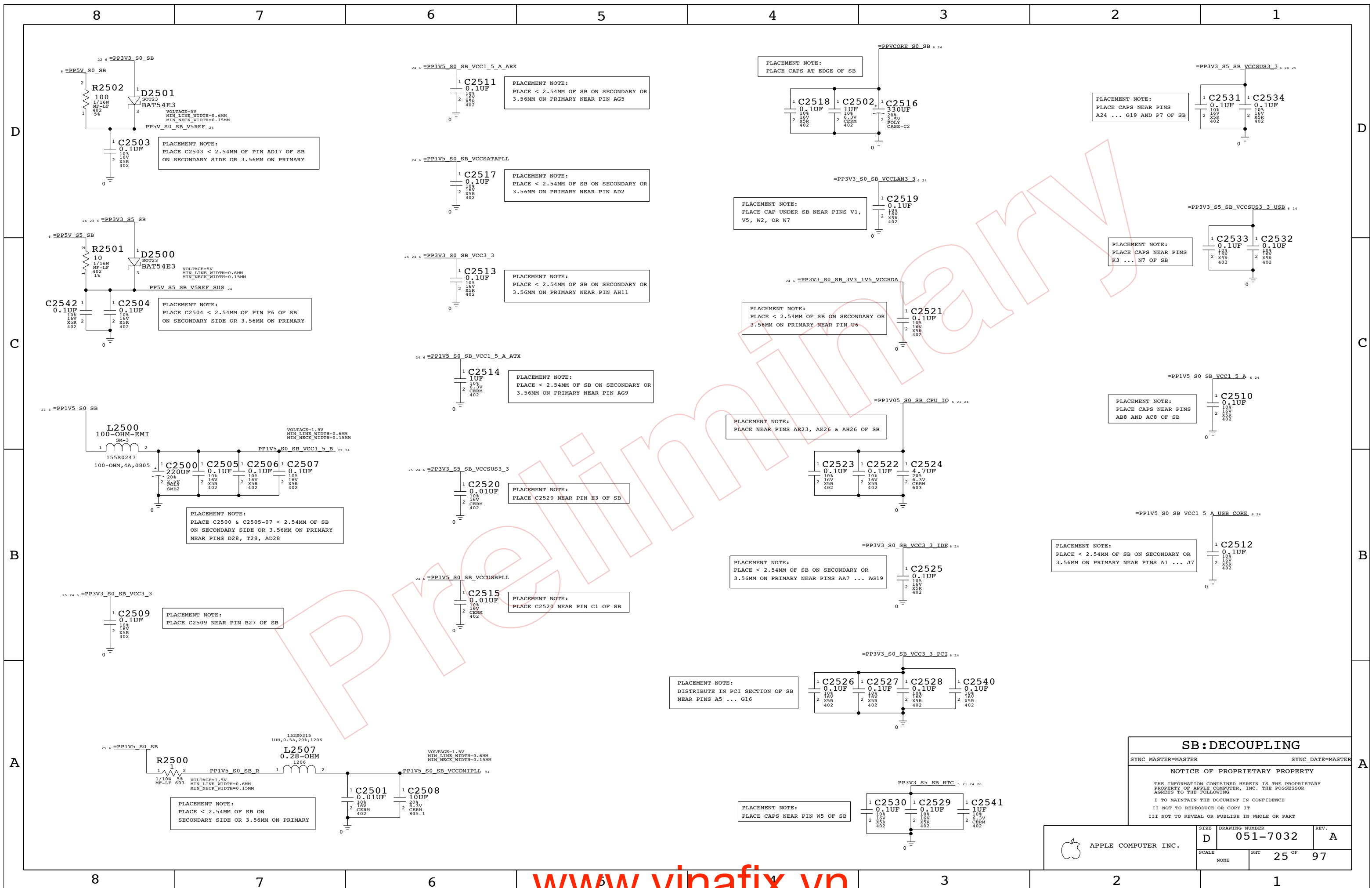
NOTE FOR GPIO25:
 * HAS INTERNAL 20K PU, ENABLED DURING RSMRST# AND DISABLED WITHIN 100MS AFTER RSMRST# DEASSERTS
 * CAN NOT BE LOW FOR 35US AFTER RSMRST# ON BOOT (DMI AC COUPLING MODE STRAP)

LAYOUT NOTE:
 PLACE R2306-14 WHERE PHYSICALLY ACCESSIBLE

NOTE:
 SV_SET_UP IS LINDACARD DETECT
 HI = PRESENT
 LO = NOT PRESENT

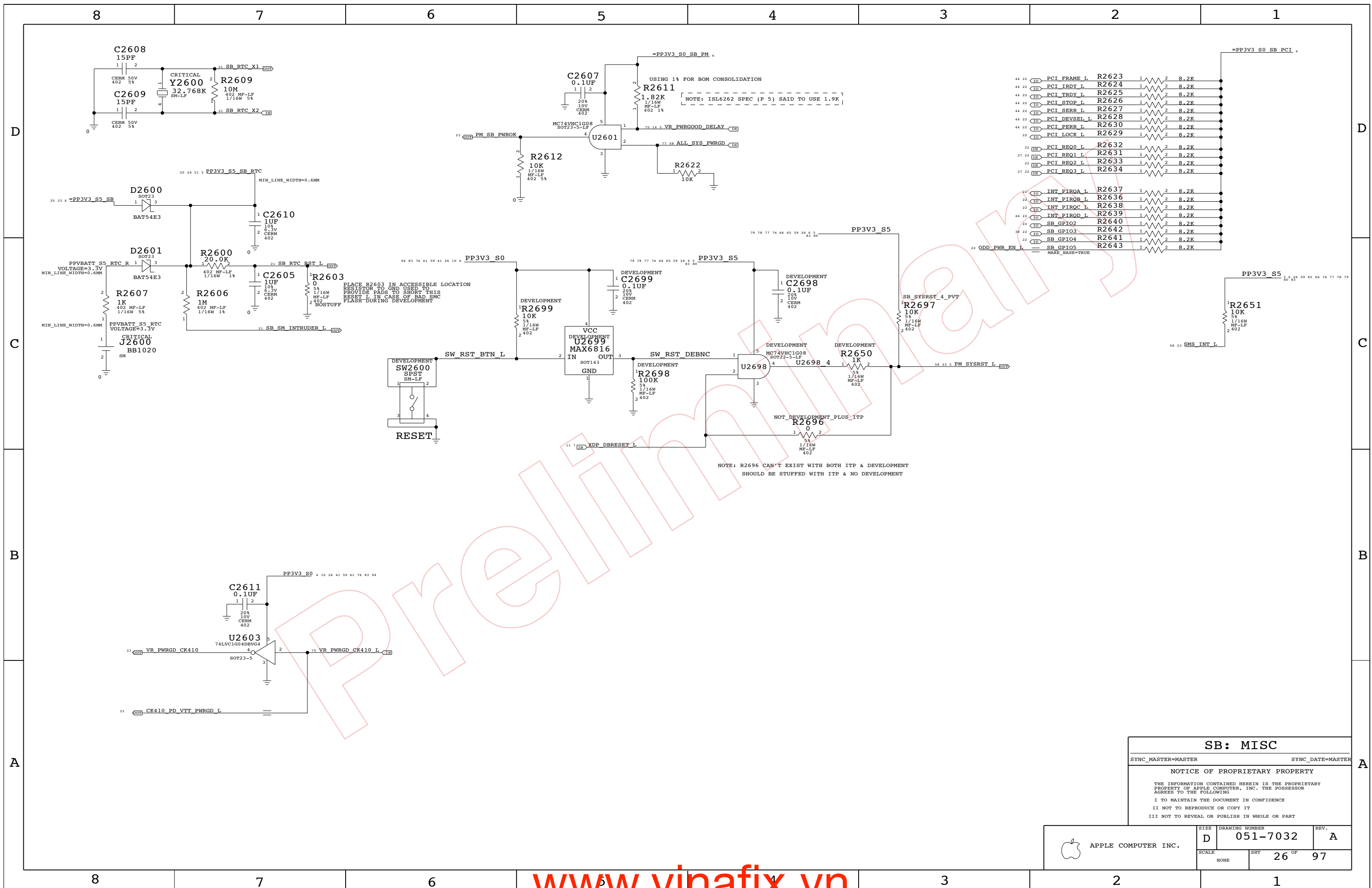
SB: 3 OF 4
 SYNC_MASTER=MASTER SYNC_DATE=MASTER
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	D	051-7032	A
SCALE	SHT		23 OF 97
NONE			



SB: DECOUPLING
 SYNC_MASTER=MASTER SYNC_DATE=MASTER
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	A
SCALE	SHT	25 OF 97	
NONE			



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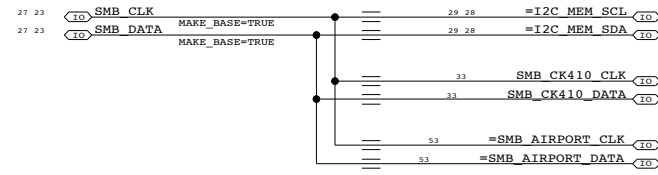
2

1

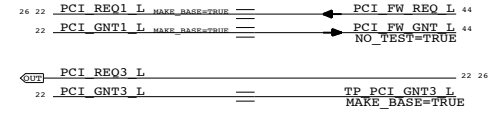
D

D

SB I2C BUSSES

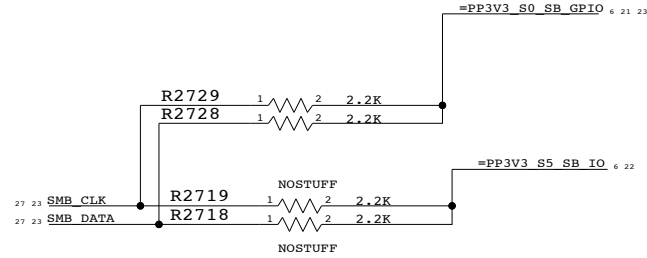


PCI CONTROL



C

C



B

B

A

A

Preliminary

SB: SMB HUB AND ALIAS

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	A
SCALE	SHT		OF
NONE	27		97

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Page Notes

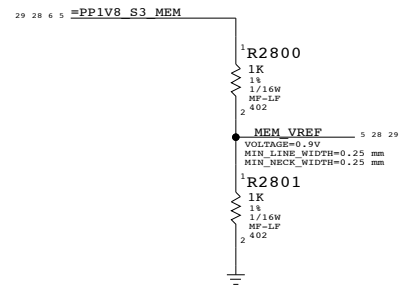
Power aliases required by this page:
 - =PP1V8_S3_MEM
 - =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
 - =I2C_MEM_SCL
 - =I2C_MEM_SDA

BOM options provided by this page:
 (NONE)

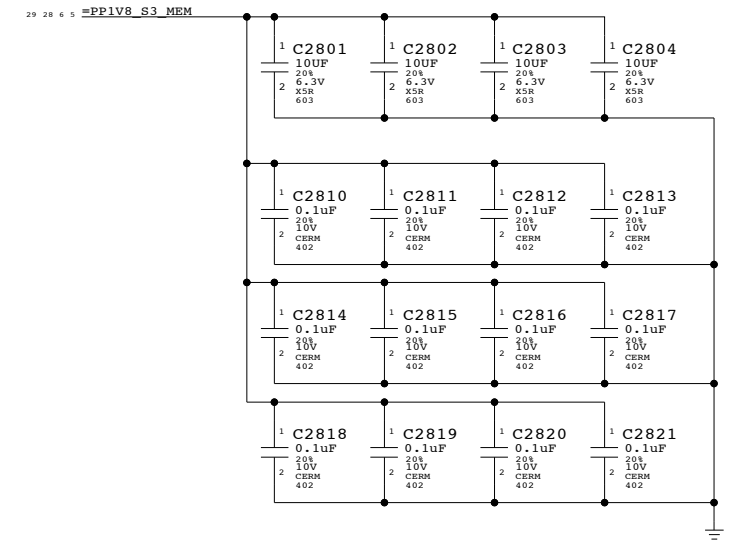
DDR2 VRef

One 0.1uF per connector



DDR2 Bypass Caps

(For return current)



DDR2 SO-DIMM Connector A

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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	D	051-7032	A
SCALE	SHT	28 OF 97	
NONE			

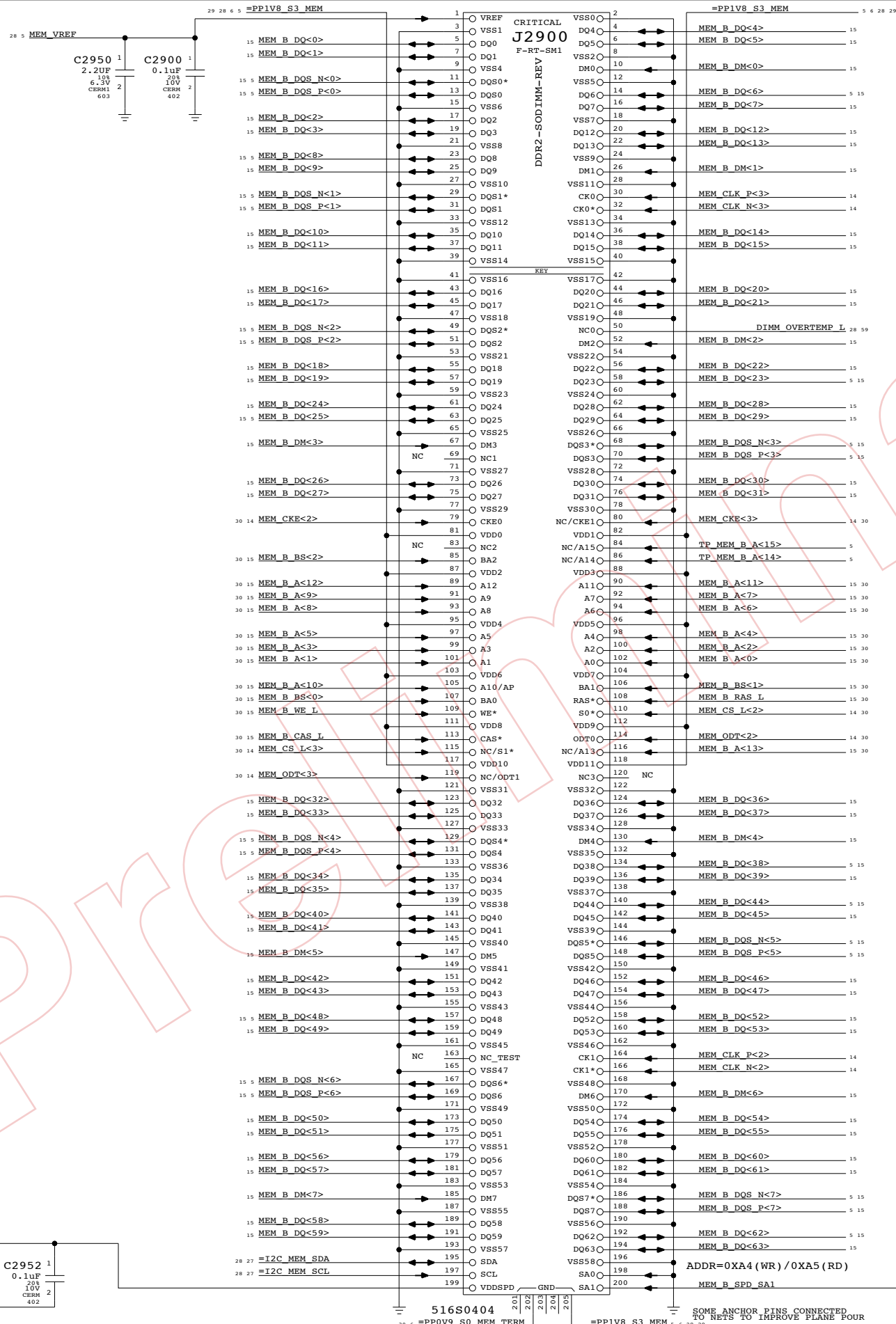
Page Notes

Power aliases required by this page:
 - =PP1V8_S3_MEM
 - =PPSPD_S0_MEM (2.5V - 3.3V)

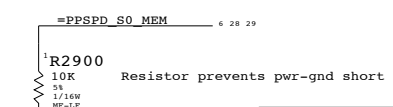
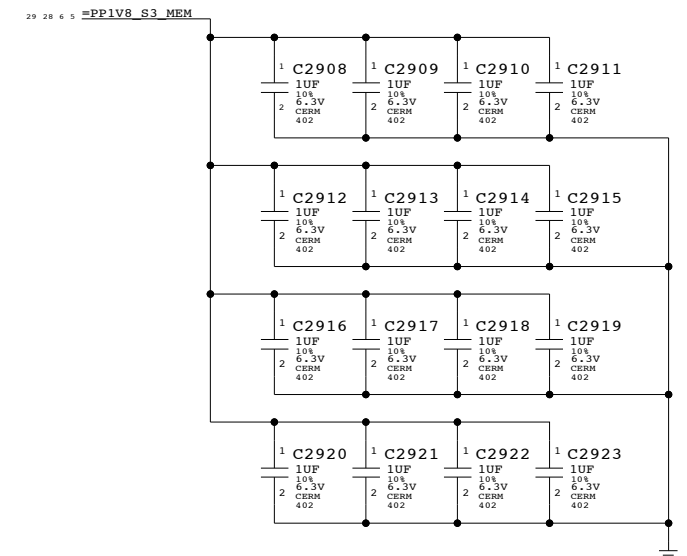
Signal aliases required by this page:
 - =I2C_MEM_SCL
 - =I2C_MEM_SDA

BOM options provided by this page:
 (NONE)

NOTE: This page does not supply VREF.
 The reference voltage must be provided by another page.



DDR2 Bypass Caps (For return current)



DDR2 SO-DIMM Connector B

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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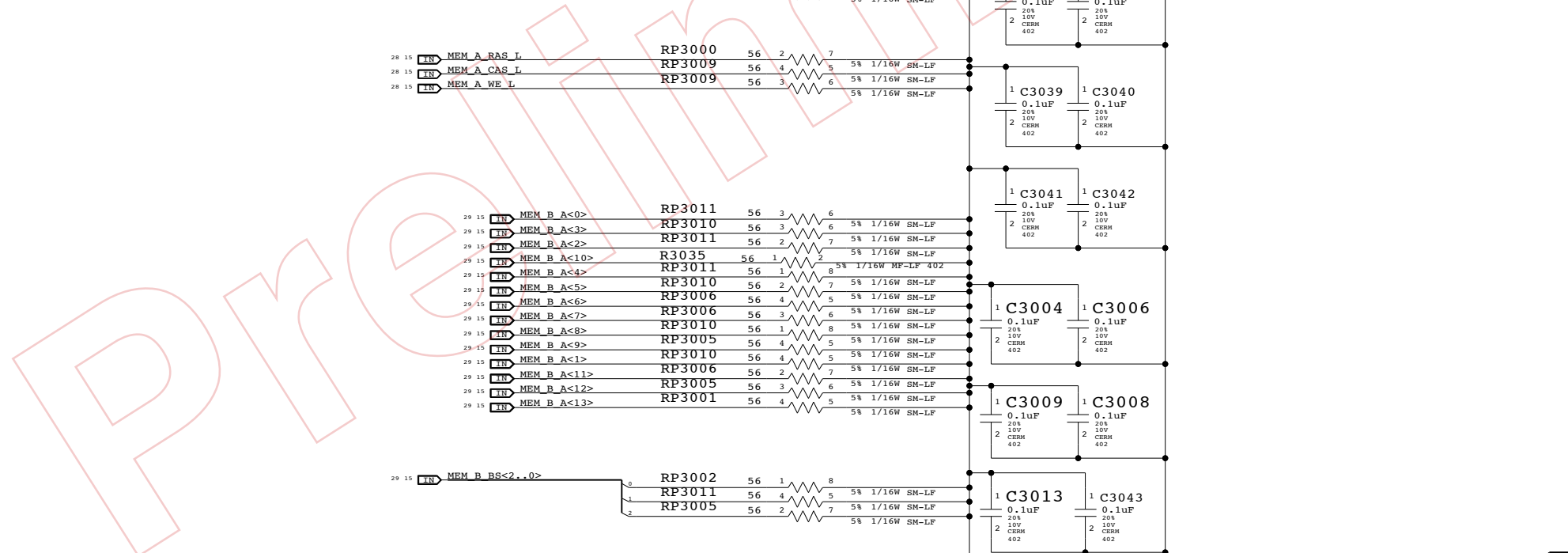
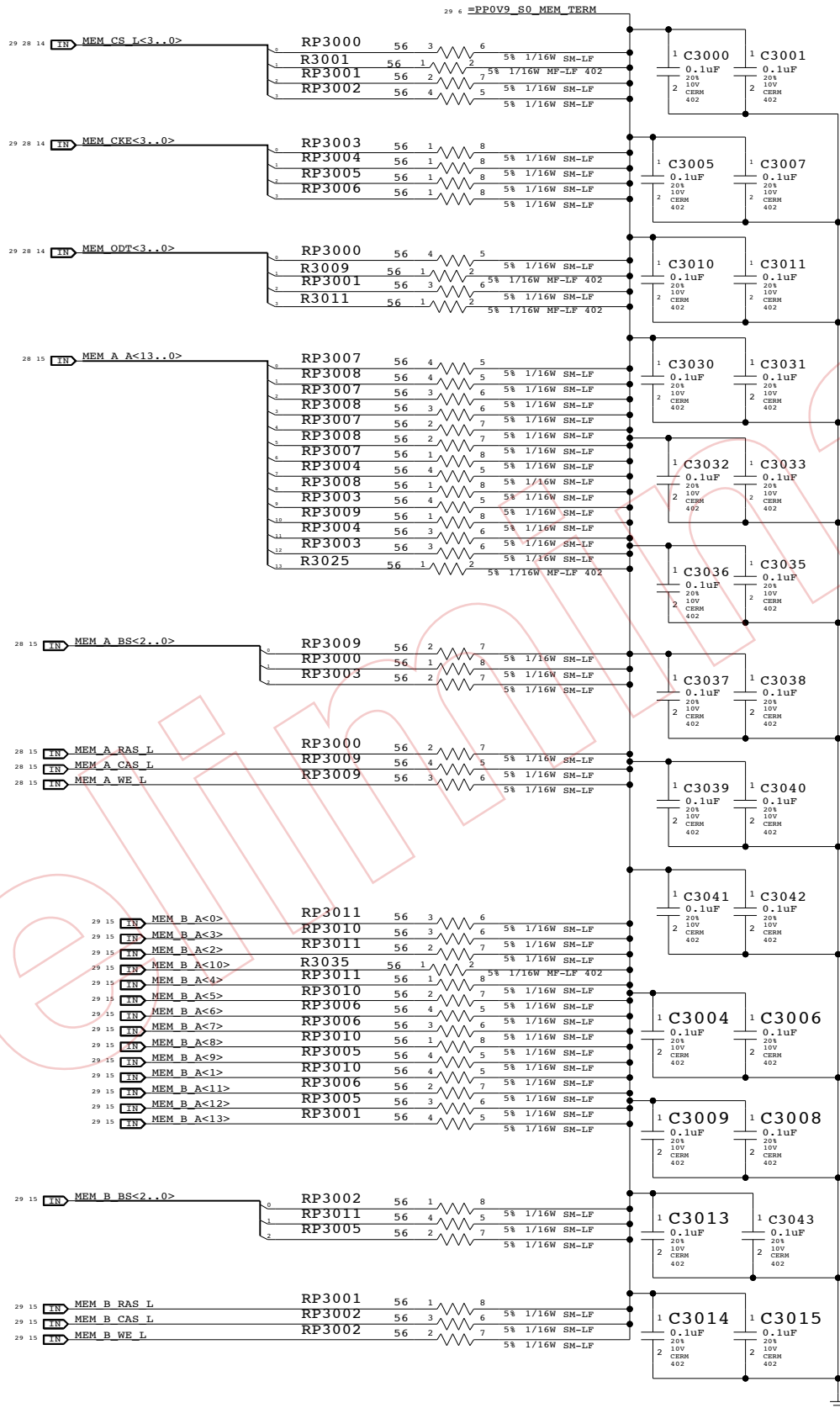
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	A
SCALE	SHT	29 OF	97
NONE			

One cap for each side of every RPAK, one cap for every two discrete resistors
BOMOPTION shown at the top of each group applies to every part below it



Memory Active Termination

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7032	REV. A
	SCALE NONE	SHT 30 OF 97	

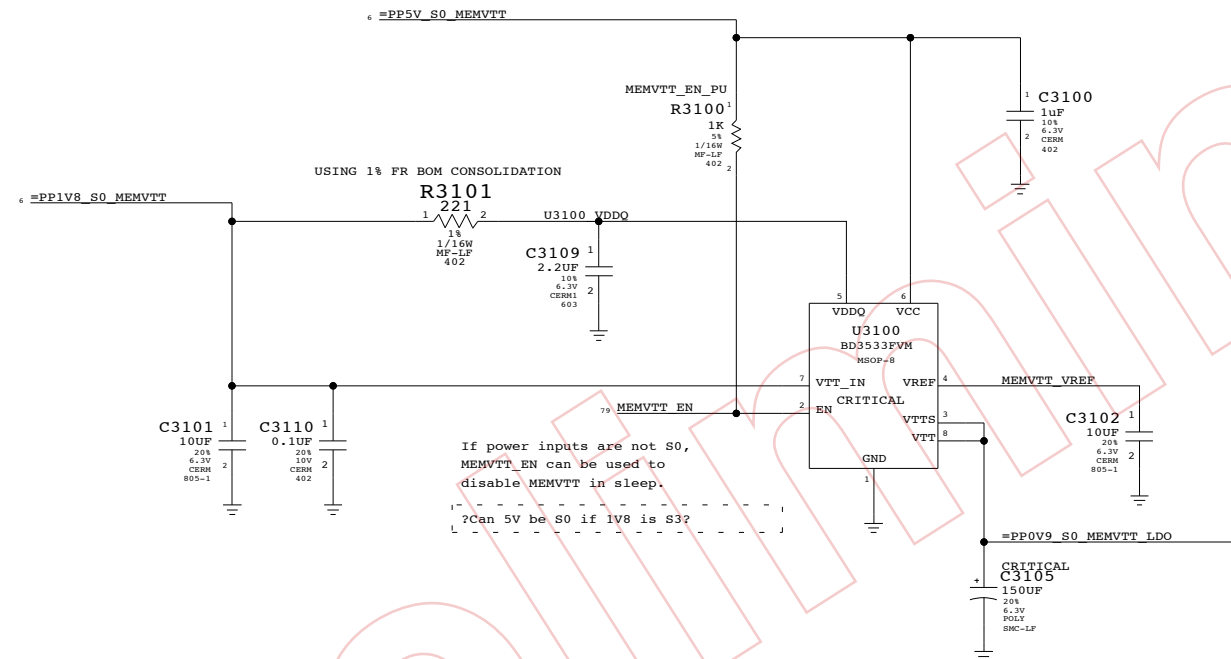
Page Notes

Power aliases required by this page:
 - =PP5V_S0_MEMVTT
 - =PP1V8_S0_MEMVTT
 - =PP0V9_S0_MEMVTT_LDO

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

DDR2 Vtt Regulator



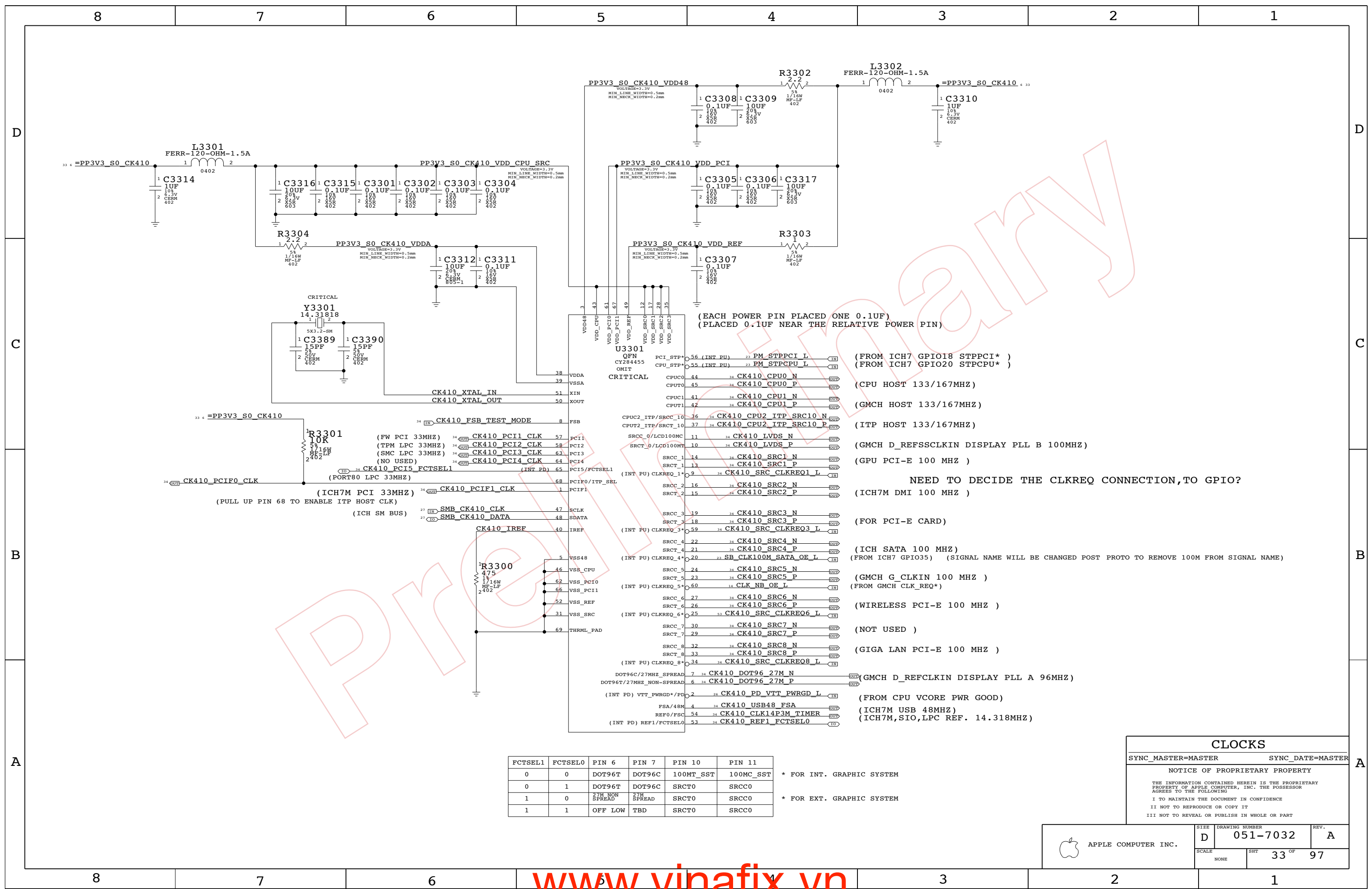
Memory Vtt Supply

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	A
SCALE	SHT	OF	
NONE	31	97	



(EACH POWER PIN PLACED ONE 0.1UF)
(PLACED 0.1UF NEAR THE RELATIVE POWER PIN)

- (FROM ICH7 GPIO18 STPPCI*)
- (FROM ICH7 GPIO20 STPCPU*)
- (CPU HOST 133/167MHZ)
- (GMCH HOST 133/167MHZ)
- (ITP HOST 133/167MHZ)
- (GMCH D_REFSSCLKIN DISPLAY PLL B 100MHZ)
- (GPU PCI-E 100 MHZ)
- NEED TO DECIDE THE CLKREQ CONNECTION, TO GPIO?
- (ICH7M DMI 100 MHZ)
- (FOR PCI-E CARD)
- (ICH SATA 100 MHZ)
- (FROM ICH7 GPIO35) (SIGNAL NAME WILL BE CHANGED POST PROTO TO REMOVE 100M FROM SIGNAL NAME)
- (GMCH G_CLKIN 100 MHZ)
- (FROM GMCH CLK_REQ*)
- (WIRELESS PCI-E 100 MHZ)
- (NOT USED)
- (GIGA LAN PCI-E 100 MHZ)
- (GMCH D_REFCLKIN DISPLAY PLL A 96MHZ)
- (FROM CPU VCORE PWR GOOD)
- (ICH7M USB 48MHZ)
- (ICH7M,SIO,LPC REF. 14.318MHZ)

FCTSEL1	FCTSEL0	PIN 6	PIN 7	PIN 10	PIN 11
0	0	DOT96T	DOT96C	100MT_SST	100MC_SST
0	1	DOT96T	DOT96C	SRCT0	SRCC0
1	0	27M_NON_SPREAD	27M_SPREAD	SRCT0	SRCC0
1	1	OFF LOW	TBD	SRCT0	SRCC0

* FOR INT. GRAPHIC SYSTEM
* FOR EXT. GRAPHIC SYSTEM

CLOCKS

SYNC_MASTER=MASTER SYNC_DATE=MASTER

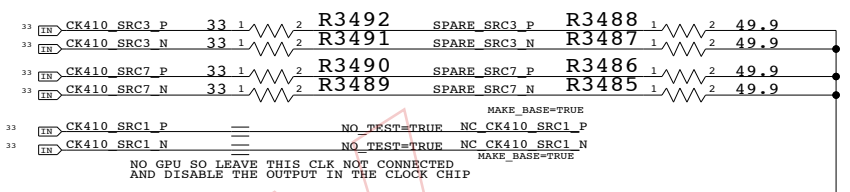
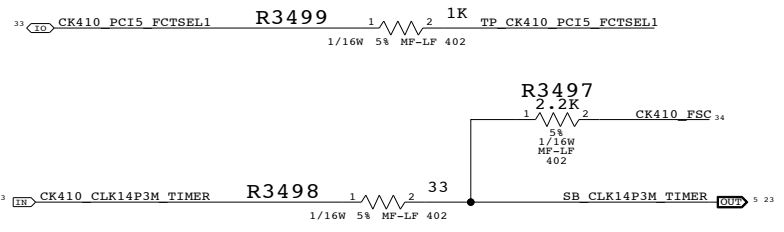
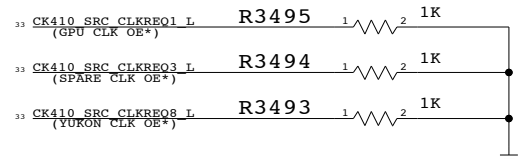
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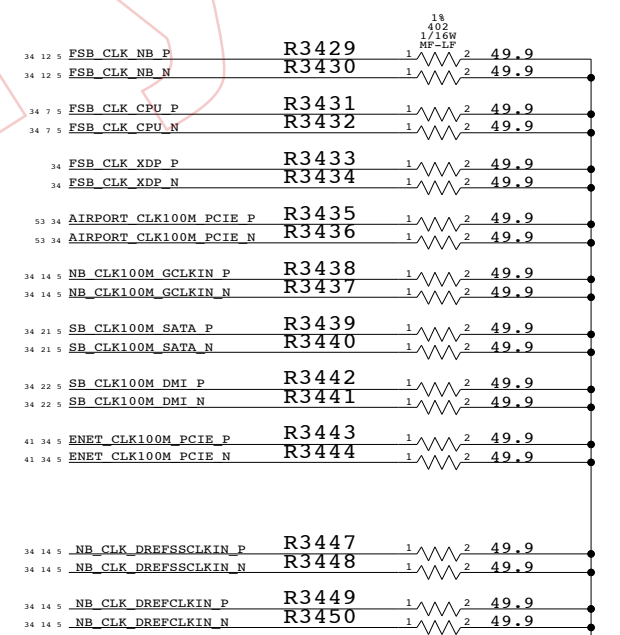
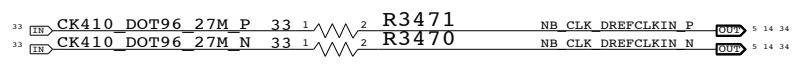
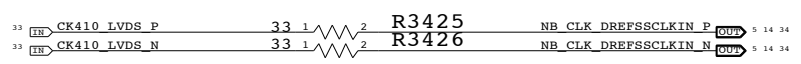
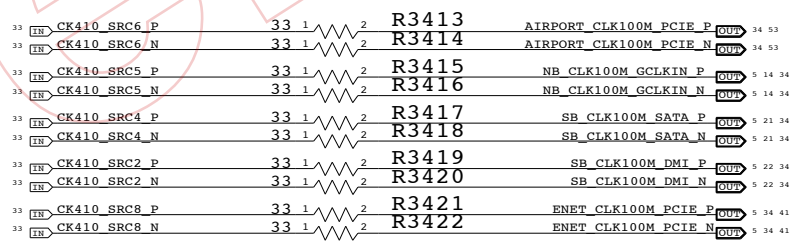
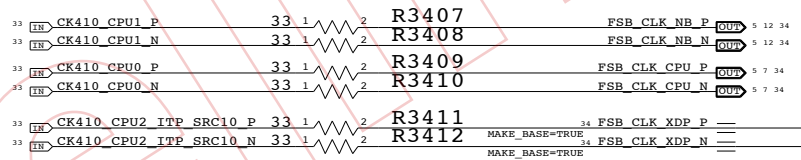
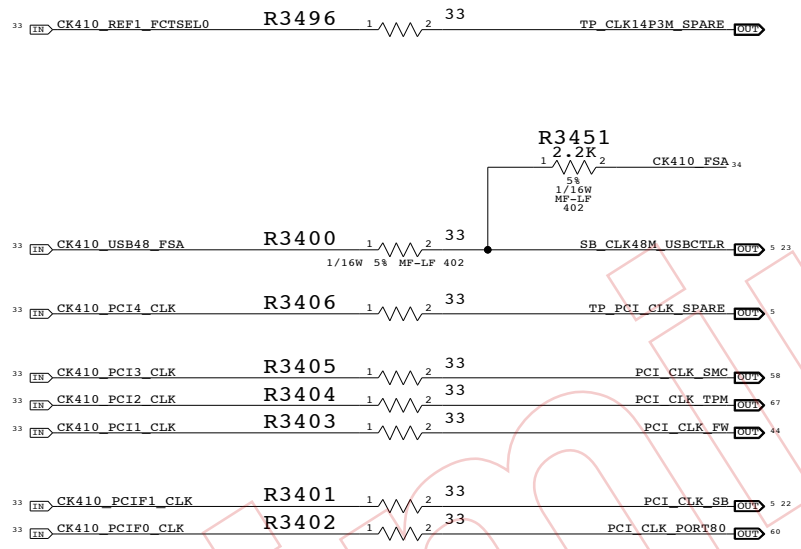
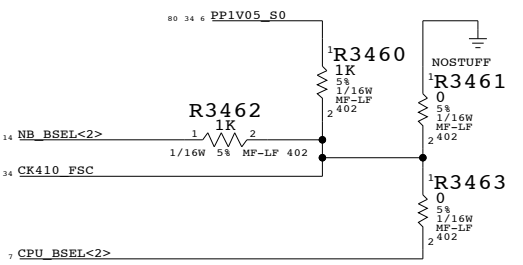
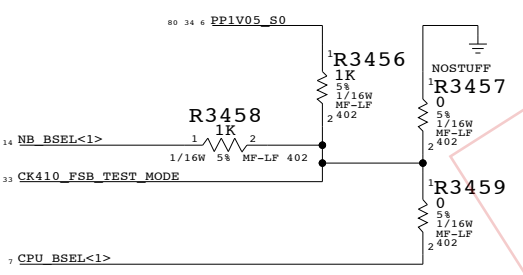
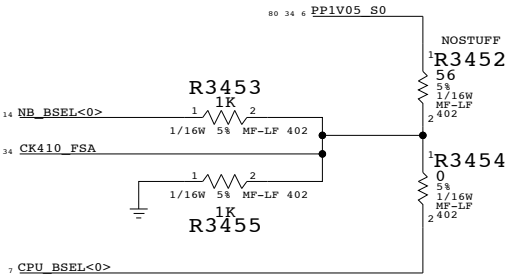
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	A
SCALE	SHT	33 OF 97	
NONE			

NOTE: USE THESE PULL-DOWNS IF NOT CONNECTED TO GPIO'S



FSB FREQUENCY SELECT:

	STUFF	NO STUFF
CPU DRIVEN	R3454 R3455 R3461	R3452 R3453 R3457
533MHZ (133MHZ CPU CLK)	R3452 R3453 R3461	R3454 R3455 R3463
667MHZ (166MHZ CPU CLK)	R3452 R3453 R3461	R3454 R3455 R3463



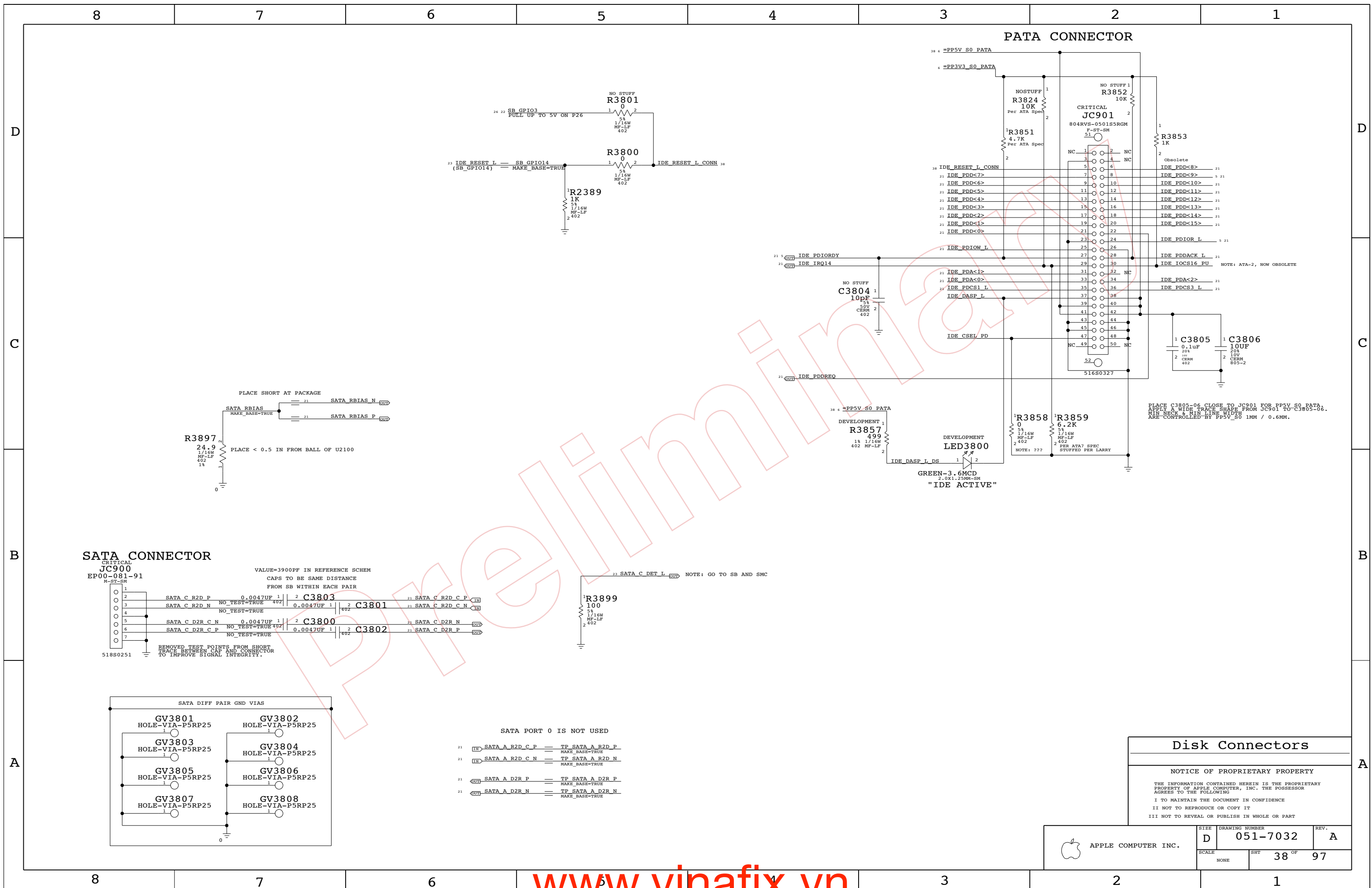
CLOCKS: TERMINATIONS

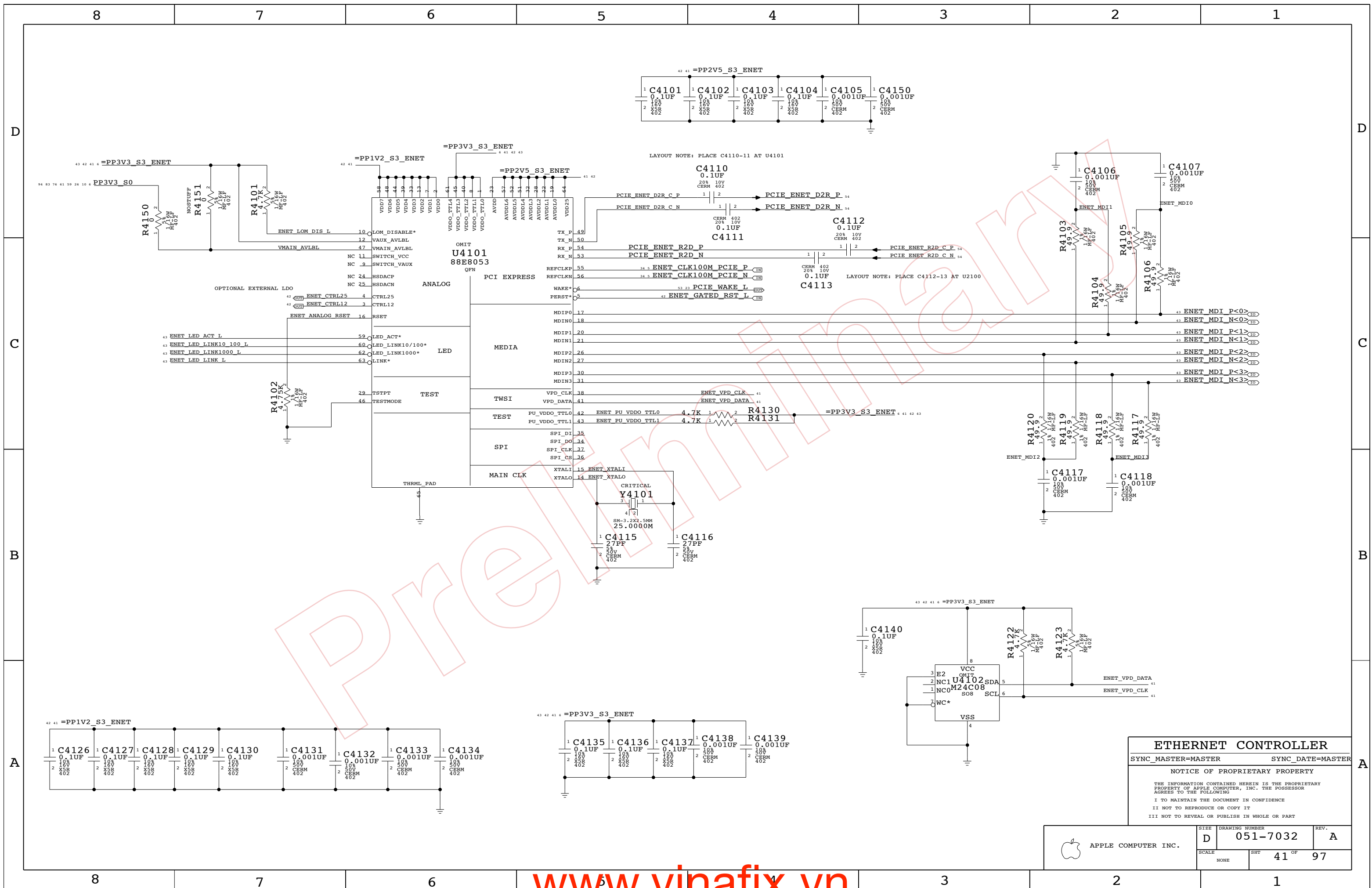
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	D	051-7032	A
SCALE	NONE	SHT	34 OF 97





ETHERNET CONTROLLER

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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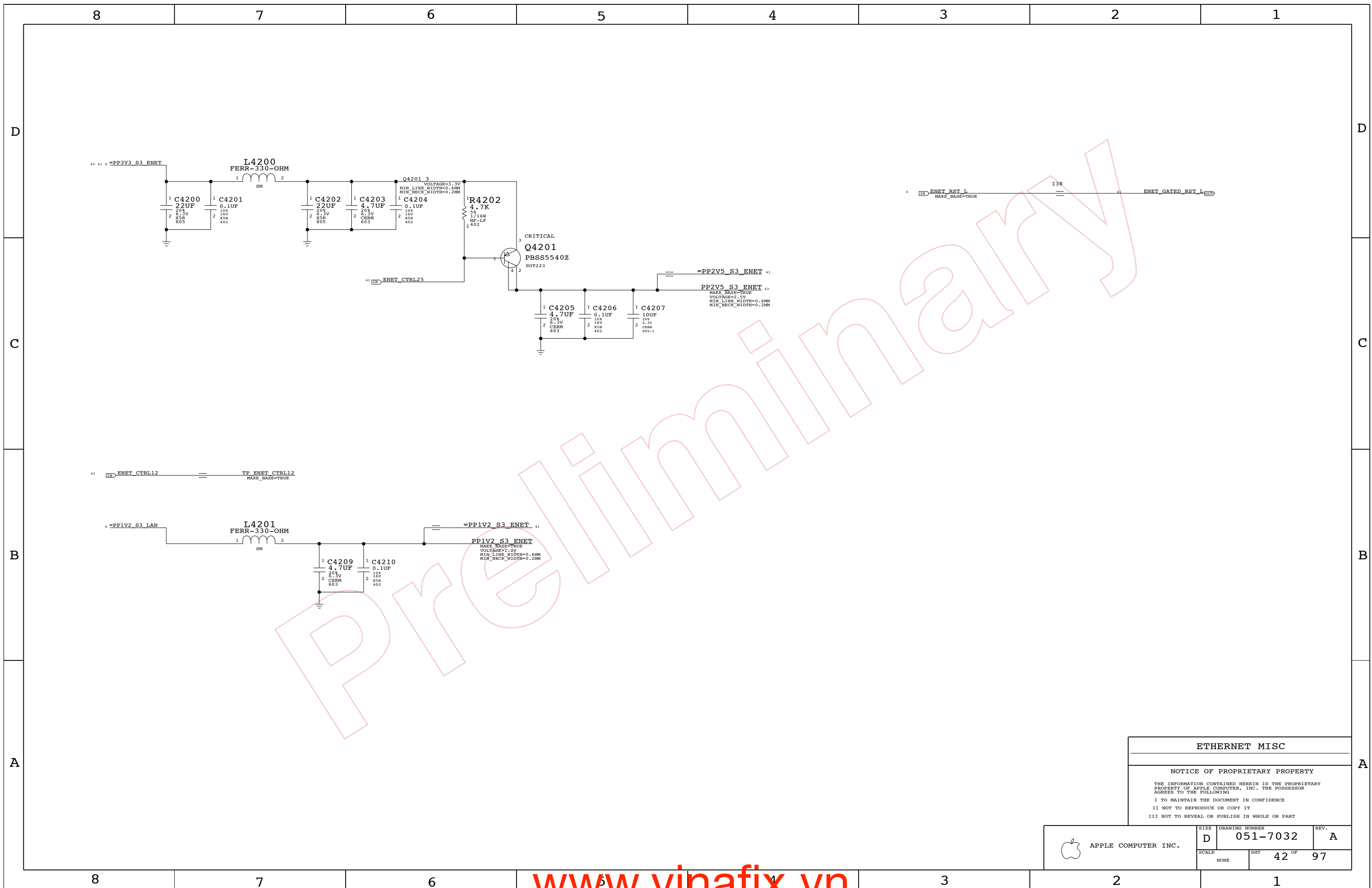
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	SCALE NONE	SHEET 41 OF 97	



ETHERNET MISC

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7032	REV. A
	SCALE NONE	SHEET 42 OF 97	

8

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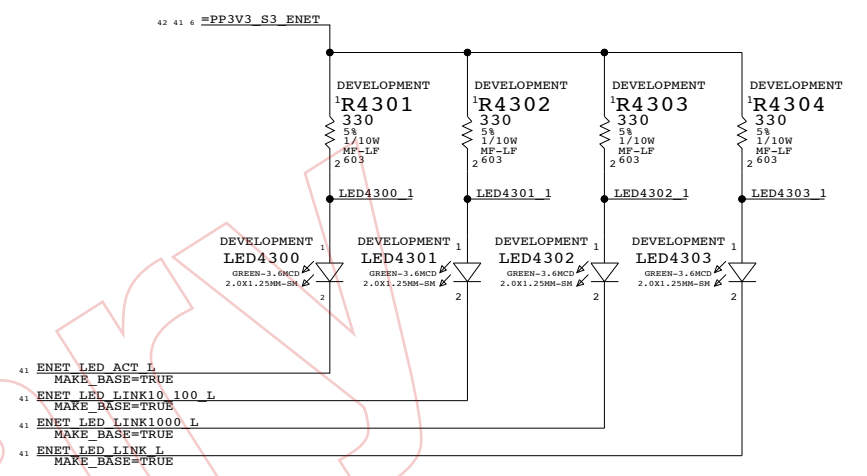
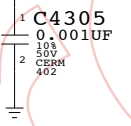
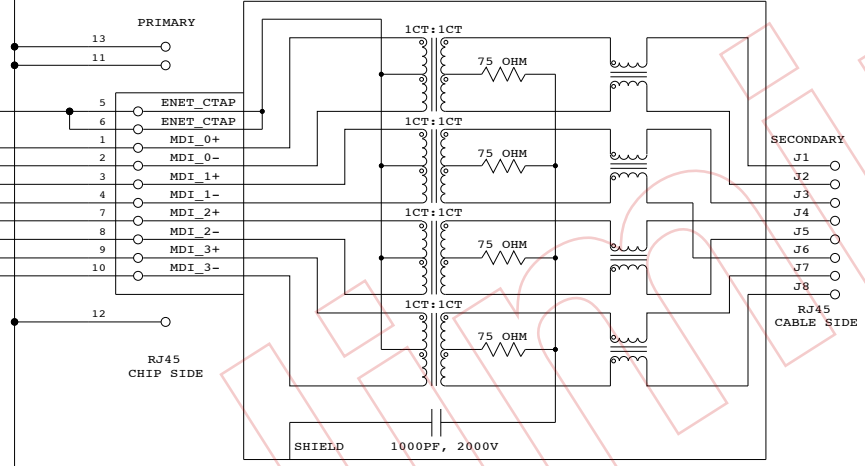
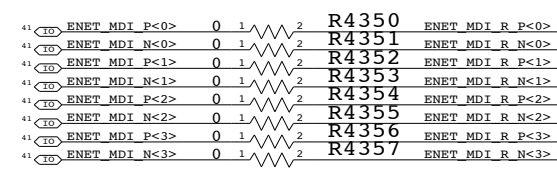
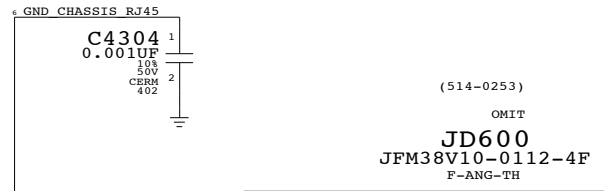
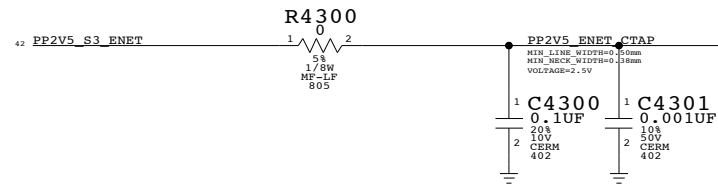
4

3

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1

RESISTOR PADS USED AS PLACEHOLDER FOR INDUCTOR IF NEEDED



D

D

C

C

B

B

A

A

ETHERNET CONNECTOR

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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0365	1	CON,RJ-45 7 DEGRESS, 243DEG C	JD600	CRITICAL	17_INCH_LCD

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	A
SCALE	SHT	43 OF 97	
NONE			

8

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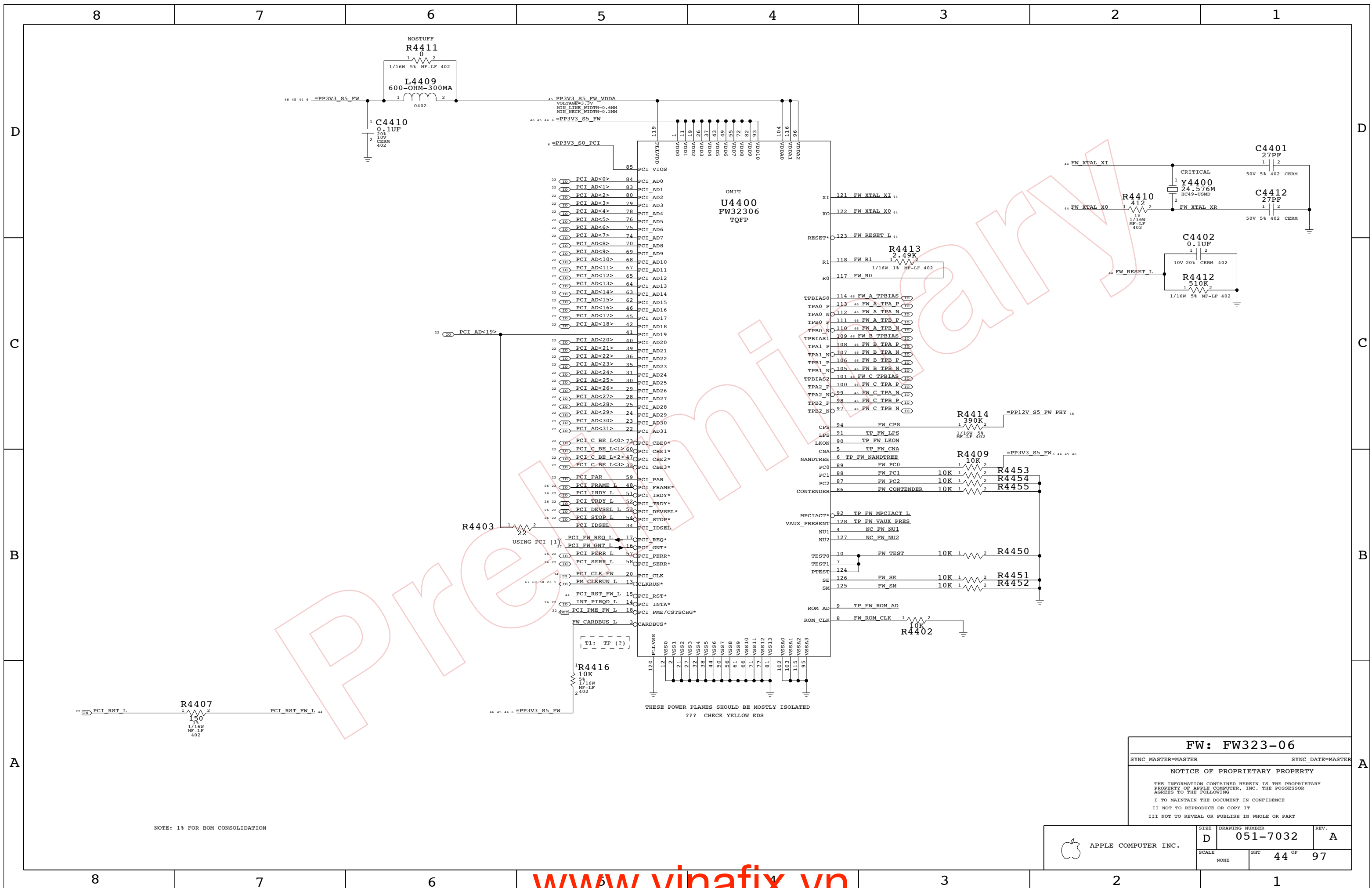
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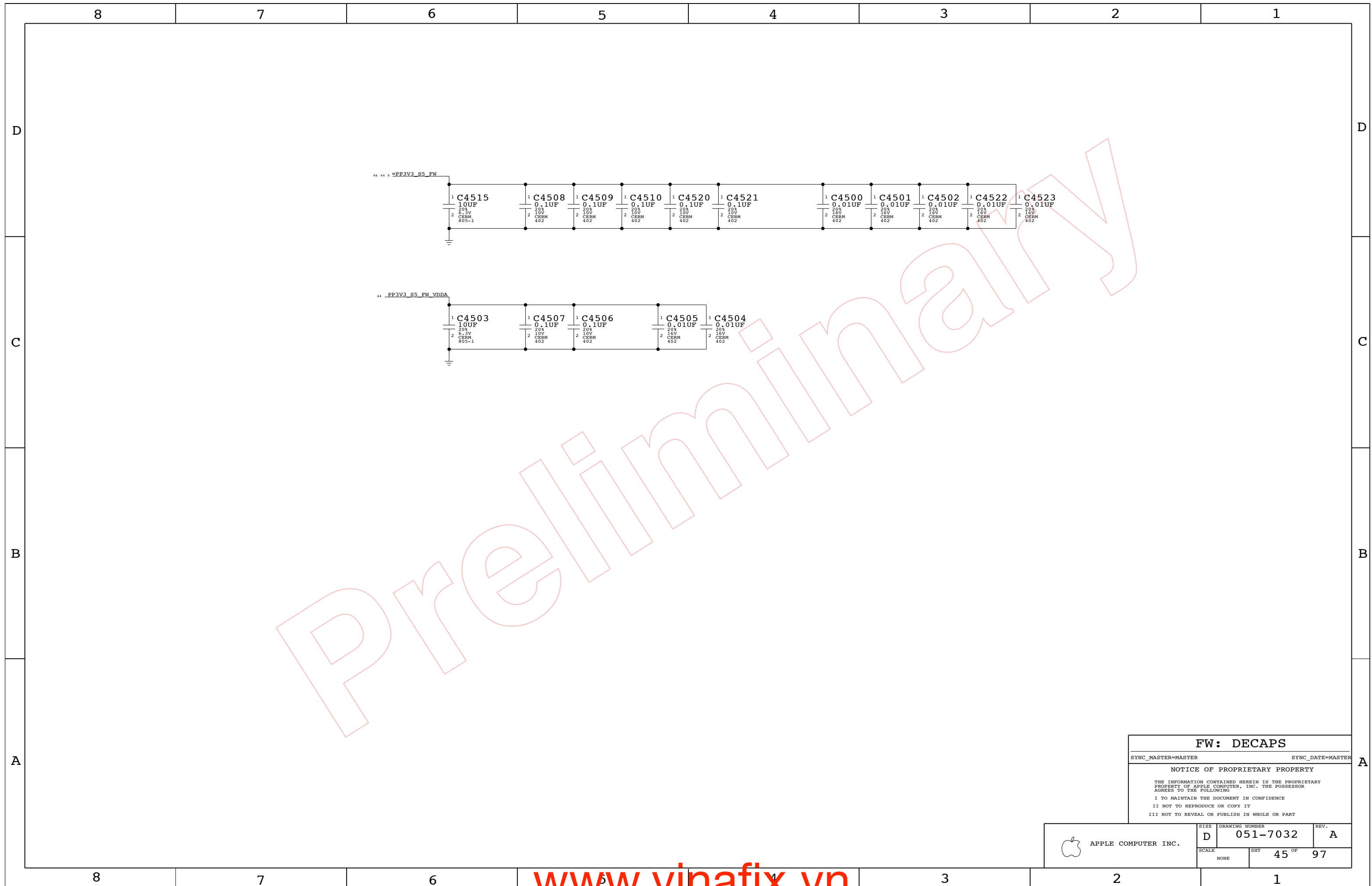
PROPRIETARY

THESE POWER PLANES SHOULD BE MOSTLY ISOLATED
 ??? CHECK YELLOW EDS

NOTE: 1% FOR BOM CONSOLIDATION

FW: FW323-06	
SYNC_MASTER=MASTER	SYNC_DATE=MASTER
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	D	051-7032	A
SCALE	SHT	44 OF	97
NONE			



Preliminary

FW: DECAPS

SYNC_MASTER=MASTER SYNC_DATE=MASTER

NOTICE OF PROPRIETARY PROPERTY

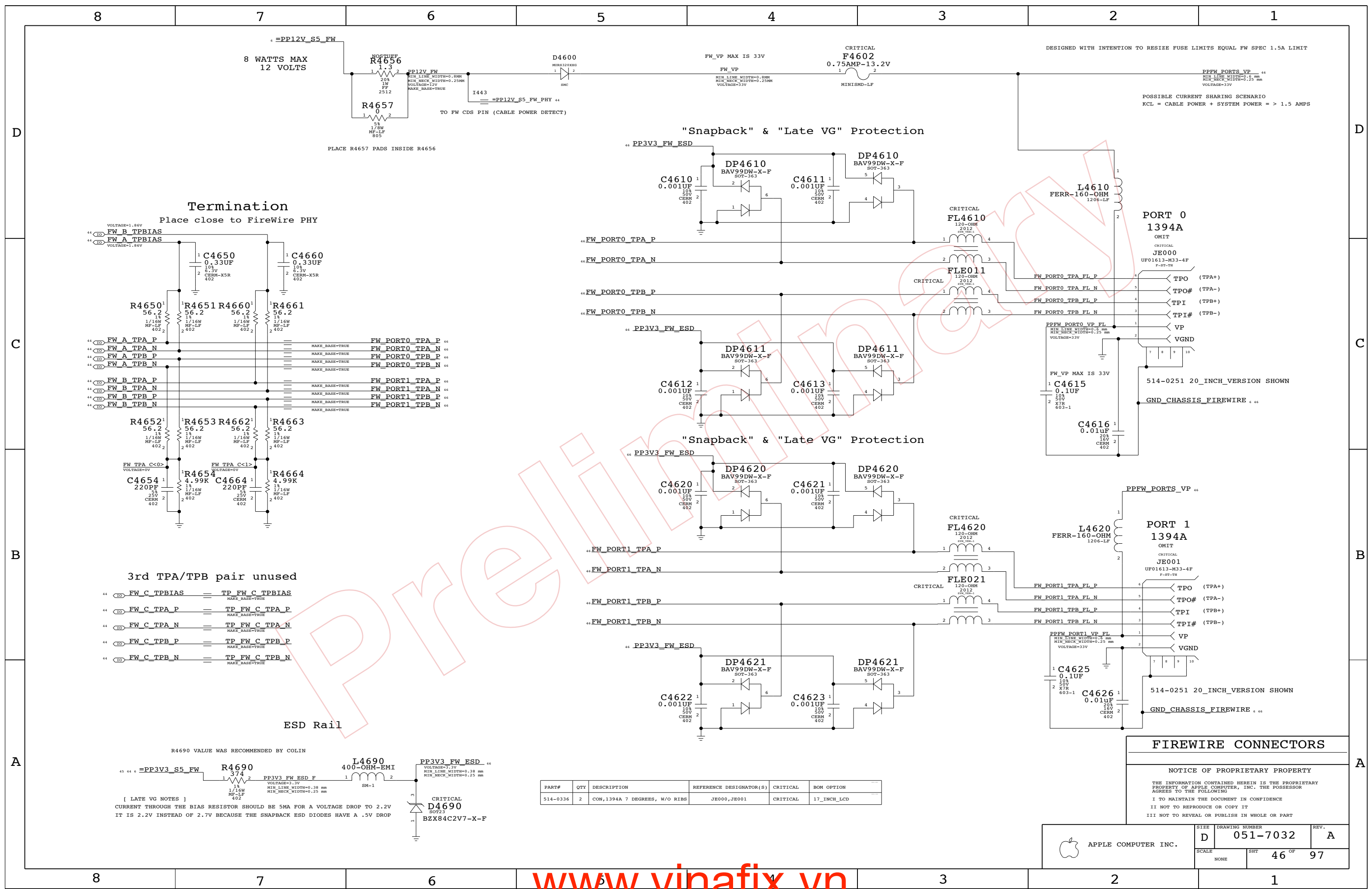
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APPLE COMPUTER INC.	SIZE	D	DRAWING NUMBER	051-7032	REV.	A
	SCALE	NONE	SHT	45 OF 97		



Termination
Place close to FireWire PHY

"Snapback" & "Late VG" Protection

"Snapback" & "Late VG" Protection

3rd TPA/TPB pair unused

ESD Rail

R4690 VALUE WAS RECOMMENDED BY COLIN

[LATE VG NOTES]
CURRENT THROUGH THE BIAS RESISTOR SHOULD BE 5MA FOR A VOLTAGE DROP TO 2.2V IT IS 2.2V INSTEAD OF 2.7V BECAUSE THE SNAPBACK ESD DIODES HAVE A .5V DROP

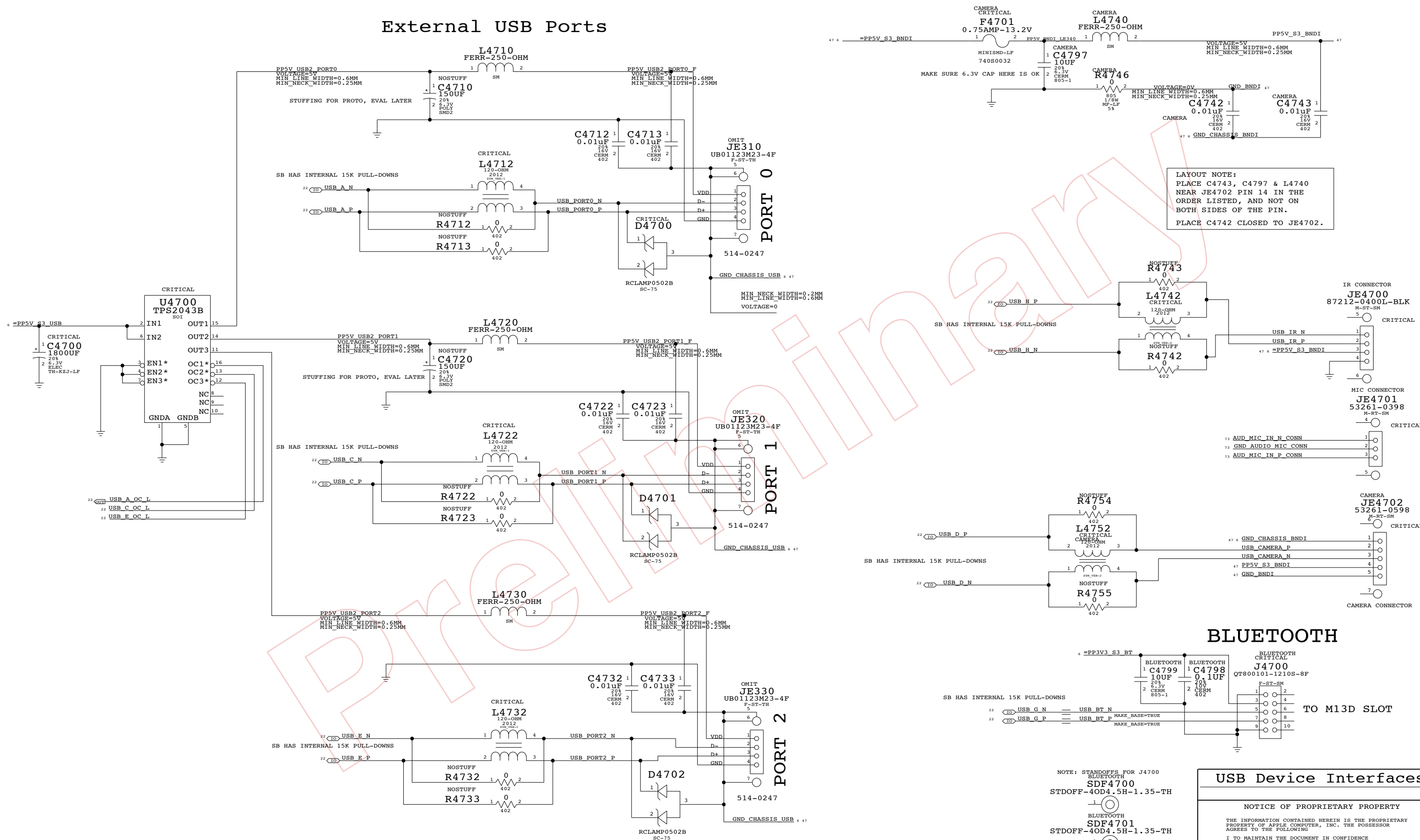
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0336	2	CON,1394A 7 DEGREES, W/O RIBS	JE000,JE001	CRITICAL	17_INCH_LCD

FIREWIRE CONNECTORS

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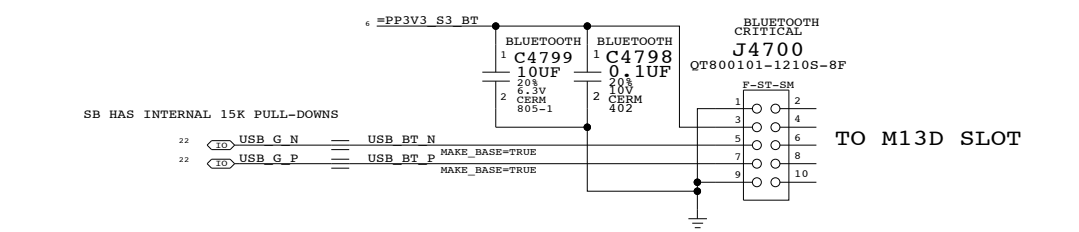
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7032	REV. A
	SCALE NONE	SHEET 46 OF 97	

External USB Ports



LAYOUT NOTE:
 PLACE C4743, C4797 & L4740
 NEAR JE4702 PIN 14 IN THE
 ORDER LISTED, AND NOT ON
 BOTH SIDES OF THE PIN.
 PLACE C4742 CLOSED TO JE4702.

BLUETOOTH



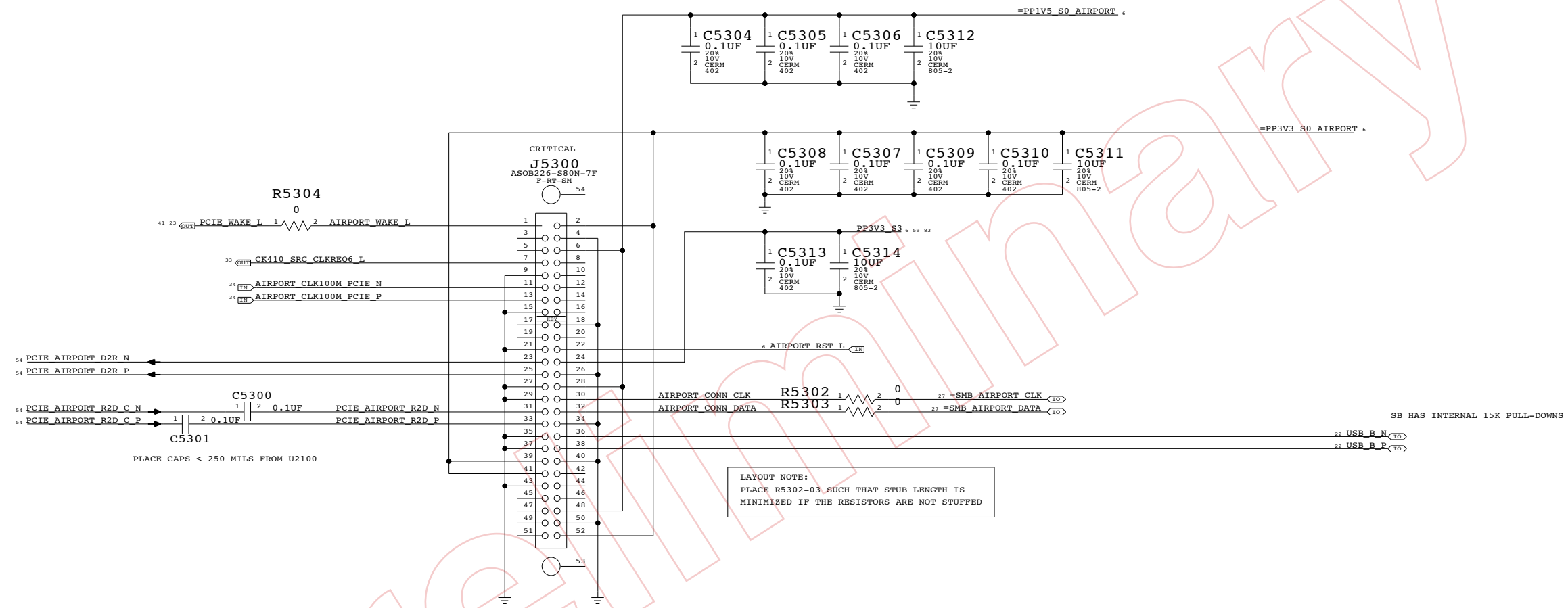
NOTE: STANDOFFS FOR J4700
 BLUETOOTH
SDF4700
 STDOFF-40D4.5H-1.35-TH
 BLUETOOTH
SDF4701
 STDOFF-40D4.5H-1.35-TH

USB Device Interfaces



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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0339	3	USB RECEPTACLE, 4P, UB1123-M50-4F	JE310, JE320, JE330	CRITICAL	17_INCH_LCD

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	A
SCALE	SHT	47 OF	97
NONE			



LAYOUT NOTE:
 PLACE R5302-03 SUCH THAT STUB LENGTH IS
 MINIMIZED IF THE RESISTORS ARE NOT STUFFED

NOTE: STANDOFFS FOR J5300
 SDF5300
 STDOFF-40D5.6H-1.35-TH

 SDF5301
 STDOFF-40D5.6H-1.35-TH


AIRPORT CONN
 SYNC_MASTER=MASTER SYNC_DATE=MASTER
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SCALE	SHT	OF	
NONE	53	97	

8

7

6

5

4

3

2

1

D

D

C

C

B

B

A

A

22 IN PCIE_C_R2D_C_N == TP_PCIE_C_R2D_C_N
MAKE_BASE=TRUE

22 IN PCIE_C_R2D_C_P == TP_PCIE_C_R2D_C_P
MAKE_BASE=TRUE

22 OUT PCIE_C_D2R_N == TP_PCIE_C_D2R_N
MAKE_BASE=TRUE

22 OUT PCIE_C_D2R_P == TP_PCIE_C_D2R_P
MAKE_BASE=TRUE

22 IN PCIE_D_R2D_C_N == TP_PCIE_D_R2D_C_N
MAKE_BASE=TRUE

22 IN PCIE_D_R2D_C_P == TP_PCIE_D_R2D_C_P
MAKE_BASE=TRUE

22 OUT PCIE_D_D2R_N == TP_PCIE_D_D2R_N
MAKE_BASE=TRUE

22 OUT PCIE_D_D2R_P == TP_PCIE_D_D2R_P
MAKE_BASE=TRUE

22 IN PCIE_E_R2D_C_N == TP_PCIE_E_R2D_C_N
MAKE_BASE=TRUE

22 IN PCIE_E_R2D_C_P == TP_PCIE_E_R2D_C_P
MAKE_BASE=TRUE

22 OUT PCIE_E_D2R_N == TP_PCIE_E_D2R_N
MAKE_BASE=TRUE

22 OUT PCIE_E_D2R_P == TP_PCIE_E_D2R_P
MAKE_BASE=TRUE

22 IN PCIE_F_R2D_C_N == TP_PCIE_F_R2D_C_N
MAKE_BASE=TRUE

22 IN PCIE_F_R2D_C_P == TP_PCIE_F_R2D_C_P
MAKE_BASE=TRUE

22 OUT PCIE_F_D2R_N == TP_PCIE_F_D2R_N
MAKE_BASE=TRUE

22 OUT PCIE_F_D2R_P == TP_PCIE_F_D2R_P
MAKE_BASE=TRUE

USED PCIE PORTS

22 IN PCIE_A_R2D_C_N == PCIE_AIRPORT_R2D_C_N 53
MAKE_BASE=TRUE

22 IN PCIE_A_R2D_C_P == PCIE_AIRPORT_R2D_C_P 53
MAKE_BASE=TRUE

22 5 OUT PCIE_A_D2R_N == PCIE_AIRPORT_D2R_N 53
MAKE_BASE=TRUE

22 5 OUT PCIE_A_D2R_P == PCIE_AIRPORT_D2R_P 53
MAKE_BASE=TRUE

22 IN PCIE_B_R2D_C_N == PCIE_ENET_R2D_C_N 41
MAKE_BASE=TRUE

22 IN PCIE_B_R2D_C_P == PCIE_ENET_R2D_C_P 41
MAKE_BASE=TRUE

22 5 OUT PCIE_B_D2R_N == PCIE_ENET_D2R_N 41
MAKE_BASE=TRUE

22 5 OUT PCIE_B_D2R_P == PCIE_ENET_D2R_P 41
MAKE_BASE=TRUE

PCIE PORT ALIASES

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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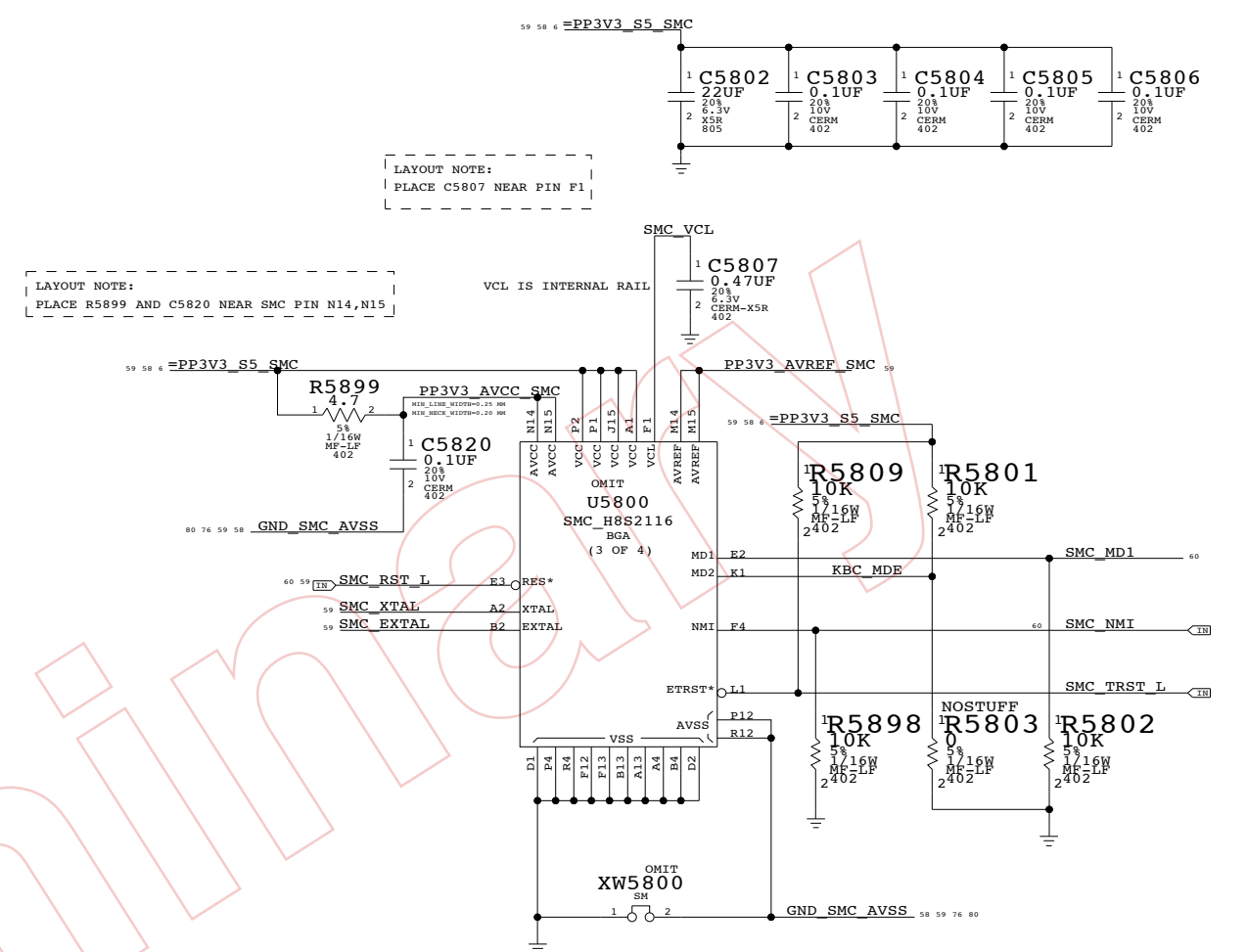
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	A
SCALE	SHT	OF	
NONE	54	97	

UNUSED PINS HAVE THE FORMAT SMC_XXX WHERE XXX IS THE PORT NUMBER. THEY ARE SET BY SOFTWARE TO BE DRIVEN OUTPUS ALWAYS SO THEY CAN BE LEFT NO-CONNECTED.

U5800 SMC_H8S2116 (1 OF 4)		U5800 SMC_H8S2116 (3 OF 4)	
P10	B12	P60/KIN0*	L13
P11	C13	P61/KIN1*	L14
P12	A15	P62/KIN2*	L15
P13	B14	P63/KIN3*	K12
P14	B15	P64/KIN4*	K13
P15	C14	P65/KIN5*	K14
P16	D12	P66/IRQ6*/KIN6*	J12
P17	C15	P67/IRQ7*/KIN7*	J13
P20	D13	P70/AN0	N12
P21	D14	P71/AN1	R13
P22	D15	P72/AN2	P13
P23	E12	P73/AN3	R14
P24	E14	P74/AN4	R14
P25	E15	P75/AN5	R15
P26	E13	P76/AN6	N13
P27	F14	P77/AN7	P15
P30/LAD0	D9	P80/PME*	C7
P31/LAD1	C9	P81/GA20	A7
P32/LAD2	A9	P82/CLKRUN*	B7
P33/LAD3	B9	P83/LPCPD*	D6
P34/LFRAME*	D8	P84/IRQ3*/TXD1	C6
P35/LRESET*	C8	P85/IRQ4*/RXD1	A6
P36/LCLK	A8	P86/IRQ5*/SCL1/SCL1	B6
P37/SERIRQ	D7	P90/IRQ2*	K4
P40/TMIO	A5	P91/IRQ1*	J2
P41/TMO0	B5	P92/IRQ0*	J1
P42/SDA1	D5	P93/IRQ12*	J3
P43/TMI1/EXSCK1	C3	P94/IRQ13*	J4
P44/TMO1	B1	P95/IRQ14*	H2
P45	C2	P96/EXCL	H1
P46/PWX0/PWM0	D3	P97/IRQ15*/SDA0	G2
P47/PWX1/PWM1	C1		
P50	G1		
P51	G4		
P52/SCL0	F2		

U5800 SMC_H8S2116 (2 OF 4)		U5800 SMC_H8S2116 (4 OF 4)	
P2	R3	PE0	M3
P3	R2	PE1*/ETCK	M2
P4	R1	PE2*/ETDI	M1
P5	R1	PE3*/ETDO	L4
P6	R1	PE4*/ETMS	L2
P7	R1	PF0/IRQ8*/PWM2	M7
P8	R1	PF1/IRQ9*/PWM3	P6
P9	R1	PF2/IRQ10*/TMOY	R6
P10	R1	PF3/IRQ11*/TMOX	N6
P11	R1	PF4/PWM4	M6
P12	R1	PF5/PWM5	R5
P13	R1	PF6/PWM6	P5
P14	R1	PF7/PWM7	N5
P15	R1	PG0/EXIRQ8*/TMIX	P9
P16	R1	PG1/EXIRQ9*/TMIY	R9
P17	R1	PG2/EXIRQ10*/SDA2	N9
P18	R1	PG3/EXIRQ11*/SCL2	P8
P19	R1	PG4/EXIRQ12*/EXSDAA	R8
P20	R1	PG5/EXIRQ13*/EXSCLA	M8
P21	R1	PG6/EXIRQ14*/EXSDAB	P7
P22	R1	PG7/EXIRQ15*/EXSCLB	R7
P23	R1	PH0/EXIRQ6*	E1
P24	R1	PH1/EXIRQ7*	E3
P25	R1	PH2/FWE	K2
P26	R1	PH3/EXEXCL	C4
P27	R1	PH4	D4
P28	R1	PH5	B3

U5800 SMC_H8S2116 (4 OF 4)	
NC0	E15
NC1	A14
NC2	C12
NC3	C10
NC4	C5
NC5	A3
NC6	B8
NC7	E4
NC8	H4
NC9	M9
NC10	M9
NC11	N8



SMC

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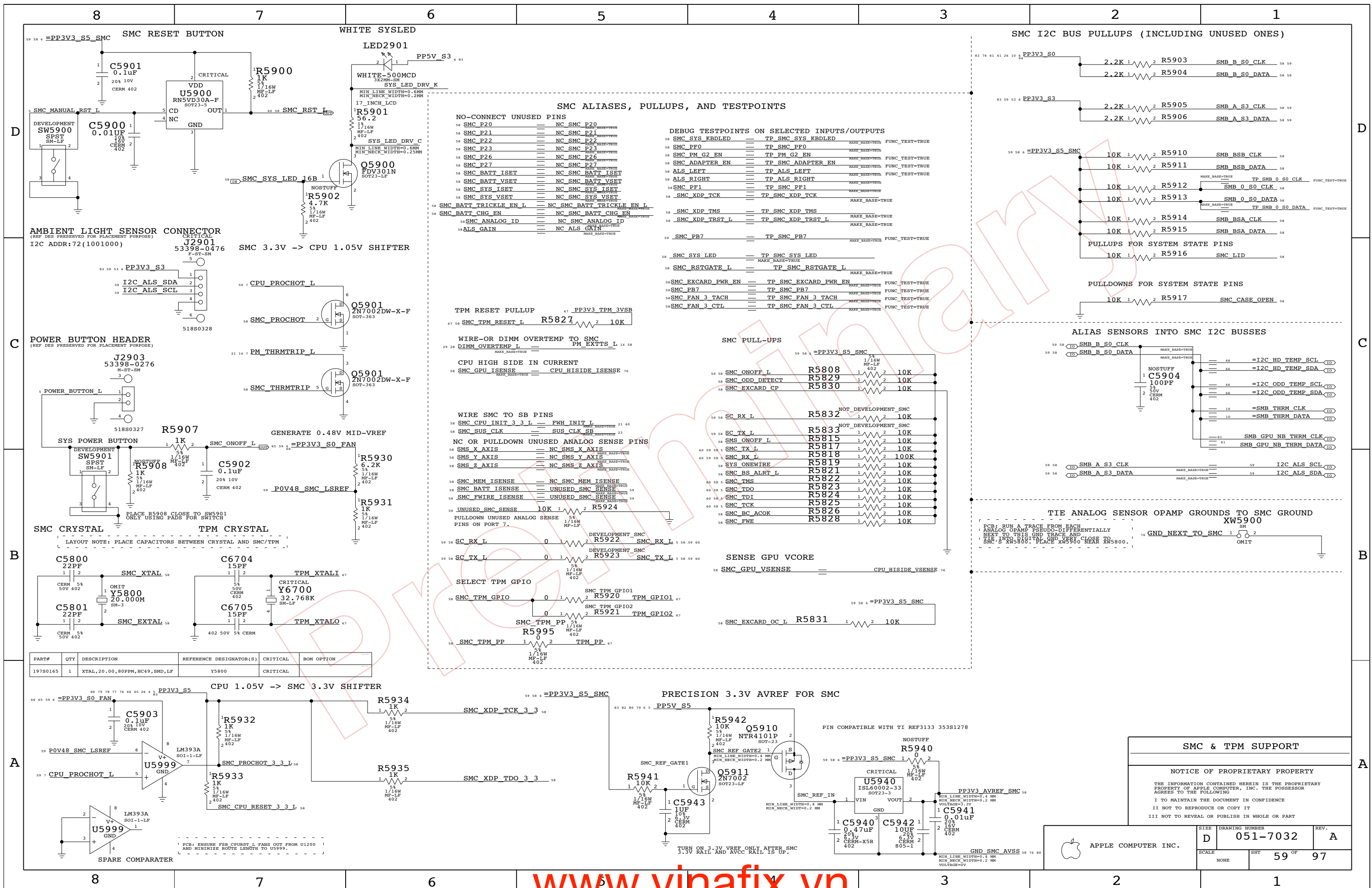
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	D	051-7032	A
SCALE	SHT	58 OF 97	
NONE			



- ### SMC ALIASES, PULLUPS, AND TESTPOINTS
- NO-CONNECT UNUSED PINS**
- SMC P20 = NC SMC P20
 - SMC P21 = NC SMC P21
 - SMC P22 = NC SMC P22
 - SMC P23 = NC SMC P23
 - SMC P26 = NC SMC P26
 - SMC P27 = NC SMC P27
 - SMC BATT_ISET = NC SMC BATT_ISET
 - SMC BATT_VSET = NC SMC BATT_VSET
 - SMC SYS_ISET = NC SMC SYS_ISET
 - SMC SYS_VSET = NC SMC SYS_VSET
 - SMC BATT_TRICKLE_EN_L = NC SMC BATT_TRICKLE_EN_L
 - SMC BATT_CHG_EN = NC SMC BATT_CHG_EN
 - SMC ANALOG_ID = NC SMC ANALOG_ID
 - ALS_GAIN = NC ALS_GAIN
- DEBUG TESTPOINTS ON SELECTED INPUTS/OUTPUTS**
- SMC_SYS_KBDLED = TP_SMC_SYS_KBDLED
 - SMC_PFO = TP_SMC_PFO
 - SMC_PM_G2_EN = TP_SMC_PM_G2_EN
 - SMC_ADAPTER_EN = TP_SMC_ADAPTER_EN
 - ALS_LEFT = TP_SMC_ALS_LEFT
 - ALS_RIGHT = TP_SMC_ALS_RIGHT
 - SMC_PFI = TP_SMC_PFI
 - SMC_XDP_TCK = TP_SMC_XDP_TCK
 - SMC_XDP_TMS = TP_SMC_XDP_TMS
 - SMC_XDP_TRST_L = TP_SMC_XDP_TRST_L
 - SMC_PB7 = TP_SMC_PB7
 - SMC_SYS_LED = TP_SMC_SYS_LED
 - SMC_RSTGATE_L = TP_SMC_RSTGATE_L
 - SMC_EXCARD_PWR_EN = TP_SMC_EXCARD_PWR_EN
 - SMC_PB7 = TP_SMC_PB7
 - SMC_FAN_3_TACH = TP_SMC_FAN_3_TACH
 - SMC_FAN_3_CTL = TP_SMC_FAN_3_CTL

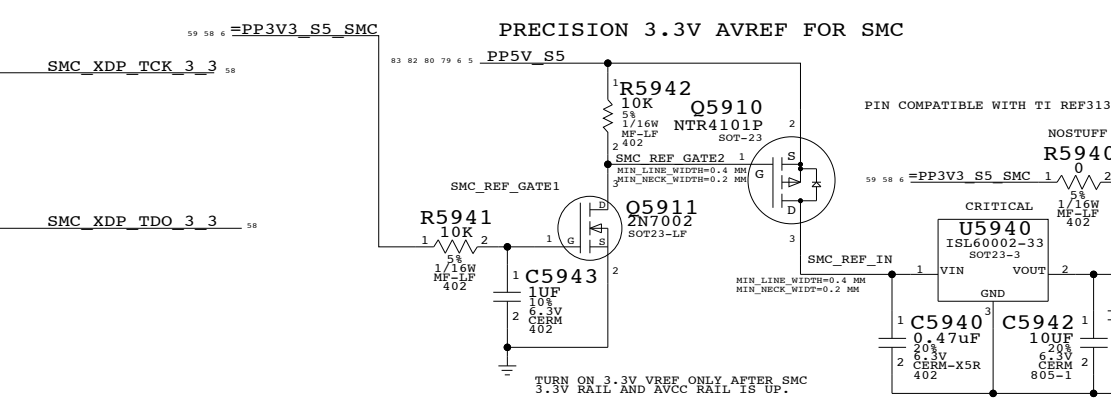
- TPM RESET PULLUP**
- SMC_TPM_RESET_L = R5827
- WIRE-OR DIMM OVERTEMP TO SMC**
- DIMM_OVERTEMP_L = PM_EXTTLS_L
- CPU HIGH SIDE IN CURRENT**
- SMC_GPU_ISENSE = CPU_HISIDE_ISENSE
- WIRE SMC TO SB PINS**
- SMC_CPU_INIT_3_3_L = FWH_INIT_L
 - SMC_SUS_CLK = SUS_CLK_SB
 - NC OR PULLDOWN UNUSED ANALOG SENSE PINS
 - SMS_X_AXIS = NC_SMS_X_AXIS
 - SMS_Y_AXIS = NC_SMS_Y_AXIS
 - SMS_Z_AXIS = NC_SMS_Z_AXIS
 - SMC_MEM_ISENSE = NC_SMC_MEM_ISENSE
 - SMC_BATT_ISENSE = UNUSED_SMC_ISENSE
 - SMC_FWIRE_ISENSE = UNUSED_SMC_ISENSE
 - UNUSED_SMC_SENSE = R5924
 - PULLDOWN UNUSED ANALOG SENSE PINS ON PORT 7.
 - SC_RX_L = R5922
 - SC_TX_L = R5923

- SMC PULL-UPS**
- SMC_ONOFF_L = R5808
 - SMC_ODD_DETECT = R5829
 - SMC_EXCARD_CP = R5830
 - SC_RX_L = R5832
 - SC_TX_L = R5833
 - SMS_ONOFF_L = R5815
 - SMC_TX_L = R5817
 - SMC_RX_L = R5818
 - SYS_ONEWIRE = R5819
 - SMC_BS_ALRT_L = R5821
 - SMC_TMS = R5822
 - SMC_TDO = R5823
 - SMC_TDI = R5824
 - SMC_TCK = R5825
 - SMC_BC_ACOK = R5826
 - SMC_FWE = R5828

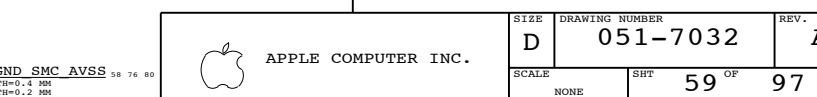
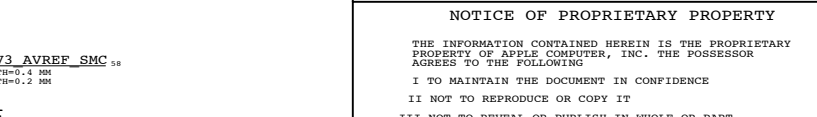
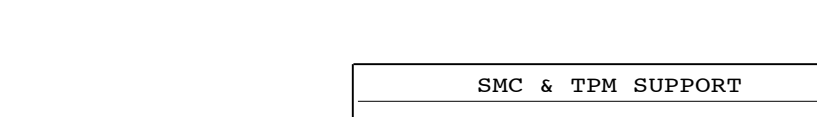
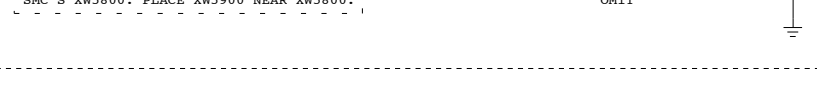
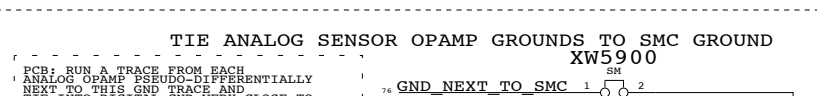
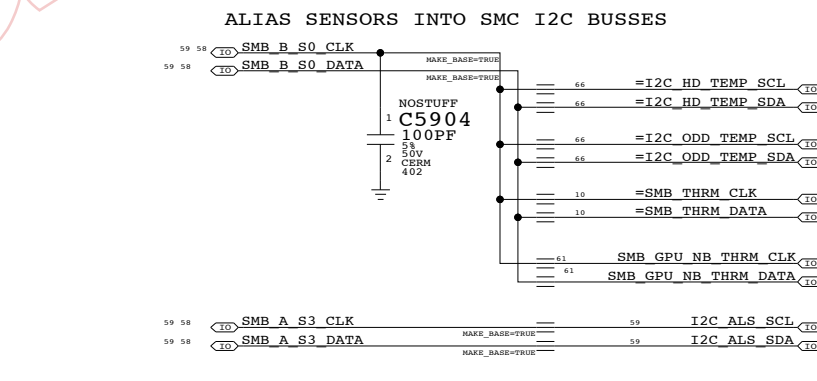
- SELECT TPM GPIO**
- SMC_TPM_GPIO = R5920
 - SMC_TPM_GPIO2 = R5921
 - SMC_TPM_PP = R5995
- SENSE GPU VCORE**
- SMC_GPU_VSENSE = CPU_HISIDE_VSENSE
- SMC EXCARD OC L**
- SMC_EXCARD_OC_L = R5831

- SMC XTAL**
- SMC_XTAL = C5800
 - SMC_EXTAL = C5801
- TPM XTAL**
- TPM_XTALI = C6704
 - TPM_XTALO = C6705

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
19780165	1	XTAL, 20.00, 80PPM, HC49, SMD, LF	Y5800	CRITICAL	



PCB: ENSURE FSB CPURESET_L PINS OUT FROM U1200 AND MINIMIZE ROUTER LENGTH TO U3999.



PCB: RUN A TRACE FROM EACH ANALOG OPAMP PSEUDO-DIFFERENTIALLY NEXT TO THIS GND TRACE AND TIE INTO DIGITAL GND VERY CLOSE TO SMC'S XW5800. PLACE XW5900 NEAR XW5800.

SMC & TPM SUPPORT

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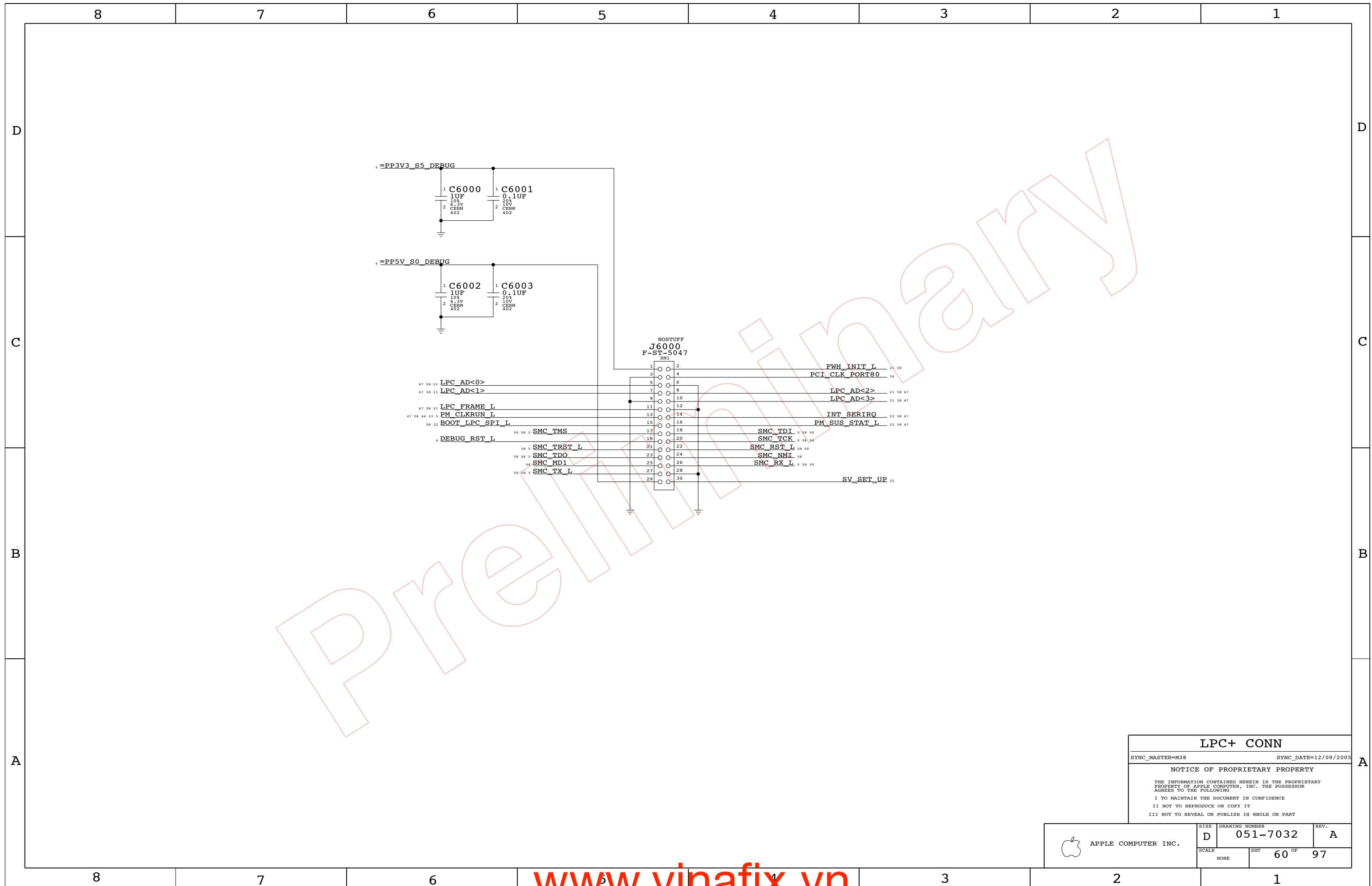
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D	051-7032	A
SCALE	SHT	59 OF 97
NONE		

APPLE COMPUTER INC.



LPC+ CONN

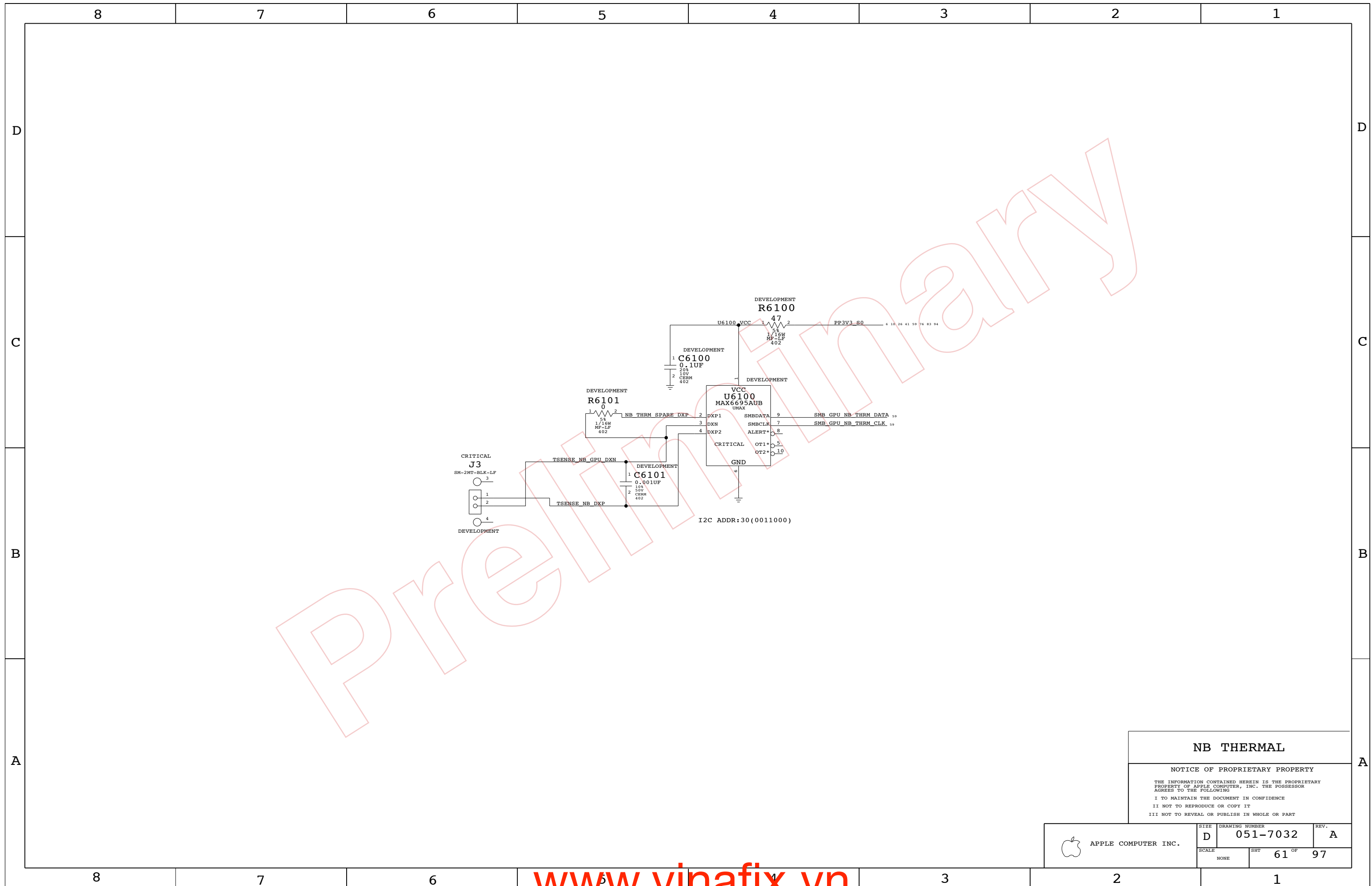
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	SCALE NONE	SHT 60 OF	97



NB THERMAL

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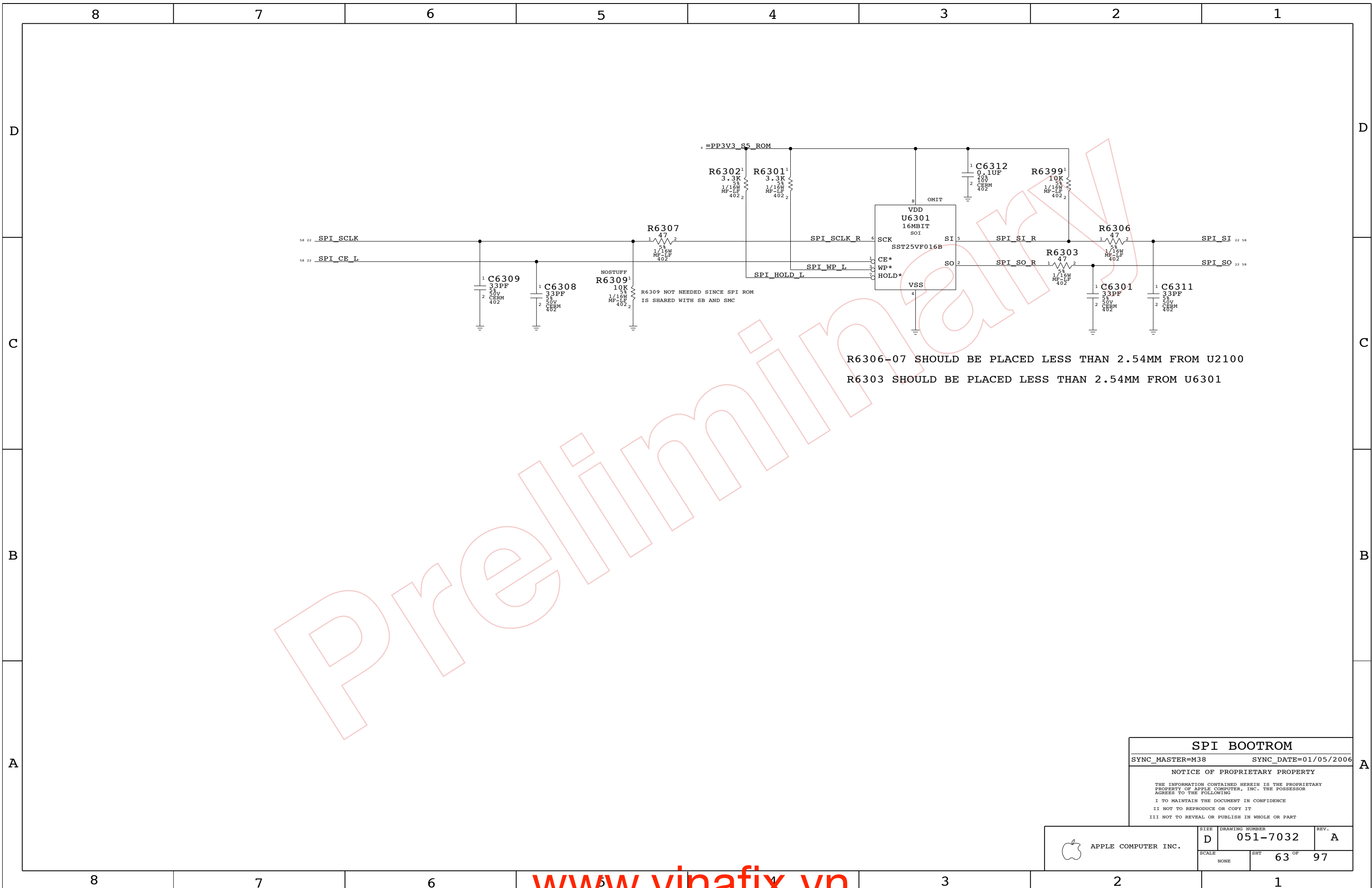
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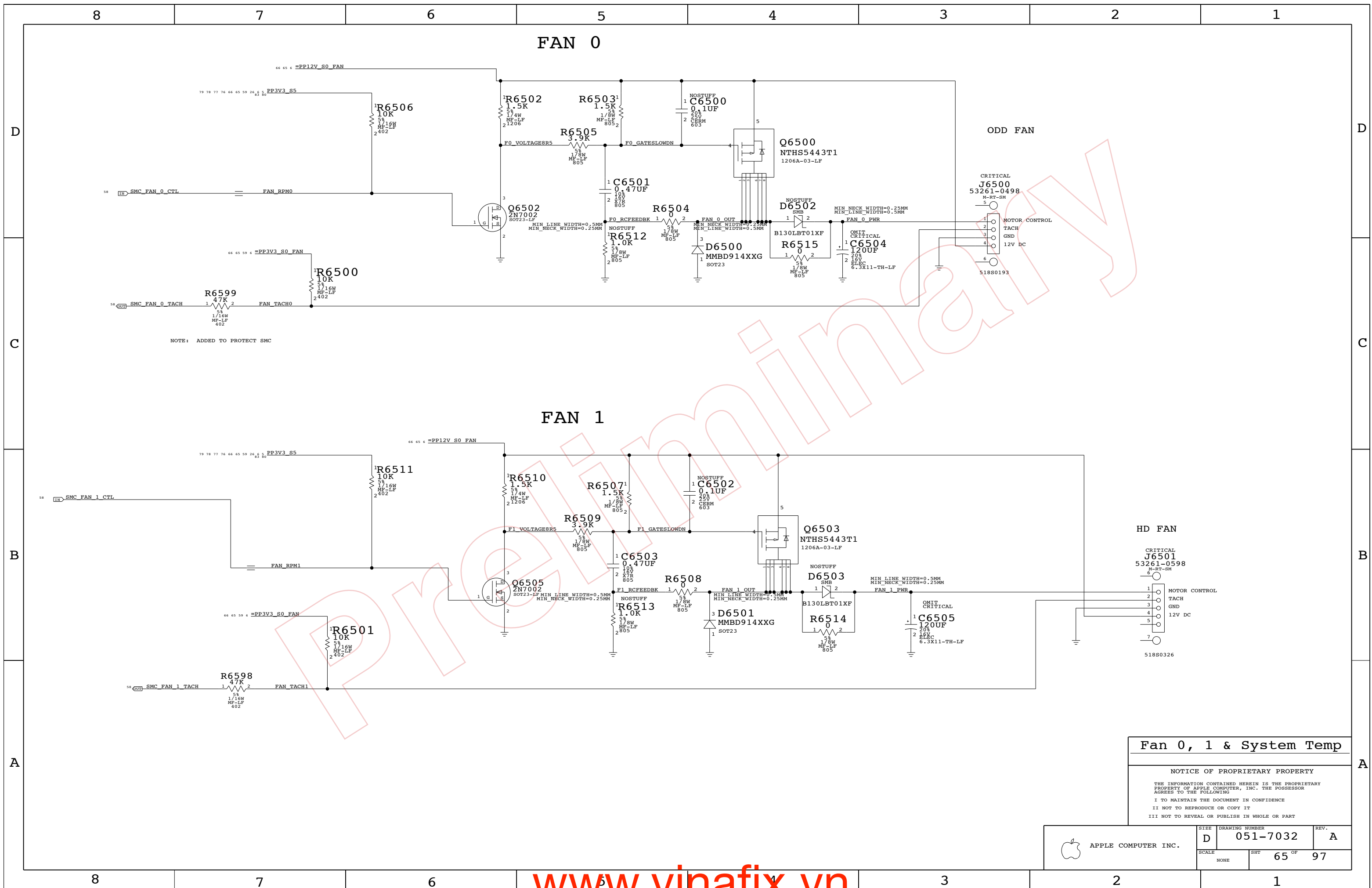
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	A
SCALE	SHT		OF
NONE	61		97



Preliminary

SPI BOOTROM
 SYNC_MASTER=M38 SYNC_DATE=01/05/2006
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SCALE	SHT		OF
NONE	63		97

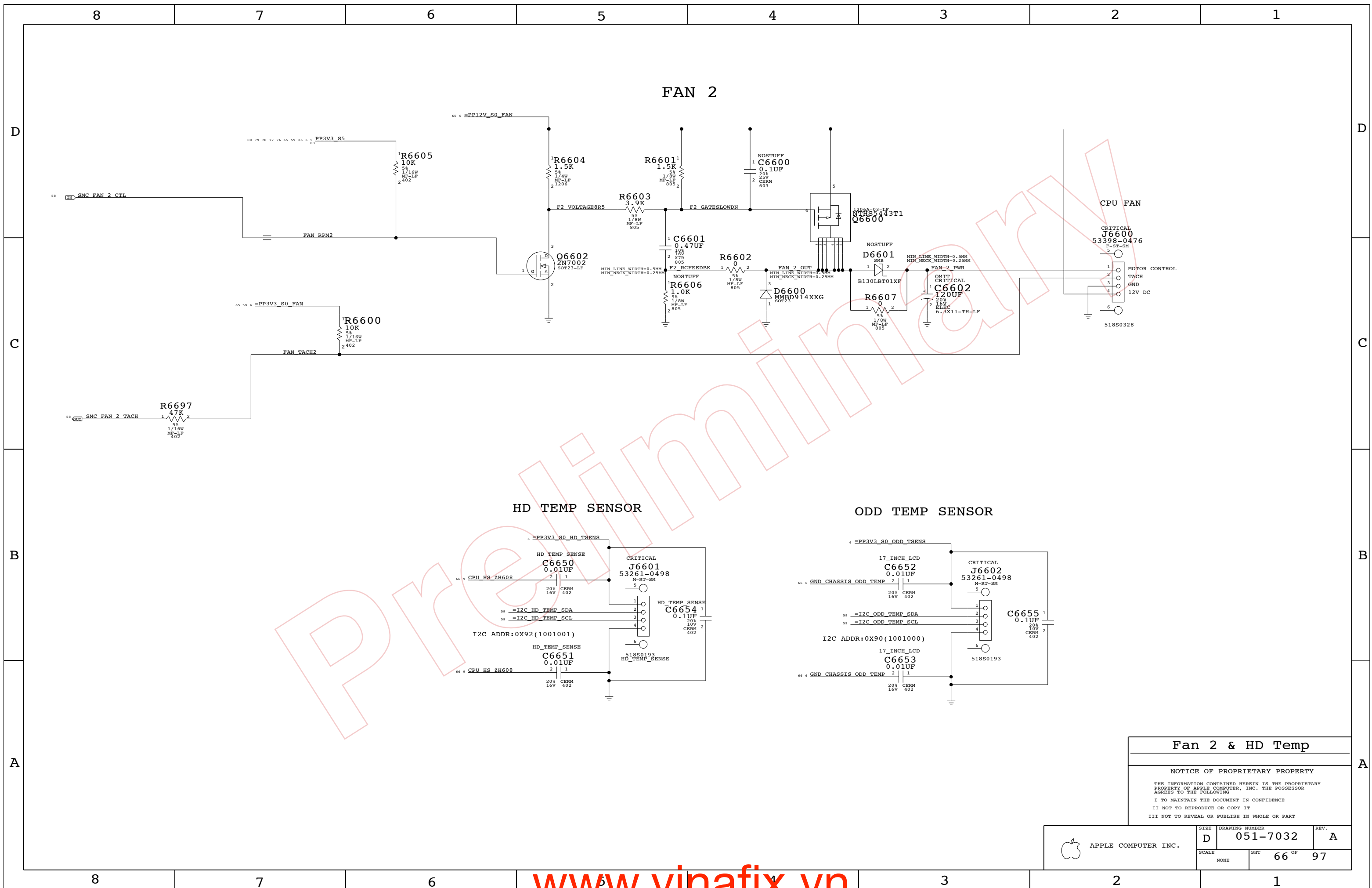


NOTE: ADDED TO PROTECT SMC

Fan 0, 1 & System Temp

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	D	051-7032	A
SCALE	SHT	65 OF	97
NONE			



Fan 2 & HD Temp

NOTICE OF PROPRIETARY PROPERTY

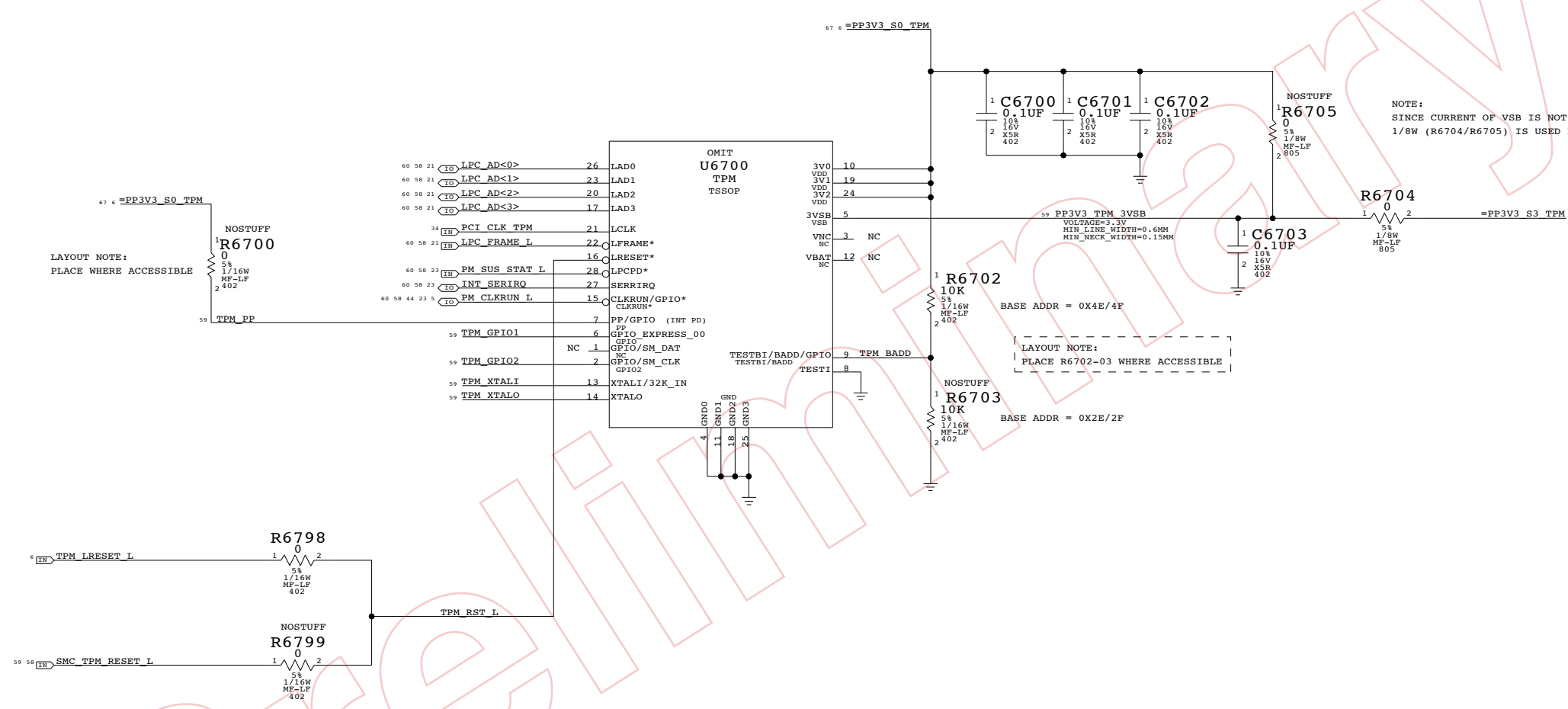
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	SCALE NONE	SHEET 66 OF 97	



TPM

SYNC_MASTER=M38 SYNC_DATE=01/05/2006

NOTICE OF PROPRIETARY PROPERTY

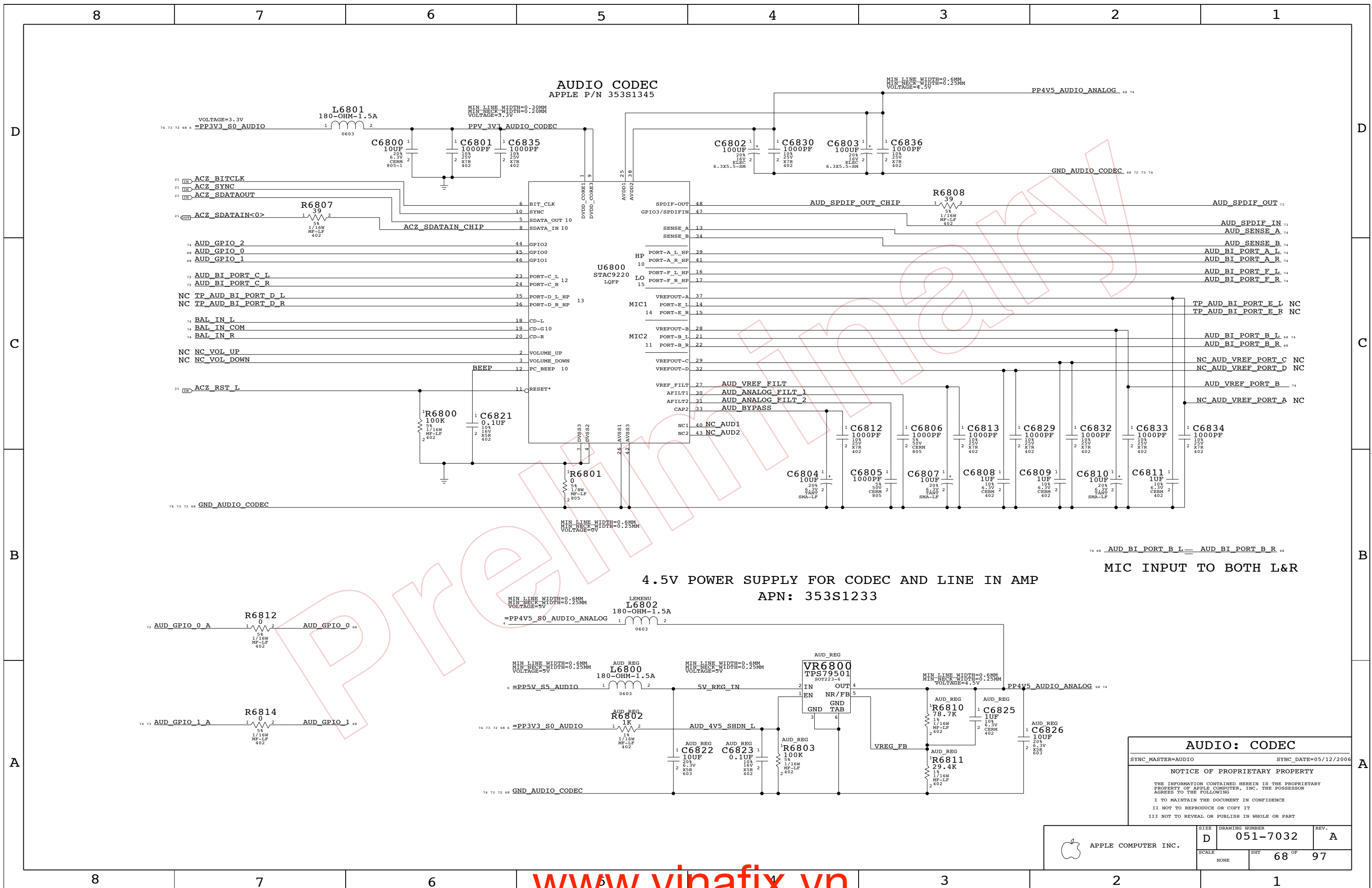
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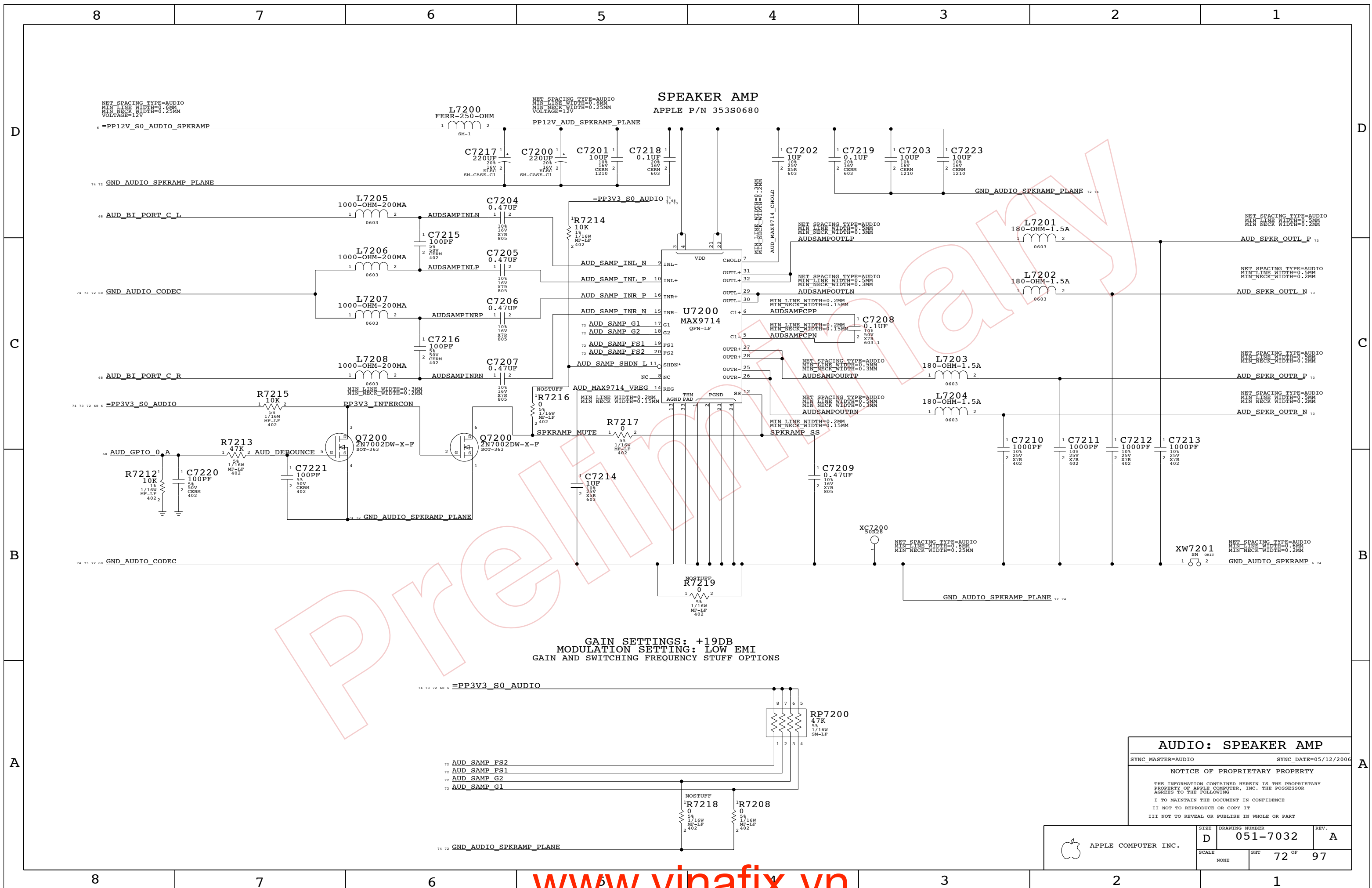
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	A
SCALE	SHT	67 OF 97	
NONE			



AUDIO: CODEC
 SYNC_MASTER=AUDIO SYNC_DATE=05/12/2006
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	A
SCALE	SHT	68 OF 97	
NONE			

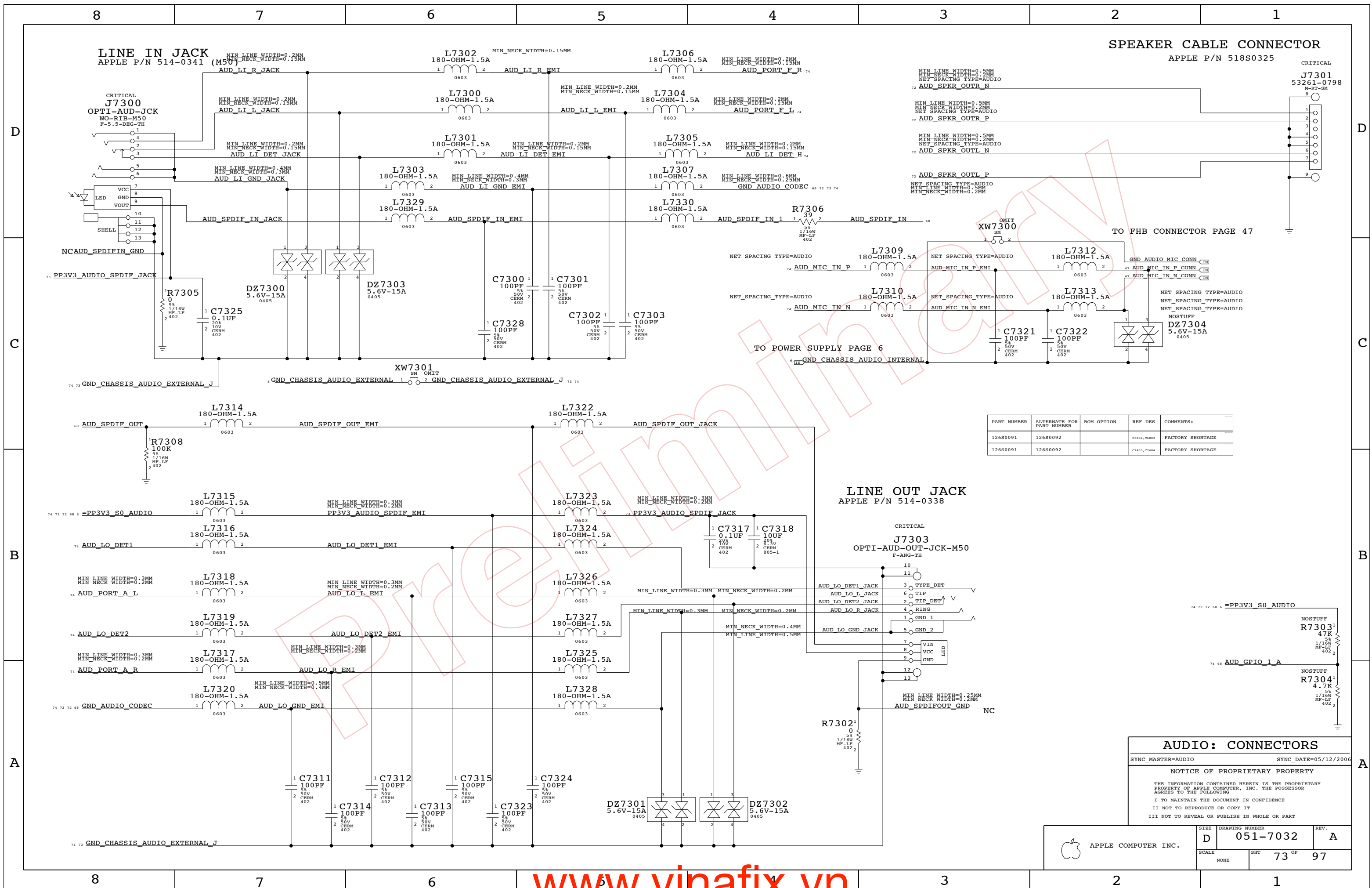


SPEAKER AMP
APPLE P/N 353S0680

GAIN SETTINGS: +19DB
MODULATION SETTING: LOW EMI
GAIN AND SWITCHING FREQUENCY STUFF OPTIONS

AUDIO: SPEAKER AMP
SYNC_MASTER=AUDIO SYNC_DATE=05/12/2006
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	D	051-7032	A
SCALE	SHT	72 OF	97
NONE			



SPEAKER CABLE CONNECTOR

APPLE P/N 518S0325

CRITICAL

J7301
53261-0798
M-RT-SM

LINE IN JACK
APPLE P/N 514-0341 (M50)

LINE OUT JACK
APPLE P/N 514-0338

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
126S0091	126S0092		C8802, C8803	FACTORY SHORTAGE
126S0091	126S0092		C7483, C7484	FACTORY SHORTAGE

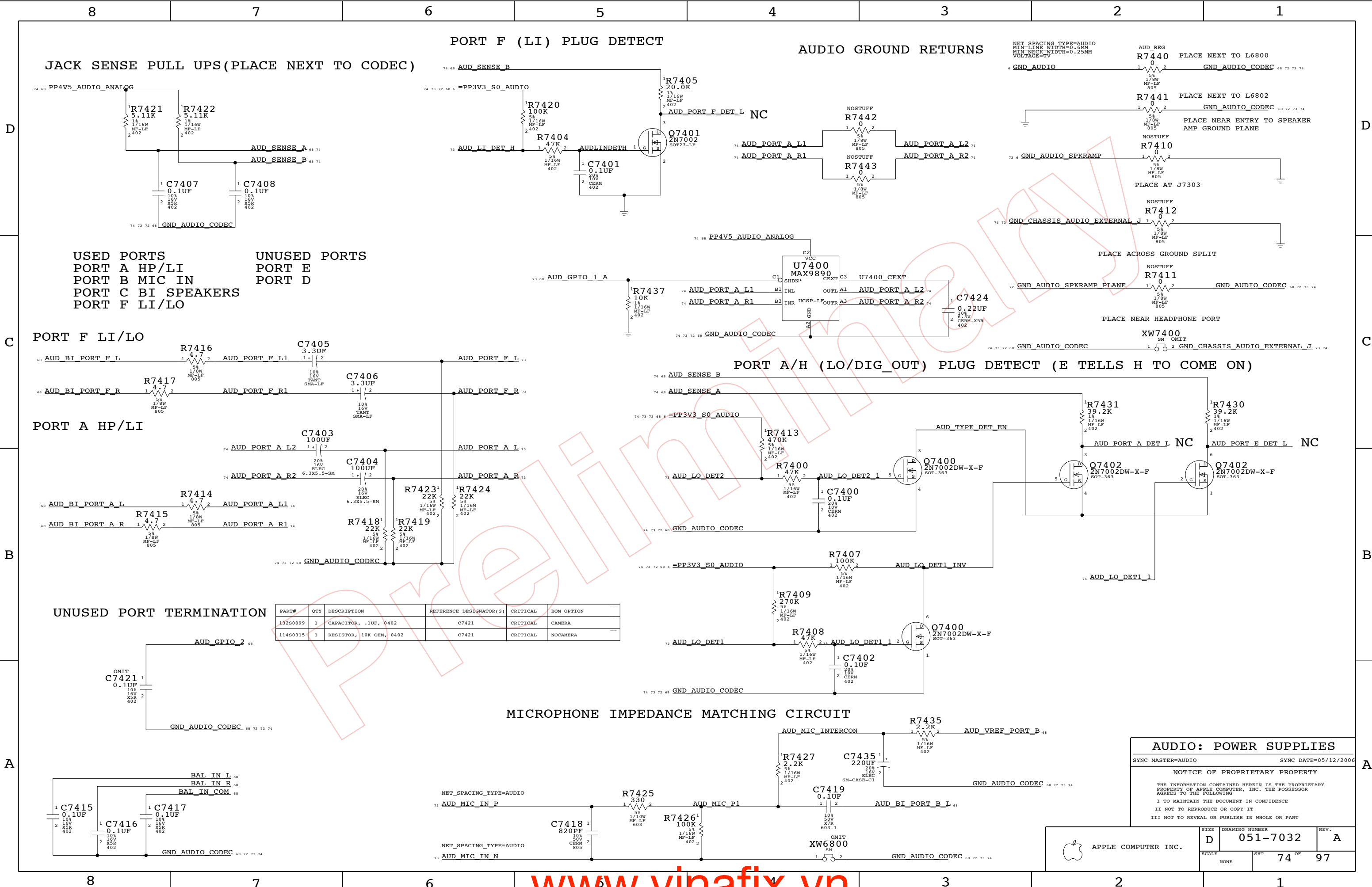
AUDIO: CONNECTORS

SYNC_MASTER=AUDIO SYNC_DATE=05/12/2006

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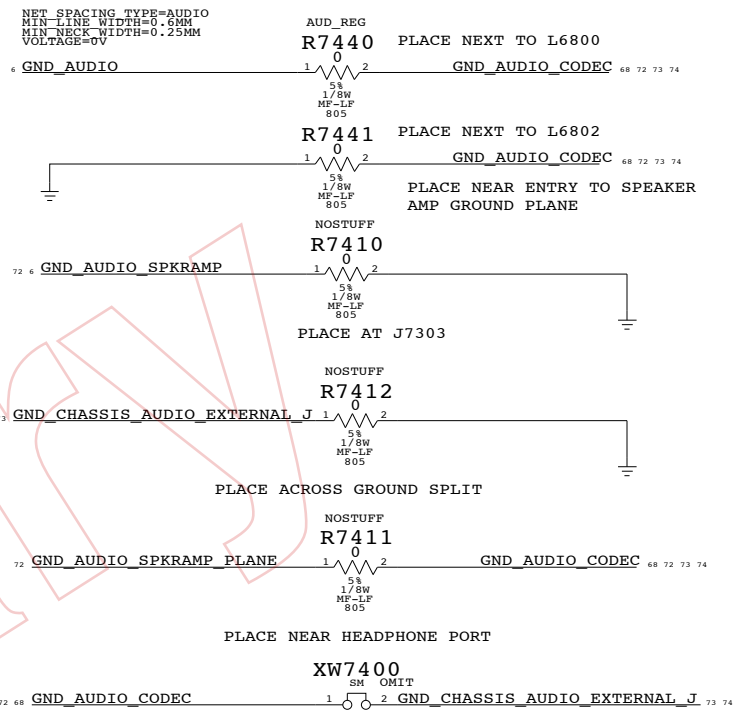
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	A
SCALE	SHT	73 OF	97
NONE			



JACK SENSE PULL UPS (PLACE NEXT TO CODEC)

PORT F (LI) PLUG DETECT

AUDIO GROUND RETURNS



USED PORTS
 PORT A HP/LI
 PORT B MIC IN
 PORT C BI SPEAKERS
 PORT F LI/LO

UNUSED PORTS
 PORT E
 PORT D

PORT F LI/LO

PORT A HP/LI

PORT A/H (LO/DIG_OUT) PLUG DETECT (E TELLS H TO COME ON)

UNUSED PORT TERMINATION

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
132S0099	1	CAPACITOR, .1UF, 0402	C7421	CRITICAL	CAMERA
11480315	1	RESISTOR, 10K OHM, 0402	C7421	CRITICAL	NOCAMERA

MICROPHONE IMPEDANCE MATCHING CIRCUIT

AUDIO: POWER SUPPLIES

SYNC_MASTER=AUDIO SYNC_DATE=05/12/2006

NOTICE OF PROPRIETARY PROPERTY

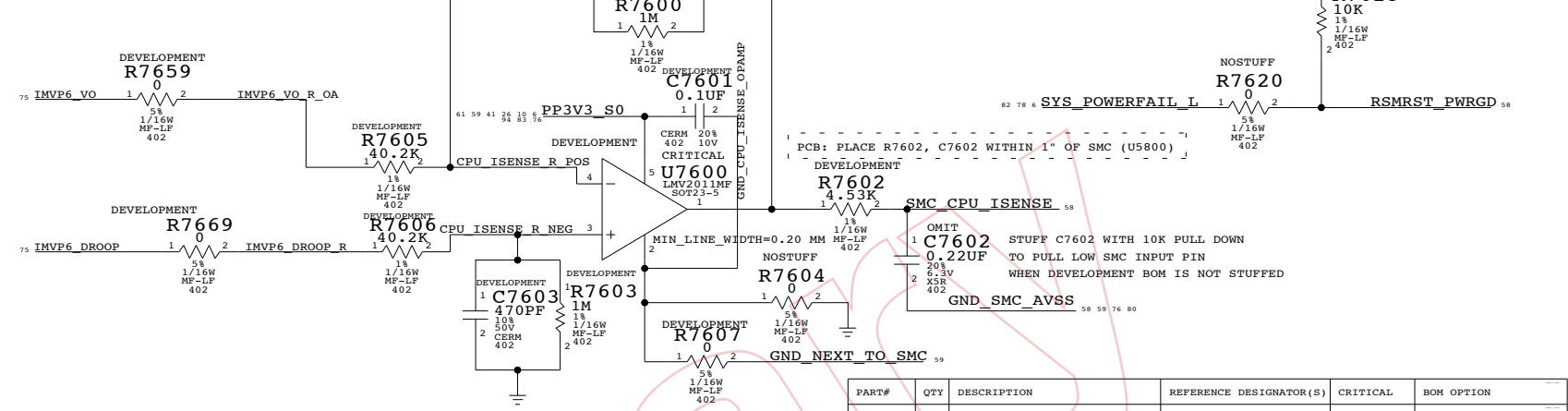
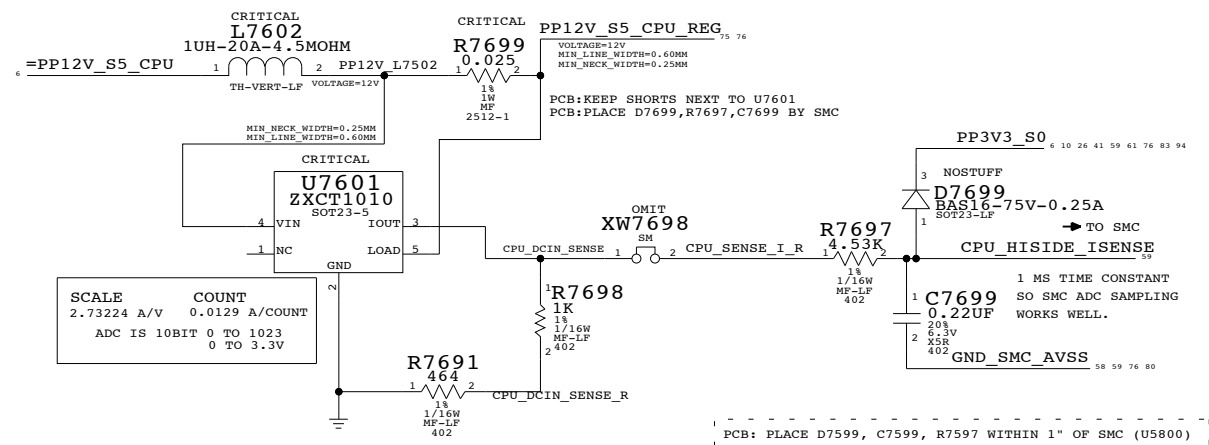
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	D	051-7032	A
SCALE	SHT	74 OF	97
NONE			

PROCESSOR VCORE CURRENT SENSE
(USING 12V INPUT CURRENT TO DERIVE CPU CURRENT)

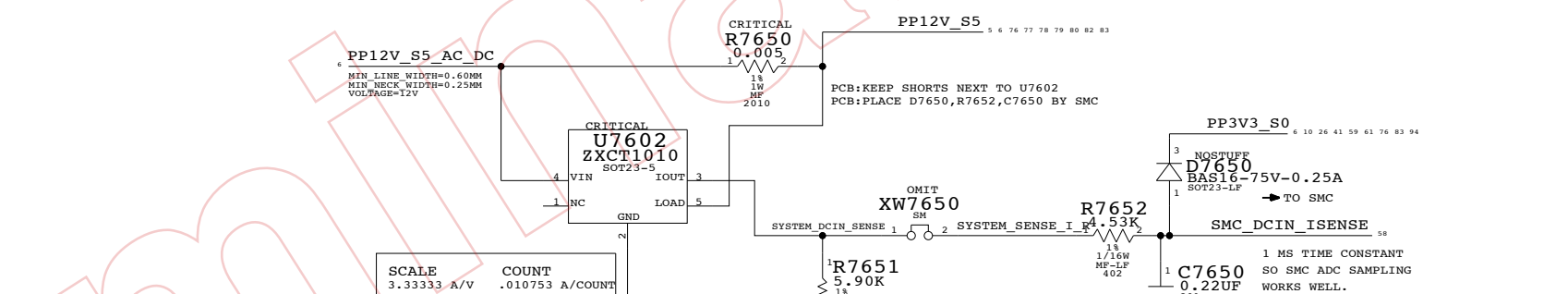
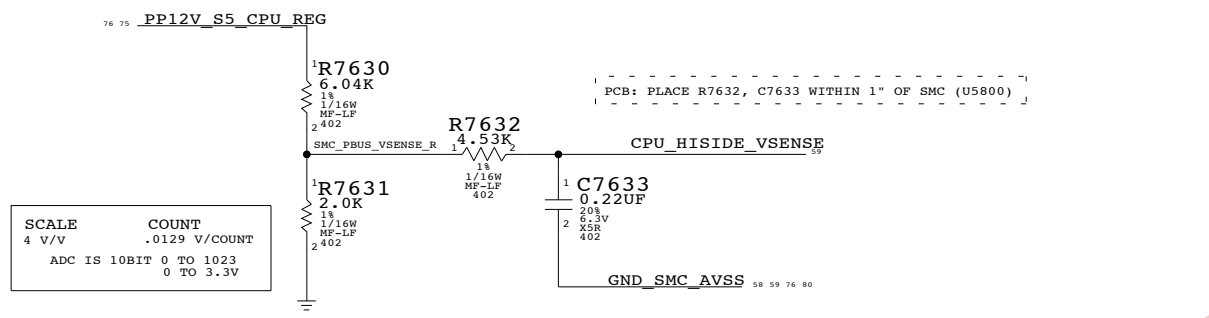
PROCESSOR VCORE CURRENT SENSE
(MEASURING DC/DC INDUCTOR DCR TO DERIVE CPU CURRENT)

SMC PWRGD PULLUP



PROCESSOR DCIN VOLTAGE SENSE
(SCALING 12V INPUT VOLTAGE TO SMC)

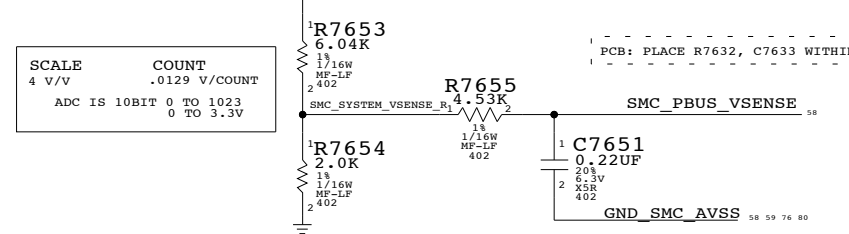
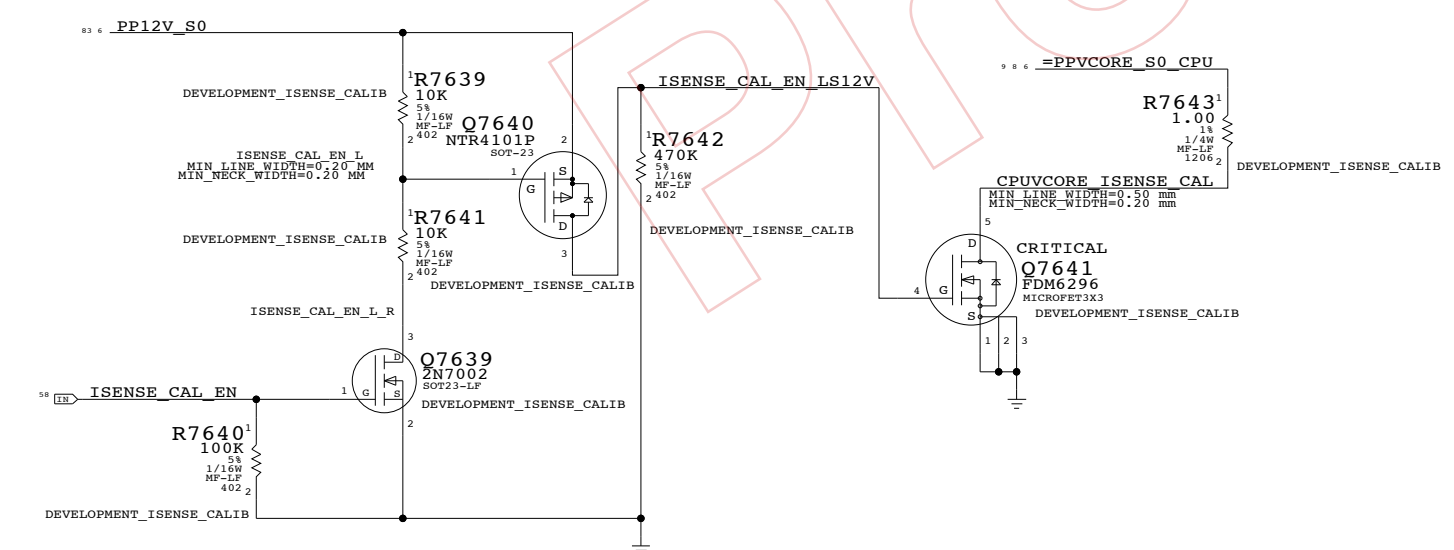
SYSTEM CURRENT SENSE



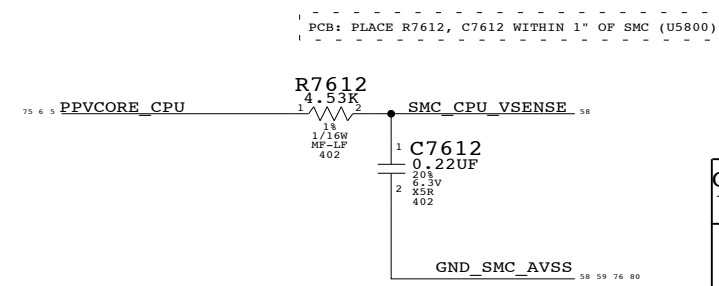
SYSTEM VOLTAGE SENSE
(SCALING 12V INPUT VOLTAGE TO SMC)

Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits



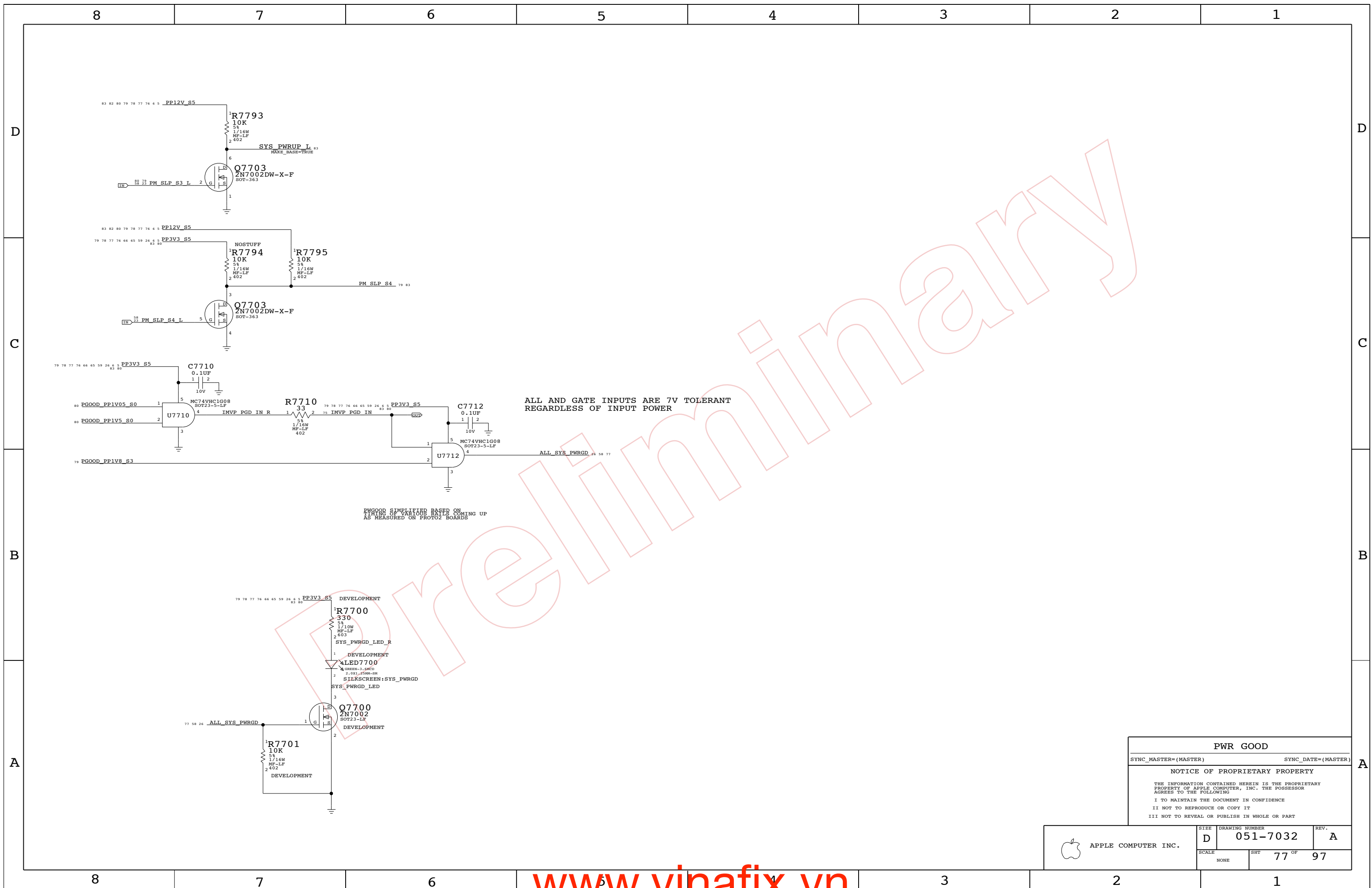
PROCESSOR VCORE SENSE



CPU & SYSTEM SENSE CIRCUITRIES

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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	D	051-7032	A
SCALE	SHT	76 OF	97
NONE			



PWR GOOD

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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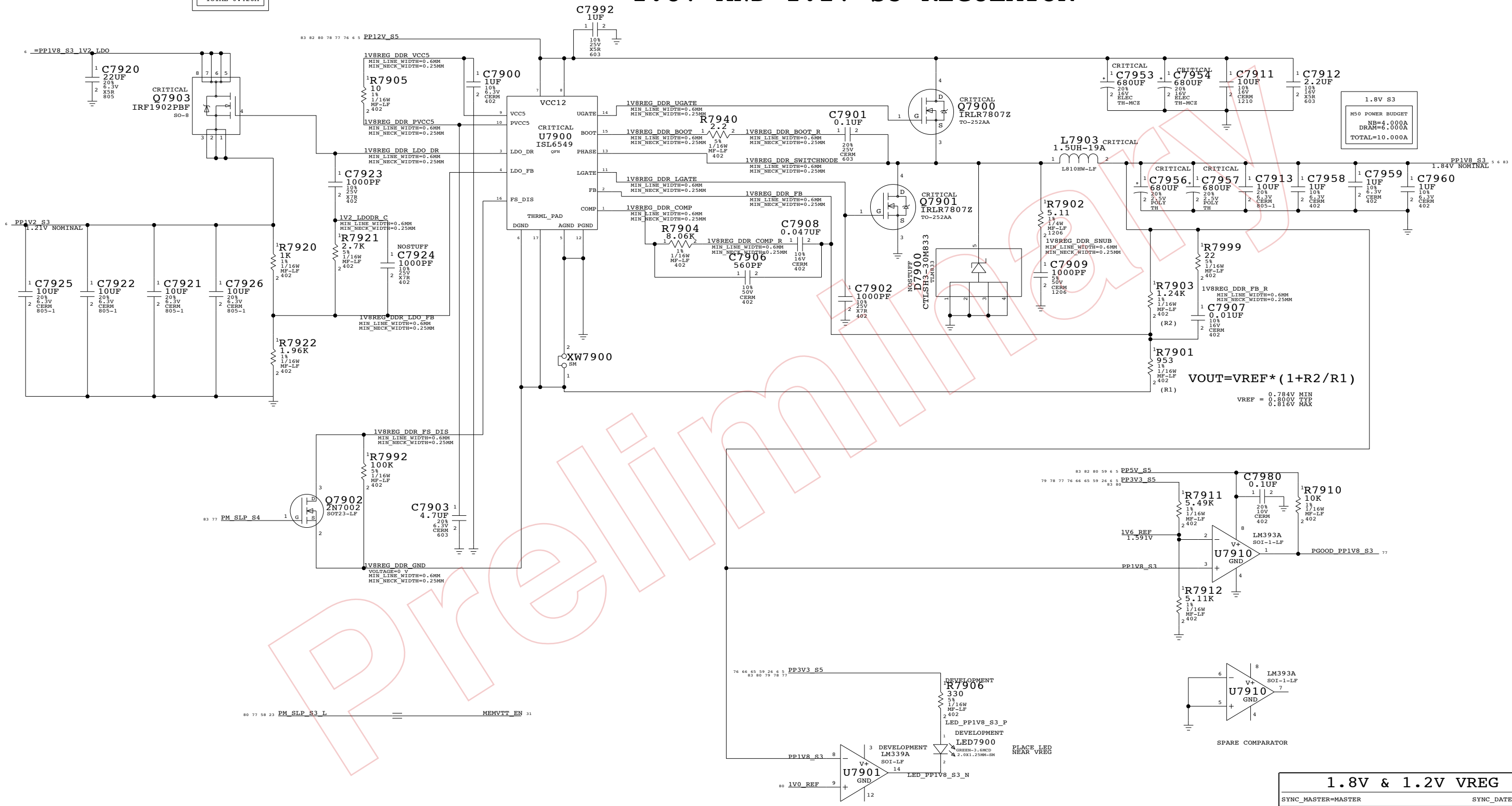
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	A
SCALE	SHT	77 OF	97
NONE			

1.8V AND 1.2V S3 REGULATOR

1.2V S3
M50 POWER BUDGET
YUKON=0.426A
TOTAL=0.426A

1.8V S3
M50 POWER BUDGET
NB=4.000A
DRAM=6.000A
TOTAL=10.000A



1.8V & 1.2V VREG

SYNC_MASTER=MASTER SYNC_DATE=MASTER

NOTICE OF PROPRIETARY PROPERTY

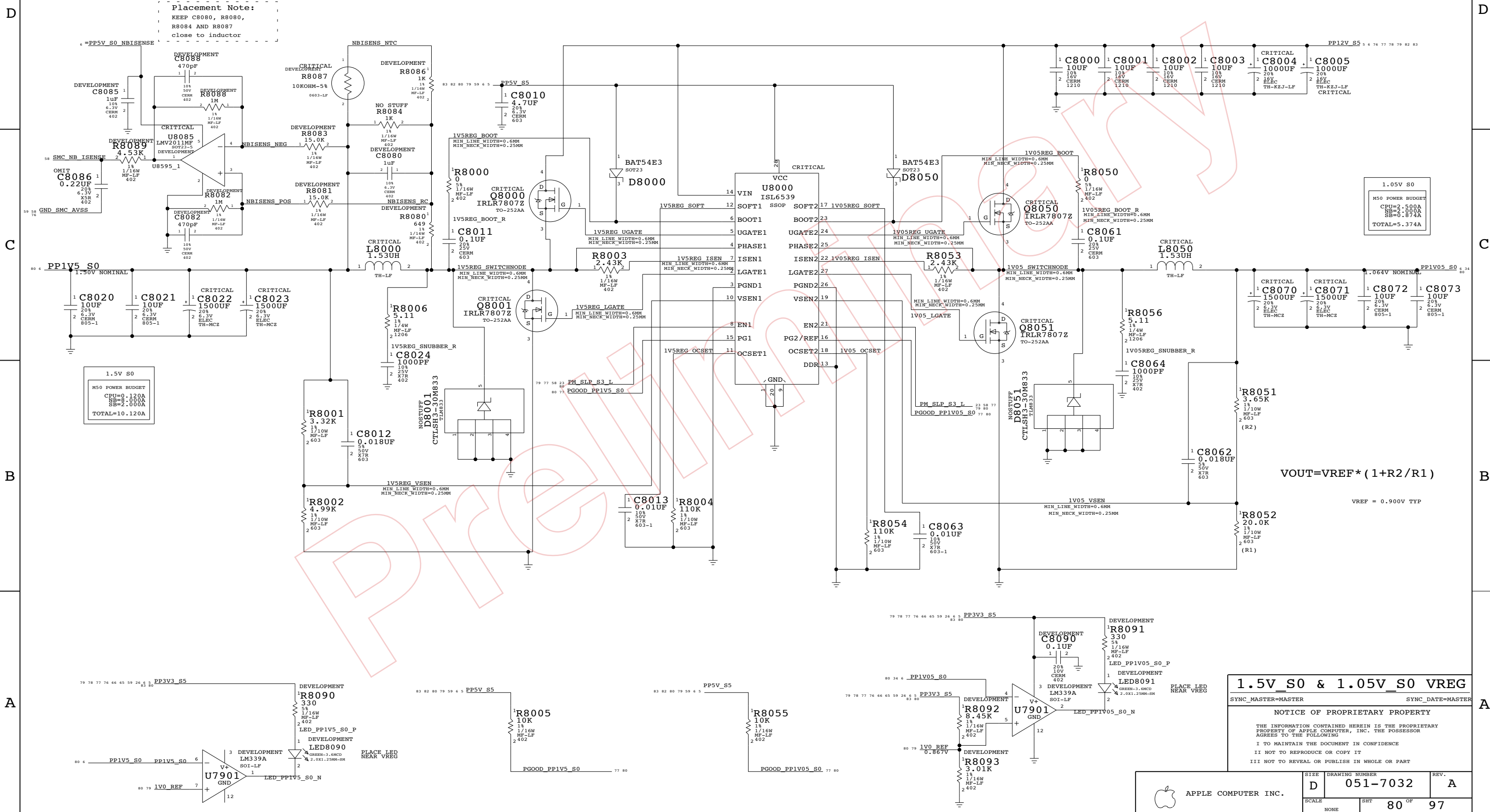
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	D	051-7032	A
SCALE	SHT	79 OF	97
NONE			

1.5V S0 AND 1.05V S0 RAILS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
13280080	1	CAP,0.22UF,6.3V,20%,0402	C8086		DEVELOPMENT
11650090	1	RES,10K,5%,0402	C8086		NOT_DEVELOPMENT

Placement Note:
KEEP C8080, R8080,
R8084 AND R8087
close to inductor



1.5V_S0 & 1.05V_S0 VREG

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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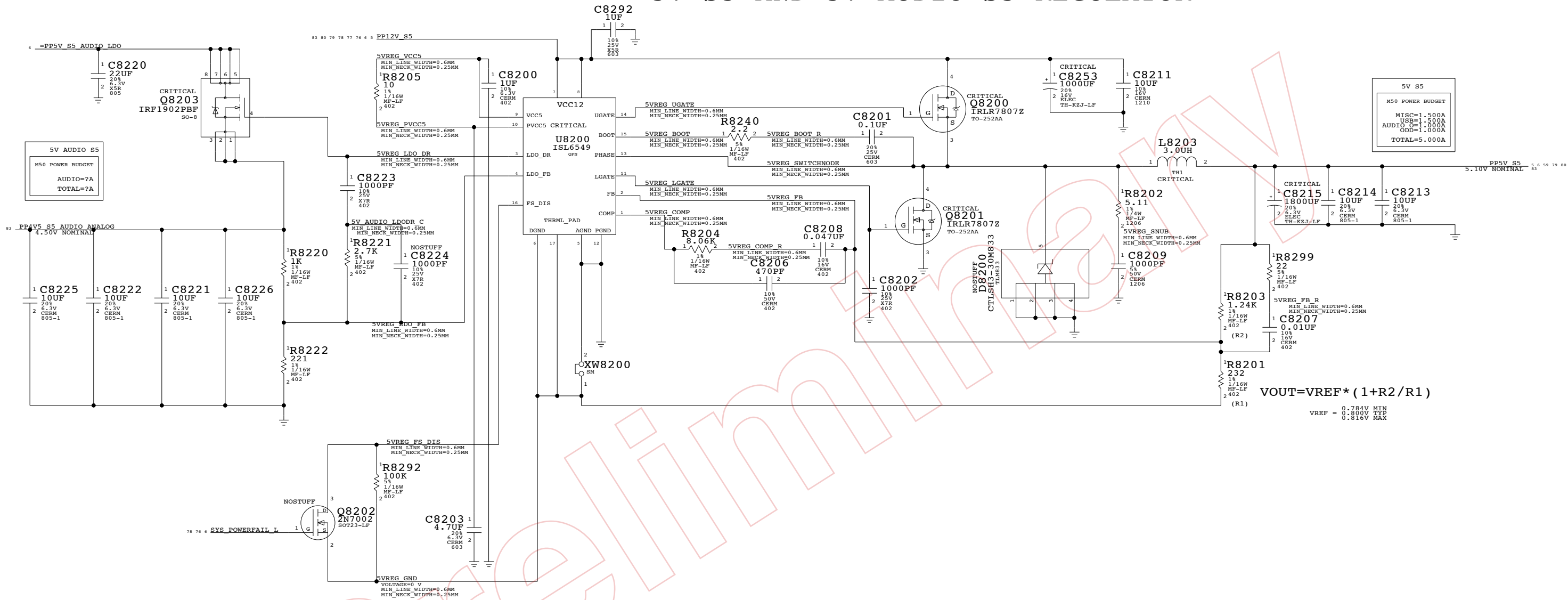
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	A
SCALE	SHT	80 OF	97
NONE			

5V S5 AND 5V AUDIO S5 REGULATOR



POWER SUPPLY 3.3V/5V MAIN SWITCH

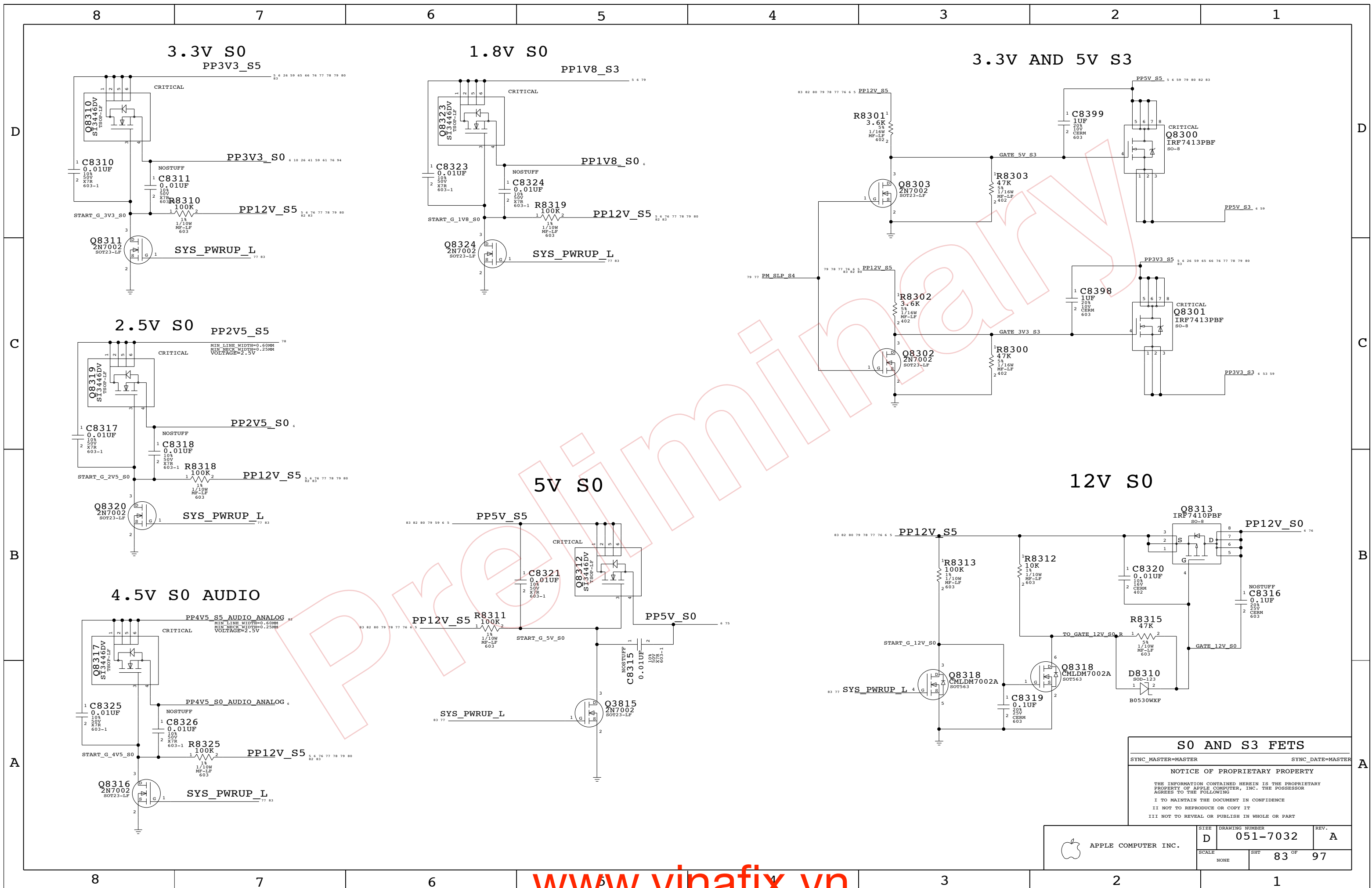
5V DC/DC

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	A
SCALE	SHT		REV.
NONE	82 OF 97		



S0 AND S3 FETS

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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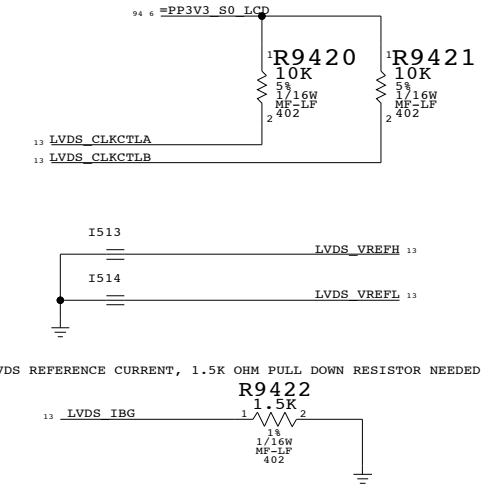
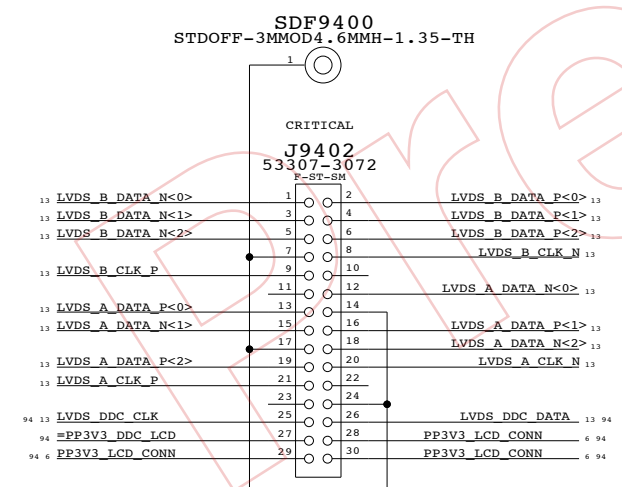
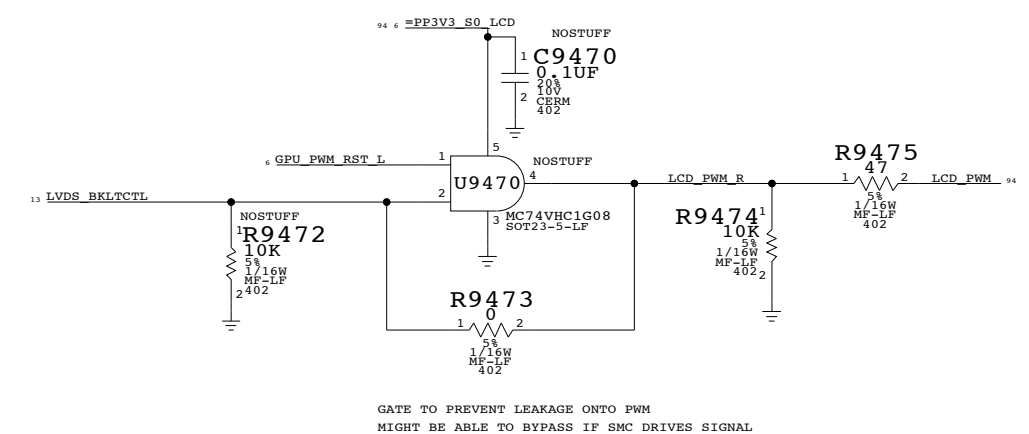
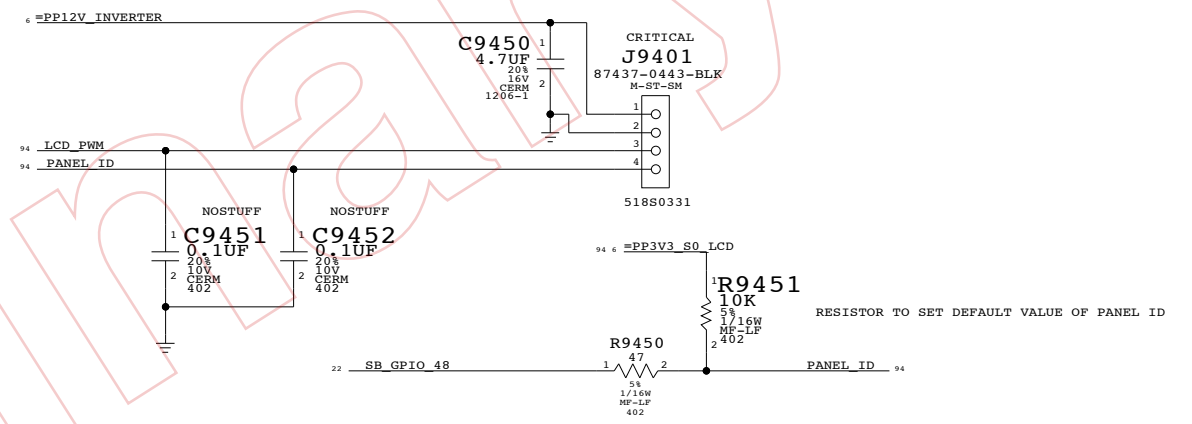
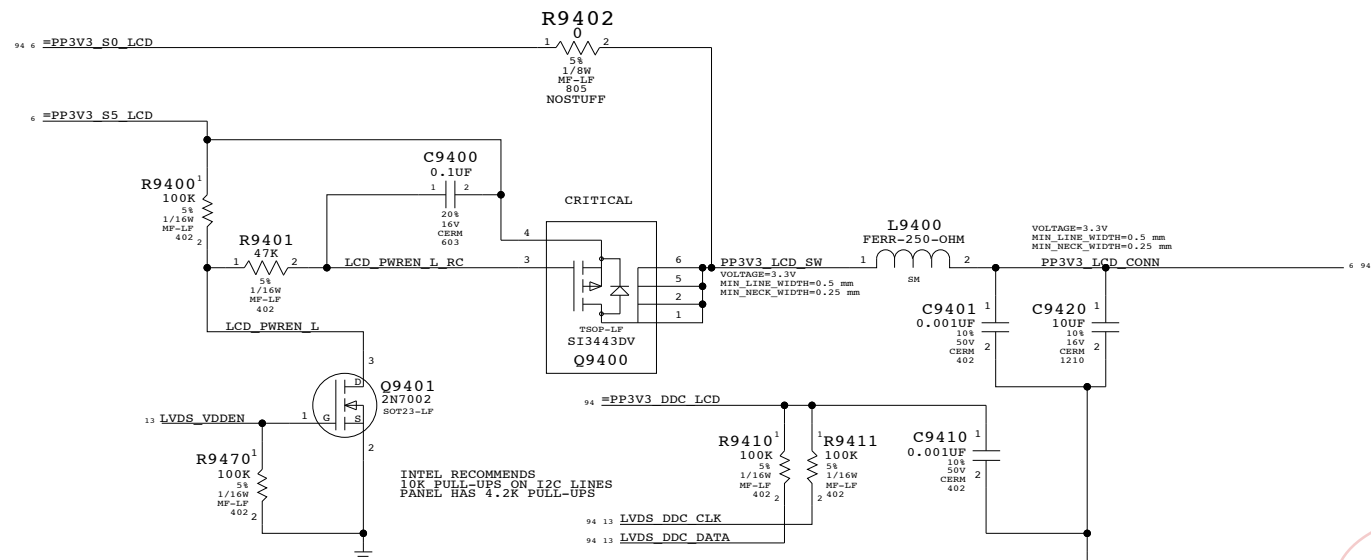
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	A
SCALE	SHT		REV.
NONE	83 OF 97		

LCD (LVDS) INTERFACE

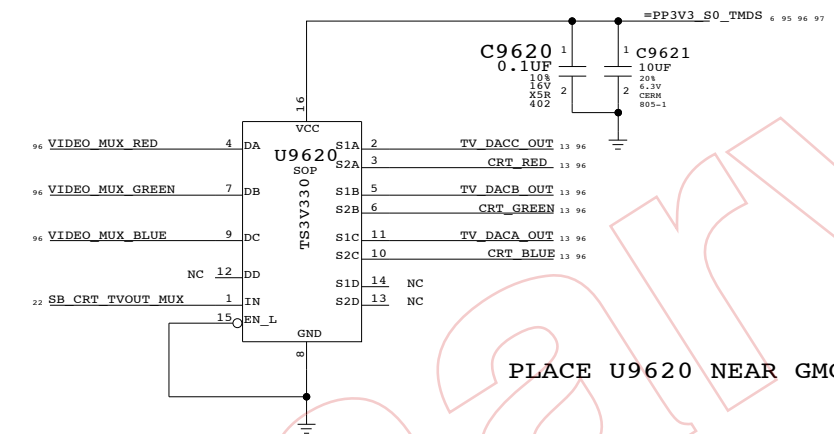
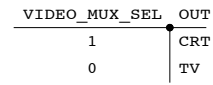
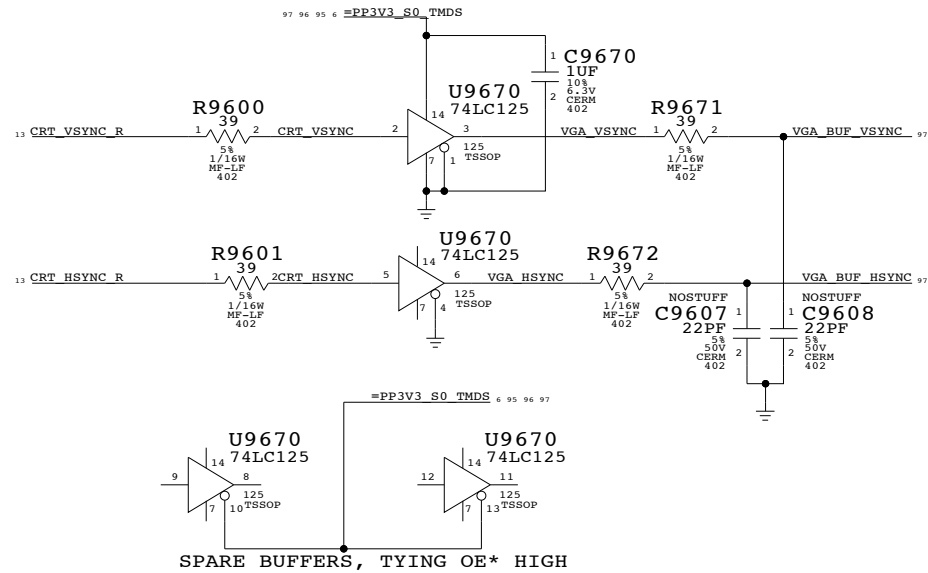
INVERTER INTERFACE



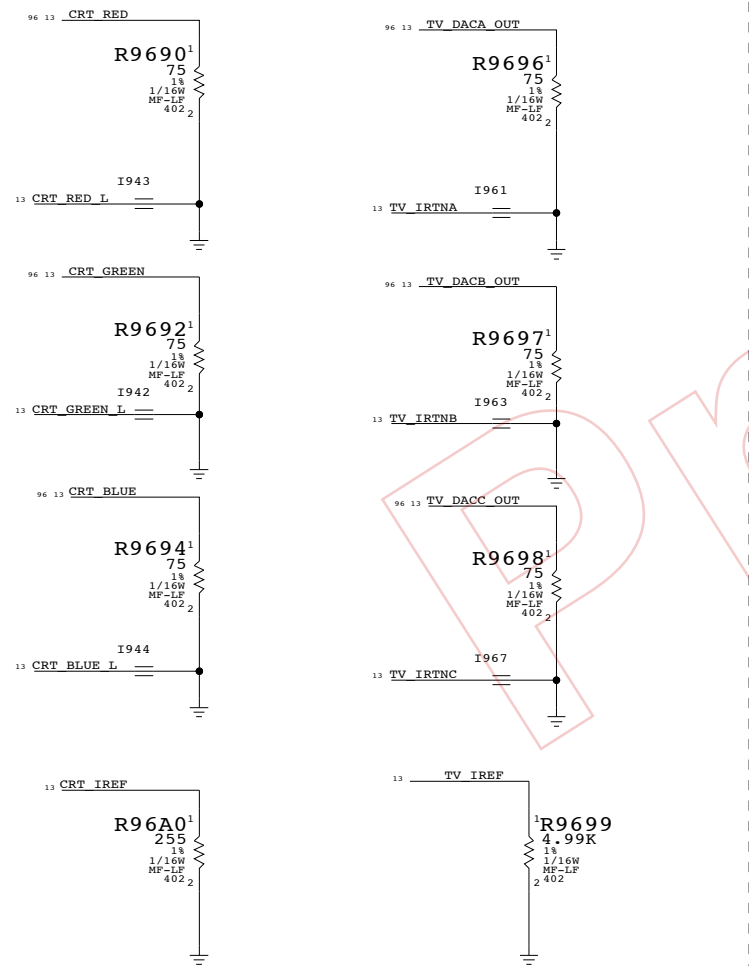
Internal Display Conns
 SYNC_MASTER=MASTER SYNC_DATE=MASTER
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	D	051-7032	A
SCALE	SHT		94 OF 97
NONE			

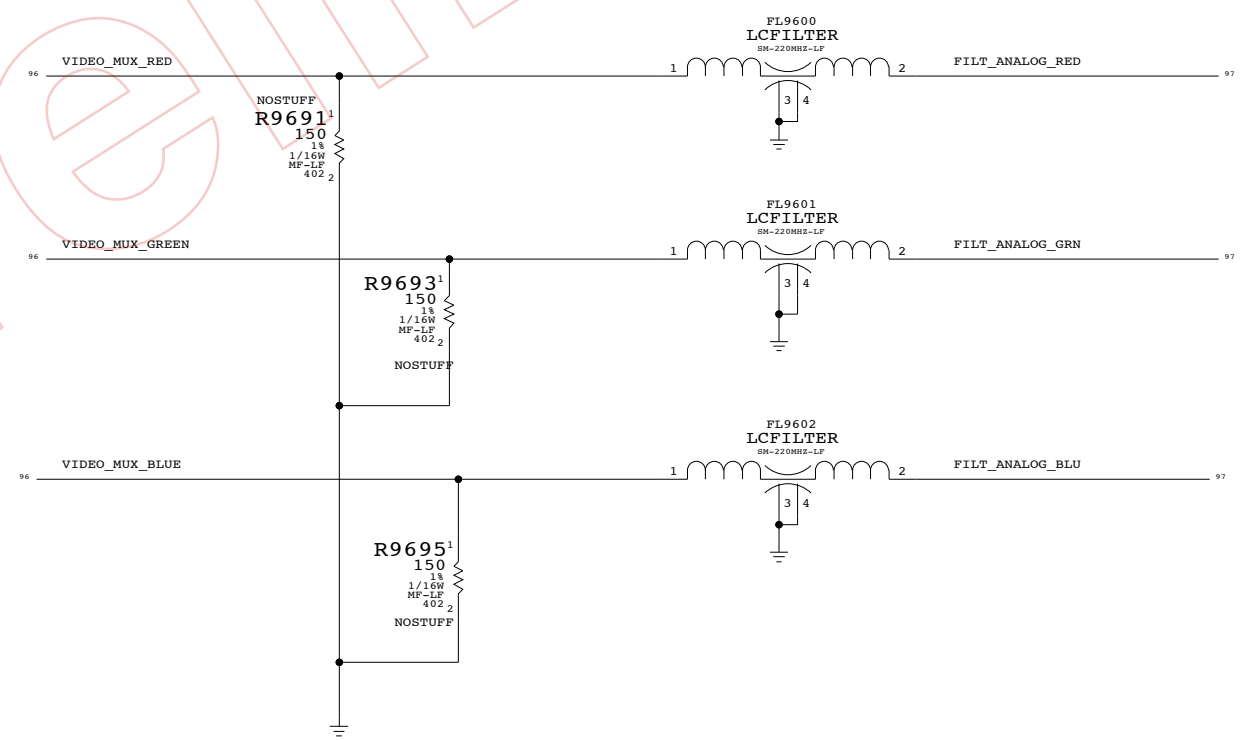
VGA SYNC BUFFERS



PLACE RESISTORS AT NORTHBRIDGE

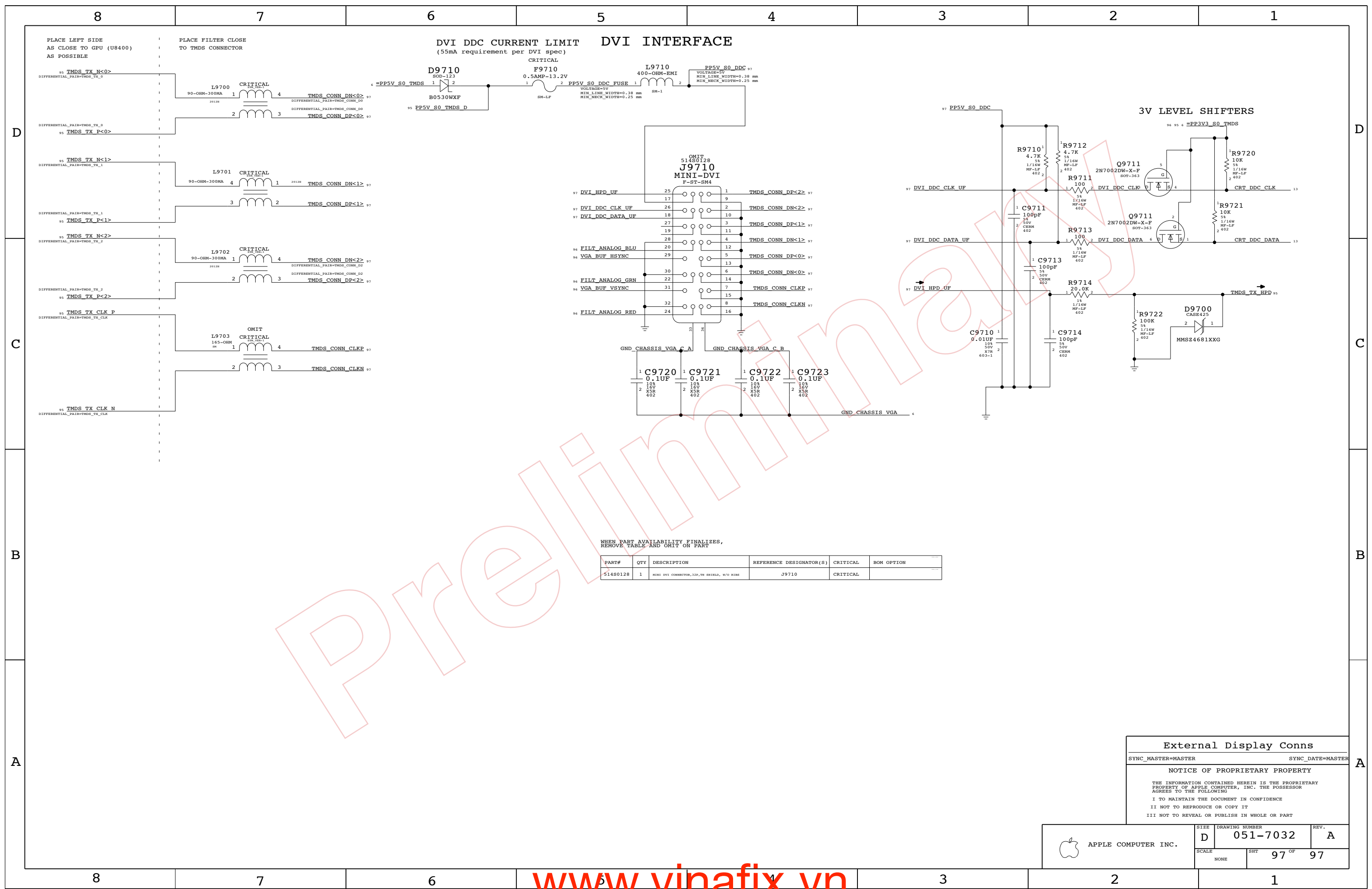


ANALOG FILTERING PLACE BY CONNECTOR



TMDS/Inverter/ExtVGA
 SYNC_MASTER=MASTER SYNC_DATE=MASTER
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	D	051-7032	A
SCALE	SHT	96 OF	97
NONE			



DVI DDC CURRENT LIMIT DVI INTERFACE
(55mA requirement per DVI spec)

514S0128
J9710
MINI-DVI
F-ST-SM4

WHEN PART AVAILABILITY FINALIZES,
REMOVE TABLE AND OMIT ON PART

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514S0128	1	MINI DVI CONNECTOR, 32P, TB SHIELD, W/O RING	J9710	CRITICAL	

External Display Conns
SYNC_MASTER=MASTER SYNC_DATE=MASTER

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