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**NEW 630 BOMS AS OF 9/7**

**CURRENT: REV D 10/17 SCH: REV G**
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<th>REFERENCE DES</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
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<tr>
<td>603-8960</td>
<td>IC,88E8053,GIGABIT ENET XCVR,64P QFN,NO</td>
<td>[EEE:WZC]</td>
<td>CRITICAL</td>
<td>CRITICAL</td>
</tr>
<tr>
<td>337S3392</td>
<td>IC,88E8053,GIGABIT ENET XCVR,64P QFN,NO</td>
<td>[EEE:WZC]</td>
<td>CRITICAL</td>
<td>CRITICAL</td>
</tr>
<tr>
<td>341T0020</td>
<td>IC,88E8053,GIGABIT ENET XCVR,64P QFN,NO</td>
<td>[EEE:WZC]</td>
<td>CRITICAL</td>
<td>CRITICAL</td>
</tr>
<tr>
<td>353S1465</td>
<td>IC,88E8053,GIGABIT ENET XCVR,64P QFN,NO</td>
<td>[EEE:WZC]</td>
<td>CRITICAL</td>
<td>CRITICAL</td>
</tr>
<tr>
<td>341S1789</td>
<td>IC,88E8053,GIGABIT ENET XCVR,64P QFN,NO</td>
<td>[EEE:WZC]</td>
<td>CRITICAL</td>
<td>CRITICAL</td>
</tr>
<tr>
<td>338S0270</td>
<td>IC,88E8053,GIGABIT ENET XCVR,64P QFN,NO</td>
<td>[EEE:WZC]</td>
<td>CRITICAL</td>
<td>CRITICAL</td>
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</table>

**CPU_TSENS_EXT, GPU_TSENS_INT, GPU_TSENS_EXT, MXM_ROM, NBCFG_PEG_REVERSE**

- CPU_TSENS_EXT
- GPU_TSENS_INT
- GPU_TSENS_EXT
- MXM_ROM
- NBCFG_PEG_REVERSE

**BATTERY IS INSTALLED AS PART**

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<th>REFERENCE DES</th>
<th>CRITICAL</th>
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</thead>
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<td>341S1797</td>
<td>IC,945PM,NORTHBRIDGE</td>
<td>[EEE:WZC]</td>
<td>CRITICAL</td>
<td>CRITICAL</td>
</tr>
<tr>
<td>359S0117</td>
<td>IC,945PM,NORTHBRIDGE</td>
<td>[EEE:WZC]</td>
<td>CRITICAL</td>
<td>CRITICAL</td>
</tr>
<tr>
<td>338S0328</td>
<td>IC,945PM,NORTHBRIDGE</td>
<td>[EEE:WZC]</td>
<td>CRITICAL</td>
<td>CRITICAL</td>
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**MEROM 2.16GHZ, M51**

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<th>PART NUMBER</th>
<th>DESCRIPTION</th>
<th>REFERENCE DES</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
</tr>
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<tr>
<td>337S3390</td>
<td>BT2600 CRITICAL</td>
<td>[EEE:WZC]</td>
<td>CRITICAL</td>
<td>CRITICAL</td>
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<td>946-0743</td>
<td>IO ALIGNMENT BOARD</td>
<td>[EEE:WZC]</td>
<td>CRITICAL</td>
<td>CRITICAL</td>
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<td>825-6447</td>
<td>IC,SB,652BGA</td>
<td>[EEE:WZC]</td>
<td>CRITICAL</td>
<td>CRITICAL</td>
</tr>
<tr>
<td>511S0025</td>
<td>IC,CPU_VREG,IMVP,TWO PHASE,SCREENED</td>
<td>[EEE:WZC]</td>
<td>CRITICAL</td>
<td>CRITICAL</td>
</tr>
<tr>
<td>421-0339</td>
<td>IC,88E8053,GIGABIT ENET XCVR,64P QFN,NO</td>
<td>[EEE:WZC]</td>
<td>CRITICAL</td>
<td>CRITICAL</td>
</tr>
<tr>
<td>421-0339</td>
<td>IC,88E8053,GIGABIT ENET XCVR,64P QFN,NO</td>
<td>[EEE:WZC]</td>
<td>CRITICAL</td>
<td>CRITICAL</td>
</tr>
<tr>
<td>421-0339</td>
<td>IC,88E8053,GIGABIT ENET XCVR,64P QFN,NO</td>
<td>[EEE:WZC]</td>
<td>CRITICAL</td>
<td>CRITICAL</td>
</tr>
<tr>
<td>421-0339</td>
<td>IC,88E8053,GIGABIT ENET XCVR,64P QFN,NO</td>
<td>[EEE:WZC]</td>
<td>CRITICAL</td>
<td>CRITICAL</td>
</tr>
<tr>
<td>421-0339</td>
<td>IC,88E8053,GIGABIT ENET XCVR,64P QFN,NO</td>
<td>[EEE:WZC]</td>
<td>CRITICAL</td>
<td>CRITICAL</td>
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**IC,88E8053,GIGABIT ENET XCVR,64P QFN,NO**

- CPU_PWR_SENSE
- MXM_PWR_SENSE
- SYS_PWR_SENSE

**NOSTUFF**

- CPU_PWR_SENSE
- MXM_PWR_SENSE
- SYS_PWR_SENSE

**BAR CODE LABLE, MLB, M51**

- BAR CODE LABLE, MLB, M51
- BAR CODE LABLE, MLB, M51
- BAR CODE LABLE, MLB, M51

**COMMENTS:**

- CPU VREG NEW REV
- GREEN LED ALT.
- SANYO ALT
- SANYO ALT for Nich.
ON L8 (NORTH SIDE SECONDARY) PLACE INSIDE SOCKET CAVITY
SOUTH SIDE SECONDARY PLACE 6 INSIDE SOCKET SECONDARY) CAVITY ON L8 (SOUTH SIDE SECONDARY

WE HAD A 330UF ELEC CAP HERE FOR 1.05V RAIL - CHECK WE CAN REMOVE

CPU HEATSINK MOUNTING HOLES

VCC CORE DECOUPLING
PLACE IN SOCKET CAVITY (NORTH SIDE SECONDARY)
PLACE IN SOCKET CAVITY (SOUTH SIDE SECONDARY)

VCC CORE DECOUPLING
PLACE IN SOCKET CAVITY (NORTH SIDE SECONDARY)
PLACE IN SOCKET CAVITY (SOUTH SIDE SECONDARY)

CPU DECAPS & VID<>

051-7039 H
CPU ITP700FLEX DEBUG SUPPORT

ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S TCK PIN AND THEN FENCE BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX CONNECTOR'S FBO PIN.
These 0.1uF caps should be close to MCH.

Layout Note: Route to caps, then GND.

MIN_LINE_WIDTH = 1.0 mm
MIN_NECK_WIDTH = 0.2 mm

Layout Note:

MIN_LINE_WIDTH = 1.0 mm
MIN_NECK_WIDTH = 0.2 mm

Layout Note: Place L and C close to MCH.
ICH7-M SMBus Connections

SMC "0" SMBus Connections

SMC "A" SMBus Connections

SMC "B" SMBus Connections

Unused SMC "Battery A/B" SMBus

SMC "B" SMBus Connections

SMC "A" SMBus Connections

SMC "0" SMBus Connections

ICH7-M SMBus Connections

SMC "B" SMBus Connections

SMC "A" SMBus Connections

SMC "0" SMBus Connections

ICH7-M SMBus Connections
DDR2 VRef
Use 1.1uF per connector

C2800
0.1uF
10V
X5R
20%

C2801
0.1uF
10V
X5R
20%

C2802
0.1uF
10V
X5R
20%

C2803
0.1uF
10V
X5R
20%

C2804
0.1uF
10V
X5R
20%

C2810
0.1uF
10V
X5R
20%

C2812
0.1uF
10V
X5R
20%

C2813
0.1uF
10V
X5R
20%

C2817
0.1uF
10V
X5R
20%

C2818
0.1uF
10V
X5R
20%

C2819
0.1uF
10V
X5R
20%

C2820
0.1uF
10V
X5R
20%

C2821
0.1uF
10V
X5R
20%
NOTE: This page does not supply VREF.

BOM options provided by this page:
- =I2C_MEM_SDA
- =I2C_MEM_SCL
- =PP1V8_S3_MEM

Power aliases required by this page:

- C2951 6.3V 603 10%
- C2952 28V 402 2%
- CERM 6.3V 10%
- DQ59
- DQ58
- VSS53
- DQ57
- VSS51
- DQ50
- DQ49
- DQ48
- VSS41
- VSS36
- DQ33
- VSS31
- VSS32

- DQ62
- DQ61
- DQ60
- DQ52
- DQ46
- DQ45
- DQ38
- DQ37
- DQ36
- OD    T0
- VDD9
- DQ31
- DQ30
- DQ21
- DQ15
- DQ13
- DQ4
- VREF
- NC
- R2900
- Resistor prevents pwr-gnd short

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PRELIMINARY
DDR2 Vtt Regulator

If power inputs are not S0, MEMVTT_EN can be used to disable MEMVTT in sleep.

Power aliases required by this page:
- =PP5V_S0_MEMVTT
- =PP1V8_S0_MEMVTT
- =PP0V9_S0_MEMVTT_LDO

MemVtt supply:
=PP1V8_S0_MEMVTT
=PP0V9_S0_MEMVTT_LDO

Vref =PP5V_S0_MEMVTT
Vtt =PP1V8_S0_MEMVTT
Vtt_in =PP0V9_S0_MEMVTT_LDO

Signal aliases required by this page:
- MEMVTT_EN:
  - MEMVTT_EN_PU

BOM options provided by this page:
- C3101: 805-1 CERM 10uF 20% 6.3V
- C3102: 805-1 CERM 10uF 20% 6.3V
- C3105: 6.3V POLY 20% 150uF SMC-LF CRITICAL
- R3100: 5% 1/16W MF-LF 402 1K
- R3101: 1% 221 1/16W MF-LF 402
- C3109: 6.3V 2.2UF 10% CERM1 603
- C3110: 20% 0.1UF 10V CERM 402
- C3100: 402 CERM 1uF 10% 6.3V

Memory Vtt Supply

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PCI-E X1 PORT "A" = ETHERNET (YUKON)
- PCIE_A_R2D_C_P
- PCIE_A_R2D_C_N
- PCIE_A_D2R_P
- PCIE_A_D2R_N
- PCIE_AIRPORT_R2D_C_P
- PCIE_AIRPORT_R2D_C_N
- PCIE_AIRPORT_D2R_P
- PCIE_AIRPORT_D2R_N
- PCIE_C_R2D_C_P
- PCIE_C_R2D_C_N
- PCIE_C_D2R_P
- PCIE_C_D2R_N
- PCIE_D_R2D_C_P
- PCIE_D_R2D_C_N
- PCIE_D_R2D_P
- PCIE_D_R2D_N
- PCIE_D_D2R_P
- PCIE_D_D2R_N
- PCIE_E_R2D_C_P
- PCIE_E_R2D_C_N
- PCIE_E_R2D_P
- PCIE_E_R2D_N
- PCIE_E_D2R_P
- PCIE_E_D2R_N
- PCIE_F_R2D_C_P
- PCIE_F_R2D_C_N
- PCIE_F_R2D_P
- PCIE_F_R2D_N
- PCIE_F_D2R_P
- PCIE_F_D2R_N

PCI-E X1 PORT "B" = MINI CARD (AIRPORT)
- PCIE_B_R2D_C_P
- PCIE_B_R2D_C_N
- PCIE_B_D2R_P
- PCIE_B_D2R_N
- PCIE_AIRPORT_R2D_C_P
- PCIE_AIRPORT_R2D_C_N
- PCIE_AIRPORT_D2R_P
- PCIE_AIRPORT_D2R_N

PCI-E X1 PORTS C, D, E, F = UNUSED
- PCIE_C_R2D_C_P
- PCIE_C_R2D_C_N
- PCIE_C_D2R_P
- PCIE_C_D2R_N
- PCIE_D_R2D_C_P
- PCIE_D_R2D_C_N
- PCIE_D_R2D_P
- PCIE_D_R2D_N
- PCIE_D_D2R_P
- PCIE_D_D2R_N
- PCIE_E_R2D_C_P
- PCIE_E_R2D_C_N
- PCIE_E_R2D_P
- PCIE_E_R2D_N
- PCIE_E_D2R_P
- PCIE_E_D2R_N
- PCIE_F_R2D_C_P
- PCIE_F_R2D_C_N
- PCIE_F_R2D_P
- PCIE_F_R2D_N
- PCIE_F_D2R_P
- PCIE_F_D2R_N
R6306-07 SHOULD BE PLACED LESS THAN 2.54MM FROM U2100
R6303 SHOULD BE PLACED LESS THAN 2.54MM FROM U6301
CPU CURRENT SENSE CALIBRATION CIRCUIT

Switches in fixed load on power supplies to calibrate current sense circuits.
ALL AND GATE INPUTS ARE 7V TOLERANT REGARDLESS OF INPUT POWER

A

B

C

D

G

D

S

G

D

S

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G

D

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DRAWING NUMBER

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Split 12V S0 is for better power plane structure. 12VSS - will connect to +5.0V, GND
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Page Notes

Signal aliases required by this page:

- = PP3V3_S0_VIDEO
- = PP12V_LCD

Power aliases required by this page:

- = PP24V_INVERTER

(B) MXM also has 2.2K pull-ups

Panel has 4.7K DDC pull-ups

BOM options provided by this page:

- PINS 6-9 (GND) are connected to LCD chassis

- LCD (LVDS) INTERFACE

- PANEL POWER SEQUENCING

- PLACE NEAR J9402

- CRITICAL

1 SDF9400

2 SDF9401

- LCD_PWREN_L

- LCD_PWREN_DIV

- GPU_DIGON

- LVDS_U_DATA_N<0>

- LVDS_U_DATA_N<1>

- LVDS_U_DATA_N<2>

- LVDS_U_DATA_N<3>

- LVDS_U_CLK_P

- LVDS_L_DATA_P<0>

- LVDS_L_DATA_P<1>

- LVDS_L_DATA_P<2>

- LVDS_L_DATA_P<3>

- LVDS_L_CLK_P

- LVDS_L_CLK_N

- LVDS_U_CLK_N

- LVDS_U_DATA_P<0>

- LVDS_U_DATA_P<1>

- LVDS_U_DATA_P<2>

- LVDS_U_DATA_P<3>

- GPU_DDC_C_DATA

- GPU_DDC_C_CLK

- LCD_PWM

- LCD_PWREN_L_RC

- PP12V_LCD_CONN

- MIN_NECK_WIDTH=0.25 mm

- MIN_LINE_WIDTH=0.5 mm

- VOLTAGE=12V

- PP12V_LCD_SW

- LCD_PWREN_DIV

- PPV_S0_VIDEO

- PPV_S0_INVERTER

- INV_ENABLE_BL

- GPU_VARY_BL

- SYNC_DATE=(MASTER)

- SYNC_MASTER=M51_DAVE

- 051-7039

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