1. **All resistance values are in ohms, 0.1 watt +/- 5%.**

2. **All capacitance values are in microfarads.**

3. **All crystals & oscillator values are in hertz.**

---

**CIRCUIT**

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Power Block Diagram

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<table>
<thead>
<tr>
<th>PART#</th>
<th>DESCRIPTION</th>
<th>QTY</th>
<th>REFERENCE DESIGNATOR(S)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>CPU CRITICAL</td>
<td>1</td>
<td>2P16_CPU2.16GHZ MEROM</td>
</tr>
<tr>
<td>B</td>
<td>GPU_VCORE_1P2V</td>
<td>1</td>
<td>GPU_B26_LP</td>
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<tr>
<td>C</td>
<td>20_INCH_LCDIC</td>
<td>1</td>
<td>20_INCH_LCDMLB1</td>
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<td>D</td>
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<td>1</td>
<td>20_INCH_LCD341T0036</td>
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<td>E</td>
<td>EFI ROM,M60</td>
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<td>20_INCH_LCDU63011</td>
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<td>CPU REGULATOR</td>
<td>1</td>
<td>22UF 0805</td>
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<tr>
<td>G</td>
<td>M56 B26 P - DIFF P/N</td>
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<td>330UF 6.3V LF</td>
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<td>H</td>
<td>126S0086</td>
<td>1</td>
<td>C9400,C1900,C1901,C1968</td>
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<tr>
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<td>124-0333</td>
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<td>CAP,AL,EL,680UF,16V,RAD,10X12.5MM</td>
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<td>C7517,C7518 SANYO 16SVP330M 330UF 16V SMD LF</td>
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<tr>
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<td>U7910</td>
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<td>Z</td>
<td>138S0580</td>
<td>1</td>
<td>LM339</td>
</tr>
</tbody>
</table>
CPU THERMAL SENSOR

PLACE R1017 AND R1019 SUCH THAT THEY SHARE ONE PAD
PLACE R1002 AND R1018 SUCH THAT THEY SHARE ONE PAD

LAYOUT NOTE:
ADD GND GUARD TRACES FOR CPU_THERMD_P/N
ROUTE ON SAME LAYER WITH 0.254MM TRACE WIDTH & SPACING.

NOTE: SYMBOL SHOULD BE SHOWN ADT7461A
CPU THERMAL SENSOR

TEMPERATURE SENSOR IMPLEMENTATION CPU_THERMD_EXT

NOTE: CONTACT MUST BE SHOWN ACCURATELY

CPU TEMP SENSOR

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CPU ITP700FLEX DEBUG SUPPORT

CPU ITP700FLEX DEBUG SUPPORT

ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S TCK PIN AND THEN FUSE BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX CONNECTOR'S PROG PIN.

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Scale: None

Drawing Number: 518S0320

Revision: 1

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rail, and tie VSSA_CRTDAC and VCC_SYNC to GND. Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie CRT Disable VCCA_TVBG to 1.5V power rail. Tie VSSA_TVBG to GND. Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail. TV-Out Disable connect to GND through 75-ohm resistors. Used DAC outputs should filtering components. Unused DAC outputs should Component: DACA, DACB & DACC

S-Video:   DACB & DACC only

Composite: DACA only

Otherwise, tie VCCD_LVDS to GND also.

Can leave all signals NC if LVDS is not implemented

LVDS Disable
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RESERVED

NB_CFG<11>

High = Mobile CPU

NB_CFG<10>

Low = DMIx2

RESERVED

NB_CFG<7>

PCI Express

Low = Reserved

NB_CFG<13:12>

MF-LF

1/16W

2.2K

5%

402

FM-PG_B,-_A3

140

DESCRIPTION

Internal pull-ups

Internal pull-up

NB_CFG<9>

High = DMIx4

NB_CFG<5>

High = Reversed

NB_CFG<3>

Internal pull-up

NB_CFG<15>

High = Enabled

Low = Disabled

NB_CFG<16>

High = DMI Lane Reversal

Low = Normal

PB Internal Design Spec says reserved

NB_CFG<20>

File System

Low = Only SDVO

RESERVED

RESERVED

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NOTE: KEYBOARD CONTROLLER RESET CPU

NOTE: LDRQ<0-1># HAVE INTERNAL 20K PU

NOTE: LAD<0-3> HAVE INTERNAL 20K PU

NOTE: DD<7> HAS INTERNAL 11.5K PD

NOTE: ALL IDE PINS HAVE INTERNAL 33-OHM SERIES R'S

NOTE: DDREQ HAS INTERNAL 11.5K PD
BOM OPTION shown at the top of each group applies to every part below it.
THESE POWER PLANES SHOULD BE MOSTLY ISOLATED
Termination
Place close to FireWire PWV

3rd TPA/TPR pair unused

ESD Rail

"Snapback" & "Late VG" Protection

PORT 0
1394A

PORT 1
1394A

FIREFIRE CONNECTORS
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IT IS 2.2V INSTEAD OF 2.7V BECAUSE THE SNAPBACK ESD DIODES HAVE A .5V DROP.
CURRENT THROUGH THE BIAS RESISTOR SHOULD BE 5MA FOR A VOLTAGE DROP TO 2.2V.
NOTE: STANDOFFS FOR J5300 MINIMIZED IF THE RESISTORS ARE NOT STUFFED
PLACE CAPS < 250 MILS FROM U2100

SDF5300 STDOFF-4OD5.6H-1.35-TH

C5300 0.1UF

C5301 0.1UF

C5304 402 10V 0.1UF 20% CERM

C5305 402 10V 0.1UF CERM

C5306 402 10V 0.1UF CERM

C5307 402 10V 0.1UF CERM

C5308 402 10V 0.1UF CERM

C5309 402 10V 0.1UF CERM

C5310 805-1 CERM 20% 6.3V 10UF

C5311 805-1 CERM 20% 6.3V 10UF

C5312 805-1 CERM 10UF 6.3V 20%

C5313 402 CERM 10V 20% 0.1UF

C5314 805-1 CERM 20% 6.3V 10UF

R5301 0

R5302 0

R5304

R5305

R5306

R5307

R5308

R5309

R5310

R5311

R5312

R5313

R5314

AIRPORT CONN

SYNC_MASTER=N/A  
SYNC_DATE=N/A

AIRPORT WAKE_L =PP3V3_S0_AIRPORT

AIRPORT_CONN_CLK =SMB_AIRPORT_CLK

AIRPORT_CONN_DATA =SMB_AIRPORT_DATA

PCIE_WAKE_L

PCIE_B_D2R_N

PCIE_B_D2R_P

PCIE_B_R2D_C_P

PCIE_B_R2D_C_N

PCIE_B_R2D_P

PCIE_B_R2D_N

PCIE_B_R2D_C_P

PCIE_B_R2D_C_N

051-7124 13

051-7124 13
R6306-07 SHOULD BE PLACED LESS THAN 2.54MM FROM U2100
R6303 SHOULD BE PLACED LESS THAN 2.54MM FROM U6301
Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits.
3.3V S0
PP3V3_S5

2.5V S0
PP2V5_S5

12V S0
PP12V_S5

4.5V S0 AUDIO
PP12V_S5

5V S0
PP5V_S0

3.3V AND 5V S3
PP5V_S5

SO AND S3 FETS

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APPLE COMPUTER, INC.

SYNC_MASTER=FINO-PC
SYNC_DATE=04/12/2005

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Note: The table contains various components and their specifications, related to electronics and circuitry.
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