

M60 - EVT

05/12/06

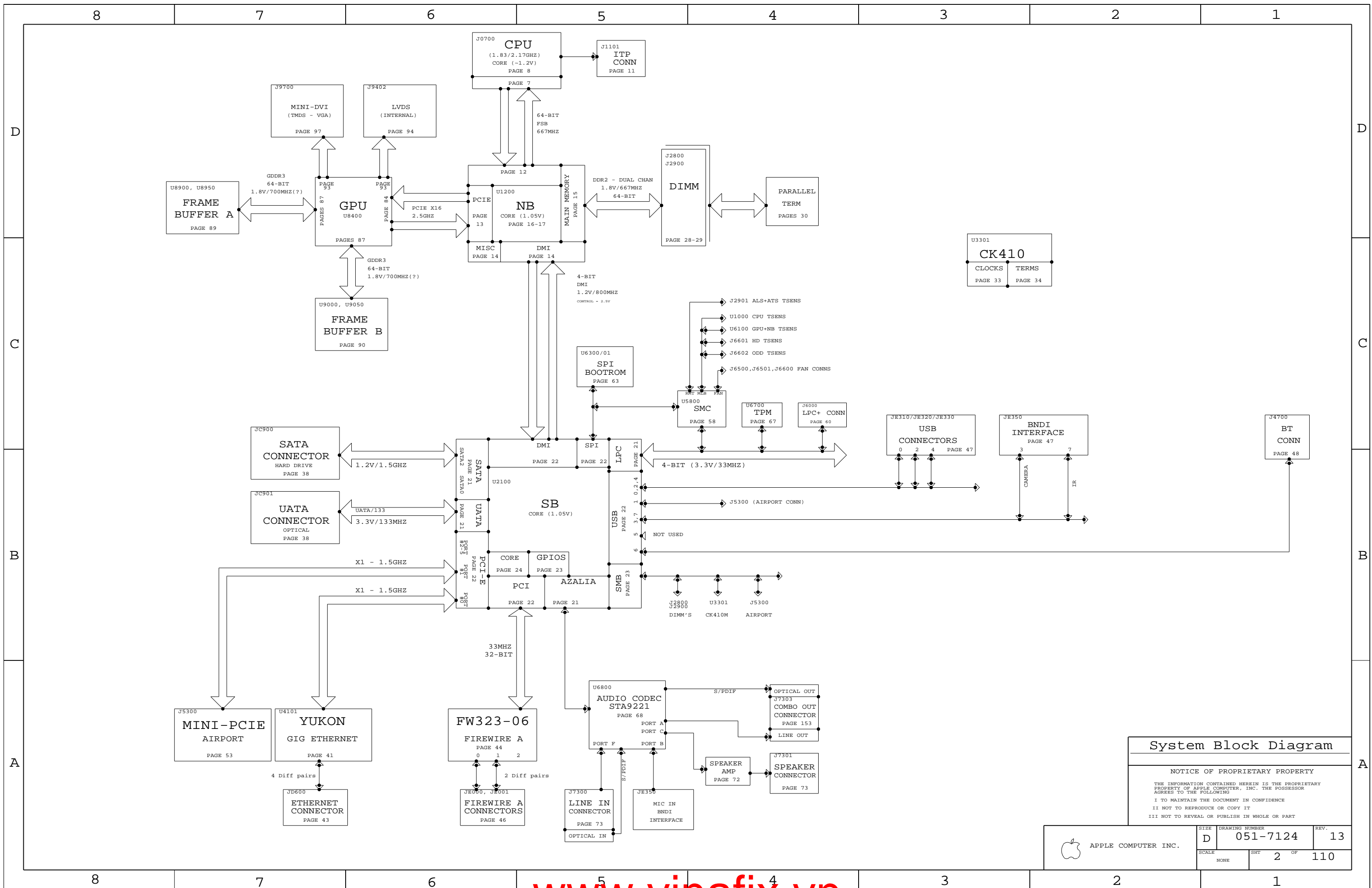
1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD	ENG APPD
				DATE	DATE
06		400374	ENGINEERING RELEASED	09/16/05	06/22/04

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12	JH	12 NB - CPU INTERFACE
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17	JH	17 NB - POWER 2
18	JH	18 NB - GROUNDS
19	JH	19 NB - DECAPS
20	JH	20 NB - CONFIG STRAPS
21	JD	21 SB - RTC, LAN, AUDIO, ATA, CPU, LPC
22	JD	22 SB - PCIE, SPI, USB, DMI, PCI
23	JD	23 SB - SMB, GPIO, PM, CLKS
24	JD	24 SB - POWERS AND GROUNDS
25	JD	25 SB - DECAPS
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31	MY	31 DDR2 - VTT SUPPLY
33	JD	32 CLOCKS - GENERATOR
34	JD	33 CLOCKS - TERMINATIONS
38	JD	34 ATA (SATA AND IDE) CONN'S
41	JD	35 LAN - YUKON'S PCIE INTERFACE
42	JD	36 LAN - YUKON'S PWR, MISC
43	JD	37 LAN - CONN
44	JD	38 FIREWIRE - FW323-06
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PAGE	PDF	CIRCUIT
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61	MY	48 SMC - GPU/NB THERMAL SENSOR
63	MY	49 SMC - SPI BOOTROM
65	MY	50 SMC - FANS
66	MY	51 SMC - FANS
67	JD	52 SMC - TPM
68	TG	53 AUDIO - CODEC, VREG, MIC BIAS
72	TG	54 AUDIO - INTERNAL SPEAKER AMP
73	TG	55 AUDIO - I/O CONN'S, EMC
74	TG	56 AUDIO - DETECT TRANSLATORS
75	MY	57 VR - CPU CORE
76	MY	58 VR - CPU I-V SENSE CKT
77	MY	59 VR - "S3" 1.2V & "S0" 1.2V
78	MY	60 VR - "S0" 1.8V
79	MY	61 VR - "S3" 1.8V
80	MY	62 VR - "S0" 1.5V
81	MY	63 VR - "S0" 1.05V
82	MY	64 VR - "S5" 5V AND "S0" 4.5V
83	MY	65 VR - FETS FOR REMAINING RAILS
84	JH	66 GPU - M56 PCI-E
85	JH	67 GPU - VCORE SUPPLY
86	JH	68 GPU - M56 CORE PWR
87	JH	69 GPU - M56 FRAME BUFFER
88	JH	70 GPU - MISC
89	JH	71 GPU - GDDR SDRAM A
90	JH	72 GPU - GDDR SDRAM B
91	JH	73 GPU - M56 GPIO, DVO, MISC
92	JH	74 GPU - M56 CLOCKS
93	JH	75 GPU - M56 VIDEO INTERFACES
94	JH	76 GPU - INTERNAL DISPLAY CONN'S
95	JH	77 GPU - TP'S
96	JH	78 GPU - TMDS, INVERTER, EXT VGA
97	JH	79 GPU - EXTERNAL DISPLAY CONN'S

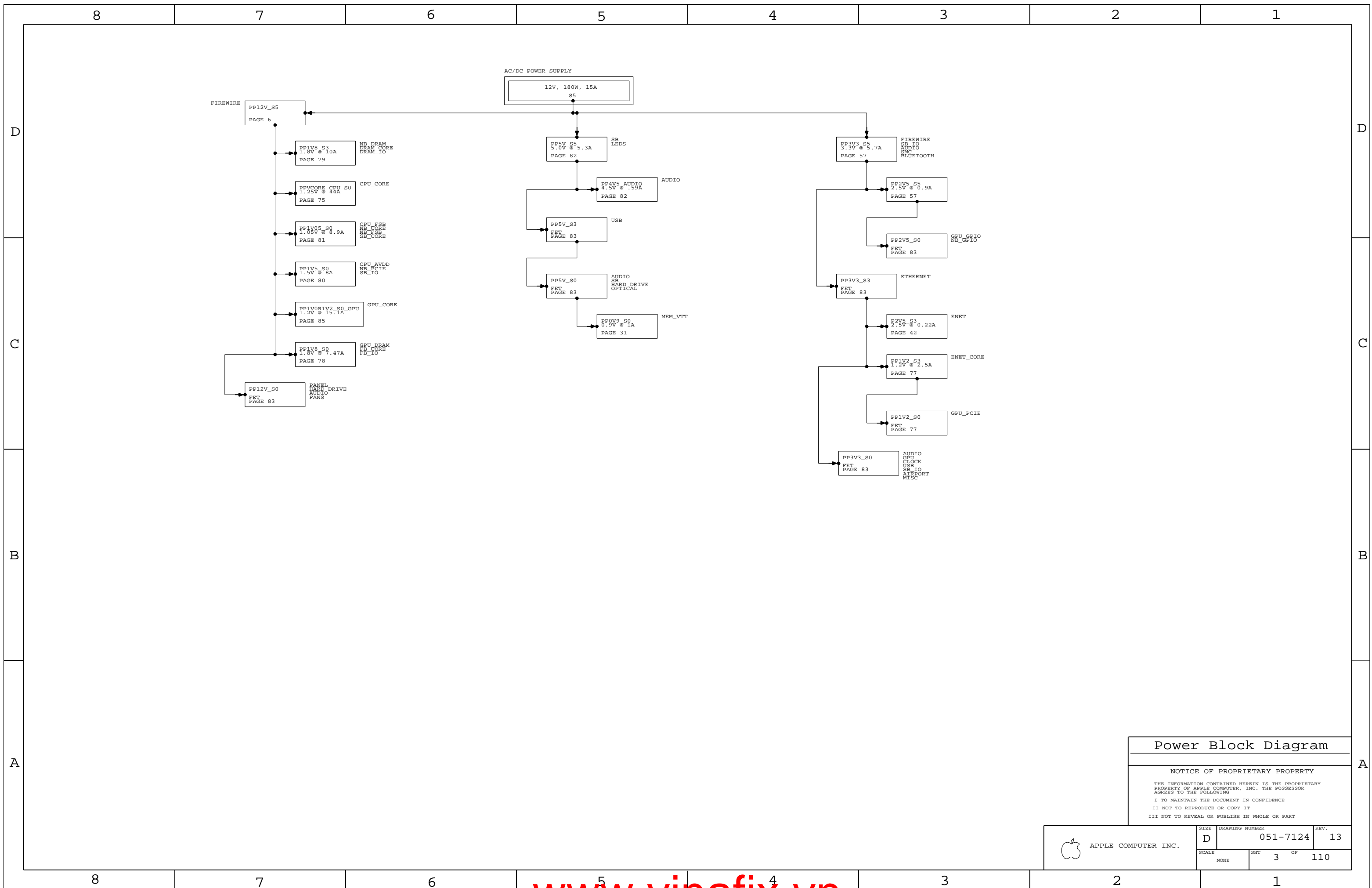
<p style="font-size: small;">DIMENSIONS ARE IN MILLIMETERS</p> <p>XX : _____</p> <p>X.XX : _____</p> <p>X.XXX : _____</p> <p>ANGLES : _____</p> <p style="font-size: x-small;">DO NOT SCALE DRAWING</p> <div style="text-align: center;"> <p style="font-size: x-small;">THIRD ANGLE PROJECTION</p> </div>	<p>METRIC</p>	<div style="text-align: right;"> <p>Apple Computer Inc.</p> </div> <p style="font-size: x-small; text-align: center;">NOTICE OF PROPRIETARY PROPERTY</p> <p style="font-size: x-small; text-align: center;">THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING</p> <p style="font-size: x-small; text-align: center;">I TO MAINTAIN THE DOCUMENT IN CONFIDENCE</p> <p style="font-size: x-small; text-align: center;">II NOT TO REPRODUCE OR COPY IT</p> <p style="font-size: x-small; text-align: center;">III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART</p> <div style="text-align: center;"> <p>SCH, MLB, M60</p> </div> <table style="width: 100%; border: none;"> <tr> <td style="width: 70%; border: none;">DRAWING NUMBER</td> <td style="width: 30%; border: none;">REV. 13</td> </tr> <tr> <td style="border: none; text-align: center;">051-7124</td> <td style="border: none;"></td> </tr> </table> <p style="font-size: x-small; text-align: right;">SHT 1 OF 110</p>	DRAWING NUMBER	REV. 13	051-7124													
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051-7124																		
<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 25%;">DRAWN</td> <td style="width: 25%;">DESIGN CK</td> <td style="width: 25%;">MFG APPD</td> <td style="width: 25%;">TITLE</td> </tr> <tr> <td style="width: 25%;">ENG APPD</td> <td style="width: 25%;">DESIGNER</td> <td style="width: 25%;">SCALE</td> <td style="width: 25%;">NONE</td> </tr> <tr> <td style="width: 25%;">QA APPD</td> <td style="width: 25%;">SCALE</td> <td style="width: 25%;">MATERIAL/FINISH NOTED AS APPLICABLE</td> <td style="width: 25%;">SIZE D</td> </tr> <tr> <td style="width: 25%;">RELEASE</td> <td style="width: 25%;">SCALE</td> <td colspan="2" style="width: 50%;"></td> </tr> </table>	DRAWN	DESIGN CK	MFG APPD	TITLE	ENG APPD	DESIGNER	SCALE	NONE	QA APPD	SCALE	MATERIAL/FINISH NOTED AS APPLICABLE	SIZE D	RELEASE	SCALE				
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RELEASE	SCALE																	



System Block Diagram

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NONE	2	110	



Power Block Diagram

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	D	051-7124	13
SCALE	SHT	OF	REV.
NONE	3	110	

8

7

6

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4

3

2

1

COMMON

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
511S0025	1	IC,CPU-SKT,479BGA	J0700	CRITICAL	
338S0328	1	IC,945PM,NORTHBRIDGE	U1200	CRITICAL	
343S0385	1	IC,SB,652BGA	U2100	CRITICAL	
338S0345	1	IC,ATI,M56D,GRAFIXCTLR,880BGA,LF	U8400	CRITICAL	
359S0101	1	IC,CY28445-5,CLK GEN,68PIN QFN	U3301	CRITICAL	
338S0270	1	IC,88E053,01GIBIT ENET XCVR,64P QFN,SMD	U4101	CRITICAL	
(335S0382) 341S1797	1	IC,ENET LAN ROM	U4102	CRITICAL	
338S0279	1	IC,FW32306,1394A LINK,TQFP	U4400	CRITICAL	

341S1789	1	IC,TPM,TSSOP,28P	U6700	CRITICAL	LEMENU
UNSCREENED P/N 353S1235 353S1465	1	IC,CPU VREG,IMVP,TWO PHASE	U7500	CRITICAL	

128S0078	2	CAP,EL,AL,330UF,20%,16V,10X12.7MM,SMD,LF	C7517,C7518	CRITICAL	
825-6447	1	MLB LABEL,48.0X4.8	X14	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
-------------	---------------------------	------------	---------	-----------

126S0086	126S0078		C940 C1900,C1901 C1968	SANYO W6CE330F8 330UF 6.3V LF
128S0080	128S0078		C7517,C7518	SANYO 160VP330M 330UF 16V SMD LF
124-0338	124-0333			CAP,AL,EL,680UF,16V,RAD,10X12.5MM
138S0580	138S0552			22UF 0805
353S1321	353S1105		U7910	LM339
338S0344	338S0345		U8400	M56 B26 P - DIFF P/N
353S1461	353S1465		U7500	CPU REGULATOR - ISL9504

(341S1904 - DEV)
(341S1905 - PVT)
(335S0384 - BLNK)
(341S1903 - PROG)
(338S0274 - BLNK)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-7124	1	PCB,SCHEM,MLB,M60	SCH1		20_INCH_LCD
820-2031	1	PCB,FAB,MLB,M60	MLB1		20_INCH_LCD
341T0036	1	EPI ROM,M60	U6301	CRITICAL	20_INCH_LCD
341T0035	1	IC,SMC,M60	U5800	CRITICAL	20_INCH_LCD
338S0315	1	IC,ATI,M56LP,GRAFIX CTLR,880BGA,LF	U8400	CRITICAL	GPU_B26_LP
114S0264	1	3.01K,1%,1/16W,402,MP-LF	R8522		GPU_VCORE_1P2V
337S3293	1	2.16GHZ MEROM	CPU	CRITICAL	2P16_CPU
337S3292	1	2.33GHZ MEROM	CPU	CRITICAL	2P33_CPU

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
333S0354	4	IC,SDRAM,GDDR3,8MX32,700MHZ,136FBGA	U8900,U8950,U9000,U9050	CRITICAL	ATI_FB_128M_SAMSUNG
333S0358	4	IC,SDRAM,GDDR3,8MX32,700MHZ,136FBGA	U8900,U8950,U9000,U9050	CRITICAL	ATI_FB_128M_HYNIX
333S0376	4	IC,SDRAM,GDDR3,8MX32,700MHZ,136FBGA	U8900,U8950,U9000,U9050	CRITICAL	ATI_FB_128M_INFINEON

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
333S0350	4	IC,SDRAM,GDDR3,16MX32,700MHZ,136FBGA	U8900,U8950,U9000,U9050	CRITICAL	ATI_FB_256M_SAMSUNG
333S0351	4	IC,SDRAM,GDDR3,16MX32,700MHZ,136FBGA	U8900,U8950,U9000,U9050	CRITICAL	ATI_FB_256M_HYNIX
333S0377	4	IC,SDRAM,GDDR3,16MX32,600MHZ,136FBGA	U8900,U8950,U9000,U9050	CRITICAL	ATI_FB_256M_INFINEON

Table Items

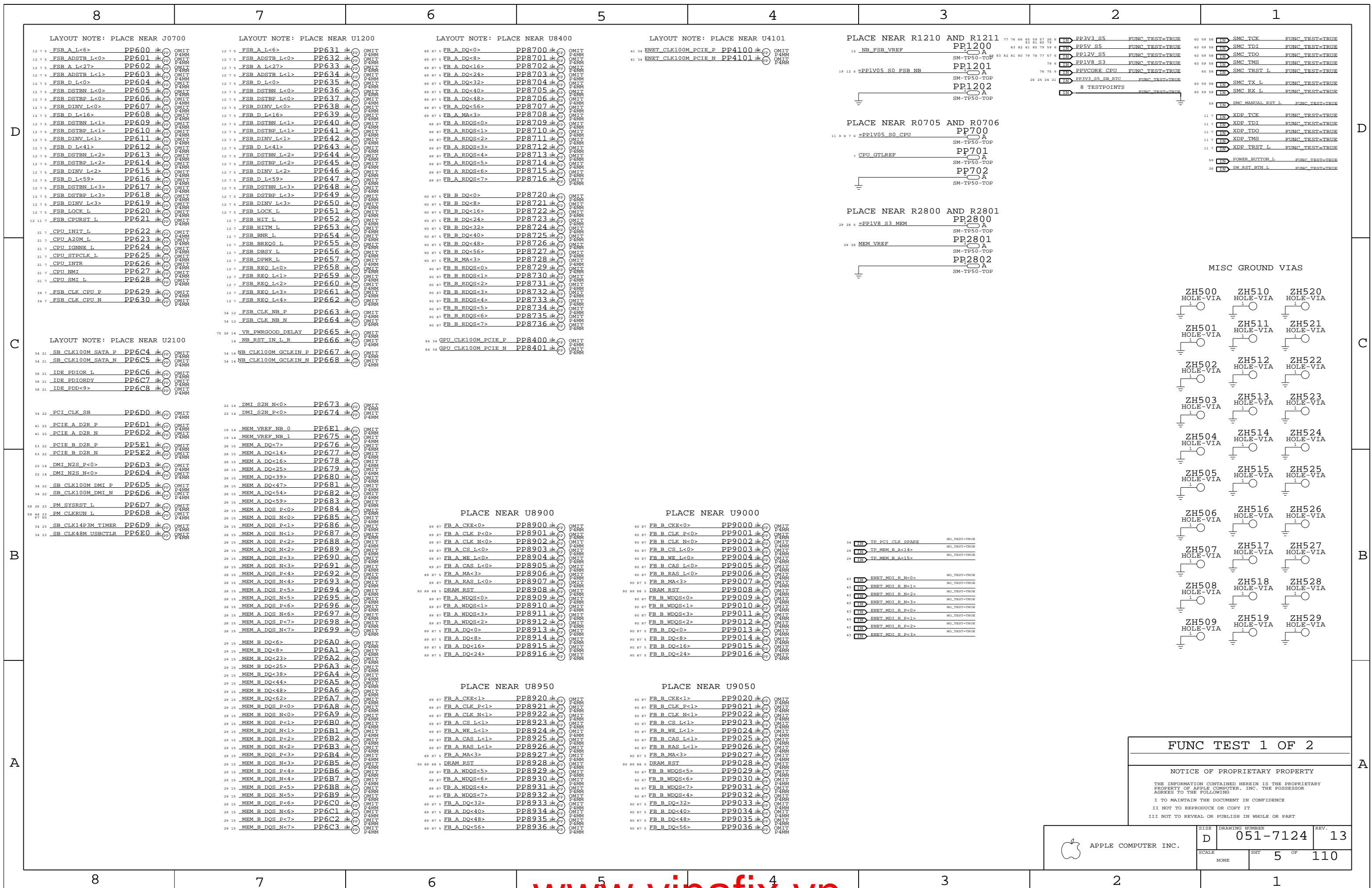
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NONE	4	110

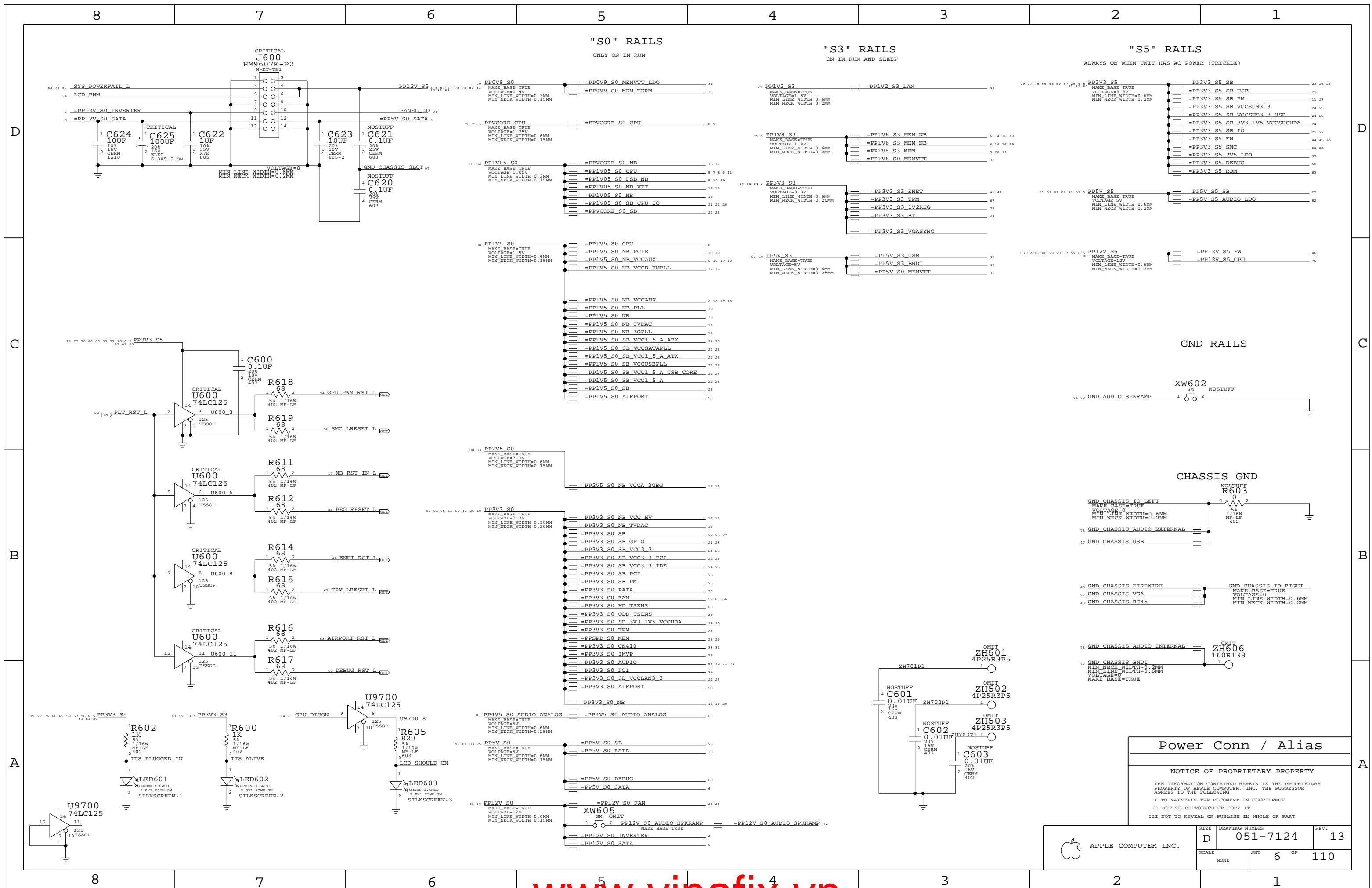


FUNC TEST 1 OF 2

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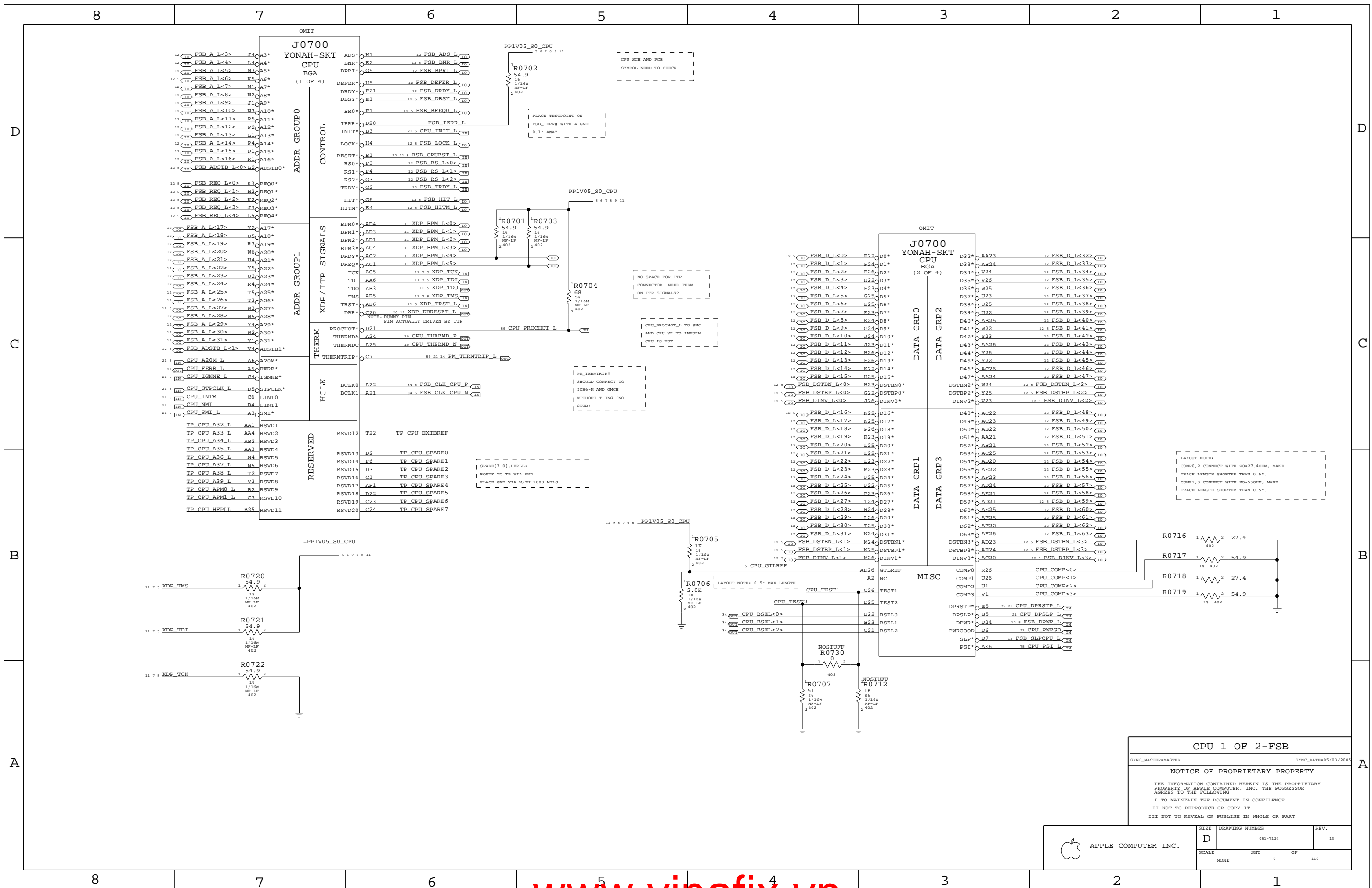


Power Conn / Alias

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	SCALE NONE	SHEET 6 OF 110	



CPU 1 OF 2-FSB

SYNC_MASTER=MASTER SYNC_DATE=05/03/2005

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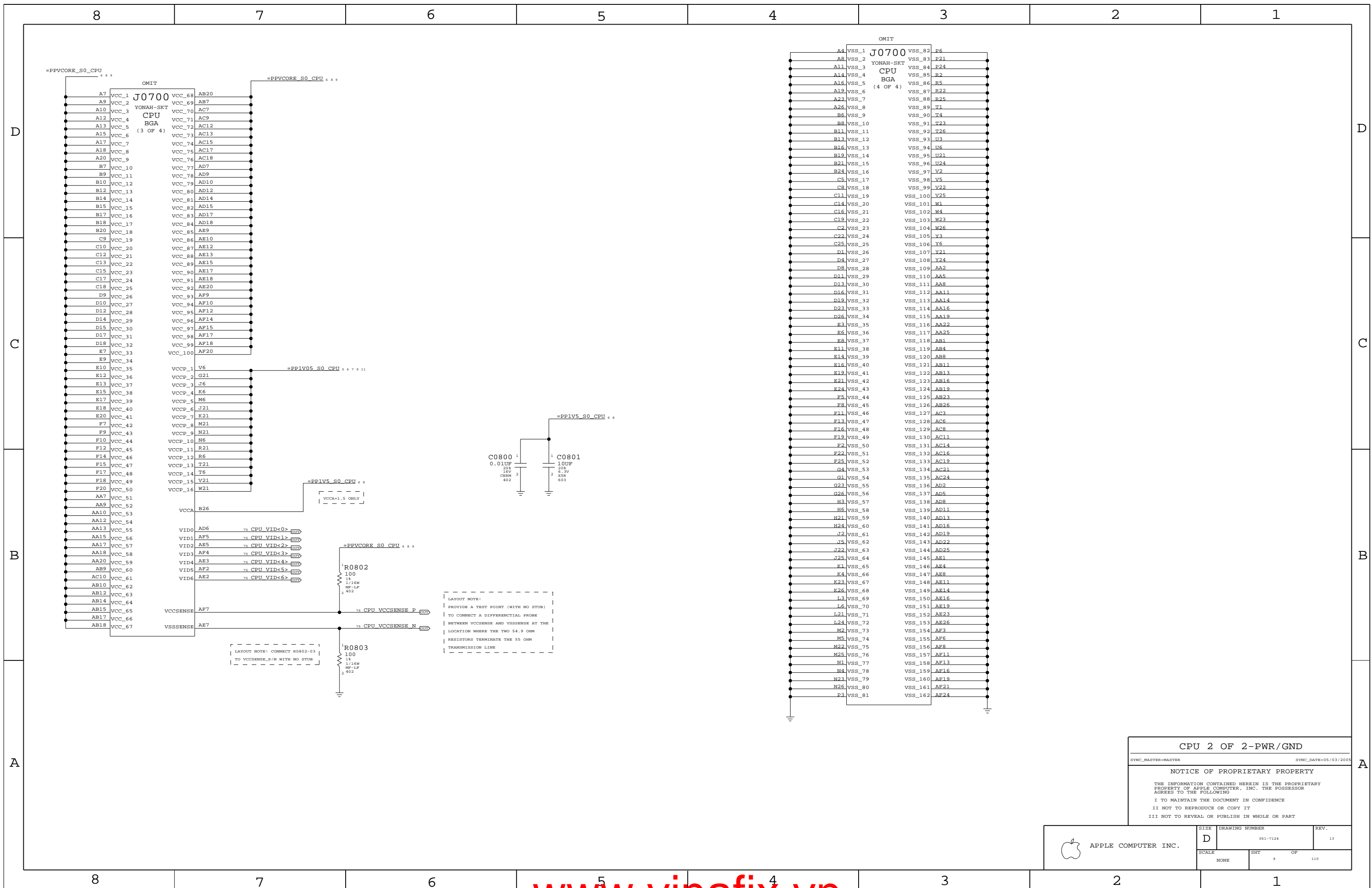
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CPU 2 OF 2-PWR/GND

SYNC_MASTER=MASTER SYNC_DATE=05/03/2005

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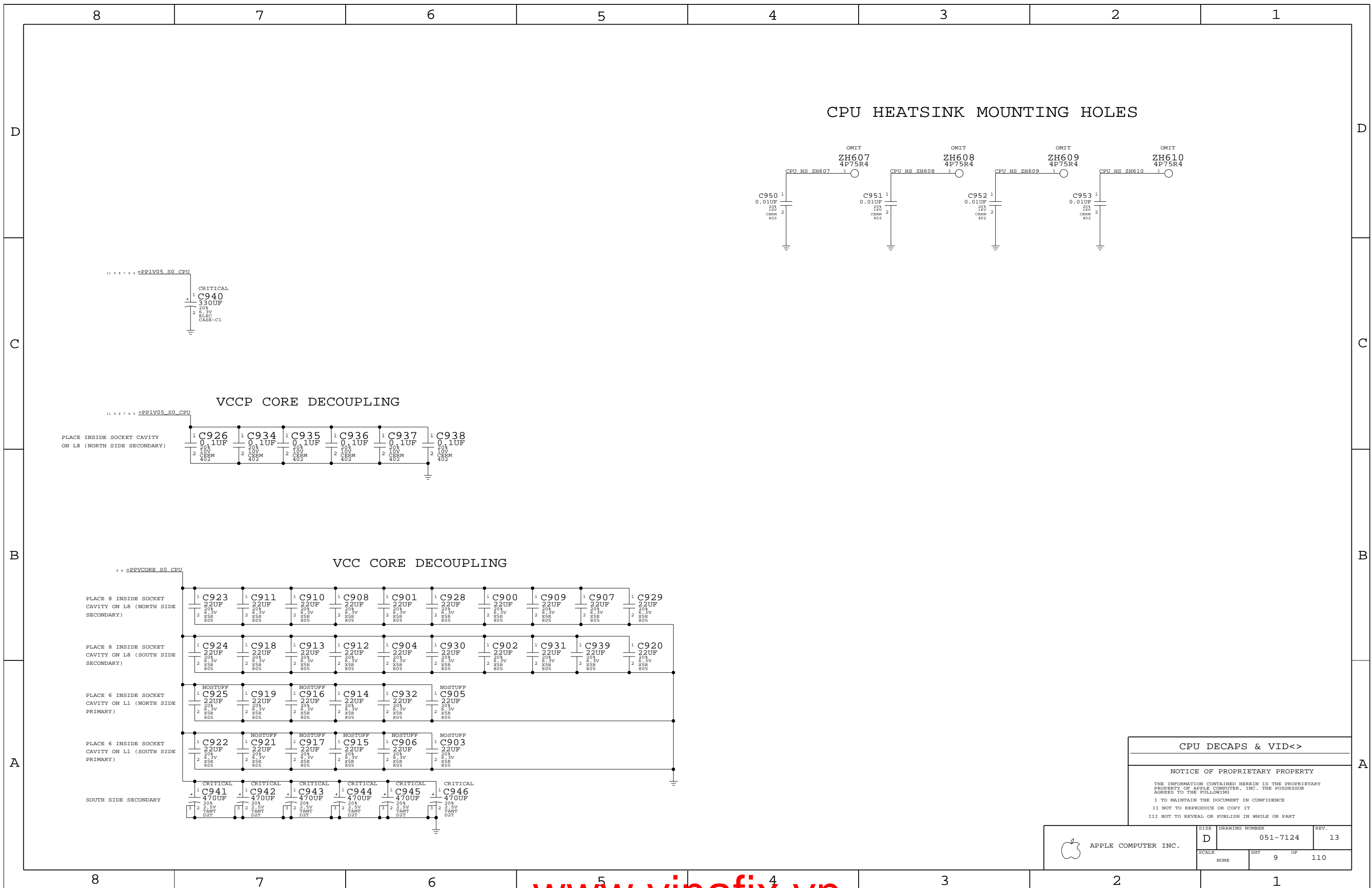
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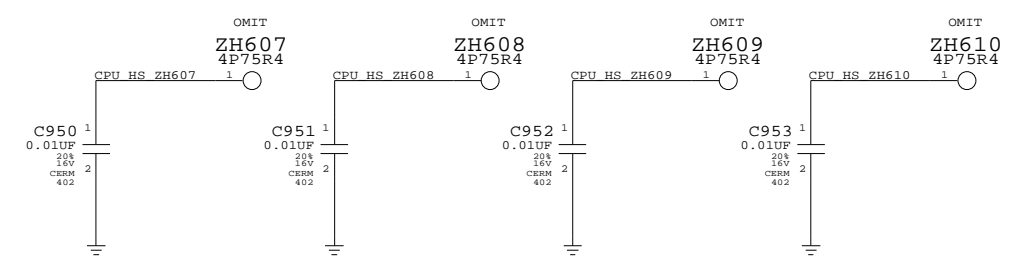
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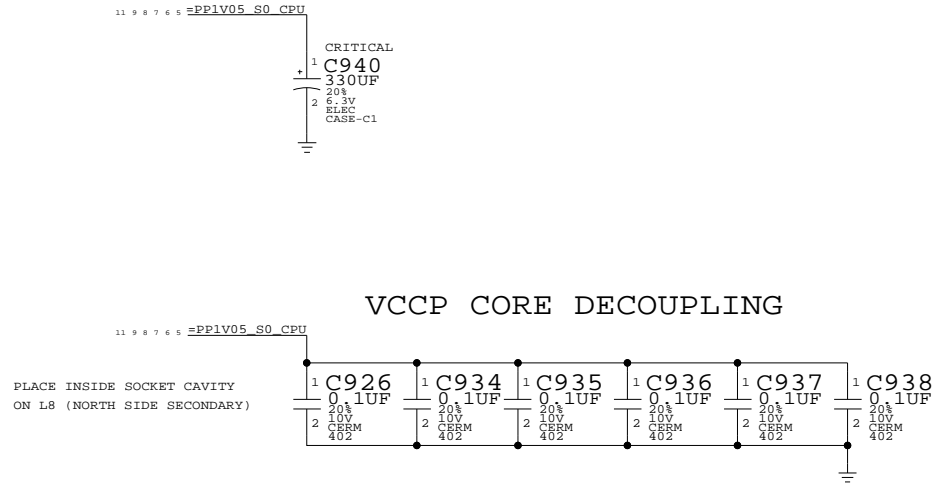
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SCALE	SHT OF		REV.
NONE	8 OF 110		



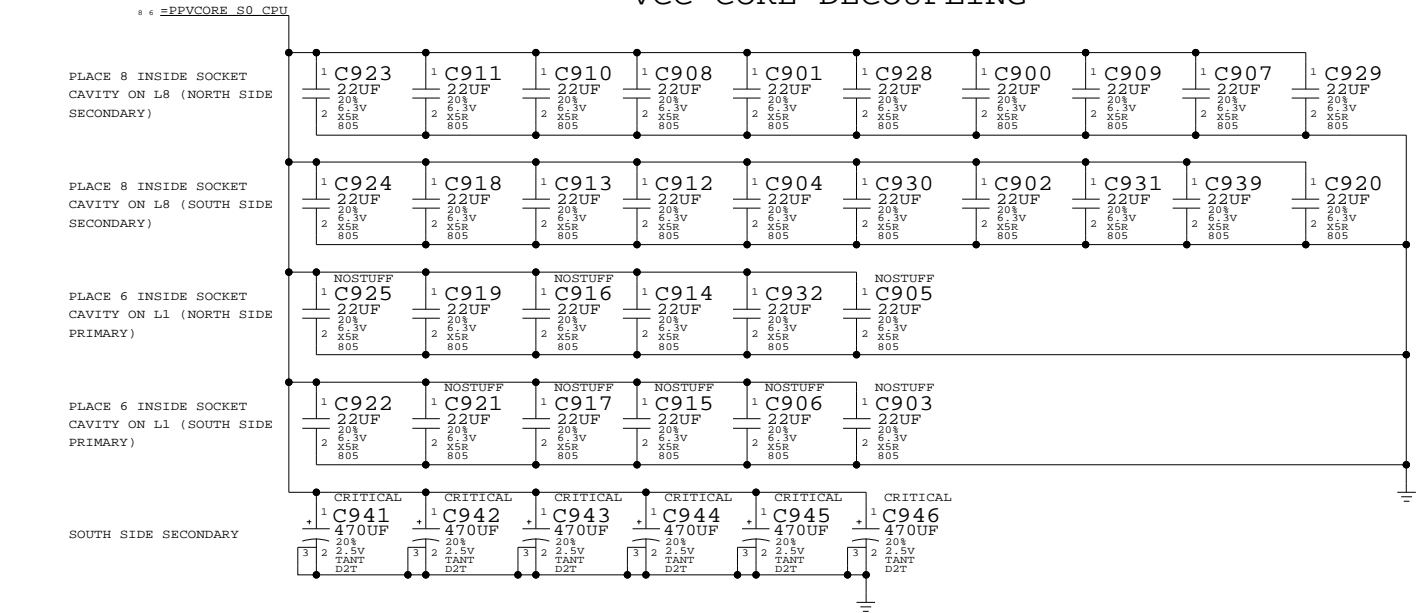
CPU HEATSINK MOUNTING HOLES



VCC CORE DECOUPLING



VCC CORE DECOUPLING



CPU DECAPS & VID<>

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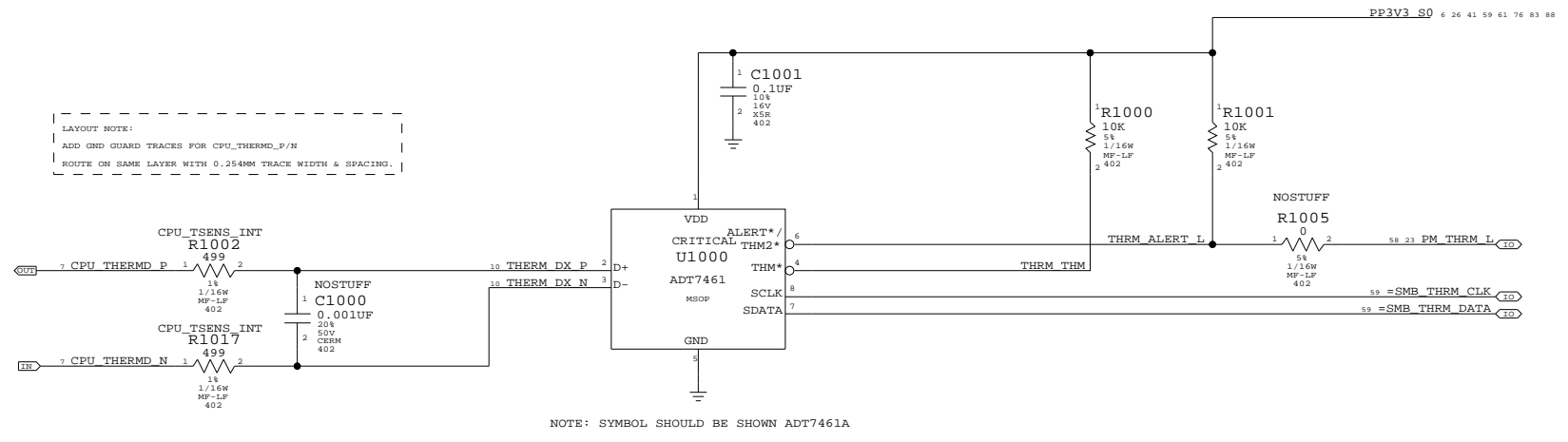
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	SCALE NONE	SHT 9	OF 110

CPU THERMAL SENSOR

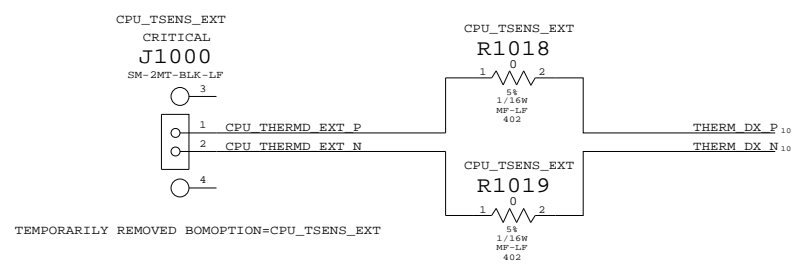
NOTE:
IF CPU T DIODE TO BE READ IN OFF STATE,
THEN THIS SHOULD BE S5

LAYOUT NOTE:
ADD GND GUARD TRACKS FOR CPU_THERMD_P/N
ROUTE ON SAME LAYER WITH 0.254MM TRACE WIDTH & SPACING.



NOTE: SYMBOL SHOULD BE SHOWN ADT7461A

LAYOUT NOTE:
PLACE R1002 AND R1018 SUCH THAT THEY SHARE ONE PAD
PLACE R1017 AND R1019 SUCH THAT THEY SHARE ONE PAD



CPU TEMP SENSOR

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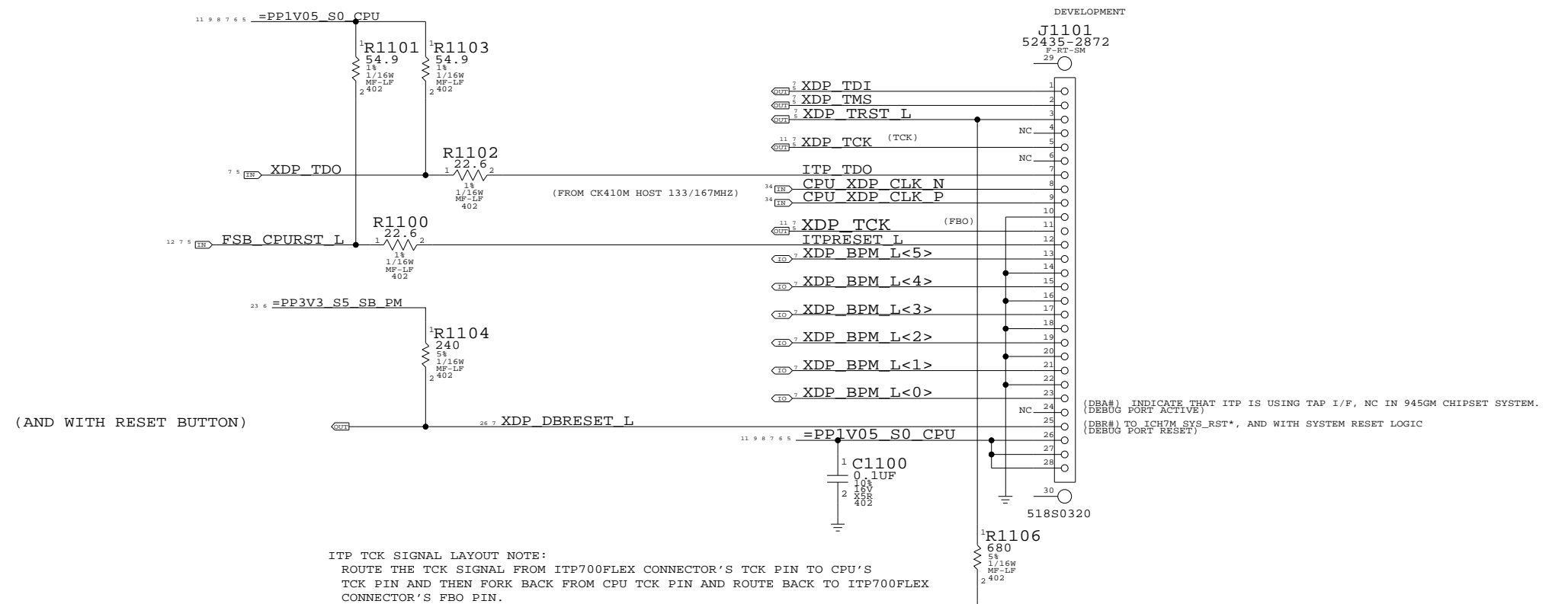
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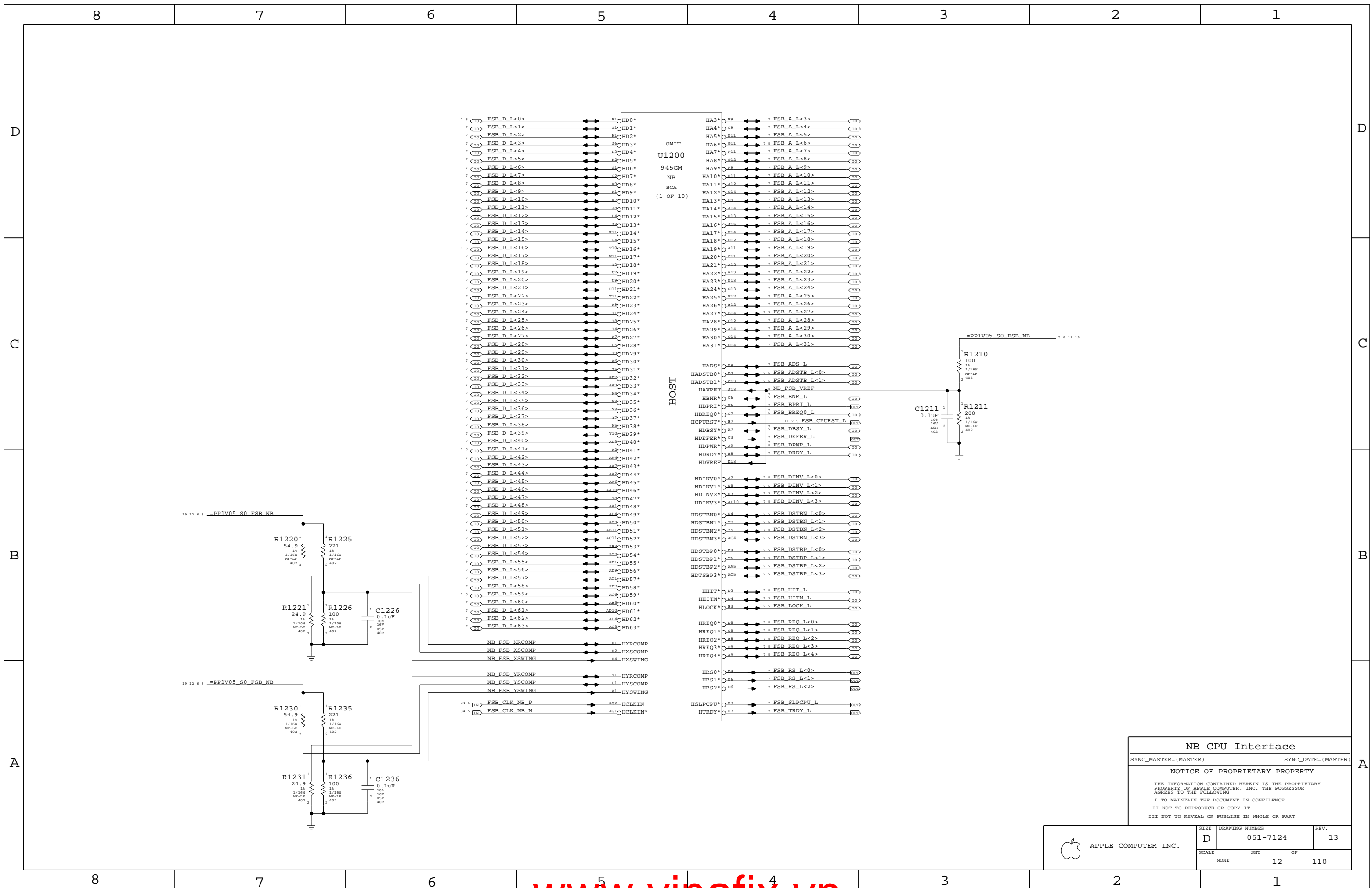
CPU ITP700FLEX DEBUG SUPPORT



CPU ITP700FLEX DEBUG
 SYNC_MASTER=MASTER SYNC_DATE=5/23/05

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SCALE	SHT	OF	110
NONE	11		



NB CPU Interface

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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	SCALE NONE	SHEET 12	OF 110

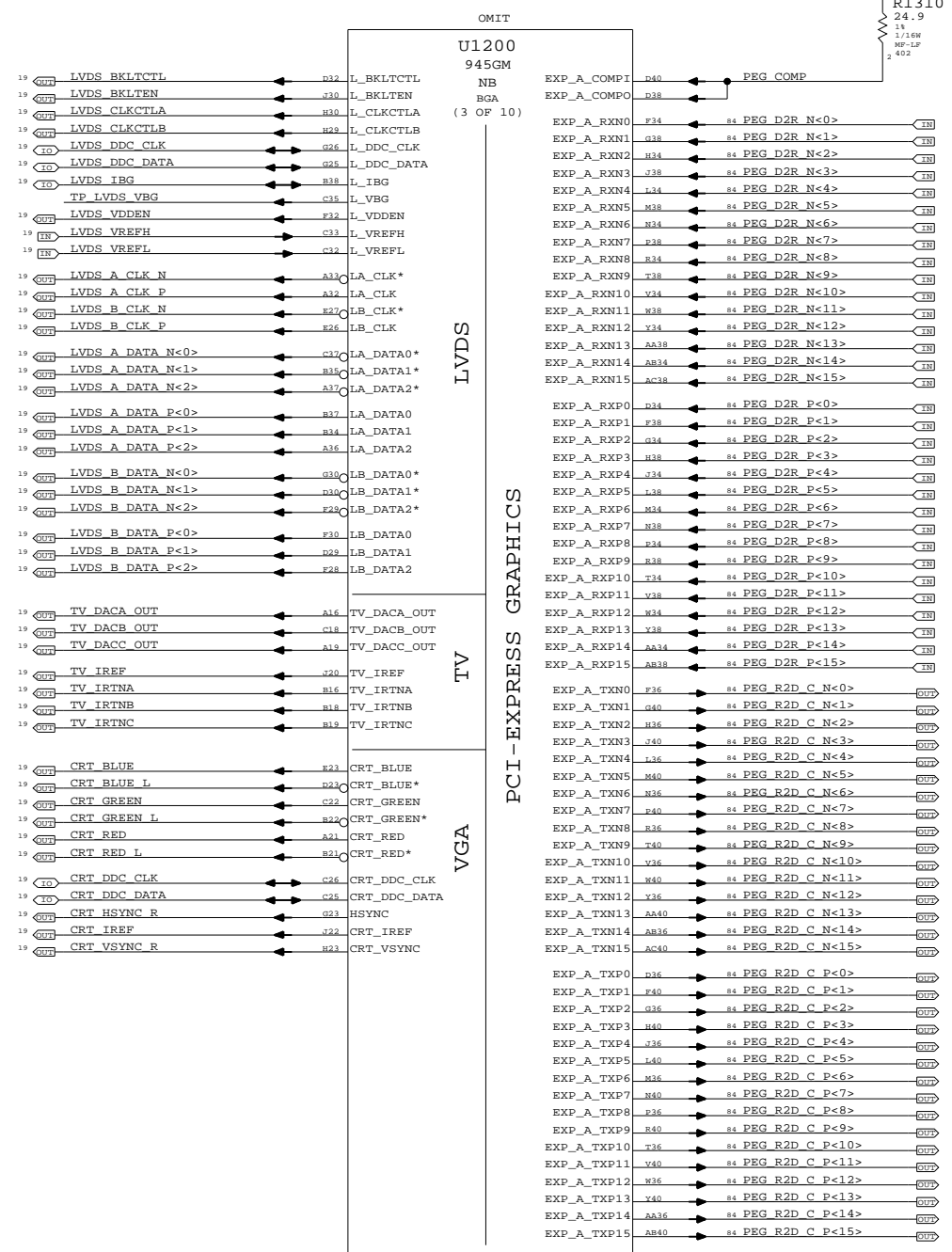
LVDS Disable
 Can leave all signals NC if LVDS is not implemented
 Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
 VCCD_LVDS must remain powered with proper decoupling.
 Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:
 Composite: DACA only
 S-Video: DACB & DACC only
 Component: DACA, DACB & DACC

Unused DAC outputs must remain powered, but can omit
 filtering components. Unused DAC outputs should
 connect to GND through 75-ohm resistors.

TV-Out Disable
 Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail.
 Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and
 VCCA_TVVBG to 1.5V power rail. Tie VSSA_TVVBG to GND.

CRT Disable
 Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie
 HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core
 rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.



SDVO Alternate Function

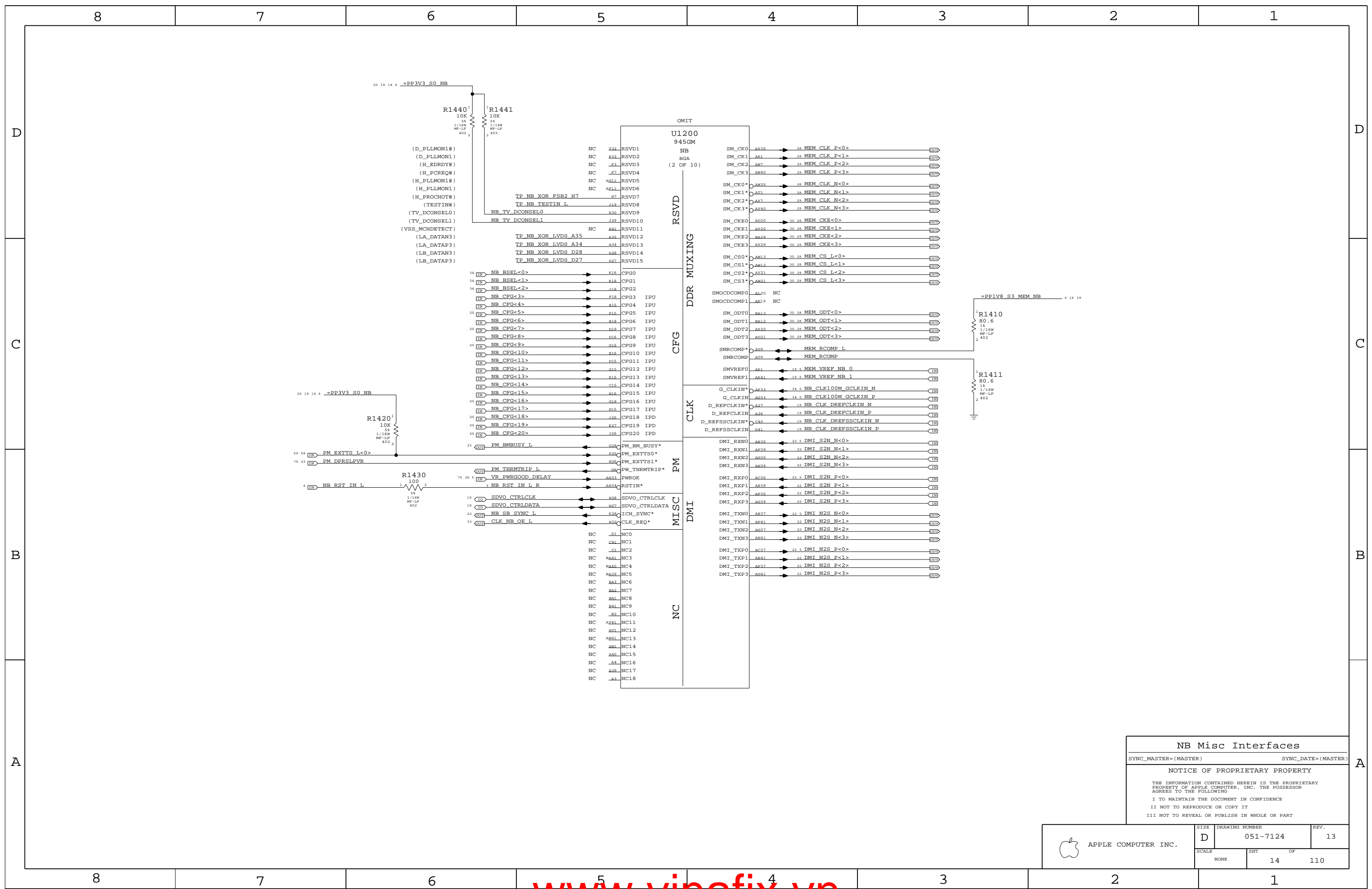
SDVO_TVCLKIN#
 SDVO_INT#
 SDVO_FLDSTALL#

SDVOB_RED#
 SDVOB_GREEN#
 SDVOB_BLUE#
 SDVOB_CLKN
 SDVOC_RED#
 SDVOC_GREEN#
 SDVOC_BLUE#
 SDVOC_CLKN

SDVOB_RED
 SDVOB_GREEN
 SDVOB_BLUE
 SDVOB_CLKP
 SDVOC_RED
 SDVOC_GREEN
 SDVOC_BLUE
 SDVOC_CLKP

NB PEG / Video Interfaces
 SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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SCALE	SHT OF		
NONE	13		110



NB Misc Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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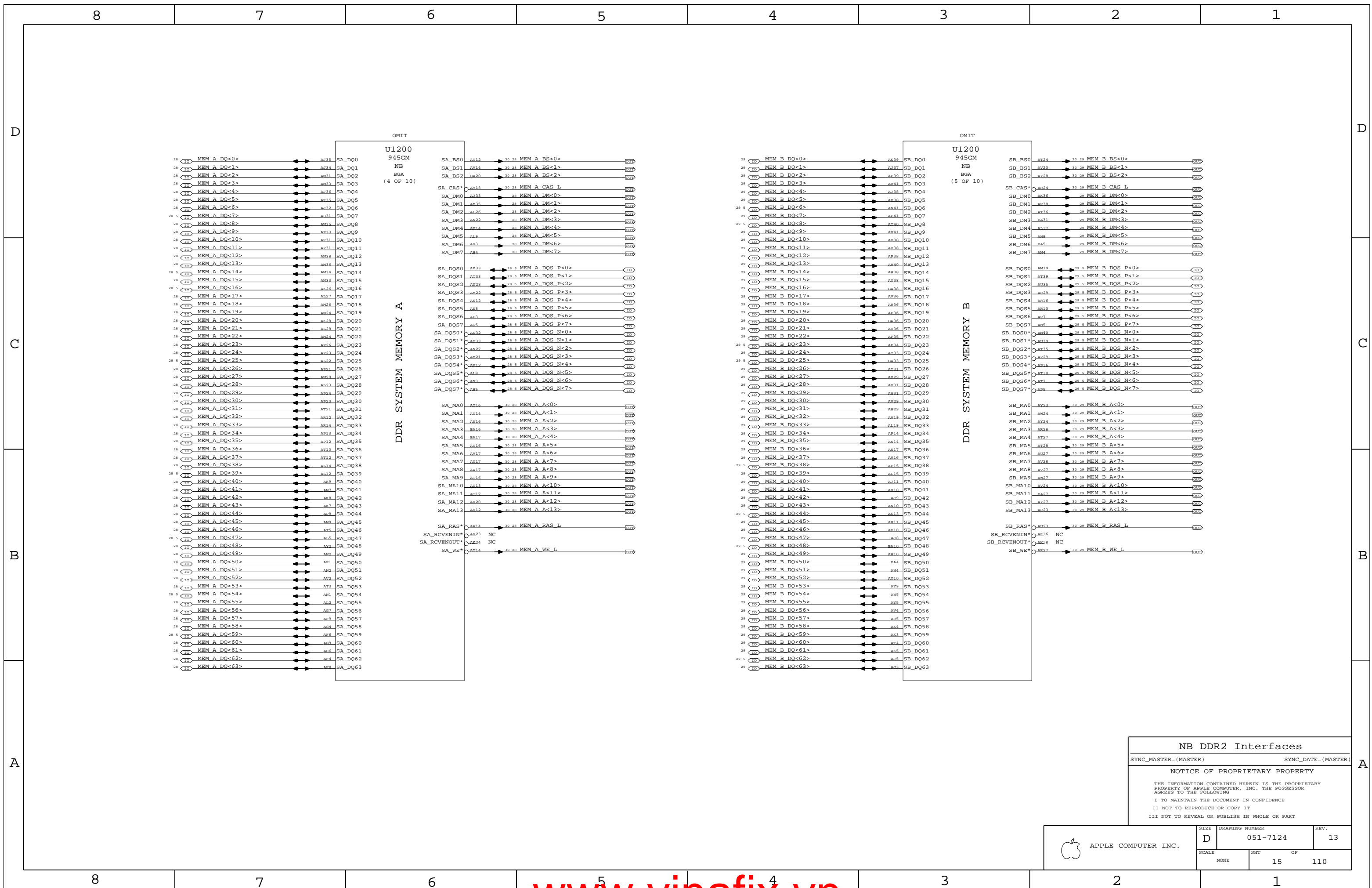
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	SCALE NONE	SHEET 14	OF 110



NB DDR2 Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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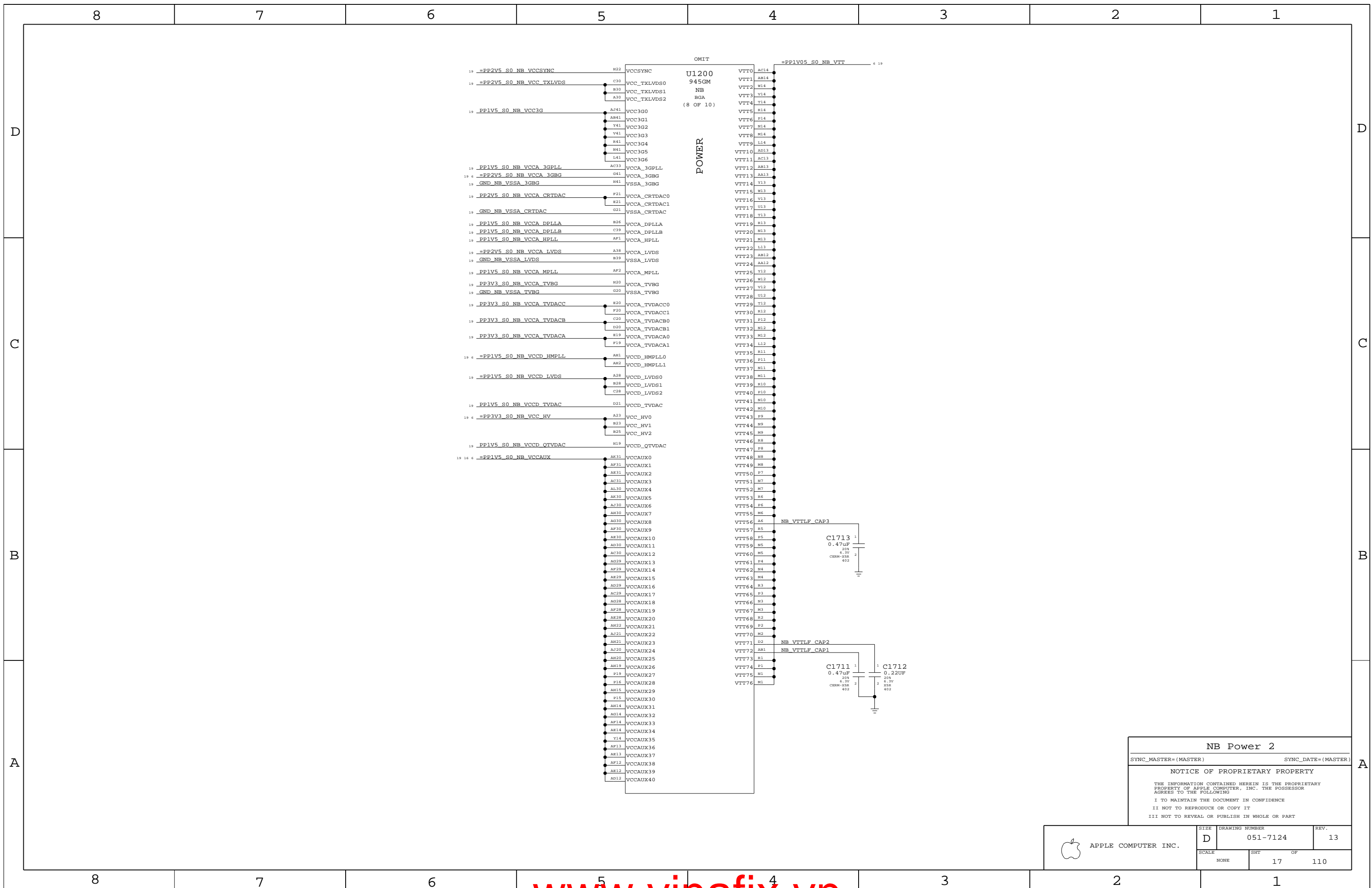
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7124	REV. 13
	SCALE NONE	SHEET 15	OF 110



NB Power 2

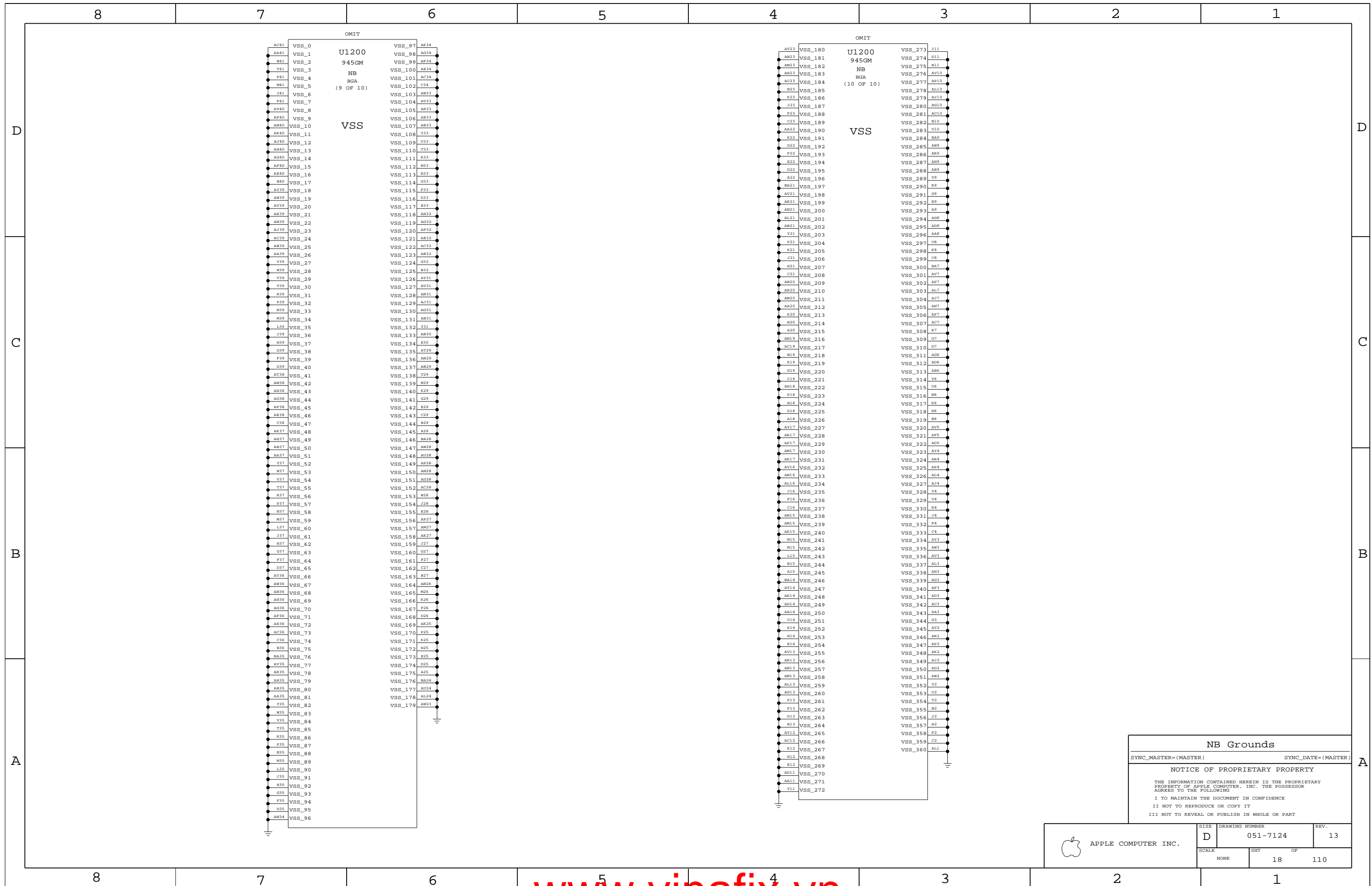
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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	D	051-7124	13
SCALE	SHT	OF	
NONE	17	110	



NB Grounds

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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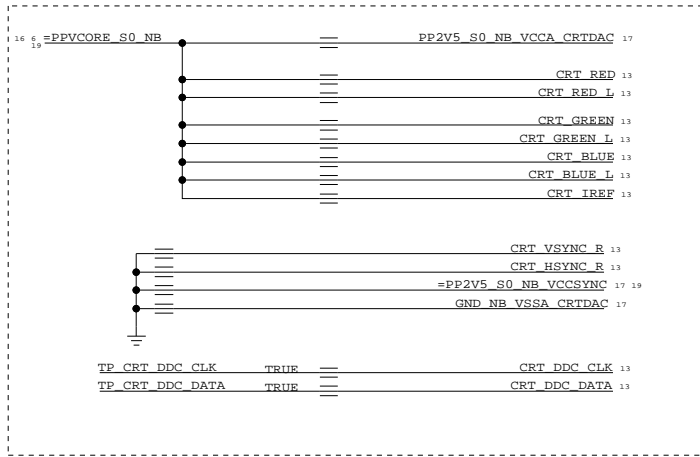
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7124	REV. 13
	SCALE NONE	SHEET 18	OF 110

Power Interface

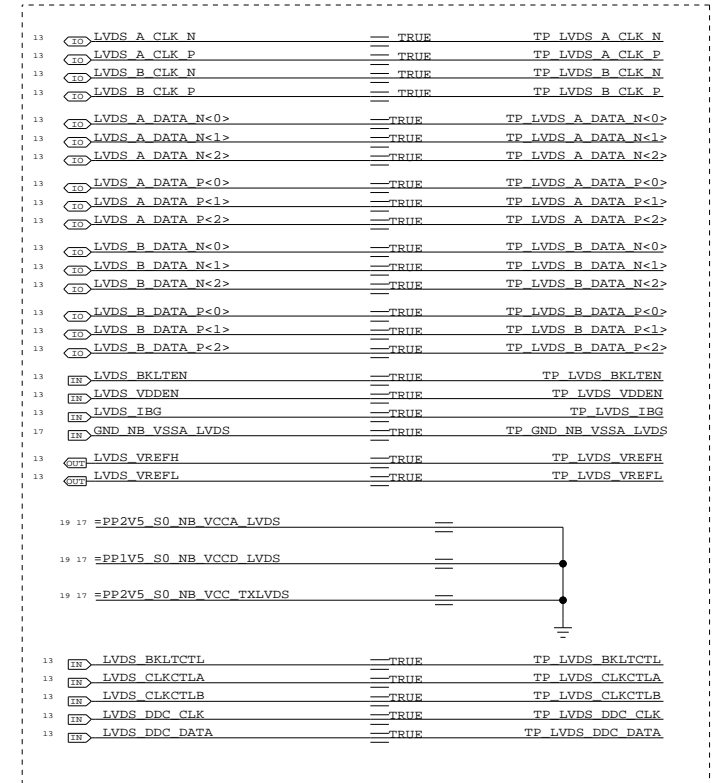
These are the power signals that leave the NB "block"

PP1V05_S0_FSB_NB	5 6 12
PPVCORE_S0_NB	6 16 19
PP1V05_S0_NB	6
PP1V05_S0_NB_VTT	6 17 19
PP1V5_S0_NB	6 19
PP1V5_S0_NB_PCIE	6 13
PP1V5_S0_NB_PLL	6 19
PP1V5_S0_NB_TVDAC	6 19
PP1V5_S0_NB_VCCD_HMPLL	6 19
PP1V5_S0_NB_VCCD_HMPLL	6 17
PP1V5_S0_NB_VCCD_LVDS	17 19
PP1V5_S0_NB_VCCAUX	6 16 17 19
PP1V8_S3_MEM_NB	6 14 16 19
PP2V5_S0_NB_VCCSYNCR	17 19
PP2V5_S0_NB_VCC_TXLVDS	17 19
PP2V5_S0_NB_VCCA_3GBG	6 17 19
PP2V5_S0_NB_VCCA_LVDS	17 19
PP3V3_S0_NB	6 14 20
PP3V3_S0_NB_TVDAC	6
PP3V3_S0_NB_VCC_HV	6 17 19

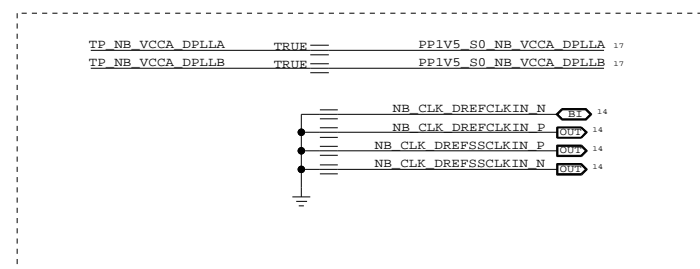
TVOUT DISABLE



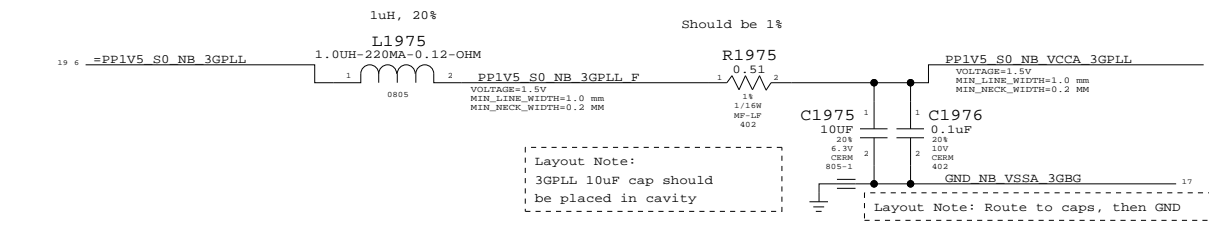
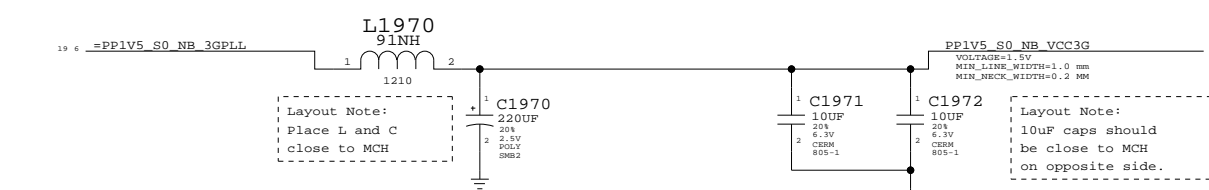
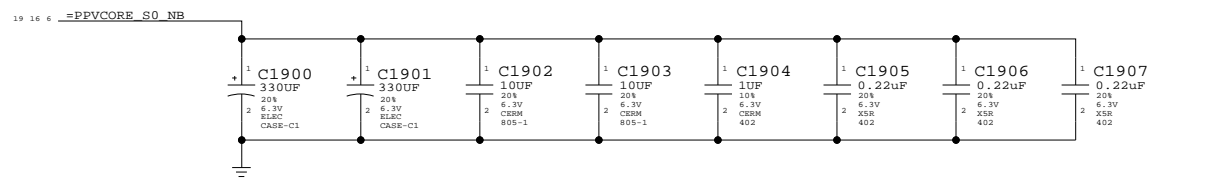
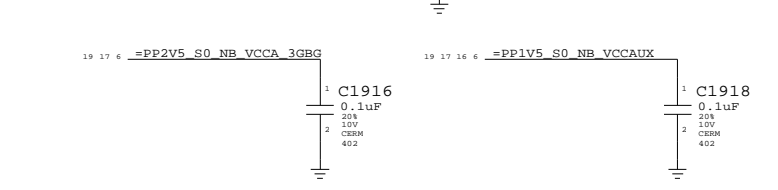
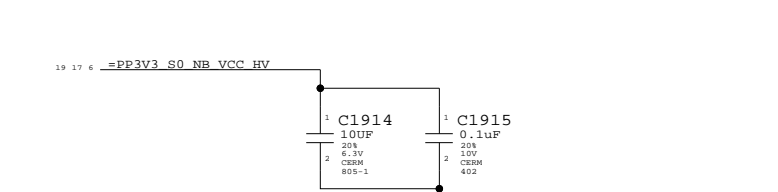
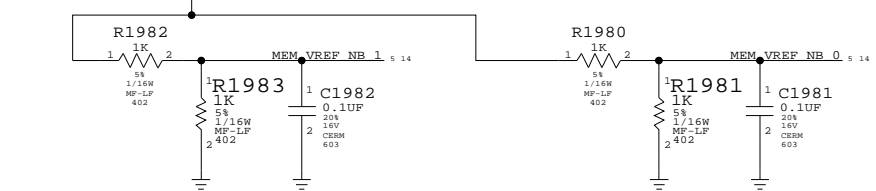
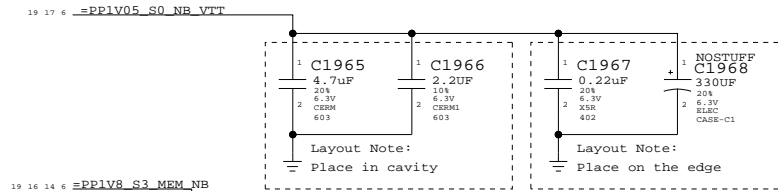
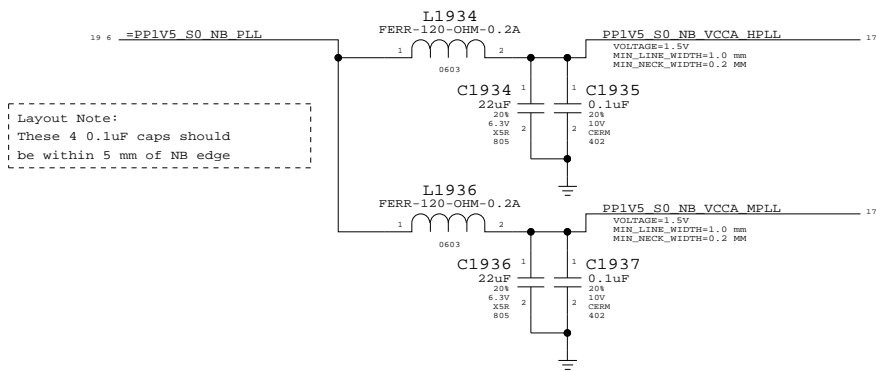
LVDS DISABLE



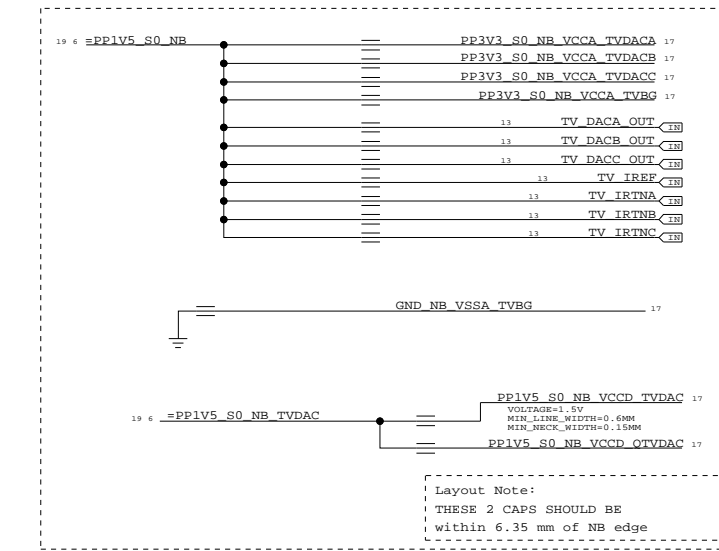
DISPLAY DISABLE



Layout Note:
These 4 0.1uF caps should be within 5 mm of NB edge



TVOUT DISABLE



Layout Note:
THESE 2 CAPS SHOULD BE WITHIN 6.35 mm OF NB EDGE

NB (GM) Decoupling

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

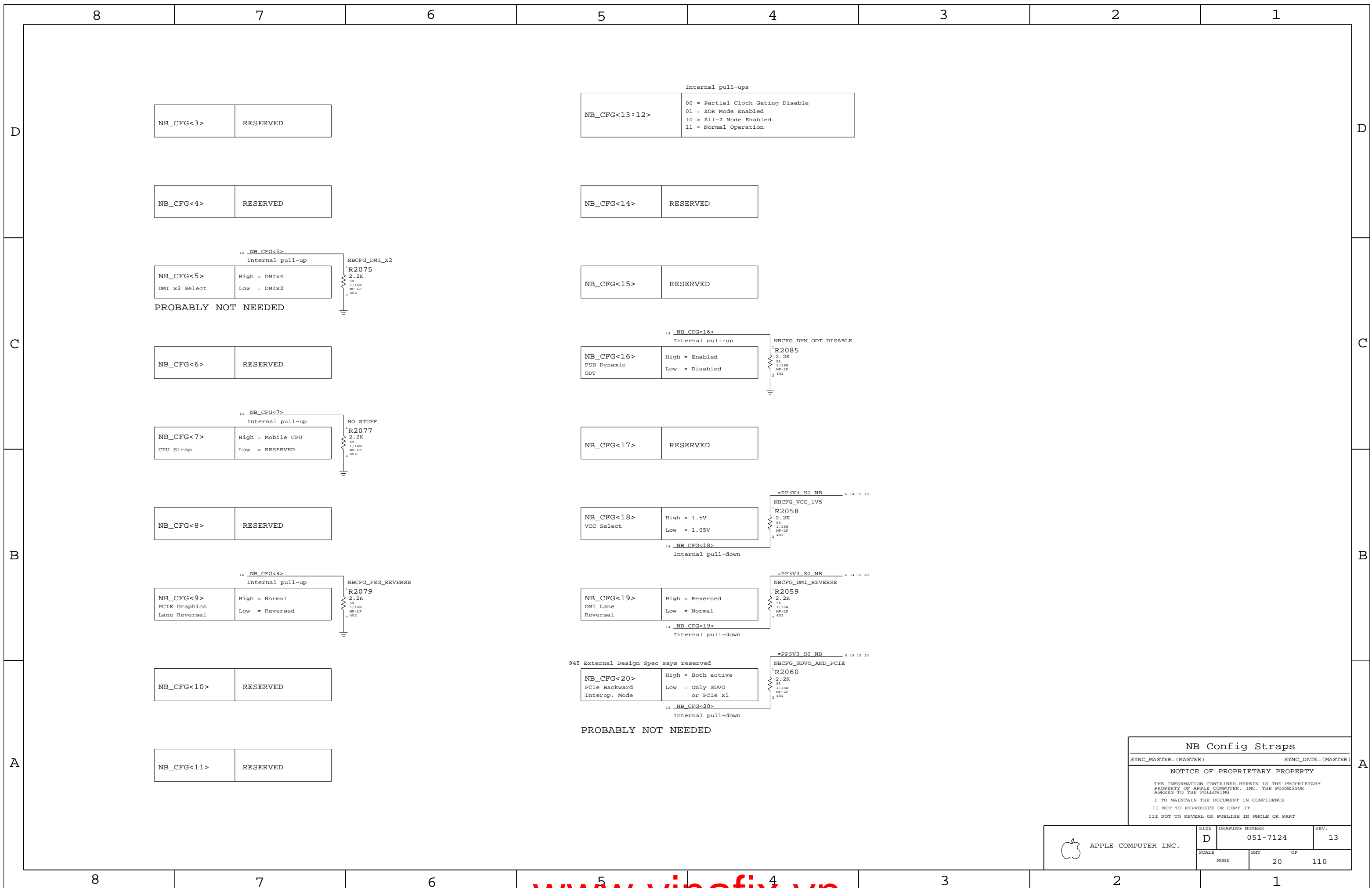
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	D	051-7124	13
SCALE	SHT	OF	
NONE	19	110	



Internal pull-ups

NB_CFG<13:12>	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal Operation
---------------	--

NB_CFG<3>	RESERVED
-----------	----------

NB_CFG<14>	RESERVED
------------	----------

NB_CFG<4>	RESERVED
-----------	----------

14 NB_CFG<5>
Internal pull-up

NB_CFG<5>	High = DMIX4 DMI x2 Select Low = DMIX2
-----------	--

PROBABLY NOT NEEDED

NBCFG_DMI_X2
R2075
2.2K
5%
1/16W
MF-LP
402

NB_CFG<15>	RESERVED
------------	----------

NB_CFG<6>	RESERVED
-----------	----------

14 NB_CFG<16>
Internal pull-up

NB_CFG<16>	High = Enabled FSB Dynamic ODT Low = Disabled
------------	--

NBCFG_DYN_ODT_DISABLE
R2085
2.2K
5%
1/16W
MF-LP
402

14 NB_CFG<7>
Internal pull-up

NB_CFG<7>	High = Mobile CPU CPU Strap Low = RESERVED
-----------	--

NO STUFF
R2077
2.2K
5%
1/16W
MF-LP
402

NB_CFG<17>	RESERVED
------------	----------

NB_CFG<8>	RESERVED
-----------	----------

14 NB_CFG<18>
Internal pull-down

NB_CFG<18>	High = 1.5V VCC Select Low = 1.05V
------------	--

=PP3V3_S0_NB
NBCFG_VCC_LV5
R2058
2.2K
5%
1/16W
MF-LP
402

14 NB_CFG<9>
Internal pull-up

NB_CFG<9>	High = Normal PCIe Graphics Lane Reversal Low = Reversed
-----------	---

NBCFG_PEG_REVERSE
R2079
2.2K
5%
1/16W
MF-LP
402

14 NB_CFG<19>
Internal pull-down

NB_CFG<19>	High = Reversed DMI Lane Reversal Low = Normal
------------	---

=PP3V3_S0_NB
NBCFG_DMI_REVERSE
R2059
2.2K
5%
1/16W
MF-LP
402

NB_CFG<10>	RESERVED
------------	----------

945 External Design Spec says reserved

14 NB_CFG<20>
Internal pull-down

NB_CFG<20>	High = Both active PCIe Backward Interop. Mode Low = Only SDVO or PCIe x1
------------	---

=PP3V3_S0_NB
NBCFG_SDVO_AND_PCIE
R2060
2.2K
5%
1/16W
MF-LP
402

NB_CFG<11>	RESERVED
------------	----------

PROBABLY NOT NEEDED

NB Config Straps

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

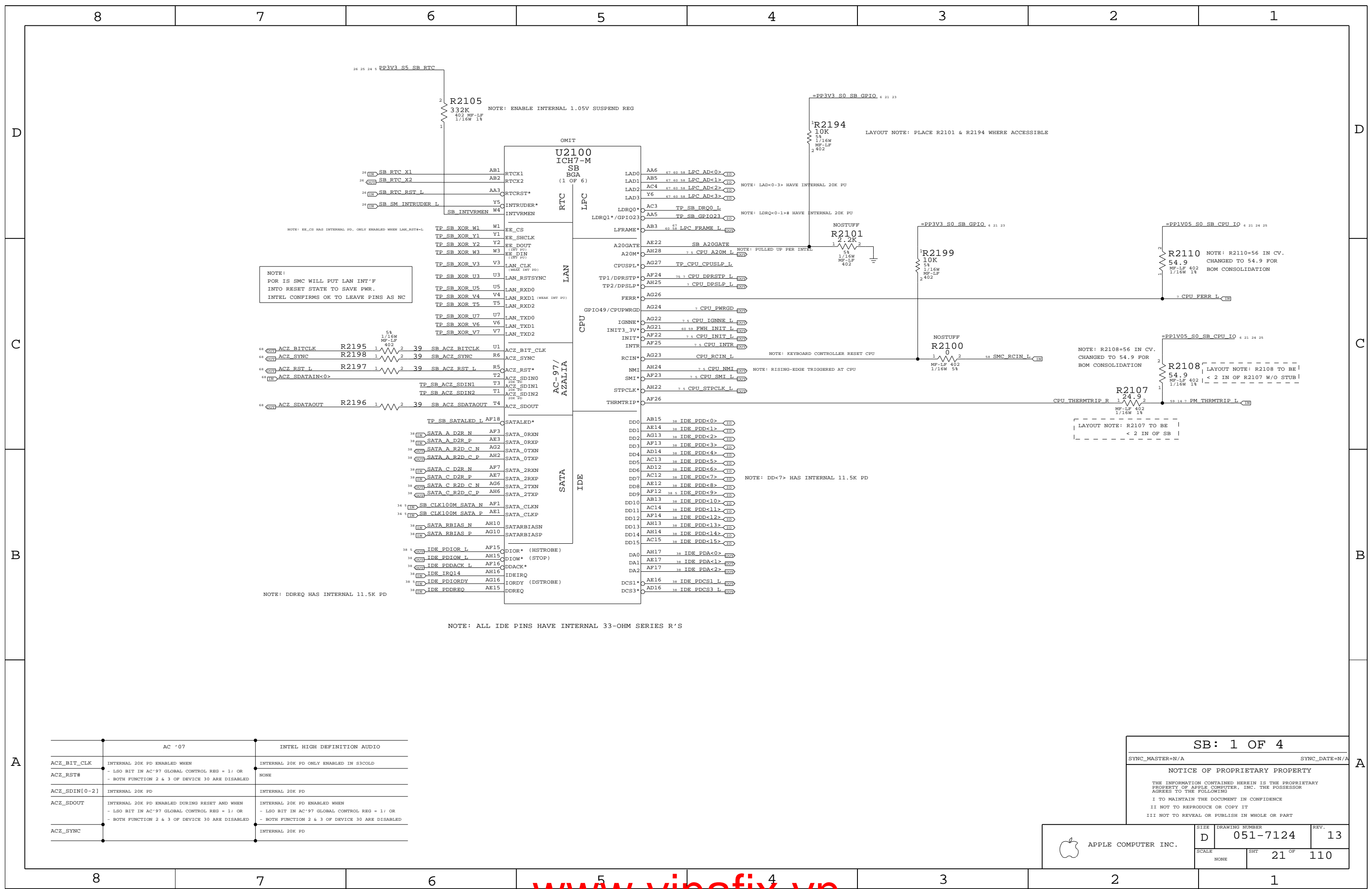
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	D	051-7124	13
SCALE	SHT	OF	
NONE	20	110	



NOTE:
 POR IS SMC WILL PUT LAN INT'F INTO RESET STATE TO SAVE PWR. INTEL CONFIRMS OK TO LEAVE PINS AS NC

NOTE: DDREQ HAS INTERNAL 11.5K PD

AC '07	INTEL HIGH DEFINITION AUDIO
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR
ACZ_RST#	NONE
ACZ_SDIN[0-2]	INTERNAL 20K PD
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
ACZ_SYNC	INTERNAL 20K PD

SB: 1 OF 4

SYNC_MASTER=N/A SYNC_DATE=N/A

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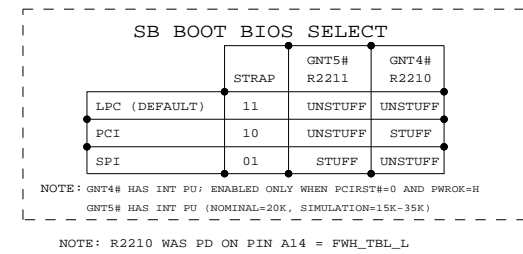
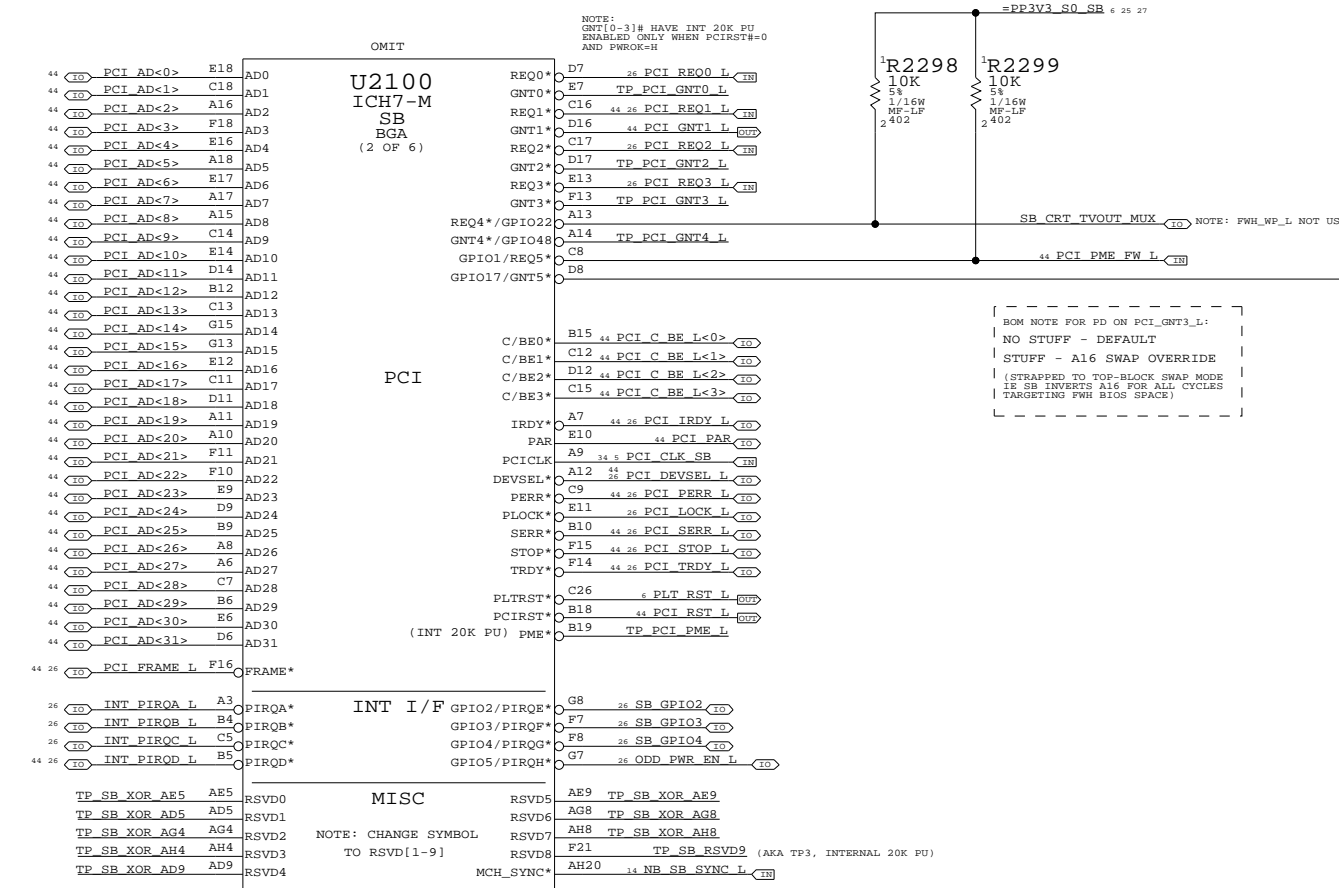
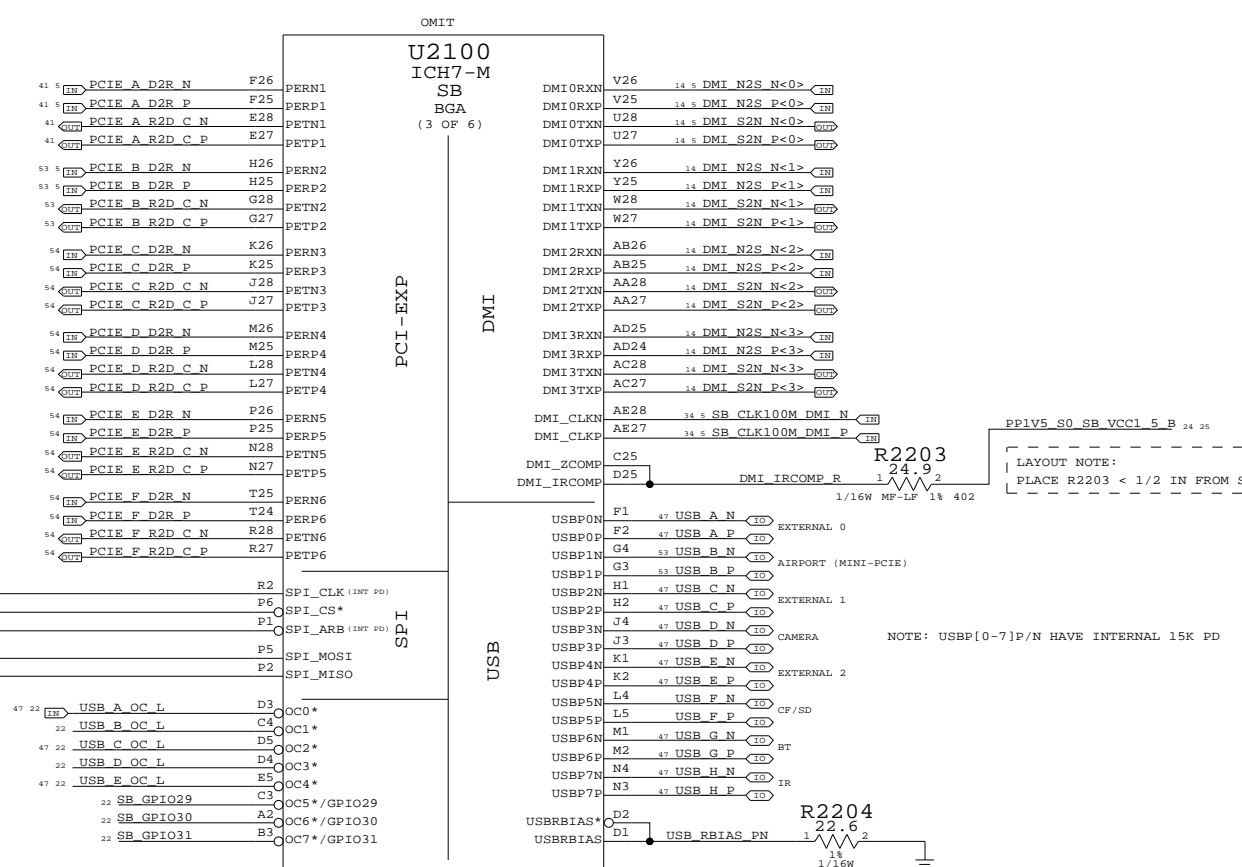
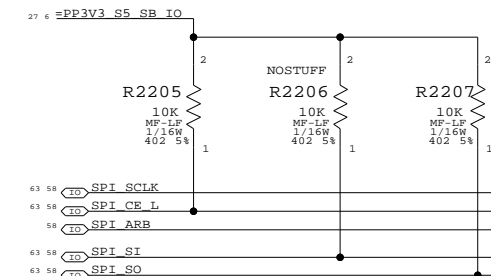
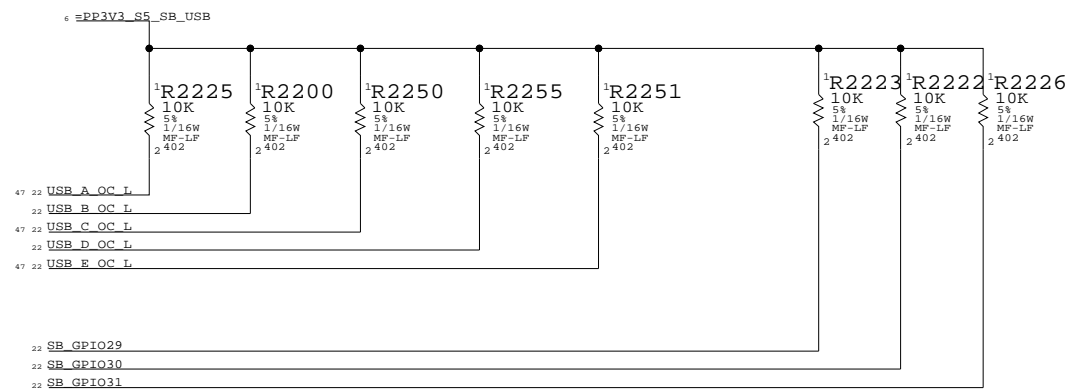
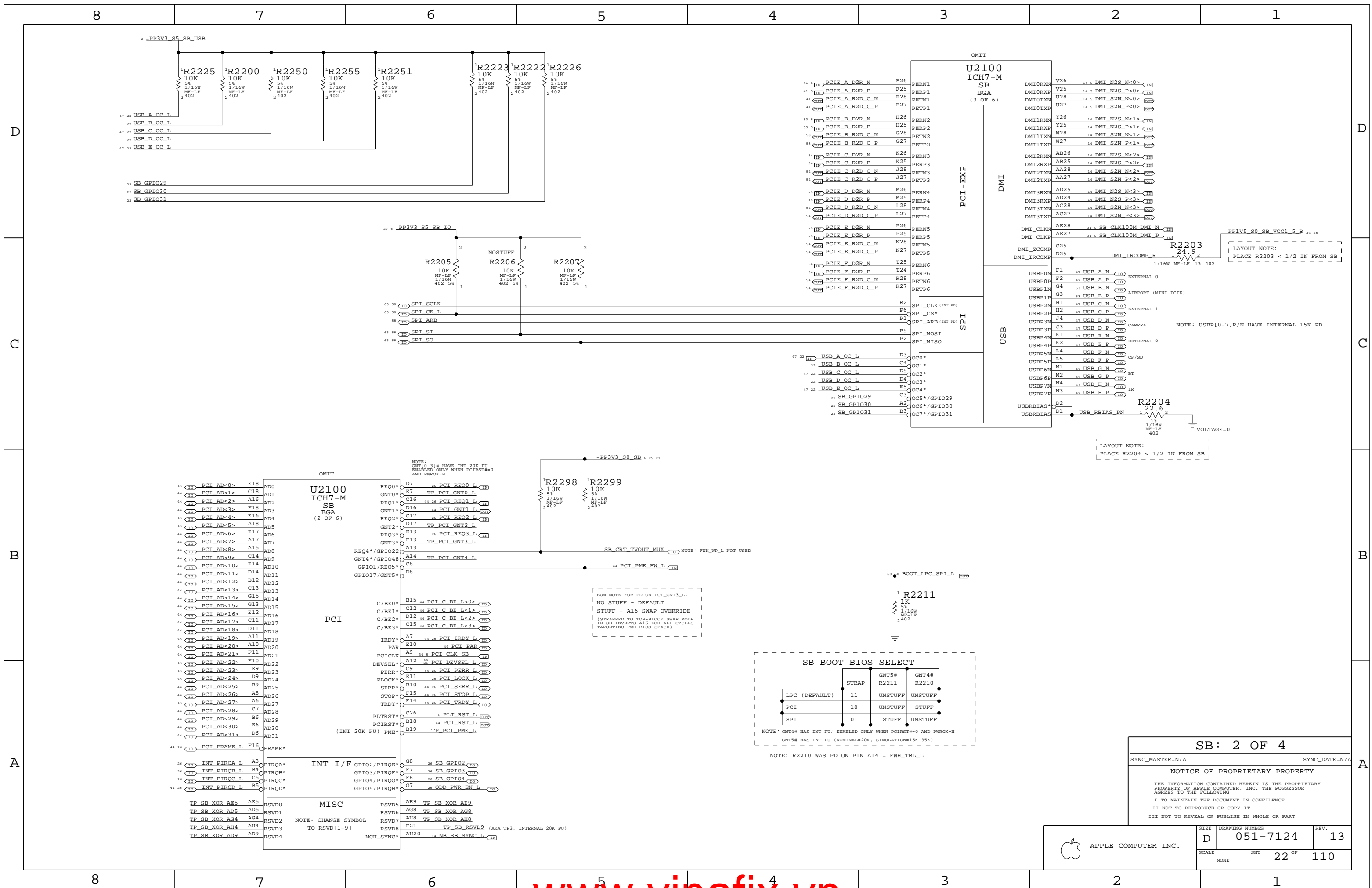
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	D	051-7124	13
SCALE	SHT	21 OF 110	
NONE			



SB: 2 OF 4

SYNC_MASTER=N/A SYNC_DATE=N/A

NOTICE OF PROPRIETARY PROPERTY

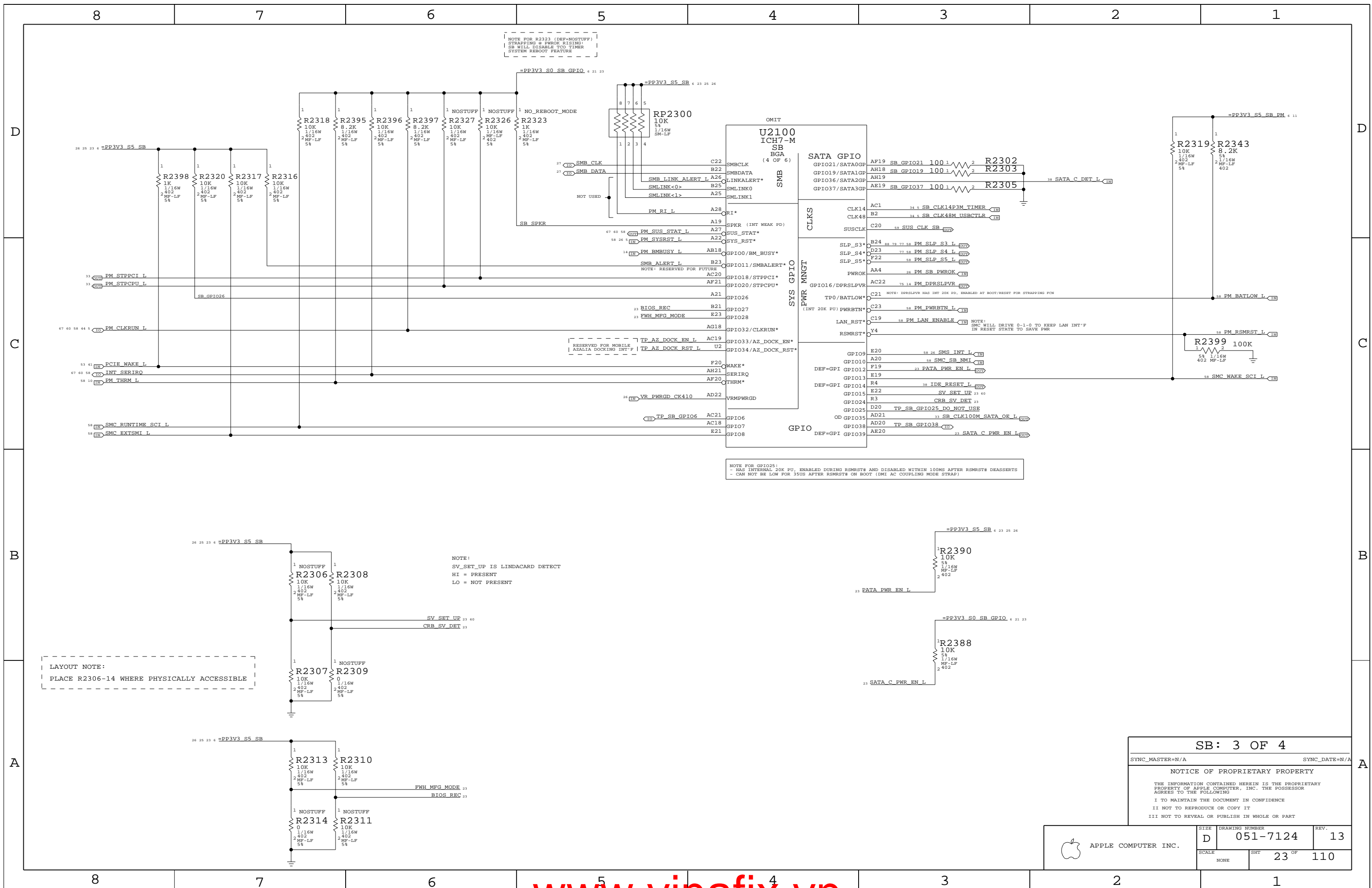
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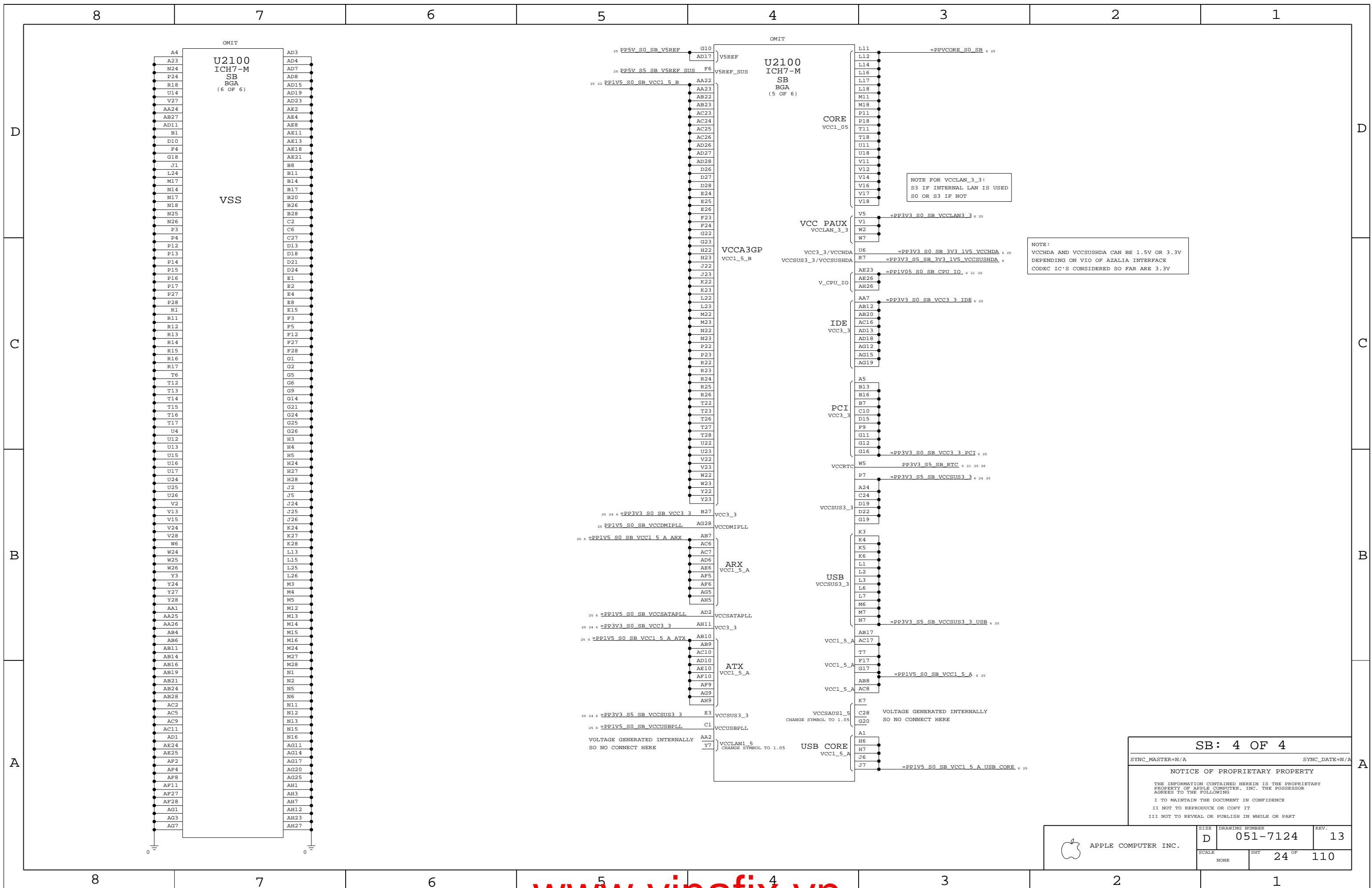
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SCALE	SHT	REV.
	NONE	22 OF 110	13



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	D	051-7124	13
SCALE	NONE	SHT	23 OF 110



NOTE FOR VCCLAN_3_3:
S3 IF INTERNAL LAN IS USED
S0 OR S3 IF NOT

NOTE:
VCC3_3 AND VCCSUS3_3 CAN BE 1.5V OR 3.3V
DEPENDING ON VIO OF AZALIA INTERFACE
CODIC IC'S CONSIDERED SO FAR ARE 3.3V

SB: 4 OF 4

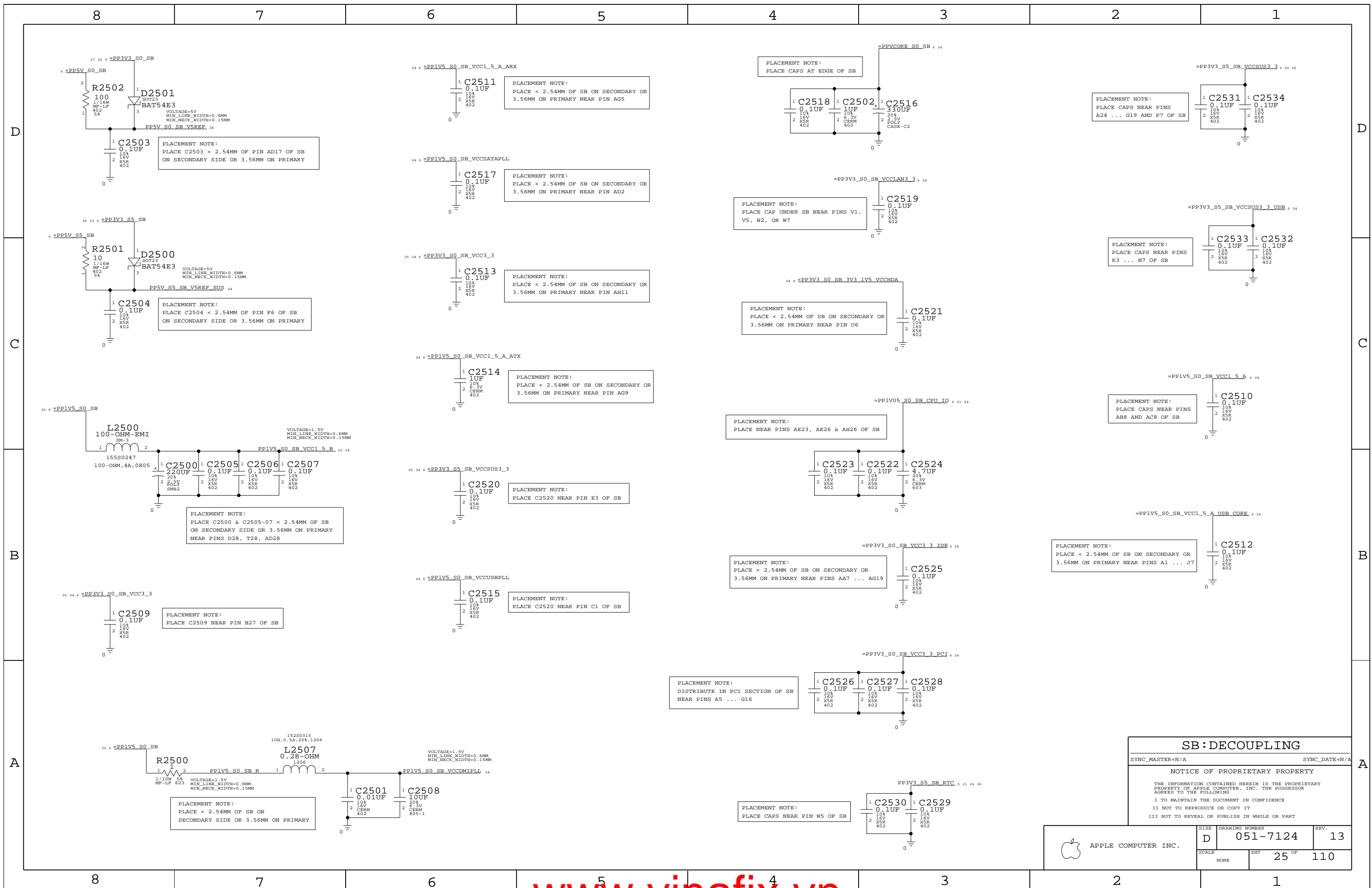
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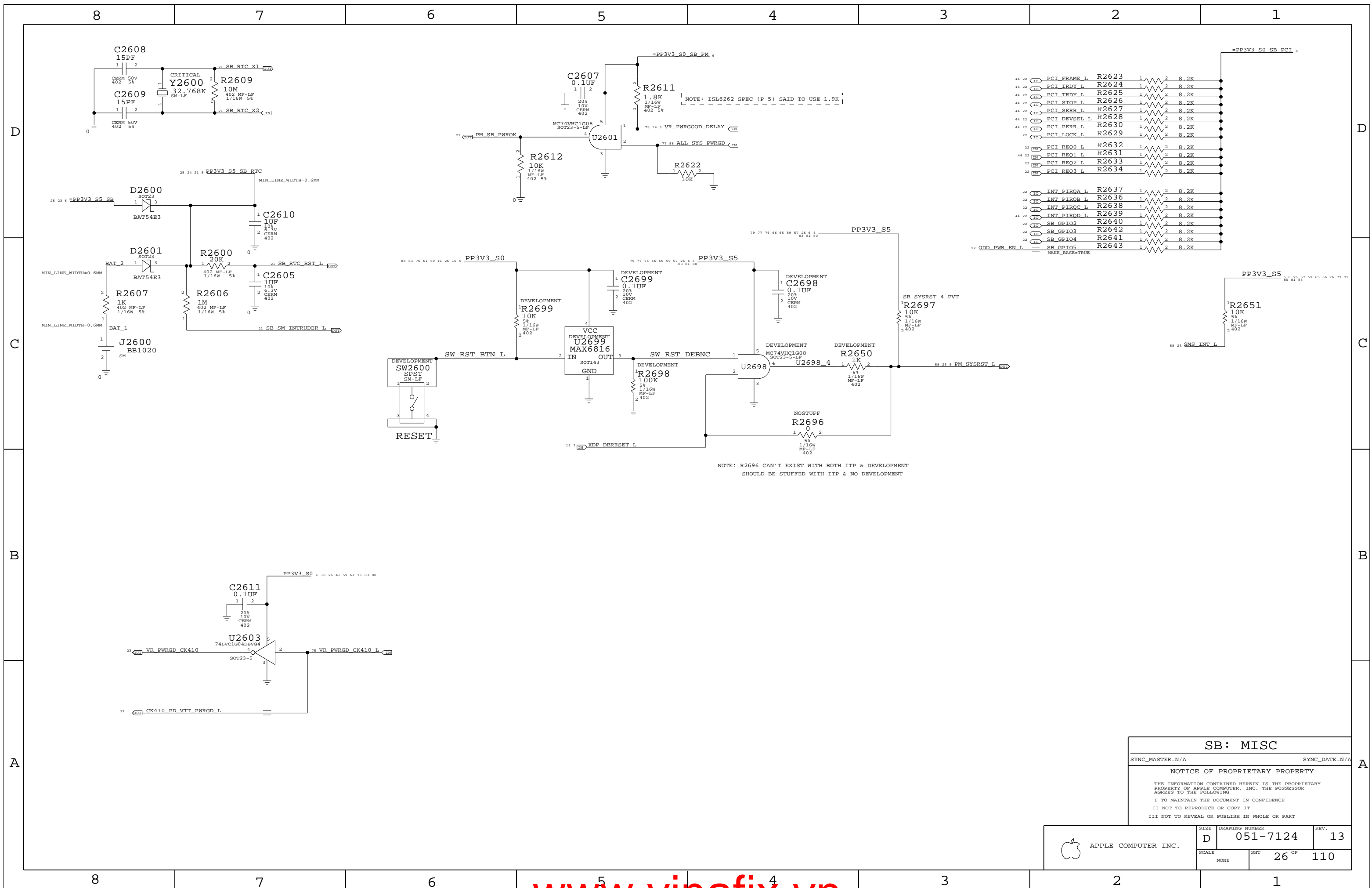
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	D	051-7124	13
SCALE	SHT	24 OF 110	
NONE			



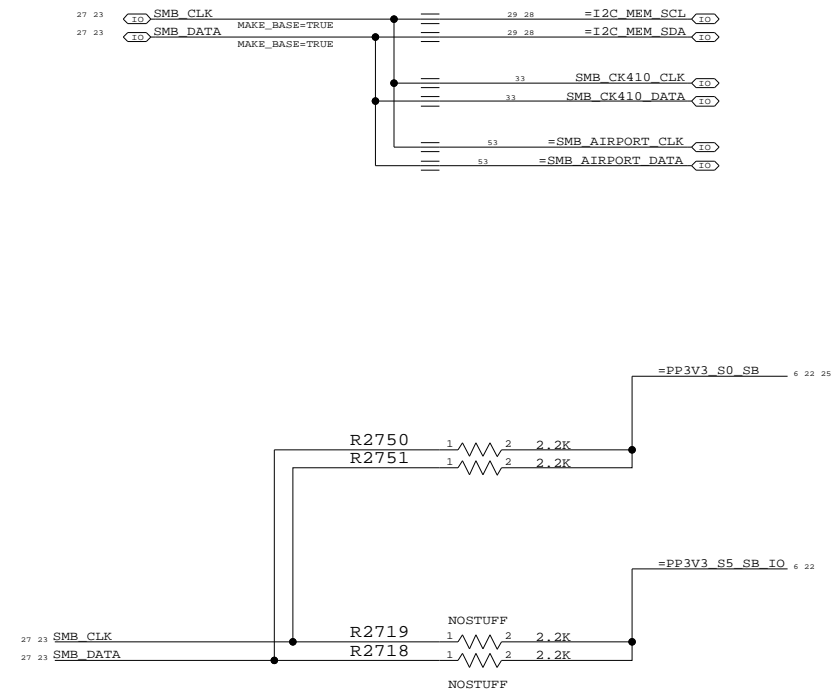


NOTE: R2696 CAN'T EXIST WITH BOTH ITP & DEVELOPMENT
SHOULD BE STUFFED WITH ITP & NO DEVELOPMENT

SB: MISC
 SYNC_MASTER=N/A SYNC_DATE=N/A
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	D	051-7124	13
SCALE	SHT	26 OF	110
NONE			

SB I2C BUSSES



SB: SMB HUB

SYNC_MASTER=N/A SYNC_DATE=N/A

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 APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7124	REV. 13
	SCALE NONE	SHIT 27 OF	110

Page Notes

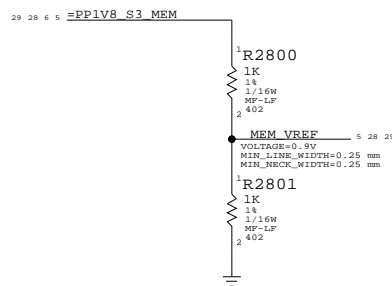
Power aliases required by this page:
 - =PP1V8_S3_MEM
 - =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
 - =I2C_MEM_SCL
 - =I2C_MEM_SDA

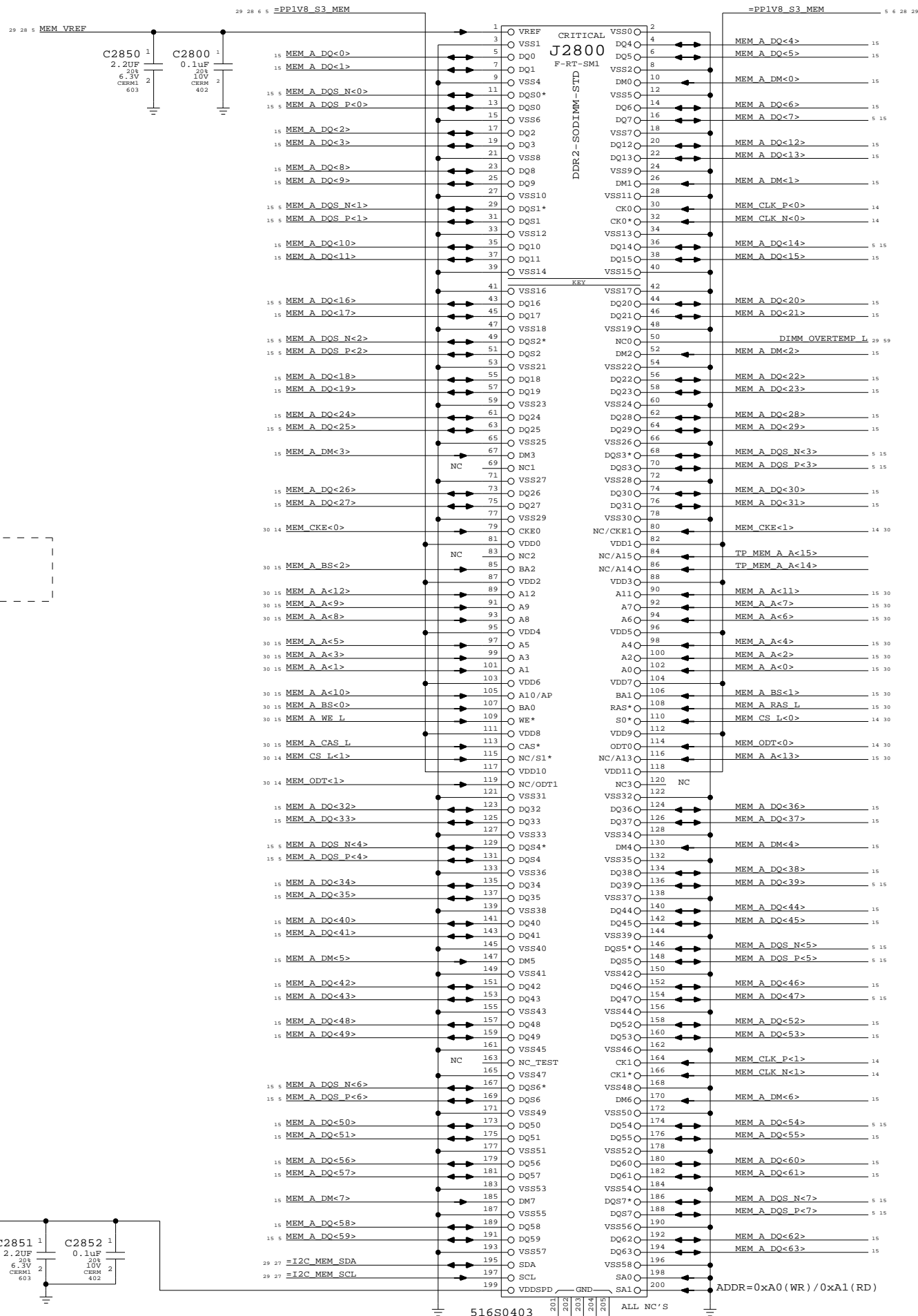
BOM options provided by this page:
 (NONE)

DDR2 VRef

One 0.1uF per connector

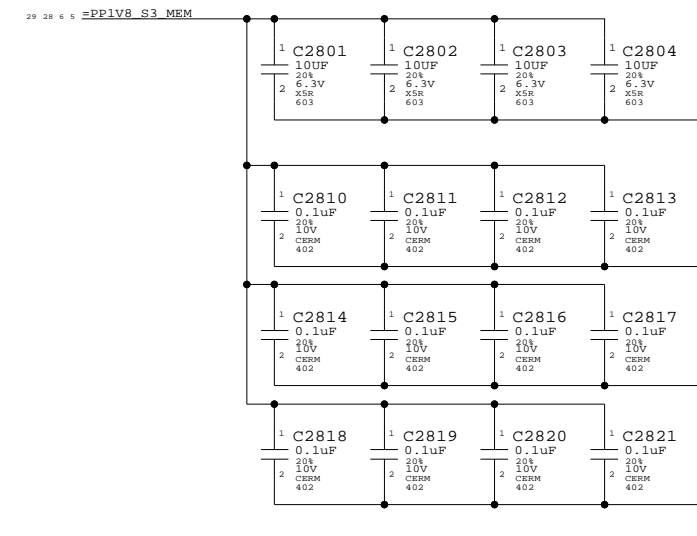


Yellow uses 10K divider and TLV2463 to drive MCH and DIMM connectors.
 (See Capell Valley pg 47)



DDR2 Bypass Caps

(For return current)



DDR2 SO-DIMM Connector A

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	13
SCALE	SHT	OF	
NONE	28	110	

Page Notes

Power aliases required by this page:
 - =PP1V8_S3_MEM
 - =PPSPD_S0_MEM (2.5V - 3.3V)

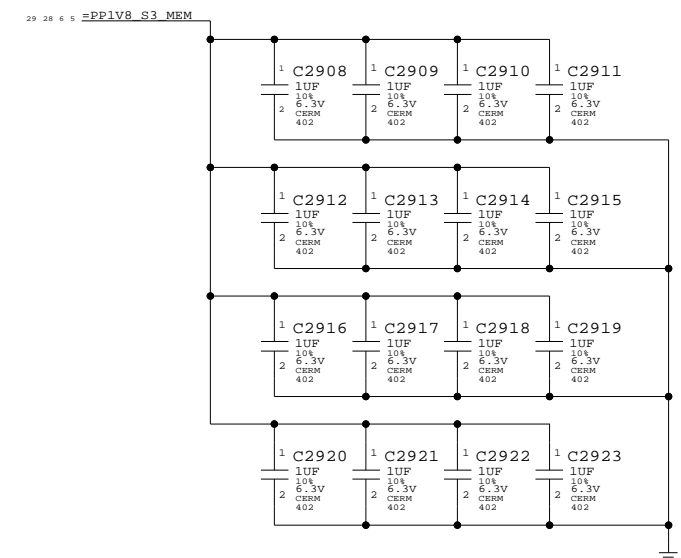
Signal aliases required by this page:
 - =I2C_MEM_SCL
 - =I2C_MEM_SDA

BOM options provided by this page:
 (NONE)

NOTE: This page does not supply VREF.
 The reference voltage must be provided by another page.



DDR2 Bypass Caps (For return current)



DDR2 SO-DIMM Connector B

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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	D	051-7124	13
SCALE	SHT	OF	
NONE	29	110	

8

7

6

5

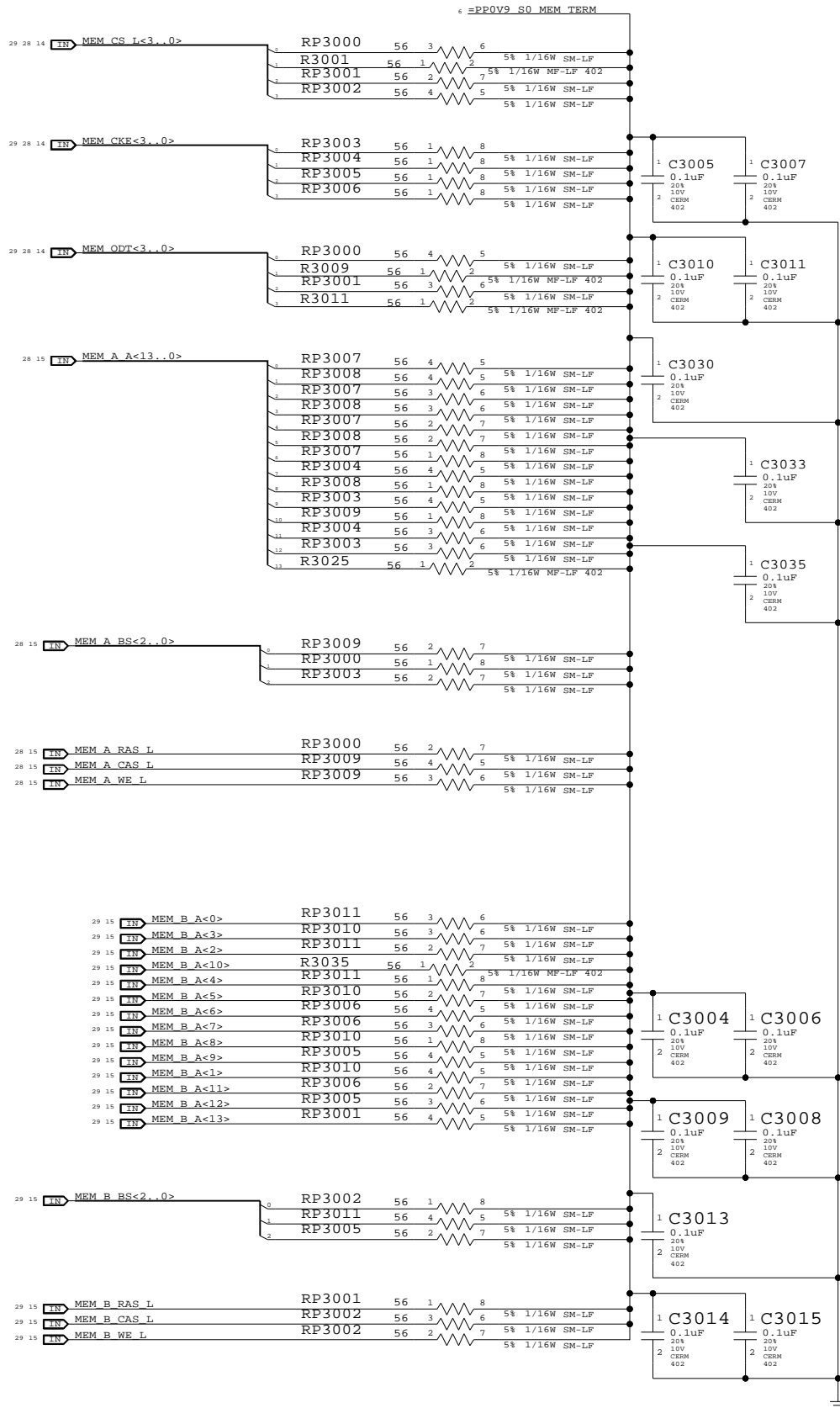
4

3

2

1

One cap for each side of every RPAK, one cap for every two discrete resistors
BOMOPTION shown at the top of each group applies to every part below it



Memory Active Termination

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	D	051-7124	13
SCALE	SHT OF		
NONE	30		110

8

7

6

5

4

3

2

1

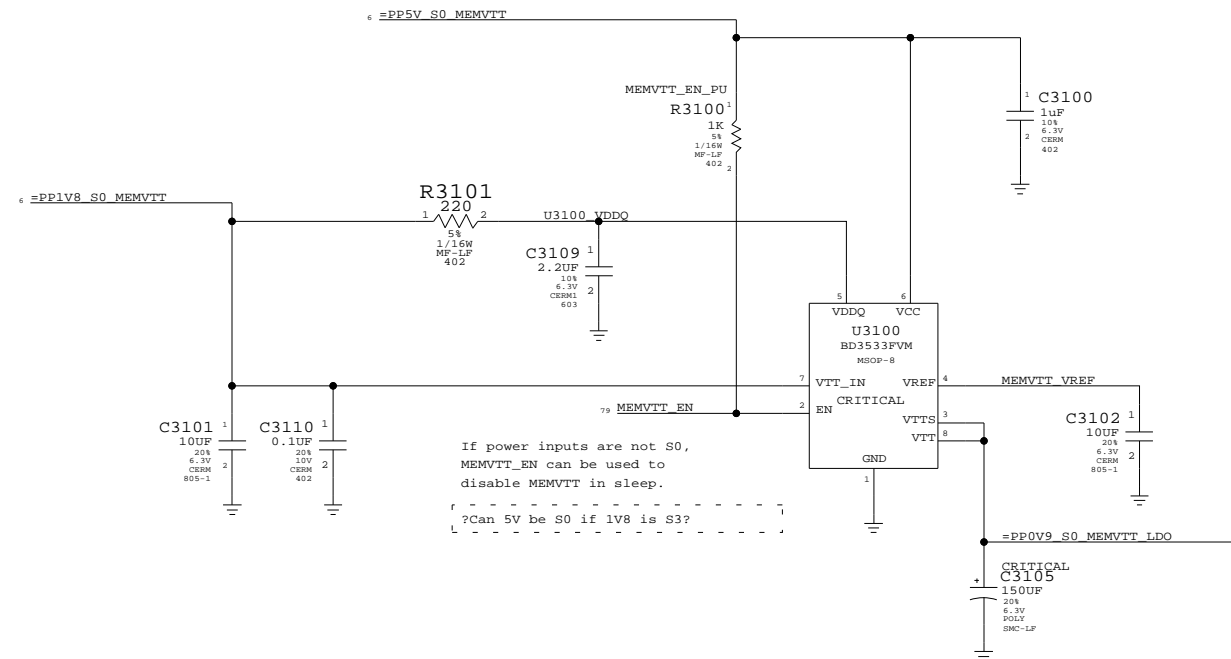
Page Notes

Power aliases required by this page:
 - =PP5V_S0_MEMVTT
 - =PP1V8_S0_MEMVTT
 - =PP0V9_S0_MEMVTT_LDO

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

DDR2 Vtt Regulator



Memory Vtt Supply

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

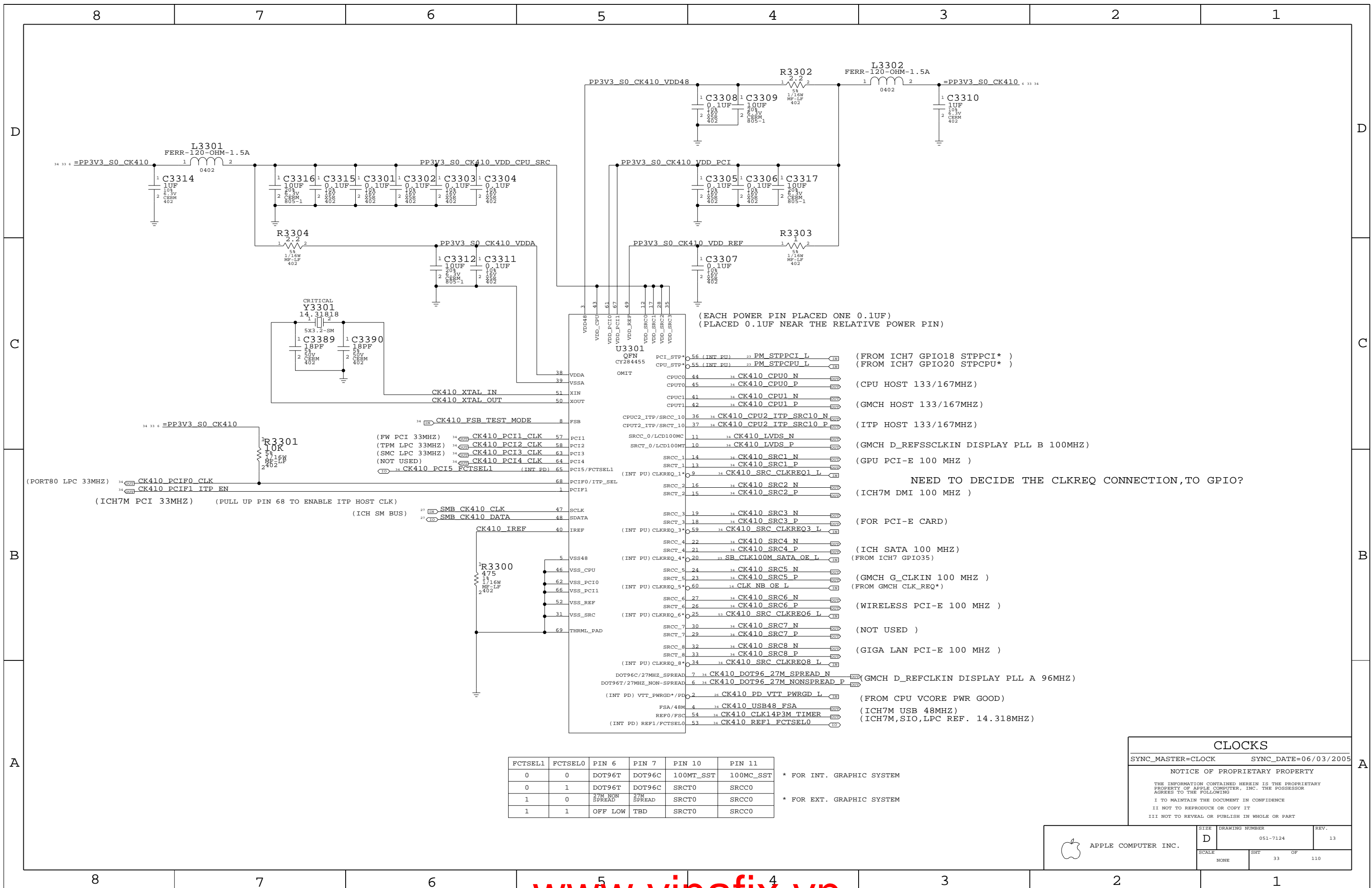
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	D	051-7124	13
SCALE	SHT	OF	
NONE	31	110	



(EACH POWER PIN PLACED ONE 0.1UF)
(PLACED 0.1UF NEAR THE RELATIVE POWER PIN)

(FROM ICH7 GPIO18 STPPCI*)
(FROM ICH7 GPIO20 STPCPU*)

(CPU HOST 133/167MHZ)

(GMCH HOST 133/167MHZ)

(ITP HOST 133/167MHZ)

(GMCH D_REFSSCLKIN DISPLAY PLL B 100MHZ)

(GPU PCI-E 100 MHZ)

NEED TO DECIDE THE CLKREQ CONNECTION, TO GPIO?

(ICH7M DMI 100 MHZ)

(FOR PCI-E CARD)

(ICH SATA 100 MHZ)

(FROM ICH7 GPIO35)

(GMCH G_CLKIN 100 MHZ)

(FROM GMCH CLK_REQ*)

(WIRELESS PCI-E 100 MHZ)

(NOT USED)

(GIGA LAN PCI-E 100 MHZ)

(GMCH D_REFCLKIN DISPLAY PLL A 96MHZ)

(FROM CPU VCORE PWR GOOD)

(ICH7M USB 48MHZ)

(ICH7M,SIO,LPC REF. 14.318MHZ)

FCTSEL1	FCTSEL0	PIN 6	PIN 7	PIN 10	PIN 11
0	0	DOT96T	DOT96C	100MT_SST	100MC_SST
0	1	DOT96T	DOT96C	SRCT0	SRCC0
1	0	27M NON SPREAD	27M SPREAD	SRCT0	SRCC0
1	1	OFF LOW	TBD	SRCT0	SRCC0

* FOR INT. GRAPHIC SYSTEM

* FOR EXT. GRAPHIC SYSTEM

CLOCKS

SYNC_MASTER=CLOCK SYNC_DATE=06/03/2005

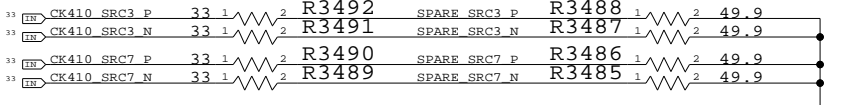
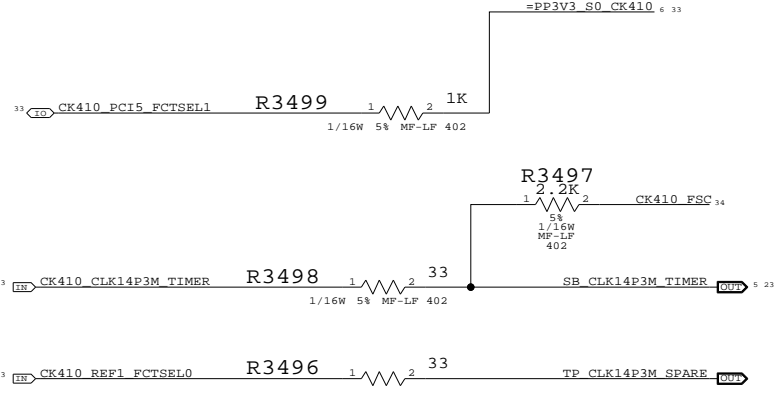
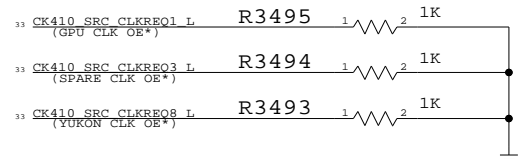
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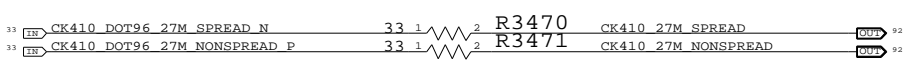
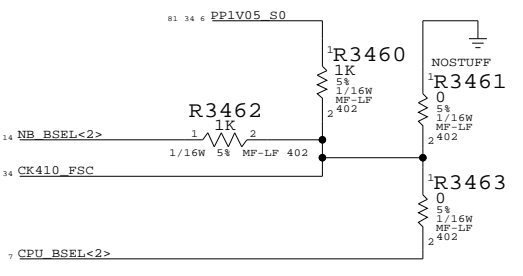
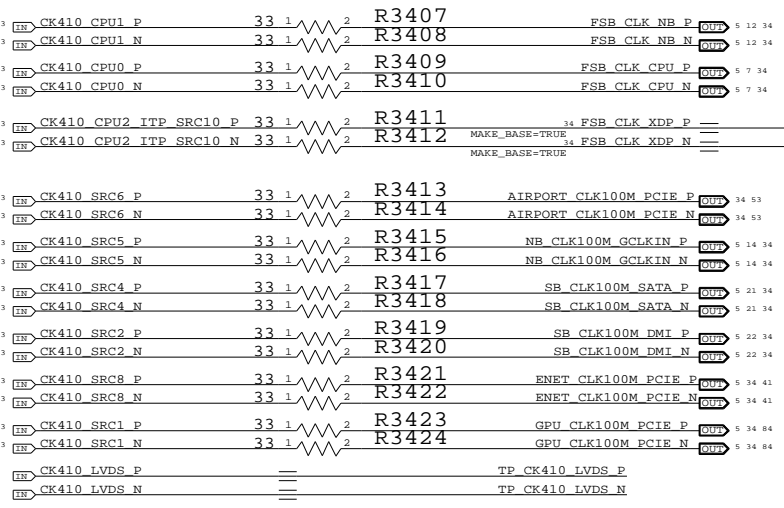
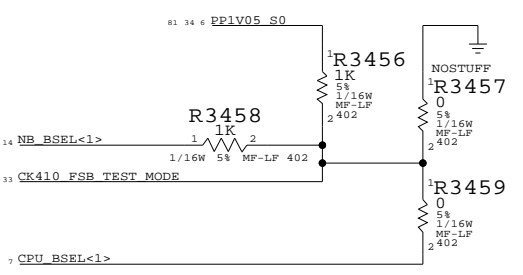
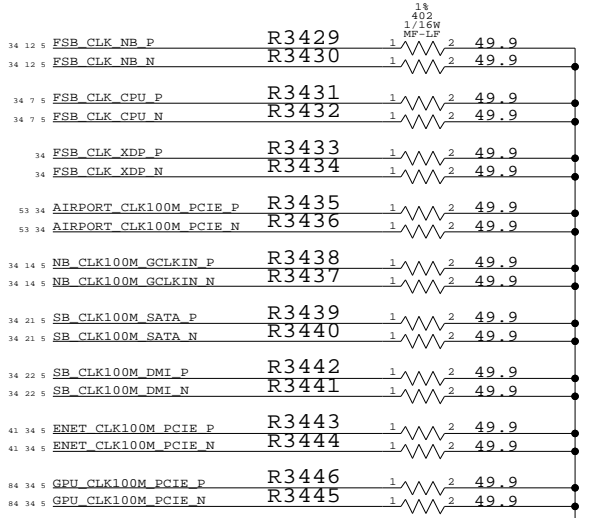
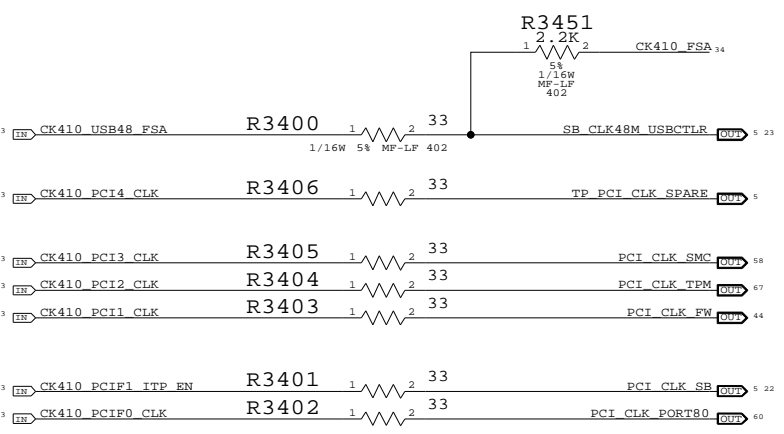
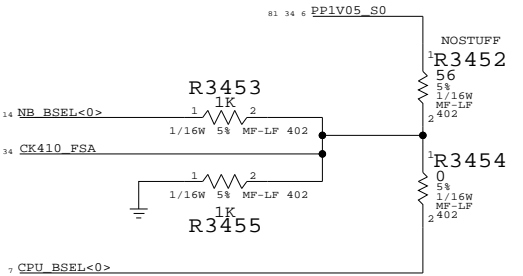
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	13
SCALE	SHT	OF	110
NONE	33		

NOTE: USE THESE PULL-DOWNS IF NOT CONNECTED TO GPIO'S



FSB FREQUENCY SELECT:

	STUFF	NO STUFF
CPU DRIVEN	R3453 R3454 R3455	R3456 R3457
533MHZ (133MHZ CPU CLK)	R3452 R3454 R3455	R3456 R3457
667MHZ (166MHZ CPU CLK)	R3452 R3454 R3455	R3456 R3457



CLOCKS: TERMINATIONS

SYNC_MASTER=N/A SYNC_DATE=N/A

NOTICE OF PROPRIETARY PROPERTY

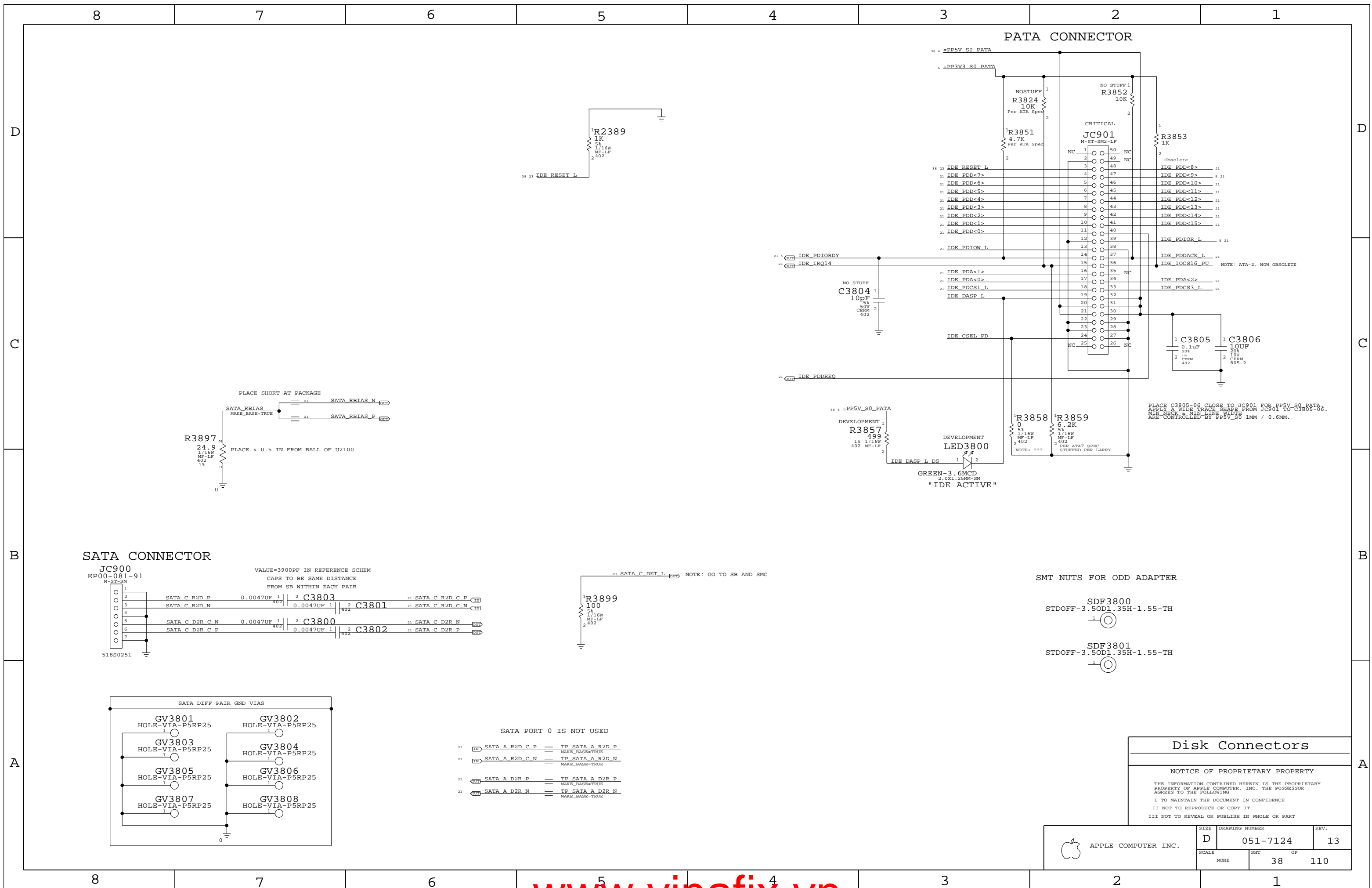
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	13
SCALE	SHT	OF	110
NONE	34		



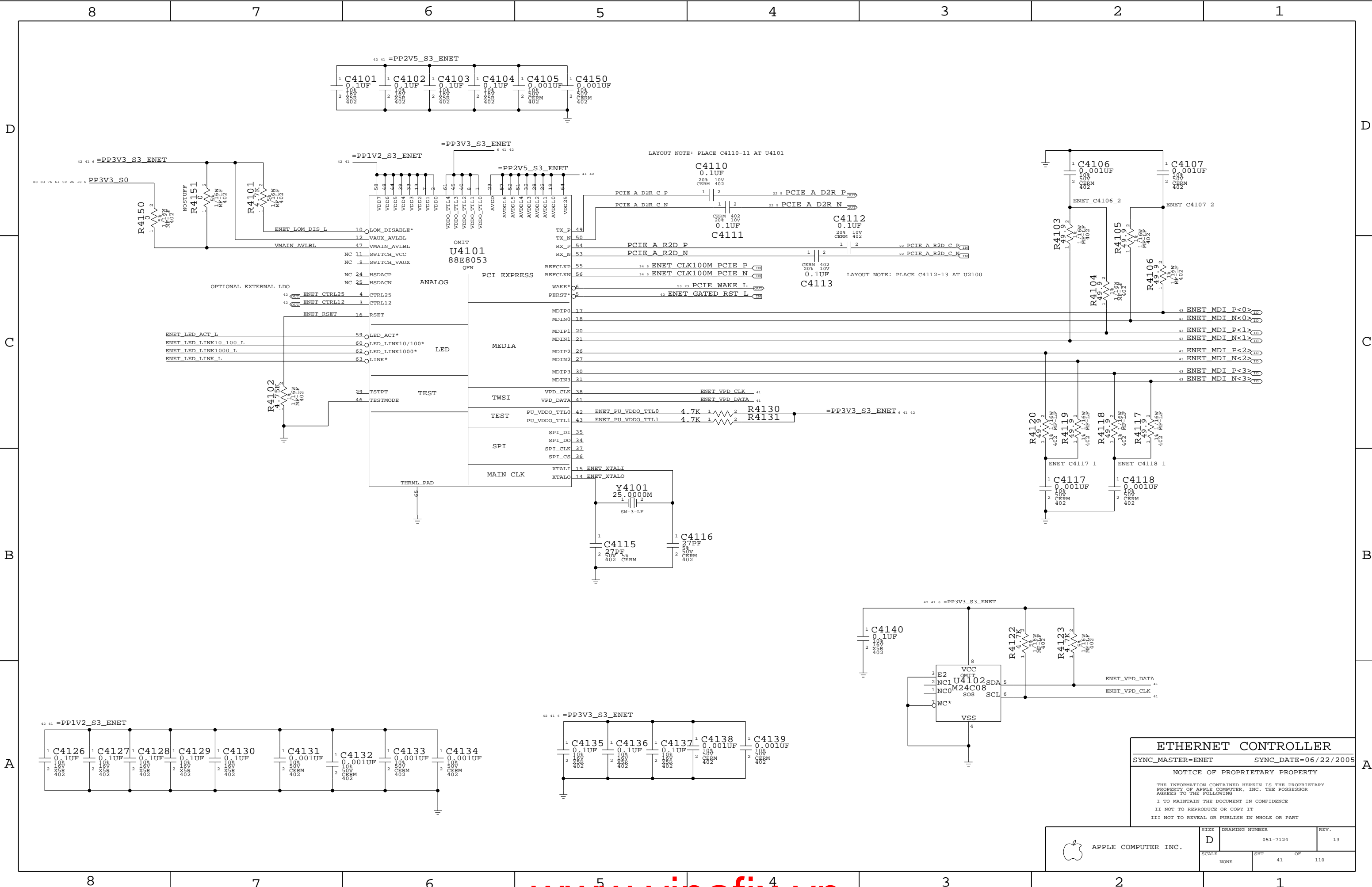
Disk Connectors

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	SCALE NONE	SHEET 38	OF 110



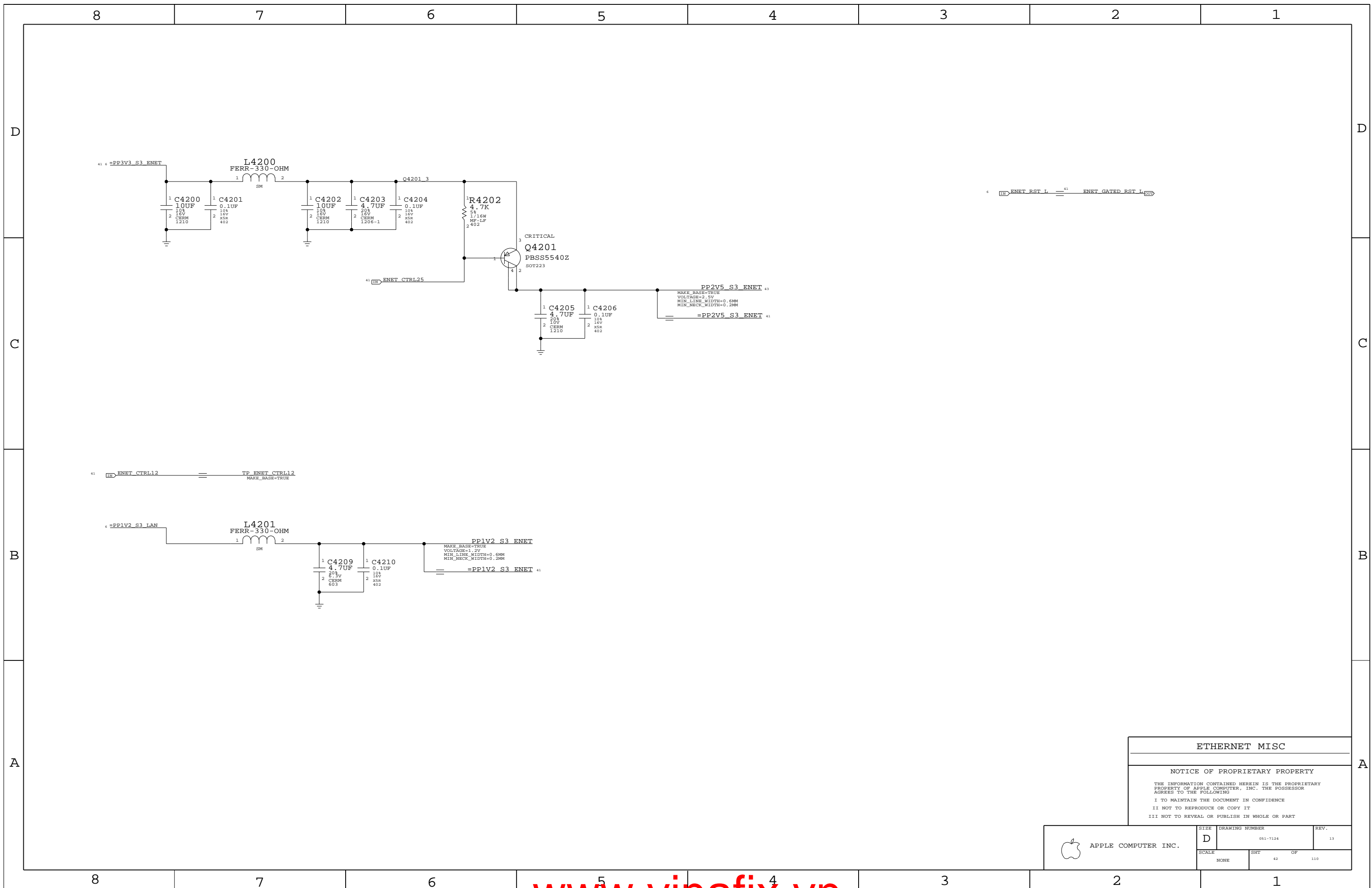
ETHERNET CONTROLLER

SYNC_MASTER=ENET SYNC_DATE=06/22/2005

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	13
SCALE	NONE	SHT	41 OF 110



ETHERNET MISC

NOTICE OF PROPRIETARY PROPERTY

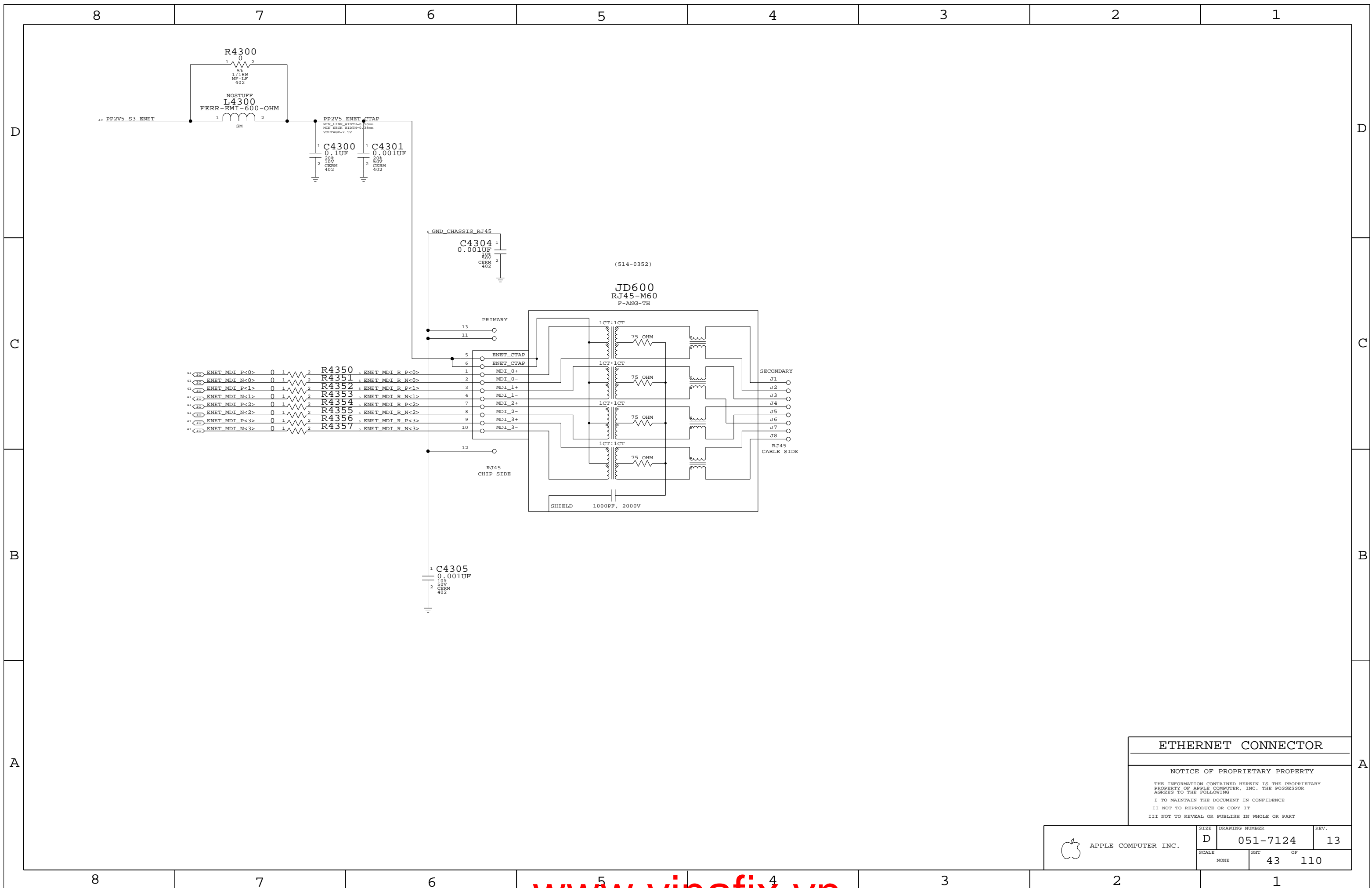
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7124	REV. 13
	SCALE NONE	SHEET 42	OF 110



ETHERNET CONNECTOR

NOTICE OF PROPRIETARY PROPERTY

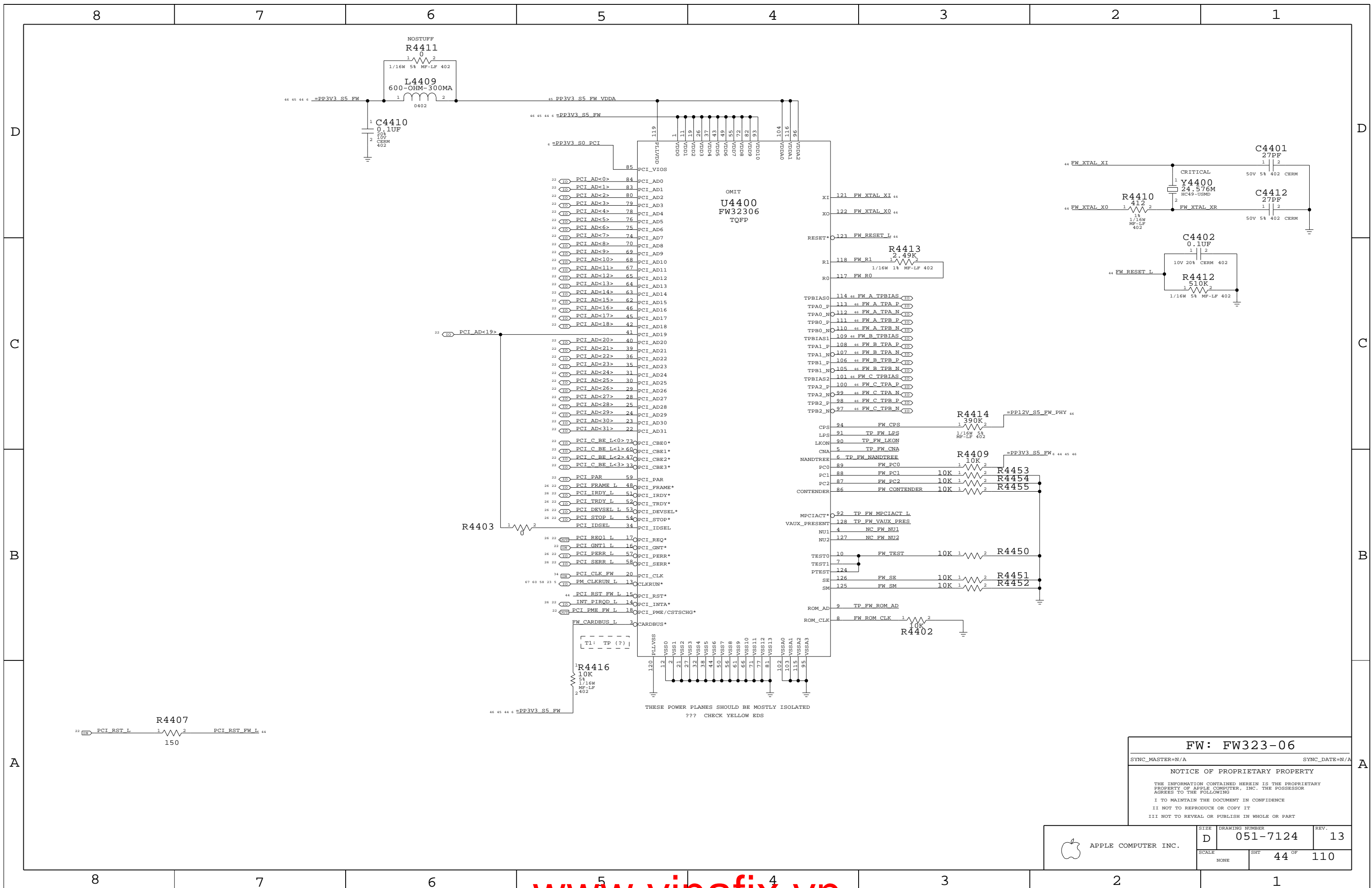
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	13
SCALE		SHT	OF
NONE		43	110



FW: FW323-06

SYNC_MASTER=N/A SYNC_DATE=N/A

NOTICE OF PROPRIETARY PROPERTY

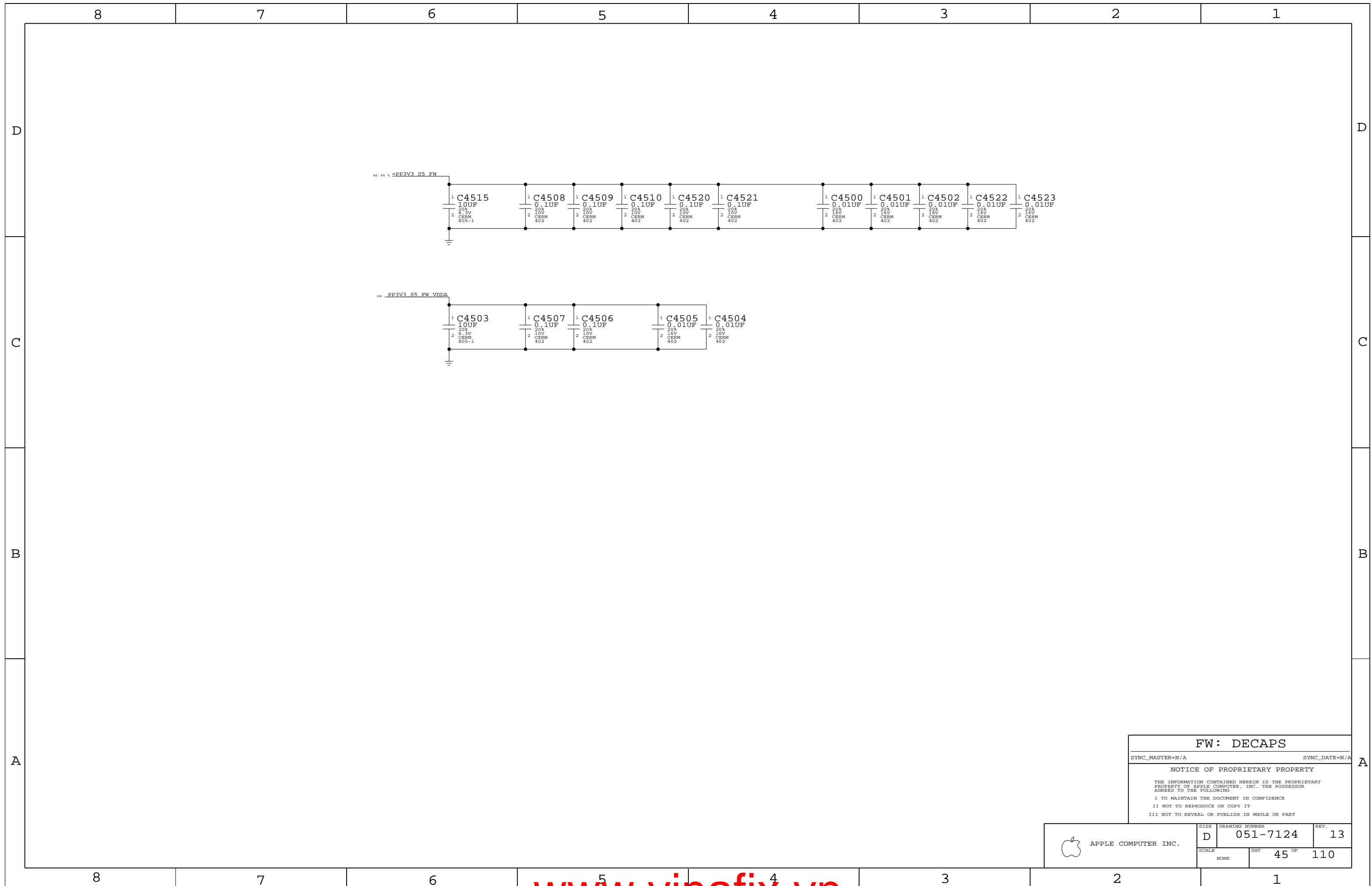
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	13
SCALE	SHT	44 OF	110
NONE			



FW: DECAPS

SYNC_MASTER=N/A SYNC_DATE=N/A

NOTICE OF PROPRIETARY PROPERTY

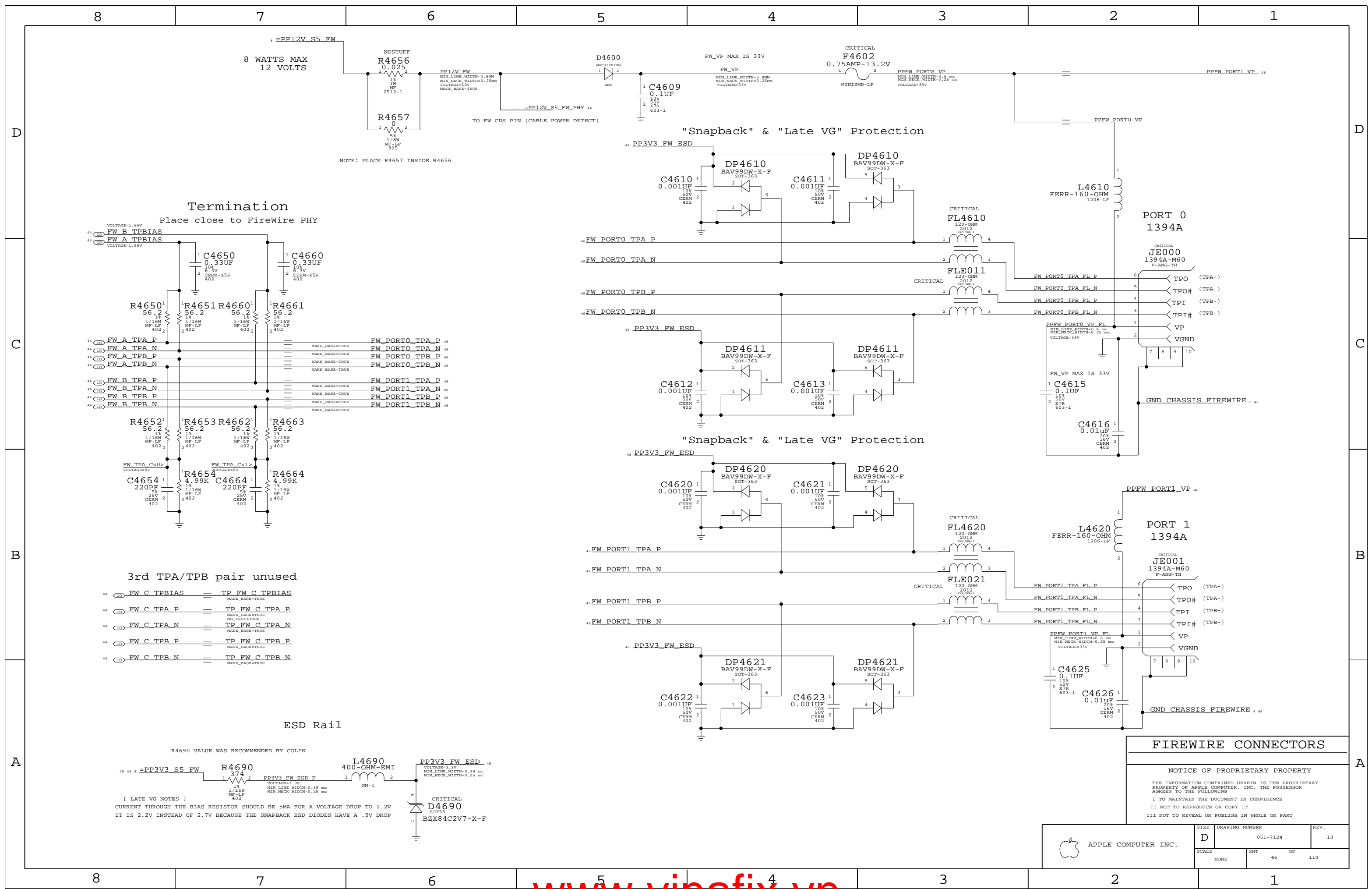
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7124	REV. 13
	SCALE NONE	SHT 45 OF	110



FIREWIRE CONNECTORS

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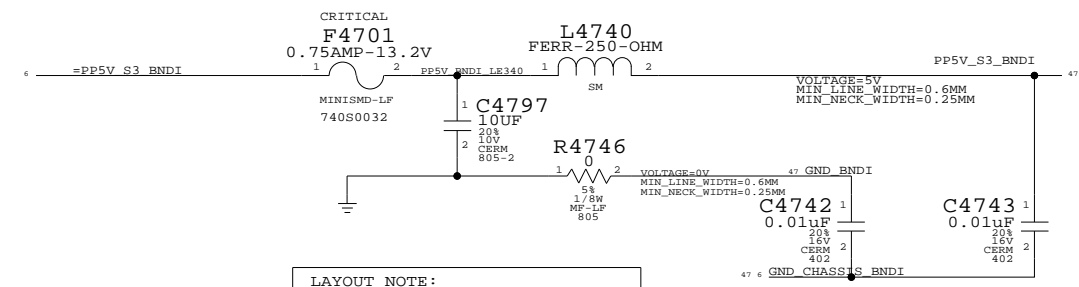
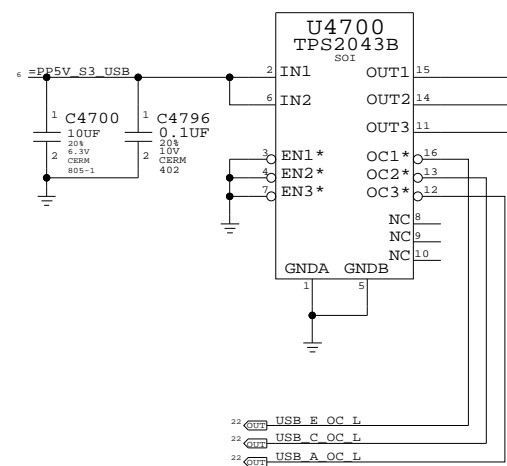
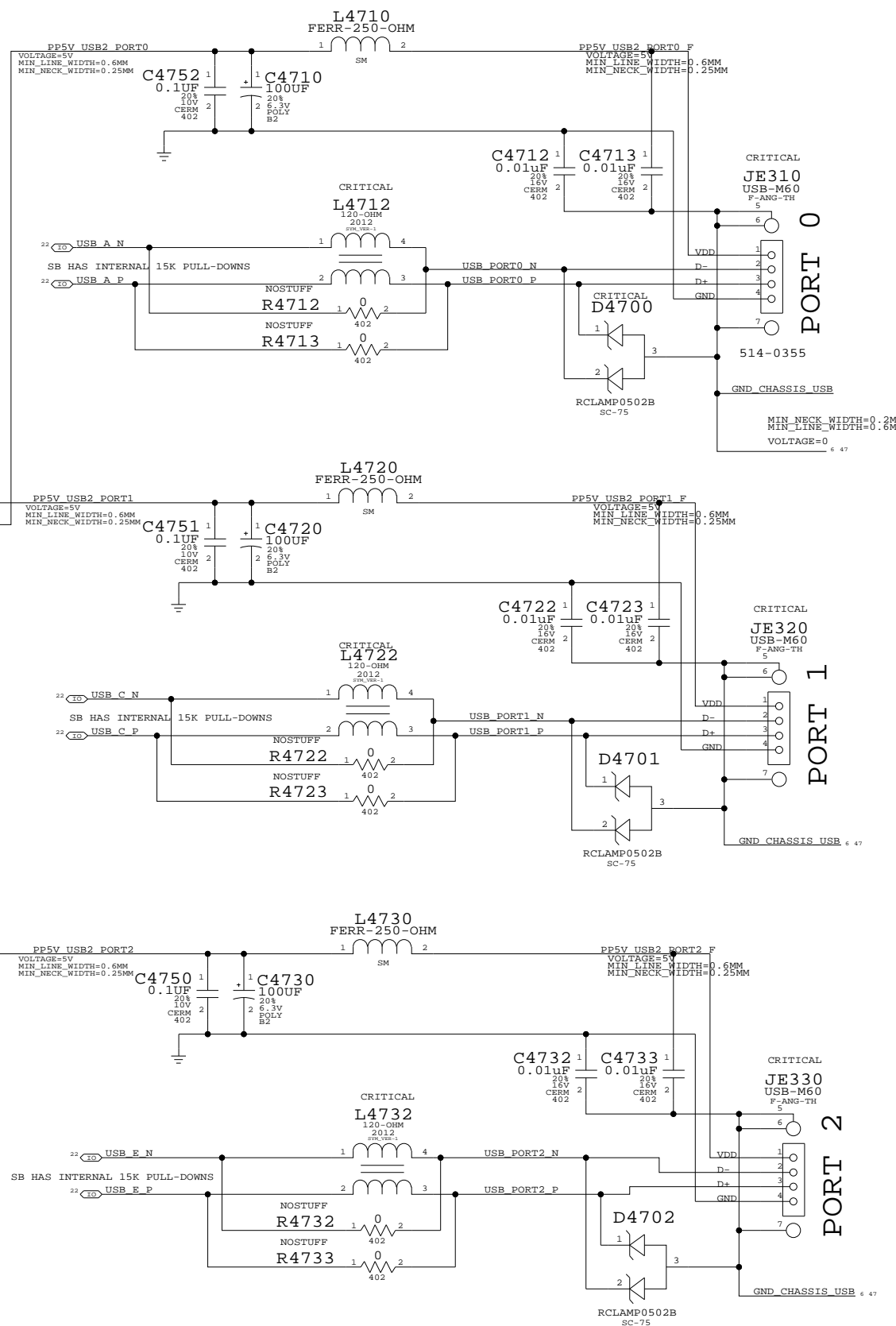
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

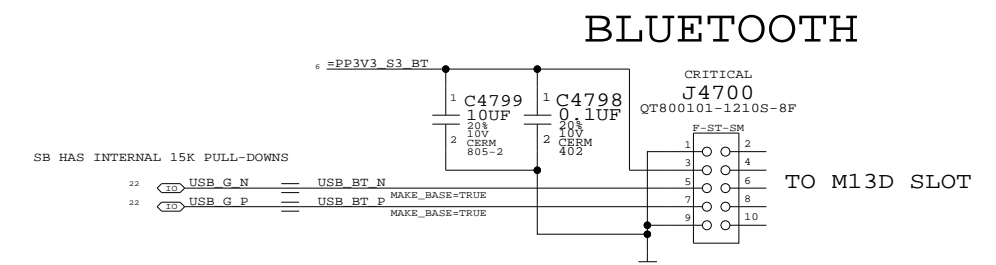
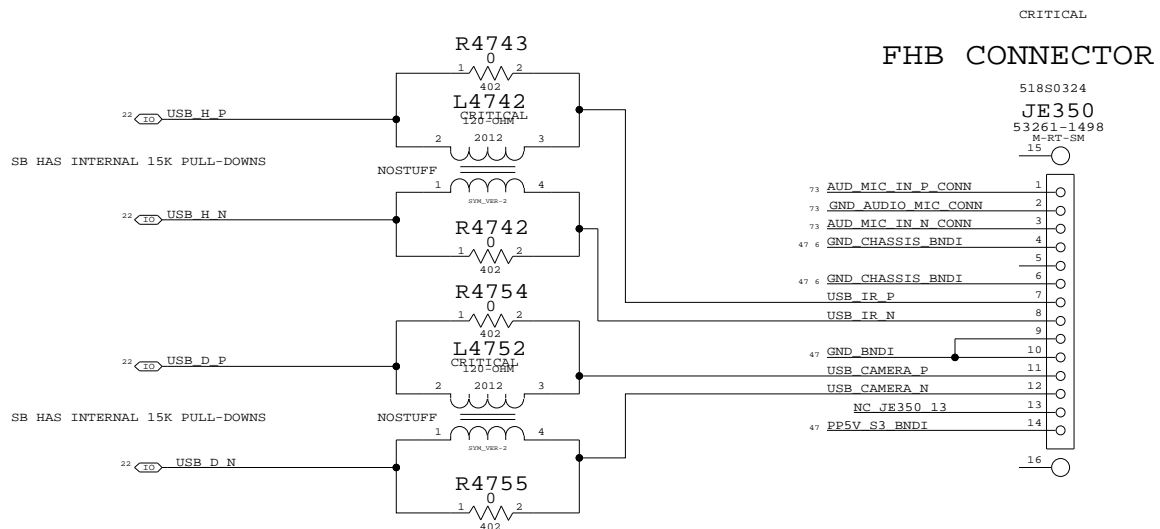
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	13
SCALE	SHT	OF	110
NONE	46		

External USB Ports



LAYOUT NOTE:
PLACE C4743, C4797 & L4740 NEAR JE350 PIN 14 IN THE ORDER LISTED, AND NOT ON BOTH SIDES OF THE PIN.
PLACE C4742 CLOSED TO JE350.



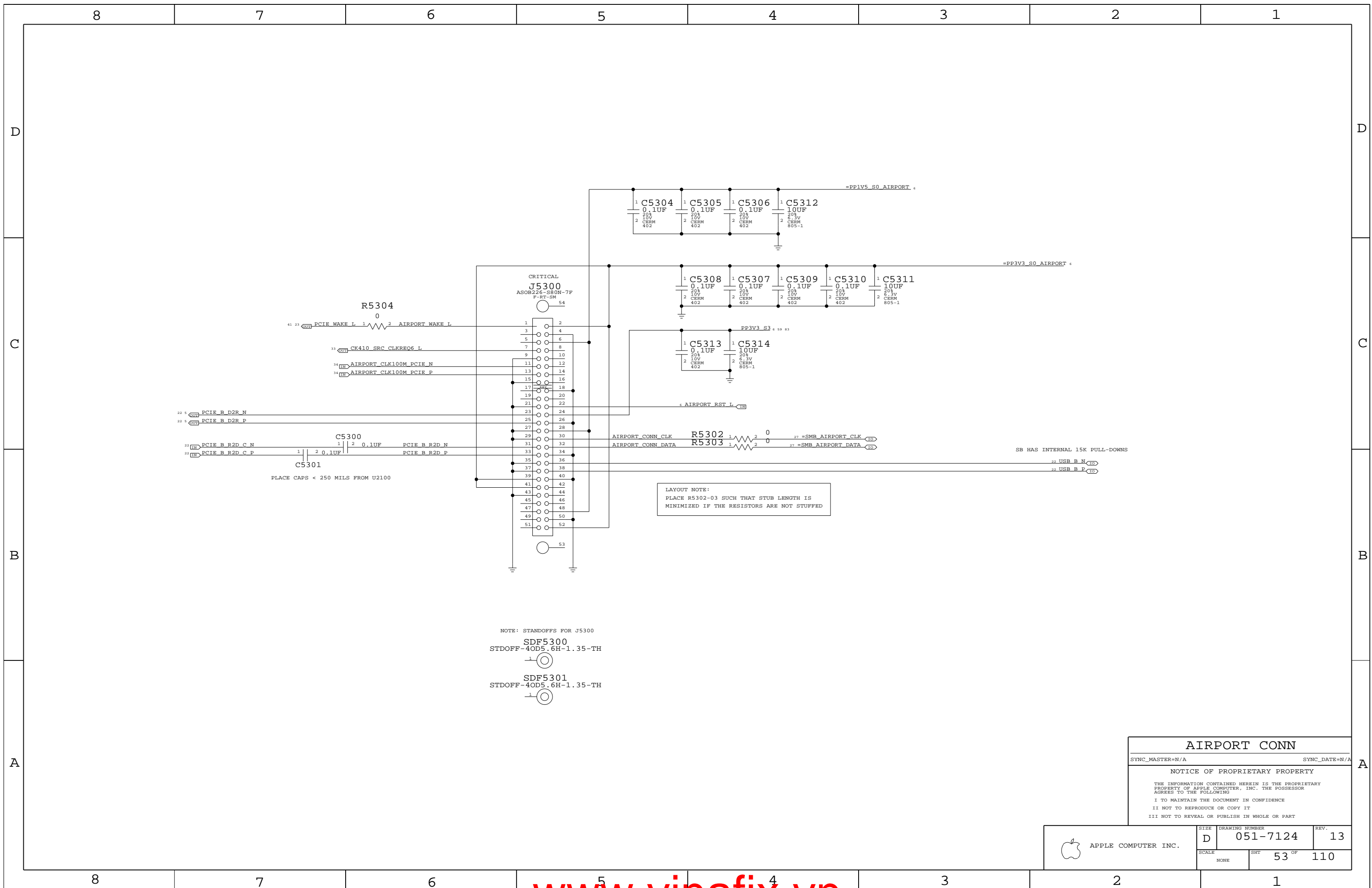
NOTE: STANDOFFS FOR J4700
SDF4700
STDOFF-40D4.5H-1.35-TH
SDF4701
STDOFF-40D4.5H-1.35-TH

USB Device Interfaces

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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0355	3	USB RECEPTACLE, 4P, RIBLESS	JE310, JE320, JE330	CRITICAL	20_INCH_LCD

APPLE COMPUTER INC.	SCALE	DRAWING NUMBER		REV.
	NONE	D	051-7124	13
		SHT	OF	
		47	110	



NOTE: STANDOFFS FOR J5300

SDF5300
STDOFF-40D5.6H-1.35-TH

SDF5301
STDOFF-40D5.6H-1.35-TH

LAYOUT NOTE:
PLACE R5302-03 SUCH THAT STUB LENGTH IS
MINIMIZED IF THE RESISTORS ARE NOT STUFFED

SB HAS INTERNAL 15K PULL-DOWNS

AIRPORT CONN

SYNC_MASTER=N/A SYNC_DATE=N/A

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7124	REV. 13
	SCALE NONE	SHEET 53 OF 110	

8

7

6

5

4

3

2

1

D

D

C

C

B

B

A

A

22	PCIE C R2D C N	==	TP PCIE C R2D C N
			MAKE_BASE=TRUE
22	PCIE C R2D C P	==	TP PCIE C R2D C P
			MAKE_BASE=TRUE
22	PCIE C D2R N	==	TP PCIE C D2R N
			MAKE_BASE=TRUE
22	PCIE C D2R P	==	TP PCIE C D2R P
			MAKE_BASE=TRUE
22	PCIE D R2D C N	==	TP PCIE D R2D C N
			MAKE_BASE=TRUE
22	PCIE D R2D C P	==	TP PCIE D R2D C P
			MAKE_BASE=TRUE
22	PCIE D D2R N	==	TP PCIE D D2R N
			MAKE_BASE=TRUE
22	PCIE D D2R P	==	TP PCIE D D2R P
			MAKE_BASE=TRUE
22	PCIE E R2D C N	==	TP PCIE E R2D C N
			MAKE_BASE=TRUE
22	PCIE E R2D C P	==	TP PCIE E R2D C P
			MAKE_BASE=TRUE
22	PCIE E D2R N	==	TP PCIE E D2R N
			MAKE_BASE=TRUE
22	PCIE E D2R P	==	TP PCIE E D2R P
			MAKE_BASE=TRUE
22	PCIE F R2D C N	==	TP PCIE F R2D C N
			MAKE_BASE=TRUE
22	PCIE F R2D C P	==	TP PCIE F R2D C P
			MAKE_BASE=TRUE
22	PCIE F D2R N	==	TP PCIE F D2R N
			MAKE_BASE=TRUE
22	PCIE F D2R P	==	TP PCIE F D2R P
			MAKE_BASE=TRUE

PCIE UNUSED PORTS

SYNC_MASTER=N/A SYNC_DATE=N/A

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	13
SCALE	SHT	54 OF 110	
NONE			

8

7

6

5

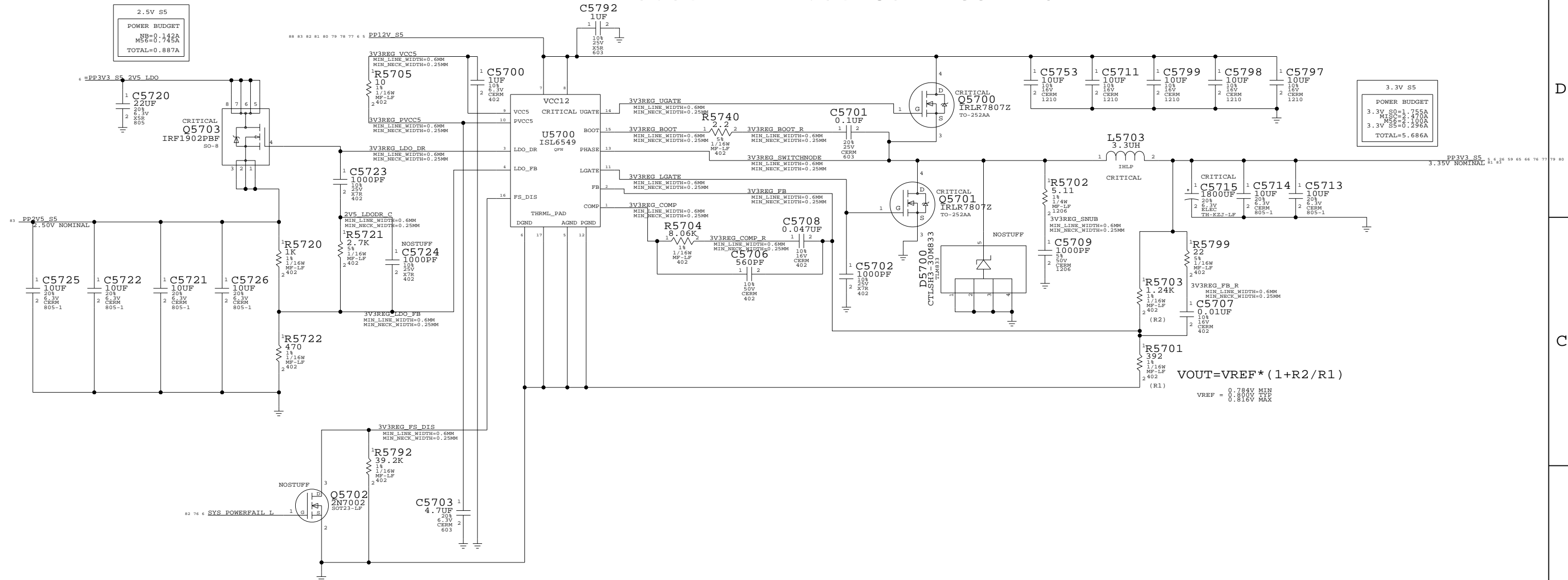
4

3

2

1

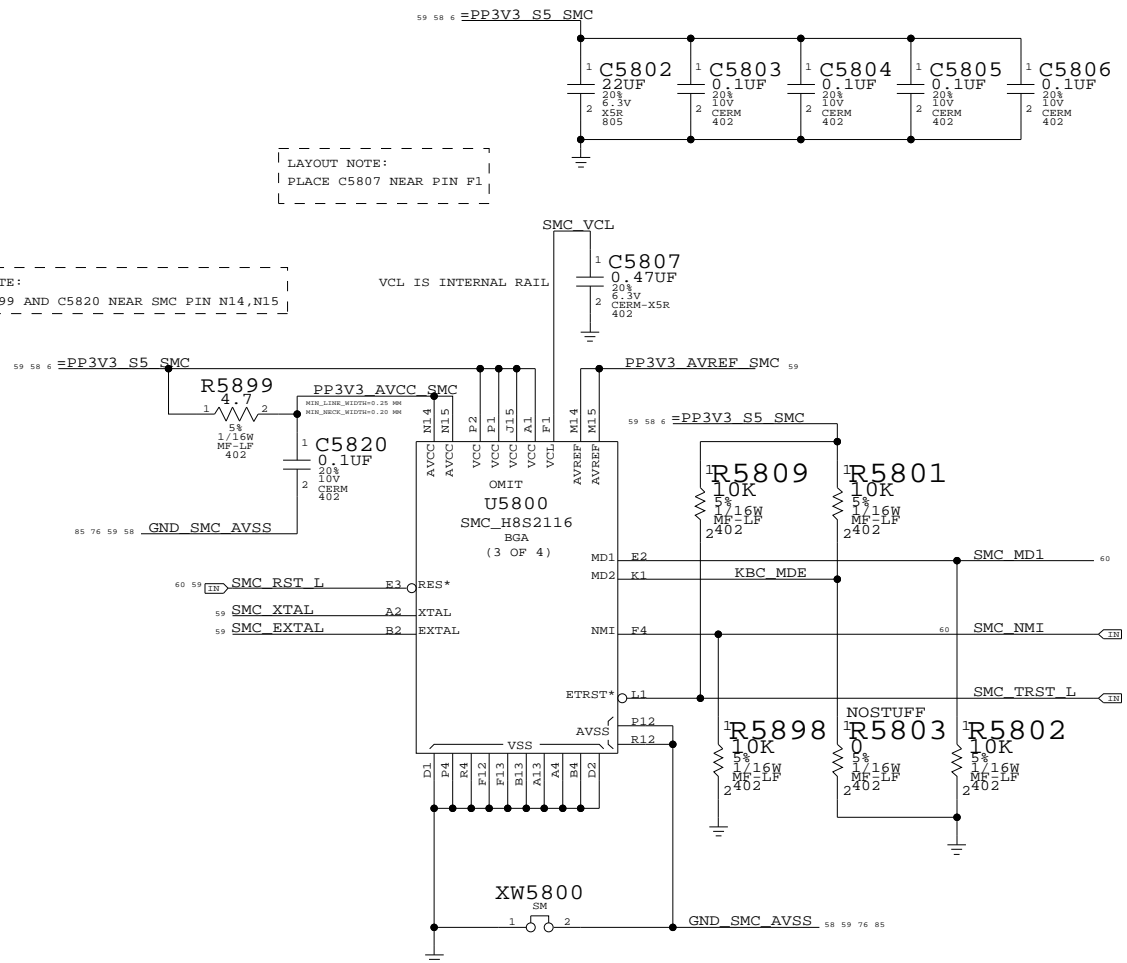
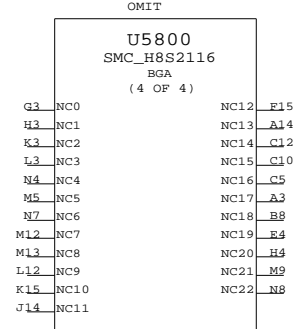
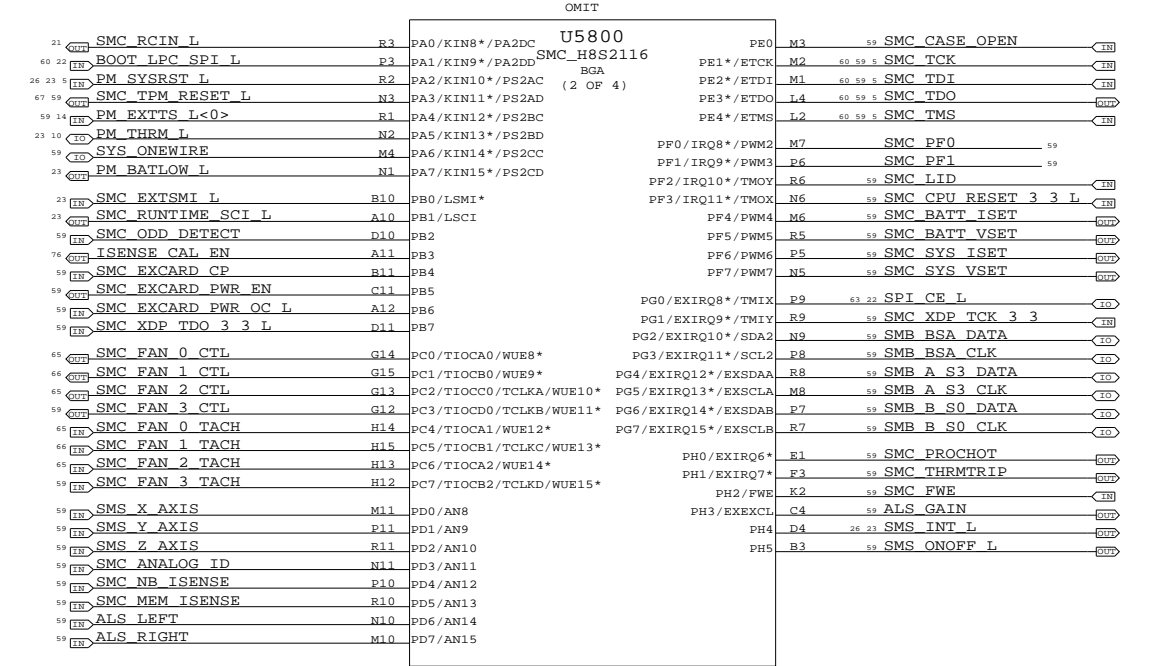
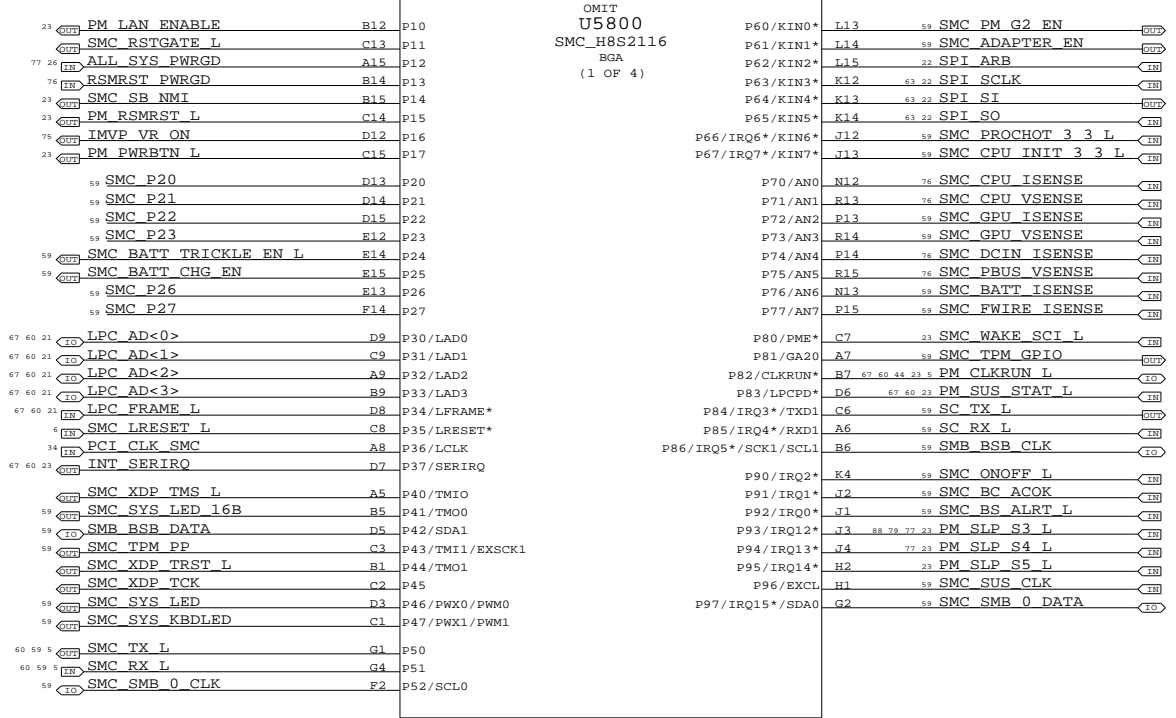
3.3V AND 2.5V S5 REGULATOR



$$V_{OUT} = V_{REF} * (1 + R2/R1)$$

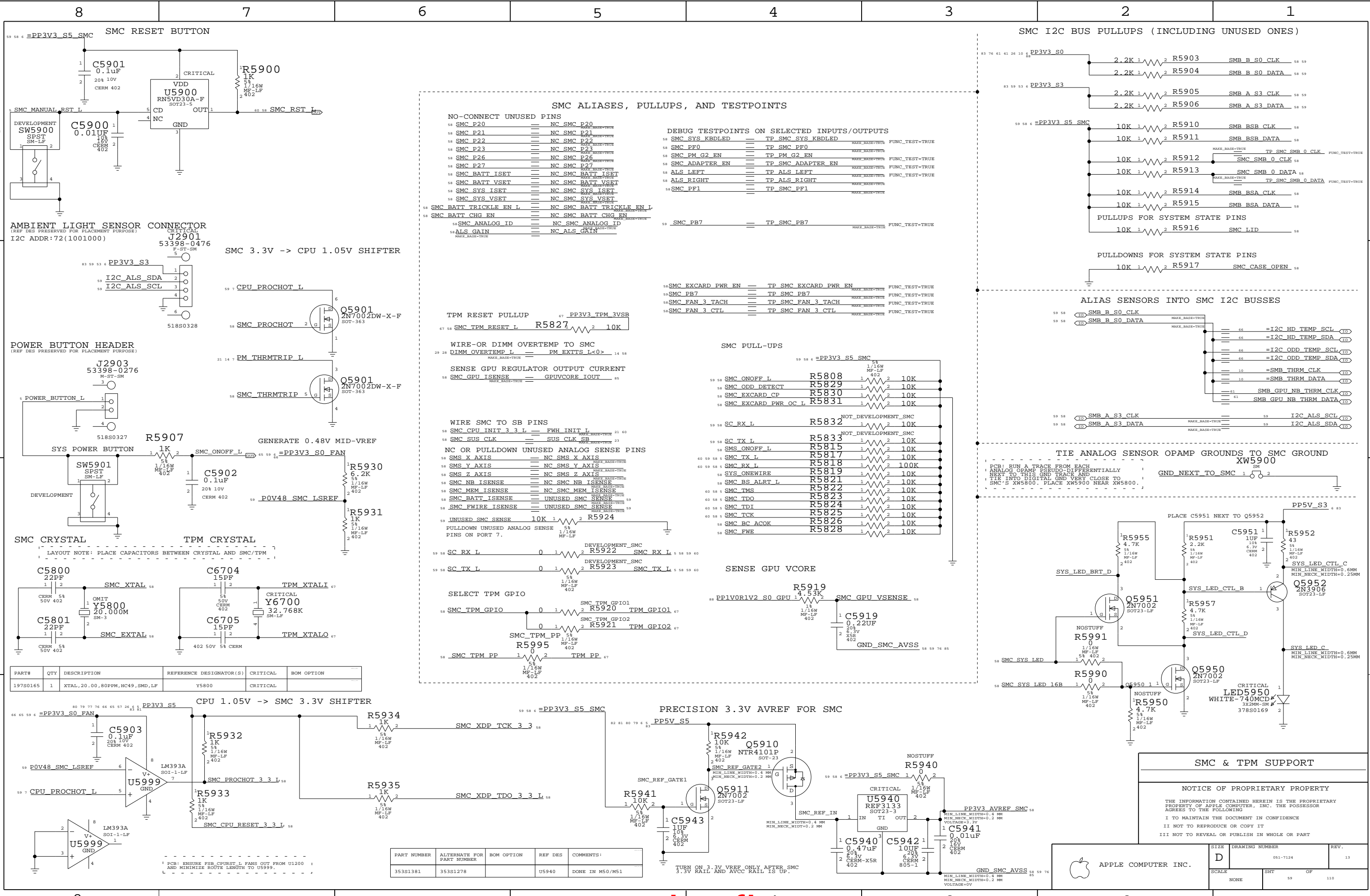
VREF = 0.784V MIN
0.800V TYP
0.816V MAX

UNUSED PINS HAVE THE FORMAT SMC_XXX WHERE XXX IS THE PORT NUMBER. THEY ARE SET BY SOFTWARE TO BE DRIVEN OUTPUTS ALWAYS SO THEY CAN BE LEFT NO-CONNECTED.

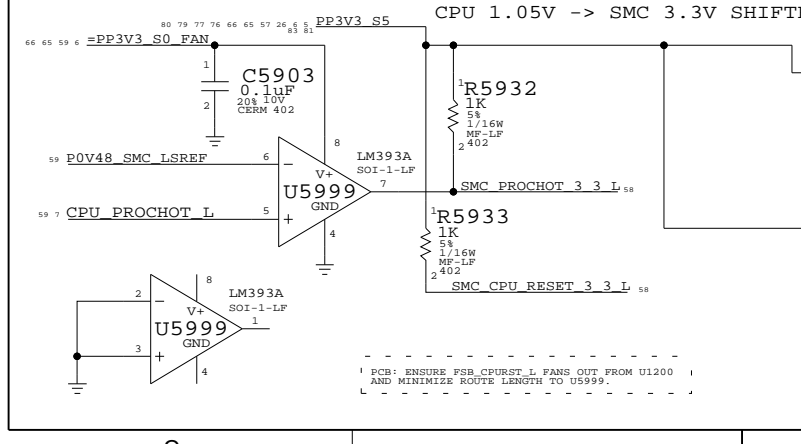


SMC
SYNC_MASTER=N/A SYNC_DATE=N/A
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	13
SCALE	SHT	58 OF	110
NONE			



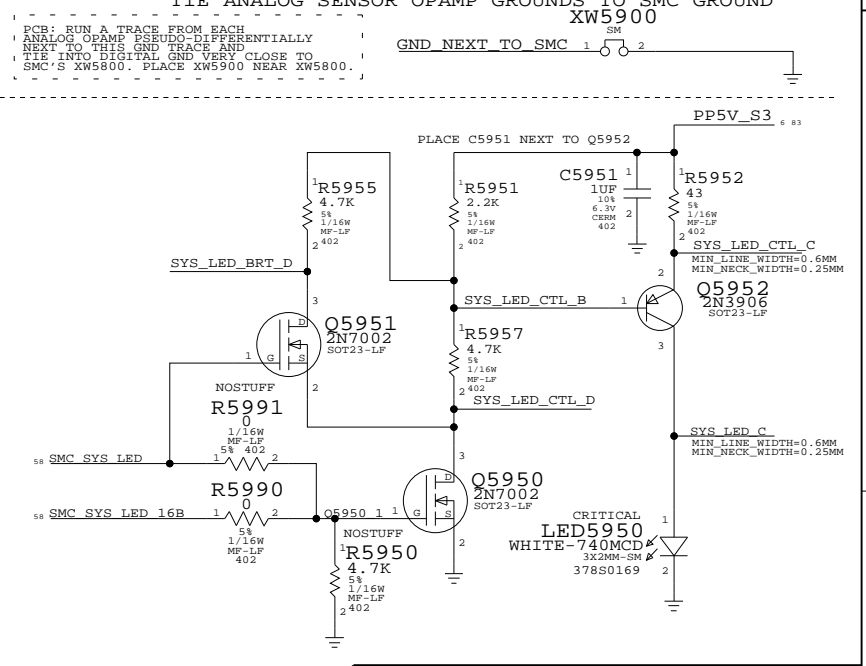
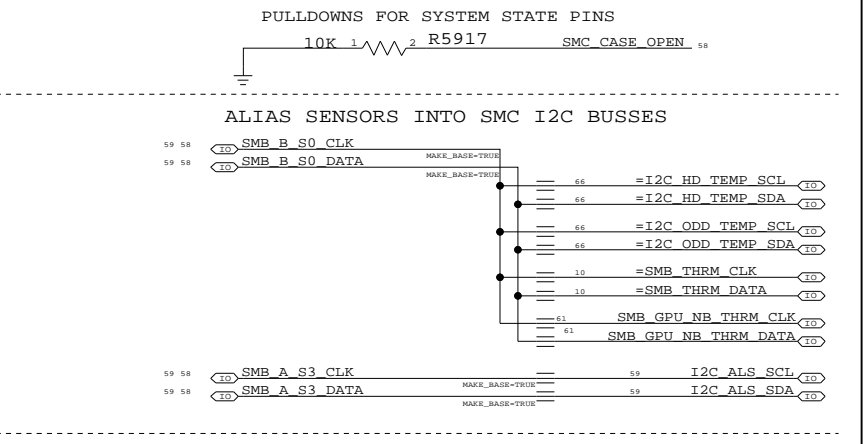
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
19750165	1	XTAL, 20.00, 80PPM, HC49, SMD, LF	Y5800	CRITICAL	



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
353S1381	353S1278		U5940	DONE IN M50/M51

SMC ALIASES, PULLUPS, AND TESTPOINTS

SMC PIN	Alias	Value	Notes
SMC P20	NC SMC P20		
SMC P21	NC SMC P21		
SMC P22	NC SMC P22		
SMC P23	NC SMC P23		
SMC P26	NC SMC P26		
SMC P27	NC SMC P27		
SMC BATT ISET	NC SMC BATT ISET		
SMC BATT VSET	NC SMC BATT VSET		
SMC SYS ISET	NC SMC SYS ISET		
SMC SYS VSET	NC SMC SYS VSET		
SMC BATT TRICKLE EN L	NC SMC BATT TRICKLE EN L		
SMC BATT CHG EN	NC SMC BATT CHG EN		
SMC ANALOG ID	NC SMC ANALOG ID		
ALS GAIN	NC ALS GAIN		



SMC & TPM SUPPORT

NOTICE OF PROPRIETARY PROPERTY

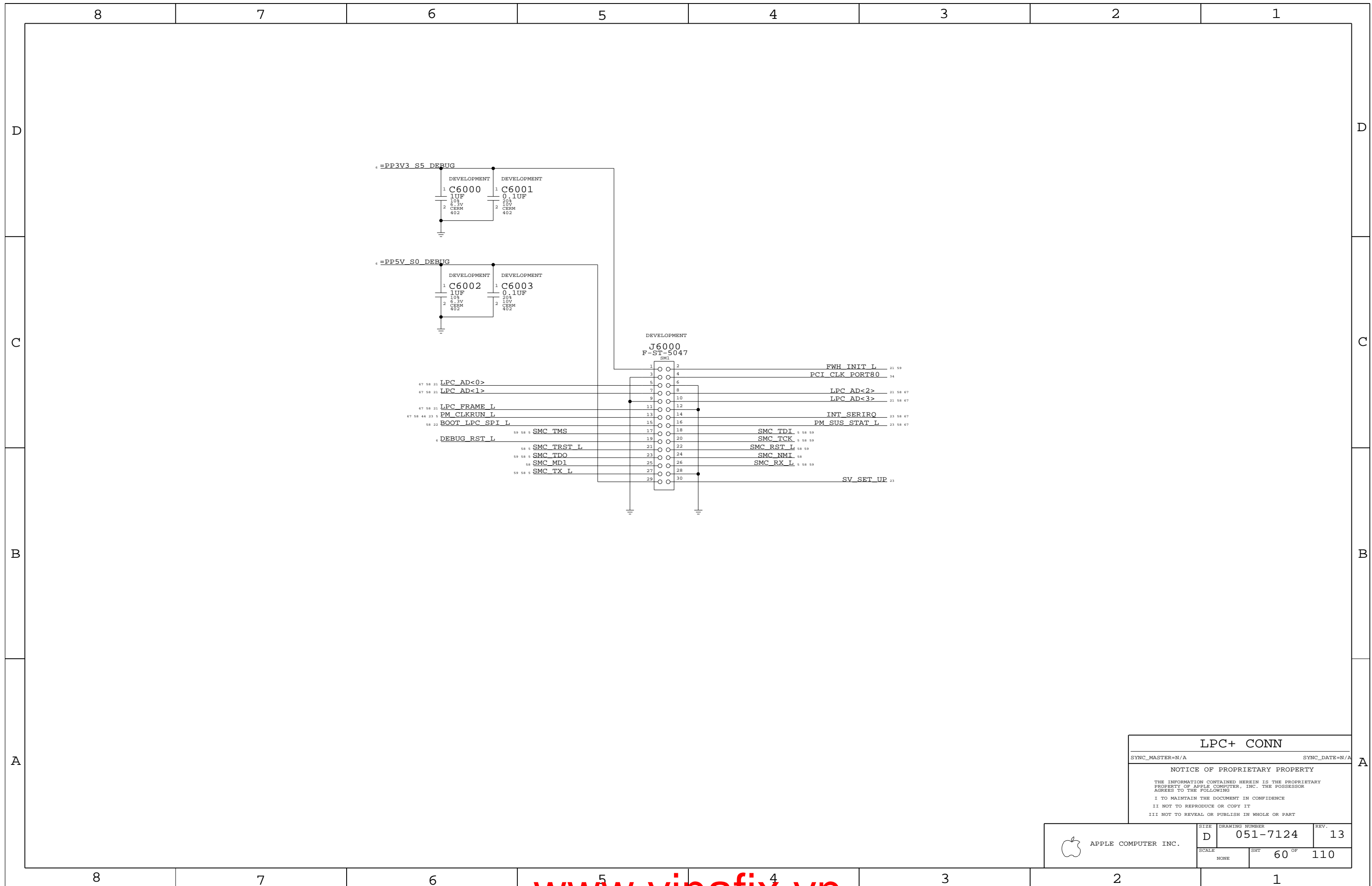
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D	051-7124	13

SCALE: NONE SHEET: 59 OF 110

APPLE COMPUTER INC.



LPC+ CONN

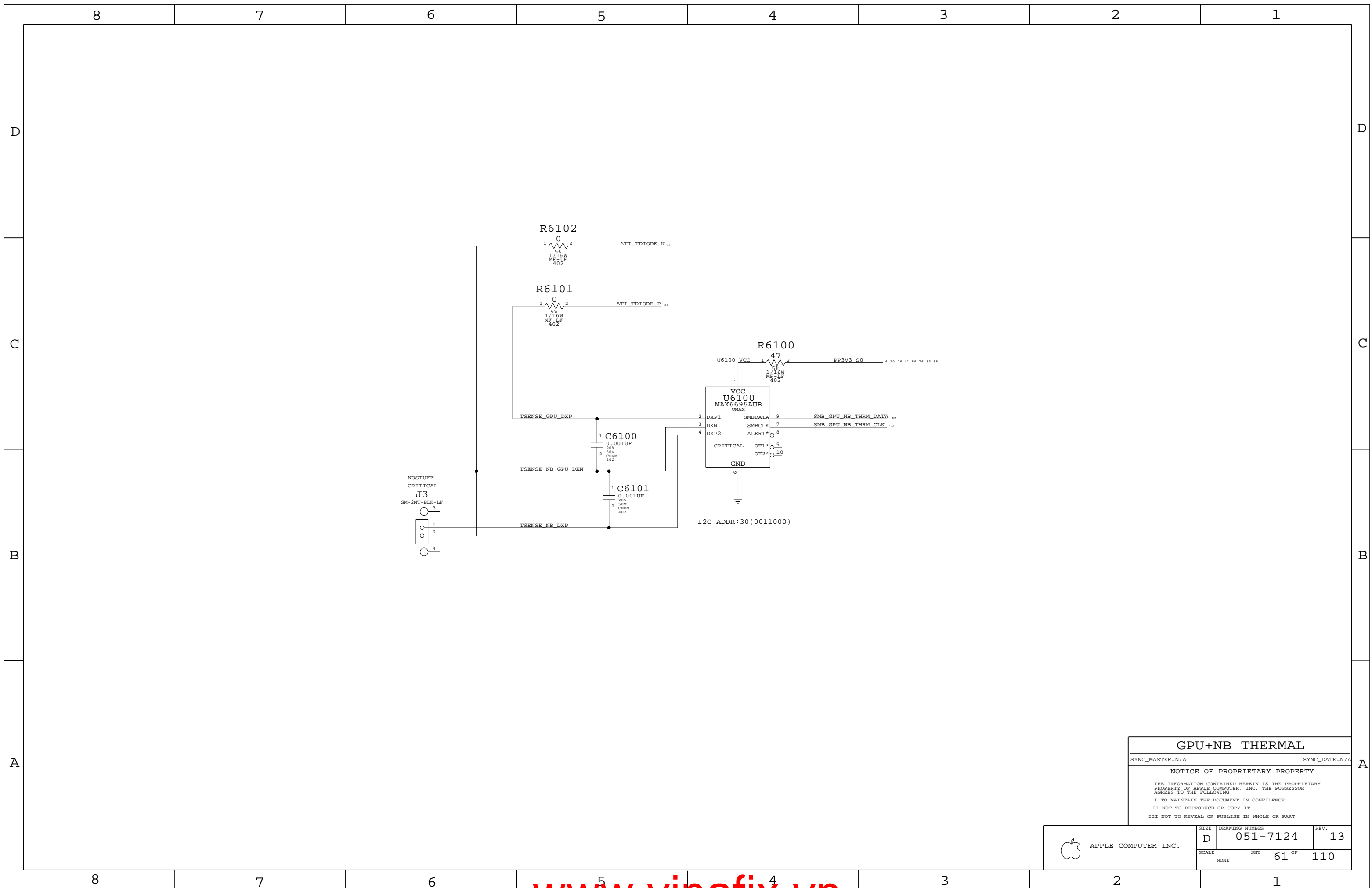
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	SCALE NONE	SHT 60 OF	110



GPU+NB THERMAL

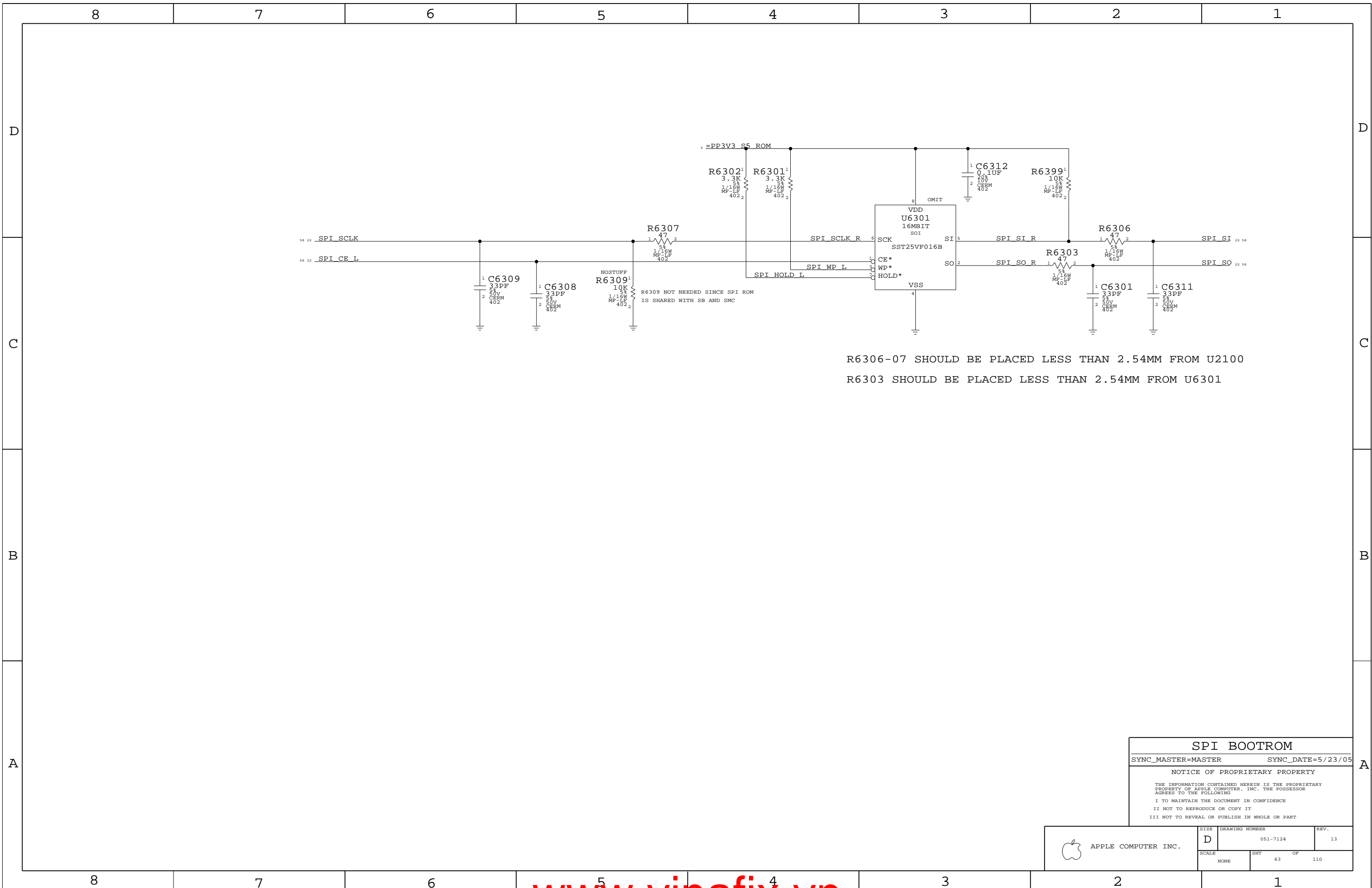
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	SCALE NONE	SHT 61 OF	110



R6306-07 SHOULD BE PLACED LESS THAN 2.54MM FROM U2100
 R6303 SHOULD BE PLACED LESS THAN 2.54MM FROM U6301

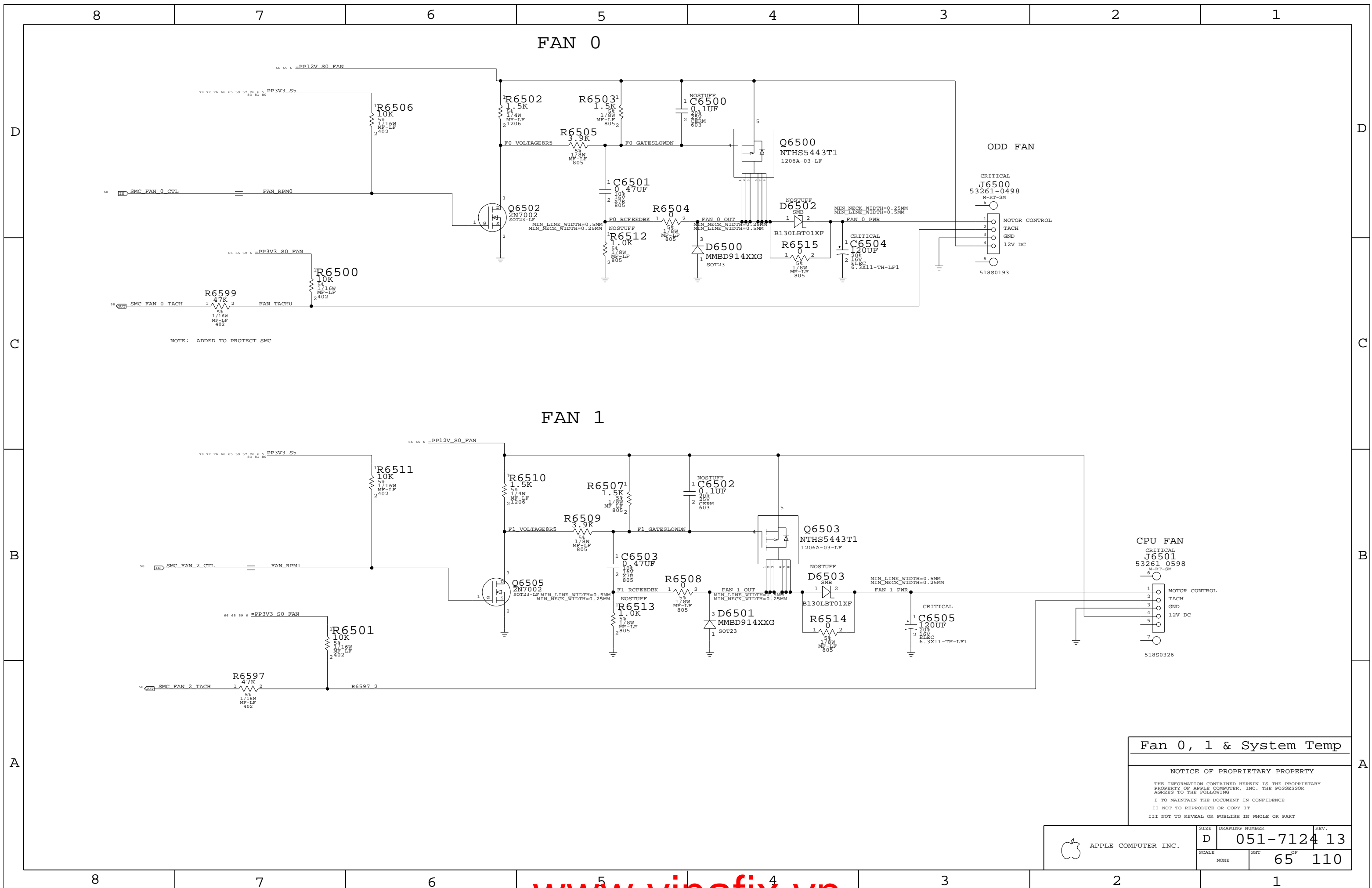
SPI BOOTROM
 SYNC_MASTER=MASTER SYNC_DATE=5/23/05

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7124	REV. 13
	SCALE NONE	SHEET 63	OF 110

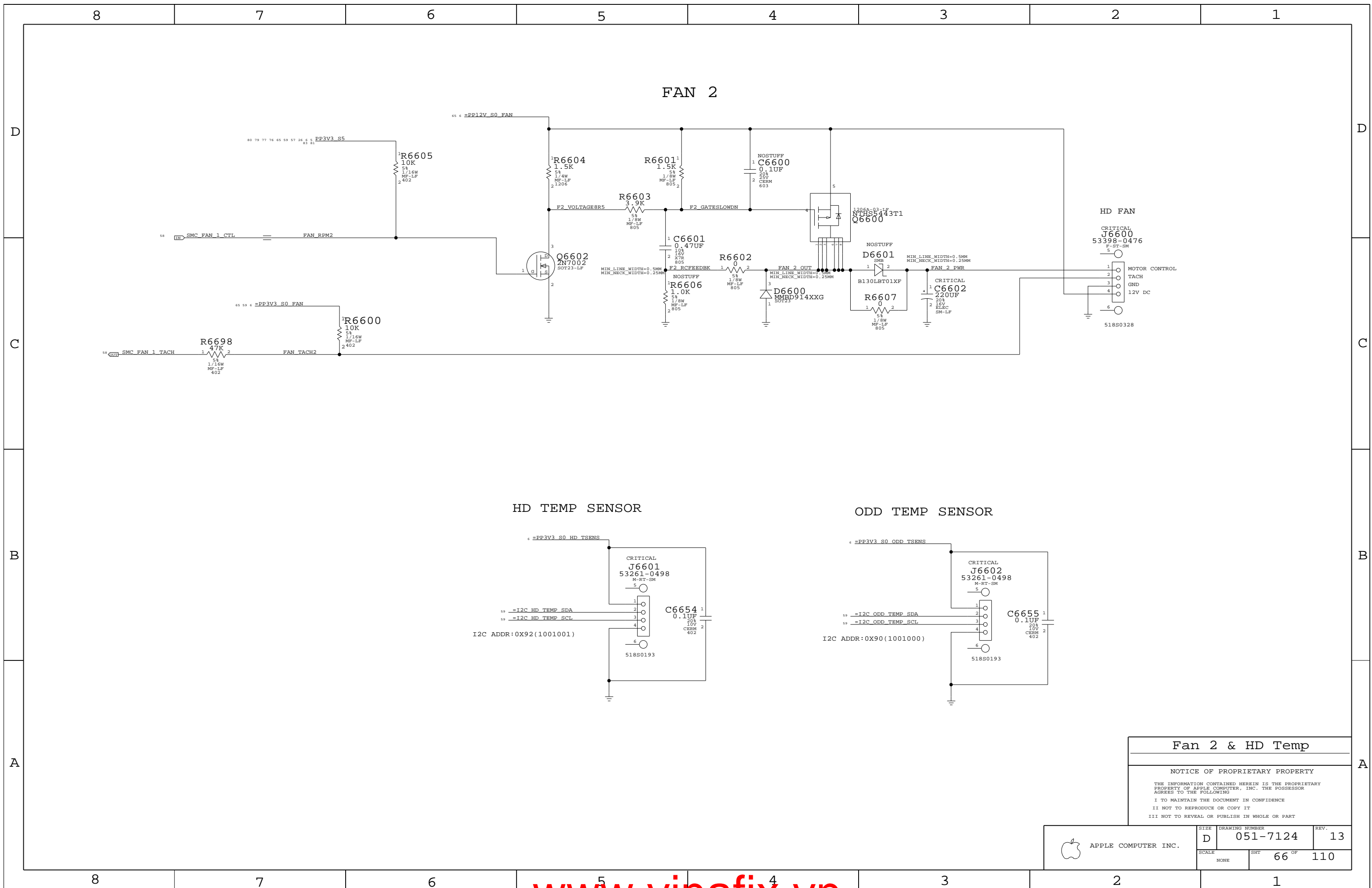


NOTE: ADDED TO PROTECT SMC

Fan 0, 1 & System Temp

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	13
SCALE	NONE	SHT	OF
		65	110



FAN 2

HD TEMP SENSOR

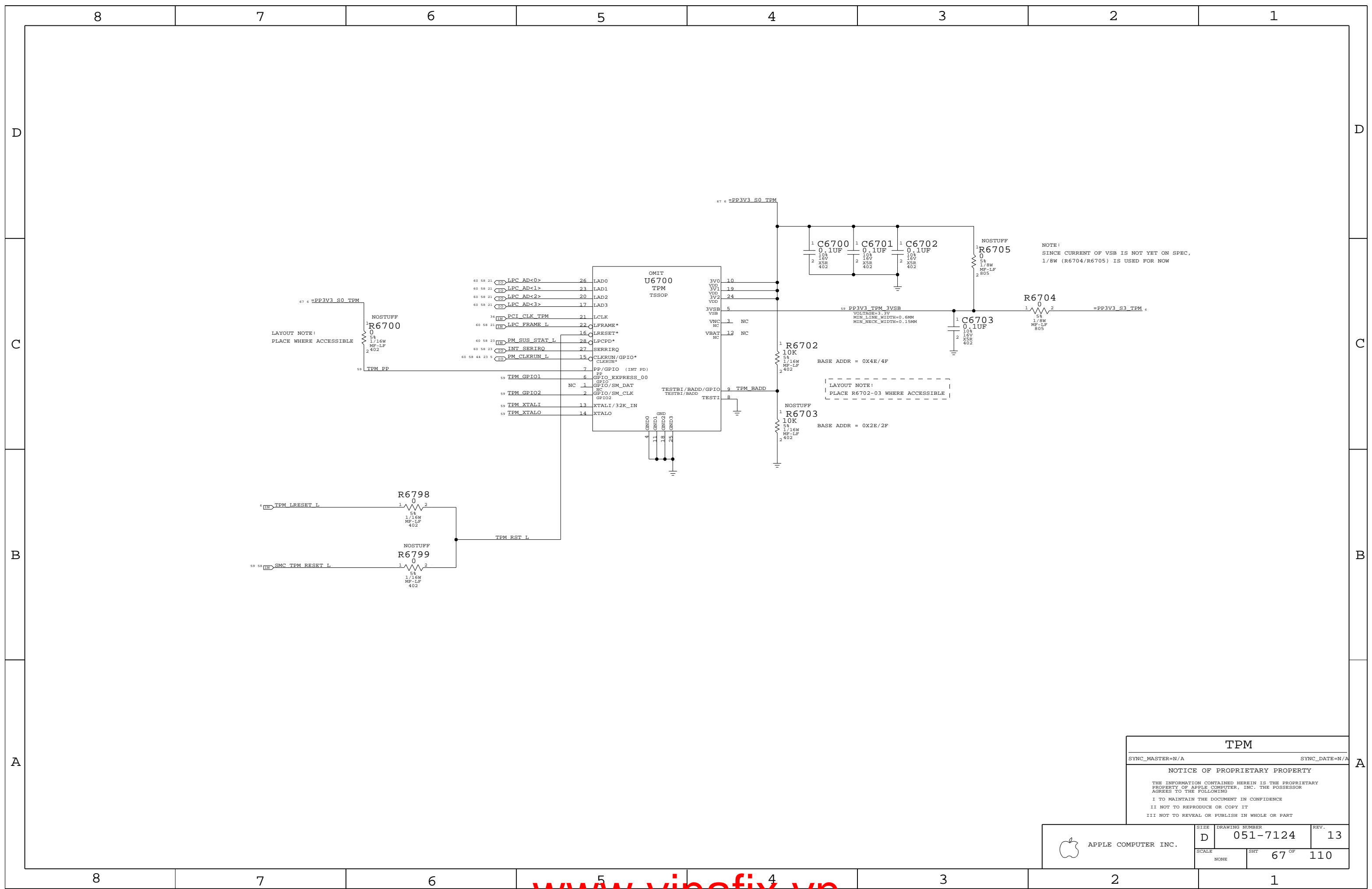
ODD TEMP SENSOR

Fan 2 & HD Temp

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	13
SCALE	SHT	OF	
NONE	66	110	



LAYOUT NOTE:
PLACE WHERE ACCESSIBLE

LAYOUT NOTE:
PLACE R6702-03 WHERE ACCESSIBLE

NOTE:
SINCE CURRENT OF VSB IS NOT YET ON SPEC,
1/8W (R6704/R6705) IS USED FOR NOW

TPM

SYNC_MASTER=N/A SYNC_DATE=N/A

NOTICE OF PROPRIETARY PROPERTY

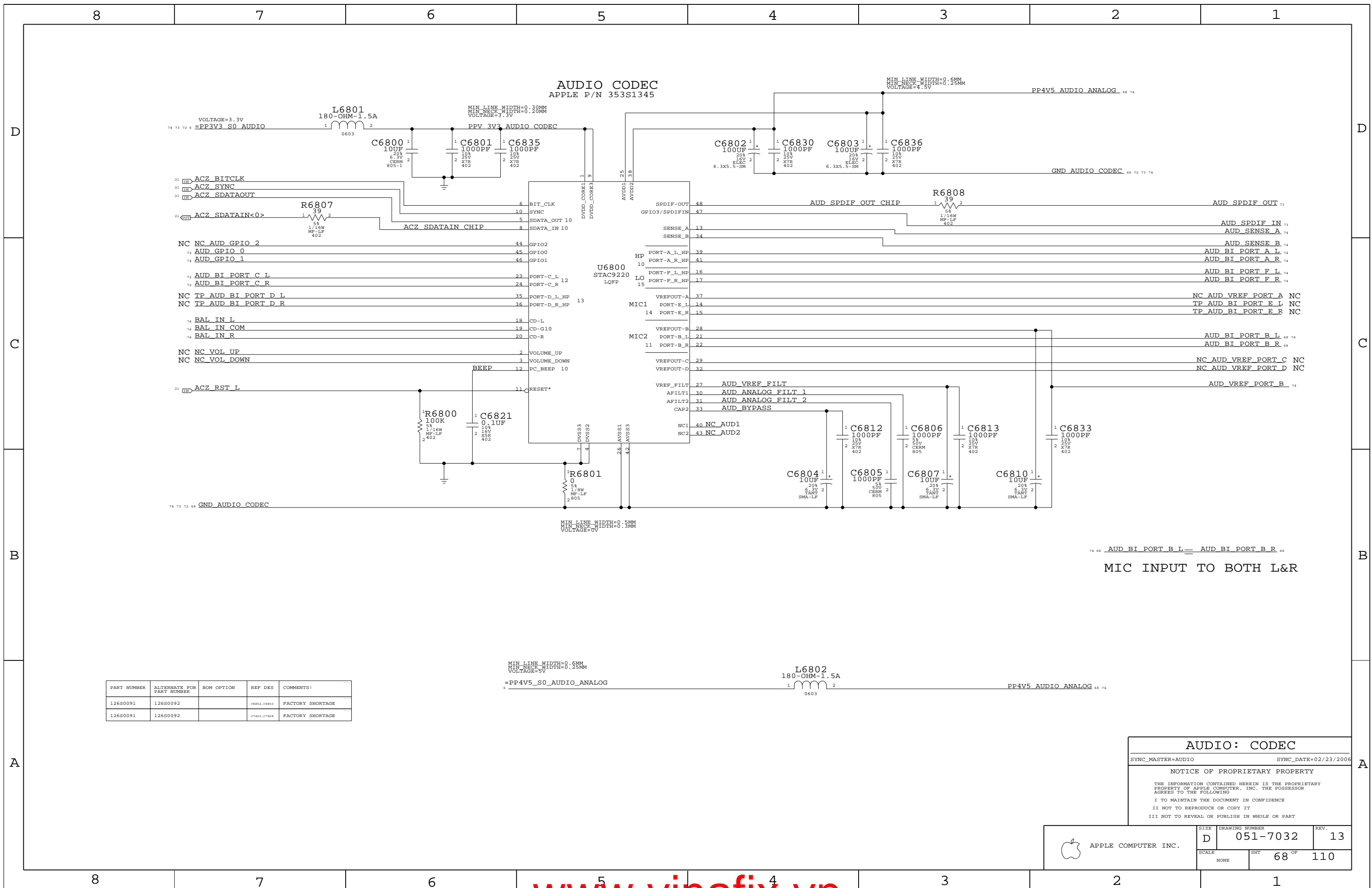
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	13
SCALE	SHT	67 OF 110	
NONE			



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
126S0091	126S0092		C802,C803	FACTORY SHORTAGE
126S0091	126S0092		C7403,C7404	FACTORY SHORTAGE

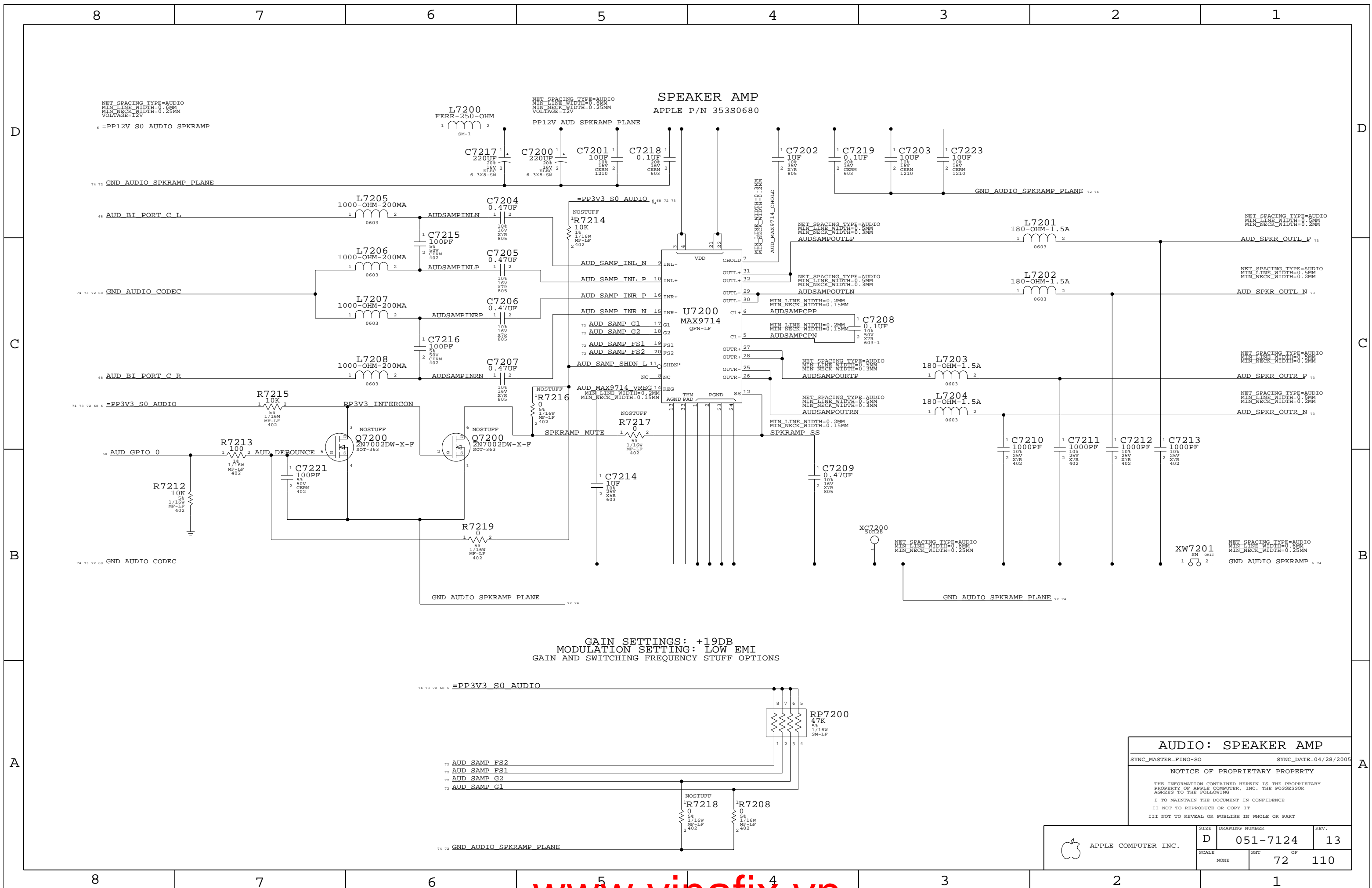
MIN LINE WIDTH=0.6MM
MIN NECK WIDTH=0.3MM
VOLTAGE=0V
=PP4V5_S0_AUDIO_ANALOG

L6802
180-OHM-1.5A
0603

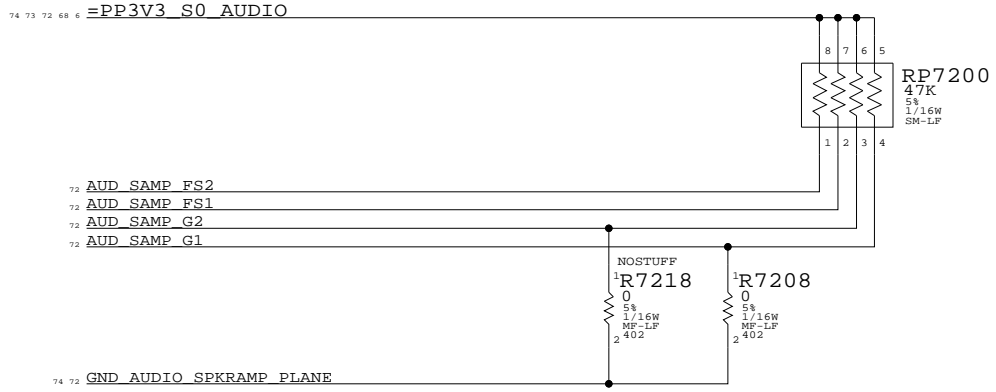
74 68 AUD BI PORT B L = AUD BI PORT B R 68
MIC INPUT TO BOTH L&R

AUDIO: CODEC				
SYNC_MASTER=AUDIO		SYNC_DATE=02/23/2006		
NOTICE OF PROPRIETARY PROPERTY				
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	13
SCALE	SHT	68 OF 110	
NONE			

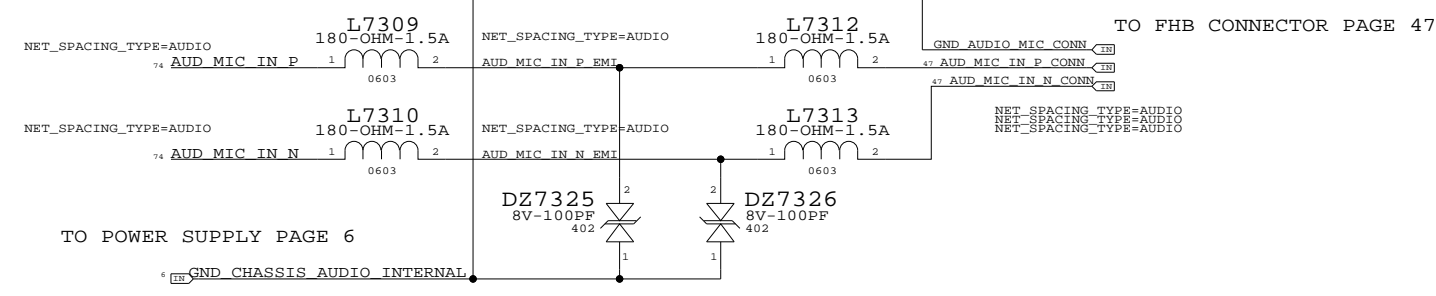
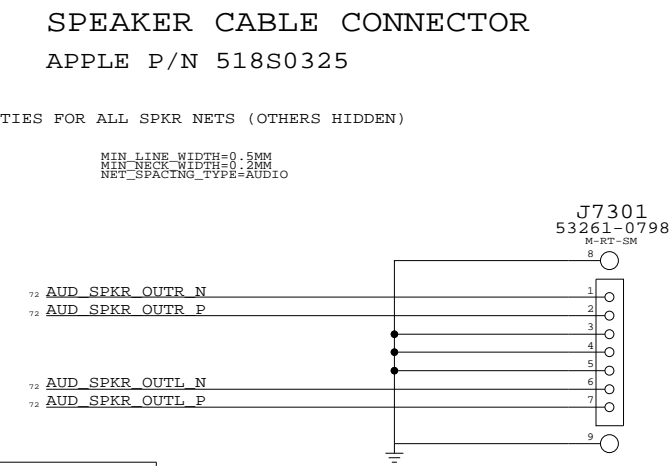
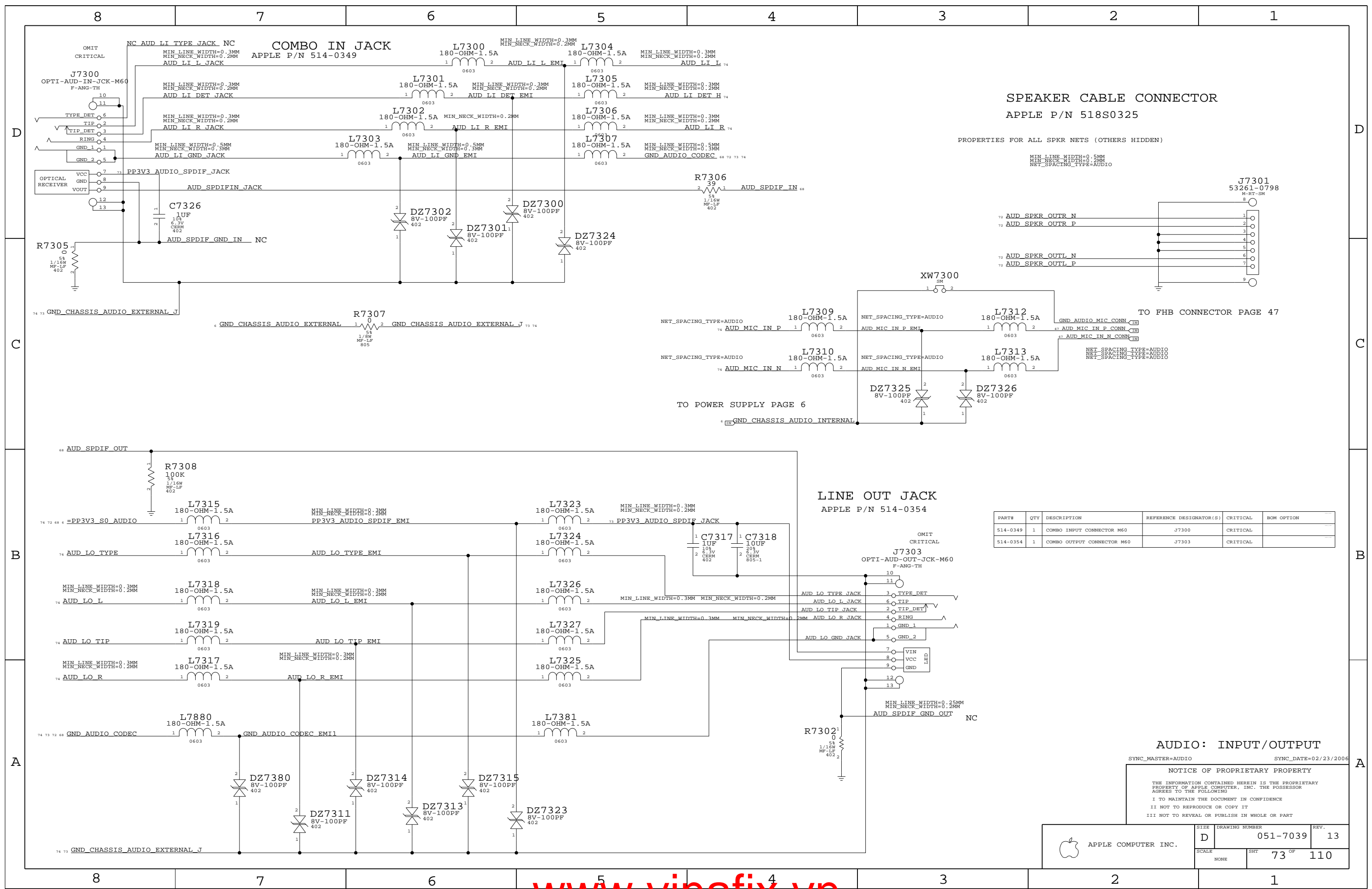


GAIN SETTINGS: +19DB
 MODULATION SETTING: LOW EMI
 GAIN AND SWITCHING FREQUENCY STUFF OPTIONS



AUDIO: SPEAKER AMP
 SYNC_MASTER=FINO-SO SYNC_DATE=04/28/2005
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	13
SCALE	NONE	SHT OF	72 OF 110



LINE OUT JACK
APPLE P/N 514-0354

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0349	1	COMBO INPUT CONNECTOR M60	J7300	CRITICAL	
514-0354	1	COMBO OUTPUT CONNECTOR M60	J7303	CRITICAL	

AUDIO: INPUT/OUTPUT

SYNC_MASTER=AUDIO SYNC_DATE=02/23/2006

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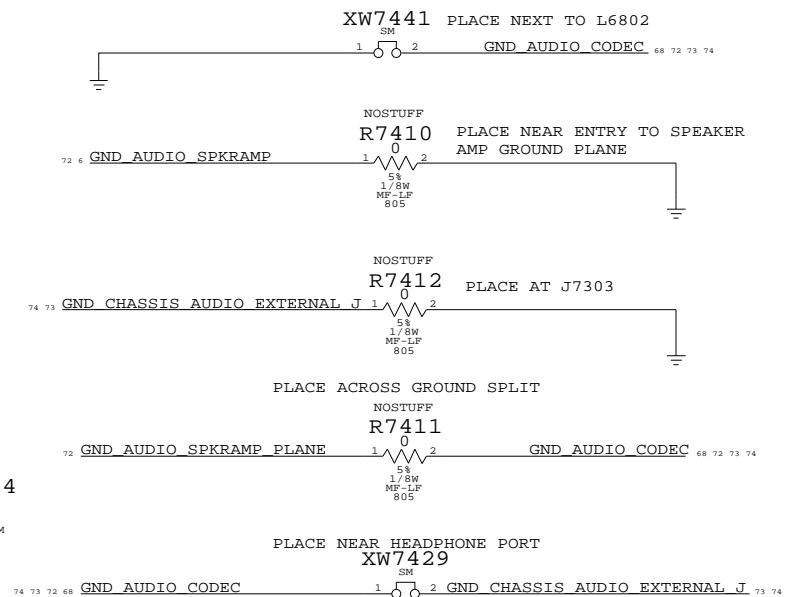
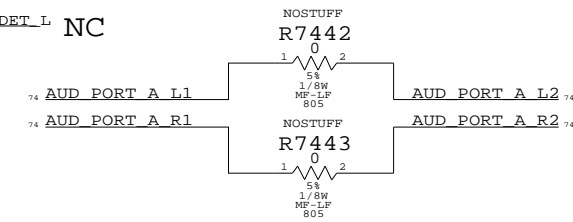
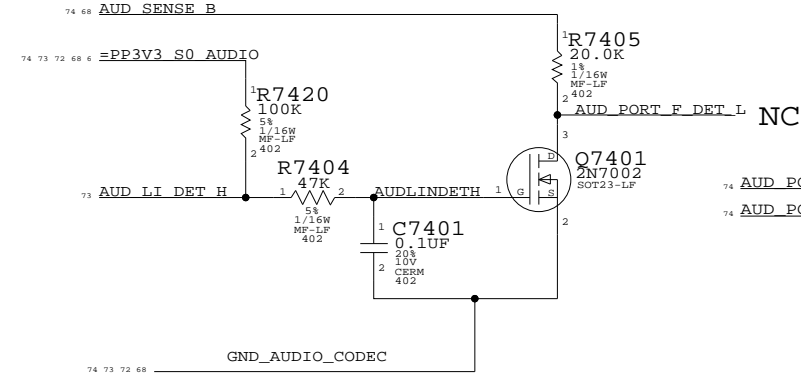
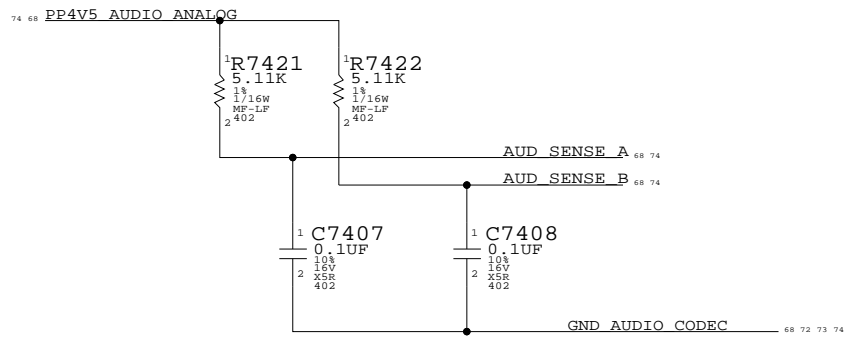
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7039	13
SCALE	SHT	73 OF	110
NONE			

PORT F (LI) PLUG DETECT

AUDIO GROUND RETURNS

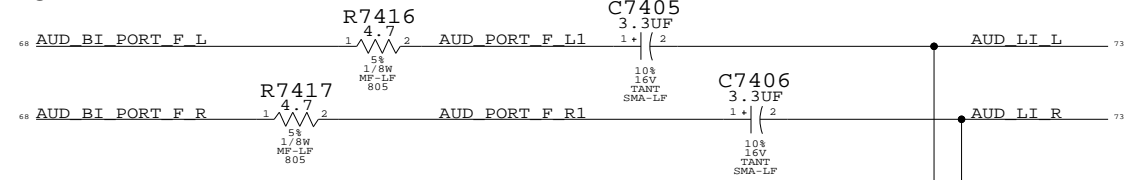
JACK SENSE PULL UPS (PLACE NEXT TO CODEC)



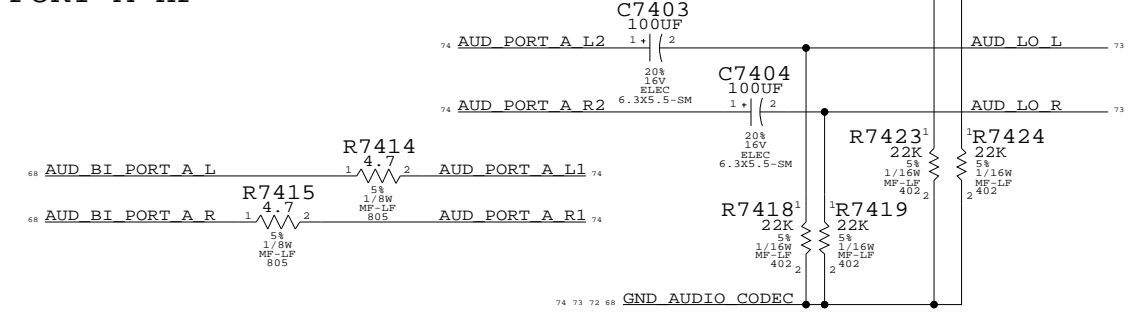
USED PORTS
 PORT A HP
 PORT B MIC IN VREF =80%
 PORT C BI SPEAKERS
 PORT F LI

UNUSED PORTS
 PORT E DETECT DELEGATE
 PORT D

PORT F LI



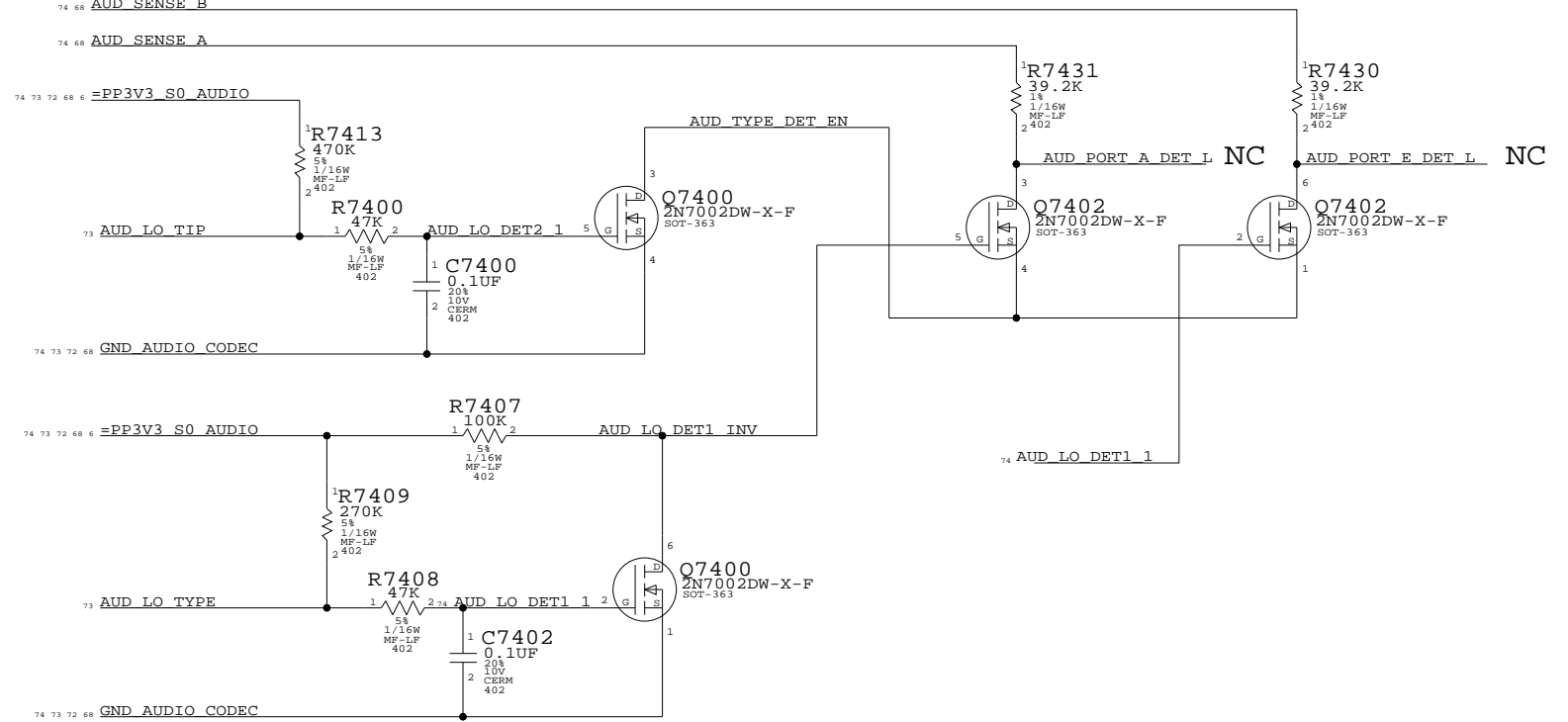
PORT A HP



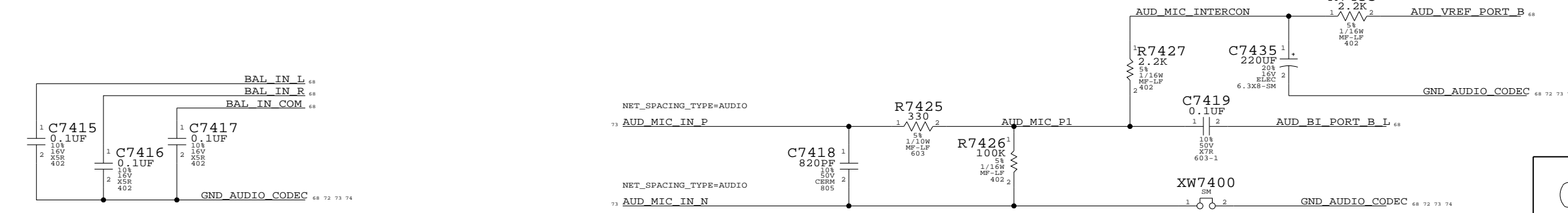
UNUSED PORT TERMINATION



PORT A/H (LO/DIG_OUT) PLUG DETECT (E TELLS H TO COME ON)

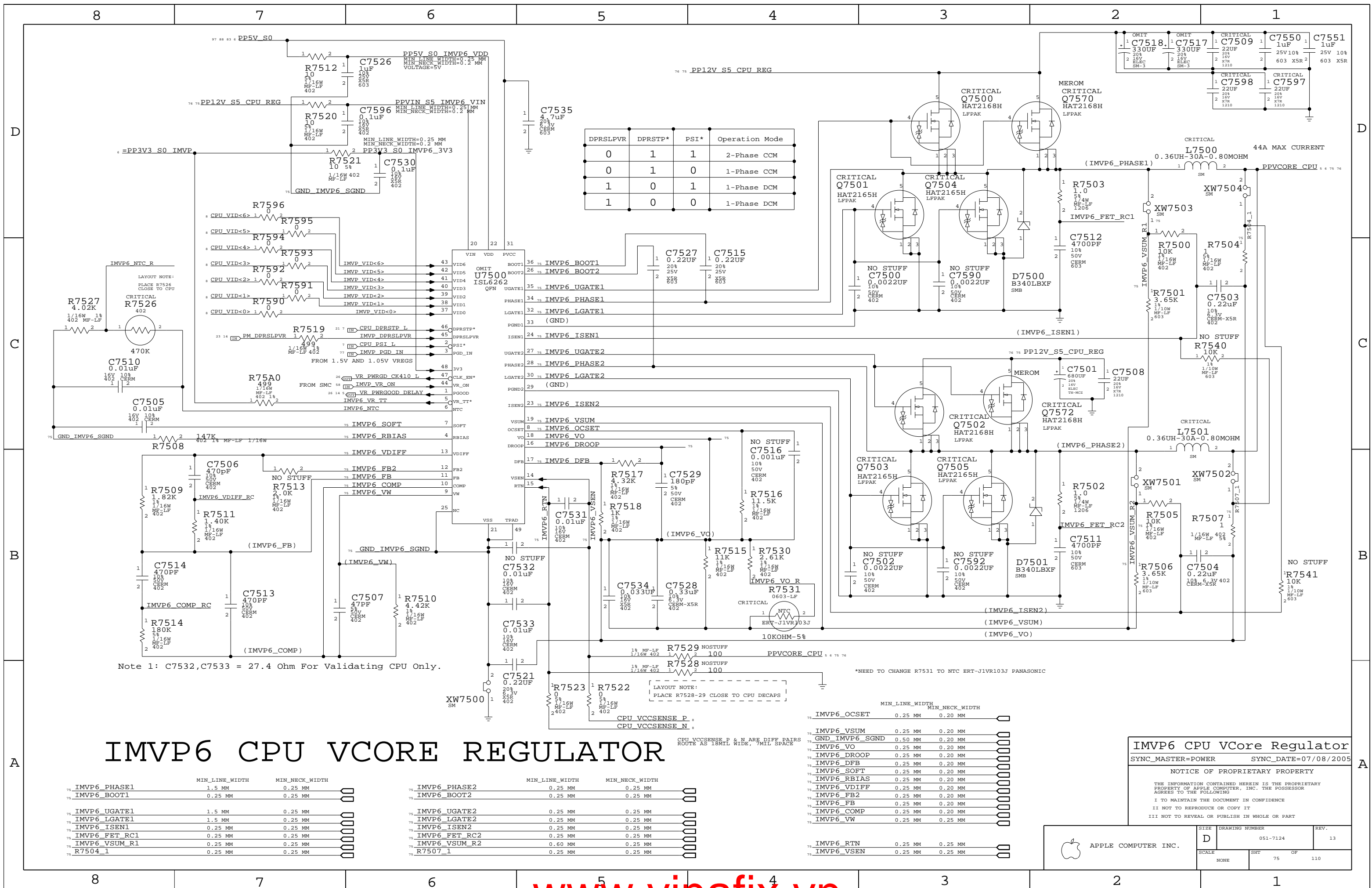


MICROPHONE IMPEDANCE MATCHING CIRCUIT



AUDIO: JACK DETECT
 SYNC_MASTER=AUDIO SYNC_DATE=02/23/2006
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	D	051-7032	13
SCALE	SHT	74 OF	110
NONE			



DPRSLPVR	DPRSTP*	PSI*	Operation Mode
0	1	1	2-Phase CCM
0	1	0	1-Phase CCM
1	0	1	1-Phase DCM
1	0	0	1-Phase DCM

Signal	Value
C7527	0.22uF
C7515	0.22uF
C7516	0.001uF
C7517	4.32K
C7529	180pF
C7531	0.01uF
C7532	0.01uF
C7533	0.01uF
C7534	0.033uF
C7528	0.33uF
C7514	470PF
C7513	470PF
C7507	47PF
C7510	4.42K
C7511	1.40K
C7509	1.82K
C7506	470pF
C7505	0.01uF
C7504	0.22uF
C7503	3.65K
C7502	0.0022uF
C7501	680uF
C7500	4700PF
C7526	1uF
C7525	0.1uF
C7524	0.1uF
C7523	0.22uF
C7522	0.22uF
C7521	0.22uF
C7520	0.1uF
C7519	0.1uF
C7518	330uF
C7517	330uF
C7516	22uF
C7515	22uF
C7514	22uF
C7513	22uF
C7512	4700PF
C7511	4700PF
C7510	4700PF
C7509	22uF
C7508	22uF
C7507	22uF
C7506	22uF
C7505	22uF
C7504	22uF
C7503	22uF
C7502	22uF
C7501	22uF
C7500	22uF

Note 1: C7532,C7533 = 27.4 Ohm For Validating CPU Only.

LAYOUT NOTE:
PLACE R7528-29 CLOSE TO CPU DECAPS

*NEED TO CHANGE R7531 TO NTC ERT-J1VR103J PANASONIC

IMVP6 CPU VCore REGULATOR

Signal	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE1	1.5 MM	0.25 MM
IMVP6_BOOT1	0.25 MM	0.25 MM
IMVP6_UGATE1	1.5 MM	0.25 MM
IMVP6_LGATE1	1.5 MM	0.25 MM
IMVP6_ISEN1	0.25 MM	0.25 MM
IMVP6_FET_RC1	0.25 MM	0.25 MM
IMVP6_VSUM_R1	0.25 MM	0.25 MM
R7504_1	0.25 MM	0.25 MM

Signal	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE2	0.25 MM	0.25 MM
IMVP6_BOOT2	0.25 MM	0.25 MM
IMVP6_UGATE2	0.25 MM	0.25 MM
IMVP6_LGATE2	0.25 MM	0.25 MM
IMVP6_ISEN2	0.25 MM	0.25 MM
IMVP6_FET_RC2	0.25 MM	0.25 MM
IMVP6_VSUM_R2	0.60 MM	0.25 MM
R7507_1	0.25 MM	0.25 MM

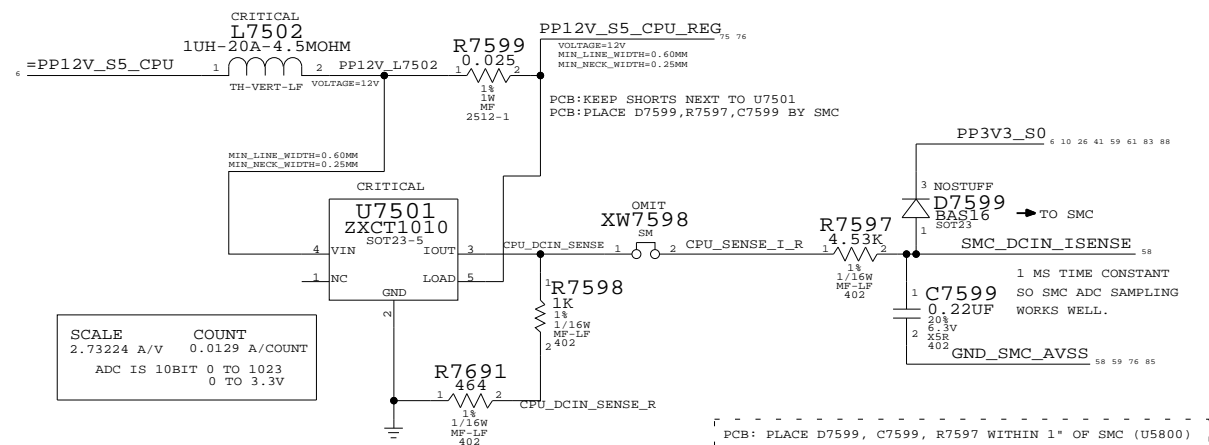
Signal	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_OCSET	0.25 MM	0.20 MM
IMVP6_VSUM	0.25 MM	0.20 MM
GND_IMVP6_SGND	0.50 MM	0.20 MM
IMVP6_VO	0.25 MM	0.20 MM
IMVP6_DROOP	0.25 MM	0.20 MM
IMVP6_DFB	0.25 MM	0.20 MM
IMVP6_SOFT	0.25 MM	0.20 MM
IMVP6_RBIAS	0.25 MM	0.20 MM
IMVP6_VDIFF	0.25 MM	0.20 MM
IMVP6_FB2	0.25 MM	0.20 MM
IMVP6_FB	0.25 MM	0.20 MM
IMVP6_COMP	0.25 MM	0.20 MM
IMVP6_VW	0.25 MM	0.25 MM
IMVP6_RTIN	0.25 MM	0.25 MM
IMVP6_VSEN	0.25 MM	0.25 MM

IMVP6 CPU VCore Regulator
 SYNC_MASTER=POWER SYNC_DATE=07/08/2005

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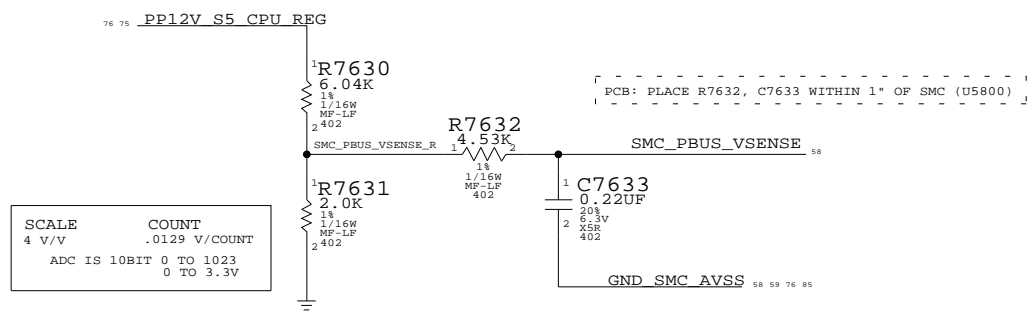
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	13
SCALE	SHEET	OF	
NONE	75	110	

PROCESSOR VCORE CURRENT SENSE
(USING 12V INPUT CURRENT TO DERIVE CPU CURRENT)



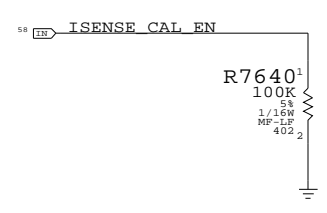
SCALE	COUNT
2.73224 A/V	0.0129 A/COUNT
ADC IS 10BIT 0 TO 1023	
0 TO 3.3V	

PROCESSOR DCIN VOLTAGE SENSE
(SCALING 12V INPUT VOLTAGE TO SMC)

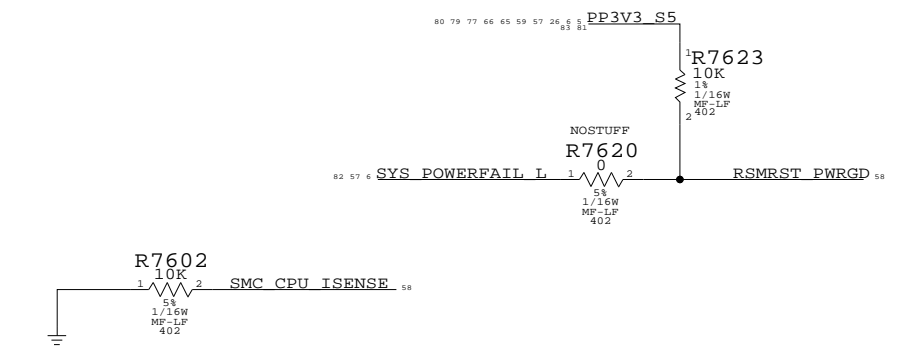


SCALE	COUNT
4 V/V	.0129 V/COUNT
ADC IS 10BIT 0 TO 1023	
0 TO 3.3V	

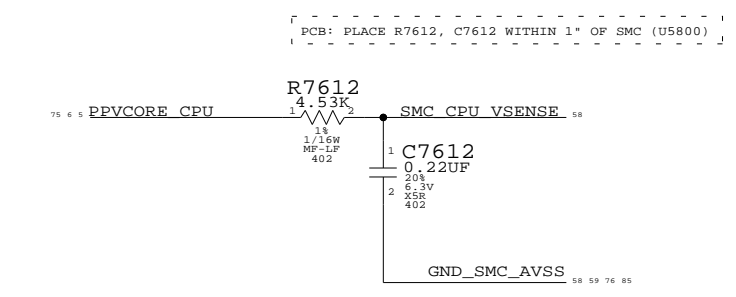
Current Sense Calibration Circuit
Switches in fixed load on power supplies to calibrate current sense circuits



SMC PWRGD PULLUP



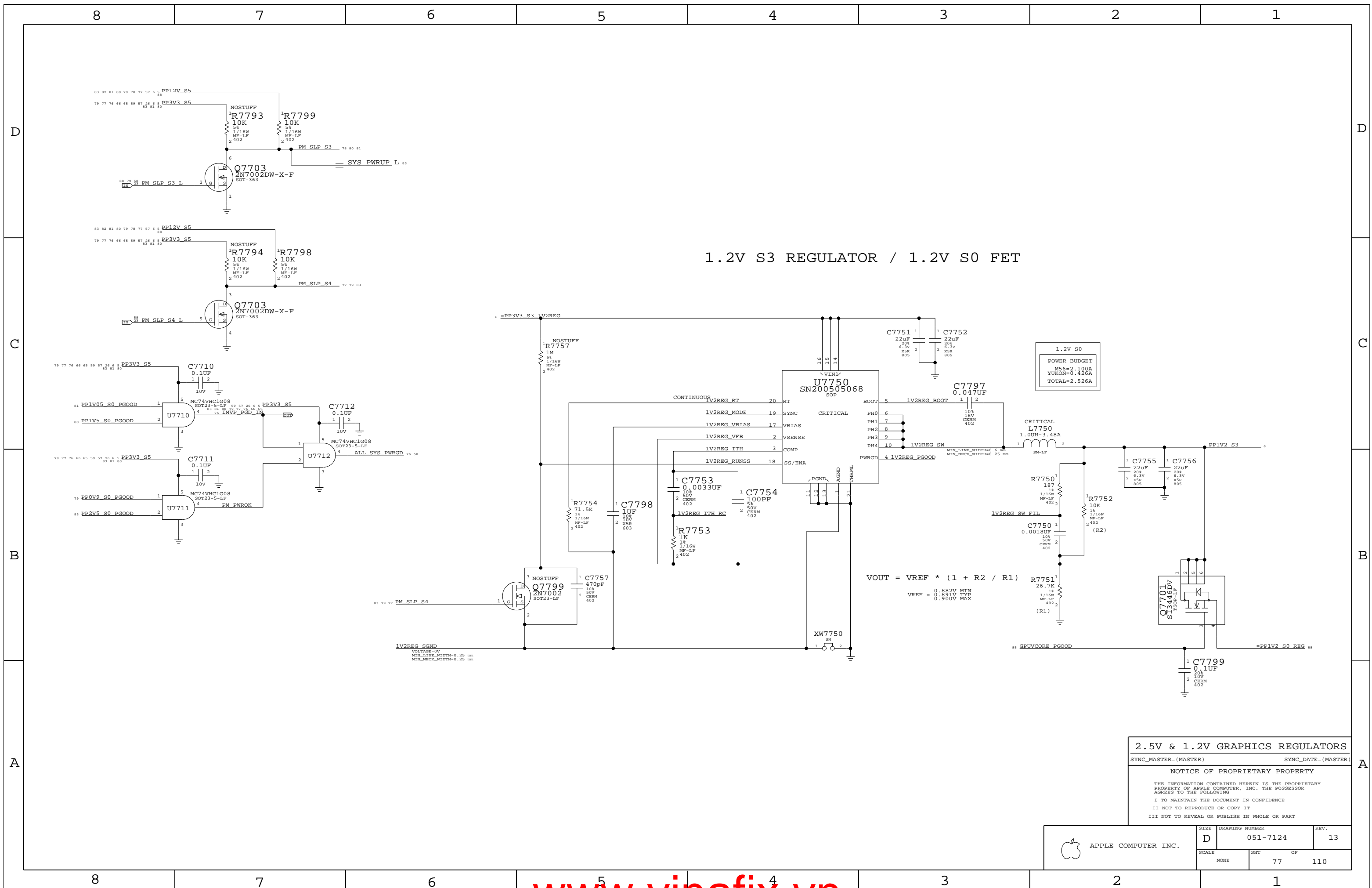
PROCESSOR VCORE SENSE



CPU SENSE CIRCUITRIES
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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	D	051-7124	13
SCALE	SHT	76 OF	110
NONE			



1.2V S3 REGULATOR / 1.2V S0 FET

1.2V S0	
POWER BUDGET	
M56=	2.100A
YUKON=	0.426A
TOTAL=	2.526A

$$V_{OUT} = V_{REF} * (1 + R2 / R1)$$

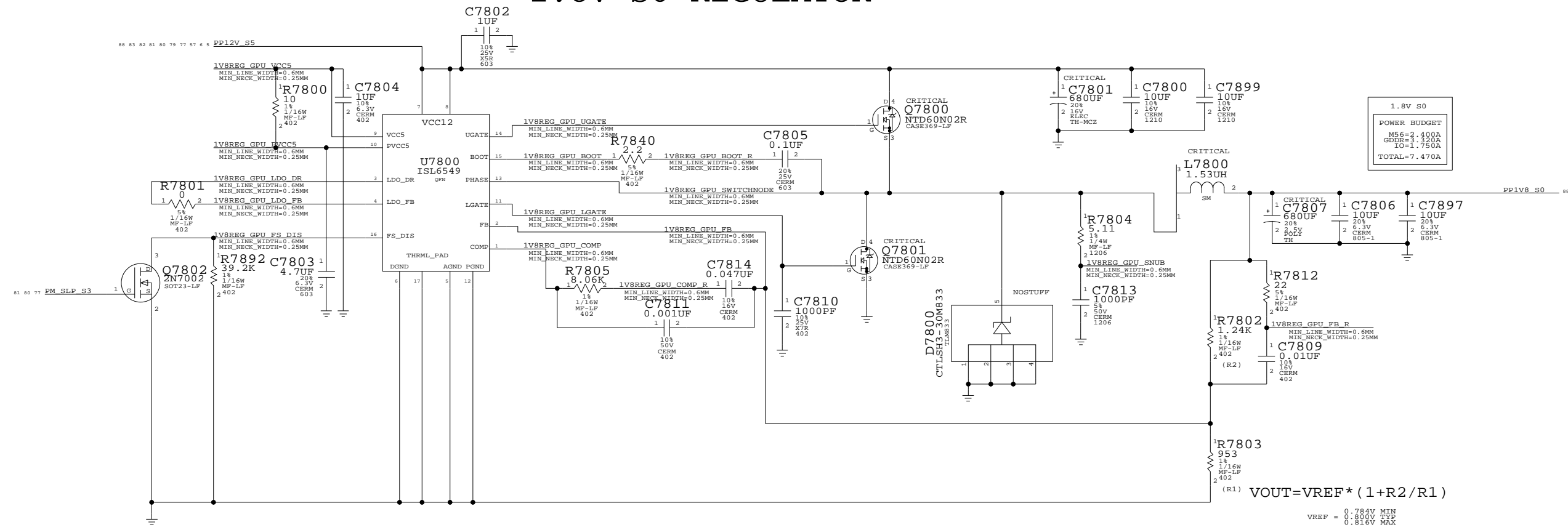
$V_{REF} = 0.82V \text{ MIN}$
 $0.891V \text{ TYP}$
 $0.900V \text{ MAX}$

2.5V & 1.2V GRAPHICS REGULATORS

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	13
SCALE	SHT	OF	
NONE	77	110	

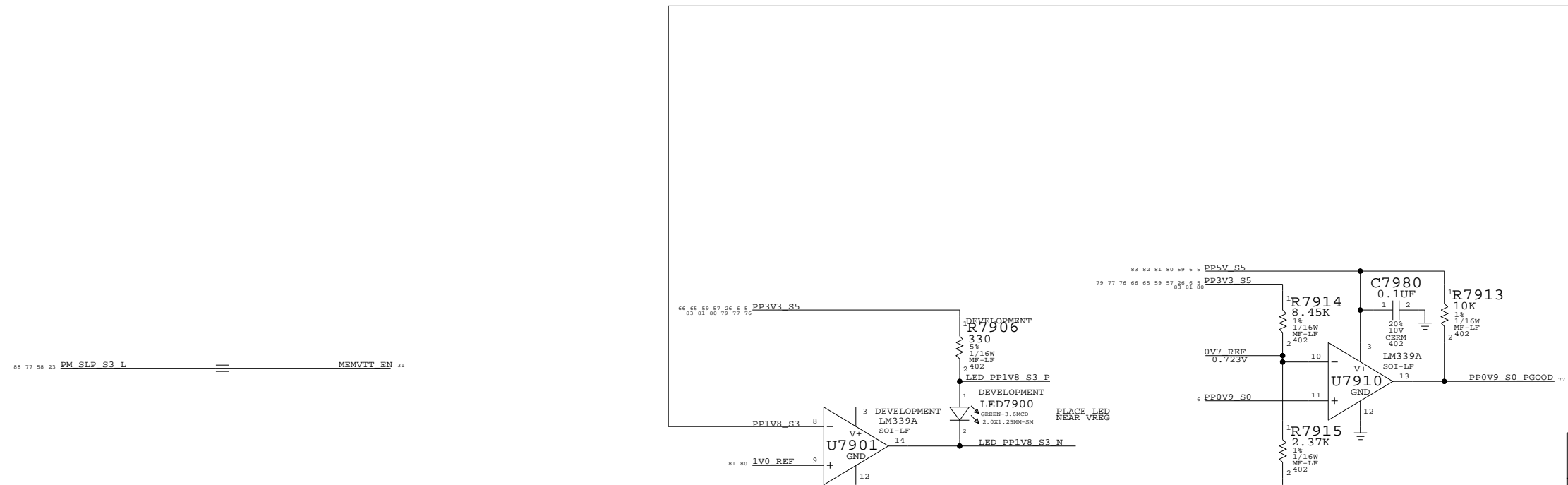
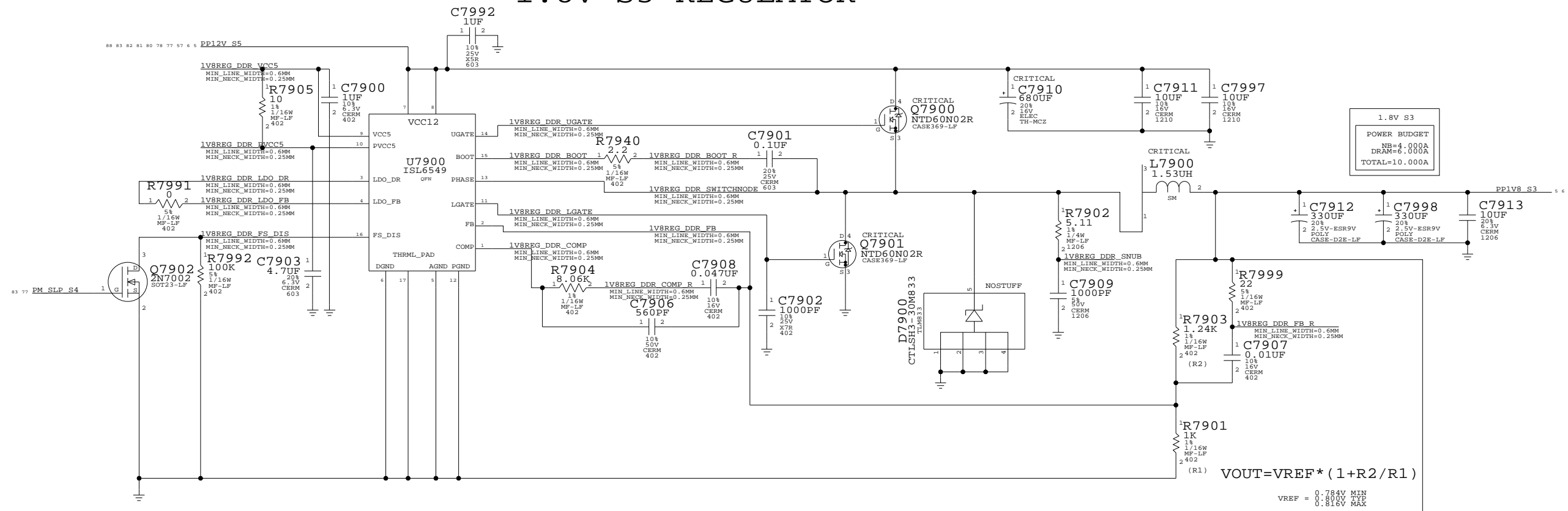
1.8V S0 REGULATOR



1.8V GDDR REGULATOR
 SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	13
SCALE	SHT	78 OF 110	
NONE		TRUE	

1.8V S3 REGULATOR

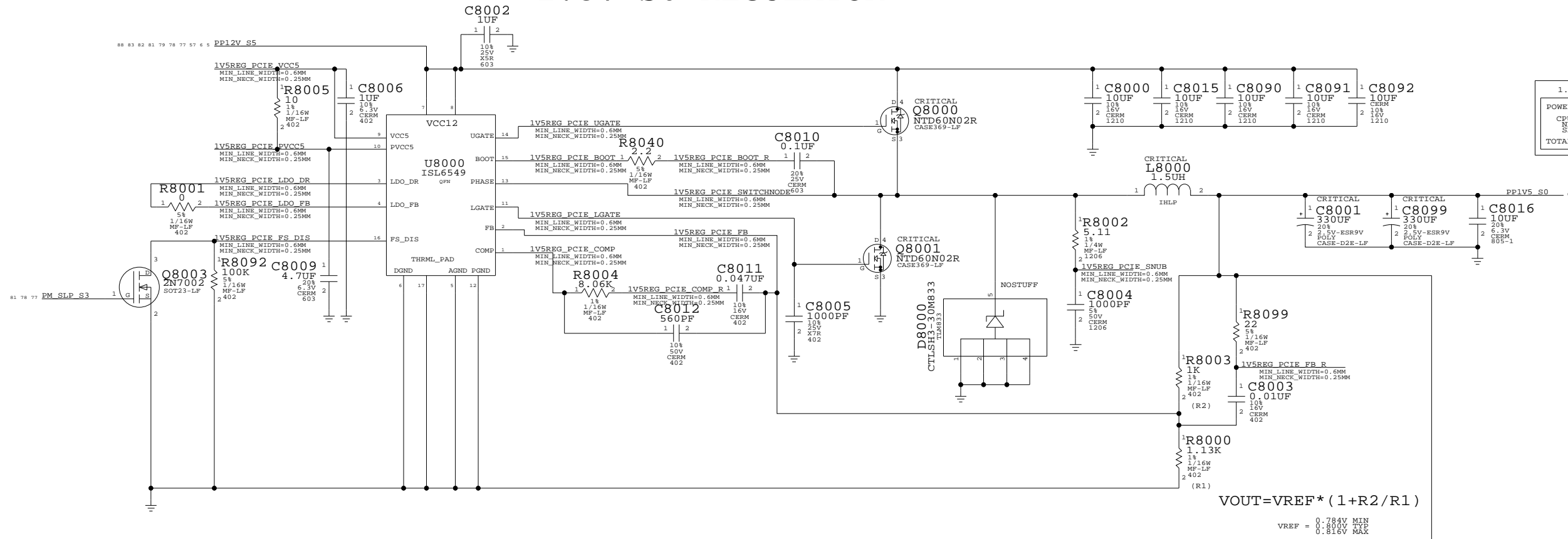


1.8V Vreg
 SYNC_MASTER=M23-PC SYNC_DATE=04/12/2005

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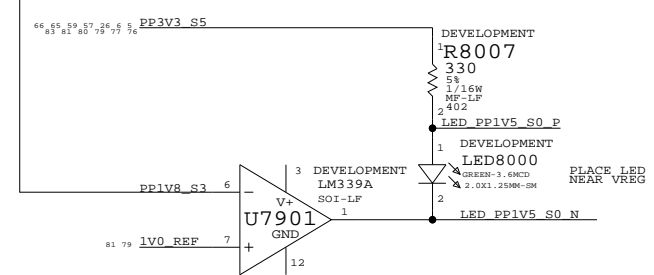
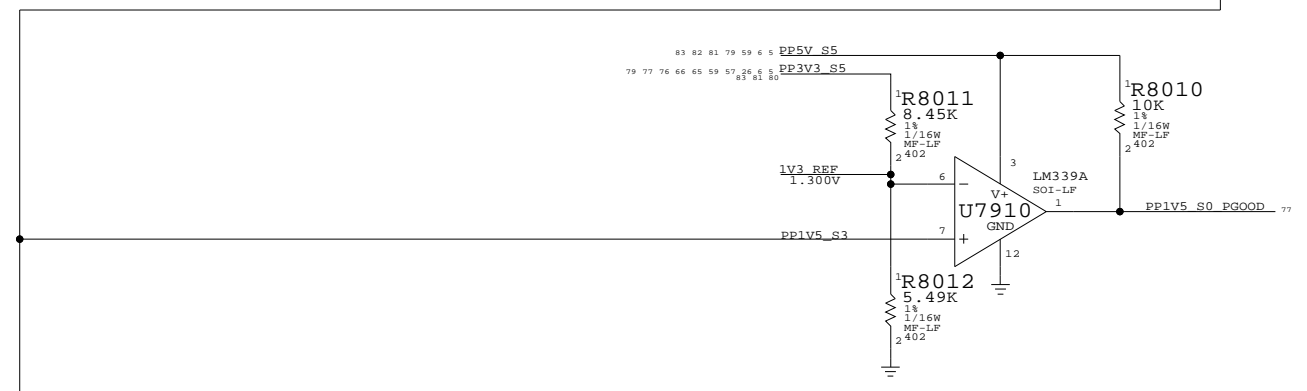
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	13
SCALE	SHT	79 OF	110
NONE			

1.5V S0 REGULATOR



$$V_{OUT} = V_{REF} * (1 + R2/R1)$$

$V_{REF} = 0.784V \text{ MIN}$
 $0.800V \text{ TYP}$
 $0.816V \text{ MAX}$



1.5V Vreg

SYNC_MASTER=FINO-PC SYNC_DATE=05/18/2005

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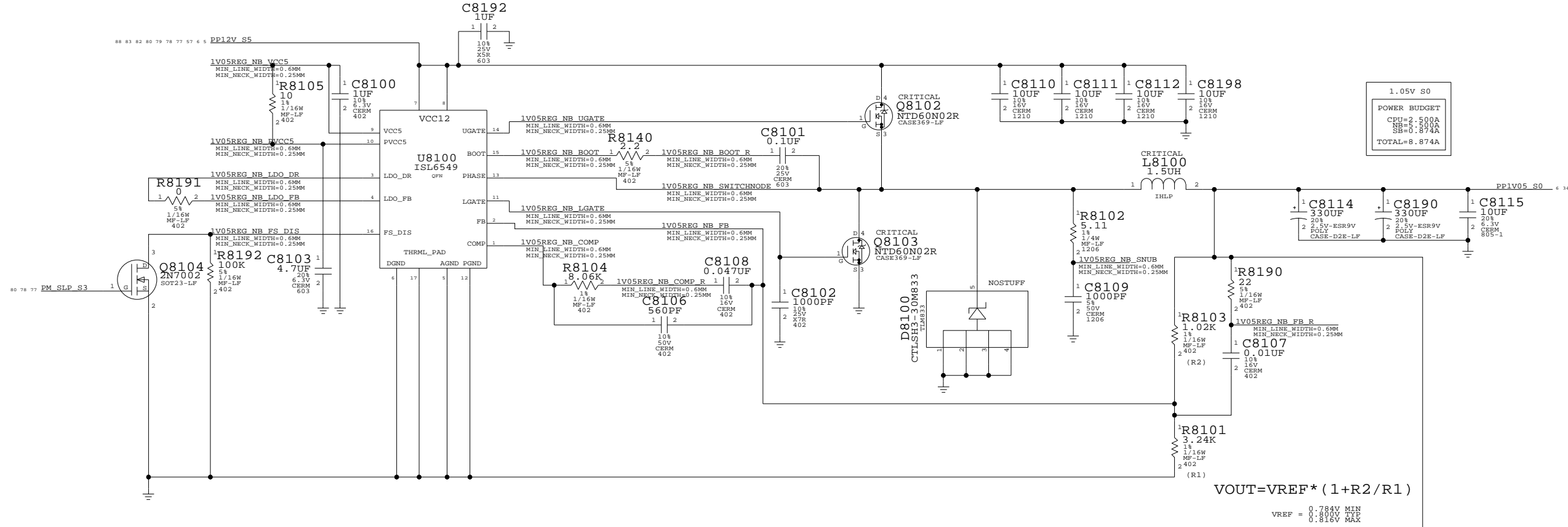
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	13
SCALE	SHT	80 OF	110
NONE			

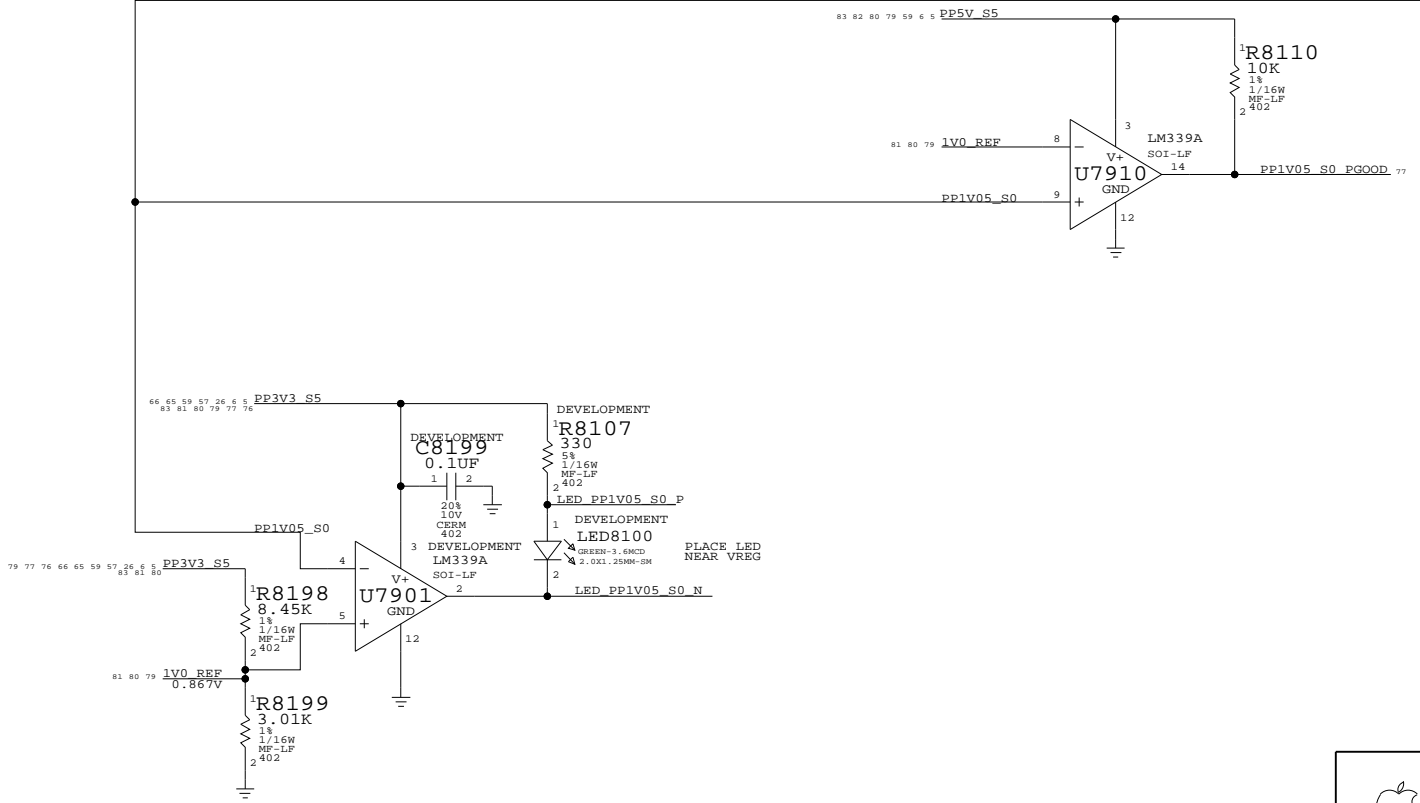
1.05V S0 REGULATOR



1.05V S0	
POWER BUDGET	
CPU=2.500A	
NB=0.800A	
SB=0.874A	
TOTAL=8.874A	

$$V_{OUT} = V_{REF} * (1 + R2/R1)$$

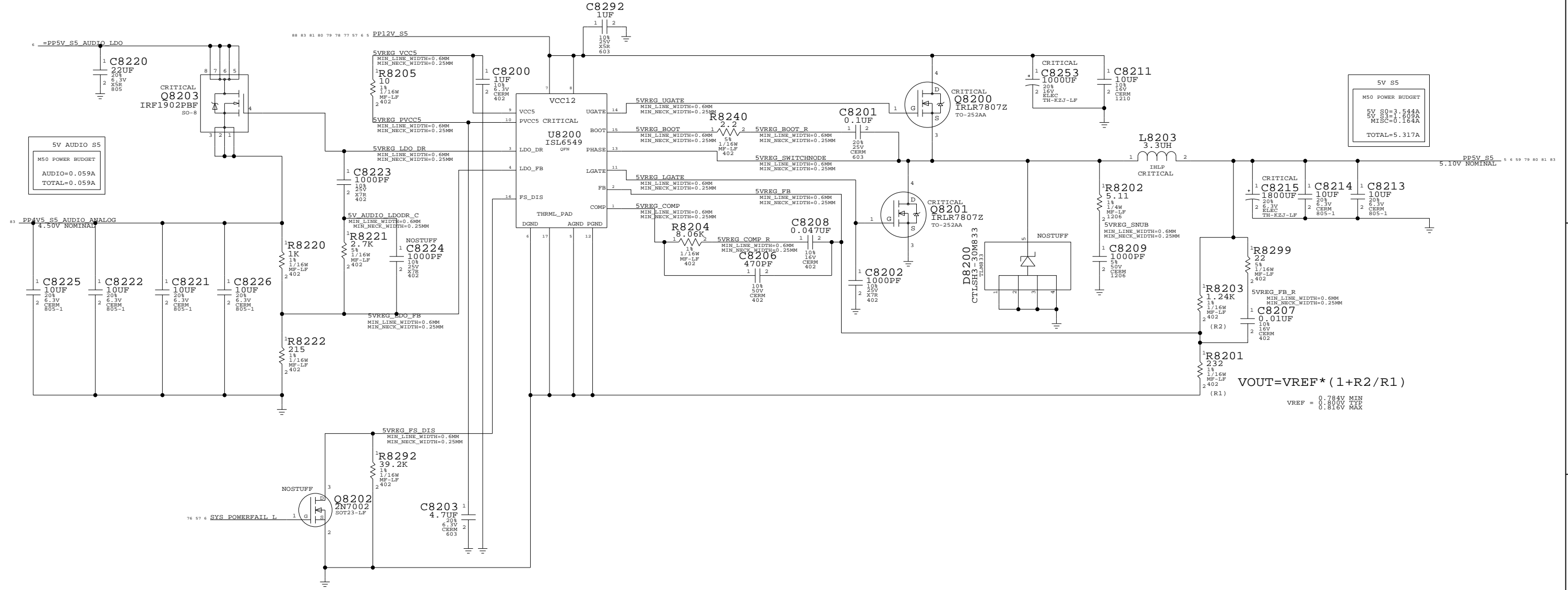
$V_{REF} = 0.784V \text{ MIN}$
 $0.800V \text{ TYP}$
 $0.816V \text{ MAX}$



1.05V VREG	
SYNC_MASTER=M38-RT	SYNC_DATE=05/18/2005
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	13
SCALE	SHT	81 OF	110
NONE			

5V S5 AND 5V AUDIO S5 REGULATOR



5V DC/DC 4.5V

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

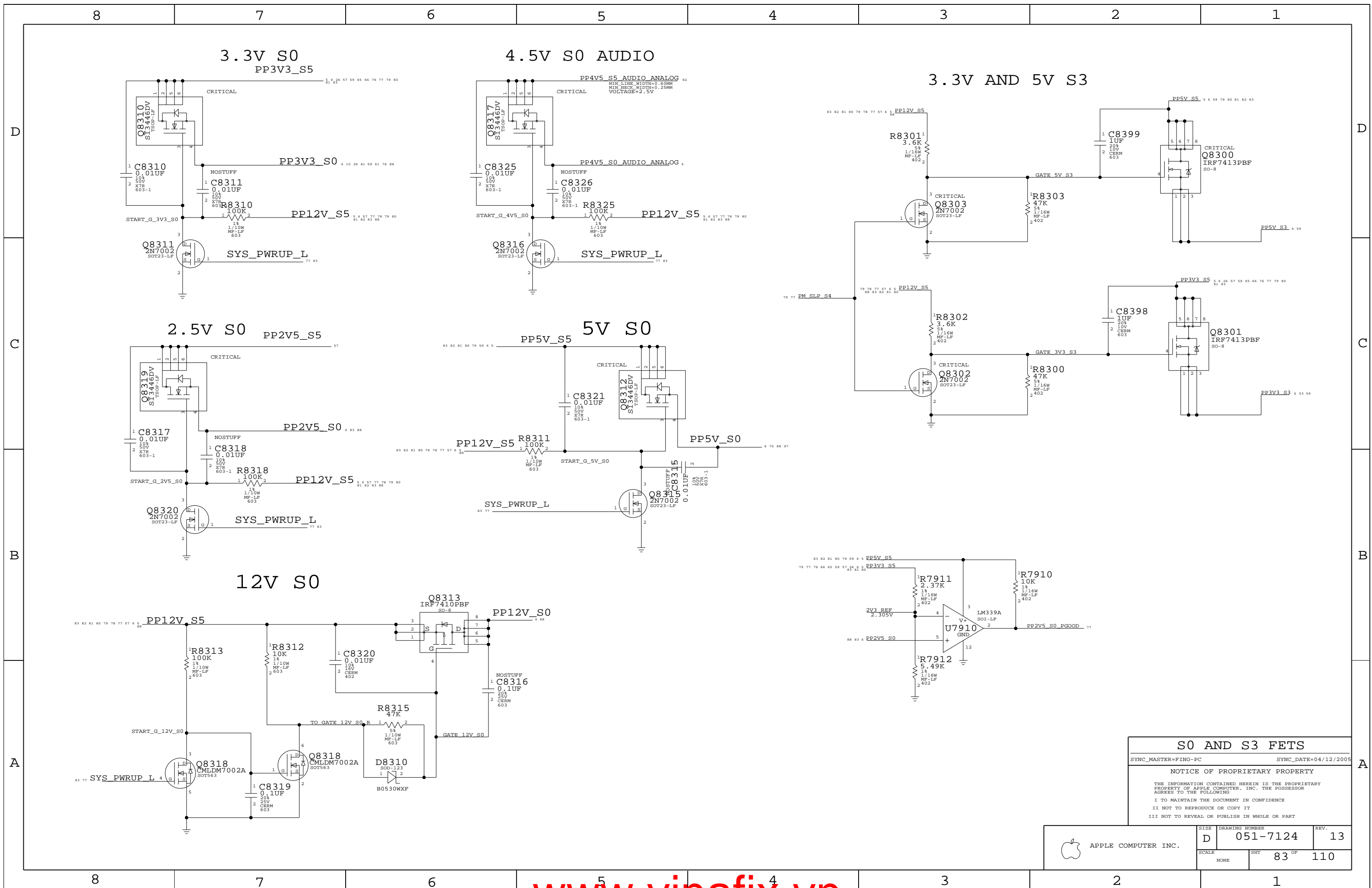
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	D	051-7124	13
SCALE	SHT	82 OF	110
NONE			



S0 AND S3 FETS

SYNC_MASTER=FINO-PC SYNC_DATE=04/12/2005

NOTICE OF PROPRIETARY PROPERTY

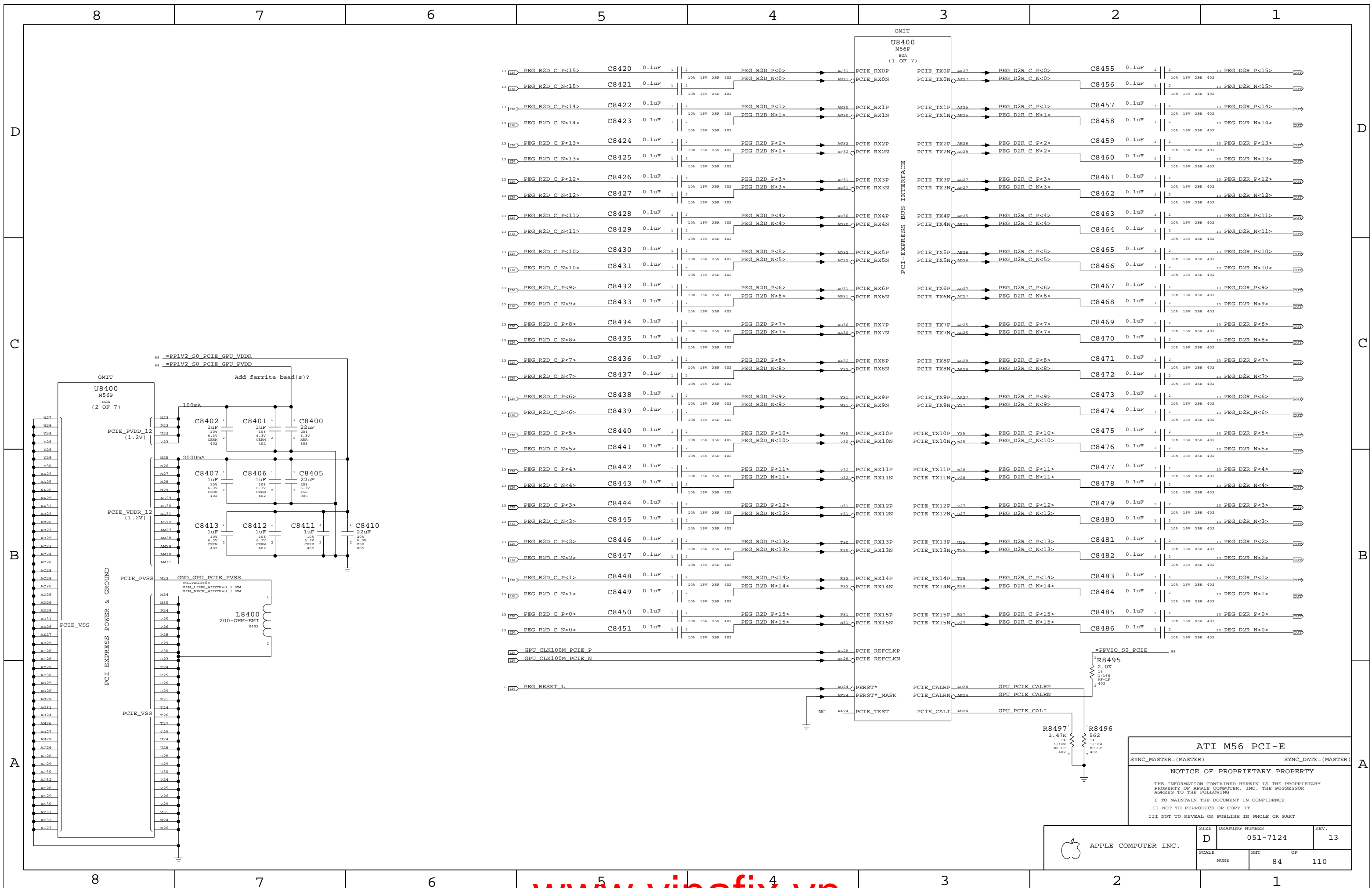
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7124	REV. 13
	SCALE NONE	SHT 83 OF	110



ATI M56 PCI-E

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

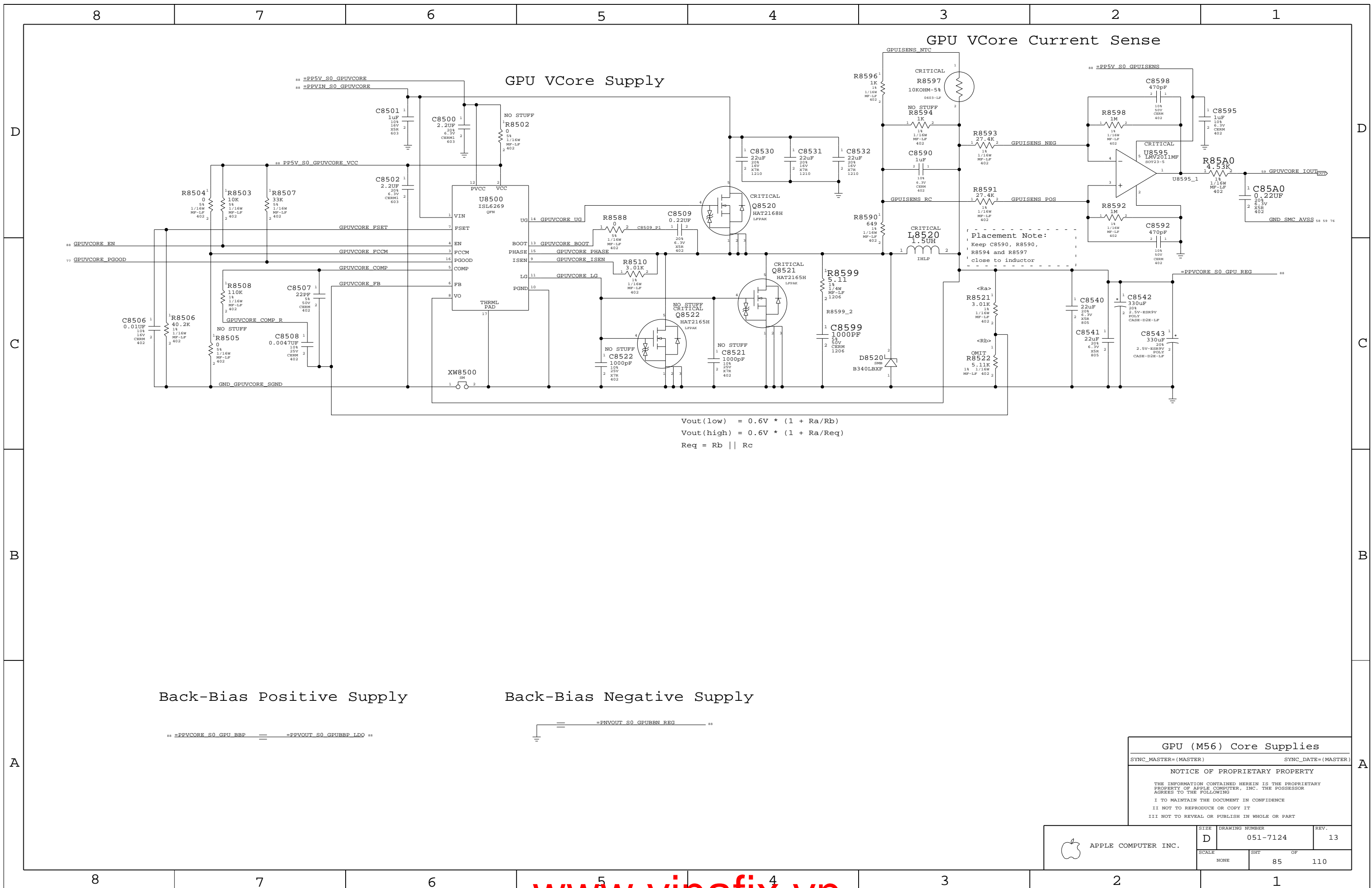
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7124	REV. 13
	SCALE NONE	SHEET 84	OF 110

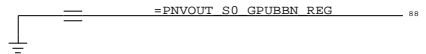


$V_{out}(low) = 0.6V * (1 + R_a/R_b)$
 $V_{out}(high) = 0.6V * (1 + R_a/R_{eq})$
 $R_{eq} = R_b || R_c$

Back-Bias Positive Supply

== PPVCORE_S0_GPU_BBP == PPVOUT_S0_GPUBBP_LDO ==

Back-Bias Negative Supply



GPU (M56) Core Supplies

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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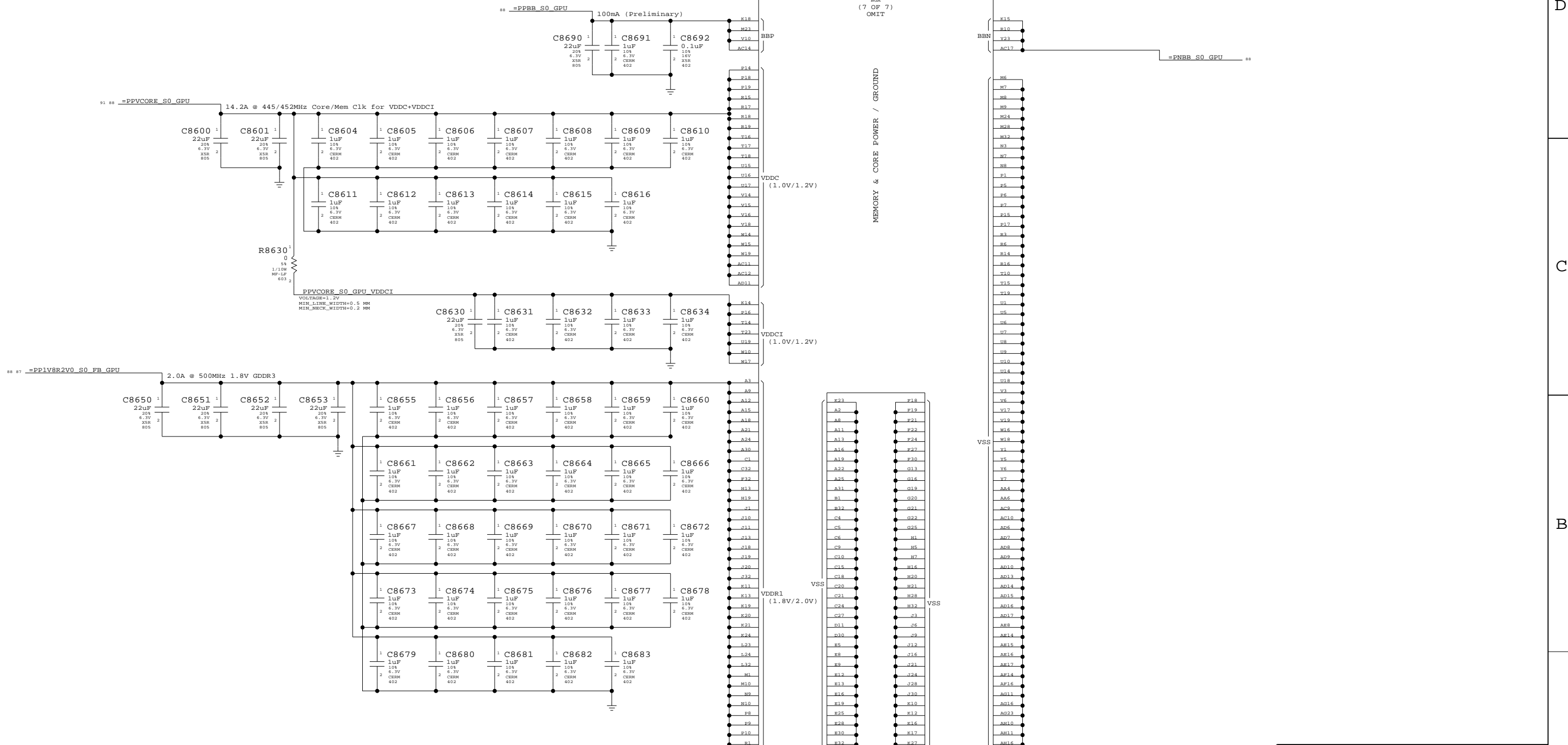
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	13
SCALE	SHT	OF	
NONE	85	110	

Page Notes

Power aliases required by this page:
 - =PP1V5_GPU_VDD15
 - =PP1VR1V3_GPU_VCORE

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)



ATI M56 Core Power

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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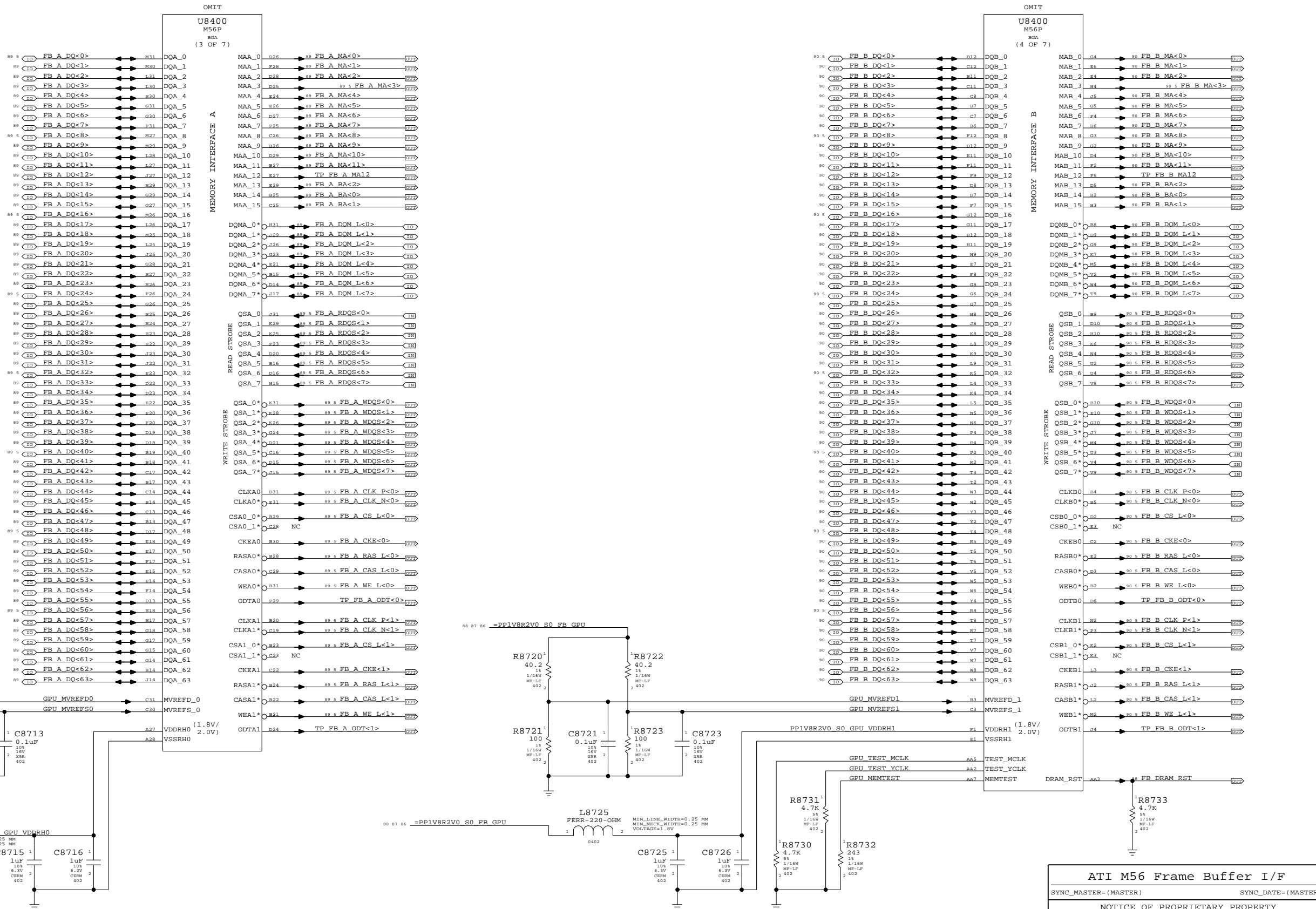
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	13
SCALE	SHT	OF	
NONE	86	110	

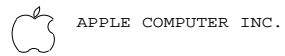
Page Notes

Power aliases required by this page:
- =PP1V8R2V0_S0_FB_GPU
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
(NONE)



ATI M56 Frame Buffer I/F
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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Table with columns: SIZE (D), DRAWING NUMBER (051-7124), REV. (13), SCALE (NONE), SHEET (87 OF 110).



8

7

6

5

4

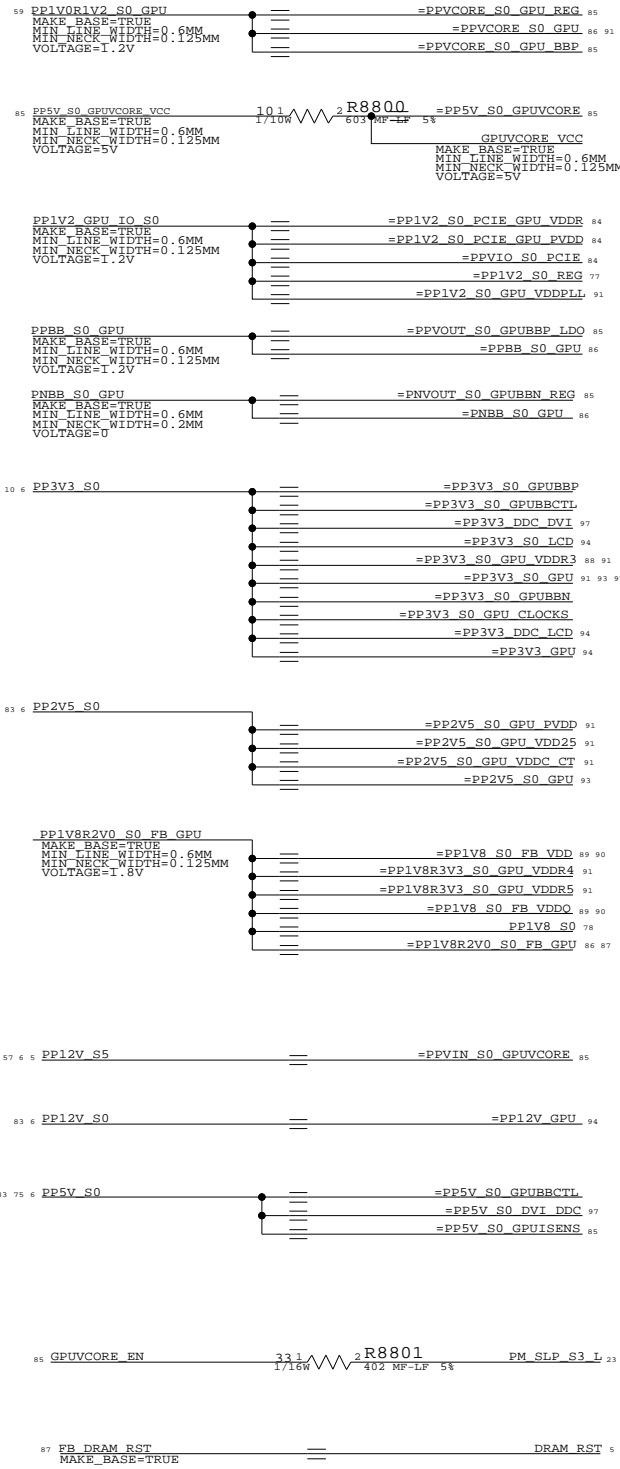
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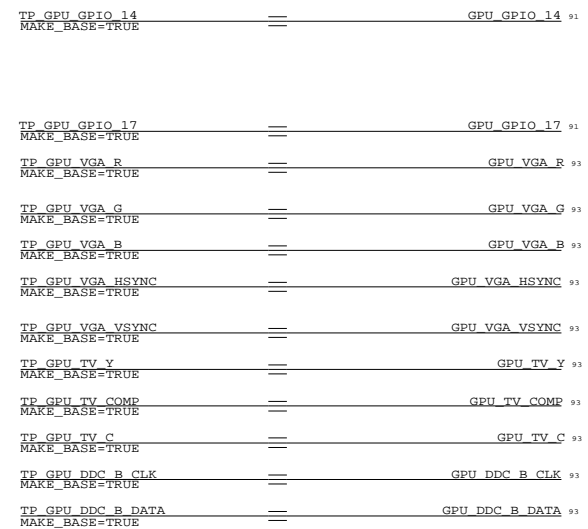
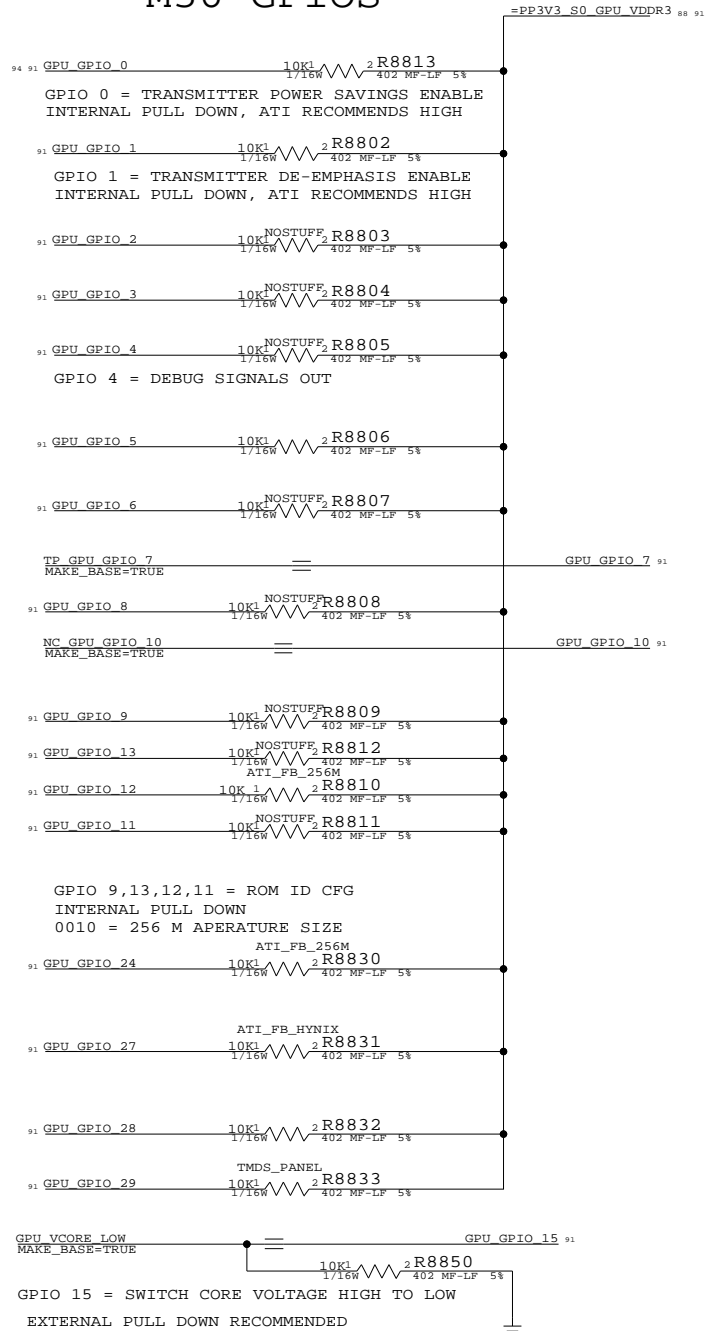
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"S0" GPU RAILS

ONLY ON IN RUN



M56 GPIOs



GPU MISC

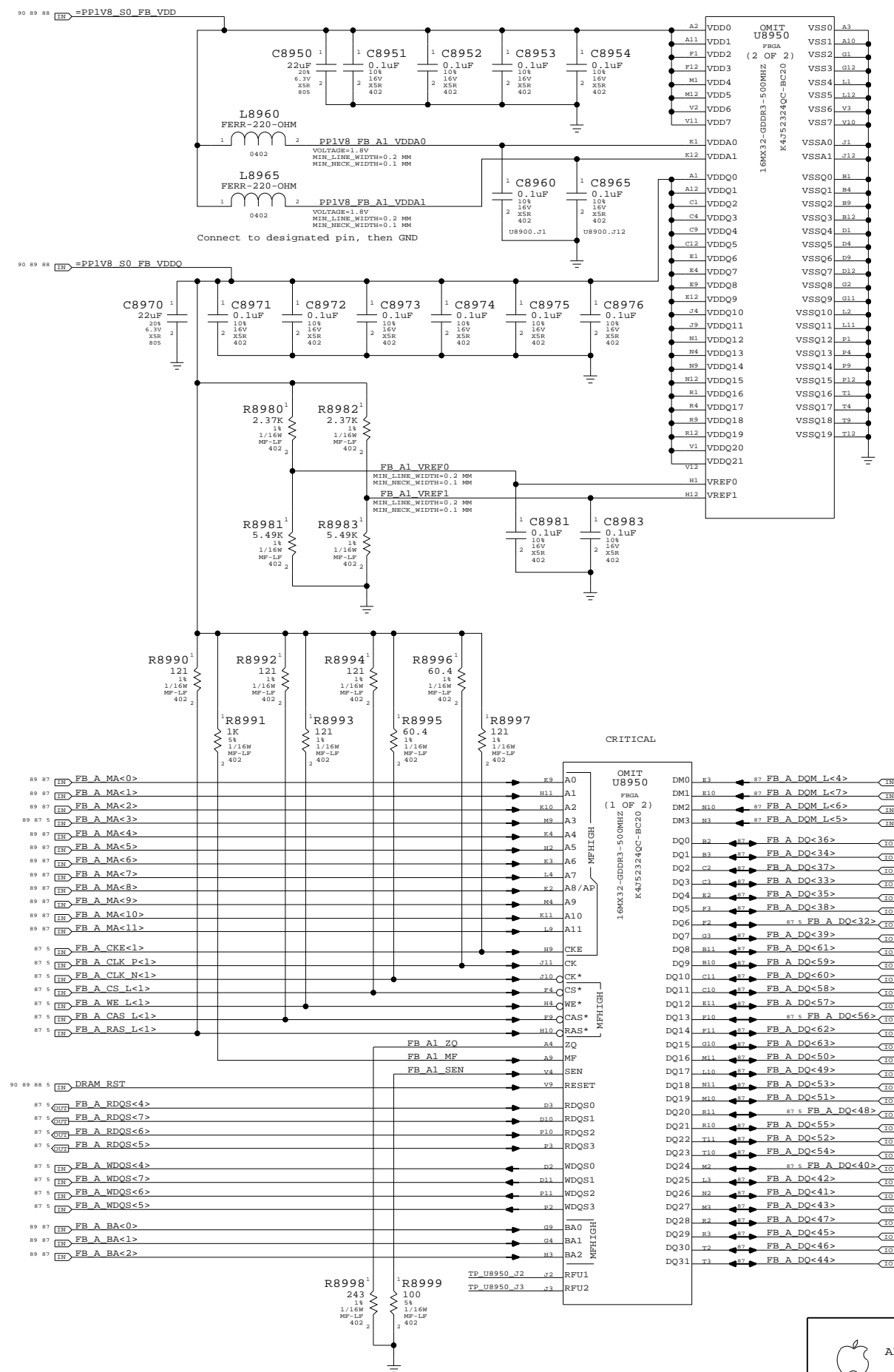
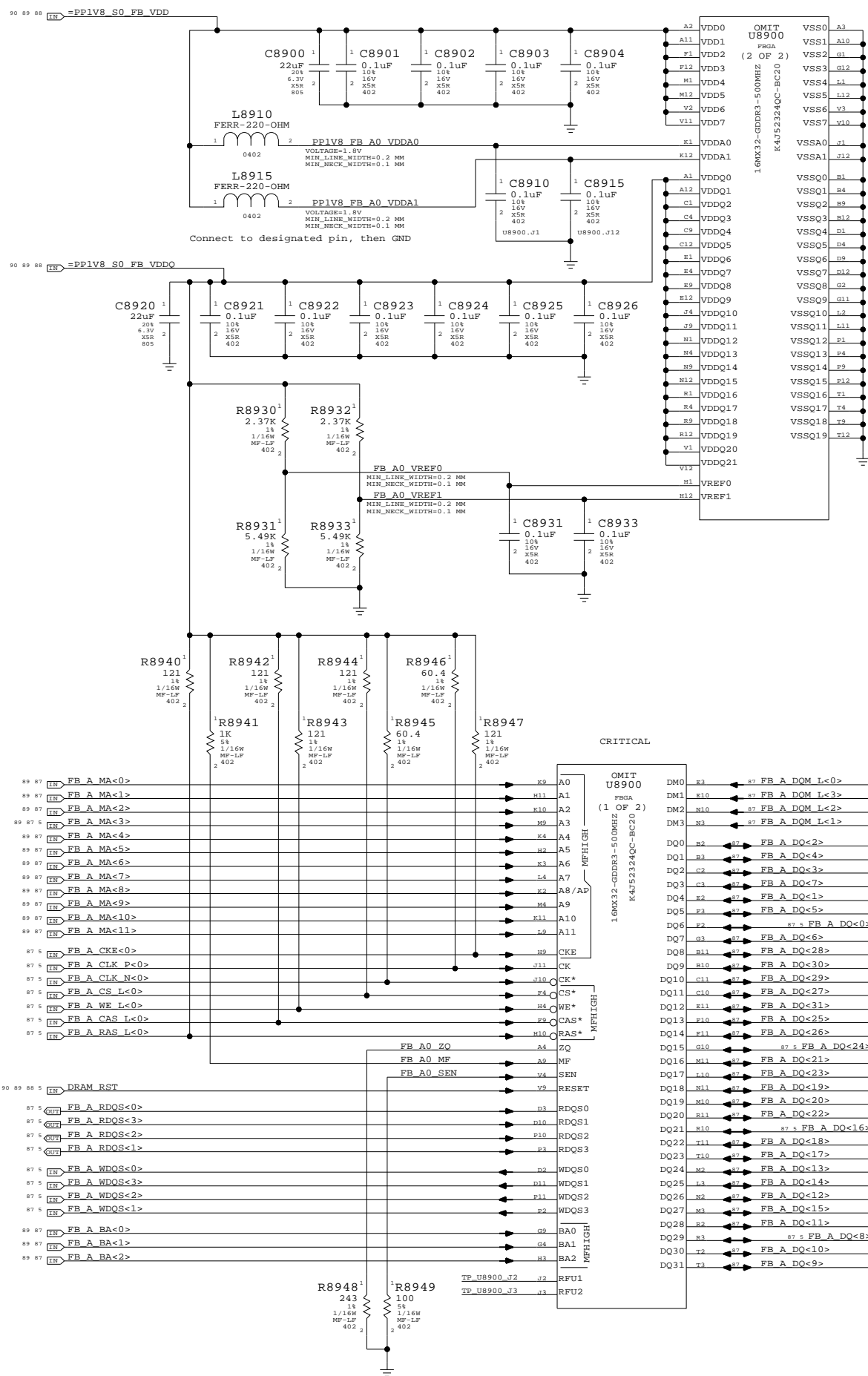
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 - =PPIV8_S0_FB_VDDQ

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

CRITICAL

CRITICAL



GDDR3 Frame Buffer A

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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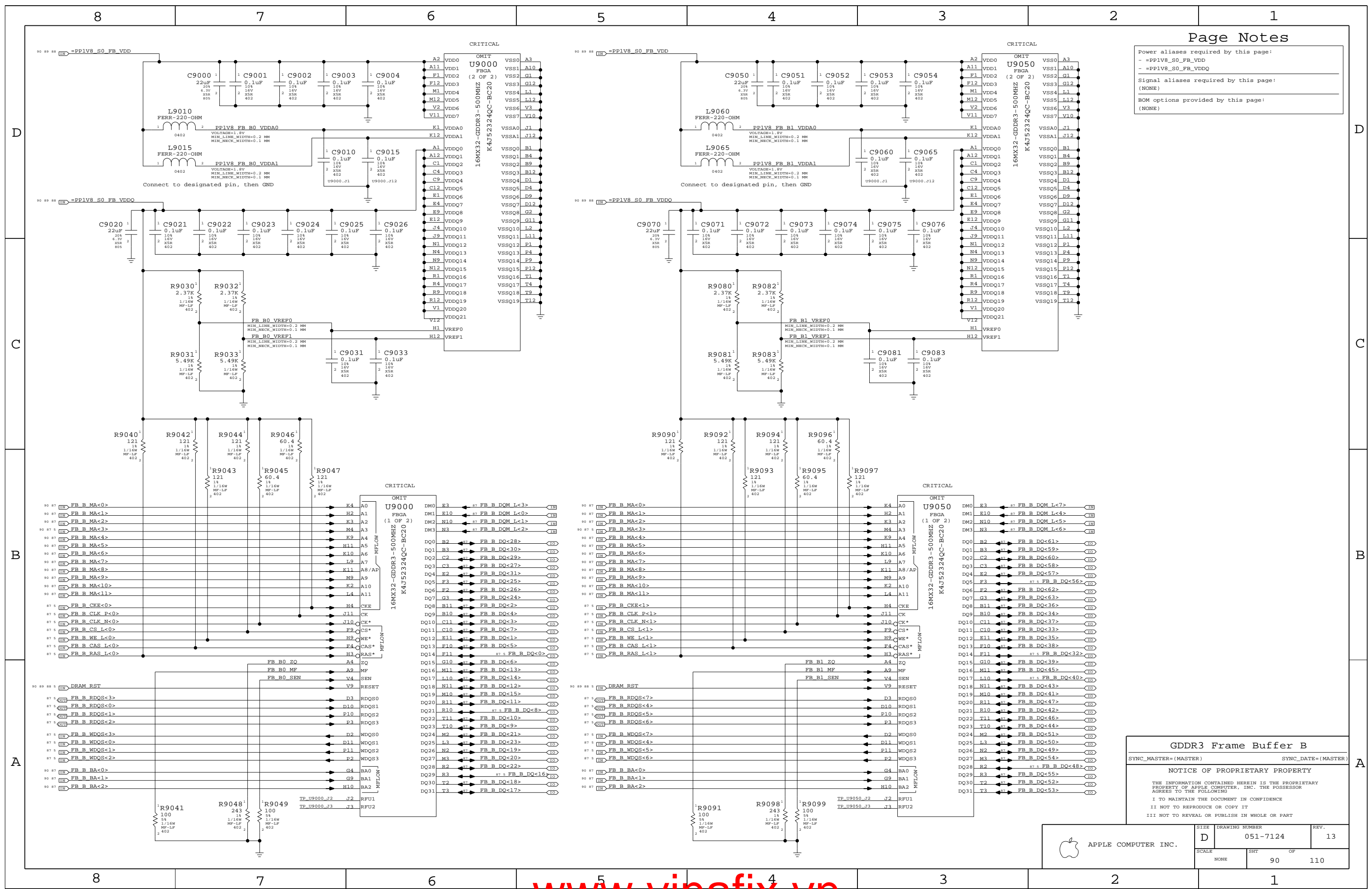
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	13
SCALE	SHT	OF	
NONE	89	110	

Power aliases required by this page:
 - =PPIV8_S0_FB_VDD
 - =PPIV8_S0_FB_VDDQ

Signal aliases required by this page:
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BOM options provided by this page:
 (NONE)



GDDR3 Frame Buffer B

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	13
SCALE	SHT	OF	
NONE	90	110	

Page Notes

Power aliases required by this page:
 - =PP3V3_GPU_GPIOS
 - =PP2V5_PVDD
 - =PP1V8_GPU_LVDS_PLL

Signal aliases required by this page:
 - =I2C_GPU_TMDS_SDA - I2C data line for external TMDS transmitters
 - =I2C_GPU_TMDS_SCL - I2C clock line for external TMDS transmitters

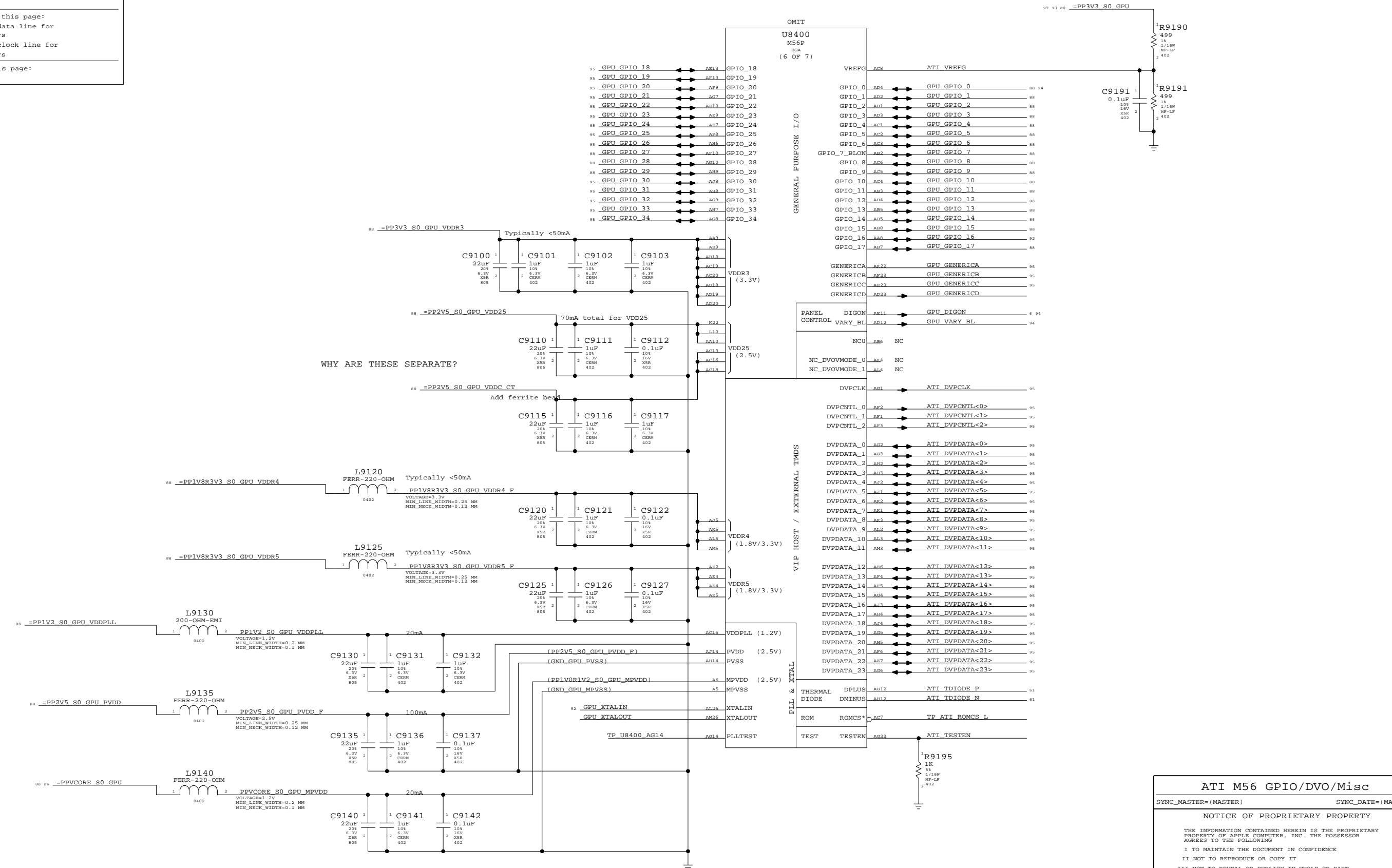
BOM options provided by this page:
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ATI M56 GPIO/DVO/Misc		
SYNC_MASTER=(MASTER)		SYNC_DATE=(MASTER)
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	13
SCALE	SHT	OF	
NONE	91	110	

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Page Notes

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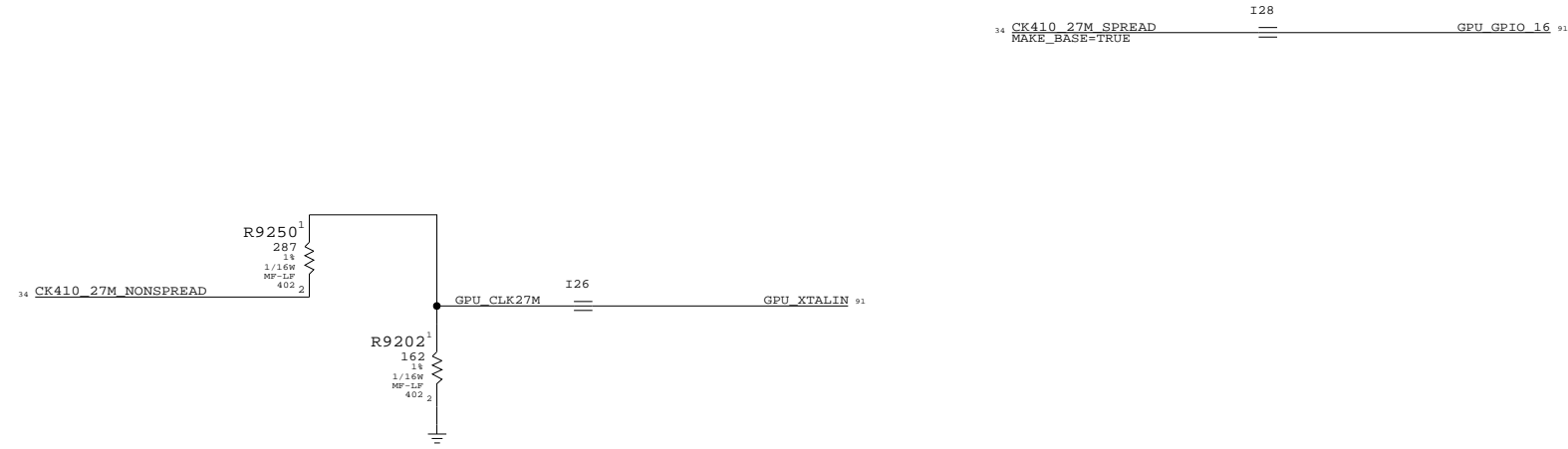
- =PP3V3_GPU_CLOCKS - =PP3V3_GPU_PWRSEQ
- =PPVIN_GPU_LVDDR_LDO - =PP2V5_GPU_PWRSEQ
- =PP2V5_GPU_LVDDR_LDO - =PP1V8_GPU_PWRSEQ
- =PP1V5_GPU_PWRSEQ

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

- GPU_SS - GPU_LVDDR_2V8




GPU CLOCKS

SYNC_MASTER=BOZEMAN SYNC_DATE=05/21/2005

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 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
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SCALE	SHT	OF	
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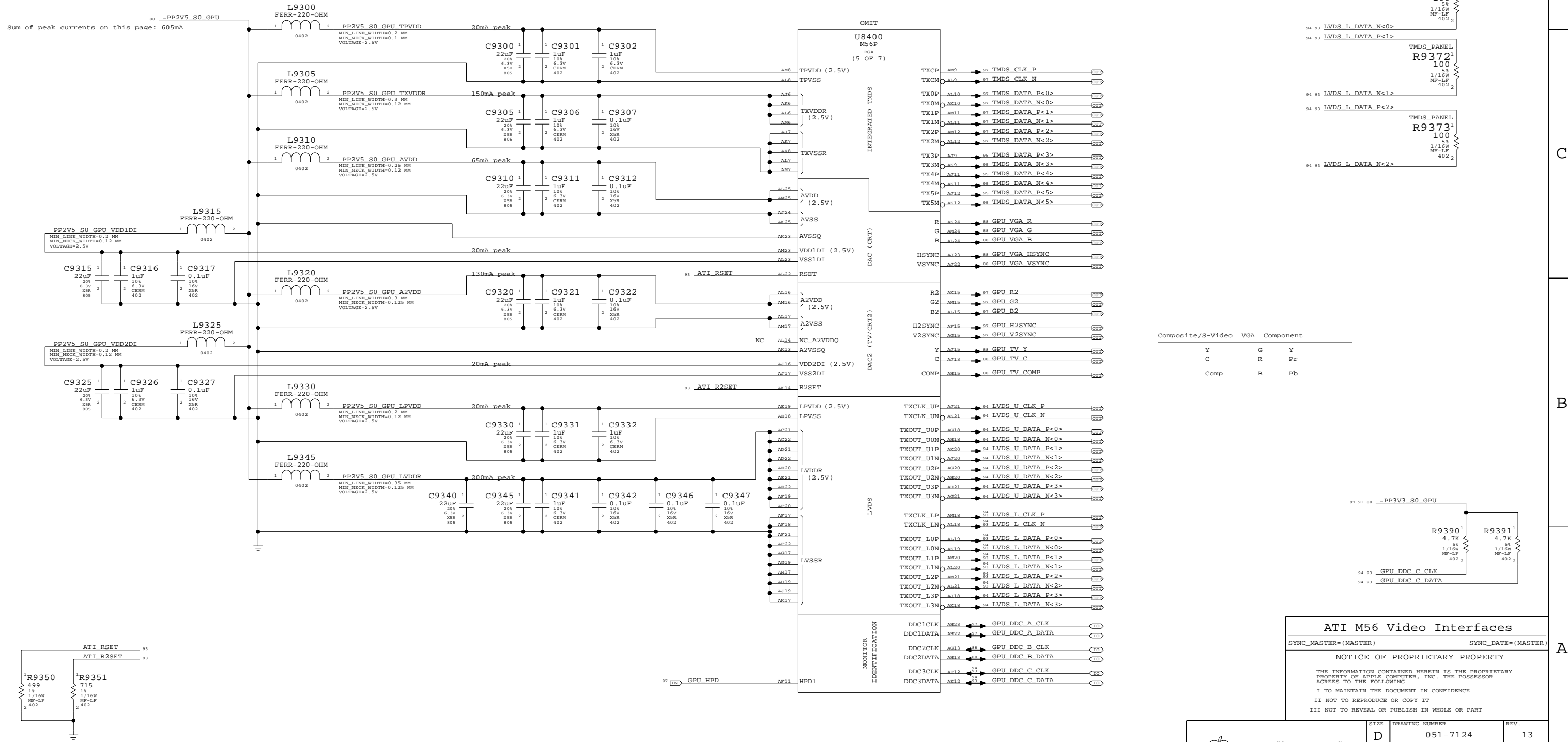
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 - =PP1V8R2V5_S0_GPU_LVDDR

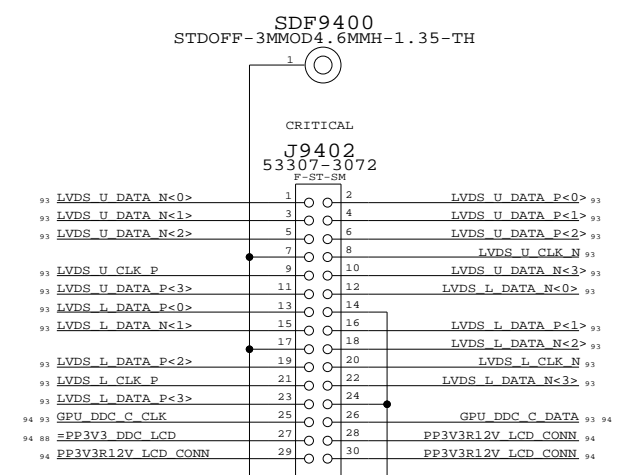
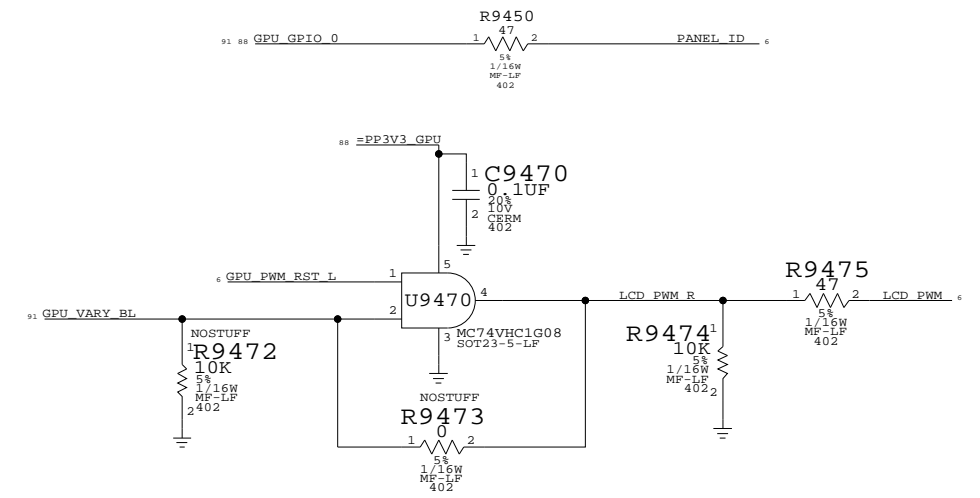
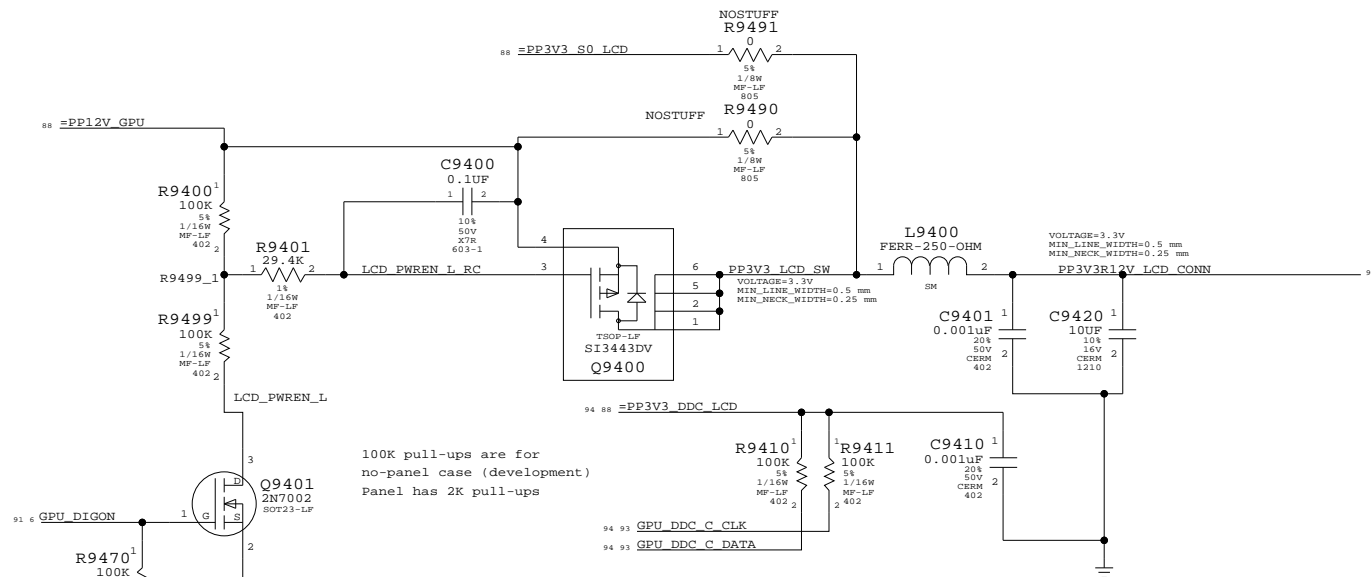
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BOM options provided by this page:
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TERMINATION FOR TMDS USAGE OF LVDS PINS
 PLACE CLOSE TO GPU (U8400)



LCD (LVDS) INTERFACE



Internal Display Conns
 SYNC_MASTER=BOZEMAN SYNC_DATE=04/27/2005
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
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SCALE	SHT	OF	
NONE	94	110	

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B

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M56 TPS


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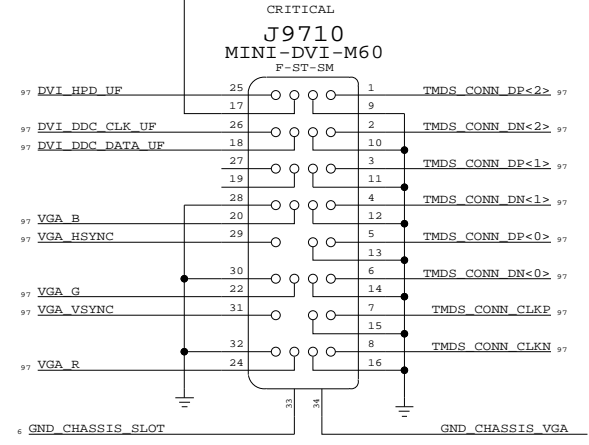
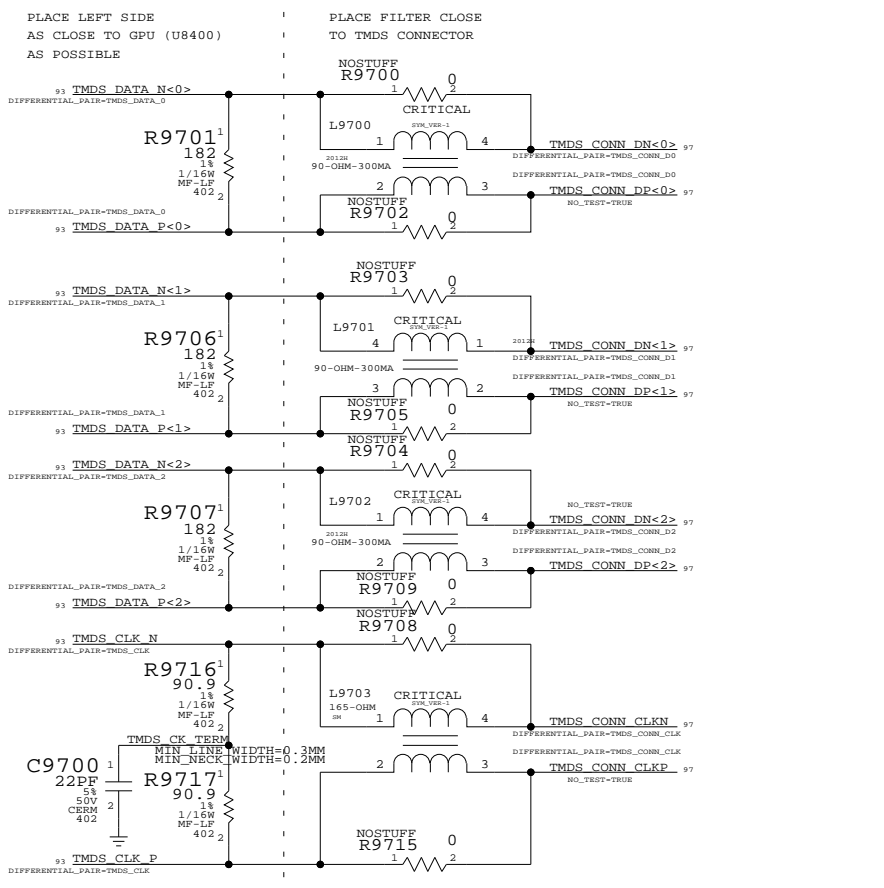
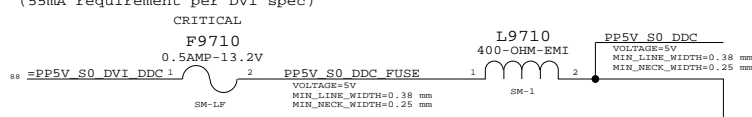
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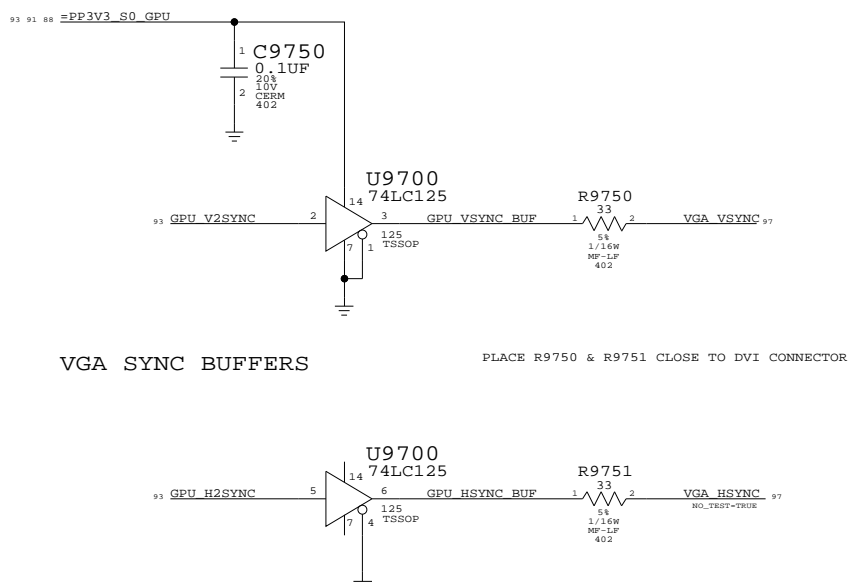
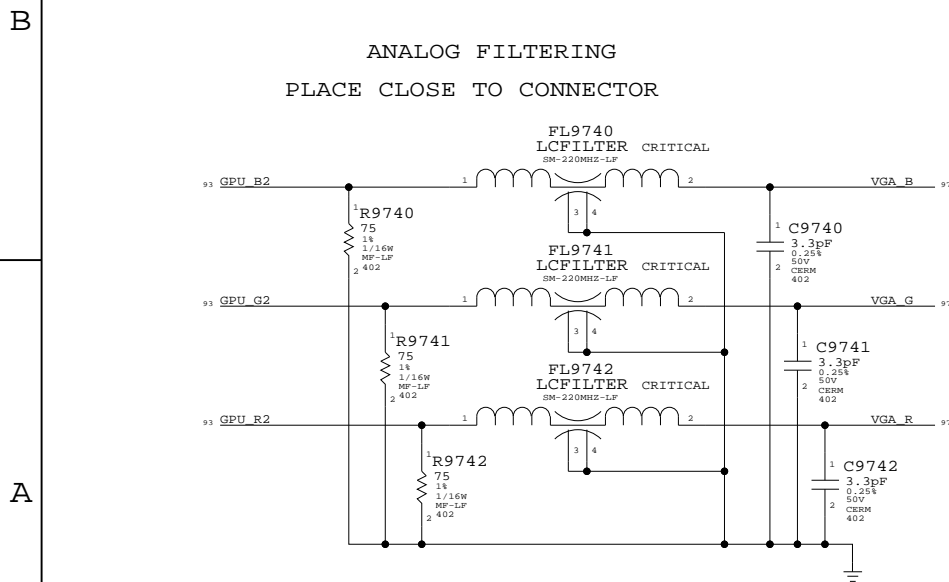
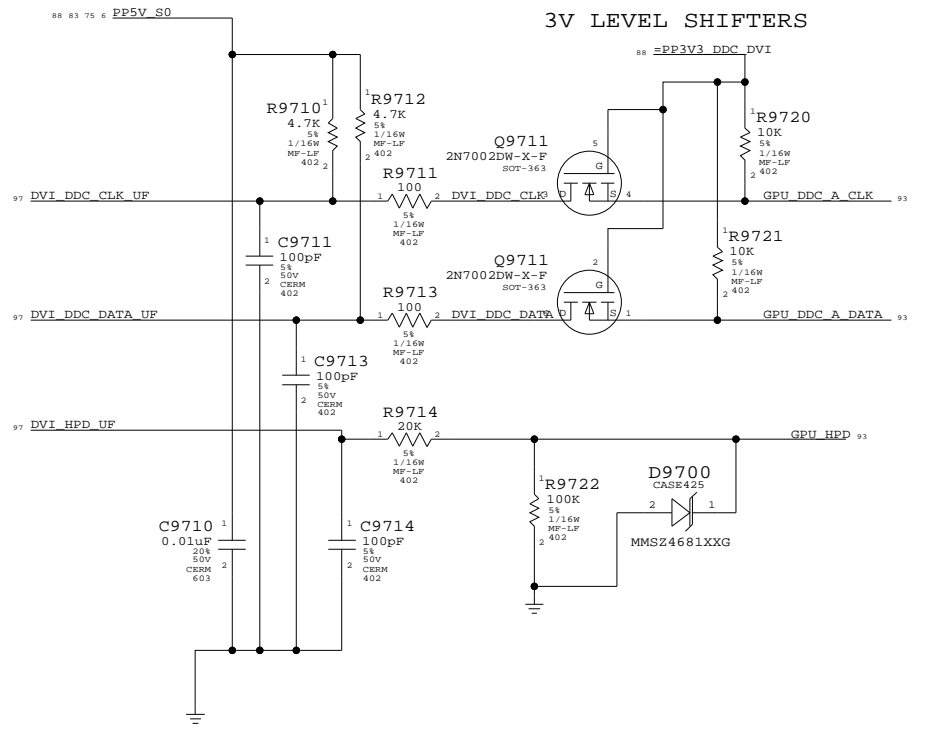
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SCALE	SHT	OF	
NONE	95	110	

DVI DDC CURRENT LIMIT DVI INTERFACE



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
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External Display Conns
 SYNC_MASTER=BOZEMAN SYNC_DATE=04/14/2005

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SCALE	SHT	OF	
NONE	97	110	

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	Design: m60	C2514 CAP_402	m60[25C6]	C4113 CAP_402	m60[41C4]	C5797 CAP_1210	m60[57D2]		
	Date: May 12 10:16:43 2006	C2515 CAP_402	m60[25B6]	C4115 CAP_402	m60[41B5]	C5798 CAP_1210	m60[57D2]		
	C85A0 CAP_402	m60[85D1]	C2516 CAP_P_CASE-C2	m60[25D3]	C4116 CAP_402	m60[41B5]	C5799 CAP_1210	m60[57D3]	
	C600 CAP_402	m60[6C7]	C2517 CAP_402	m60[25D6]	C4117 CAP_402	m60[41B2]	C5800 CAP_402	m60[59B8]	
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	C620 CAP_603	m60[6D6]	C2521 CAP_402	m60[25C3]	C4128 CAP_402	m60[41A8]	C5804 CAP_402	m60[58D2]	
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C	C622 CAP_805	m60[6D7]	C2523 CAP_402	m60[25B4]	C4130 CAP_402	m60[41A7]	C5806 CAP_402	m60[58D1]	
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C924 CAP_805	m60[9A7]	C2815 CAP_402	m60[28B2]	C4501 CAP_402	m60[45D3]	C6600 CAP_603	m60[66D4]		

Table with columns labeled 8, 7, 6, 5, 4, 3, 2, 1. Rows are organized into sections A, B, C, D. Each row contains a reference ID, a part number, and a manufacturer code.

8

7

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5

4

3

2

1

ZH608	MTGHOLE	m60[9D3]
ZH609	MTGHOLE	m60[9D2]
ZH610	MTGHOLE	m60[9D2]

D

D

C

C

B

B

A

A

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