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### Schematic / PCB #’s

<table>
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<th>Reference</th>
<th>Ref</th>
<th>Critical</th>
<th>BOM Option</th>
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<tr>
<td>501-7225</td>
<td>A.0.0</td>
<td>P74</td>
<td>CRITICAL</td>
</tr>
<tr>
<td>239-2101</td>
<td>B</td>
<td>P74</td>
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Approximate System Block Diagram

System Block Diagram

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Core 1.2V Page 14

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2.7 GHz
Core -1.2V Page 14

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Core 1.65 - 1.25V Page 15

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Parallel
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Clocks
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UC500
Clocks
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800/1066 MHz

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Line Out Amp 1
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Codec
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J5810/20/30  ALS SENS
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U5920 Sudden Motion Detect
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Sync Date=08/23/2006

System Block Diagram
## BOM Variants

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>VAR NAME</th>
<th>VAR OPTIONS</th>
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<tr>
<td>630-1225</td>
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<td>630-1226</td>
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<td>630-1228</td>
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## M75 BOM Groups

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>VAR NAME</th>
<th>VAR OPTIONS</th>
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<tbody>
<tr>
<td>78-100001</td>
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<td></td>
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<tr>
<td>78-100002</td>
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## Bar Code Labels / EEE #'s

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>REFERENCE SHEET</th>
<th>CRITICAL</th>
<th>VAR OPTIONS</th>
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<tbody>
<tr>
<td>024-0393</td>
<td>1</td>
<td>U1000 CPU_2_2GHZ</td>
<td>[EEE:X5D]</td>
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<tr>
<td>024-0393</td>
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<td>[EEE:X5E]</td>
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## Module Parts

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<thead>
<tr>
<th>PART NUMBER</th>
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<th>DESCRIPTION</th>
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<th>VAR OPTIONS</th>
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<tr>
<td>122-0268</td>
<td>4</td>
<td>VRAM_128_SAMSUNG</td>
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<td>122-0268</td>
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<td>VRAM_128_HYNIX</td>
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<td>VRAM_128_SAMSUNG</td>
<td>[EEE:XXS]</td>
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## BOM Configuration

<table>
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<tr>
<th>BAR CODE</th>
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<th>M75_COMMON1</th>
<th>M75_COMMON2</th>
<th>M75_DEBUG</th>
<th>M75_PROG</th>
<th>M75_PROG PARTS</th>
<th>M75_DEBUG SMC</th>
<th>M75_DEBUG_NO</th>
<th>XDP</th>
<th>LPCPLUS</th>
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<tr>
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<td>2.4GHZ</td>
<td>2.2GHZ</td>
<td>2.4GHZ</td>
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**www.vinafix.vn**
<table>
<thead>
<tr>
<th>Date</th>
<th>Description</th>
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<tbody>
<tr>
<td>03/06/07</td>
<td>DDR2 Regulator: Changed FB resistors to 0.1% to raise guaranteed lowest output voltage</td>
</tr>
<tr>
<td>03/06/07</td>
<td>Ethernet Connector: Removed RX shorts on Ethernet MDI lines per EMC request</td>
</tr>
<tr>
<td>03/06/07</td>
<td>Power FETs: Changed Q7080 to RJK0301 which provides much lower Rds(on)</td>
</tr>
<tr>
<td>03/01/07</td>
<td>NB GFX Decoupling: Added R2260 (0.3 ohm, 0603) to bring ESR of regulator output cap in spec (rdar://5000272)</td>
</tr>
<tr>
<td>03/01/07</td>
<td>NB GFX Decoupling/Power Aliases: Connected VCCD_CRT of NB to GND per CRT disable guidelines</td>
</tr>
<tr>
<td>02/28/07</td>
<td>NB GFX Core: Changed Vcore controller to ISL6263B (part consolidation effort between Apple/Intersil - rdar://5009109)</td>
</tr>
<tr>
<td>02/28/07</td>
<td>Left Clutch IC: Updated both I-PEX connectors to new APN (part update for shell plating)</td>
</tr>
<tr>
<td>02/19/07</td>
<td>Released post-EVT to document what was built (Schem Rev 12)</td>
</tr>
<tr>
<td>02/19/07</td>
<td>Power Sequencing Rework: Short pins 2 and 4 of U7885 to complete PWROK chain</td>
</tr>
<tr>
<td>02/19/07</td>
<td>Power Sequencing: NO STUFFed U7885 to remove GPU PGOOD from PWROK chain</td>
</tr>
<tr>
<td>01/25/07</td>
<td>Released for EVT (Schem Rev 11, PCB Rev 03)</td>
</tr>
<tr>
<td>01/25/07</td>
<td>BOM: Updated all Intel APNs to use QS parts</td>
</tr>
<tr>
<td>01/25/07</td>
<td>BOM: Changed FB memories to new Samsung and Hynix APNs (also added new BOMOPTIONs to GPU straps)</td>
</tr>
<tr>
<td>01/24/07</td>
<td>BOM: Changed C3860/61 to 22pF from 27 pF based on -R characterization (T9_noME change 41248)</td>
</tr>
<tr>
<td>01/22/07</td>
<td>BOM: Added BOMOPTIONs for SLG2AP101 (primary) and SLG8LP537 (backup)</td>
</tr>
<tr>
<td>01/19/07</td>
<td>GPU FB: Reconnected ODD power FET gate control circuitry to properly implement soft start (added one cap)</td>
</tr>
<tr>
<td>01/19/07</td>
<td>SMBus: Changed R5260 &amp; R5261 from 4.7K to 3.3K</td>
</tr>
<tr>
<td>01/17/07</td>
<td>GPU GPIOs: Added 2 TPs on GPIOs to make G-state externally visible</td>
</tr>
<tr>
<td>01/17/07</td>
<td>Power Sequencing: Changed power rail for U7850 to PP3V3_S5 to eliminate a leakage path</td>
</tr>
<tr>
<td>01/17/07</td>
<td>Power Sequencing: Added C7859 to create RC delay for 1.5 and 1.05V S0 rails</td>
</tr>
<tr>
<td>01/16/07</td>
<td>Power Aliases: Deleted alias that accidentally eliminated filtering on PP1V5_S0_SB_VCC1_5_B</td>
</tr>
<tr>
<td>01/17/07</td>
<td>Testpoints: Removed FUNC_TEST from NB_RESET_L and FSB_DPWR_L per PCB request</td>
</tr>
<tr>
<td>01/17/07</td>
<td>Sync with T9 noME (6.1.4) to pull in WOL_EN and Wake-on-Wireless support</td>
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<tr>
<td>01/16/07</td>
<td>Power FETs: Changed R7097 to 220K to maintain EnergyStar compliance with FET gate pulled to PBUS</td>
</tr>
<tr>
<td>01/16/07</td>
<td>Power FETs: Changed Q7095 to FDM6296 and pulled up to PBUS for better PP1V25_S0 FET Rds(on)</td>
</tr>
<tr>
<td>01/15/07</td>
<td>Power Sequencing: NO STUFFED U7858 and stuffed R7860 to allow SMC to drive 05 pin directly</td>
</tr>
<tr>
<td>01/13/07</td>
<td>Released for DVT (As-Built)</td>
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<tr>
<td>01/12/07</td>
<td>GPU Misc: Added RD375-87 to implement PCI HBRD 4474 in hardware</td>
</tr>
<tr>
<td>01/12/07</td>
<td>Power FETs: Changed Q7062 to FDM294 and pulled up to PBUS for better PP1V25_S0 FET Rds(on)</td>
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<td>01/11/07</td>
<td>Modules: Updated Intel chipset to PB2 parts</td>
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<tr>
<td>01/08/07</td>
<td>Power Sequencing: Changed T9076 to 26V to maintain EnergyStar compliance with FET gate pulled to PBUS</td>
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<tr>
<td>01/08/07</td>
<td>Power Sequencing: Changed T9076 to 16V for proper rating of parts tied to PBUS</td>
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<tr>
<td>01/07/07</td>
<td>Power Sequencing: NO STUFFED T9076 to maintain a dummy bus (rdar://5056900)</td>
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<tr>
<td>01/06/07</td>
<td>No changes. Weekly BOM release</td>
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<tr>
<td>01/06/07</td>
<td>USB Decoupling: Changed L2700 from 150uH to 15uH for smaller footprint to simplify layout targets</td>
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<tr>
<td>01/04/07</td>
<td>Released for DVT</td>
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<tr>
<td>01/03/07</td>
<td>Power Sequencing: Changed T9051 to 2.0mH to save 0.55A to meet 55 W limit on S5</td>
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<tr>
<td>12/29/06</td>
<td>Released for Proto (Schem Rev 08, PCB Rev 01)</td>
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<tr>
<td>12/29/06</td>
<td>See Perforce change notes for updates before Proto Release</td>
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<tr>
<td>12/22/06</td>
<td>GPU Misc: Changed Q5500 to 3.3V for S5 power management</td>
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<tr>
<td>12/22/06</td>
<td>Power Sequencing: Changed FB clock termination to 242 ohms (2x121) per Nvidia PUN</td>
</tr>
<tr>
<td>12/22/06</td>
<td>Clocks: Changed series termination on all single ended clocks to 12K for lower frequency</td>
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**Note:** This is a partial listing of changes for the document. For a complete list, refer to the full document or the revision history section.
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APPLE COMPUTER INC.

Digital Ground

Signal Aliases

Board Holes

(Don’t be PTH)

Frame Holes

(Don’t be PTH)

Notches

(Don’t be PTH)

Thermal Module Holes

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PLACEMENT NOTE: Place R1024 near ITP connector (if present)

LAYOUT NOTE:
- COMP0,2 connect with ZO=27.4ohm
- COMP1,3 connect with ZO=55ohm
- MARK TRACK LENGTH SHORTER THAN 0.1" TO AVOID TRACK LENGTH SHORTER THAN 0.1"

 примечание местоположения: поместите R1024 рядом с соединителем ITP (если он есть)

заметка о размещении:
- COMP0,2 подключите с ZO=27.4ом
- COMP1,3 подключите с ZO=55ом
- УЧТИТЕ: НЕ ЗАКАРМЫВАЙТЕ ТРАКТ ДЛИНОЙ БОЛЕЕ 0.1", ЧТОБЫ избежать трассы длиной менее 0.1"
CPU Decoupling & VID

CPU VCCORE HF AND BULK DECOUPLING
- 1x 330uF, 20x 22uF 0805
- CRITICAL

CPU VCCORE VID CONNECTIONS
- CRITICAL

VCCP (CPU I/O) DECOUPLING
- CRITICAL

VCCA (CPU AVdd) DECOUPLING
- CRITICAL

PLACEMENT NOTE=Place near CPU pin B26.

PLACEMENT NOTE=Place in CPU center cavity.

CRITICAL

PLACEMENT NOTE=Place in CPU center cavity.

CRITICAL

CRITICAL

10%
Mini-XDP Connector

NOTE: This is not the standard XDP pinout. Use with 920-0451 adapter board to support CPU, NB & SM debugging.

Direction of XDP module

Please avoid any obstructions on even-numbered side of J1300.
Leave GFX_VID<3..0> and GFX_VR_EN as NC.

Tie VCC_AXG and VCC_AXG_NCTF to GND.

Tie VCCA_DPLLA and VCCA_DPLLB to VCC (VCore).

Tie DPLL_REF_CLK* and DPLL_REF_SSCLK* to VCC (VCore).

Tie DPLL_REF_CLK and DPLL_REF_SSCLK to GND.

TV_DCONSELx to GND.

NOTE: Must keep VDDC_TVDAC powered VCCD_CRT, VCCD_QDAC and VCC_SYNC.

VCCA_CRT_DAC, VCCA_DAC_BG, VCCA_TVx_DAC,

Can tie the following rails to GND:

Tie TVx_DAC, TVx_RTN, R/R#/G/G#/B/B#, HSYNC,

All CRT/TVDAC rails must be powered. All TVDC DAC rails. VCCA_TVx_DAC and VCCA_DAC_BG can

Tie TVx_DAC and TVx_RTN to GND. Must power all TV-Out Disable / CRT Enable

Unused DAC outputs must remain powered, but can

TV-Out Disable / CRT Enable

Tie TVilinx TVO REF to GND. Must power all

VCC DAC files. VCCA TVO DAC and VCCA DAC_BG can share filtering with VCCA CRT DAC.

CRT Enable / TV-Out Enable

Tie VD/0/V0/0/0/0 to GND. HDVC and VYFMC to GND. All CRT/TVDAC rails must be powered. All

CRT & TV-Out Disable

rails must be filtered except for VCCA CRT.

CRT & TV-Out Disable

Tie TVistine TVO REF file/5/0/5 to GND. CRT

VYFMC and CRT TVO REF to GND.

Can tie the following rails to GND:

VCC CRT, VCCA CRT DAC and VCCA CRT_VCC.

Note: Must keep VDDC_TVDAC powered and filtered at all times!

Internal Graphics Disable

Power instructions for TVDVC and CRT & TV-Out Enable above.

Can also tie CRT TVO_DEC, L_CTRL, L_DEC, CRT TVO CTRL, and

TV SVC SIGNALS to GND.

L_CTRL, L_DEC, CRT TVO CTRL, CRT TVO DEC to GND.

Tie DPLL REF_CLK and DPLL REF SSCLK to VCC (VCore).

Tie VCCA_DAC and VCCA_DAC_BG to VCC (VCore).

Tie VCC AXG and VCC AXG NCTF to GND.

Tie VDDC_TVDAC and VDDC_TVDAC_N as NC.

TV_OUT_DISABLE

Tie VCC AXG and VCC AXG NCTF to GND.

Tie VCCA_DPLLA and VCCA_DPLLB to VCC (VCore).

Tie DPLL_REF_CLK and DPLL_REF_SSCLK to GND.

TV_DCONSELx to GND.

NOTE: Must keep VDDC_TVDAC powered VCCD_CRT, VCCD_QDAC and VCC_SYNC.

VCCA_CRT_DAC, VCCA_DAC_BG, VCCA_TVx_DAC,
Current numbers from Crestline EDS, doc #21749.

2700 mA (2 ch, 533MHz)
3300 mA (2 ch, 667MHz)

HCTF balls are Not Critical To Function
These connections can break without impacting part performance.

NB Power 1

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Current numbers from Crestline EDS, doc #21749.
Current numbers from Crestline EDS, doc #21749.

- 550 mA (533MHz DDR)
- 640 mA (667MHz DDR)
- 0.4 mA
- 150 mA
- 100 mA
- 22

S0 or S3M is acceptable

PP3V3_S0_NB_VCCA_TVDACA = PP1V8_S0_NB_VCCD_LVDS = PP1V25_S0M_NB_VCCD_HPLL = PP1V5_S0_NB_VCCD_QDAC = PP1V5_S0_NB_VCCD_TVDAC = PP1V5_S0_NB_VCCD_CRT = PP3V3_S0_NB_VCCA_TVDACB = PP1V25_S0M_NB_VCCA_SM_CK = PP1V25_S0M_NB_VCCA_SM = PP1V25_S0M_NB_VCCA_PEG_PLL = GND_NB_VSSA_PEG_BG = PP3V3_S0_NB_VCCA_PEG_BG = GND_NB_VSSA_LVDS = PP1V8_S0_NB_VCCTXLVDS = PP1V25_S0M_NB_VCCA_MPLL = PP1V25_S0M_NB_VCCA_HPLL = PP1V25_S0_NB_VCCA_DPLLB = PP1V25_S0_NB_VCCA_DPLLA = GND_NB_VSSA_DAC_BG = PP3V3_S0_NB_VCCA_DAC_BG = PP3V3_S0_NB_VCCA_CRTDAC = PP3V3_S0_NB_VCCSYNC.

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SYNC_MASTER=T9_NOME
SYNC_DATE=03/16/2007

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NB Power 2

SCALE

SIZE

DRAWING NUMBER

OFSHT 12345678

REV. A.0.0051-7225
Crestline Thermal Diode Pins

Mainly for investigation. If not used, alias these nets directly to GND.

NOTE: TDB = _N

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SCALE

SIZE

A.0.0051-7225

www.vinafix.vn
RTC Power Sources

Platform Reset Connections
Unbuffered

SB RTC Crystal

System Reset "Button"

VRMPWRGD Inverter

PWROK Circuit

CPU VCore ForcePSI

Platform Reset Connections
Unbuffered

SB Misc

Coin-Cell Connector

NOTE: R2809 and R2885 form the double-fault protection for RTC battery.

VCORE

INPUT

OUTPUT

INPUT

OUTPUT

INPUT

OUTPUT

INPUT

OUTPUT
One cap for each side of every RPAK, one cap for every two discrete resistors

Ensure CL and CMT resistors are close to SO-DIMM connector
ENET Enable Generation

3.3V ENET FET

WLAN Enable Generation

Yukon AVDDL LDO

Yukon Crystal

Yukon Power Control
Strap via alias on port page.

Lo: Beta Mode enable (1394b).

Multi-port Portable systems are Power Class 4 ('100').

Power Class:

8

=PP3V3_FW_PHY

=FWPHY_DS1

=FWPHY_DS0

=PPVP_FW_CPS

=FWPHY_PC0

=FWPHY_BMODE

VOLTAGE=3.3V

VOLTAGE=1.95V

MIN_NECK_WIDTH=0.22 mm

VOLTAGE=1.86V

MIN_NECK_WIDTH=0.22 mm

VOLTAGE=1.86V

SYNC_MASTER=M76_MLB

SYNC_DATE=03/19/2007

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SCALE

DRAWING NUMBER

A

B

C

D

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Current Limit/Active Late-VG Protection

Late-VG Event Detection

Enables port power when machine is running or on AC.

Current Limits:
0.033 ohm => 1.5A
0.030 ohm => 1.66A (Ideal)
0.020 ohm => 2.4A

MAX5944 current limiter trips if integrator (counter) reaches it. A new sample (taken every 0.1s) is weighted as 1 if over the limit (at any point during the period) and 0.8 if below the limit. As a result, the decision tends to trip easily on devices that produce periodic current spikes. Current limit has been set higher to compensate.

FireWire Port Power

---

**Page Notes**

- **Signal aliases required by this page:**
  - =PP3V3_FW_LATEVG_ACTIVE

- **Page Notes**

---
FireWire PHY Design Guide (FWDG 0.6, 5/14/03)

Termination

FireWire TPA/TPB pairs to their constrained on this page. It is

NOTE: This page is expected to contain Signal aliases required by this page:

- =GND_CHASSIS_FW_PORT0L
- =PP3V3_FW_LATEVG
- =PPVP_FW_PORT1
- =PPVP_FW_PORT0

Page Notes

R4390 should be 390 Ohms max for a 3.3V rail and should be biased to 2.4V for margin to at least 2.1V for FW signal integrity

Late-VG Protection Power

PPDVF,PPDVF needs to be biased.

FFW,FFW needs to be biased 2.4V for 3.3V signal integrity and should be biased to 2.4V for margin. R4390 should be 390 Ohms and for a 3.3V rail

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Port Power Switch

Right USB Port

USB/SMC Debug Mux

External USB Connector
NOTE: Unused pins have "(OC)" name. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.
LPC+ Connector

FWH_INIT_L Generation

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1/16W 5%

PLACEMENT_NOTE=Place R5190 to minimize CPU_INIT_L stub

PLACEMENT_NOTE=Place Q5190 close to R5190

SYNC_DATE=03/19/2007

SYNC_MASTER=M76_MLB
ICH8-M SMBus Connections

- SMB_ME_DATA
- SMB_ME_CLK

SMC "0" SMBus Connections

- SMB_MGMT_CLK
- SMB_MGMT_SDA

SMC "A" SMBus Connections

- SMB_0_S0_CLK
- SMB_0_S0_DATA

SMC "B" SMBus Connections

- SMB_A_S3_DATA
- SMB_A_S3_CLK

SMC "Battery A" SMBus Connections

- SMB_B_S0_CLK
- SMB_B_S0_DATA

SMC "Management" SMBus Connections

- SMB_A_S3_CLK
- SMB_A_S3_DATA

Clock Chip

- (Address determined by ARP)

Left I/O SMBus Connections:

- (MASTER)

Left I/O Board

- (See Table)

SMC SMBus Connections

- CPU Temp (Int)
- CPU Temp (Ext)

ExpressCard Slot

- Address determined by AMP
Left ALS Filter

Left ALS circuit has 1K series-R

Right ALS Circuit

RTALS_GAIN_L and RTALS_PHOTODIODE need to be matched

Keyboard LED Driver

RTALS_OP_IN and RTALS_OP_COMP need to be matched

ALS Support

SYNC_MASTER=M76_MLB  SYNC_DATE=03/19/2007

KLDM.sys_KBDLED KBDLED_ANODE

SMC_SYS_KBDLED KBDLED_SW

www.vinafix.vn
I2C addresses:
Address low = 0x30, 0x31
Address high = 0x32, 0x33
Alias SCL/SDA to GND if using analog outputs only

Desired orientation when placed on board top-side:
Package Top

Desired orientation when placed on board bottom-side:
Top-through View

Sudden Motion Sensor (SMS)
SYNC_MASTER=M76_MLB
SYNC_DATE=03/19/2007
SMS_ONOFF_L
SMS_Z_AXIS
SMS_Y_AXIS
SMS_X_AXIS

APN: 33850354

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TPS51120 LDO/Buffer outputs

*Vout = 5.0V*

8A max output

50mA max load when EN5 & EN3 high

100mA max load when EN5 high

NOTE: EN5 can float or tie to VIN for automatic 5V LDO mode
EN5 can float or tie to VIN for automatic 3.3V LDO mode
When both are low TPS51120 VIN current drops from 100-150uA to 10-20uA.
3.3V FW PHY Supply

Backup power in case of FW bus.
VP short to keep PHY powered.

Vout = 3.316V
200mA max output (Switcher limit)

1.95V FW PHY Supply

Vout = 1.25V * (1 + Ra / Rb)
3.425V "G3Hot" Supply

Supply needs to guarantee 3.3V delivered to SMC VRef generator

Vout = 1.25V + (1 + Ra / Rb)

Unused PGOOD Signals

Other S0 Rails PWRGD Circuit

Does not include GFX rails

NOTE: 0.9V/2.5V is not checked!

Other S0 Rails PWRGD Circuit

Does not include HP rails
**Left ALS Connector**

White colored version of 5180369

**SATA HDD & IR & SIL Flex Connector**

NOTE: SATA _UF_ nets cross DDR2 signals and pick up significant noise. Common-mode chokes are to remove this noise from SATA signals.
### FSB (Front-Side Bus) Constraints

<table>
<thead>
<tr>
<th>Constraint Type</th>
<th>Layer Min.</th>
<th>Neck Width</th>
<th>Max. Length</th>
<th>Diff. Pair Phys. Rule Set</th>
</tr>
</thead>
<tbody>
<tr>
<td>FSB Common</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CPU/27P4S</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CPU/55S</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DSTB</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

All FSB signals with impedance requirements are 55-ohm single-ended.
- Worst-case spacing is 2:1 within FSB bus, 3:1 spacing to other sections.
- A single-ended FSB signal is a signal added to an existing FSB driver.
- FSB complementary pairs are spaced 1:1 and routed as differential pairs.
- Design Guide recommends most signal pairs be routed on the same layer.
- Design Guide recommends FSB signals be routed only on internal layers.

**Note:** Design Guide does not indicate FSB spacing to other signals, assumed 3:1.

**Source:** Santa Rosa Platform DD, Rev 0.9 (#20517), Sections 4.2.4.2

### CPU Signal Constraints

<table>
<thead>
<tr>
<th>Constraint Type</th>
<th>Layer Min.</th>
<th>Neck Width</th>
<th>Max. Length</th>
<th>Diff. Pair Phys. Rule Set</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU/27P4S</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CPU/55S</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CPU/2TO1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- Worst CPU signals with impedance requirements are 55-ohm single-ended.
- Some signals require 27.4-ohm single-ended impedance.

**Source:** Santa Rosa Platform DD, Rev 0.9 (#20517), Sections 4.2.4.2

### CPU / FSB Net Properties

<table>
<thead>
<tr>
<th>Net</th>
<th>Min. Size</th>
<th>Max. Size</th>
<th>Min. Size</th>
<th>Max. Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>FSB Addr</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FSB Data</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Intel says to route with 7 mil spacing without specifying a target differential impedance.

**Source:** Santa Rosa Platform DD, Rev 0.9 (#20517), Sections 4.2.4.2

### CPU/FSB Constraints

**Source:** Santa Rosa Platform DD, Rev 0.9 (#20517), Sections 4.2.4.2
CRT_HSYNC/CRT_VSYNC signals are 55-ohm +/- 15% single-ended impedence.
- 55-ohm +/- 15% from second termination resistor to connector.
- 50-ohm +/- 15% from first to second termination resistor.
- 37.5-ohm +/- 15% from GMCH to first termination resistor.

CRT & TVDAC signal single-ended impedence varies by location:

LVDS signals are 100-ohm +/- 20% differential impedence.

Video Signal Constraints

Source: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 7.2, 9.2 & 10.5
### Table

<table>
<thead>
<tr>
<th>AREA_TYPE</th>
<th>SPACING_RULE_SET</th>
<th>NET_SPACING_TYPE1</th>
<th>NET_SPACING_TYPE2</th>
</tr>
</thead>
<tbody>
<tr>
<td>MEM_CTRL</td>
<td>MEM_CTRL2MEM</td>
<td>MEM_DATA2DATA</td>
<td>1.5:1_SPACING</td>
</tr>
<tr>
<td>MEM_DATA</td>
<td>MEM_MAND2MEM</td>
<td>MEM_CLK2MEM</td>
<td>3:1_SPACING</td>
</tr>
<tr>
<td>MEM_DATA</td>
<td>MEM_CMD2MEM</td>
<td>MEM_CTRL2MEM</td>
<td>3:1_SPACING</td>
</tr>
<tr>
<td>MEM_DATA</td>
<td>MEM_CTRL2MEM</td>
<td>MEM_DATA2MEM</td>
<td>3:1_SPACING</td>
</tr>
</tbody>
</table>

### Diagram

- **Memory Bus Constellations**
- **Memory Net Properties**
- **Table Physical Rules**
- **Table Spacing Assignment**
- **Table Spacing Rules**

### Source

Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

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Internal Interface Constraints

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 10.13.2

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.9.1

HD Audio Interface Constraints

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.7 & 10.9

USB 2.0 Interface Constraints

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 10.12.2

Internal Interface Constraints

SOURCE: Santa Platform DG, Rev 1.0 (#21112), Section 10.17

**SCALE**

**SIZE**

**DRAWING NUMBER**
### Video Signal Constraints

<table>
<thead>
<tr>
<th>Feature</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><em>GDDR3_CMD</em></td>
<td>2.5:1_SPACING</td>
</tr>
<tr>
<td><em>VGA_SYNC</em></td>
<td>TMDS</td>
</tr>
</tbody>
</table>

### GDDR3 Frame Buffer Signal Constraints

<table>
<thead>
<tr>
<th>Feature</th>
<th>Measurement</th>
</tr>
</thead>
<tbody>
<tr>
<td><em>GDDR3_80D</em></td>
<td>80_OHM_DIFF</td>
</tr>
<tr>
<td><em>20_MIL</em></td>
<td>20_MIL</td>
</tr>
<tr>
<td><em>50_OHM_SE</em></td>
<td>50_OHM_SE</td>
</tr>
<tr>
<td><em>100_OHM_DIFF</em></td>
<td>100_OHM_DIFF</td>
</tr>
<tr>
<td><em>STANDARD</em></td>
<td>12.7_MM</td>
</tr>
<tr>
<td><em>GDDR3_40R50SE</em></td>
<td>40_OHM_SE</td>
</tr>
<tr>
<td><em>GDDR3_50SE</em></td>
<td>50_OHM_SE</td>
</tr>
<tr>
<td><em>GDDR3_FB</em></td>
<td>GDDR3_FB</td>
</tr>
</tbody>
</table>

### GDDR3 Net Properties

<table>
<thead>
<tr>
<th>Feature</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><em>FB_AB_CMD</em></td>
<td>GDDR3_FB</td>
</tr>
<tr>
<td><em>FB_B_RDQS1</em></td>
<td>GDDR3_FB</td>
</tr>
<tr>
<td><em>FB_B_RDQS0</em></td>
<td>GDDR3_FB</td>
</tr>
<tr>
<td><em>FB_B_WDQS3</em></td>
<td>GDDR3_FB</td>
</tr>
<tr>
<td><em>FB_A_RDQS0</em></td>
<td>GDDR3_FB</td>
</tr>
<tr>
<td><em>FB_A_WDQS3</em></td>
<td>GDDR3_FB</td>
</tr>
<tr>
<td><em>FB_A_CS0_L</em></td>
<td>GDDR3_FB</td>
</tr>
<tr>
<td><em>FB_A_CLK_P</em></td>
<td>GDDR3_FB</td>
</tr>
<tr>
<td><em>FB_B_CLK_P</em></td>
<td>GDDR3_FB</td>
</tr>
<tr>
<td><em>VGA_B_TV_COMP</em></td>
<td>GDDR3_FB</td>
</tr>
<tr>
<td><em>VGA_SYNC</em></td>
<td>GDDR3_FB</td>
</tr>
</tbody>
</table>

### GPU (G84M) Constraints

<table>
<thead>
<tr>
<th>Feature</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><em>GDDR3_FB</em></td>
<td>GDDR3_FB</td>
</tr>
<tr>
<td><em>GDDR3_FB_AB</em></td>
<td>GDDR3_FB</td>
</tr>
<tr>
<td><em>GDDR3_FB_B</em></td>
<td>GDDR3_FB</td>
</tr>
<tr>
<td><em>GDDR3_FB_C</em></td>
<td>GDDR3_FB</td>
</tr>
<tr>
<td><em>GDDR3_FB_D</em></td>
<td>GDDR3_FB</td>
</tr>
</tbody>
</table>

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**Scale: O/FSHT**

**Drawing Number: D 051-1235 A-0-0**
### Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for GNRN fanout.

<table>
<thead>
<tr>
<th>Layer</th>
<th>Minimum Neck Width</th>
<th>Maximum Neck Length</th>
<th>Diffpair Primary Gap</th>
<th>Diffpair Neck Gap</th>
</tr>
</thead>
<tbody>
<tr>
<td>PP1V8_MEM</td>
<td>&gt;0.20 MM</td>
<td>&gt;0.25 MM</td>
<td>&gt;0.25 MM</td>
<td>&gt;0.25 MM</td>
</tr>
</tbody>
</table>

Allow 0.1 mm necks for >0.1 mm lines between thru-hole SO-DIMM pins.

### Graphics Constraint Relaxations

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

<table>
<thead>
<tr>
<th>Layer</th>
<th>Minimum Neck Width</th>
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</table>

### SIM Card Constraints

<table>
<thead>
<tr>
<th>Layer</th>
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