1. All resistance values are in ohms, 0.1 watt +/- 5%.
2. All capacitance values are in microfarads.
3. All crystal & oscillator values are in micro-seconds.

**SCHEM, MBP 15" MLB**

12/07/2007

**Schematic / PCB #’s**

<table>
<thead>
<tr>
<th>Reference</th>
<th>Critical</th>
<th>Drawn On</th>
</tr>
</thead>
<tbody>
<tr>
<td>051-7413</td>
<td>1</td>
<td>SCHEM, TAUPO, M87</td>
</tr>
<tr>
<td>320-2249</td>
<td>1</td>
<td>FMP, TAUPO, M87</td>
</tr>
</tbody>
</table>

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**Sync**

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- LPC+ Debug Connector
- SMBus Connections
- Current & Voltage Sensing
- Current Sensing
- Thermal Sensing History
- Fan Connectors
- ALS Support
- Sudden Motion Sensor (SMS)
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- Power FETs
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- 5V / 1.3V Power Supply
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- NV G84M Core/FP Power
- NV G84M Frame Buffer 1/7
- GDDR3 Frame Buffer A (Top)
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- NV G84M GPID/MIO/Gpio
- GPU Straps
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- GPU (G84M) Core Supply
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- DVI Display Connector
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- NB Constraints
- Memory Constraints
- 3B Constraints (1st of 2)
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- GPU (G84M) Constraints
- Project Specific Constraints
- PCB Rule Definitions

**Metric**

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Power Block Diagram
### BOM Variants

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>M87 BOM Options</th>
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</thead>
<tbody>
<tr>
<td>630-9286</td>
<td>M87_PROGPARTS</td>
</tr>
<tr>
<td>630-9238</td>
<td>M87_COMMON</td>
</tr>
<tr>
<td>630-9213</td>
<td>M87_DEBUG</td>
</tr>
<tr>
<td>630-9091</td>
<td>M87_COMMON</td>
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</table>

### M87 BOM Groups

<table>
<thead>
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<th>PART NUMBER</th>
<th>M87 BOM Options</th>
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<td>826-4393</td>
<td>M87_COMMON</td>
</tr>
<tr>
<td>826-4393</td>
<td>M87_COMMON</td>
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</tbody>
</table>

### Bar Code Labels / EEE #’s

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>BOM 1</td>
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</table>

### Module Parts

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
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### Functional / ICT Test

**Sync Master**
- (MASTER)

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---

### Functional Test Points

#### Fan Connectors

- **FUNCTION TEST**
  - PM_1V8P1V5P1V05S0_PGOOD
  - NB_RESET_L
  - IMVP6_VID<6..0>
  - IMVP_VR_ON
  - USB_CAMERA_P
  - PM_S4_STATE_L
  - PM_SLP_S3_L

#### Battery Digital Connector

- **FUNCTION TEST**
  - CPU_GB_BBPL L
  - CPU_BBPL L
  - CPU_BBPL L
  - CPU_BBPL L
  - CPU_BBPL L
  - CPU_BBPL L
  - CPU_BBPL L
  - CPU_BBPL L

#### LPC+ Debug Connector

- **FUNCTION TEST**
  - SB_RTC_RST_L
  - LTALS_OUT
  - CPUTHMSNS_D2_N
  - RSFSTHMSNS_D_N
  - SMC_TX_L
  - LINDACARD_GPIO
  - LSI_PCP_LBLE
  - LSP_PCP_LBLE
  - LSI_PCP_LB
  - LSP_PCP_LB
  - LSI_CPR_LBLE
  - LSP_CPR_LBLE
  - LSI_CPR_LB
  - LSP_CPR_LB
  - LSI_PCP_L
  - LSP_PCP_L
  - LSI_CPR_L
  - LSP_CPR_L
  - LSI_PCP
  - LSP_PCP
  - LSI_CPR
  - LSP_CPR
  - LSI_THERMTHL
  - LSP_THERMTHL

#### Left I/O Power Connector

- **FUNCTION TEST**
  - VR_PWRGOOD_DELAY
  - NB_SB_SYNC_L
  - FSB_CPUSLP_L
  - SB_RTC_RST_L
  - HSTHMSNS_D_N
  - SMC_TDO
  - SMC_TRST_L
  - SMC_BS_ALRT_L
  - FWH_INIT_L
  - HSTHMSNS_D_N
  - LINDACARD_GPIO
  - SMC_TX_L
  - PM_SLP_S3_L
  - CPU_DPSLP_L
  - CURRENT_CAL B
  - PM_CLKRUN_L
  - LPC_FRAME_L
  - DEBUG_RESET_L

#### RTC Battery Connector

- **FUNCTION TEST**
  - CURRENT CAL B
  - CURRENT CAL B
  - CURRENT CAL B
  - CURRENT CAL B

#### Left ALS Connector

- **FUNCTION TEST**
  - PM_STPCPU_L
  - PM_RSMRST_L
  - PM_STPCPU_L

#### Thermal Diode Connectors

- **FUNCTION TEST**
  - IMVP6_VID<6..0>
  - IMVP_VR_ON
  - USB_CAMERA_P
  - PM_S4_STATE_L
  - PM_SLP_S3_L

**OTHER FUNCTION TESTS**

#### System Validation TPs

- **FUNCTION TEST**
  - CPU_PCP_L
  - CPU_CPR_L
  - CPU_PCP_L
  - CPU_CPR_L
  - CPU_PCP_L
  - CPU_CPR_L
  - CPU_PCP_L
  - CPU_CPR_L
  - CPU_PCP_L
  - CPU_CPR_L

---

### ICT Test Points

#### CPU FSB NO_TESTS

- **FUNCTION TEST**
  - CPU_GB_BBPL L
  - CPU_GB_BBPL L
  - CPU_GB_BBPL L
  - CPU_GB_BBPL L
  - CPU_GB_BBPL L
  - CPU_GB_BBPL L
  - CPU_GB_BBPL L
  - CPU_GB_BBPL L

#### NB NO_TESTS

- **FUNCTION TEST**
  - CPU_GB_BBPL L
  - CPU_GB_BBPL L
  - CPU_GB_BBPL L
  - CPU_GB_BBPL L
  - CPU_GB_BBPL L
  - CPU_GB_BBPL L
  - CPU_GB_BBPL L
  - CPU_GB_BBPL L

---

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## CPU Power & Ground

**Standard Voltage:**
- 41.0 A (HPM)
- 30.0 A (HPM)
- 25.5 A (SuperLPM)
- 27.3 A (Auto-Halt/Stop-Grant HPM)
- 17.9 A (Auto-Halt/Stop-Grant SuperLPM)
- 16.3 A (Sleep/HPM)
- 16.1 A (Sleep SuperLPM)
- 15.4 A (Sleep Super Deep Sleep)
- 13.0 A (Sleep HFM)
- 11.5 A (Sleep Ultra Deep Sleep)
- 9.6 A (Enhanced Deeper Sleep)

**Low Voltage:**
- 21.0 A (HPM)
- 18.7 A (LPM)
- TBD A (Auto-Halt/Stop-Grant HPM)
- TBD A (Auto-Halt/Stop-Grant LPM)
- TBD A (Sleep/HPM)
- TBD A (Sleep LPM)
- TBD A (Sleep SuperLPM)
- TBD A (Sleep Super Deep Sleep)
- TBD A (Sleep HFM)
- TBD A (Sleep Ultra Deep Sleep)
- TBD A (Sleep Ultra Deep Sleep)
- TBD A (Sleep HFM)

**Ultra Low Voltage:**
- TBD A (Ultra Deep Sleep)
- TBD A (Deep Sleep SuperLFM)
- TBD A (Deep Sleep SuperLFM)
- TBD A (Deep Sleep SuperLFM)
- TBD A (Deep Sleep SuperLFM)
- TBD A (Deep Sleep SuperLFM)
- TBD A (Deep Sleep SuperLFM)
- TBD A (Deep Sleep SuperLFM)
- TBD A (Deep Sleep SuperLFM)
- TBD A (Deep Sleep SuperLFM)

**CPU Power:**
- 25.5 A (Design Target)
- 30.4 A (LPM)
- 41.0 A (HFM)
- 44.0 A (Design Target)

**CPU Core Power & Ground**

<table>
<thead>
<tr>
<th>Condition</th>
<th>Current (A)</th>
</tr>
</thead>
<tbody>
<tr>
<td>4000 mA (before VCC stable)</td>
<td>130 A</td>
</tr>
<tr>
<td>2000 mA (after VCC stable)</td>
<td></td>
</tr>
</tbody>
</table>

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TBD = To Be Determined

---

Current numbers from Memo for Santa Rosa EMTS, doc #22221.

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Mini-XDP Connector

NOTE: This is not the standard XDP pinout.
Use with 920-0451 adapter board to support CPU, NB & SB debugging.

Direction of XDP module
Please avoid any obstructions on even-numbered side of J1300
Tie VCC_AXG and VCC_AXG_NCTF to GND.

Tie VCCA_DPLLA and VCCA_DPLLB to VCC (VCore).

Tie DPLL_REF_CLK* and DPLL_REF_SSCLK* to VCC (VCore).

Tie DPLL_REF_CLK and DPLL_REF_SSCLK to GND.

TV_DCONSELx to GND.

Internal Graphics Disable
VCCD_CRT, VCCD_QDAC and VCC_SYNC.

VCCA_CRT_DAC, VCCA_DAC_BAD, VCCA_TVx_DAC,
Can tie the following rails to GND:
CRT & TV-Out Disable
CRT Disable / TV-Out Enable
share filtering with VCCA_CRT_DAC.

TV-Out Disable / CRT Enable
omit filtering components. Unused DAC outputs
Unused DAC outputs must remain powered, but can
S-Video: DACB & DACC only
recommendation is to float both signals, see Radar #5067636.
be glitch during wake-up on LVDS DATA/CLE pairs. New
decoupling. Otherwise, tie VCCD_LVDS to GND also.
Can leave all signals NC if LVDS is not implemented.

Note: SR SR says to tie LVDS_VREFP/L to GND. This causes a

Tie VCCA_AXG and VCCA_AXG_NCTF to GND.

Tie VCCA_DPLLA and VCCA_DPLLB to VCC (VCore).

Tie DPLL_REF_CLK* and DPLL_REF_SSCLK* to VCC (VCore).

Tie DPLL_REF_CLK and DPLL_REF_SSCLK to GND.

TV_DCONSELx to GND.

Internal Graphics Disable
VCCD_CRT, VCCD_QDAC and VCC_SYNC.

VCCA_CRT_DAC, VCCA_DAC_BAD, VCCA_TVx_DAC,
Can tie the following rails to GND:
CRT & TV-Out Disable
CRT Disable / TV-Out Enable
share filtering with VCCA_CRT_DAC.

TV-Out Disable / CRT Enable
omit filtering components. Unused DAC outputs
Unused DAC outputs must remain powered, but can
S-Video: DACB & DACC only
recommendation is to float both signals, see Radar #5067636.
be glitch during wake-up on LVDS DATA/CLE pairs. New
decoupling. Otherwise, tie VCCD_LVDS to GND also.
Can leave all signals NC if LVDS is not implemented.
Current numbers from Crestline EDS, doc #21749.

**Power Connections**

- **18 mA (standby)**
- **1700 mA (1 ch, 667MHz)**
- **1310 mA (Ext Graphics)**

These connections can break without impacting part performance.
Crestline Thermal Diode Pins

Mainly for investigation. If not used, tie these nets directly to GND.

NOTE: TDB = _NB_TDB_SENSE

NOTE: TDE = _NB_TDE_FORCE

VSS

NB Grounds

APPLE INC.
NOTE: This filter is required even if using only external graphics. VCCD_TVDAC also powers internal thermal sensors.

Current numbers from Crestline EDS Addendum, doc #20127.
One cap for each side of every SRAK, one cap for every two discrete resistors

Ensure CS_L and ODT resistors are close to SO-DIMM connector
To support Yukon EC and Ultra on the same board:

- Pin 42 should be NC (or TP) net.
- yukon EC: Add 1x 0.1uF & 1x 0.001uF caps
- yukon Ultra: Add 1x 0.001uF cap
- ENET_MDI3, ENET_MDI2, ENET_MDI1, ENET_MDI0
- Must be high in S0 state (can use PP3V3_S0 as input)
- ENET_RESET_L
- PCIE_WAKE_L
- PCIE_ENET_R2D_C_P
- PCIE_ENET_D2R_N
- ENET_MDI_P<2>
- ENET_MDI_N<0>
- ENET_CLK_REQ_L (NC/TP for yukon EC)
- ENET_VMAIN_AVLBL

Signal aliases required by this page:
- =YUKON_EC_PP2V5_ENET
- =PP1V8R2V5_ENET_PHY
- =PP3V3_ENET_PHY

- Connect =ENET_CLKREQ_L to clock generator via 0-ohm resistor (BOM_OPTION: YUKON_ULTRA)

- =ENET_MDI_P<2>
- =ENET_MDI_N<0>
- =ENET_RESET_L
- =PCIE_WAKE_L
- =PCIE_ENET_R2D_C_P
- =PCIE_ENET_D2R_N

---

**Yukon Ultra schematic support.**

- No link: 82 mA
- 100 Mbps: 4 mA
- 10 Mbps: 70 mA
- 1000 Mbps: 426 mA
- No link: 4 mA
- 10 Mbps: 130 mA
- 100 Mbps: 150 mA
- 1000 Mbps: 290 mA
- No link: 130 mA

---

**ETH_RLD蜅ayout.**

- YUKON EC: 2.5V
- 100 Mbps: 126 mA
- 10 Mbps: 108 mA
- No link: 108 mA
- YUKON Ultra: 1.8V
- 1000 Mbps: 426 mA
- 100 Mbps: 203 mA
- 10 Mbps: 179 mA
- No link: 171 mA

---

**Yukon EC (2.5V).**

- YUKON VPD_CLK
- YUKON RSET
- TP_YUKON_CTRL12
- TP_YUKON_CTRL18
- ENET_LOM_DIS_L
- Must be high in S0 state (can use PP3V3_S0 as input)
- ENET_MDI_P<2>
- ENET_MDI_N<0>
- ENET_RESET_L
- PCIE_WAKE_L
- PCIE_ENET_R2D_C_P
- PCIE_ENET_D2R_N

---

**Ethernet (Yukon)**

- C3780
- R3780
- R3781

---

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**Yukon Power Control**

EC: $V_{out} = 2.510V$

Ultra: $V_{out} = 1.912V$

Yukon Ultra requires 1.9V on its magnetics to pass compliance tests

Ultra: Vout = 1.912V
500 mA max output

(V3850 limit)

**Yukon AVDDL LDO**

Vout = 1.2246V * (1 + Ra / Rb)

NC

Yukon Crystal

**ENET Enable Generation**

3.3V ENET FET

33V ENET FET

NOTE: S3 term is guaranteed by source of R3800 & Q3810, MUST BE S3 RAIL.

3.3V ENET FET

WLAN Enable Generation

"ENET" = "S0" || ("S3" && "AC" && "WOL_EN")

"WLAN" = "S0" || ("S3" && "AC" && "WOL_EN")

NOTE: S3 term is guaranteed by source of R3800 & Q3810, MUST BE S3 RAIL.

EC: $V_{out} = 2.510V$

Yukon Ultra requires 1.9V on its magnetics to pass compliance tests

Yukon AVDDL LDO

"WLAN" = "S0" || ("S3" && "AC" && "WOL_EN")

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Transformers should be mirrored on opposite sides of the board.

- Place one cap at each pin of transformers.

C3900, C3901, C3902, C3903

R3900, R3901, R3902, R3903

514-0277

Short shielded RJ-45

Place close to connector.

---

**:BOM Options**

- **Critical**
  - XFR-SM
  - 1000BT-824-00275
  - JM36113-P2054-7F

- **Power Aliases**
  - CERM
  - MF-LF

- **Signal Aliases**
  - T3900, T3901

---

**:Page Notes**

Page dimensions: 1224.0x792.0

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notice of proprietary property

drawling number

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Strap via alias on port page.

Hi: Data-Strobe only (1394a).

Implement 1K pull-up or pull-down on port page.

Multi-port Portable systems are Power Class 4 ('100').

Single-port / Desktop systems are Power Class 0 ('000').

Power Class:

41 = PP3V3_FW_PHY
41 = FWPHY_DS0

R4145
R4142
R4140

R4144

R4150 with internal pull-up prevents PHY power-up reset.

PHY power-up reset.
**FireWire Port Power Switch**

- **C4260**: 0.1uF 25V
- **R4261**: 0.1MF-LF 1/16W 5%

**Current Limit/Active Late-VG Protection**

- **Q4261**: 2N7002DW-X-F
- **R4260**: 100K MF-LF 1/16W 5%

**Late-VG Event Detection**

- **FWLATEGV_3V_REF**: 2.95V when port power is on
- **FWLATEGV_3V_REF Hysteresis**: 2.81V on late Vg event and port power is off

**FireWire Port Power**

- **SYNC_DATE**: 03/19/2007
- **SYNC_MASTER**: M76_MLB

---

**Page Notes**

- **Power aliases required by this page**: `=PPBUS_S5_FW_FWPWRSW (system supply for bus power)`
- **Power aliases required by this page**: `=FW_PORT_FAULT_PU (FireWire Port Power Switch)`

**Signal aliases required by this page**: `=PPVP_FW_SUMNODE (power passthru summation node)`

**Power aliases required by this page**: `=PP3V3_FW_LATEVG_ACTIVE`
FireWire PHY Config Straps

Configured PHY for:
- 2-port Portable Power Class (8)
- Port 1: Data-Drive only (1394A)
- Port 2: Full-duplex (1394B)

Signal aliases required by this page:
- =FWPHY_DS0
- =FWPHY_DS1
- =FWPHY_LATEVG

Termination
Place close to FireWire PHY
V1 spec calls out 2.1V for FW signal integrity

Late-VG Protection Power

PPV_WORLD needs to be biased to at least 2.0V to ensure signal integrity and should be biased to 2.0V for optimal signal quality. 84300 should be in series with a 2.0V rail for this configuration.

Cable Power

"Snapback" & "Late VG" Protection

Note: Trace PPVP_FW_PORT1 must handle up to 1A peak currents per 1394b V1.3 spec.
When a bilingual device is connected to a data-only device, there is no DC path between them, so avoid ground offset issues. This should be hand-connected to logic ground for speed signaling and connection detection currents per 1394b V1.3 spec.
If power source is S3, can tie EN to IN.

SEL=0 Choose SMC

SEL=1 Choose USB

External USB Connector

---

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Drawn by: 
Checked by: 
Rev.: A
Drawn Date: 2007/01/14

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NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

If SMS interrupt is not used, pull up to SMC rail.

If SMS interrupt can be active high or low, rename net accordingly. If SMS interrupt is not used, pull up to SMC rail.
Left ALS Filter

Left ALS circuit has 1K series-R

Right ALS Circuit

RTALS_OP_IN and RTALS_OP_COMP need to be matched

Keyboard LED Driver

MP. This circuit does not use relays, can tie cathode to VCC on topcase flex

ALS Support
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DRAWING NUMBER

SHEET OF

SIZE

APN: 338S0354

Desired orientation when placed on board top-side:

Desired orientation when placed on board bottom-side:

I2C addresses:

ADDR low => 0x30, 0x31
ADDR high => 0x32, 0x33

I2C addresses:

Alias SCL/SDA to GND if using analog outputs only

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TPS51120 LDO/Buffer outputs

Vout = 5.0V
8A max output (L7320 limit)

Vout = 3.3V
5.5A max output (L7360 limit)

50mA max load when EN5 & EN3 high
100mA max load when EN5 high

CRITICAL

C7352
1
330UF
POLY6.3V

D3L
20%

C7351
C7350
1
10UF
CERM
10V20%

=PPVIN_S5_P5VS5

CRITICAL

C7340
1
22UF

XW7320
XW7325

IHLP2525CZ-SM
SI7108DNS

1 2
2.2UH-14A
PWRPK-1212-8

CRITICAL

C7341
1UF
603
X5R

C7324
0.1UF
603
X5R603-1

VOLTAGE=5V
MIN_NECK_WIDTH=0.2 mm
MIN_LINE_WIDTH=0.6 mm
SWITCH_NODE=TRUE

VOLTAGE=0V
MIN_NECK_WIDTH=0.2 mm
MIN_LINE_WIDTH=0.6 mm
GATE_NODE=TRUE
MIN_NECK_WIDTH=0.2 mm

MIN_NECK_WIDTH=0.2 mm
MIN_LINE_WIDTH=0.6 mm

CRITICAL

R7325
4.7
402MF-LF
1/16W
1%

R7306
3.57K
MF-LF 402
1/16W 1%

CRITICAL

Q2
Q1

CASE-D2-LF

C7380
1

C7381

C7381

CRITICAL

IHLP2525CZ

1UF
603
X5R

C7390
10UF
603X5R
20%

5V / 3.3V Power Supply

NOTE: EN5 can float or tie to VIN for automatic 5V LDO enable

NOTE: EN3 can float or tie to VREG5 for automatic 3.3V LDO enable

VOLTEGE=5V
MIN_NECK_WIDTH=0.2 mm
MIN_LINE_WIDTH=0.6 mm

VOLTEGE=0V
MIN_NECK_WIDTH=0.2 mm
MIN_LINE_WIDTH=0.6 mm

50mA max load when EN5 & EN3 high
100mA max load when EN5 high

www.vinafix.vn
Vout = 0.75V * (1 + Ra / Rb)

Vout = 1.50V

R7610
R7611

C7600
C7601

R7601
R7602

C7610
C7615
C7620
C7621

L7620

Q7620

XW7620

1.5V Power Supply

-- Apple Inc. --

www.vinafix.vn
3.3V FW PHY Supply

1.95V FW PHY Supply
3.425V "G3Hot" Supply

Supply needs to guarantee 3.3V delivered to MMC VRM at one time.

Potential Output PPD 7.3V - 45V

PM_G2_P3V3_EN = PM_G2_P5V5_EN

PM_SLP_S3_L = GPUVCORE_PGOOD

100K 1/16W 1%

TPS51117 PGOOD threshold 92.5-97.5% (0.98 - 1.02V)

1.5V / 1.05V PWRGD Circuit

Reports when 1.5V S0 and 1.05V S0 are in regulation.

NOTE: 0.9V is not checked!

Other S0 Rails PWRGD Circuit
1.8V Frame Buffer Regulator

Vout = 0.6V * (1 + Ra / Rb)

1.8V FB Power Supply

Vout = 1.8V
15A max output

MIN_NECK_WIDTH=0.25 mm
MIN_LINE_WIDTH=0.6 mm

MIN_NECK_WIDTH=0.25 mm
MIN_LINE_WIDTH=0.25 mm

www.vinafix.vn
SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

Most CPU signals with impedance requirements are 55-ohm single-ended.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.2 & 4.3

NOTE: Design Guide allows closer spacing if signal lengths can be shortened.

Design Guide recommends each strobe/signal group is routed on the same layer.

Worst-case spacing is 2:1 within Data bus, with 3:1 spacing to the DSTBs.

FSB (Front-Side Bus) Constraints

CPU_VCCSENSE * 25 MIL
CPU_2TO1 *
CPU_55S = 55_OHM_SE

NOTE: 7 mil gap is for VCCSense pair, which

specifying a target differential impedance.

NOTE: 7 mil gap is for VCCSense pair, which

specifying a target differential impedance.

All FSB signals with impedance requirements are 55-ohm single-ended.

Worst-case spacing is 2:1 within Data bus, with 3:1 spacing to the DSTBs.

DSTB complementary pairs are spaced 1:1 and routed as differential pairs.

Design Guide recommends each strobe/signal group be routed on the same layer.

Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Design Guide does not indicate FSB spacing to other signals, assumed 3:1.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 4.2

C

CPU / FSB Net Properties

D

CPU Signal Constraints

E

CPU / FSB Constraints
### Video Signal Constraints

**SOURCE:** Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 7.2, 9.2 & 10.5.

**PCI-Express / DMI Bus Constraints**

**SOURCE:** Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 8.1 - 8.3.

**CRT & TVDAC Signal Single-ended Impedance Varies by Location:**

LVDS signals are 100-ohm +/- 20% differential impedance.

**Video Signal Constraints**

**SOURCE:** Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 7.2, 9.2 & 10.5.

**PCI-Express / DMI Bus Constraints**

**CRT_SYNC2SYNC** 20 MIL

**TVDAC_2TVDAC** *=100_OHM_DIFF*

**TVDAC** 25 MIL *

**CRT** 25 MIL *

**DMI** 20 MIL

**PCIE** 25 MIL *

**LAYER MINIMUM NECK WIDTH**

**MAXIMUM NECK LENGTH**

**DIFFPAIR PRIMARY GAP**

**DIFFPAIR NECK GAP**

**PHYSICAL RULE_SET**

**AREA_TYPE**

**SPACING_RULE_SET**

**WEIGHT**

**LINE-TO-LINE SPACING**

**LAYERS**

**SPACING_RULE_SET**

**NET_SPACING_TYPE1**

**NET_SPACING_TYPE2**

**TABLE_SPACING_RULE_ITEM**

**TABLE_SPACING_ASSIGNMENT_ITEM**

**TABLE_PHYSICAL_RULE_ITEM**

**TABLE_PHYSICAL_RULE_HEAD**

**ELECTRICAL_CONSTRAINT_SET**

**PHYSICAL**

**SPACING**

**SOURCE:** Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 8.1 - 8.3.
### FireWire Interface Constraints

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<th>LAYER</th>
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<th>DIFFPAIR PRIMARY GAP</th>
<th>DIFFPAIR NECK GAP</th>
<th>PHYSICAL RULE_ITEM</th>
<th>SPACING RULE_SET</th>
<th>MULTIPLE NECK WIDTH</th>
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### FireWire Net Properties

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</table>

### FireWire Constraints

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**SYNC_DATE=01/17/2007**
**SYNC_MASTER=T9_NOME**
**051-7413**

**WWW.VINAFIX.VN**
### GDDR3 Frame Buffer Signal Constraints

<table>
<thead>
<tr>
<th>Net Type</th>
<th>Signal</th>
<th>Description</th>
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<tr>
<td>GDDR3 FBM</td>
<td>GDDR3 Frame Buffer</td>
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<tr>
<td>TMDS</td>
<td>TMDS_100D</td>
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<tr>
<td>VGA</td>
<td>VGA_50S</td>
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<td>VGA</td>
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#### Table 1: GDDR3 FB A/B Net Properties

<table>
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<tr>
<th>PHYSICAL_NET</th>
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#### Table 2: GDDR3 FB C/D Net Properties

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<td>PHYSICAL_NET_2</td>
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### Video Signal Constraints

- **GDDR3 Clocks:**
  - GDDR3_CLK
  - VGA_CLK
- **TMDS:**
  - TMDS_100D
  - TMDS_80D

### GPU (G84M) Constraints

#### Electric Constraints

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<thead>
<tr>
<th>ELECTRICAL_CONSTRAINT</th>
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#### Physical Constraints

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---

These tables and constraints apply to the specific GDDR3 Frame Buffer Signal and Video Signal needs, ensuring compatibility and performance across the board.

---

**Note:** This document contains proprietary information and must be handled with confidentiality and care.
### Memory Constraint Relaxations

Allow 0.127 mm spacing for >0.127 mm lines for GND nets.

Allow 0.1 mm spacing for >0.1 mm lines between thru-hole SO-DIMM pins.

### Graphics, SATA Constraint Relaxations

Alternate diff-pair width/gap through BGA fanout areas (95-ohm diff)

---

**MR7 Specific Net Properties**

<table>
<thead>
<tr>
<th>Property</th>
<th>Value</th>
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<td>MEM_70D 6.35 MM</td>
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**Table:**

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---

**Notes:**

- Along with the general constraints, MR7 has specific net properties and constraints that need to be followed.
- Memory constraint relaxations allow for specific spacing rules for high-speed lines and thru-hole pins.
- Graphics and SATA constraint relaxations provide guidelines for alternate diff-pair configurations.

---

**Appendix:**

- Project specific constraints include:
  - SHT: 88 89
  - REV.: 051-7413 14.0.0

---

**Contact:**

- Apple Inc.
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**NOTE:** 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.