## Schematic / PCB #'s

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### ALIASES RESOLVED

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- **Table of Contents**: 4
- **System Block Diagram**: 3
- **Power Block Diagram**: 2
- **BCM Configuration**: 1
- **Functional / ICT Test**: 0
- **Signal Aliases**: 0
- **CPU 1 of 2-FSB**: 0
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- **NB CPU Interface**: 0
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- **NB Misc Interfaces**: 0
- **NB DDR2 Interfaces**: 0
- **NB Power 1**: 0
- **NB Power 2**: 0
- **NB Misc**: 0
- **NB (GM) Decoupling**: 0
- **NB Clock Straps**: 0
- **SB 1 of 4**: 0
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- **SB Decoupling**: 0
- **SB Misc**: 0
- **M9 SMBus Connections**: 0
- **DDR2 2-0 DIMM Connector A**: 0
- **DDR2 2-0 DIMM Connector B**: 0
- **Memory Active Termination**: 0
- **Memory VLT Supply**: 0
- **DDR2 UVGA**: 0
- **CLOCK**: 0
- **Clock Termination**: 0
- **Mobile Clocking**: 0
- **PATA Connector**: 0
- **FireWire PHY (75BB3AA22)**: 0
- **External Controller**: 0
- **Ethernet Connectors**: 0
- **FireWire Port Power**: 0

### M9 MLB

**4/12/2006**

**PVT**

**ALIASES RESOLVED**
### Bar Code Labels / EEE #’s

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<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>REFERENCE DEC</th>
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### Module Parts

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### BOM Options

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*Apple Computer Inc.*
Chassis connection to be made at the mounting hole northwest of the DVI connector.

Chassis connection to be made at the fan cutout near the right ALS.

Chassis connection to be made at the mounting hole southeast of the USB 2.0 connector.

Chassis connection to be made at the mounting hole southeast of the USB connector.

Chassis connection to be made at the mounting hole east of the USB connector.

Chassis connection to be made at the mounting hole southeast of the USB connector.

Digital connection to be made at the heat sink or lower left frame screw as appropriate.

Chassis connection to be made at the fan cutout near the right ALS.

Ethernet Power Management Support

NOTE: ROM options "USB_G_OC_PU" and "NB_CFG<13..12>" are mutually exclusive.

NOTE: Software not expected to implement this feature.

FireWire Aliases

Signal Aliases
CPU VCORE HF AND BULK DECOUPLING

4x 470µF, 20x 22µF 0805

VCCA (CPU AVdd) Decoupling

1x 10µF, 1x 0.01µF

VCCP (CPU I/O) Decoupling

1x 470µF, 6x 0.1µF 0402

NOTE: This cap is shared between CPU and NB.
CPU ZONE THERMAL SENSOR

PLACE U1001 NEAR THE U1200

ADD GND GUARD TRACE

ROUTE CPU_THERMD_P AND CPU_THERMD_N ON SAME LAYER.

10 MIL TRACE

LAYOUT NOTE:

CPU_THERMD_N (TO CPU INTERNAL THERMAL DIODE)

LAYOUT NOTE:

PLACEHOLDER ADT7461A U1001

R1001 1 2
499 1/16W MF-LF 1%

C1001 1 2
CERM50V 0.001uF 10%

R1002 1 2
499 1/16W MF-LF 1%

C1002 1 2
X5R 0.1UF 16V10%

R1005 1 2
10K 1/16W5% MF-LF

R1006 1 2
10K 1/16W MF-LF 5%

CPU_MISC1-TEMP SENSOR

SYNC_MASTER=M1_MLB  
SYNC_DATE=02/10/2006

PP3V3_S0

THRM_CPU_DX_P

THRM_CPU_DX_N

THRM_ALERT_L

THRM_ALERT

SMBUS_SMC_B_S0_SCL

SMBUS_SMC_B_S0_SDA

THRM_ALERT*/

ALERT*/
CPU ITP700FLEX DEBUG SUPPORT

ITP TCK SIGNAL LAYOUT NOTE:
ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU TCK PIN AND THEN FORD BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX CONNECTOR'S FBO PIN.
HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC core rail, tie R#/G#/B#/IREF to VCC Core rail, tie VCCA_TVBG to 1.5V power rail. Tie VSSA_TVBG to GND.

Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and DACx_OUT, IRTNx, and IREF to 1.5V power rail.

TV-Out Disable

Component: DACA, DACB & DACC

S-Video: DACB & DACC only

TV-Out Signal Usage:

VCCD_LVDS must remain powered with proper decoupling. Can leave all signals NC if LVDS is not implemented

LVDS Disable
RTC Battery Connector

- CRITICAL
- SB RTC X2
- VR_PWRGD_CK410
- R2609
- CERM
- R2608
- MF-LF
- 0.1UF
- SC70-5
- R2607
- CERM
- 12pF
- MF-LF
- 2
- 3
- 5
- 1
- 4
- 2
- 1
- MAKE_BASE=TRUE

**Platform Reset Connections**

**Unbuffered**

- Silk: "SYS RST"

**Buffered**

- Initial resistor values are based on CNR, but may change after characterization.

**SB Misc**

Apple Computer Inc.
"Lower" (surface-mount) slot
"Upper" (thru-hole) slot
One cap for each side of every RPAK, one cap for every two discrete resistors

Ensure CS_L and ODT resistors are close to SO-DIMM connector
disable MEMVTT in sleep.

MEMVTT_EN can be used to leave 1.8V powered in S3.

Okay to turn off 5V and

Optional options provided by this page:

C3101

6.3V 20%

X5R

603

10uF

C3102

6.3V

X5R

20%

10uF

R3100

1K

402

MF-LF

1/16W

5%

C3104

6.3V

2.2uF

603

C3100

6.3V

1uF

CERM

402

C3103

1%

16V

X5R

0.1uF

402

C3105

6.3V

SMC-LF

Poly

20%

150uF

PP0V9_S0_MEMVTT_LDO

PP1V8_S0_MEMVTT

PP5V_S0

MEMVTT_VREF

MEMVTT_EN

PP1V8_S3

MEMVTT_EN_PU

1K

R3104

122

220

5%

1/16W

MF-LF

402

PP1V8_S0_MEMVTT_VDDQ

PP1V8_S0

VDDQ VCC

VREF VTT

GND

VTT_IN

EN VTTS

D SIZE

OFSHT

DRAWING NUMBER

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SYNC_DATE=02/10/2006

SYNC_MASTER=M1_MLB
Yukon Power Control

Allows powering Yukon down during battery sleep to save power

R4302

1.2V enable has pull-up to 3.3V

When ENETPWR_S3 BOMOPTION is active:

State: PM_SLP_S4_L PM_SLP_S3BATT PM_SLP_S3BATT_L P2V5S3_EN_L P1V2S3_RUNSS

S0 Batt: 0V 3.3V 0V (3.3V ON) 3.3V 0V (2.5V ON) 3.3V (1.2V ON)

S3 AC: 0V 3.3V 0V (3.3V ON) 3.3V 0V (2.5V ON) 3.3V (1.2V ON)

S3 Batt: PBUS 3.3V PBUS (3.3V OFF) 0V 3.3V (2.5V OFF) 0V (1.2V OFF)

S5 AC: 0V 0V PBUS (3.3V OFF) 0V Hi-Z (2.5V OFF) 0V (1.2V OFF)

G3H Batt: PBUS 0V PBUS (3.3V OFF) 0V Hi-Z (2.5V OFF) 0V (1.2V OFF)

S0: 3.3V 0V (3.3V ON) 3.3V 0V (2.5V ON) 3.3V (1.2V ON)

S3: 3.3V 0V (3.3V ON) 3.3V 0V (2.5V ON) 3.3V (1.2V ON)

S5: 0V PBUS (3.3V OFF) 0V Hi-Z (2.5V OFF) 0V (1.2V OFF)

G3H: 0V PBUS (3.3V OFF) 0V Hi-Z (2.5V OFF) 0V (1.2V OFF)
165mA MAX LOAD

\[ V_{out} = 1.22V \times (1 + \frac{R_a}{R_b}) + (I_{adj} \times R_a) \]

\[ I_{adj} = 30nA @ 25 \text{ deg C} \]

\[ V_{out} = \text{1.22V} \times (1 + \frac{R_a}{R_b}) + (30nA \times R_a) \]
Current Limit/Active Late-VG Protection

Late-VG Event Detection

Current Limits

- 0.005 A
- 0.016 A
- 0.033 A

In the event of current spikes, the device will trip. Current limits are set to accommodate this scenario.

**Note:**
- VIN+ VIN- = 33V
- MIN_NECK_WIDTH = 0.25 mm
- MIN_LINE_WIDTH = 0.5 mm

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ABEF needs to be isolated from all local grounds per 1394b spec.

When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue).

ABEF should be hard connected to logic ground for speed signaling and connection detection currents per 1394b V1.33.

"Snapback" & "Late VG" Protection

When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue).

When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue).

Signal aliases required by this page:
- =PP3V3_S5_FWLATEVG

Port 1
BILINGUAL

Cable Power

Port 2
1394A

FireWire Ports

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Rev. 5140-0133
Port Power Switch

Place L5200, L5205 and L5206 across moat

Right USB Port
**CPU Back-Up Thermal Diode**

- **CPU Back-Up Diode**: R1690
- **Description**: CRITICAL
- **Reference Design**: CRITICAL
- **BOM Option**: CRITICAL

**Placement Note**: Place near CPU center.

**Diagram Notes**: R1001 / R1002 are not currently BOM OPTIONed. Can not programatically unstuff those parts to stuff these.

---

**Right-Side/Fin Stack Thermal Sensor**

- **Part Number**: 518S0226
- **Description**: CRITICAL
- **Reference Design**: CRITICAL
- **BOM Option**: CRITICAL

**Placement Notes**:
- Place near speaker hole.
- Place in between VRAM.
- Place near GPU center.

**Diagram Notes**: Minimize stubs between R1001 & R1002.

---

**GPU / Heat Pipe Thermal Sensor**

- **Part Number**: 518S0226
- **Description**: CRITICAL
- **Reference Design**: CRITICAL
- **BOM Option**: CRITICAL

**Placement Notes**:
- Place near CPU center.
- Place near speaker hole.
- Place near GPU center.

**Diagram Notes**: Keep all 4 XWs as close to U6100 as possible. Minimize stubs between these R's and R1001 & R1002.
R6309 is not needed when sharing SPI flash with ICH7M and Tegra (LAN chip).

R6307 and R6306 should be placed less than 100 mils from ICH7M.

R6303 should be placed less than 100 mils from Flash ROM.
Connect to R7622 pins to control outputs. If unconnected, powers up with VIN.

Vout = 4.98V
8A max output
(L7620 limit)

Vout = 0.8V * (1 + Ra / Rb)
\[ V_{\text{ref}} = 3.42V \times \frac{R_{2a}}{R_{1a} + R_{2a}} \]
\[ V_{\text{th}} = \frac{V_{\text{ref}}}{\frac{R_{2b}}{R_{1b} + R_{2b}}} \]
\[ V_{\text{ref}} = 1.20V \]
\[ V_{\text{th}} = 13.4V \]
LVDS Interface Pull-downs

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The information contained herein is the proprietary property of Apple Computer, Inc., the possessor of M56 part. Bias voltage is present on LVDS interface pins even when they should be tri-stated to meet panel power sequence requirements. Resulting pump-up in LCD panel can cause startup and long-term reliability issues. Pull-down resistors reduce the pump-up in the panel, though some voltage will still be seen on LVDS signals when they should be 0V.

LVDS Interface Pull-downs

- RP9900
  - 1 8
  - 4 5
  - 2 7
  - 3 6
  - 8.2K SM-LF LVDS_PD 1/16W 5%

- RP9901
  - 1 8
  - 2 7
  - 3 6
  - 4 5
  - 8.2K SM-LF LVDS_PD 1/16W 5%

- RP9902
  - 1 8
  - 2 7
  - 3 6
  - 4 5
  - 8.2K SM-LF LVDS_PD 1/16W 5%

- RP9903
  - 1 8
  - 2 7
  - 3 6
  - 4 5
  - 8.2K SM-LF LVDS_PD 1/16W 5%
### DDR2 Memory Bus Constraints

Most CPU signals with impedance requirements are 55-ohm single-ended.

**NOTE:** Design Guide allows closer spacing if signal lengths can be shortened.

**NOTE:** Design Guide does not indicate FSB spacing to other signals, assumed 3:1.

Design Guide recommends each strobe/signal group is routed on the same layer.

Worst-case spacing is 2:1 within Data bus, with 3:1 spacing to the DSTBs.

All FSB signals with impedance requirements are 55-ohm single-ended.

<table>
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<tr>
<th>MEM_CLK2MEM</th>
<th>4:1_SPACING*</th>
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<tbody>
<tr>
<td>CPU_2TO1</td>
<td>=2:1_SPACING</td>
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<tr>
<td>FSB_ADDR</td>
<td>3:1_SPACING*</td>
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</tbody>
</table>

*MEM_CLK2MEM = 4:1_SPACING*, CPU_2TO1 * = 2:1_SPACING, FSB_ADDR = 3:1_SPACING*.

### CPU Signal Constraints

Most CPU signals with impedance requirements are 55-ohm single-ended.

Some signals require 1.8-ohm single-ended impedance.

**SOURCE:** Napa Platform DG, Rev 0.9 (#17978), Sections 4.2.4.4

### FSB (Front-Side Bus) Constraints

<table>
<thead>
<tr>
<th>FSB_CLK</th>
<th>3:1_SPACING</th>
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</thead>
<tbody>
<tr>
<td>FSB_DATA</td>
<td>3:1_SPACING</td>
</tr>
</tbody>
</table>

*FSB_CLK = 3:1_SPACING, FSB_DATA = 3:1_SPACING.*

### Audio Interface Constraints

**SOURCE:** Napa Platform DG, Rev 0.9 (#17978), Sections 10.6 & 10.7.2

### Disk Interface Constraints

**SOURCE:** Napa Platform DG, Rev 0.9 (#17978), Sections 7.2, 9.2 & 10.5.2

### PCI-Express / DMI Bus Constraints

**SOURCE:** Napa Platform DG, Rev 0.9 (#17978), Sections 10.9.1

### USB 2.0 Interface Constraints

**SOURCE:** Napa Platform DG, Rev 0.9 (#17978), Section 10.9.1

### Internal Interface Constraints

**SOURCE:** Napa Platform DG, Rev 0.9 (#17978), Section 10.10.1.2

### Clock Signal Constraints

**SOURCE:** Napa Platform DG, Rev 0.9 (#17978), Section 10.17.1.1

### Napa Platform Constraints

**SOURCE:** Napa Platform DG, Rev 0.9 (#17978), Section 6.2
**Video Signal Constraints**

SOURCE: ATI Layout Guide, Rev 0.5 (DSG-216MOBRADEON-05), Sections 7 & 8.1.2.

- **DQ/DQM/DQS lines** are 40-ohm single-ended impedance.
- **CTRL lines** are 55-ohm single-ended impedance.
- **LVDS and TMDS signals** are 100-ohm +/- 10% differential impedance.
- **LVDS and TMDS pairs** should be kept at least 25 mils apart.
- **Ground shields** can be used around each pair if spacing cannot be met.
- **Ground shields recommended around VGA signals.**
- **VGA should be routed** as close to 75-ohms single-ended impedance as possible.

**High-Speed I/O Interface Constraints**

**PCI Bus Constraints**

- **NOTE:** Layout Guide does not specify LVDS/TMDS spacing to other traces other than “do not run close”

- **ADDR/CTRL lines** should route 35-ohms to T, then 55-ohms to each VRAM device.

**GDDR3 (Frame Buffer) Memory Bus Constraints**

- **NOTE:** Layout Guide does not specify LVDS/TMDS spacing to other traces other than “do not run close”

**GDDR3**

- **ADDR/CTRL** lines should route 35-ohms to T, then 55-ohms to each VRAM device.

**PCI Bus Constraints**

- **PCI** = 2:1_SPACING

**PCI_55S** = 55_OHM_SE = STAND = STAND

- **PCI_CLK** = 2.5:1_SPACING

**PCI_55S** = 55_OHM_SE = STAND = STAND

**More System Constraints**

**SYNC_MASTER=M1_MLB**

**SYNC_DATE=02/10/2006**

**ENET_100D** = 100_OHM_DIFF

**FW_110D**

**TMDS** = 100_OHM_DIFF

- **LVDS** = 100_OHM_DIFF

**TMDS_PAIR2PAIR 25 MIL**

**LVDS_PAIR2PAIR 25 MIL**
### M9 Board-Specific Spacing & Physical Constraints

<table>
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<tr>
<th>Table</th>
<th>Description</th>
<th>MINIMUM NECK LENGTH</th>
<th>MINIMUM NECK WIDTH</th>
<th>PHYSICAL_RULE_SET</th>
<th>MINIMUM LINE WIDTH</th>
<th>ON LAYER?</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>Unsupported rule</td>
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<td>D</td>
<td>Rules for &quot;Topology #3&quot; for FSB signals, Napa DG tables 4-7 &amp; 4-12.</td>
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<tr>
<td>C</td>
<td>Allow 0.1 MM on blind-to-buried via dogbones (layers 2 &amp; 11).</td>
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<tr>
<td>B</td>
<td>&quot;Stale&quot; physical / spacing types</td>
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<tr>
<td>A</td>
<td>Rules for &quot;Topology #9&quot; for FSB signals, Napa DG tables 4-7 &amp; 4-12.</td>
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</table>

**Notes:**
- OVERRIDE = STANDARD
- STAMP = DEFAULT

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**Additional Information:**
- Allow 0.1 MM on blind-to-buried via dogbones (layers 2 & 11).
- "Stale" physical / spacing types.
- Rules for "Topology #9" for FSB signals, Napa DG tables 4-7 & 4-12.

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**Table:**
- Table of physical/spacing rules for M9 board with specific constraints for various signals and layers.