**ALIASES RESOLVED**

**SCHEM,MLB,M96**

**PVT**

**09/26/2008**

---

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**Date**

- 09/26/2008
- 02/04/2008
- 01/09/2007
- 01/09/2007
- 02/01/2008
- 02/01/2008
- 02/01/2008
- 02/01/2008
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- 02/01/2008
- 02/01/2008
- 02/01/2008
- 02/01/2008

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---

**SCHEM,MLB,M96**

---

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### Bar Code Label / EEE #s

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>REFERENCE DDI</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
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<tbody>
<tr>
<td>BOM142-592</td>
<td>[EEE:5P8]</td>
<td>CRITICAL</td>
<td>EEE_5P8</td>
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<td>BOM142-592</td>
<td>[EEE:2AM]</td>
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<td>EEE_2AM</td>
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### Alternate Parts

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<th>PART NUMBER</th>
<th>REFERENCES DESIGNATION(S)</th>
<th>DESCRIPTION</th>
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### Module Parts

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### Configuration Options

**SCS, Masterchip(s)/A**

- **A142592**

**Options of Proprietary Properties**

- **A142592**

---

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## Acoustic Cap BOM Config Tables

### 1UF 0402 Capacitor Vendor Tables for Acoustics

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Qty</th>
<th>Description</th>
<th>Reference Des</th>
<th>Critical</th>
<th>BOM Option</th>
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### 2.2UF 0402 Capacitor Vendor Tables for Acoustics

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<tr>
<th>Part Number</th>
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<th>Critical</th>
<th>BOM Option</th>
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<td></td>
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### 10UF 0603 Capacitor Vendor Tables for Acoustics

<table>
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<th>Qty</th>
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<th>Reference Des</th>
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<th>BOM Option</th>
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<td>Critical</td>
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</table>

---

**Note:** This document contains confidential and proprietary information. Use is subject to the conditions specified in the Acoustic Cap BOM Config Tables. Failure to comply with these conditions may result in legal action.
MCP79-specific pinout

From XDP connector

U1000 CPU

and/or level translator

To XDP connector

U1400 MCP

XDP connector

Extended Debug Port (XDP)
Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).
SYNC FROM M97

WF: Checklist says 0-ohm resistor placeholder for ferrite bead.

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

WF: Checklist says 0-ohm resistor placeholder for ferrite bead.

CURRENT NUMBERS FROM EMAIL Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

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DDR3 RESET Support

MCP79 cannot control this signal directly since it must be high in sleep and MEM rails are not powered in sleep.

1. C1003 must be pulled before 1.5V starts to rise to avoid glitch on MEM_RESET_L.

3.3V input must be stable before 1/20W 5% MF 201 1K 2 1

R3010

MEMRESET_HW 201 0.1UF X5R 6.3V 10%

2 1

C3000

5% 10K MEMRESET_HW

2 1

R3000

MEMRESET_MCP MF 5% 1/20W 0 201 2

1 2

R3009

MEMRESET_HW

5% 1/20W MF 2

2 1

R3005

MEMRESET_HW

SOT-363-LF MMDT3904-X-G

1 6 2

Q3005

27 28 29 30 66

5% 20K MEMRESET_HW

2 1

R3001

MEMRESET_HW

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APPROXIMATE CAP ARRANGEMENT

COLUMN OF THREE CAPS BETWEEN PACKAGES

COLUMN OF THREE CAPS BETWEEN PACKAGES

2 CAPS ALONG PACKAGE EDGE

2 CAPS ALONG PACKAGE EDGE
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APPROXIMATE CAP ARRANGEMENT

DDR BYPASSING 2

A.0.0

06/20/2005

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JEDEC recommends 30 Ohm term to VTT for CS, CKE, ODT and 36 Ohm for BA, A, RAS, CAS, WE
M93 WIRELESS AIRPORT & BT CONNECTOR

APN: 516S0580
Micro-DisplayPort / USB to RIO Hatch Assembly
those designated as inputs require pull-ups.
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LOCAL TEMP NEAR POWER SUPPLIES

(WRITE: 0x90 READ: 0x91)

LOCAL TEMP NEAR AIR VENT

(WRITE: 0x92 READ: 0x93)

LOCAL TEMP NEAR FRONT EDGE

(WRITE: 0x92 READ: 0x93)
FAN CONNECTOR

---

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**Drawings**

- **Drawing Number**: 518S0658
- **Sheet of**: 5
- **Size**: 21

**Motor Control**

- **FAN CONNECTOR**
- **Fan Connector**
- **NC**: Fan Connector
- **NC**: Fan Connector
- **TACH**: 5V DC
- **5%**: 1/20W
- **MF**: 201
- **47K**: 2

**Critical Components**

- **R5665**: 100K 1/20W MF 100K
- **R5660**: 5% 1/20W 47K
- **R5661**: 5% 1/20W 47K
- **Q5660**: SSM3K15FV SOD-VESM-HF
- **J5600**: CRITICAL F-RT-SM SM04B-SURKHF-GAN-TF-LF-SN

---

**Schematic**

- **Fans**: SMC_FAN_0_CTL, SMC_FAN_0_TACH
- **Power Supply**: PP5V_S0, PP3V3_S0
- **Sync Date**: 01/09/2007
- **Sync Master**: M70

---

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SUDDEN MOTION SENSOR

Desired orientation when placed on board top-side:

Circle indicates pin 1 location when placed in correct orientation.
1V05 S5 POWER SUPPLY

supply for MCP1V05 AUX, FSB (CPU & MCP) VTT, 1V05 S0

MAX CURRENT = 12A
PWM FREQ = 400KHZ

Critical
1V05 S5 Power Supply

www.vinafix.vn
1.5V/0.75V POWER SUPPLY

<table>
<thead>
<tr>
<th>State</th>
<th>PM_S4_STATE_H</th>
<th>PM_SLP_S3</th>
<th>PP1V5_S3</th>
<th>PP0V75_S0</th>
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</thead>
<tbody>
<tr>
<td>S0</td>
<td>HIGH</td>
<td>HIGH</td>
<td>1.5V</td>
<td>0.75V</td>
</tr>
<tr>
<td>S3</td>
<td>HIGH</td>
<td>LOW</td>
<td>1.5V</td>
<td>0.0V</td>
</tr>
<tr>
<td>S5/G3Hot</td>
<td>LOW</td>
<td>LOW</td>
<td>0.0V</td>
<td>0.0V</td>
</tr>
</tbody>
</table>

Vout = 0.75V * (1 + Ra / Rb)

Routing Note:
- 402-1 X5R 10V
- 402 X5R 16V 10%
- 1UF C7500
- 1UF C7540
- put 6 vias under the thermal pad
- OMIT Q7521 PIN1,2.3
- Connect CS_GND to GND
- PLACE XW7500, NEAR C7542 PIN 2
- PLACE C7507, C7508 GND NEAR PIN 1
- PP0V75_S0
- PP0V75_S3

1.5V/0.75V Supplies

PWM FREQ. = 400 kHz
MAX CURRENT = 11A
(inductor limited)

1.5V Supplies

- sync_master=sync
- sync_date=01/09/2007

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Power Control Signals

S0 ENABLE

S3 ENABLE

3.3V 1.05V AND 1.5V S0 RAILS MONITOR CIRCUIT

OTHER S0 RAILS PGOOD
PBUS SUPPLY / BATTERY Charger

PWM FREQ. = 400 kHz
MAX CURRENT = 5.35A??
(AC adapter limited?)
NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

Intel Design Guide recommends FSB signals be routed only on internal layers.

Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

DSTB# complementary pairs are spaced normally and are NOT routed as differential pairs.

Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.

FSB 4X signals / groups shown in signal table on right.

### Physical Rule Set

**Line-To-Line Spacing**
- **Top, Bottom:**
  - Minimum Line Width = 100_OHM_DIFF
  - Weight = 7 mil
  - Table Spacing Rule Item: 27P4_OHM_SE

**Spacing Rule Set**
- **On Layer?**
  - = 50_OHM_SE
  - = 2x_DIELECTRIC
  - = STANDARD
  - = 25 MILD

### CPU Signal Constraints

**Minimum Line Width**
- **Top, Bottom:** = 9 mil

**Weight**
- **Top, Bottom:** = 9 mil

**Table Spacing Rule Item**
- **DIFFPAIR NECK GAP:** = 1:1_DIFFPAIR
- **7 MIL**

**Table Physical Rule Head**
- **Table Physical Rule Item**

**CPU/FSB Net Properties**

**Minimum Line Width**
- **Top, Bottom:** = 9 mil

**Weight**
- **Top, Bottom:** = 9 mil

**Table Spacing Rule Item**
- **DIFFPAIR NECK GAP:** = 1:1_DIFFPAIR
- **7 MIL**

**Table Physical Rule Head**
- **Table Physical Rule Item**

**CPU/FSB Constraints**

**Minimum Line Width**
- **Top, Bottom:** = 9 mil

**Weight**
- **Top, Bottom:** = 9 mil

**Table Spacing Rule Item**
- **DIFFPAIR NECK GAP:** = 1:1_DIFFPAIR
- **7 MIL**

**Table Physical Rule Head**
- **Table Physical Rule Item**

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All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).

A/BA/cmd signals should be matched within 5 ps of CLK pairs. CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.

DQ signals should be matched within 5 ps of associated DQS pair.

Memory Bus Spacing Group Assignments

Memory Bus Constraints

Memory Net Properties

Memory Constraints
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.

**Digital Video Signal Constraints**

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.1 & 2.5.2.

- R/G/B signals should be matched as close as possible and < 10 inches.
- 75-ohm from output of three-pole filter to connector (if possible).
- CRT signal single-ended impedance varies by location.

**PHYSICAL_RULE_SET**

- POINT-TO-POINT SPACING RULES
  - CRT-50S
  - PCIE_90D
  - CRT
  - PCIE
  - SATA
  - PCIE_90D

**SPACING_RULE_SET**

- PHYSICAL RULES
  - CRT_2CLK
  - CRT_2CRT
  - LVDS_100D
  - LVDS_2CLK
  - LVDS_2CRT
  - LVDS_IG_B_CLK
  - LVDS_IG_B_DATA_P<3>
  - LVDS_IG_B_DATA_P<2..0>
  - LVDS_IG_A_DATA_P<2..0>
  - LVDS_IG_A_DATA_F_P<2..0>
  - LVDS_IG_A_CLK_P
  - CLK_PCIE_100D
  - CLK_PCIE
  - PCIE
  - PEG_D2R

**ELECTRICAL_CONSTRAINT_SET**

- SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.5.2.

**OTHERS**

- MCP_IFPAB_VPROBE
  - LVDS_IG_B_CLK
  - LVDS_IG_B_DATA_P<3>
  - LVDS_IG_B_DATA_P<2..0>
  - NC_LVDS_IG_A_DATA_P3
  - LVDS_IG_A_DATA_P<2..0>
  - LVDS_IG_A_DATA_F_P<2..0>
  - LVDS_IG_A_CLK_P
  - DP_AUX_CH
  - DP_ML
  - TMDS_IG_TXC
  - MCP_PEX_CLK_COMP
  - PCIE_CLK100M_EXCARD_N
  - PCIE_CLK100M_EXCARD_P
  - PCIE_CLK100M_FC_N
  - PCIE_CLK100M_MINI_N
  - PCIE_FC_D2R_N
  - PCIE_FC_D2R_P
  - PCIE_FC_R2D_C_P
  - PCIE_EXCARD_R2D_C_P
  - PCIE_EXCARD_R2D_P
  - PCIE_FW_D2R_C_N
  - PCIE_FW_R2D_C_N
  - PCIE_FW_R2D_N
  - PCIE_E_D2R_P
  - PCIE_E_R2D_C_N
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  - PEG_D2R_N<15..0>
  - PEG_D2R_P<15..0>
  - PEG_R2D_C_N<15..0>
  - PEG_R2D_P<15..0>

**TABLE_PHYSICAL_RULE_ITEM**

- PHYSICAL RULES
  - CRT-50S
  - PCIE_90D
  - CRT
  - PCIE
  - SATA
  - PCIE_90D

**TABLE_PHYSICAL_RULE_HEAD**

- PHYSICAL RULES
  - CRT-50S
  - PCIE_90D
  - CRT
  - PCIE
  - SATA
  - PCIE_90D

**TABLE_SPACING_RULE_ITEM**

- PHYSICAL RULES
  - CRT-50S
  - PCIE_90D
  - CRT
  - PCIE
  - SATA
  - PCIE_90D

**TABLE_SPACING_RULE_HEAD**

- PHYSICAL RULES
  - CRT-50S
  - PCIE_90D
  - CRT
  - PCIE
  - SATA
  - PCIE_90D

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Sync Date = 02/04/2008
Sync Master = M97

SMbus Charger Net Properties

SMbus Net Properties

SMbus Charger Net Properties

SMbus Constraints
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**Table: Board-Specific Spacing & Physical Constraints**

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