1. All resistance values are in ohms, 0.1 watt +/- 5%.
2. All capacitance values are in microfarads.
3. All crystals & oscillator values are in hertz.

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</tr>
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</table>

**PVT BUILD**

**M97 MLB SCHEMATIC**

REFERENCED FROM T18

08/27/2008
## M97 BOARD STACK-UP

**Top**
- SIGNAL
- GROUND
- SIGNAL (High Speed)
- SIGNAL (High Speed)
- GROUND
- POWER
- POWER
- GROUND
- SIGNAL (High Speed)
- SIGNAL (High Speed)
- GROUND
- BOTTOM

**Diagram**

![Diagram](https://www.vinafix.vn)

**Notes**
- Preliminary

---

**R0M Variants**

<table>
<thead>
<tr>
<th>R0M Option</th>
<th>R0M Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>M97(Common)</td>
<td>PDC,SL3BU,PRQ,2.26,25W,1066,C0,3M,BGA</td>
<td>CRITICAL</td>
</tr>
<tr>
<td>M97(Common)</td>
<td>PDC,SLG8E,PRQ,2.0,25W,1066,M0,3M,BGA</td>
<td>CRITICAL</td>
</tr>
<tr>
<td>M97(Common)</td>
<td>PDC,QDYJ,QS,2.4,25W,1066,M0,3M,BGA</td>
<td>CRITICAL</td>
</tr>
<tr>
<td>M97(Common)</td>
<td>PDC,QJGL,QS,2.0,25W,1066,M0,3M,BGA</td>
<td>CRITICAL</td>
</tr>
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</table>

**Bar Code Labels / EEE #’s**

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>DESCRIPTION</th>
<th>REFERENCE DES</th>
<th>CRITICAL</th>
<th>R0M OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>338S0540</td>
<td>IC,GMCP,MCP79,35X35MM,BGA1437,A01</td>
<td>CRITICAL-U1400</td>
<td>MCP_A011</td>
<td></td>
</tr>
<tr>
<td>338S0603</td>
<td>IC,GMCP,MCP79,35X35MM,BGA1437,A01</td>
<td>CRITICAL-U1400</td>
<td>MCP_A01Q</td>
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<tr>
<td>338S0600</td>
<td>IC,GMCP,MCP79,35X35MM,BGA1437,B01</td>
<td>CRITICAL-U1400</td>
<td>MCP_B01</td>
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</tbody>
</table>

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**Module Parts**

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>DESCRIPTION</th>
<th>REFERENCE DES</th>
<th>CRITICAL</th>
<th>R0M OPTION</th>
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</thead>
<tbody>
<tr>
<td>337S3653</td>
<td>CRITICAL-U1000 CPU_2_26GHZ</td>
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<tr>
<td>337S3646</td>
<td>CRITICAL-U1000 CPU_2_0GHZ</td>
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<tr>
<td>337S3625</td>
<td>CRITICAL-U1000 CPU_2_4GHZ_QS</td>
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<tr>
<td>337S3622</td>
<td>CRITICAL-U1000 CPU_2_4GHZ</td>
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**Programmable Parts**

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>DESCRIPTION</th>
<th>REFERENCE DES</th>
<th>CRITICAL</th>
<th>R0M OPTION</th>
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</thead>
<tbody>
<tr>
<td>338S0591</td>
<td>CRITICAL-U1000 CPU_2_26GHZ</td>
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<tr>
<td>338S0563</td>
<td>CRITICAL-U1000 CPU_2_0GHZ</td>
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<tr>
<td>338S0570</td>
<td>CRITICAL-U1000 CPU_2_4GHZ</td>
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</tbody>
</table>

---

**Alternate Parts**

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>DESCRIPTION</th>
<th>REFERENCE DES</th>
<th>CRITICAL</th>
<th>R0M OPTION</th>
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</thead>
<tbody>
<tr>
<td>337S3639</td>
<td>CRITICAL-U1000 CPU_2_4GHZ</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>338S0540</td>
<td>CRITICAL-U1000 CPU_2_0GHZ</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>338S0603</td>
<td>CRITICAL-U1000 CPU_2_4GHZ</td>
<td></td>
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</tr>
</tbody>
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Revision History

Sync_Master=M97_MLB

Preliminary

www.vinafix.vn
1.05V TO 3.3V LEVEL TRANSLATOR (M97: ON ICT FIXTURE)

From XDP connector or via level translator

U1000
CPU

To XDP connector and/or level translator

U1400
MCP

From XDP connector

XDP connector

JTAG Scan Chain

JTAG_LVL_TRANS_EN_L

=PP3V3_S0_XDP

JTAG_LVL_TRANS_EN_H

=PP1V05_S0_CPU

JTAG_MCP_TDI

XDP_TDI

JTAG_MCP_TDO

XDP_TDO

JTAG_MCP_TMS

XDP_TMS

JTAG_MCP_TCK

XDP_TCK

JTAG_MCP_TRST_L

XDP_TRST_L
SYNC FROM T18
CHANGE CPU FROM SOCKET TO BGA SYMBOL
SYNC FROM T18
CHANGE CPU FROM SOCKET TO BGA SYMBOL

Current numbers from Merom for Santa Rosa EMTS, doc #20905.
Change C1240-C1243 and C1260 from 128S0241 (9 milli-ohm) to 128S0231 (6 milli-ohm).

Remove C1244 & C1245.

Remove no stuff caps C1220 to C1231.

Sync from T18.

Place inside socket cavity on secondary side.

VCCA (CPU AVdd) Decoupling
1x 10µF, 1x 0.1µF.

Place on secondary side.

VCCP (CPU I/O) Decoupling
1x 10µF, 1x 0.01µF.

Place on secondary side.

CPU Decoupling

Placing Note: Place C1260 between CPU & NB. 1x 330µF, 6x 0.1µF. 0402

Sync from T18.

Place inside socket cavity on secondary side.

CPU VCore HF and Bulk Decoupling
MCP79-specific pinout

SYNC FROM T18
CHANGE STANDARD XDP CONNECTOR TO SMALLER ONE 516S0625
RENAME JTAG_MCP_TDO TO JTAG_MCP_TDO_CONN
RENAME XDP_TDO TO XDP_TDO_CONN
Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

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<th>Preliminary</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
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<tr>
<td>36A3</td>
<td>73A3</td>
<td>36A3</td>
<td>73A3</td>
<td>36B2</td>
<td>73A3</td>
<td>OUT</td>
<td>OUT</td>
<td></td>
</tr>
<tr>
<td>8A6</td>
<td>8A6</td>
<td>73A3</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>127 mA (A01, AVDD0 &amp; 1)</td>
<td>2.49K</td>
<td>402</td>
<td>MF-LF</td>
<td>1/16W</td>
<td>1%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MCP_SATA_TERMP</td>
<td>=PP1V05_S0_MCP_SATA_DVDD0</td>
<td>PP1V05_S0_MCP_PLL_SATA</td>
<td>TP_SATA_F_D2RN</td>
<td>TP_SATA_F_R2D_CN</td>
<td>TP_SATA_F_R2D_CP</td>
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<tr>
<td></td>
<td>TP_SATA_E_D2RP</td>
<td>TP_SATA_E_D2RN</td>
<td>TP_SATA_E_R2D_CN</td>
<td>TP_SATA_D_D2RN</td>
<td>TP_SATA_D_R2D_CN</td>
<td>TP_SATA_D_R2D_CP</td>
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<td></td>
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<tr>
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<td></td>
<td>TP_SATA_C_R2D_CN</td>
<td>TP_SATA_C_R2D_CP</td>
<td>SATA_ODD_D2R_P</td>
<td>SATA_ODD_D2R_N</td>
<td>SATA_HDD_D2R_P</td>
<td>SATA_HDD_D2R_N</td>
<td>SATA_HDD_R2D_C_P</td>
</tr>
</tbody>
</table>

If all SATA_Cx pins are not used, ground DVDD1_SATA and AVDD1_SATA.

If all SATA_Ax & Bx pins are not used, ground DVDD0_SATA and AVDD0_SATA.
3.3V Interface Pull-ups

These internal pull-ups are missing in Revs A01 & A01P.

3.3V Interface Pull-ups

MCP_SAFE_MODE SIGNAL TO SUPPORT ROM FAILURE OVERRIDE

SMC_MCP_SAFE_MODE = PP3V3_S5_MCP_A01
Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

8B5

25A8

25A7

8B7

18A6

18A3

18A6

18A6

18B6 18C3

8A7

8C5

73A3 73B3

73A3

18A3

18A6

18A6

224x224

222x188

234x201

237x180

220x175

370x194

371x200

222x124

SCL

SDA

WP

GND

VCC

IN

BI

SCL

SDA

WP

GND

VCC

DEF. Omron caps 4mm resistor placeholder for service board.
DEF. In 4mm 0402, in 0.1uf 0603 (4.8 uF)
Apple: In 2.2uf 0402 (4.4 uF)

16 mA (A01)

190 mA (A01, 1.8V)

95 mA (A01)

206 mA (A01)

WF: Checklist says 0-ohm resistor placeholder for ferrite bead.
WF: Checklist says 0-ohm resistor placeholder for ferrite bead.

WF: Open question on which packge option(s) nVidia can support.

1x 4.7uF 0603, 2x 0.1uF 0402 (4.9 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)

CHANGE C2651 TO R2651 TO GND PP3V3_S0_MCP_DAC

NO STUFF PP3V3_S0_MCP_DAC RAIL COMPONENTS (L2650 AND C2650)

WASHINGTON MCP GRAPHICS SUPPORT

SYNC FROM T18

REPLACE MCP 27MHZ CRYSTAL CIRCUIT SINCE NOT SUPPORTING TV-OUT

REPLACE DAC TERMINATIONS R2665, C2665 AND R2670 TO R2672

NO STUFF PP3V3_S0_MCP_DAC_UF

MORE T2665, C2665 RAIL COMPONENTS (L2650 AND C2650)

CHANGE C2651 TO R2651 TO GND PP3V3_S0_MCP_DAC

PP3V3_S0_MCP_DAC_UF

PP1V05_S0_MCP_HDMI_VDD = PP3V3R1V8_S0_MCP_IFP_VDD

PP3V3_S0_HDCPROM

= PP1V05_S0_MCP_HDMI_VDD

= PP3V3_S0_MCP_IFP_VDD

= I2C_HDCPROM_SCL

= I2C_HDCPROM_SDA

HDCP ROM

RF: Open question on which package option(s) nVidia can support.

RF: Omron caps 4mm resistor placeholder for service board.
DEF. In 4mm 0402, in 0.1uf 0603 (4.8 uF)
Apple: In 2.2uf 0402 (4.4 uF)

16 mA (A01)

190 mA (A01, 1.8V)

95 mA (A01)

206 mA (A01)

WF: Checklist says 0-ohm resistor placeholder for ferrite bead.
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1x 4.7uF 0603, 2x 0.1uF 0402 (4.9 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)

CHANGE C2651 TO R2651 TO GND PP3V3_S0_MCP_DAC

NO STUFF PP3V3_S0_MCP_DAC RAIL COMPONENTS (L2650 AND C2650)

WASHINGTON MCP GRAPHICS SUPPORT

SYNC FROM T18

REPLACE MCP 27MHZ CRYSTAL CIRCUIT SINCE NOT SUPPORTING TV-OUT

REPLACE DAC TERMINATIONS R2665, C2665 AND R2670 TO R2672

NO STUFF PP3V3_S0_MCP_DAC_UF

MORE T2665, C2665 RAIL COMPONENTS (L2650 AND C2650)

CHANGE C2651 TO R2651 TO GND PP3V3_S0_MCP_DAC

PP3V3_S0_MCP_DAC_UF

PP1V05_S0_MCP_HDMI_VDD = PP3V3R1V8_S0_MCP_IFP_VDD

PP3V3_S0_HDCPROM

= PP1V05_S0_MCP_HDMI_VDD

= PP3V3_S0_HDCPROM

= PP1V05_S0_MCP_HDMI_VDD

= PP3V3_S0_HDCPROM

= PP1V05_S0_MCP_HDMI_VDD

= PP3V3_S0_HDCPROM

= PP1V05_S0_MCP_HDMI_VDD

= PP3V3_S0_HDCPROM

= PP1V05_S0_MCP_HDMI_VDD

= PP3V3_S0_HDCPROM

= PP1V05_S0_MCP_HDMI_VDD

= PP3V3_S0_HDCPROM

= PP1V05_S0_MCP_HDMI_VDD

= PP3V3_S0_HDCPROM

= PP1V05_S0_MCP_HDMI_VDD

= PP3V3_S0_HDCPROM

= PP1V05_S0_MCP_HDMI_VDD

= PP3V3_S0_HDCPROM

= PP1V05_S0_MCP_HDMI_VDD

= PP3V3_S0_HDCPROM

= PP1V05_S0_MCP_HDMI_VDD

= PP3V3_S0_HDCPROM

= PP1V05_S0_MCP_HDMI_VDD

= PP3V3_S0_HDCPROM

= PP1V05_S0_MCP_HDMI_VDD

= PP3V3_S0_HDCPROM

= PP1V05_S0_MCP_HDMI_VDD

= PP3V3_S0_HDCPROM

= PP1V05_S0_MCP_HDMI_VDD

= PP3V3_S0_HDCPROM

= PP1V05_S0_MCP_HDMI_VDD

= PP3V3_S0_HDCPROM

= PP1V05_S0_MCP_HDMI_VDD

= PP3V3_S0_HDCPROM

= PP1V05_S0_MCP_HDMI_VDD

= PP3V3_S0_HDCPROM

= PP1V05_S0_MCP_HDMI_VDD

= PP3V3_S0_HDCPROM

= PP1V05_S0_MCP_HDMI_VDD

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= PP1V05_S0_MCP_HDMI_VDD

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= PP1V05_S0_MCP_HDMI_VDD

= PP3V3_S0_HDCPROM

= PP1V05_S0_MCP_HDMI_VDD

= PP3V3_S0_HDCPROM

= PP1V05_S0_MCP_HDMI_VDD

= PP3V3_S0_HDCPROM

= PP1V05_S0_MCP_HDMI_VDD

= PP3V3_S0_HDCPROM

= PP1V05_S0_MCP_HDMI_VDD

= PP3V3_S0_HDCPROM

= PP1V05_S0_MCP_HDMI_VDD

= PP3V3_S0_HDCPROM

= PP1V05_S0_MCP_HDMI_VDD

= PP3V3_S0_HDCPROM

(119,186),(989,774)
DDR3 RESET Support

MCP cannot control this signal directly since it must be high in sleep and MEM Reset rails are not powered in sleep.

Avoid glitch on MEM_RESET_L. Before 1.5V starts to rise to 3.3V input must be stable before 1.5V.

MCP79 cannot control this signal directly since it must be high in sleep and MEM rails are not powered in sleep.

DDR3 RESET Support

1/16W
5%
MF-LF
1K
402
R3310
1
2

CERM
0.1UF
MEMRESET_HW
402
10V
C3300
1
2

20%
5%
10K
MEMRESET_HW
1/16W
MF-LF
402
R3300
1
2

MMDT3904-X-G
MEMRESET_HW
SOT-363-LF
Q3305
5
3
4

16C3
MEMRESET_MCP
MF-LF
5%
1/16W
0
402
R3309
1
2

MEMRESET_HW
SOT-363-LF
MMDT3904-X-G
Q3305
2
6
1

28C2 29C2
5%
20K
MEMRESET_HW
1/16W
MF-LF
402
R3301
1
2

Preliminary

www.vinafix.vn
WLAN Enable Generation

NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.

3.3V ENET FET

NOTE: 3.3V FET provided 25MHz clock. See clock connections above.

1.05V ENET FET

NOTE: 1.05V FET provided 25MHz clock. See clock connections above.

RTL8211 25MHz Clock

NOTE: R171 is 25MHz clock. See clock connections above.
We can remove C4690 later if the output cap of the 5V_S5 regulator is close enough.

---

**USB/SMC Debug Mux**

---

We can add protection to 5V if we want, but leaving NC for now

---

**Port Power Switch**

---

**USB PORT A (FRONT PORT)**

---

**USB PORT B (BACK PORT)**

---

**External USB Connectors**
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating.

If SMS interrupt is not used, pull up to SMC rail.

NOTE: SMS Interrupt can be active high or low, rename net accordingly.
MCP VCore Current Sense

MCP VCore Current Sense Filter

MCP MEM VDD Current Sense

MCP MEM VDD Current Sense Filter

CPU 1.05V AND CPU VCORE HIGH SIDE CURRENT SENSE

BMON CURRENT SENSE

PLACE U5413, R5423, R5431, C5459 NEAR SMC (U4900)

CPU VCore Load Side Current Sense / Filter

DC-IN (AMON) CURRENT SENSE

NOTE: MONITORING CURRENT FROM BATTERY TO FRC (BATTERY DISCHARGE ACROSS R7008)

PLACE U5403 AND C5418 NEAR R7008
Digital SMS

Pull-up required if SMS_INT_L is not used.

Staff R5931 and pull-up R5932 to use U5930

NoStuff R5931 and pull-up R5932 if U5930 is not used

Desired orientation when placed on board top-side:

Circle indicates pin 1 location when placed in correct orientation:

Analog SMS

Pull-up of SMS_PWRDN to turn off SMS when PIN is not being driven by SMC

Desired orientation when placed on board top-side:

Circle indicates pin 1 location when placed in correct orientation:

R5921 Preliminary
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Apple Inc.
5V_RT/3.3V POWER SUPPLY

VOUT = (2 * RA / RB) + 2

VOUT = (2 * RC / RD) + 2

PWM FREQ. = 300 KHz
MAX CURRENT = 4A

PWM FREQ. = 375 KHz
MAX CURRENT = 4A

Place XW7201 between Pin 15 and Pin 25 of U7200.

Place XW7202 by C7292.

Place XW7203 by Pin 1 of L7220.

Place XW7204 by Pin 2 of L7220.

Place XW7205 by Pin 2 of L7260.

Place XW7206 by Pin 2 of L7260.
1.5V/0.75V (DDR3) POWER SUPPLY

VOUT = 0.75V * (1 + RA / RB)

MAX CURRENT = 12A
PWM FREQ. = 400 KHZ

1.5V HIGH
LOW 0.0V

1.5V
0.75V

PP0V75_S0

PWM FREQ. = 400 KHZ

1.5V/0.75V DDR3 SUPPLY

CTRL:...PM_SLP_S4_L | PM_SLP_S3_L | PP1V5_S3 | PP0V75_S0
S0 | HIGH | HIGH | 1.5V | 0.75V
S3 | HIGH | LOW | 1.5V | 0.0V
S5/G3HOT | LOW | LOW | 0.0V | 0.0V

VENF/5V_S0_REG

CRITICAL

U7300
TPS1116

CRITICAL

Q7320
SI7110DN
PWRPK-1212-8-HF

CRITICAL

Q7321
SI7108DN
PWRPK-1212-8-HF

SYNC_DATE=01/31/2008
SYNC_MASTER=RAYMOND
CPUVTT POWER SUPPLY

Place XW7600 between Pin 7 and Pin 15 of U7600.

Vout = 1.052V

Place XW7601 by C7660.

Vout = 0.75V * (1 + Ra / Rb)

F = 400 KHZ

Q7620 CRITICAL SI7110DN PWRPK-1212-8-HF

Q7621 CRITICAL SI7108DN PWRPK-1212-8-HF

X5R 20% CRITICAL 2 1

C7660 330UF POLY-TANT

C7665 10UF SM

XW7665 PLACEMENT_NOTE=Place XW7665 next to L7620

402 CASE-C2-SM 2.5V 20%

C7695 1UF 10% 25V

C7630 CRITICAL 20% 16V 33UF

C7603 6.3V X5R-CERM 4.7UF 10%

TPS51117RGY_QFN14 QFN CRITICAL 3 5 14 4 10 11 2 15 6 8 12 7 1 9 13 10 11

U7600 XW7600 SM 21

C7601 10% 64C1 64A5

R7601 6.65K 402 MF-LF 1% 1/16W

R7603 MF-LF 1/16W 1% MF-LF 187K 2 1

R7604 MF-LF 1/16W 1% MF-LF 402 1%

C7696 50VCERM402 0.001UF 20%

C7661 SM-IHLP-1 1.0UH-13A-5.6M-OHM

C7604 6.3V 603 X5R-CERM

C7605 603-1 0.1UF

C7606 10% 250V 603-1

C7607 X7R 1

C7608 4.7UF 10%

C7609 10% 250V 603-1

C7610 25V 50V 0.001UF 20%

C7611 20%

C7612 16V 33UF

C7613 1UF 10V X5R 402-1

C7614 10% 50VCERM402 0.001UF 20%

C7615 2

C7616 1

L7620 1.0OH-13A-5.6M-OHM CRITICAL

CPU VTT (1.05V) SUPPLY =PP5V_S0_CPUVTTS0

SWITCH_NODE=TRUE

CPUVTTS0_LL MIN_LINE_WIDTH=0.6MM

MIN_NECK_WIDTH=0.2MM

MIN_LINE_WIDTH=0.6MM

CPUVTTS0_PGOOD

MIN_NECK_WIDTH=0.2MM

MIN_LINE_WIDTH=0.6MM

CPUVTTS0_TRIP

MIN_NECK_WIDTH=0.2MM

MIN_LINE_WIDTH=0.6MM

CPUVTTS0_VBST

MIN_NECK_WIDTH=0.2MM

MIN_LINE_WIDTH=0.6MM

CPUVTTS0_DRVL

GATE_NODE=TRUE

MIN_LINE_WIDTH=0.6MM

MIN_NECK_WIDTH=0.2MM

VOLTAGE=0V GND_CPUVTTS0_SGND

MIN_NECK_WIDTH=0.2 mm

VOLTAGE=5V MIN_LINE_WIDTH=0.6 mm

PP5V_S0_CPUVTTS0_V5FILT

=PPCPUVTT_S0_REG

MIN_NECK_WIDTH=0.2MM

MIN_LINE_WIDTH=0.6MM

CPUVTTS0_DRVH

GATE_NODE=TRUE MIN_LINE_WIDTH=0.6MM

CPUVTTS0_VSNS

CPUVTTS0_TON

MIN_NECK_WIDTH=0.2MM

MIN_LINE_WIDTH=0.6MM

CPUVTTS0_VOUT

Sync Date=02/08/2008 Sync Master=RAYMOND

50A6 8D5 8C1 8D8

Preliminary

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1.8V S0 SWITCHER

MCP 1.05V_S5 AUXC SUPPLY

VOUT = 0.6V * (1 + Ra / Rb)

MCP79 Rev A01 requires higher voltage

VOUT = 1.102V

MAX Current = 1.5A

FREQ = 1Mhz

MAX CURRENT = 200MA

INPUT RAIL IS 3.3V S0

1.8V S0 SWITCHER

MISC POWER SUPPLIES

PART NUMBER QTY DESCRIPTION REFERENCE DES CRITICAL BOM OPTION

R7722 1 CRITICAL C120

R7780 1 CRITICAL 1/16W 348K 1% 0402 SMD LF

C7781 2 6.3V 22UF 20% 805CERM

C7782 2 22PF 1% 1/16W MF-LF

R7781 2 1.8V 1% 1/16W MF-LF

C7783 2 1/16W MF-LF 5% 805CERM

C7720 2 50V 5% 402

C7780 2 10uF 20% X5R 6.3V 603

L7720 2 10UH-0.55A-330MOHM CRITICAL SOT23-5

R7780 2 22UF CRITICAL 20% 6.3V CERM 805 603

C7760 2 6.3V 10uF 20% X5R

C7762 2 10uF 20% X5R

R7781 2 6.3V X5R 20% 10uF 603 CRITICAL

U7760 2 TPS62202 SOT23-5 33

R7781 MCP_A01&MCP_A01P&MCP_A01Q =PP3V3_S5_P1V05S5_FB

=PP1V05_S5_REG

=PPVIN_S0_P1V8S0

=PP1V8_S0_REG

=PP1V8S0_EN P1V8S0_SW

=PP1V05_S5_EN

1V05S5_SGND

1V05S5_PGOOD

1V05S5_AVIN

8A3

8B4

8B5

8B8 64C1

8A3

64D6

64B1

Preliminary

www.vinafix.vn
Display Port Interoperability spec says that sources or sinks which are both DP and DVI must depend on the external adapter for pull ups on DDC lines (since DP or sinks which do both DP and DVI has the pull up on the DP side).
B

Q9440 must have Drain to Gate leakage of <500nA and Gate to Source resistance of >5MOhm pull-up to DP_PWR.

DisplayPort Connector

Port Power Switch

DP_ML_P<0> DP_ML_N<0>
DP_ML_C_P<0> DP_ML_C_N<0>

DP_ML_P<1> DP_ML_N<1>
DP_ML_C_P<1> DP_ML_C_N<1>

DP_ML_P<2> DP_ML_N<2>
DP_ML_C_P<2> DP_ML_C_N<2>

DP_PWR GND HDMI_CEC D9411

Q9440

DisplayPort Connector

Port Power Switch

DP_ML_P<0> DP_ML_N<0>
DP_ML_C_P<0> DP_ML_C_N<0>

DP_ML_P<1> DP_ML_N<1>
DP_ML_C_P<1> DP_ML_C_N<1>

DP_ML_P<2> DP_ML_N<2>
DP_ML_C_P<2> DP_ML_C_N<2>

DP_PWR GND HDMI_CEC D9411

Q9440

DisplayPort Connector

Port Power Switch
**CPU/FSB Constraints**

**CPU**

- **CPU_VCCSENSE**: 50 Ohm differential, with 7 mil spacing for VCCSense pair, Intel recommends routing with 7 mil spacing without specifying a target impedance.

**FSB**

- **FSB_CLK_CPU_N**: 100 Ohm differential, with 7 mil spacing for FSB_CLK_CPU_N pair, Intel recommends routing with 7 mil spacing without specifying a target impedance.

**MCP**

- **MCP_CPU_COMP**, **MCP_FSB_COMP**, **MCP_50S**, **MCP_BCLK_VML_COMP_GND**, **MCP_50S**, **MCP_8MIL**: 50 Ohm single-ended, with 7 mil spacing.

**Note**: Intel Design Guide allows closer spacing if signal lengths can be shortened.

**Spacing**

- **ADDR#**, **REQ#**: 1x dielectric between ADDR#, REQ#, with 2x dielectric spacing to ADSTB#.

**Intel Design Guide**

- Intel Design Guide recommends FSB signals be routed only on internal layers.

**ADTSB#s**: Matched within 20 ps.

**Intel Design Guide**

- Intel Design Guide allows closer spacing if signal lengths can be shortened.

**Intel Design Guide**

- Intel Design Guide recommends FSB signals be routed only on internal layers.

**FSB 2X**

- **FSB_DATA**
  - **FSB_DATA_GROUP0**: 50 Ohm single-ended, with 7 mil spacing for FSB_DATA pair.
  - **FSB_DATA_GROUP1**: 50 Ohm single-ended, with 7 mil spacing for FSB_DATA pair.

**NOTES**

- **NOTE**: Intel Design Guide allows closer spacing if signal lengths can be shortened.

**Physical Rules**

- **TOP, BOTTOM**
  - **FSB_DSTB**, **FSB_DSTB0**: 5x dielectric, with 7 mil spacing for FSB_DSTB pair.
  - **FSB_DSTB1**, **FSB_DSTB2**, **FSB_DSTB3**: 5x dielectric, with 7 mil spacing for FSB_DSTB pair.

**Table**

<table>
<thead>
<tr>
<th>Net Type</th>
<th>Size</th>
<th>Scale</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU_VCCSENSE</td>
<td>100</td>
<td>1</td>
</tr>
<tr>
<td>CPU_VCCSENSE_P</td>
<td>100</td>
<td>1</td>
</tr>
<tr>
<td>XDP_BPM_L&lt;4..0&gt;</td>
<td>10B3</td>
<td></td>
</tr>
<tr>
<td>XDP_BPM_L&lt;5..0&gt;</td>
<td>10B3</td>
<td></td>
</tr>
<tr>
<td>CPU_ITP</td>
<td>10B3</td>
<td></td>
</tr>
<tr>
<td>CPU_ITP</td>
<td>10B3</td>
<td></td>
</tr>
<tr>
<td>CPU_ITP</td>
<td>10B6</td>
<td></td>
</tr>
<tr>
<td>CPU_ITP</td>
<td>10B6</td>
<td></td>
</tr>
<tr>
<td>CPU_ITP</td>
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<tr>
<td>CPU_ITP</td>
<td>10D6</td>
<td></td>
</tr>
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<td>CPU_ITP</td>
<td>10C6</td>
<td></td>
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<td>CPU_ITP</td>
<td>10B6</td>
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<td>CPU_ITP</td>
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<td>10C6</td>
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<tr>
<td>CPU_ITP</td>
<td>10B6</td>
<td></td>
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<tr>
<td>CPU_ITP</td>
<td>10C6</td>
<td></td>
</tr>
<tr>
<td>CPU_ITP</td>
<td>10B6</td>
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<tr>
<td>CPU_ITP</td>
<td>10C6</td>
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<tr>
<td>CPU_ITP</td>
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<td></td>
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<tr>
<td>CPU_ITP</td>
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<td>CPU_ITP</td>
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<tr>
<td>CPU_ITP</td>
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<td></td>
</tr>
<tr>
<td>CPU_ITP</td>
<td>10B6</td>
<td></td>
</tr>
</tbody>
</table>
DDR3: MCP MEM COMP Signal Constraints

All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).

No DQS to clock matching requirement.
A/BA/cmd signals should be matched within 75 ps, no CLK matching requirement.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 140 ps.

Memory Net Properties

<table>
<thead>
<tr>
<th>Property</th>
<th>Value</th>
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<tbody>
<tr>
<td>Memory B_DQ_BYTE7</td>
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<tr>
<td>Memory B_DQ_BYTE3</td>
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<tr>
<td>MCP_MEM_COMP_GND</td>
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</tr>
<tr>
<td>Memory B_DQS_N&lt;6&gt;</td>
<td></td>
</tr>
<tr>
<td>Memory B_DQS_N&lt;5&gt;</td>
<td></td>
</tr>
<tr>
<td>Memory B_DQS5</td>
<td></td>
</tr>
<tr>
<td>Memory B_DQS4</td>
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</tr>
<tr>
<td>Memory B_DQS_N&lt;3&gt;</td>
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<tr>
<td>Memory B_DQS_N&lt;2&gt;</td>
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<tr>
<td>Memory B_DQS2</td>
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</tr>
<tr>
<td>Memory B_DQS_P&lt;2&gt;</td>
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<tr>
<td>Memory B_DQS1</td>
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<tr>
<td>Memory B_DQS_P&lt;0&gt;</td>
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</tr>
<tr>
<td>Memory B_DQ_BYTE6</td>
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<td>Memory B_DQ_BYTE5</td>
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<tr>
<td>MCP_40S</td>
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<tr>
<td>Memory B_DQ&lt;39..32&gt;</td>
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<tr>
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<tr>
<td>Memory B_DM&lt;6&gt;</td>
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<td>Memory B_DM&lt;4&gt;</td>
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<td>Memory B_DM&lt;2&gt;</td>
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<tr>
<td>Memory B_DQ_BYTE6</td>
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<tr>
<td>Memory B_DQ&lt;7..0&gt;</td>
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<tr>
<td>Memory B_CMD</td>
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<tr>
<td>Memory B_CAS_L</td>
<td></td>
</tr>
<tr>
<td>Memory B_RAS_L</td>
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<tr>
<td>Memory B_CMD</td>
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<td>Memory B_CMD</td>
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<tr>
<td>Memory B_CNTL</td>
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<td>MCP_40S_VDD</td>
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<td>Memory A_DQS_P&lt;7&gt;</td>
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<td>Memory A_DQS3</td>
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<td>Memory A_DQS_N&lt;2&gt;</td>
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<td>Memory A_DQS0</td>
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<td>MCP_70D_VDD</td>
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<td>Memory A_CMD</td>
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<td>Memory A_RAS_L</td>
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<td>Memory B_CLK_P&lt;5..0&gt;</td>
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<tr>
<td>Memory_70D_VDD</td>
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</tr>
</tbody>
</table>
SATA Interface Constraints

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

Max length of LVDS/DisplayPort/TMDS traces: 12 inches.

DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.4
### MCP Constraints

**PCI Bus Constraints**

<table>
<thead>
<tr>
<th>Source</th>
<th>Section</th>
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</thead>
<tbody>
<tr>
<td>MCP79 Interface DG (DG-03328-001_v0D)</td>
<td>2.11.1</td>
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**LPC Bus Constraints**

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**USB 2.0 Interface Constraints**

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**HDA Audio Interface Constraints**

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**SIO Signal Constraints**

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**SPI Interface Constraints**

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<th>Section</th>
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<tbody>
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<td>2.13.1</td>
</tr>
</tbody>
</table>

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**Electrical Constraint Sets**

- **Physical Rule Set**
- **Spacing Rule Set**
- **Lines to Line Spacing**

**Table of Physical Rules**

<table>
<thead>
<tr>
<th>Layer</th>
<th>Minimum Neck Width</th>
<th>Maximum Neck Length</th>
<th>Diffpair Primary Gap</th>
<th>Diffpair Neck Gap</th>
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</thead>
<tbody>
<tr>
<td></td>
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<td></td>
<td></td>
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</tbody>
</table>

**Table of Spacing Rules**

<table>
<thead>
<tr>
<th>Lines to Line Spacing</th>
<th>Layer</th>
<th>Spacing Rule Set</th>
<th>Weight</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
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<td></td>
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</tbody>
</table>

---

**References**

- MCP79 Interface DG (DG-03328-001_v0D)
- Section 2.11.1
- Section 2.12.1
- Section 2.13.1
- Section 2.13.1
- Section 2.13.1
**MCP RGMII (Ethernet) Constraints**

<table>
<thead>
<tr>
<th>Net Type</th>
<th>Min. Line Width</th>
<th>Allow Route</th>
<th>On Layer?</th>
</tr>
</thead>
</table>
| ENET_MDI | 100_OHM_DIFF    | =100_OHM_DIFF | =100_OHM_DIFF=
| ENET_RXD<3..0> | ENET_MII | ENET_MII_55S | ENET_MII |

<table>
<thead>
<tr>
<th>Net Type</th>
<th>Min. Line Width</th>
<th>Allow Route</th>
<th>On Layer?</th>
</tr>
</thead>
<tbody>
<tr>
<td>ENET_RXD&lt;0&gt;</td>
<td>ENET_MII</td>
<td>ENET_MII_55S</td>
<td>ENET_MII</td>
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</tbody>
</table>

**Ethernet Constraints**

<table>
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<th>On Layer?</th>
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</thead>
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| ENET_MDI | 100_OHM_DIFF    | =100_OHM_DIFF | =100_OHM_DIFF=
| ENET_RXD<3..0> | ENET_MII | ENET_MII_55S | ENET_MII |

<table>
<thead>
<tr>
<th>Net Type</th>
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<tr>
<td>ENET_RXD&lt;0&gt;</td>
<td>ENET_MII</td>
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<td>ENET_MII</td>
</tr>
</tbody>
</table>

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### SMC SMBus Net Properties

<table>
<thead>
<tr>
<th>Net Type</th>
<th>Min Width</th>
<th>Max Length</th>
<th>Min Gap</th>
</tr>
</thead>
<tbody>
<tr>
<td>SMBUS_SMC_B_S0_SCL</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
</tr>
<tr>
<td>SMBUS_SMC_B_S0_SDA</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
</tr>
<tr>
<td>SMBUS_SMC_0_S0_SCL</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
</tr>
<tr>
<td>SMBUS_SMC_0_S0_SDA</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
</tr>
<tr>
<td>SMBUS_SMC_BSA_SCL</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
</tr>
<tr>
<td>SMBUS_SMC_BSA_SDA</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
</tr>
<tr>
<td>SMBUS_SMC_A_S3_SCL</td>
<td>0.1 MM</td>
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<td>0.1 MM</td>
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<tr>
<td>SMBUS_SMC_A_S3_SDA</td>
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### SMBus Charger Net Properties

<table>
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<th>Max Length</th>
<th>Min Gap</th>
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</thead>
<tbody>
<tr>
<td>CHGR_CSI_N</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
</tr>
<tr>
<td>CHGR_CSI_P</td>
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<td>0.1 MM</td>
</tr>
<tr>
<td>CHGR_CSO_P</td>
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<td>0.1 MM</td>
</tr>
<tr>
<td>CHGR_CSO_N</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
</tr>
</tbody>
</table>

### SMC Constraints

- **SYNC_MASTER**: T18_MLB
- **SYNC_DATE**: 01/04/2008

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DRAWING NUMBER

SIZE

D

M97 SENSOR NET PROPERTIES

NET_TYPE

ELECTRICAL_CONSTRAINT_SET PHYSICAL SPACING

DIFFPAIR = STANDARD = STANDARD 0.1 MM 0.1 MM

SYNC_MASTER = M97_MLB

M97 SPECIAL CONSTRAINTS

ISNS_CPUVTT_N

DIFFPAIR

ISNS_P1V5S0MCP_P

DIFFPAIR

ISNS_P1V5S0MCP_N

DIFFPAIR

ISNS_PVCORES0MCP_P

DIFFPAIR

ISNS_PVCORES0MCP_N

DIFFPAIR

MCPTHMSNS_D2_P

DIFFPAIR

MCPTHMSNS_D2_N

DIFFPAIR

CPUTHMSNS_D2_P

DIFFPAIR

CPUTHMSNS_D2_N

DIFFPAIR

CHGR_CSO_R_N

DIFFPAIR

CHGR_CSO_R_P

DIFFPAIR

MCP_THMDIODE_N

DIFFPAIR

MCP_THMDIODE_P

DIFFPAIR

CPU_THERMD_N

DIFFPAIR

CPU_THERMD_P

DIFFPAIR

M97 SENSOR NET PROPERTIES

M97 SENSOR NET PROPERTIES