**FLASH ROM**

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**Strap Name** | **Pin Straps description** | **Default Value**
--- | --- | ---
**TX_PWR_ENABLE** | GPIO0 | 0 - 50% Tx output swing for mobile mode
1 - Full Tx output swing (Default setting for Desktop)**

**TX_DEEMPH_ENABLE** | GPIO1 | 0 - Tx de-emphasis disabled for mobile mode
1 - Tx de-emphasis enabled (Default setting for Desktop)**

**BIF_GEN2_ENABLE** | GPIO2 | 0 - Advertises the PCI-E device as 2.5 GT/s capable at power-on.
1 - Advertises the PCI-E device as 5.0 GT/s capable at power-on.
5.0 GT/s capability will be controlled by software.

**STRAP_BIF_CLK_PM_ENABLE** | GPIO8 | 0 - CLKREQ# power management capability is disabled
1 - CLKREQ# power management capability is enabled

**CONFIG[3]** | GPIO9 | 000 = 128MB
001 = 256MB
010 = 64MB
011 = 32MB
100 = 512MB
101 = 1GB
110 = 2GB
111 = 4GB**

**BIOS_ROM_ENABLE** | GPIO22 | 0 - Disable external BIOS ROM device
1 - Enable external BIOS ROM device

**AUD[0]** | VSYNC | 0 - No audio function;
01 - Audio for DisplayPort and HDMI if adapter is detected;
10 - Audio for DisplayPort only;
11 - Audio for both DisplayPort and HDMI.

**AUD[1]** | HSYNC | 0 - Audio must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.

**VIP_DEVICE_STRIP_DIS** | V2SYNC | If VIP_DEVICE_STRIP_DIS is set to '0', then this pin is not used as a strap at all (i.e. its value during reset is unimportant), and it can be used as a regular GPIO.
VDDCI REGULATOR 1.1V @ 15A

- DNI
- Overlapped with 10uf Input Caps

Top and bottom as mirror image

Current Limit = 25A
### Title
M97 1GB GDDR5 Dell Reebok

### Schematic No.
105-B779xx-10

### Date:
Friday, September 04, 2009

### REVISION HISTORY

<table>
<thead>
<tr>
<th>Sch Rev</th>
<th>PCB Rev</th>
<th>Date</th>
<th>Description</th>
</tr>
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<tr>
<td>0</td>
<td>00A</td>
<td>10/08/08</td>
<td>Original Design for NIKE System</td>
</tr>
<tr>
<td>0</td>
<td>00B</td>
<td>01/14/09</td>
<td>Added Regulator for VDDCI</td>
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<td></td>
<td></td>
<td></td>
<td>Added 0ohm resistors close ASIC on SMBUS</td>
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<tr>
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<td></td>
<td>Added new CTF circuit</td>
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<tr>
<td>0</td>
<td>00C</td>
<td>02/24/09</td>
<td>Added Caps for LCDVCC</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>added Snubber for 1.8V</td>
</tr>
<tr>
<td>0</td>
<td>00E</td>
<td>09/03/09</td>
<td>Changed to drive the ADM1032 device (and its related pull-ups) with 3Vsus instead of 3Vrun for Reebok</td>
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### NOTE:
This schematic represents the PCB, it does not represent any specific SKU.

For Stuffing options (component values, DNI’s, …) please consult the product specific BOM.

Please contact AMD representative to obtain latest BOM closest to the application desired.

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M97 1GB GDDR5 Dell Reebok

Friday, September 04, 2009

Original Design for NIKE System

01/14/09 Added Regulator for VDDCI
- Added 0ohm resistors close ASIC on SMBUS
- Added new CTF circuit

02/24/09 Added Caps for LCDVCC
- added Snubber for 1.8V

09/03/09 Changed to drive the ADM1032 device (and its related pull-ups) with +3Vsus instead of +3Vrun for Reebok

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