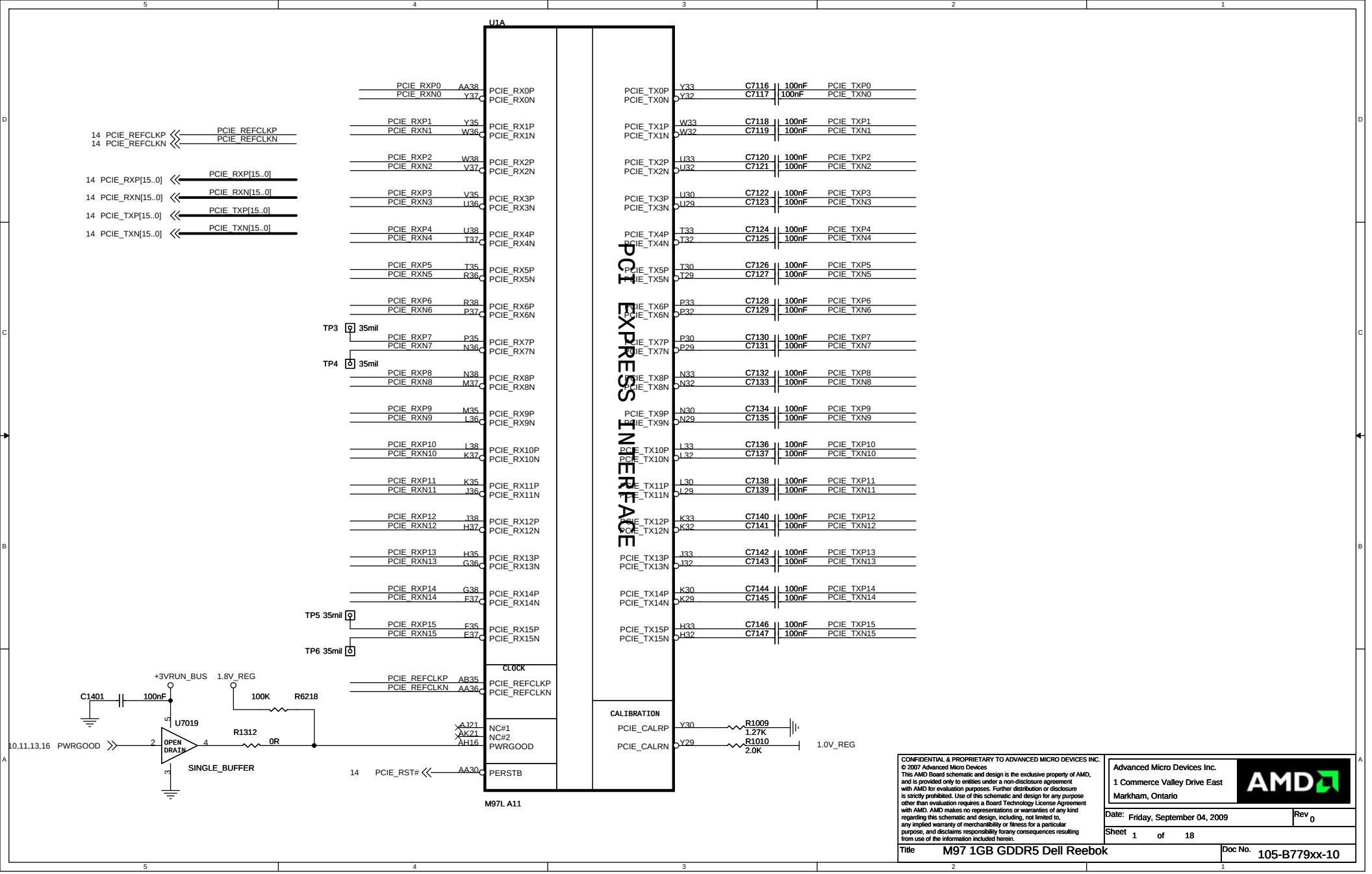

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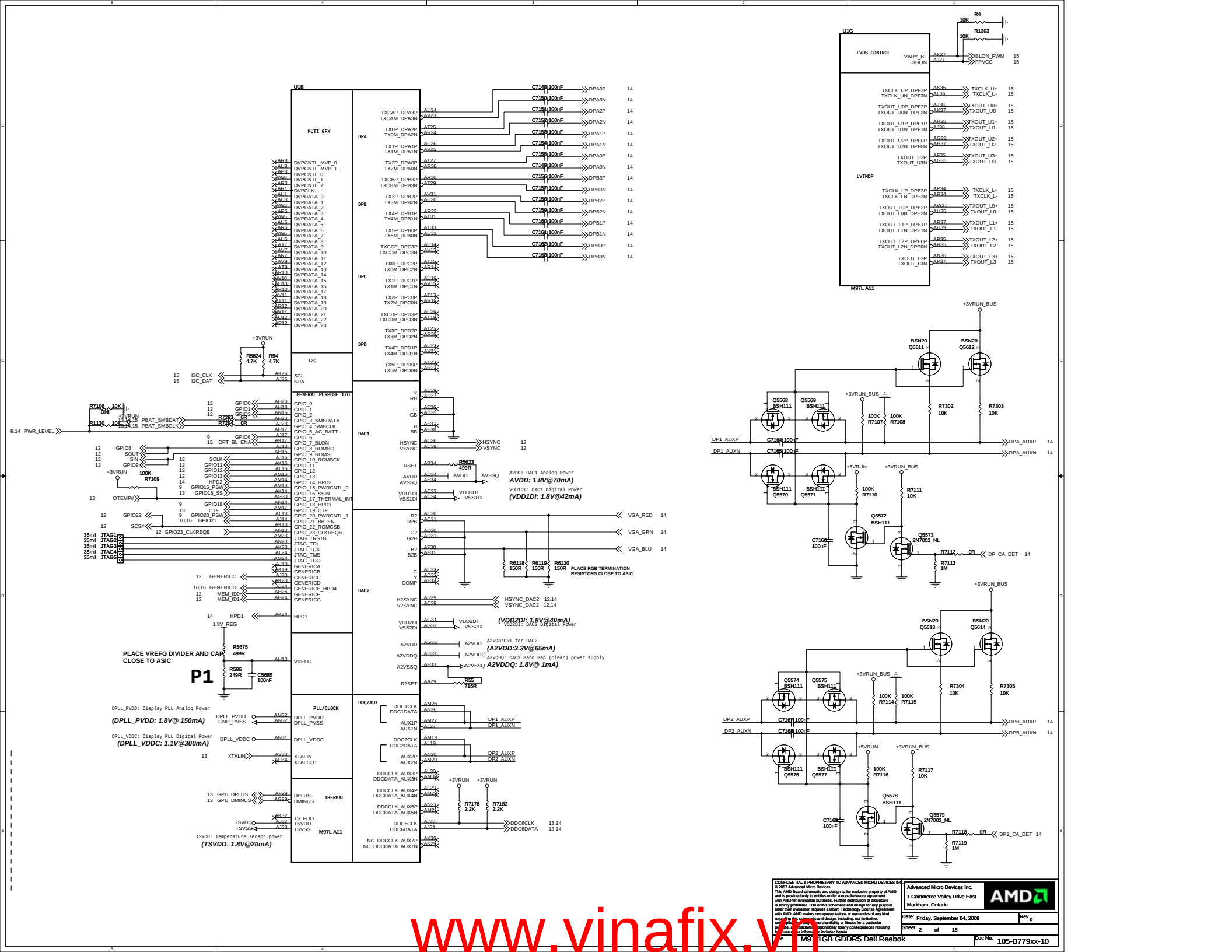
Sheet 1 of 18

Title M97 1GB GDDR5 Dell Reebok

Doc No. 105-B779xx-10



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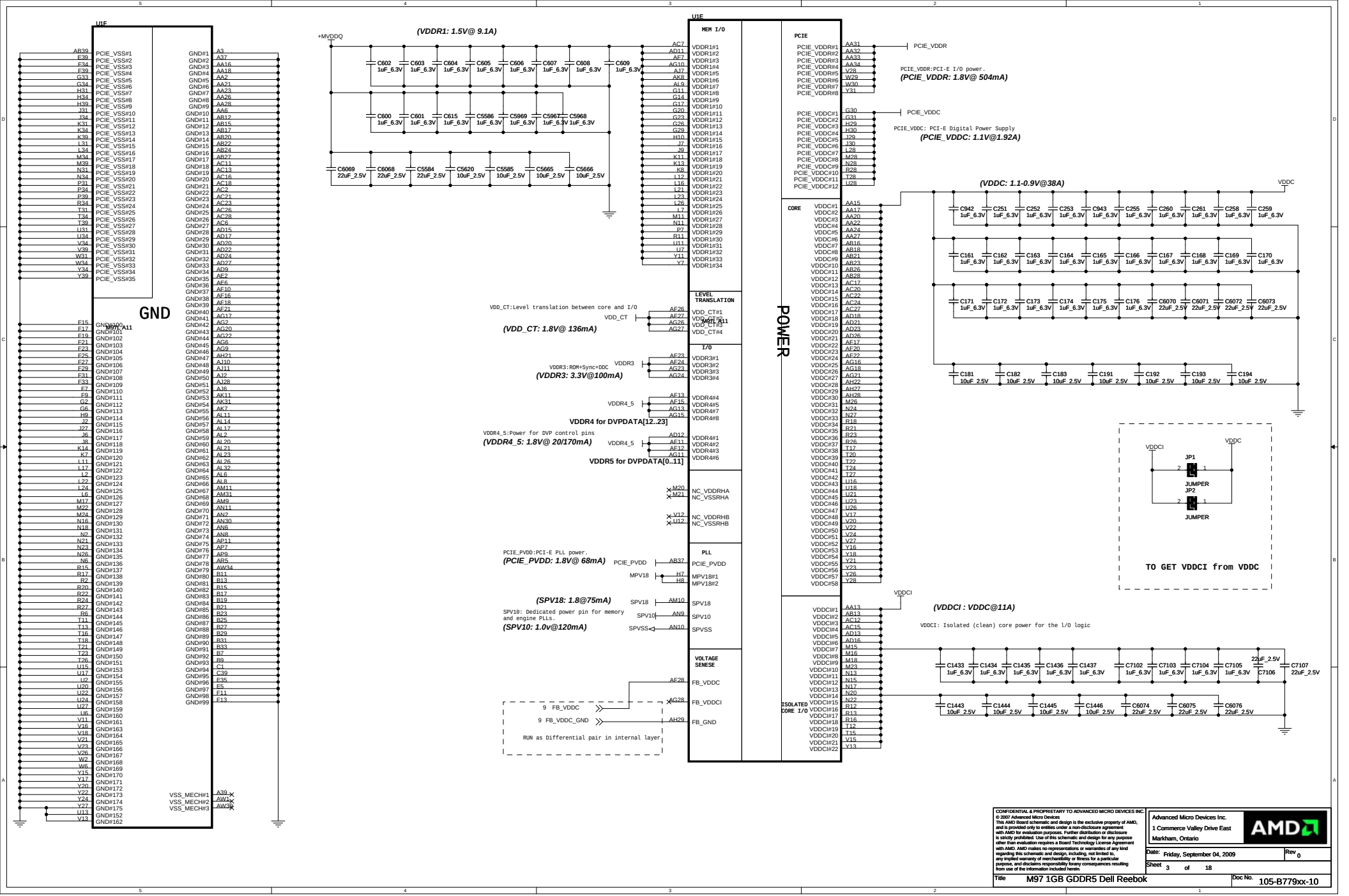

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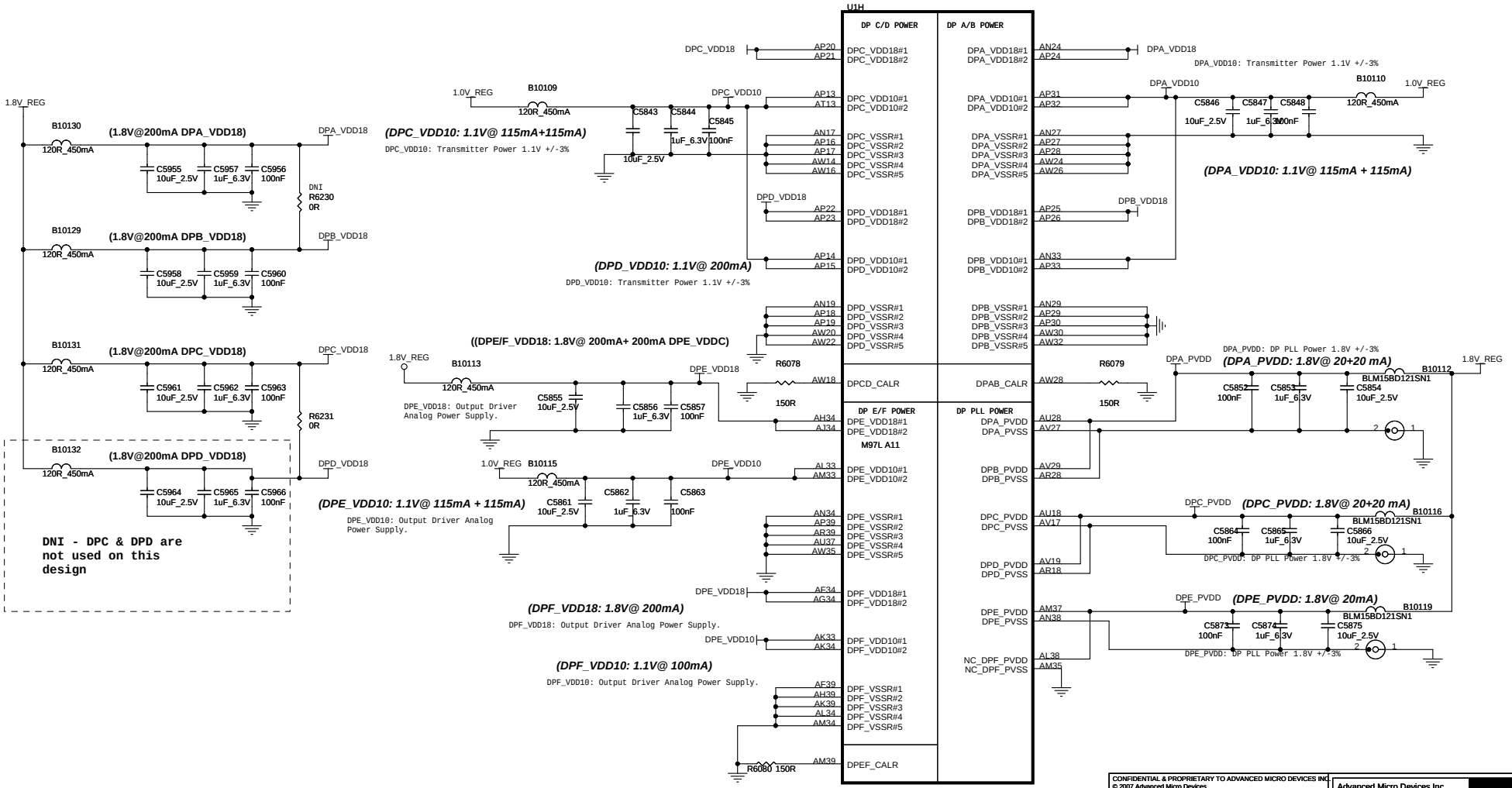

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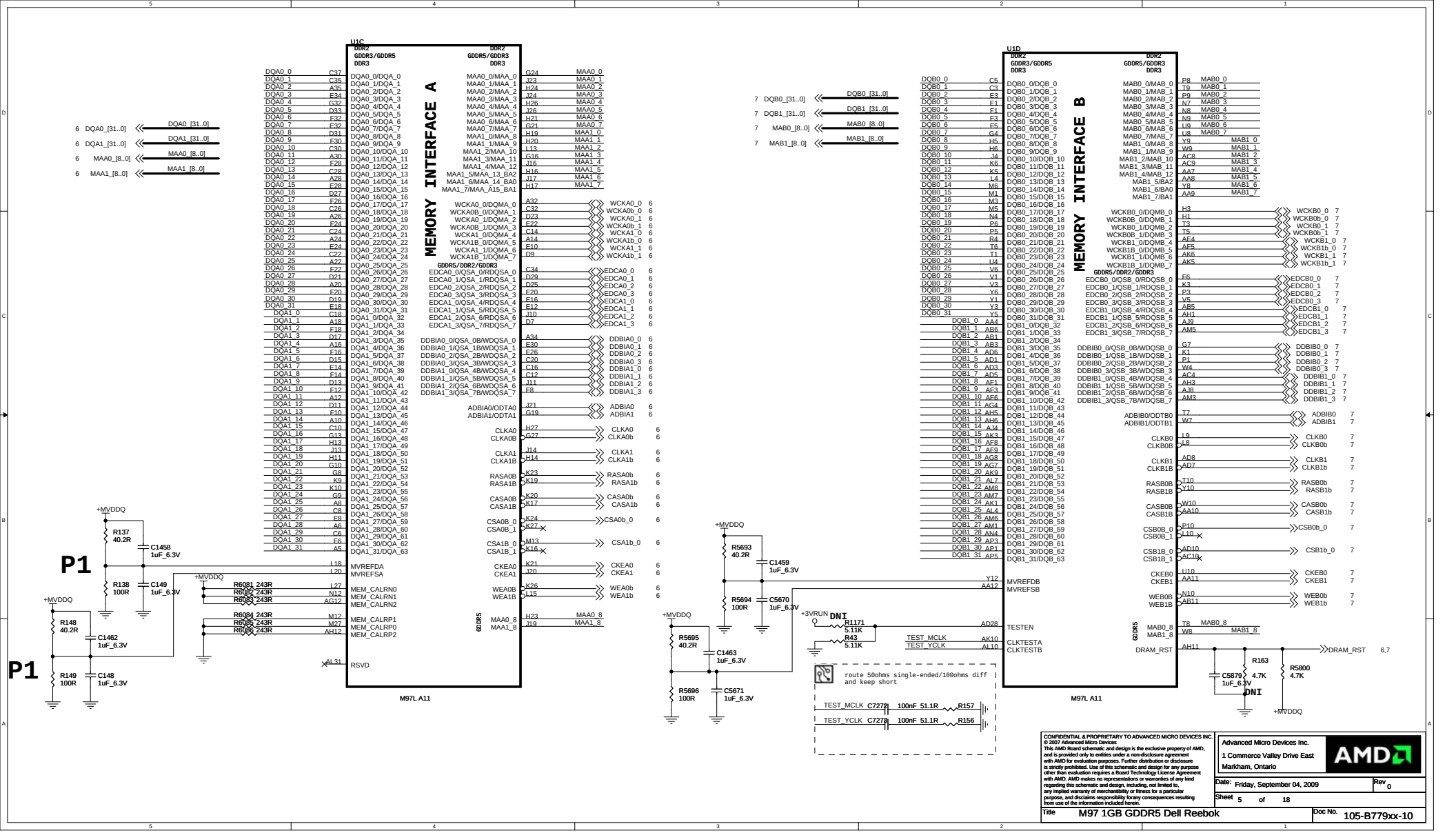

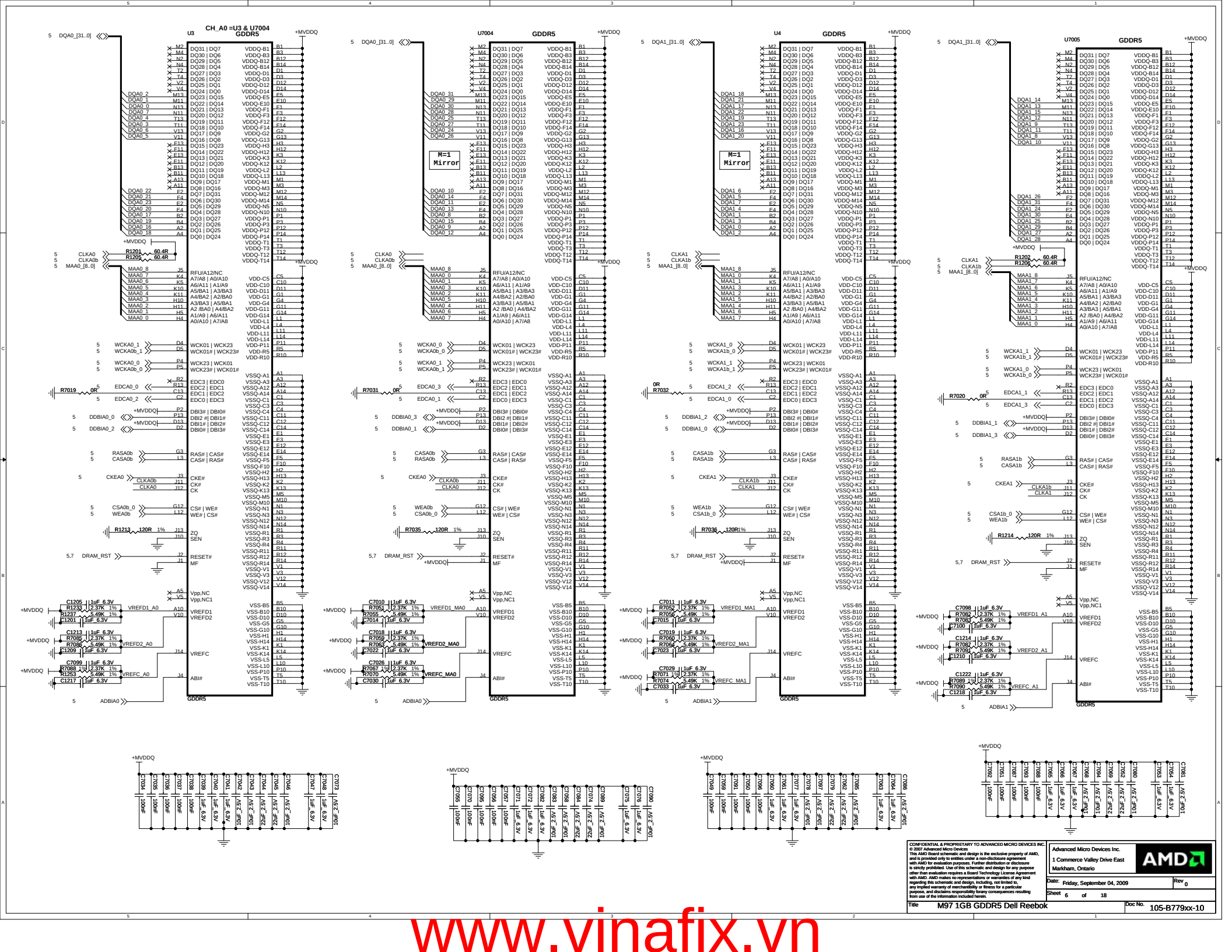

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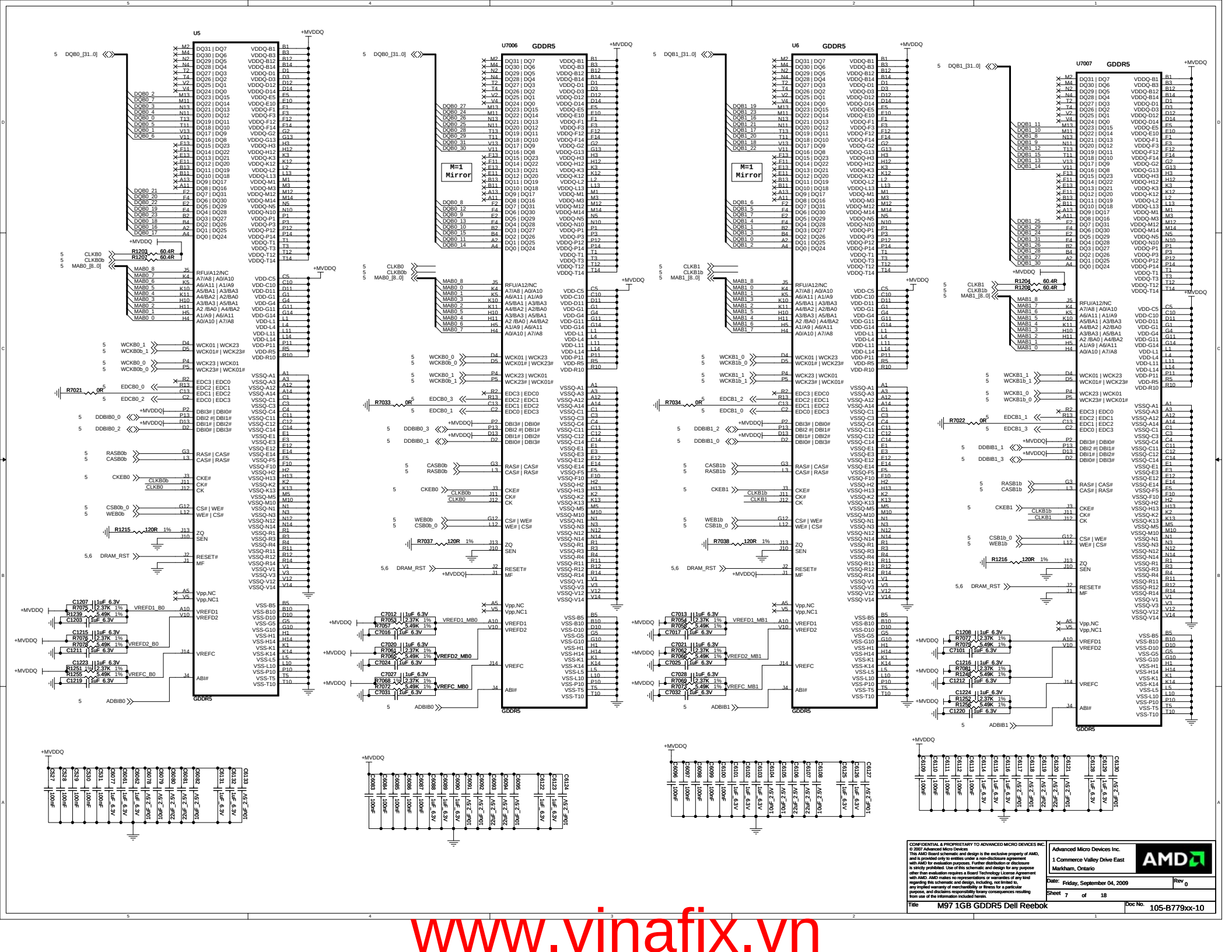

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1.8V_REG

B10122 BLM15BD121SN1 — TSVDD
TSVDD: Temperature sensor power
(TSVDD: 1.8V@20mA)
C5923 10uF_2.5V, C5924 1uF_6.3V
TSVSS

B29 BLM15BD121SN1 — AVDD
(65mA 1.8V AVDD) AVDD: DAC1 Analog Power
(DAC1_AVDD: 1.8V@70mA)
P1: C1325 1uF_6.3V
AVSSQ

B30 BLM15BD121SN1 — VDD1DI
VDD1DI: DAC1 Digital Power
(VDD1DI: 1.8V@42mA)
P2: C6059 1uF_6.3V
VSS1DI

B10063 BLM15BD121SN1 — A2VDDQ
A2VDDQ: DAC2 Band Gap (clean) power supply
(A2VDDQ: 1.8V@ 1mA)
P1: C5627 1uF_6.3V, C5628 100nF
A2VSSQ

B10064 BLM15BD121SN1 — VDD2DI
VDD2DI: DAC2 Digital Power
(VDD2DI: 1.8V@40mA)
P2: C5708 10uF_2.5V, C5610 1uF_6.3V, C36 100nF
VSS2DI

B10100 BLM15BD121SN1 — VDD_CT
(150mA 1.8V VDD_CT)
VDD_CT:Level translation between core and I/O
(VDD_CT: 1.8V@ 136mA)
P1: C5824 10uF_2.5V, C5821 1uF_6.3V, C5826 100nF

B10101 BLM15BD121SN1 — VDDR4_5
(300mA 1.8V VDDR4_5)
VDDR4_5:Power for DVP control pins
(VDDR4_5: 1.8V@ 20/170mA)
P3: C5829 100nF, C5932 1uF_6.3V, C7114 10uF_2.5V

L115 470R_1000mA — PCIE_VDDR
PCIE_VDDR:PCI-E I/O power.
(PCIE_VDDR: 1.8V@ 500mA)
P2: C5802 10uF_2.5V, C5800 1uF_6.3V, C5929 1uF_6.3V, C5928 10uF_2.5V

B10105 BLM15BD121SN1 — PCIE_PVDD
PCIE_PVDD:PCI-E PLL power.
(PCIE_PVDD: 1.8V@ 40mA)
P1: C5832 10uF_2.5V, C5833 1uF_6.3V, C5834 100nF

B10098 470R_1000mA — DPLL_PVDD
(40mA 1.8V DPLL_PVDD)
DPLL_PVDD: Display PLL Analog Power
(DPLL_PVDD: 1.8V@ 150mA)
P1: C5784 10uF_2.5V, C5785 1uF_6.3V, C5786 100nF
GND_PVSS

(1.8V@75mA SPV18)
B10127 BLM15BD121SN1 — SPV18
SPV18: Dedicated Analog power pin for PLL .
P1: C5947 10uF_2.5V, C5948 1uF_6.3V, C5949 100nF
SPVSS

B10128 470R_1000mA (1.8V@500mA MPV18) — MPV18
MPV18: Dedicated power pin for MPLL .
P1: C7115 10uF_2.5V, C5950 10uF_2.5V, C5951 1uF_6.3V, C5954 100nF

1.0V_REG

P1: C983 100nF, C972 100nF, C5927 1uF_6.3V, C5930 1uF_6.3V, C973 1uF_6.3V, C1668 10uF_2.5V
PCIE_VDDC
PCIE_VDDC: PCI-E Digital Power Supply
(PCIE_VDDC: 1.1V@2.0A)

B10099 470R_1000mA
P1: C5787 10uF_2.5V, C6067 1uF_6.3V, C5789 100nF
DPLL_VDDC
DPLL_VDDC: Display PLL Digital Power
(DPLL_VDDC: 1.1V@300mA)
GND_PVSS

1.0V_REG

B10124 120R_450mA — SPV10
SPV10: Dedicated power pin for SPLL,UVD PLLs.
(SPV10: VDDC@120mA)
P1: C5694 10uF_2.5V, C45 1uF_6.3V, C5614 100nF
SPVSS

+3VRUN

B10061 BLM15BD121SN1 — A2VDD
A2VDD:CRT for DAC2
(A2VDD:3.3V@65mA)
P1: C5706 10uF_2.5V, C31 1uF_6.3V

B27 BLM15BD121SN1 — VDDR3
VDDR3:ROM+Sync+DDC
(VDDR3: 3.3V@60mA)
P2: C5591 10uF_2.5V, C5592 1uF_6.3V

For Placement: P1 is Priority 1, P2 Second Priority and so on.....

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Title: 1GB GDDR5 DDR3 Reebok | Doc No. 105-B779xx-10

GPIO18	GPIO6	GPIO20	GPIO15	
VID5	VID4	VID3	VID2	VDDC
0	1	0	1	1.250V
0	1	1	0	1.200V
0	1	1	1	1.150V
1	0	0	0	1.100V
1	0	0	1	1.050V
1	0	1	0	1.000V
1	0	1	1	0.950V
1	1	0	0	0.900V
1	1	0	1	0.850V
1	1	1	0	0.800V
1	1	1	1	0.750V

4.7Uf X6S overlapped with 10uf input Caps for PMW1 — DNI — C7275 C7276 C7277 C7278 C7279 4.7UF_25V

4.7Uf X6S : overlapped with 10uf input Caps for PMW3 — DNI — C7280 C7281 C7282 C7283 4.7UF_25V

4.7Uf X6S : overlapped with 10uf input Caps for PMW2 — DNI — C7284 C7285 C7286 C7288 4.7UF_25V

Place R238 close to the pin — use 147K (3160147300G)

RT2 s/b placed close to phase 1 ouput inductor

MPL73-R33 LF INDUCTOR 0.33uH 20% Irms=20A, Isat=30A, DCR=3.9mR — 470Uf, 9mohm

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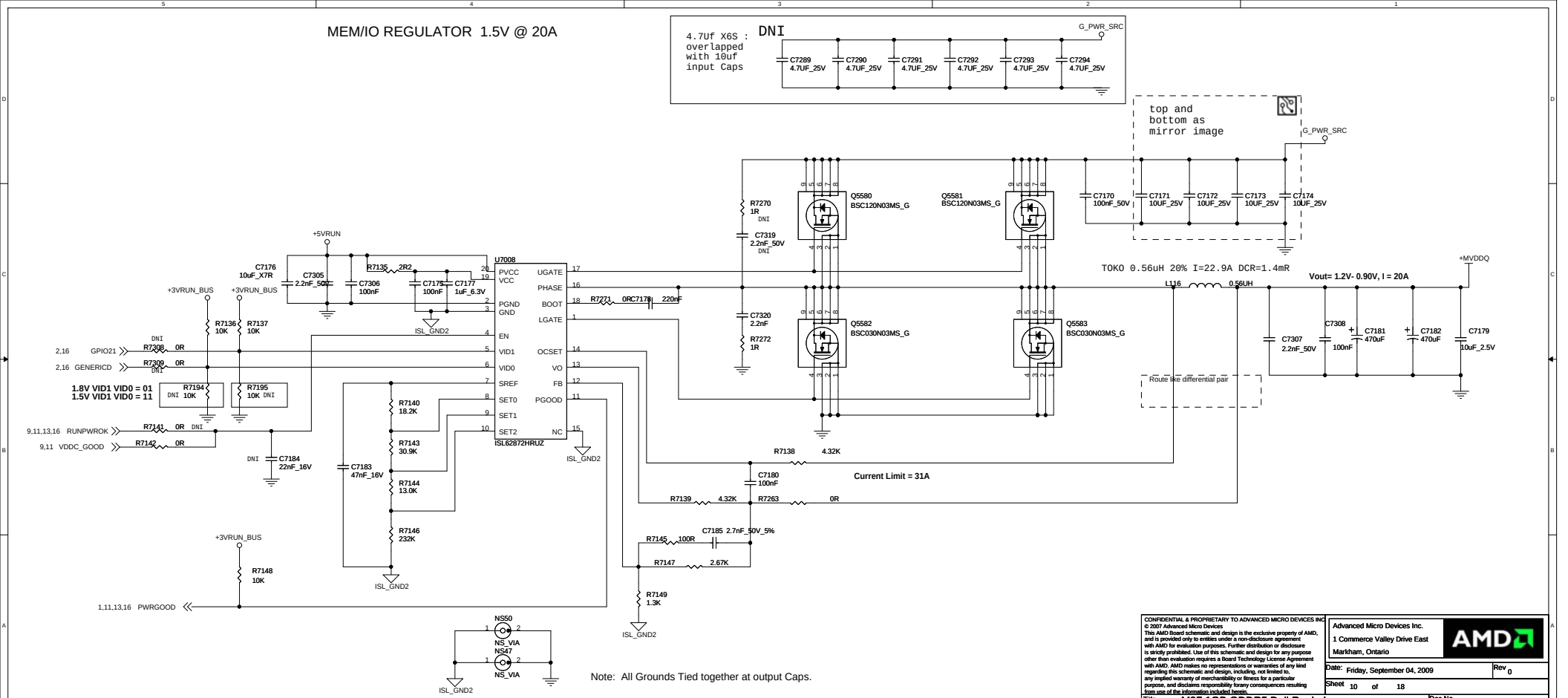
MEM/IO REGULATOR 1.5V @ 20A



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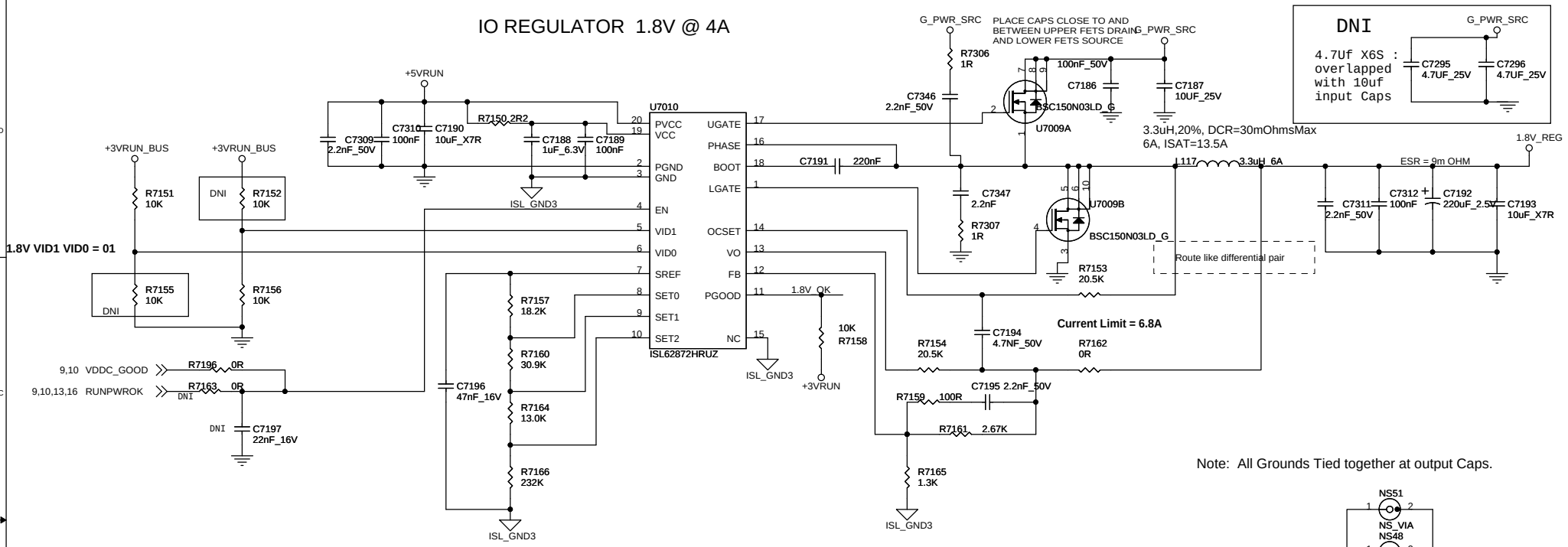
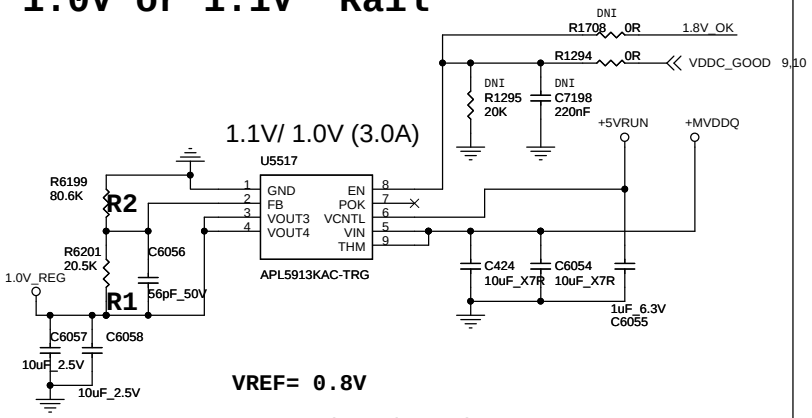
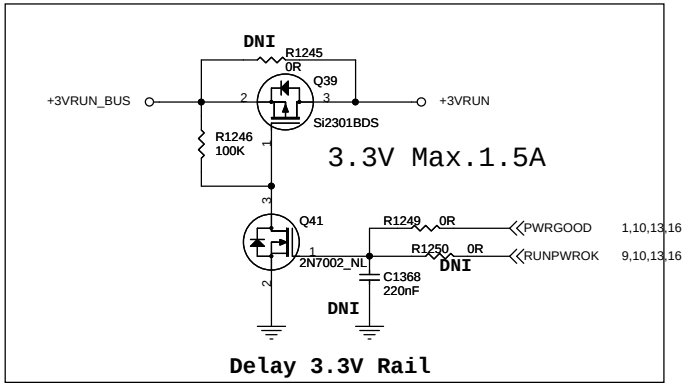
IO REGULATOR 1.8V @ 4A



1.0V or 1.1V Rail





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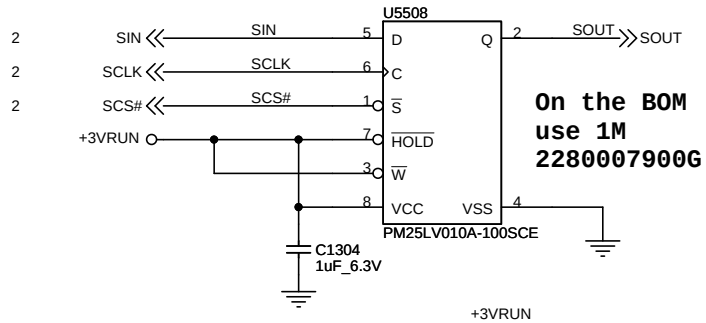
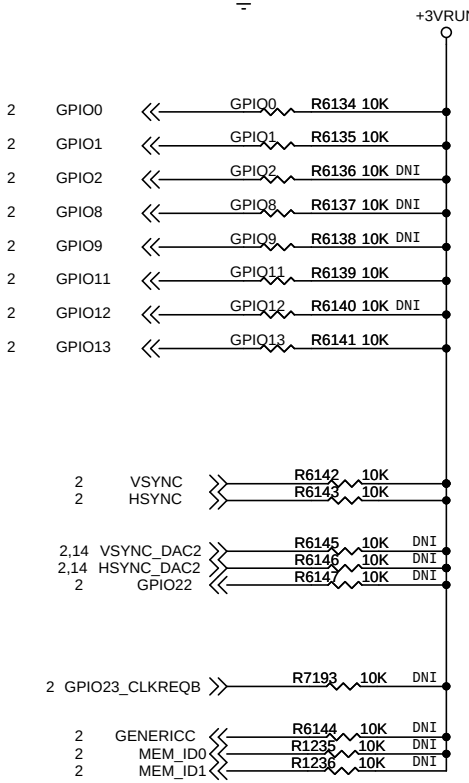
FLASH ROM



On the BOM use 1M 2280007900G



Strap Name		Pin Straps description	Default Value
TX_PWRS_ENB	GPIO0	**Transmitter Power Savings Enable** 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	**PCI Express Transmitter De-emphasis Enable** 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN	GPIO2	0 = Advertises the PCI-E device as 2.5 GT/s capable at power-on. 1 = Advertises the PCI-E device as 5.0 GT/s capable at power-on. 5.0 GT/s capability will be controlled by software.	0
STRAP_BIF_CLK_PM_EN	GPIO8	Enable CLKREQ# Power Management 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0
CONFIG[3] CONFIG[2] CONFIG[1] CONFIG[0]	GPIO9 GPIO13 GPIO12 GPIO11	GPIO9,13,12,11 (config 3,2,1,0): a> If BIOS_ROM_EN = 1, then Config[3:0] defines the ROM Type: b> If BIOS_ROM_EN = 0, then Config[3:0] defines the Aperture size:Size of the primary memory apertures claimed in PCI configuration space 000 = 128MB 001 = 256MB 010 = 64MB 011 = 32MB 100 = 512MB 101 = 1GB 110 = 2GB 111 = 4GB	0101
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0 - Disable external BIOS ROM device 1 - Enable external BIOS ROM device	0
AUD[0]	VSYNC	AUD[1:0]: 00 - No audio function; 01 - Audio for DisplayPort and HDMI if adapter is detected; 10 - Audio for DisplayPort only; 11 - Audio for both DisplayPort and HDMI. HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	1
AUD(1)	HSYNC		1
VIP_DEVICE_STRAP_DIS	V2SYNC	If VIP_DEVICE_STRAP_EN is set to '1', then this pin is used to sense whether a VIP slave device is connected to the VIP Host interface. If VIP_DEVICE_STRAP_EN is set to '0', then this pin is not used as a strap at all (i.e. its value during reset is unimportant), and it can be used as a regular GPIO	0
SMS_EN_HARD	H2SYNC		0
Reserve	GENERICC		0

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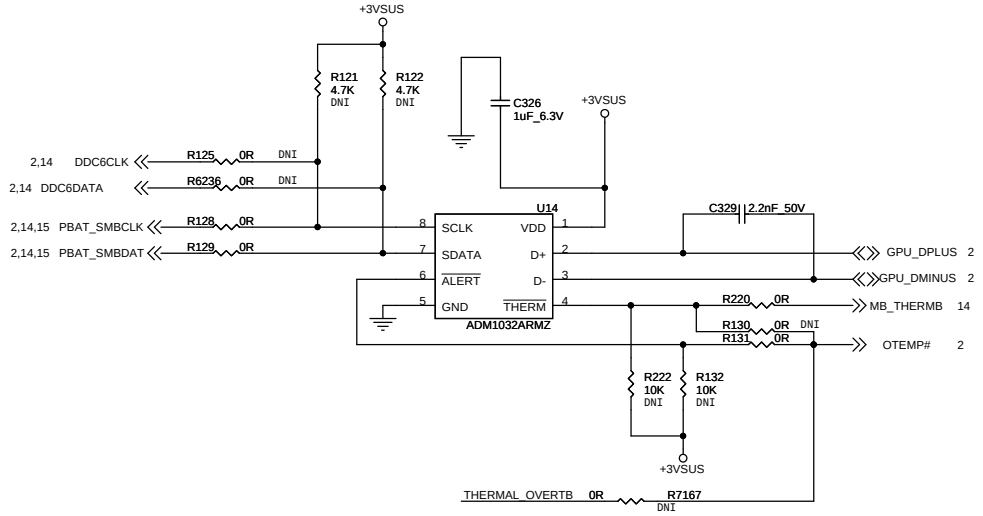

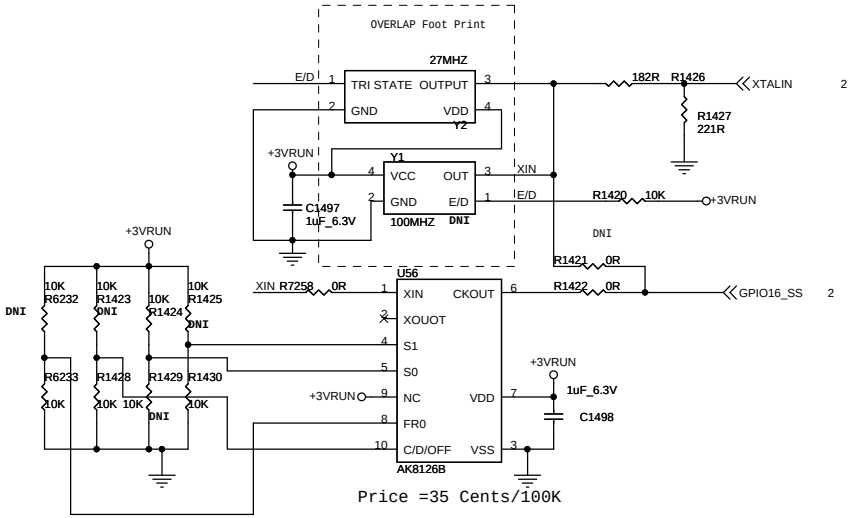

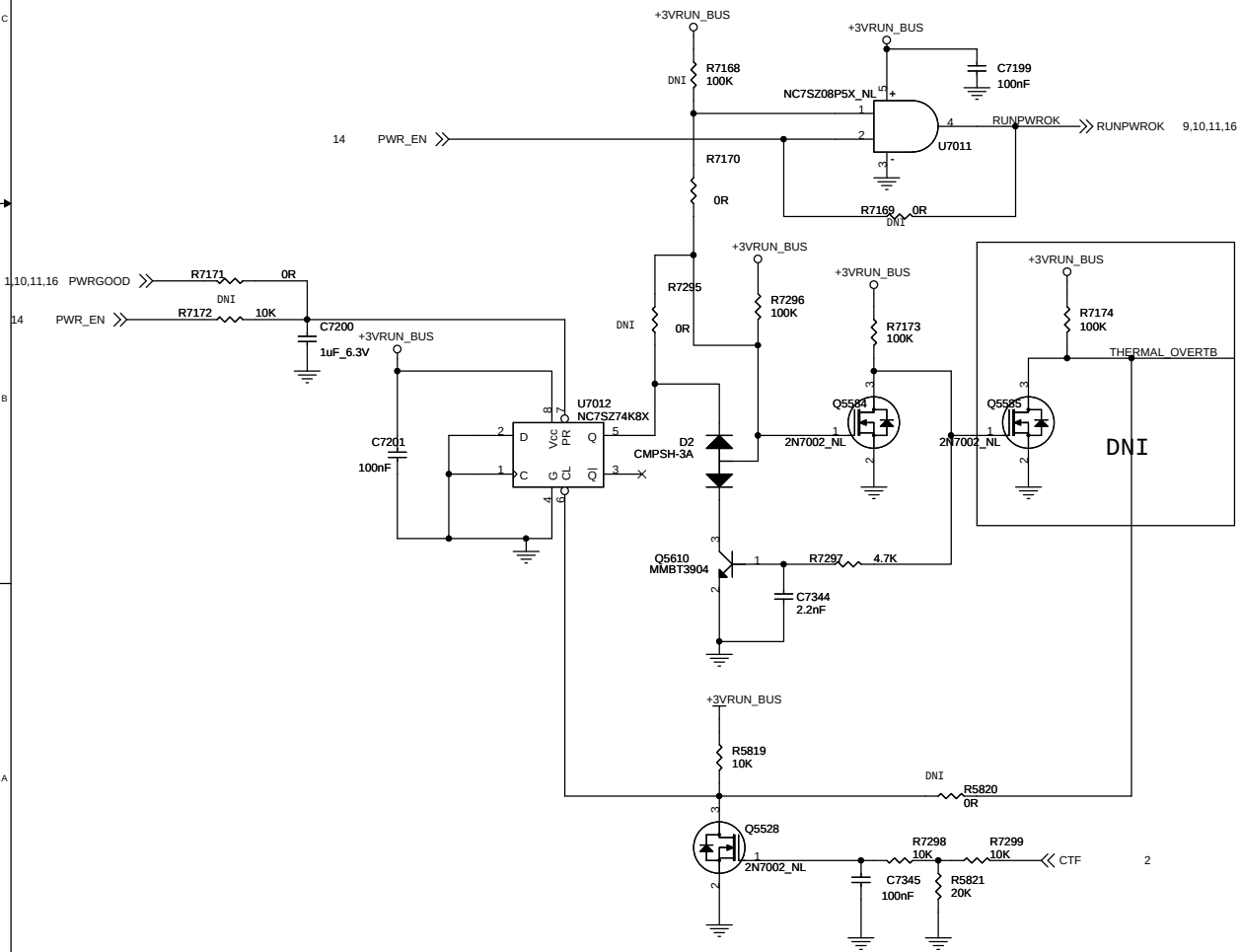

Pin Setting C/D/OFF	Modulation Mode
L	Down Spread
M	No Modulation
H	Center Spread

Pin Setting FR0	Input Frequency (MHz)	Output Frequency (MHz)
L	90 – 128	90 – 128
H	24.3 – 32.4	90 – 120

Pin Setting		Modulation Ratio (%)	
S1	S0	Center Spread Mode	Down Spread Mode
L	L	± 0.5	-1.0
L	H	± 0.25	- 0.5
H	L	± 1.0	-2.0
H	H	± 1.5	- 3.0

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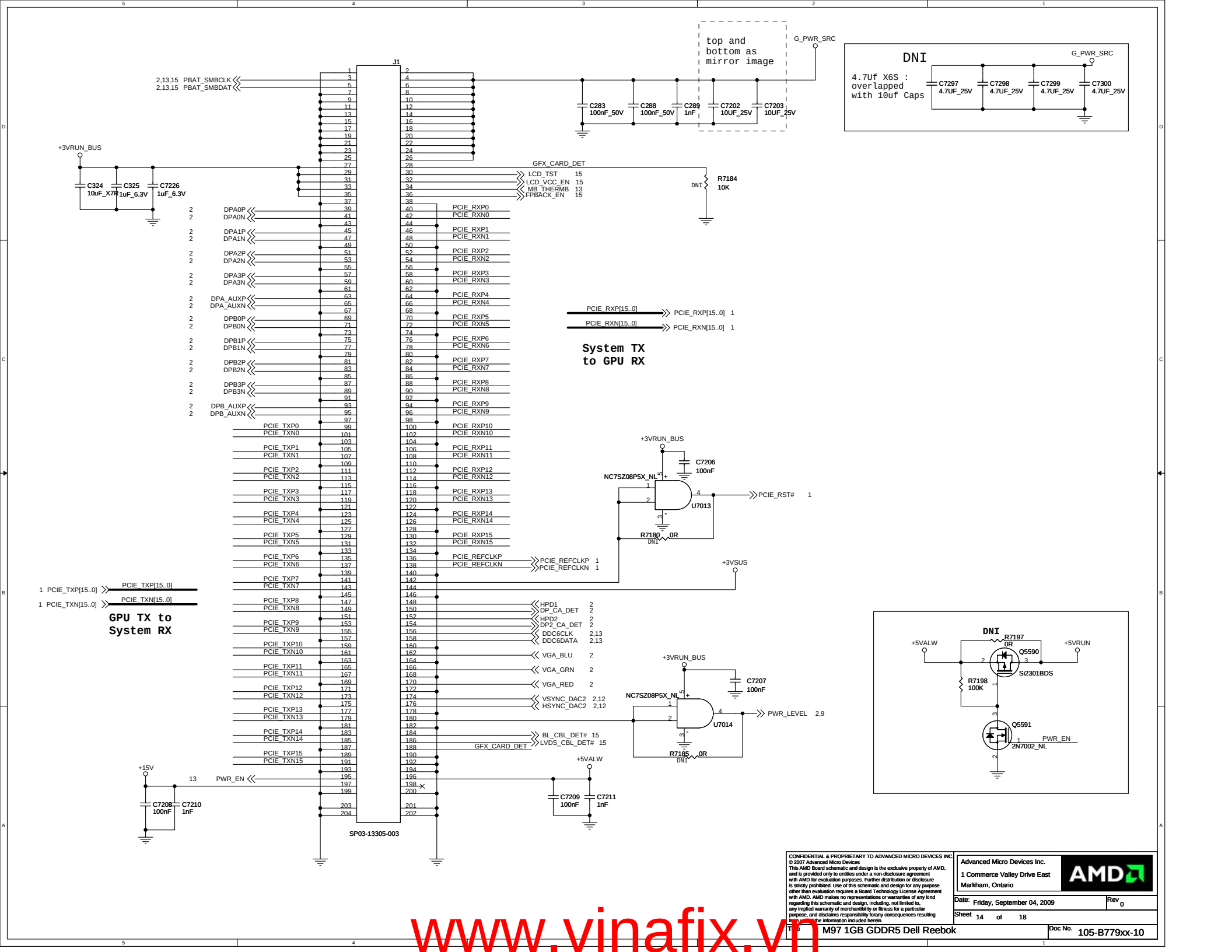

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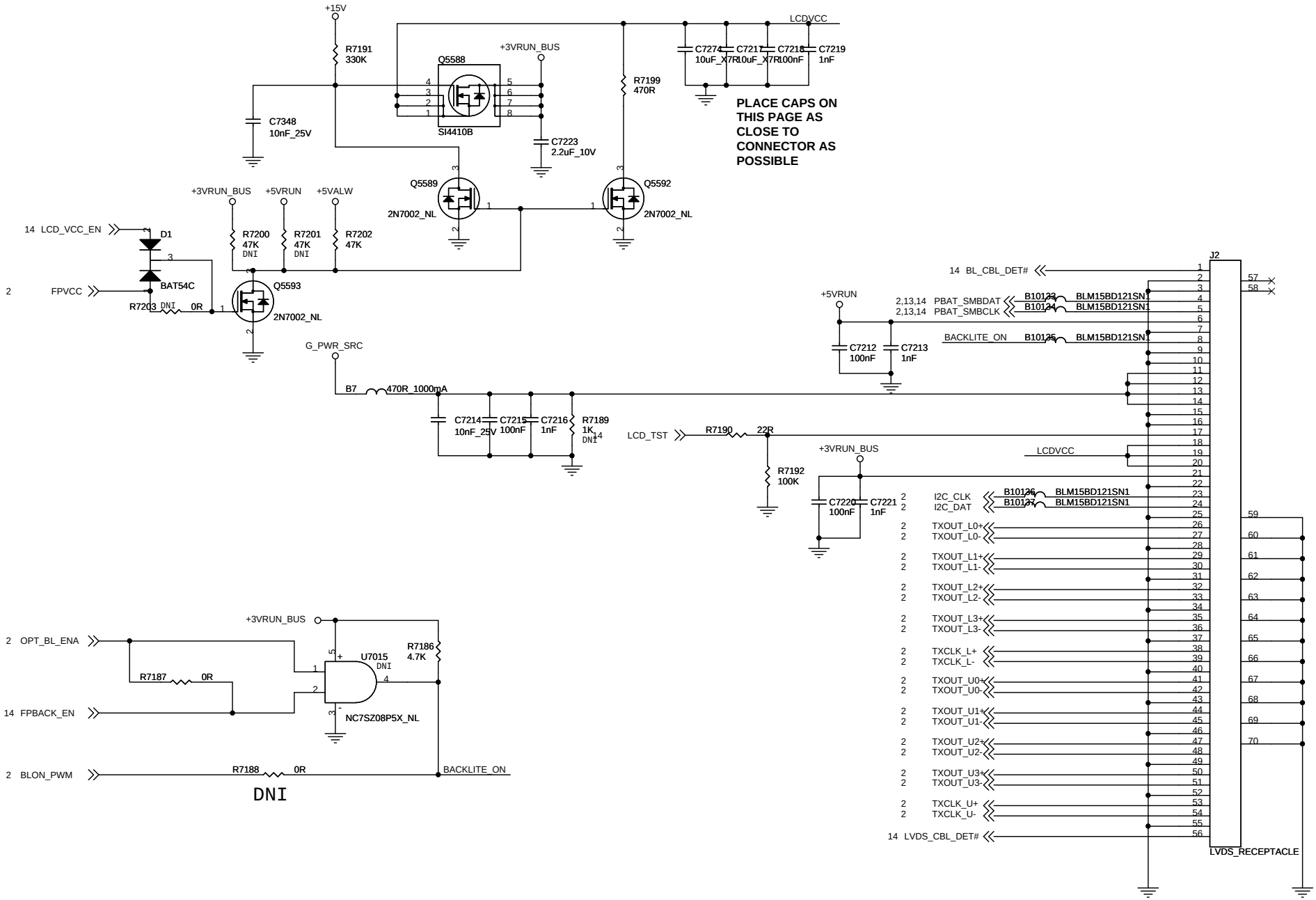

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VDDCI REGULATOR 1.1V @ 15A

VID1	VID0	VDDC
1	1	0.92V
0	1	1.02V
1	0	1.12V
0	0	1.22V

4.7Uf X6S : overlapped with 10uf input Caps

DNI

G_PWR_SRC

C7321 4.7UF_25V
C7322 4.7UF_25V
C7323 4.7UF_25V
C7324 4.7UF_25V

top and bottom as mirror image

G_PWR_SRC

C7325 100nF_50V
C7326 10UF_25V
C7327 10UF_25V

+5VRUN

C7329 10uF_X7R
C7330 2.2nF_50V
C7331 100nF
R7274 2R2
C7332 100nF
C7333 1uF_6.3V

U7020

ISL62872HRUZ

PVCC
VCC
PGND
GND
EN
VID1
VID0
SREF
SET0
SET1
SET2
UGATE
PHASE
BOOT
LGATE
OCSET
VO
FB
PGOOD
NC

VDDCI_GND

+3VRUN_BUS
+3VRUN_BUS

R7276 10K
R7277 10K DNI

2,10 GPIO21
R7300 0R DNI
2,10 GENERICD
R7301 0R DNI
R7279 10K DNI
R7280 10K

9,10,11,13 RUNPWROK
R7292 0R

R7281 32.4K
R7283 26.7K
C7341 47nF_16V
R7285 22.1K
R7288 249K

1,10,11,13 PWRGOOD

R7273 1R DNI
C7328 2.2nF_50V DNI
C7339 2.2nF
R7278 1R

Q5606 BSZ100N03MS G
Q5607 BSZ100N03MS G
Q5608 BSZ035N03MS G
Q5609 BSZ035N03MS G

R7275 0R
C7334 220nF

0.82uH 20% Irms=13A, Isat=24A, DCR=6.8mR

L121 .82uH

Vout= 1.1V- 1V, I = 15A

VDDCI

C7335 2.2nF_50V
C7336 100nF
C7337 470uF
C7338 470uF
C7340 10uF_2.5V

Route like differential pair

R7284 16.9K

Current Limit = 25A

C7342 6.8nF_25V
R7286 16.9K
R7287 0R

R7289 100R
C7343 2.7nF_50V_5%
R7291 2.49K
R7292 3.09K

NS52 NS_VIA
NS53 NS_VIA

Note: All Grounds Tied together at output Caps.

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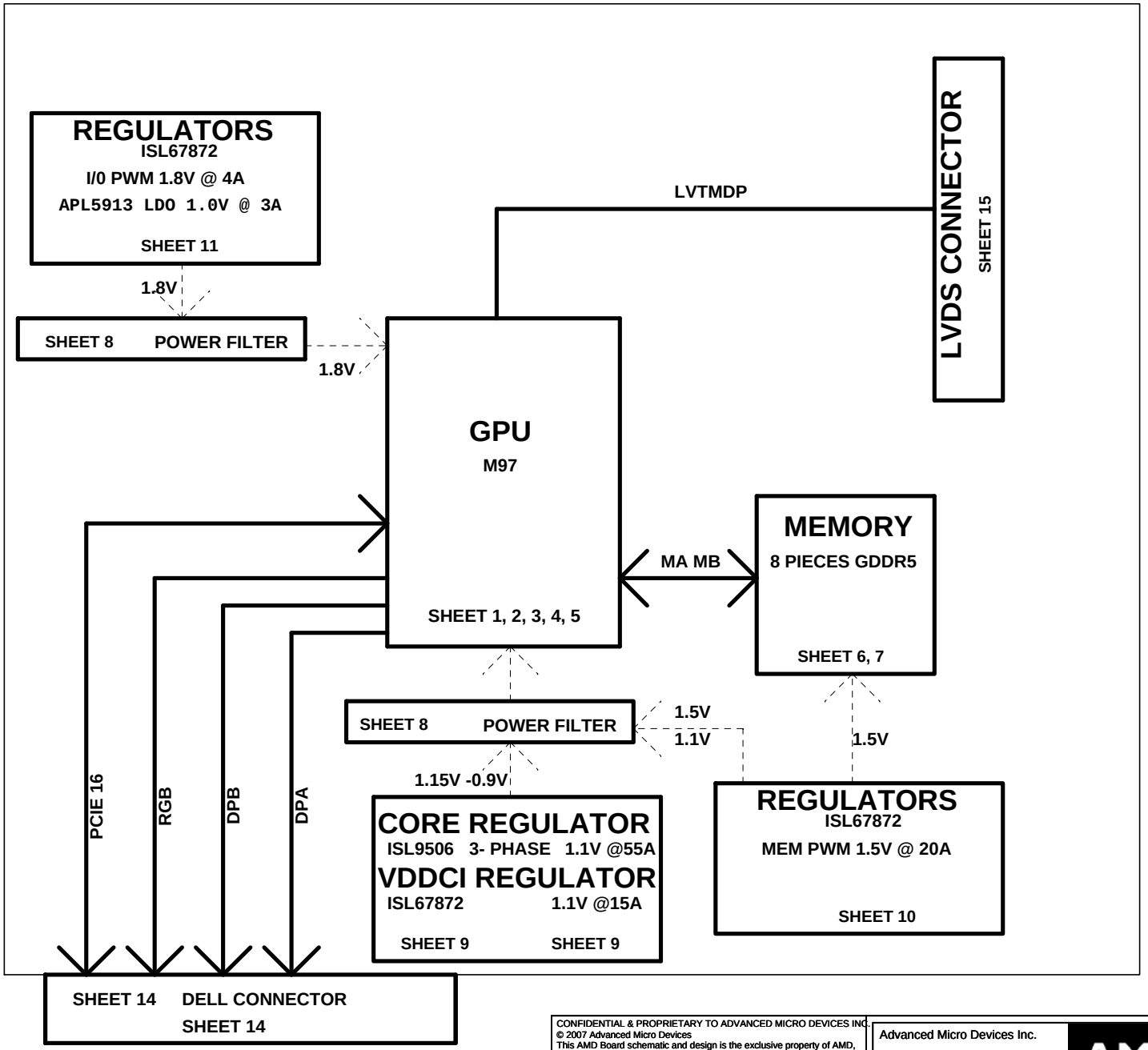
DELL REEBOK BLOCK DIAGRAM



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Title	Schematic No.	Date:
M97 1GB GDDR5 Dell Reebok	105-B779xx-10	Friday, September 04, 2009

REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.
For Stuffing options (component values, DNI's, ...) please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.**

Rev 0

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	10/08/08	Orginal Design for NIKE System
0	00B	01/14/09	Added Regulator for VDDCI Added 0ohm resistors close ASIC on SMBUS Added new CTF circuit
0	00C	02/24/09	Added Caps for LCDVCC added Snubber for 1.8V
0	00E	09/03/09	Changed to drive the ADM1032 device (and its related pull-ups) with +3Vsus instead of +3Vrun for Reebok