1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

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REV	ECN	DESCRIPTION OF REVISION	CK APPD	DATE
				2012-05-09

SCHEM,MLB,KEPLER,2PHASE,D2

FSB, 5/9/2012

Schematic / PCB #'s

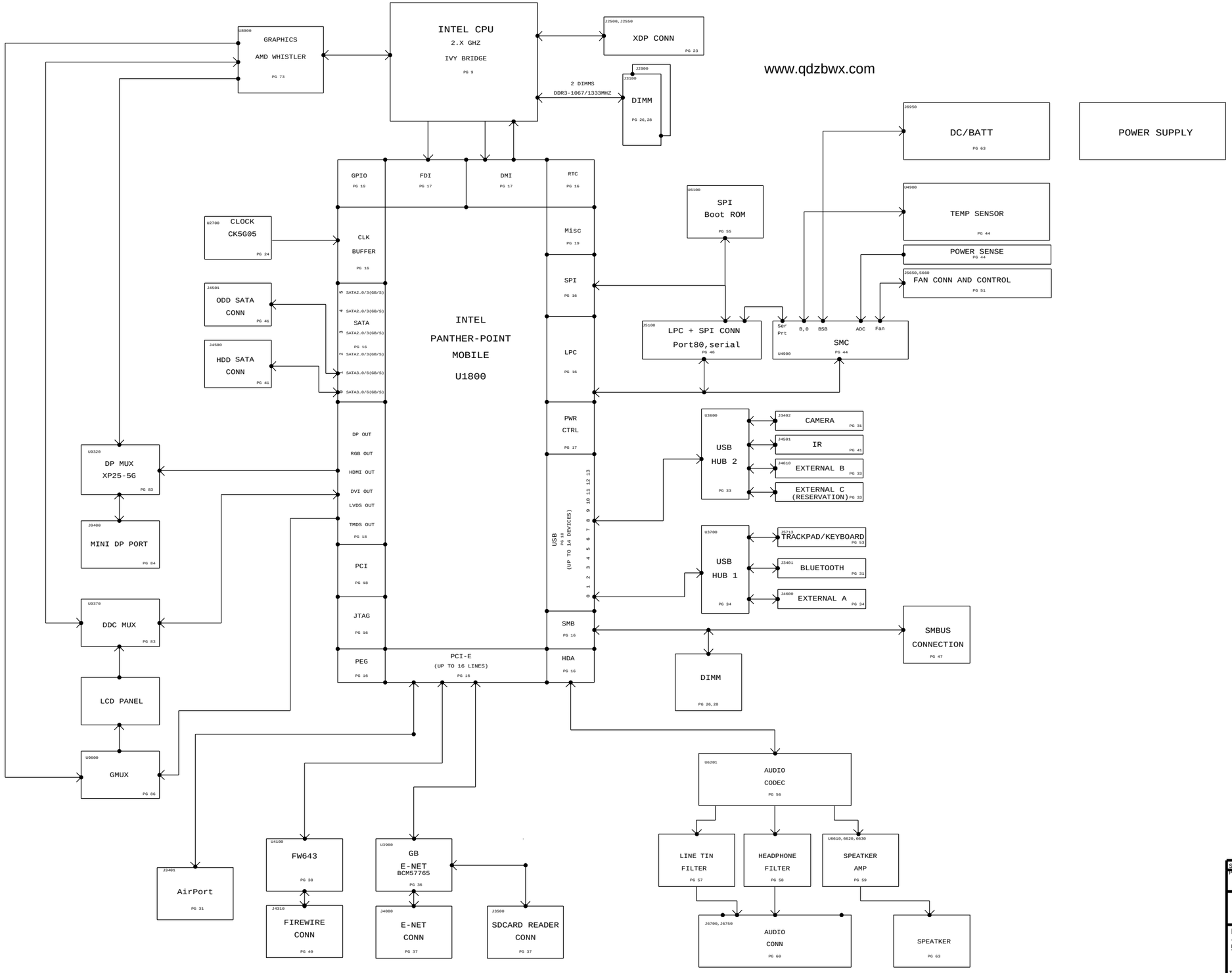
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-9589	1	SCHEM,MLB,KEPLER_2PHASE,D2	SCH	CRITICAL	
820-3332	1	PCBF,MLB,KEPLER_2PHASE,D2	PCB	CRITICAL	

DRAWING
TITLE=MLB
ABBREV=ABBREV
LAST_MODIFIED=Wed May 9 13:50:52 2012

DRAWING TITLE
SCHEM,MLB,KEPLER,2PHASE,D2

Apple Inc.

DRAWING NUMBER 051-9589 | SIZE D
REVISION 4.18.0
BRANCH



SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE

System Block Diagram

Apple Inc.

DRAWING NUMBER 051-9589 SIZE D

REVISION 4.18.0

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D2 POWER SYSTEM ARCHITECTURE

J6900 AC ADAPTER IN
DCIN(16.5V)
F6905 6A FUSE
SMC_DCIN_ISENSE
R7020
U7000 ISL6259HRTZ PBUS SUPPLY/ BATTERY CHARGER (PAGE 64)
SMC_RESET_L
PPVBAT_G3H
R7050
SMC_BATT_ISENSE
PP18V5_DCIN_CONN
R6990
D6990
PPBUS_G3H
F7040 8A FUSE
SMC_PBUS_VSENSE
Q5315
ENABLE 3.425V G3HOT PM6640 U6990 (PAGE 62)
PP3V42_G3H
SMC PWRGD NCP303LSN U5000 (PAGE 45)
SMC_RESET_L
SMC AVREF SUPPLY REF3333 U5001 (PAGE 45)
PP3V3_S5_AVREF_SMC
PP3V3_S5_SMC
SMC_TPAD_RST_L
SMC_ONOFF_L
U5001
J6950 3S2P (9 TO 12.6V)
PPVBATT_G3H_CONN
Q7055
CHGR_BGATE
PPVBAT_G3H_CHGR_R
PP5V_S3_GFXIMVP6_VDD
GPU VCORE ISL6263C U8900 (PAGE 82)
GPUVCORE_EN
GPUVCORE_PGOOD
R5388/U5388
U5410
SMC_GPU_ISENSE
SMC_GPU_VSENSE
PPVCORE_GPU
PP5V_S0_CPUVTTS0
1.05V ISL95870 U7600 (PAGE 70)
CPUVTTS0_EN
CPUVTTS0_PGOOD
R7640
PPCPUVTT_S0
SMC_CPU_FSB_ISENSE
TPS22924 U4202 (PAGE 39)
PP1V0_FW_FWPHY
FW_PWR_EN
SMC_CPU_HI_ISENSE
CPU VCORE ISL95831 U7400 (PAGE 67)
CPUIMVP7_VR_ON
SMC_CPU_ISENSE
SMC_CPU_VSENSE
PPVCORE_S0_CPU
CPUIMVP7_AXG_PGOOD
PM_PCH_PWRGD
U2850
PANTHER_POINT U1800 (PAGE 16~21)
PM_PWRBTN_L
PLT_RERST_L
CPU_PWRGD
PM_MEM_PWRGD
GMUX U9600 XP25-5 (PAGE 86)
EG_RAIL1_EN
EG_RAIL2_EN
EG_RAIL3_EN
EG_RAIL4_EN
PM_ALL_GPU_PGOOD
P1V1GPU_EN
P3V3GPU_EN
GPUVCORE_EN
SMC U4900 (PAGE 44)
P60
SMC_PM_G2_EN
RC DELAY
P3V3S5_EN
PANTHER-POINT MOBILE U1800 (PAGE 16~21)
SLP_S5#(E4)
SLP_S4#(H7)
SLP_S3#(P12)
PM_SLP_S5_L
PM_SLP_S4_L
PM_SLP_S3_L
P5VS3_EN
DDRREG_EN
P3V3S3_EN
R7978
PM_SLP_S3_L_R
P1V8S0_EN
P1V2S0_EN
CPUVTTS0_EN
P1V5CPU_EN
P5VS0_EN
P3V3S0_EN
PBUSVSENS_EN
PP5V_S3_DDRREG
P1V0GPU_EN
P1V5FB_EN
1.003V(L/H)
1.503V(R/H)
ISL6236 U9500 (PAGE 85)
PP1V0_S0GPU_REG
PP1V5_GPU_REG
SMC_GPU_1V8_ISENSE
R5413
P1V0GPU_PGOOD
P1V5FB_PGOOD
DDRREG_EN
DDRVTT_EN
1.5V
0.75V
TPS51116 U7300 (PAGE 66)
PPDDR_S3_REG
PPVTT_S0_DDR_LDO
DDRREG_PGOOD
R7350
SMC_DDR_ISENSE
U5440
SMC_CPU_DDR_VSENSE
PP1V5_S3
4.5V MAX8840 U6200
PP4V5_AUDIO_ANALOG
PP3V3_S0
P1V5CPU_EN
SLG5AP020 U7801
PP1V5_S3
PP1V5_S3RS0
Q7801
P1V5S0FET_GATE
Q7860
PP5V_S0
P5V_S3
P5V_S0_EN
P5VS3_EN
P3V3S5_EN
5V (L/H)
3.3V (R/H)
TPS51125 U7201 (PAGE 65)
PP3V3_S5
P5V3V3_PGOOD
Q9806
BKLT_PLT_RST_L && LCD_BKLT_NO
BKLT_EN
LP8550 U9701 (PAGE 87)
PPVOUT_S0_LCDBKLT
Q4260
PFWB0OST
SMC_ADAPTER_EN&&PM_SLP_S3_L
Q7870
PP3V3_S0GPU_
P3V3GPU_EN
Q7810
PP3V3_S3
P3V3S3_EN
Q7830
PP3V3_S0_FET
P3V3S0_EN
Q7922
PP3V3_ENET
PM_SLP_S3_L&&WOL_EN|SMC_ADAPTER_EN
TPS22924 U4201 (PAGE 39)
PP3V3_FW_FWPHY
FW_PWR_EN
P1V8FB_EN
SLG5AP020 U7880
PP1V8_S0
Q7880
PP1V8_GPUIFPX
P1V8GPUIFPXFET_GATE
U7980
PM_ALL_GPU_PGOOD
PP3V3_S0_PWRCTL
P1V8S0_PGOOD
P5V3V3_PGOOD
S0PGOOD_PWROK
ALL_SYS_PWRGD
RSMRST_PWRGD
SMC_ONOFF_L
SMC
H8S2117 U4900 (PAGE 45)
SMC_ADAPTER_EN
PM_RSMRST_L
CPUIMVP_VR_ON
PM_SYSRST_L
PM_PWRBTN_L
SMC_RESET_L
PM_SLP_S5_L
PM_SLP_S4_L
PM_SLP_S3_L
P1V8_S0_EN
ISL8014A U7720 (PAGE 70)
PP1V8_S0
P1V8S0_PGOOD
P1V2ENET_EN
ISL8014A U7760 (PAGE 70)
PP1V2_ENET
P1V2ENET_PGOOD
Q7850
PP1V2_S0
P1V2S0_EN
U7971 ISL88042IRTJJZ
PP3V3_S0
PP1V5_S0
PP1V05_S0
TRST = 200mS
CPU U1000 (PAGE 9~14)
SM_DRAMPWROK
VCCCPUPWRGD
RESET*

SYNC_MASTER=D2_KEPLER
SYNC_DATE=01/13/2012
PAGE TITLE
Power Block Diagram
Apple Inc.
DRAWING NUMBER 051-9589
SIZE D
REVISION 4.18.0
BRANCH

8 7 6 5 4 3 2 1

D C B A

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE

Revision History

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DRAWING NUMBER 051-9589 SIZE D

REVISION 4.18.0

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BOM Variants (continued on CSA 6)

BOM NUMBER	BOM NAME	BOM OPTIONS
085-3726	D2,MLB,KEPLER,DEV	D2_DEVEL:ENG
085-4776	D2,MLB,KEPLER,FSB DEV	D2_DEVEL:FSB
607-9546	D2,MLB,KEPLER_2PHASE,COMMON	D2_COMMON,POSCAP_MYLAR_PAIR
685-0016	PBUS PAIR,KEMET POSCAP,TALL MYLAR,D2	PBUS_CAP:KEMET
685-0017	PBUS PAIR,SANYO POSCAP,SHORT MYLAR,D2	PBUS_CAP:SANYO
639-3378	PCBA,2.3G,8G_HYN,VRAM_HYN,MLB_KEPLER,D2,DY3V	BASE_BOM,CPU_IVY:2_3GHZ,FB_2G_HYNIX_A_DIE,EEEE:DY3V,DEVEL_BOM,RAM_2G_HYNIX_1600
639-3379	PCBA,2.3G,8G_HYN,VRAM_SAM,MLB_KEPLER,D2,DY3W	BASE_BOM,CPU_IVY:2_3GHZ,FB_2G_SAMSUNG,EEEE:DY3W,DEVEL_BOM,RAM_2G_HYNIX_1600
639-3380	PCBA,2.3G,8G_SAM,VRAM_HYN,MLB_KEPLER,D2,DY3Y	BASE_BOM,CPU_IVY:2_3GHZ,FB_2G_HYNIX_A_DIE,EEEE:DY3Y,DEVEL_BOM,RAM_2G_SAMSUNG_1600
639-3381	PCBA,2.3G,8G_SAM,VRAM_SAM,MLB_KEPLER,D2,DY40	BASE_BOM,CPU_IVY:2_3GHZ,FB_2G_SAMSUNG,EEEE:DY40,DEVEL_BOM,RAM_2G_SAMSUNG_1600
639-3384	PCBA,2.3G,16G_HYN,VRAM_HYN,MLB_KEPLER,D2,DY43	BASE_BOM,CPU_IVY:2_3GHZ,FB_2G_HYNIX_A_DIE,EEEE:DY43,DEVEL_BOM,RAM_4G_HYNIX_1600
639-3385	PCBA,2.3G,16G_HYN,VRAM_SAM,MLB_KEPLER,D2,DY44	BASE_BOM,CPU_IVY:2_3GHZ,FB_2G_SAMSUNG,EEEE:DY44,DEVEL_BOM,RAM_4G_HYNIX_1600
639-3386	PCBA,2.3G,16G_SAM,VRAM_HYN,MLB_KEPLER,D2,DY45	BASE_BOM,CPU_IVY:2_3GHZ,FB_2G_HYNIX_A_DIE,EEEE:DY45,DEVEL_BOM,RAM_4G_SAMSUNG_1600
639-3387	PCBA,2.3G,16G_SAM,VRAM_SAM,MLB_KEPLER,D2,DY4C	BASE_BOM,CPU_IVY:2_3GHZ,FB_2G_SAMSUNG,EEEE:DY4C,DEVEL_BOM,RAM_4G_SAMSUNG_1600
639-2821	PCBA,2.6G,8G_HYN,VRAM_HYN,MLB_KEPLER,D2,DRF1	BASE_BOM,CPU_IVY:2_6GHZ,FB_2G_HYNIX_A_DIE,EEEE:DRF1,DEVEL_BOM,RAM_2G_HYNIX_1600
639-2825	PCBA,2.6G,8G_HYN,VRAM_SAM,MLB_KEPLER,D2,DRF4	BASE_BOM,CPU_IVY:2_6GHZ,FB_2G_SAMSUNG,EEEE:DRF4,DEVEL_BOM,RAM_2G_HYNIX_1600
639-2817	PCBA,2.6G,8G_SAM,VRAM_HYN,MLB_KEPLER,D2,DRDN	BASE_BOM,CPU_IVY:2_6GHZ,FB_2G_HYNIX_A_DIE,EEEE:DRDN,DEVEL_BOM,RAM_2G_SAMSUNG_1600
639-2815	PCBA,2.6G,8G_SAM,VRAM_SAM,MLB_KEPLER,D2,DRDW	BASE_BOM,CPU_IVY:2_6GHZ,FB_2G_SAMSUNG,EEEE:DRDW,DEVEL_BOM,RAM_2G_SAMSUNG_1600
639-2979	PCBA,2.6G,16G_HYN,VRAM_HYN,MLB_KEPLER,D2,DT9H	BASE_BOM,CPU_IVY:2_6GHZ,FB_2G_HYNIX_A_DIE,EEEE:DT9H,DEVEL_BOM,RAM_4G_HYNIX_1600
639-2980	PCBA,2.6G,16G_HYN,VRAM_SAM,MLB_KEPLER,D2,DT9D	BASE_BOM,CPU_IVY:2_6GHZ,FB_2G_SAMSUNG,EEEE:DT9D,DEVEL_BOM,RAM_4G_HYNIX_1600
639-2981	PCBA,2.6G,16G_SAM,VRAM_HYN,MLB_KEPLER,D2,DT9F	BASE_BOM,CPU_IVY:2_6GHZ,FB_2G_HYNIX_A_DIE,EEEE:DT9F,DEVEL_BOM,RAM_4G_SAMSUNG_1600
639-2982	PCBA,2.6G,16G_SAM,VRAM_SAM,MLB_KEPLER,D2,DT9G	BASE_BOM,CPU_IVY:2_6GHZ,FB_2G_SAMSUNG,EEEE:DT9G,DEVEL_BOM,RAM_4G_SAMSUNG_1600
639-3618	PCBA,2.7G,8G_HYN,VRAM_HYN,MLB_KEPLER,D2,F0HN	BASE_BOM,CPU_IVY:2_7GHZ,FB_2G_HYNIX_A_DIE,EEEE:F0HN,DEVEL_BOM,RAM_2G_HYNIX_1600
639-3619	PCBA,2.7G,8G_HYN,VRAM_SAM,MLB_KEPLER,D2,F0HR	BASE_BOM,CPU_IVY:2_7GHZ,FB_2G_SAMSUNG,EEEE:F0HR,DEVEL_BOM,RAM_2G_HYNIX_1600
639-3561	PCBA,2.7G,8G_SAM,VRAM_HYN,MLB_KEPLER,D2,DYW4	BASE_BOM,CPU_IVY:2_7GHZ,FB_2G_HYNIX_A_DIE,EEEE:DYW4,DEVEL_BOM,RAM_2G_SAMSUNG_1600
639-3620	PCBA,2.7G,8G_SAM,VRAM_SAM,MLB_KEPLER,D2,F0HV	BASE_BOM,CPU_IVY:2_7GHZ,FB_2G_SAMSUNG,EEEE:F0HV,DEVEL_BOM,RAM_2G_SAMSUNG_1600
639-3627	PCBA,2.7G,16G_HYN,VRAM_HYN,MLB_KEPLER,D2,F0HM	BASE_BOM,CPU_IVY:2_7GHZ,FB_2G_HYNIX_A_DIE,EEEE:F0HM,DEVEL_BOM,RAM_4G_HYNIX_1600
639-3562	PCBA,2.7G,16G_HYN,VRAM_SAM,MLB_KEPLER,D2,DYW5	BASE_BOM,CPU_IVY:2_7GHZ,FB_2G_SAMSUNG,EEEE:DYW5,DEVEL_BOM,RAM_4G_HYNIX_1600
639-3628	PCBA,2.7G,16G_SAM,VRAM_HYN,MLB_KEPLER,D2,F0HY	BASE_BOM,CPU_IVY:2_7GHZ,FB_2G_HYNIX_A_DIE,EEEE:F0HY,DEVEL_BOM,RAM_4G_SAMSUNG_1600
639-3629	PCBA,2.7G,16G_SAM,VRAM_SAM,MLB_KEPLER,D2,F0HT	BASE_BOM,CPU_IVY:2_7GHZ,FB_2G_SAMSUNG,EEEE:F0HT,DEVEL_BOM,RAM_4G_SAMSUNG_1600

BOM Groups

BOM GROUP	BOM OPTIONS
D2_COMMON	ALTERNATE,COMMON,D2_COMMON1,D2_COMMON2,D2_PROGPARTS,D2_PVB
D2_COMMON1	CPUMEM_S0,SMC_DEBUG_YES,DPMUX:HOCO,TBTRTR:PRQ,TBTBST:Y,TBTHV:P15V,HUB_2NONREM,USBHUB2512B,SPEAKERID,SMC_PACKAGE:PROD,SKIP_5V3V3:AUDIBLE,CHGR_5V:LDO,P1V5S0:LDO
D2_COMMON2	EDP:YES,MIKEY,PPCPUVCCIO:IVB,PPDDR:1V35,LPCPLUS_CONN:YES,LPCPLUS_R:YES,KBD_BL:SANDWICH,CAPS:INT,BTPWR:S4,XDP,XDP_CPU:BPM,GPU:2P,TPAD_5V:LDO_S5
D2_PVB	VREF:PROD,D_BKL:PROD,SENSOR_NONPROD:N
D2_PROGPARTS	SMC_PROG:FSB,BOOTROM_PROG:FSB,DPMUXMCU:PROG,TPAD_PSOC:PROG,TBTROM:PROG
D2_DEVEL:ENG	ALTERNATE,IVB_PPT_XDP,S0PGOOD_ISL,DPMUX_DEBUG,DDRVREF_DAC,VREF:ENG_M3,SENSOR_NONPROD:Y,D_BKL:DEV
D2_DEVEL:FSB	ALTERNATE,IVB_PPT_XDP
IVB_PPT_XDP	XDP_CONN,XDP_PCH

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4266	1	IVB,S RBMP,PRQ,E1,2.3,45W,4+2,1.2,BM,BGA	U1000	CRITICAL	CPU_IVY:2_3GHZ
337S4267	1	IVB,S RBMP,PRQ,E1,2.6,45W,4+2,1.25,BM,BGA	U1000	CRITICAL	CPU_IVY:2_6GHZ
337S4268	1	IVB,S RBMP,PRQ,E1,2.7,45W,4+2,1.25,BM,BGA	U1000	CRITICAL	CPU_IVY:2_7GHZ
337S4269	1	PANTHER POINT,C1,SLJ8C,PRQ,BD82HM77	U1800	CRITICAL	
337S4256	1	IC,GPU,NV GK107-GTX-PS-A2	U8000	CRITICAL	
338S1113	1	IC,TBT,CR-4C,B1,PRQ,C20,220 12X12 FC:CSP	U3600	CRITICAL	TBTRTR:PRQ
333S0622	32	IC,SDRAM,DDR3-1600,256MX8,78FBGA,HYNIX,C-DIE,38NM		CRITICAL	2G_HYNIX_1600
333S0623	32	IC,SDRAM,DDR3-1600,256MX8,78FBGA,SAMSUNG		CRITICAL	2G_SAMSUNG_1600
333S0628	32	IC,SDRAM,DDR3-1600,256MX8,78FBGA,D-DIE,ELPIDA		CRITICAL	2G_ELPIDA_1600
333S0625	32	IC,SDRAM,DDR3-1600,512MX8,78FBGA,HYNIX		CRITICAL	4G_HYNIX_1600
333S0624	32	IC,SDRAM,DDR3-1600,512MX8,78FBGA,C-DIE,SAMSUNG		CRITICAL	4G_SAMSUNG_1600
333S0629	32	IC,SDRAM,DDR3-1600,512MX8,78FBGA,B-DIE,ELPIDA		CRITICAL	4G_ELPIDA_1600
333S0630	4	IC,SDRAM,GDDR5,64MX32,A-DIE,HYNIX	U8400,U8450,U8500,U8550	CRITICAL	FB_2G_HYNIX_A_DIE
333S0631	4	IC,SDRAM,GDDR5,64MX32,D-DIE,SAMSUNG	U8400,U8450,U8500,U8550	CRITICAL	FB_2G_SAMSUNG
128S0264	30	CAP,TANT,POLY,68UF,20%,16V,50MOHM,D2E		CRITICAL	PBUS_CAP:SANYO
128S0257	30	CAP,TANT,POLY,68UF,20%,16V,50MOHM,D,LF		CRITICAL	PBUS_CAP:KEMET
725-1614	1	INSULATOR,SHORT,REAR,MLB,D2	REAR_INSULATOR	CRITICAL	PBUS_CAP:SANYO
725-1648	1	INSULATOR,TALL,REAR,MLB,D2	REAR_INSULATOR	CRITICAL	PBUS_CAP:KEMET
725-1568	1	INSULATOR,CPU,D2	CPU_INSULATOR	CRITICAL	
725-1569	1	INSULATOR,GPU,D2	GPU_INSULATOR	CRITICAL	
725-1621	1	INSULATOR,PCH,D2	PCH_INSULATOR	CRITICAL	
806-2897	2	CAN,COVER,2,J5	CAN_COVER1,CAN_COVER2	CRITICAL	
825-7697	1	TEXT,LABEL,MLB,D2	TEXT_LABEL	CRITICAL	
946-3819	1	D2 MLB DYMAX ADHESIVE SEE-CURE 29993-SC	EDGE_BOND	CRITICAL	
825-7841	1	LBL,PART CONFIG,BOARDS,D2	CONFIG_LABEL	CRITICAL	

PD Parts

Bar Code Labels / EEEE #'s (continued on CSA 6)

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DY3V]	CRITICAL	EEEE:DY3V
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DY3W]	CRITICAL	EEEE:DY3W
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DY3Y]	CRITICAL	EEEE:DY3Y
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DY40]	CRITICAL	EEEE:DY40
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DY43]	CRITICAL	EEEE:DY43
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DY44]	CRITICAL	EEEE:DY44
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DY45]	CRITICAL	EEEE:DY45
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DY4C]	CRITICAL	EEEE:DY4C
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DRF1]	CRITICAL	EEEE:DRF1
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DRF4]	CRITICAL	EEEE:DRF4
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DRDN]	CRITICAL	EEEE:DRDN
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DRDW]	CRITICAL	EEEE:DRDW
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DT9H]	CRITICAL	EEEE:DT9H
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DT9D]	CRITICAL	EEEE:DT9D
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DT9F]	CRITICAL	EEEE:DT9F
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DT9G]	CRITICAL	EEEE:DT9G
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:F0HN]	CRITICAL	EEEE:F0HN
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:F0HR]	CRITICAL	EEEE:F0HR
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DYW4]	CRITICAL	EEEE:DYW4
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:F0HV]	CRITICAL	EEEE:F0HV
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:F0HM]	CRITICAL	EEEE:F0HM
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DYW5]	CRITICAL	EEEE:DYW5
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:F0HY]	CRITICAL	EEEE:F0HY
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:F0HT]	CRITICAL	EEEE:F0HT

Programmables

341S3584	1	IC,TRKPD/KYBD CNTRLR,DVB,D2	U5701	CRITICAL	TPAD_PSOC:PROG
337S2983	1	IC,TP PSOC,QFN,BLANK	U5701	CRITICAL	TPAD_PSOC:BLANK
341S3597	1	IC,EEPROM,CACTUS RIDGE (0.1) FSB,D2	U3690	CRITICAL	TBTROM:PROG
335S0865	1	EEPROM,256KBIT,SPI,5MHZ,1.8V,2X3QFN	U3690	CRITICAL	TBTROM:BLANK
335S0852	1	IC,GPU ROM,D2,BLANK	U8701	CRITICAL	GPUROM:BLANK
341S3565	1	IC,EDP MUX-95C, (RENESAS) V3.2.8,DVB,D2	U9100	CRITICAL	DPMUXMCU:PROG
337S4313	1	IC,MCU,H8S/2113,8X8MM,TLP-145V	U9100	CRITICAL	DPMUXMCU:BLANK

DRAM VREF Configs

BOM GROUP	BOM OPTIONS
VREF:PROD	VREFDQ:M1_M3,VREFCA:LDO
VREF:ENG_M3	VREFDQ:M1_M3,VREFCA:LDO_DAC
VREF:ENG_LDO	VREFDQ:M1_DAC,VREFCA:LDO_DAC

DRAM SPD Straps

BOM GROUP	BOM OPTIONS
RAM_4G_HYNIX_1600_S	RAMCFG3:L,RAMCFG2:L,RAMCFG1:L,RAMCFG0:L
RAM_1G_SAMSUNG_1600	RAMCFG3:L,RAMCFG2:L,RAMCFG1:L,RAMCFG0:H
RAM_4G_SAMSUNG_1600_S	RAMCFG3:L,RAMCFG2:L,RAMCFG1:H,RAMCFG0:L
RAM_1G_HYNIX_1600	RAMCFG3:L,RAMCFG2:L,RAMCFG1:H,RAMCFG0:H
RAM_4G_ELPIDA_1600_S	RAMCFG3:L,RAMCFG2:H,RAMCFG1:L,RAMCFG0:L
RAM_2G_SAMSUNG_1600	2G_SAMSUNG_1600,RAMCFG3:L,RAMCFG2:H,RAMCFG1:L,RAMCFG0:H
RAM_2G_SAMSUNG_1333	RAMCFG3:L,RAMCFG2:H,RAMCFG1:H,RAMCFG0:L
RAM_2G_HYNIX_1600	2G_HYNIX_1600,RAMCFG3:L,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H
RAM_4G_SAMSUNG_1600	4G_SAMSUNG_1600,RAMCFG3:H,RAMCFG2:L,RAMCFG1:L,RAMCFG0:L
RAM_4G_HYNIX_1600	4G_HYNIX_1600,RAMCFG3:H,RAMCFG2:L,RAMCFG1:L,RAMCFG0:H
RAM_2G_ELPIDA_1600_S	RAMCFG3:H,RAMCFG2:L,RAMCFG1:H,RAMCFG0:L
RAM_2G_ELPIDA_1600	2G_ELPIDA_1600,RAMCFG3:H,RAMCFG2:L,RAMCFG1:H,RAMCFG0:H
RAM_4G_ELPIDA_1600	4G_ELPIDA_1600,RAMCFG3:H,RAMCFG2:H,RAMCFG1:L,RAMCFG0:L
RAM_2G_SAMSUNG_1600_S	RAMCFG3:H,RAMCFG2:H,RAMCFG1:L,RAMCFG0:H
RAM_2G_HYNIX_1600_S	RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:L

DEVELOPMENT/BASE BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-3726	1	D2 MLB KEPLER DEVEL BOM	DEVEL	CRITICAL	DEVEL_BOM
085-4776	1	D2 MLB KEPLER FSB DEVEL BOM	DEVEL_FSB	CRITICAL	DEVEL_FSB_BOM
607-9546	1	D2 MLB KEPLER 2PHASE BASE BOM	BASE	CRITICAL	BASE_BOM
685-0016	1	PBUS PAIR,KEMET POSCAP,TALL MYLAR,D2	POSCAP_MYLAR	CRITICAL	POSCAP_MYLAR_PAIR

SMC

341S3308	1	IC,SMC,DEVELOPMENT-FSB,A3,D2	U4900	CRITICAL	SMC_PROG:FSB
341S3309	1	IC,SMC,PVB,A3,2.2F36,D2	U4900	CRITICAL	SMC_PROG:PVB

EFI ROM

341S3595	1	IC,EFI,ROM,FSB, D2	U6100	CRITICAL	BOOTROM_PROG:FSB

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0257	128S0264		ALL	Kemet alt to Sanyo
353S3527	353S3528		ALL	Pericom eDP MUX
353S3526	353S3528		ALL	TI eDP MUX
376S0855	376S0613		ALL	Diodes alt to Toshiba
376S0855	376S0613	VREFDQ:M1_M3	ALL	Diodes alt to Toshiba
376S1076	376S0634		ALL	Diodes alt to On Semi
376S0903	376S0796		ALL	Fairchild alt to Siliconix
376S0977	376S0859		ALL	Diodes alt to Toshiba
376S1053	376S0604		ALL	Diodes alt to Fairchild
128S0311	128S0329		ALL	NEC alt to Sanyo
138S0739	138S0706		ALL	Samsung alt to Murata
197S0434	197S0343		ALL	Epson Alt to TXC
197S0435	197S0343		ALL	NDK Alt to TXC
197S0432	197S0431		ALL	NDK Alt to Epson
197S0452	197S0181		ALL	Epson Alt to TXC
197S0453	197S0181		ALL	NDK Alt to TXC
685-0017	685-0016		ALL	Sanyo POSCAP/Mylar alt to Kemet
376S0975	376S1081		ALL	Toshiba alt to diodes
371S0709	371S0652		ALL	NXP alt to infineon
371S0713	371S0558		ALL	DDS alt to ST
377S0126	377S0066		ALL	New Semtech package
377S0147	377S0066		ALL	On Semi alt to Semtech
152S0461	152S1645		ALL	Cyntec alt to Vishay
376S1080	376S0820		ALL	Diodes alt to On Semi
155S0667	155S0583		ALL	Panasonic alt to TDK
107S0232	107S0129		ALL	Cyntec alt to TFT
197S0466	197S0464		ALL	Epson alt to NDK
341S3564	341S3565		ALL	Avnet eDP MUX alt to Renesas

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

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BOM Configuration

Apple Inc.

DRAWING NUMBER 051-9589 SIZE D

REVISION 4.18.0

BRANCH

BOM Variants (continued from CSA 5)

BOM NUMBER	BOM NAME	BOM OPTIONS
639-3382	PCBA,2.3G,8G_ELP,VRAM_HYN,MLB_KEPLER,D2,DY41	BASE_BOM,CPU_IVY:2_3GHZ,FB_2G_HYNIX_A_DIE,EEEE:DY41,DEVEL_BOM,RAM_2G_ELPIDA_1600
639-3383	PCBA,2.3G,8G_ELP,VRAM_SAM,MLB_KEPLER,D2,DY42	BASE_BOM,CPU_IVY:2_3GHZ,FB_2G_SAMSUNG,EEEE:DY42,DEVEL_BOM,RAM_2G_ELPIDA_1600
639-3445	PCBA,2.3G,16G_ELP,VRAM_HYN,MLB_KEPLER,D2,DYJ5	BASE_BOM,CPU_IVY:2_3GHZ,FB_2G_HYNIX_A_DIE,EEEE:DYJ5,DEVEL_BOM,RAM_4G_ELPIDA_1600
639-3446	PCBA,2.3G,16G_ELP,VRAM_SAM,MLB_KEPLER,D2,DYJ6	BASE_BOM,CPU_IVY:2_3GHZ,FB_2G_SAMSUNG,EEEE:DYJ6,DEVEL_BOM,RAM_4G_ELPIDA_1600
639-2818	PCBA,2.6G,8G_ELP,VRAM_HYN,MLB_KEPLER,D2,DRF0	BASE_BOM,CPU_IVY:2_6GHZ,FB_2G_HYNIX_A_DIE,EEEE:DRF0,DEVEL_BOM,RAM_2G_ELPIDA_1600
639-2820	PCBA,2.6G,8G_ELP,VRAM_SAM,MLB_KEPLER,D2,DRDP	BASE_BOM,CPU_IVY:2_6GHZ,FB_2G_SAMSUNG,EEEE:DRDP,DEVEL_BOM,RAM_2G_ELPIDA_1600
639-2823	PCBA,2.6G,16G_ELP,VRAM_HYN,MLB_KEPLER,D2,DRDT	BASE_BOM,CPU_IVY:2_6GHZ,FB_2G_HYNIX_A_DIE,EEEE:DRDT,DEVEL_BOM,RAM_4G_ELPIDA_1600
639-2819	PCBA,2.6G,16G_ELP,VRAM_SAM,MLB_KEPLER,D2,DRDQ	BASE_BOM,CPU_IVY:2_6GHZ,FB_2G_SAMSUNG,EEEE:DRDQ,DEVEL_BOM,RAM_4G_ELPIDA_1600
639-3632	PCBA,2.7G,8G_ELP,VRAM_HYN,MLB_KEPLER,D2,F0JD	BASE_BOM,CPU_IVY:2_7GHZ,FB_2G_HYNIX_A_DIE,EEEE:F0JD,DEVEL_BOM,RAM_2G_ELPIDA_1600
639-3633	PCBA,2.7G,8G_ELP,VRAM_SAM,MLB_KEPLER,D2,F0J3	BASE_BOM,CPU_IVY:2_7GHZ,FB_2G_SAMSUNG,EEEE:F0J3,DEVEL_BOM,RAM_2G_ELPIDA_1600
639-3630	PCBA,2.7G,16G_ELP,VRAM_HYN,MLB_KEPLER,D2,F0J4	BASE_BOM,CPU_IVY:2_7GHZ,FB_2G_HYNIX_A_DIE,EEEE:F0J4,DEVEL_BOM,RAM_4G_ELPIDA_1600
639-3631	PCBA,2.7G,16G_ELP,VRAM_SAM,MLB_KEPLER,D2,F0JC	BASE_BOM,CPU_IVY:2_7GHZ,FB_2G_SAMSUNG,EEEE:F0JC,DEVEL_BOM,RAM_4G_ELPIDA_1600

Bar Code Labels / EEEE #’s (continued from CSA 5)

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DY41]	CRITICAL	EEEE:DY41
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DY42]	CRITICAL	EEEE:DY42
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DYJ5]	CRITICAL	EEEE:DYJ5
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DYJ6]	CRITICAL	EEEE:DYJ6
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DRF0]	CRITICAL	EEEE:DRF0
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DRDP]	CRITICAL	EEEE:DRDP
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DRDT]	CRITICAL	EEEE:DRDT
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DRDQ]	CRITICAL	EEEE:DRDQ
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:F0JD]	CRITICAL	EEEE:F0JD
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:F0J3]	CRITICAL	EEEE:F0J3
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:F0J4]	CRITICAL	EEEE:F0J4
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:F0JC]	CRITICAL	EEEE:F0JC

Elipda DQ’d
Keeping for PRQ

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

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Apple Inc.

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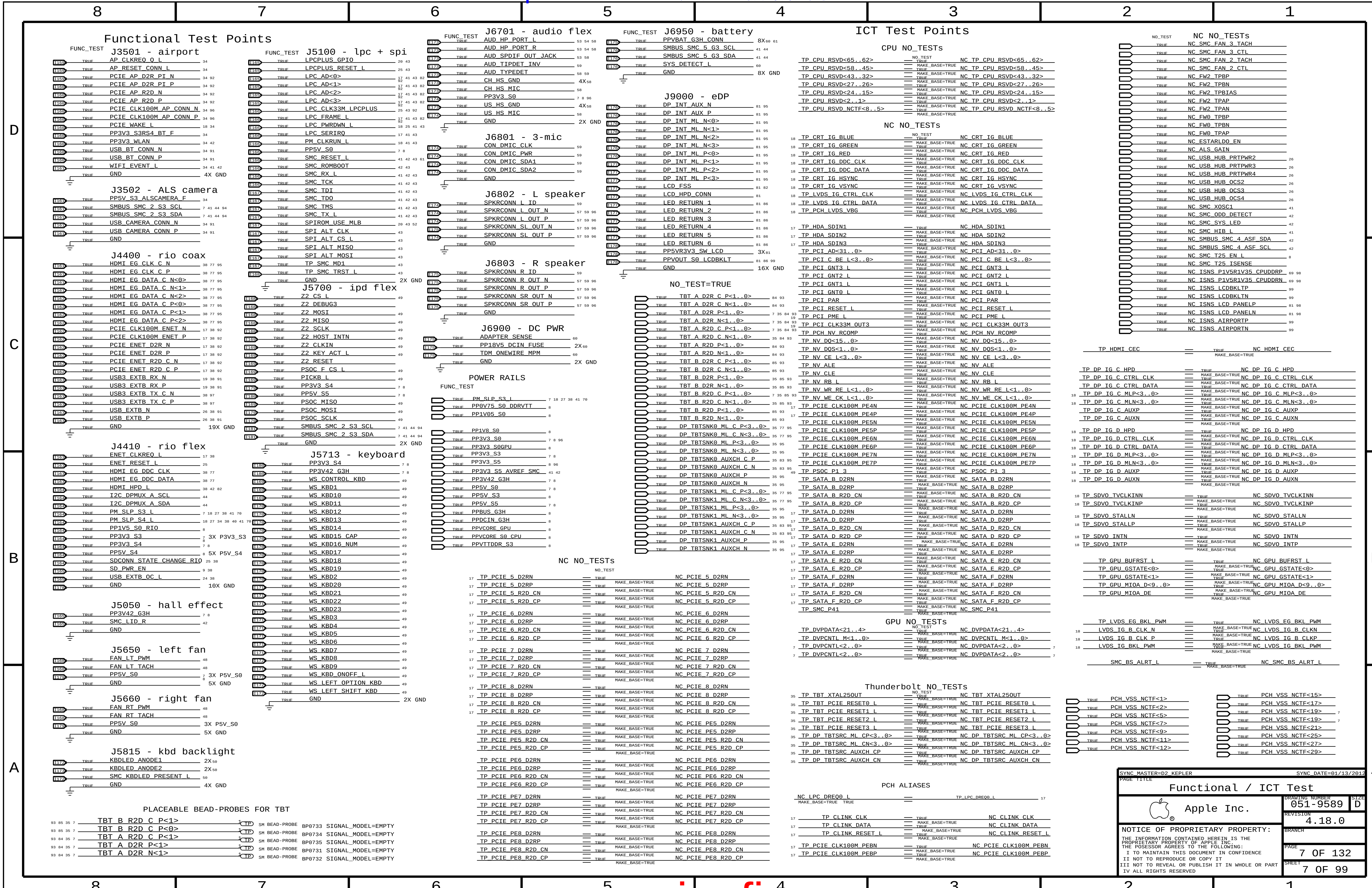

G3H Rails

=PPBUS_G3H
PPBUS_G3H
MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=12.8V MAKE_BASE=TRUE
=PPBUS_S0_LCDBKLT
=PPVIN_S5_HS_OTHER_ISNS_R
=PPVIN_S5_HS_COMPUTING_ISNS_R
=PPVIN_S5_HS_GPU_ISNS_R
=PPVIN_SW_TBTBST
=PPBUS_S0_VSENSE
=PPBUS_G3H_T25_R

=PPVIN_S5_HS_COMPUTING_ISNS
PPVIN_S5_HS_COMPUTING_ISNS
MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=12.8V MAKE_BASE=TRUE
=PPVIN_S0_CPUIMVP
=PPVIN_S3_DDRREG
=PPVIN_S0_CPUVCCIOS0
=PPVIN_S0_CPUAXG
=PPVIN_S0_VCCSAS0
=PPVIN_S0_PCHVCCIOS0

=PPVIN_S5_HS_GPU_ISNS
PPVIN_S5_HS_GPU_ISNS
MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=12.8V MAKE_BASE=TRUE
=PPVIN_S0_GFXIMVP
=PPVIN_S0GPU_P1V5P1V0

=PPVIN_S5_HS_OTHER_ISNS
PPVIN_S5_HS_OTHER_ISNS
MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=12.8V MAKE_BASE=TRUE
=PPVIN_S5_P5VP3V3

=PP18V5_DCIN_CONN
PPDCIN_G3H
MIN_LINE_WIDTH=0.6 MM MIN_NECK_WIDTH=0.25 MM VOLTAGE=18.5V MAKE_BASE=TRUE
=PPDCIN_S5_CHGR

=PP18V5_DCIN_ISOL
PPDCIN_G3H_ISOL
MIN_LINE_WIDTH=0.6 MM MIN_NECK_WIDTH=0.25 MM VOLTAGE=18.5V MAKE_BASE=TRUE
=PPDCIN_S5_CHGR_ISOL
=PPDCIN_S5_VSENSE

=PP3V42_G3H_REG
PP3V42_G3H
MIN_LINE_WIDTH=0.3 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=3.42V MAKE_BASE=TRUE
=PP3V3_S5_LPCPLUS
=PP3V3_S5_SMC
=PP3V42_G3H_CHGR
=PP3V42_G3H_ONEWIREPROT
=PP3V42_G3H_PWRCTL
=PP3V42_G3H_SMBUS_SMC_5
=PP3V42_G3H_SMCUSBMUX
=PP3V42_G3H_TPAD
=PPVIN_S5_SMCVREF
=PPVBAT_G3_SYSCLK

=PP3V42_G3H_AUDIO
=PP3V42_G3H_TDM
=PP3V42_S3_HALL
For PCH RTC Power

=PPVRTC_G3_OUT
PPVRTC_G3H
MIN_LINE_WIDTH=0.3 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=3.42V MAKE_BASE=TRUE
=PPVRTC_G3_PCH

5V Rails

=PP5V_S5_LDO
PP5V_S5
MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.1 MM VOLTAGE=5V MAKE_BASE=TRUE
=PP5V_S5_P1V5S3RS0FET
=PP5V_S5_P5VSUSFET
=PP5V_S5_TPAD

=PP5V_SUS_FET
PP5V_SUS
MIN_LINE_WIDTH=0.6 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=5V MAKE_BASE=TRUE
=PP5V_SUS_PCH

=PP5V_S4_REG
PP5V_S4
MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=5V MAKE_BASE=TRUE
=PP5V_S4_RIO
=PP5V_S4_P5V5Q0FET
=PP5V_S4_P5V3FET
=PP5V_S0_LCD
=PP5V_S3_LTUSB
=PP5V_S4_ISNS
=PP5V_S4_TPAD
=PP5V_S4_AUDIO

=PP5V_S3_FET
PP5V_S3
MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=5V MAKE_BASE=TRUE
=PP5V_S3_ISNS
=PP5V_S3_ALSCAMERA
=PP5V_S3_DDRREG
=PP5V_S3_DEBUG_ADC_AVDD
=PP5V_S3_DEBUG_ADC_DVDD
=PP5V_S3_DEBUG_ISNS
=PP5V_S3_MEMRESET

=PP5V_S0_FET
PP5V_S0
MIN_LINE_WIDTH=0.4 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=5V MAKE_BASE=TRUE
=PP5V_S0GPU_P1V0P1V35_GPU

=PP5V_S0_P1V5_LDO
=PP5V_S0_AUDIO_XW
=PP5V_S0_BKL
=PP5V_S0_CPUIMVP
=PP5V_S0_CPUVCCIOS0
=PP5V_S0_FAN_LT
=PP5V_S0_FAN_RT
=PP5V_S0_GFXIMVP
=PP5V_S0_KBDLED
=PP5V_S0_LPCPLUS
=PP5V_S0_PCH
=PP5V_S0_PCHVCCIOS0
=PP5V_S0_RMC
=PP5V_S0_VCCSAS0
=PP5V_S0_VMON

3.3V Rails

=PP3V3_S4_FET
PP3V3_S4
MIN_LINE_WIDTH=0.6 MM MIN_NECK_WIDTH=0.1 MM VOLTAGE=3.3V MAKE_BASE=TRUE
=PP3V3_S4_TBT_R
=PP3V3_S4_TPAD
=PP3V3_S4_SMC
=PP3V3_S4_RIO
=PP3V3_S4_BT

=PP3V3_SUS_FET
PP3V3_SUS
MIN_LINE_WIDTH=0.6 MM MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PP3V3_SUS_P1V05SUSLDO
=PP3V3_SUS_PCH_VCCSUS
=PP3V3_SUS_PCH_VCCSUS_GPIO
=PP3V3_SUS_PCH_GPIO
=PP3V3_SUS_PCH_VCCSUS_USB
=PP3V3_SUS_CNTRL
=PP3V3_SUS_SMC

=PP3V3_SUS_ROM
=PP3V3_SUS_PCH_VCC_SPI

=PP3V3_S5_REG
PP3V3_S5
MIN_LINE_WIDTH=0.6 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=3.3V MAKE_BASE=TRUE
=PP3V3_GPU_P3V3GPUFET
=PP3V3_GPU_MISC_P3V3GPUMISCFET
=PP3V3_S0_P3V3S0FET
=PP3V3_S3_P3V3S3FET
=PP3V3_S4_DPAPWRSW
=PP3V3_S4_DPBPWRSW
=PP3V3_S4_P3V3S4FET
=PP3V3_S5_CPU_VCCDDR
=PP3V3_S5_P1V2P1V8
=PP3V3_S5_P1V5S0
=PP3V3_S5_P3V3SUSFET
=PP3V3_S5_PCH
=PP3V3_S5_PCHPWRGD
=PP3V3_S5_PCH_GPIO
=PP3V3_S5_PCH_VCCDSW
=PP3V3_S5_PWRCTL
=PP3V3_S5_SMCBATLOW
=PP3V3_S5_SYSCLK
=PP3V3_S5_VMON
=PP3V3_S5_XDP
=PP3V3_S4_TBTAPWRSW
=PP3V3_S4_TBTBPWRSW

=PP3V3_S3_FET
PP3V3_S3
MIN_LINE_WIDTH=0.50MM MIN_NECK_WIDTH=0.20MM VOLTAGE=3.3V MAKE_BASE=TRUE
=PP3V3_S3_BT
=PP3V3_S3_DPMUX_UC
=PP3V3_S3_ISNS
=PP3V3_S3_MEMRESET
=PP3V3_S3_PCH_GPIO
=PP3V3_S3_RIO
=PP3V3_S3_SMBUS_SMC_2_S3
=PP3V3_S3_SMBUS_SMC_3
=PP3V3_S3_TPAD
=PP3V3_S3_USBMUX
=PP3V3_S3_USB_HUB
=PP3V3_S3_USB_RESET
=PP3V3_S3_VREFMRGN
=PP3V3_S3_WLAN
=PP3V3_S3_GYRO
=PP3V3_S3_SMS
=PP3V3_S3_SDBUF

=PP3V3_S0_FET
PP3V3_S0
MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.075 mm VOLTAGE=3.3V MAKE_BASE=TRUE
=PP3V3_S0_AUDIO
=PP3V3_S0_AUDIO_DIG
=PP3V3_S0_BKL_VDDIO
=PP3V3_S0_CPUTHMSNS
=PP3V3_S0_CPU_VCCIO_SEL
=PP3V3_S0_DPMUX
=PP3V3_S0_DPMUXI2C
=PP3V3_S0_DPMUX_UC
=PP3V3_S0_FAN_LT
=PP3V3_S0_FAN_RT
=PP3V3_S0_GPUTHMSNS
=PP3V3_S0_HS_ISNS
=PP3V3_S0_IMVPISNS
=PP3V3_S0_ISNS
=PP3V3_S0_LCD
=PP3V3_S0_P1V8GPUFET
=PP3V3_S0_P3V3TBTFET
=PP3V3_S0_PCH
=PP3V3_S0_PCH_GPIO
=PP3V3_S0_PCH_VCC3_3_CLK
=PP3V3_S0_PCH_VCC3_3_GPIO
=PP3V3_S0_PCH_VCC3_3_HVCMOS
=PP3V3_S0_PCH_VCC3_3_PCI
=PP3V3_S0_PCH_VCC3_3_SATA
=PP3V3_S0_PCH_VCCADAC
=PP3V3_S0_PWRCTL
=PP3V3_S0_RSTBUF
=PP3V3_S0_SATAMUX
=PP3V3_S0_SB_PM
=PP3V3_S0_SMBUS_PCH
=PP3V3_S0_SMBUS_SMC_0_S0
=PP3V3_S0_SMBUS_SMC_1_S0
=PP3V3_S0_SSD
=PP3V3_S0_SYSCLK
=PP3V3_S0_TBTI2C
=PP3V3_S0_TBTPWRCTL
=PP3V3_S0_TPAD
=PP3V3_S0_VMON
=PP3V3_S0_X29THMSNS
=PP3V3_S0_XDP
=PP3V3_S0_DDR3THMSNS
=PP3V3_S0_SPKRTHMSNS

TBT RAILS

=PP3V3_TBTLC_FET
PP3V3_TBTLC
MIN_LINE_WIDTH=0.4 MM VOLTAGE=3.3V MIN_NECK_WIDTH=0.15 MM MAKE_BASE=TRUE
=PP3V3_TBT_PCH_GPIO
=PPVDDIO_TBT_CLK
=PP3V3_TBTLC_RTR

=PP1V05_TBTLC_FET
PP1V05_TBTLC
MIN_LINE_WIDTH=0.4 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=1.05V MAKE_BASE=TRUE
=PP1V05_TBTLC_RTR

=PP1V05_TBTCIO_FET
PP1V05_TBTCIO
MIN_LINE_WIDTH=0.4 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=1.05V MAKE_BASE=TRUE
=PP1V05_TBTCIO_RTR

=PP15V_TBT_REG
PP15V_TBT
MIN_LINE_WIDTH=0.4 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=15V MAKE_BASE=TRUE
=PPHV_SW_TBTAPWRSW
=PPHV_SW_TBTBPWRSW

1.8V/1.5V/1.2V/1.05V Rails

=PP1V8_S0_REG
4A max supply
PP1V8_S0
MIN_LINE_WIDTH=0.6 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=1.5V MAKE_BASE=TRUE
=PP1V8R1V5_S0_PCH_VCCVRM
=PP1V8_S0_AUDIO
=PP1V8_S0_CPU_VCCPLL
=PP1V8_S0_GPUFET
=PP1V8_S0_PCH_VCCTX_LVDS
=PP1V8_S0_PCH_VCC_DFTERM
=PPVDDIO_S0_SBCLK
=PP1V8_S0_P1V5_LDO

=PP1V8_S0_CPU_VCCPLL_R
PP1V8_S0_CPU_VCCPLL_R
MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=1.8V MAKE_BASE=TRUE

=PPDDR_S3_REG
PP1V5R1V35_S3
MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.17 mm VOLTAGE=1.5V MAKE_BASE=TRUE
=PP1V5_S3_MEMRESET
=PPDDR_S3_MEMVREF
=PPVIN_S3_P1V5S3RS0_FET
=PPVIN_S0_DDRREG_LDO
=PPVIN_S3_MEM_ISNS_R

=PPVIN_S3_MEM_ISNS
PP1V5R1V35_MEM
MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.17 mm VOLTAGE=1.5V MAKE_BASE=TRUE
=PP1V5R1V35_S3_MEM_A
=PP1V5R1V35_S3_MEM_B

=PP1V5_S3RS0_FET_ISNS
PP1V5_S3RS0_CPUDDR
MIN_LINE_WIDTH=0.6 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=1.5V MAKE_BASE=TRUE
=PP1V5_S3RS0_VMON
=PP1V5_S3_CPU_VCCDDR

=PP1V5_S0_REG
PP1V5_S0
MIN_LINE_WIDTH=0.6 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=1.5V MAKE_BASE=TRUE
=PP1V5_S0_AUDIO
=PP3V3R1V5_S0_PCH_VCCSUSHDA

=PP1V5_S0_RIO_LDO
PP1V5_S0_RIO
MIN_LINE_WIDTH=0.6 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=1.5V MAKE_BASE=TRUE
=PP1V5_S0_RIO

=PPVTT_S3_DDR_BUF
PPVTTDDR_S3
MIN_LINE_WIDTH=0.3 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=0.75V MAKE_BASE=TRUE

=PPVTT_S0_DDR_LDO
PP0V75_S0_DDRVTT
MIN_LINE_WIDTH=2 mm MIN_NECK_WIDTH=0.17 mm VOLTAGE=0.75V MAKE_BASE=TRUE
=PP0V75_S0_MEM_VTT_A
=PP0V75_S0_MEM_VTT_B
=PPVTT_S0_VTTCLAMP

=PP1V05_SUS_LDO
PP1V05_SUS
MIN_LINE_WIDTH=0.4 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=1.05V MAKE_BASE=TRUE
=PP1V05_SUS_PCH_JTAG

=PPCPUVCCIO_S0_REG
PP1V05_S0
MIN_LINE_WIDTH=0.6 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=1.05V MAKE_BASE=TRUE
=PP1V05_S0_CPU_VCCIO
=PPVCCIO_S0_XDP
=PPVCCIO_S0_CPUIMVP
=PPVCCIO_S0_SMC
=PP1V05_S0_VMON
=PP1V05_S0_RMC

=PPPCHVCCIO_S0_REG
PP1V05_PCHVCCIO_S0
MIN_LINE_WIDTH=0.6 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=1.05V MAKE_BASE=TRUE
=PP1V05_S0_PCH_VCCIO_PLLPCIE
=PP1V05_S0_PCH_VCCADPLL
=PP1V05_S0_PCH_VCCIO
=PP1V05_S0_PCH_VCCIO_PCIE
=PP1V05_S0_PCH_VCCIO_SATA
=PP1V05_S0_PCH_VCCIO_CLK
=PP1V05_S0_PCH_VCCIO_USB
=PP1V05_S0_PCH_VCC_CORE
=PP1V05_S0_PCH_VCCASW
=PP1V05_S0_PCH_VCCIO_CLK
=PP1V05_S0_PCH_VCCDIFFCLK
=PP1V05_S0_PCH
=PP1V05_S0_PCH_VCCSSC
=PP1V05_S0_PCH_V_PROC_IO
=PP1V05_S0_PCH_VCCIO_PLLUSB
=PP1V05_S0_PCH_VCC_DMI
=PP1V05_S0_PCH_VCCIO_PLLFDI
=PP1V05_S0_PCH_VCCDMI_FDI
=PP1V05_S0_P1V05TBTFET_R

Defined here since TBT page does not know PBUS voltage
16cp PPVIN_SW_TBTBST 37
VOLTAGE=12.8V

Backlight Rails

=PPBUS_SW_BKL
PPBUS_SW_BKL
MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.25 MM MAKE_BASE=TRUE VOLTAGE=12.6V
PPBUS_S0_LCDBKLT_PWR

SMC_T25_EN_L
NC_SMC_T25_EN_L
MAKE_BASE=TRUE

=PP1V05_S0_P1V05TBTFET
PP1V05_S0_P1V05TBTFET
MIN_LINE_WIDTH=0.4 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=1.05V MAKE_BASE=TRUE

"GPU" Rails

=PP3V3_S0GPU_FET
PP3V3_S0GPU
MIN_LINE_WIDTH=0.3 MM MIN_NECK_WIDTH=0.10MM VOLTAGE=3.3V MAKE_BASE=TRUE
=PP3V3_GPU_IFPX_PLLVDD
=PP3V3_S0_GFX3V3BIAS
=PP3V3_GPU_VDD33

=PP3V3_S0GPU_MISC_FET
PP3V3_S0GPU_MISC
MIN_LINE_WIDTH=0.3 MM MIN_NECK_WIDTH=0.10MM VOLTAGE=3.3V MAKE_BASE=TRUE
=PP3V3_GPU_MISC

TP_P1V8GPU_EN =P1V8GPU_EN

=PP1V5R1V35_GPU_REG
PP1V5R1V35_S0GPU
MIN_LINE_WIDTH=0.6 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=1.5V MAKE_BASE=TRUE
=PP1V35_GPU_FBVDDQ
=PP1V35_GPU_S0_FB

=PP1V8_GPU_FET
TP_GPU_PGOOD2
MAKE_BASE=TRUE

=PP1V05_S0GPU_REG
PP1V0_S0GPU_ISNS
MIN_LINE_WIDTH=0.6 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=1.05V MAKE_BASE=TRUE
=PP1V0_GPU_DPLL
=PP1V0_GPU_DP_AB
=PP1V0_GPU_DP_CD
=PP1V05_GPU_IFPCD_IOVDD
=PP1V05_GPU_IFPEF_IOVDD
=PP1V05_GPU_PEX_IOVDD
=PP1V05_GPU_PEX_PLLVDD

=PPVCORE_GPU_REG
PPVCORE_GPU
MIN_LINE_WIDTH=0.6 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=1.0V MAKE_BASE=TRUE
=PPVCORE_GPU
=PPVCORE_S0_GFX_REG

GND =LVDS_VCCA
MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.08SMM VOLTAGE=0V MAKE_BASE=TRUE

Chipset "VCore" Rails

=PPVCORE_S0_CPU_REG
PPVCORE_S0_CPU
MIN_LINE_WIDTH=0.6 MM MIN_NECK_WIDTH=0.25 MM MAKE_BASE=TRUE VOLTAGE=1.25V
=PPVCORE_S0_CPU

=PPVCORE_S0_AXG_REG
PPVCORE_S0_AXG
MIN_LINE_WIDTH=0.6 MM MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE VOLTAGE=1.05V
=PPVCORE_S0_CPU_VCCAXG

=PP1V5_S3_CPU_VCCDQ
PP1V5_S3_CPU_VCCDQ
MIN_LINE_WIDTH=0.6 MM MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE VOLTAGE=1.5V

=PP1V05_S0_CPU_VCCPQE
PP1V05_S0_CPU_VCCPQE
MIN_LINE_WIDTH=0.6 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=1.05V MAKE_BASE=TRUE

=PPVCCSA_S0_REG
PPVCCSA_S0_REG
MIN_LINE_WIDTH=0.6 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=0.9V MAKE_BASE=TRUE
=PPVCCSA_S0_CPU

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

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Power Aliases

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Frame Holes

ZT0915 2.8R2.3 — GND_BATT_CHGND

ZT0950 TH-NSP (SL-2.3X3.9-2.9X4.5) — GND_CHASSIS_FAN

ZT0974 TH-NSP (SL-1.1X0.45-1.4x0.75) — GND_CHASSIS_MLBCAN5

ZT0975 TH-NSP (SL-1.1X0.45-1.4x0.75) — GND_CHASSIS_MLBCAN6

GND (MAKE_BASE=TRUE) — GND_CHASSIS_MLBCAN4

ZT0970 TH-NSP (SL-1.1X0.45-1.4x0.75) — GND_CHASSIS_MLBCAN1

ZT0971 TH-NSP (SL-1.1X0.45-1.4x0.75) — GND_CHASSIS_MLBCAN2

ZT0972 TH-NSP (SL-1.1X0.45-1.4x0.75) — GND_CHASSIS_MLBCAN3

ZT0973 TH-NSP (SL-1.1X0.45-1.4x0.75) — GND_CHASSIS_MLBCAN4

THERMAL MODULE STANDOFFS

SH0920 STDOFF-4.5OD2.15H-SM
SH0927 STDOFF-4.5OD2.15H-SM
SH0926 STDOFF-4.5OD2.15H-SM
SH0925 STDOFF-4.5OD1.8H-SM
SH0928 STDOFF-4.5OD2.15H-SM
SH0921 STDOFF-4.5OD2.15H-SM-1
SH0929 STDOFF-4.5OD2.15H-SM
SH0923 STDOFF-4.5OD1.8H-SM
SH0922 STDOFF-4.5OD2.15H-SM
SH0930 STDOFF-4.5OD2.15H-SM
SH0924 STDOFF-4.5OD1.9H-SM
SH0946 STDOFF-4.9OD2.38H-SM-2
SH0945 STDOFF-4.9OD2.38H-SM-SL-2.6X2NP-2

APN 806-2247

BR0901 MLB-MTG-BRKT-J5

SH0950 SM — SHLD-J5-USB
SH0952 SM — SHLD-J5-CAN-FENCE-MDP-2
SH0951 SM — SHLD-J5-CAN-FENCE-MDP-1

POGO PINS

SH0931 POGO-2.3OD-5.5H-SM-LOW-FORCE SM
SH0932 POGO-2.3OD-5.5H-SM-LOW-FORCE SM
SH0933 POGO-2.3OD-5.5H-SM-LOW-FORCE SM
SH0934 POGO-2.3OD-5.5H-SM-LOW-FORCE SM
SH0935 POGO-2.3OD-5.5H-SM-LOW-FORCE SM
SH0936 POGO-2.3OD-5.5H-SM-LOW-FORCE SM
SH0940 2.8OD1.2ID-1.35H-SM
SH0941 2.8OD1.2ID-1.35H-SM
SH0944 2.8OD1.2ID-1.35H-SM
SH0942 2.8OD1.2ID-1.35H-SM
SH0943 2.8OD1.2ID-1.35H-SM

T29 / GMUX JTAG Signals

TBT_LSOE<3> — TBT_LSEO_LSOE3 (MAKE_BASE=TRUE, NO_TEST=TRUE) — TBT_LSEO<3>
TBT_LSOE<2> — TBT_LSEO_LSOE2 (MAKE_BASE=TRUE, NO_TEST=TRUE) — TBT_LSEO<2>

GMUX ALIASES

82 EG_RESET_L — GPU_RESET_L 71 78
18 LVDS_IG_BKL_ON — IG_BKLT_EN 82
18 LVDS_IG_PANEL_PWR — IG_LCD_PWR_EN 82
PEX_CLKREQ_L — EG_CLKREQ_IN_L 78 82
17 PEG_CLKREQ_L — EG_CLKREQ_OUT_L 82
82 DP_TBTSNK0_HPD_IG — DPA_IG_HPD 18 82
82 DP_TBTSNK1_HPD_IG — DPB_IG_HPD 18 82

17 PCIE_EXCARD_D2R_N — TRUE — NC_PCIE_EXCARD_D2R_N
17 PCIE_EXCARD_D2R_P — TRUE — NC_PCIE_EXCARD_D2R_P
17 PCIE_EXCARD_R2D_C_N — TRUE — NC_PCIE_EXCARD_R2D_C_N
17 PCIE_EXCARD_R2D_C_P — TRUE — NC_PCIE_EXCARD_R2D_C_P
(MAKE_BASE=TRUE)

92 17 PCIE_CLK100M_EXCARD_N — TRUE — NC_PCIE_CLK100M_EXCARD_N
92 17 PCIE_CLK100M_EXCARD_P — TRUE — NC_PCIE_CLK100M_EXCARD_P
(MAKE_BASE=TRUE)

17 TP_PCH_CLKOUT_DPN — TRUE — DPLL_REF_CLKN 11 89
17 TP_PCH_CLKOUT_DPP — TRUE — DPLL_REF_CLKP 11 89
(MAKE_BASE=TRUE)

17 TP_PCH_GPIO64_CLKOUTFLEX0 — TRUE — NC_PCH_GPIO64_CLKOUTFLEX0
17 TP_PCH_GPIO65_CLKOUTFLEX1 — TRUE — NC_PCH_GPIO65_CLKOUTFLEX1
17 TP_PCH_GPIO66_CLKOUTFLEX2 — TRUE — NC_PCH_GPIO66_CLKOUTFLEX2
17 TP_PCH_GPIO67_CLKOUTFLEX3 — TRUE — NC_PCH_GPIO67_CLKOUTFLEX3
(MAKE_BASE=TRUE)

SD_PWR_EN_PCH — ENET_LOW_PWR_PCH 20 24 25
38 7 SD_PWR_EN — ENET_LOW_PWR 25
TP_FW_PWR_EN — FW_PWR_EN 25
(MAKE_BASE=TRUE)

SMT GND TEST PONTS

ZT0990 2.1SM2.0MM-CIR SMT-PAD-NSP
ZT0991 2.1SM2.0MM-CIR SMT-PAD-NSP
ZT0992 2.1SM2.0MM-CIR SMT-PAD-NSP
SH0937 POGO-2.3OD-5.5H-SM-LOW-FORCE SM
ZT0993 2.1SM2.0MM-CIR SMT-PAD-NSP
SH0960 2.8OD1.2ID-1.35H-SM
SH0961 2.8OD1.2ID-1.35H-SM

Digital Ground

MLB_RAMCFG3 — RAMCFG3:L R0913 1K 5% 1/20W MF 201
MLB_RAMCFG2 — RAMCFG2:L R0912 1K 5% 1/20W MF 201
MLB_RAMCFG1 — RAMCFG1:L R0911 1K 5% 1/20W MF 201
MLB_RAMCFG0 — RAMCFG0:L R0910 1K 5% 1/20W MF 201

CPU signals

CPU_VID<0..6> (MAKE_BASE=TRUE) — CPUIMVP_VID<0..6>
TP_CPU_VTT_SELECT (MAKE_BASE=TRUE) — CPU_VTTSELECT
27 MEMVTT_EN (MAKE_BASE=TRUE) — =DDRVTT_EN 27 64

Unused PEG signals

NC_PEG_D2R_P<15..14> — =PEG_D2R_P<15..14> 10
NC_PEG_D2R_N<15..14> — =PEG_D2R_N<15..14> 10
NC_PEG_R2D_C_P<15..14> — =PEG_R2D_C_P<15..14> 10
NC_PEG_R2D_C_N<15..14> — =PEG_R2D_C_N<15..14> 10
(MAKE_BASE=TRUE, NO_TEST=TRUE)

T29 Signals Through PEG

92 35 PCIE_TBT_D2R_P<3..0> — =PEG_D2R_P<11..8> 10
92 35 PCIE_TBT_D2R_N<3..0> — =PEG_D2R_N<11..8> 10
92 35 PCIE_TBT_R2D_C_P<3..0> — =PEG_R2D_C_P<11..8> 10
92 35 PCIE_TBT_R2D_C_N<3..0> — =PEG_R2D_C_N<11..8> 10
(MAKE_BASE=TRUE)

GPU signals

89 88 71 PEG_D2R_P<7..0> — =PEG_D2R_P<7..0> 10
89 88 71 PEG_D2R_N<7..0> — =PEG_D2R_N<7..0> 10
89 71 PEG_R2D_C_P<7..0> — =PEG_R2D_C_P<7..0> 10
89 71 PEG_R2D_C_N<7..0> — =PEG_R2D_C_N<7..0> 10
(MAKE_BASE=TRUE)

UNUSED TBT PORTS

TBT_D2R_P<3..2> — NC_TBT_D2RP<3..2> (MAKE_BASE=TRUE, NO_TEST=TRUE)
TBT_D2R_N<3..2> — NC_TBT_D2RN<3..2> (MAKE_BASE=TRUE, NO_TEST=TRUE)
TBT_R2D_C_P<3..2> — NC_TBT_R2D_CP<3..2> (MAKE_BASE=TRUE, NO_TEST=TRUE)
TBT_R2D_C_N<3..2> — NC_TBT_R2D_CN<3..2> (MAKE_BASE=TRUE, NO_TEST=TRUE)

DPMUX TX & RX

82 DPMUX_UC_BOOT_TX — DPMUX_UC_TX (MAKE_BASE=TRUE) 82
82 DPMUX_UC_BOOT_RX — DPMUX_UC_RX (MAKE_BASE=TRUE) 82

SSD PCIE SIGNALS

92 39 PCIE_SSD_D2R_P<1..0> — =PEG_D2R_P<13..12> 10
92 39 PCIE_SSD_D2R_N<1..0> — =PEG_D2R_N<13..12> 10
92 39 PCIE_SSD_R2D_C_P<1..0> — =PEG_R2D_C_P<13..12> 10
92 39 PCIE_SSD_R2D_C_N<1..0> — =PEG_R2D_C_N<13..12> 10
(MAKE_BASE=TRUE)

TP_PCIE_CLK100M_FW_P — PCIE_CLK100M_FW_P 17 92
TP_PCIE_CLK100M_FW_N — PCIE_CLK100M_FW_N 17 92
(MAKE_BASE=TRUE)

UNUSED FDI SIGNALS

NC_PCH_FDI_DATA_N<7..0> — =FDI_DATA_N<7..0> 18
NC_PCH_FDI_DATA_P<7..0> — =FDI_DATA_P<7..0> 18
NC_PCH_FDI_FSYNC<1..0> — =FDI_FSYNC<1..0> 18
NC_PCH_FDI_LSYNC<1..0> — =FDI_LSYNC<1..0> 18
(MAKE_BASE=TRUE, NO_TEST=TRUE)

NC_CPU_FDI_DATA_N<7..0> — FDI_DATA_N<7..0> 10 89
NC_CPU_FDI_DATA_P<7..0> — FDI_DATA_P<7..0> 10 89
NC_CPU_FDI_FSYNC<1..0> — FDI_FSYNC<1..0> 10 89
NC_CPU_FDI_LSYNC<1..0> — FDI_LSYNC<1..0> 10 89
(MAKE_BASE=TRUE, NO_TEST=TRUE)

USB SIGNALS

91 34 USB_BT_P — USBHUB_DN1_P 26
91 34 USB_BT_N — USBHUB_DN1_N 26
91 49 USB_TPAD_P — USBHUB_DN2_P 26
91 49 USB_TPAD_N — USBHUB_DN2_N 26
91 41 USB_SMC_P — USBHUB_DN3_P 26
91 41 USB_SMC_N — USBHUB_DN3_N 26
PU_USBHUB_DN4P — USBHUB_DN4_P 26
PU_USBHUB_DN4N — USBHUB_DN4_N 26
(MAKE_BASE=TRUE)

8 =PP5V_S0_AUDIO_XW

XW0902 SM — PP5V_S0_AUDIO_AMP_L 57
XW0903 SM — PP5V_S0_AUDIO_AMP_R 57
(MIN_LINE_WIDTH=0.4MM, MIN_NECK_WIDTH=0.2MM, VOLTAGE=5V)

LVDS

NC_LVDS_IG_A_DATAP<3> — LVDS_IG_A_DATA_P<3> 18 91
NC_LVDS_IG_A_DATAN<3> — LVDS_IG_A_DATA_N<3> 18 91
NC_LVDS_IG_B_DATAP<3> — LVDS_IG_B_DATA_P<3> 18
NC_LVDS_IG_B_DATAN<3> — LVDS_IG_B_DATA_N<3> 18
NC_LVDS_IG_A_CLK_N — LVDS_IG_A_CLK_N 18 91
NC_LVDS_IG_A_CLK_P — LVDS_IG_A_CLK_P 18 91
NC_LVDS_IG_A_DATA_N<2..0> — LVDS_IG_A_DATA_N<2..0> 18 91
NC_LVDS_IG_A_DATA_P<2..0> — LVDS_IG_A_DATA_P<2..0> 18 91
NC_LVDS_IG_B_DATA_N<2..0> — LVDS_IG_B_DATA_N<2..0> 18 91
NC_LVDS_IG_B_DATA_P<2..0> — LVDS_IG_B_DATA_P<2..0> 18 91
NC_LVDS_IG_DDC_CLK — LVDS_IG_DDC_CLK 18
NC_LVDS_IG_DDC_DATA — LVDS_IG_DDC_DATA 18
(MAKE_BASE=TRUE, NO_TEST=TRUE)

PCIE

NC_PCIE_FW_D2RN — PCIE_FW_D2R_N 17
NC_PCIE_FW_D2RP — PCIE_FW_D2R_P 17
NC_PCIE_FW_R2D_CN — PCIE_FW_R2D_C_N 17
NC_PCIE_FW_R2D_CP — PCIE_FW_R2D_C_P 17
(MAKE_BASE=TRUE, NO_TEST=TRUE)

SATA

NC_SATA_ODD_R2D_N — SATA_ODD_D2R_N 17 91
NC_SATA_ODD_R2D_P — SATA_ODD_D2R_P 17 91
NC_SATA_ODD_R2D_C_N — SATA_ODD_R2D_C_N 17 91
NC_SATA_ODD_R2D_C_P — SATA_ODD_R2D_C_P 17 91
(MAKE_BASE=TRUE)

NC_DP_IG_MLP<3..0> — TP_DP_IG_B_MLP<3..0> 18
NC_DP_IG_MLN<3..0> — TP_DP_IG_B_MLN<3..0> 18
(MAKE_BASE=TRUE, NO_TEST=TRUE)

TBTBST:N

37 8 =PPVIN_SW_TBTBST — R0950 0 5% 1/8W MF-LF 805 — =PP15V_TBT_REG 8 37

UNUSED USB SIGNALS

NC_USB3_EXTD_TX_P — USB3_EXTD_TX_P 19
NC_USB3_EXTD_TX_N — USB3_EXTD_TX_N 19
NC_USB3_EXTD_RX_P — USB3_EXTD_RX_P 19
NC_USB3_EXTD_RX_N — USB3_EXTD_RX_N 19
NC_USB_EXTD_EHCI_P — USB_EXTD_EHCI_P 19
NC_USB_EXTD_EHCI_N — USB_EXTD_EHCI_N 19
NC_USB3_EXTC_TX_P — USB3_EXTC_TX_P 19 91
NC_USB3_EXTC_TX_N — USB3_EXTC_TX_N 19 91
NC_USB3_EXTC_RX_P — USB3_EXTC_RX_P 19 91
NC_USB3_EXTC_RX_N — USB3_EXTC_RX_N 19 91
NC_USB_EXTC_P — USB_EXTC_P 19 91
NC_USB_EXTC_N — USB_EXTC_N 19 91
(MAKE_BASE=TRUE, NO_TEST=TRUE)

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

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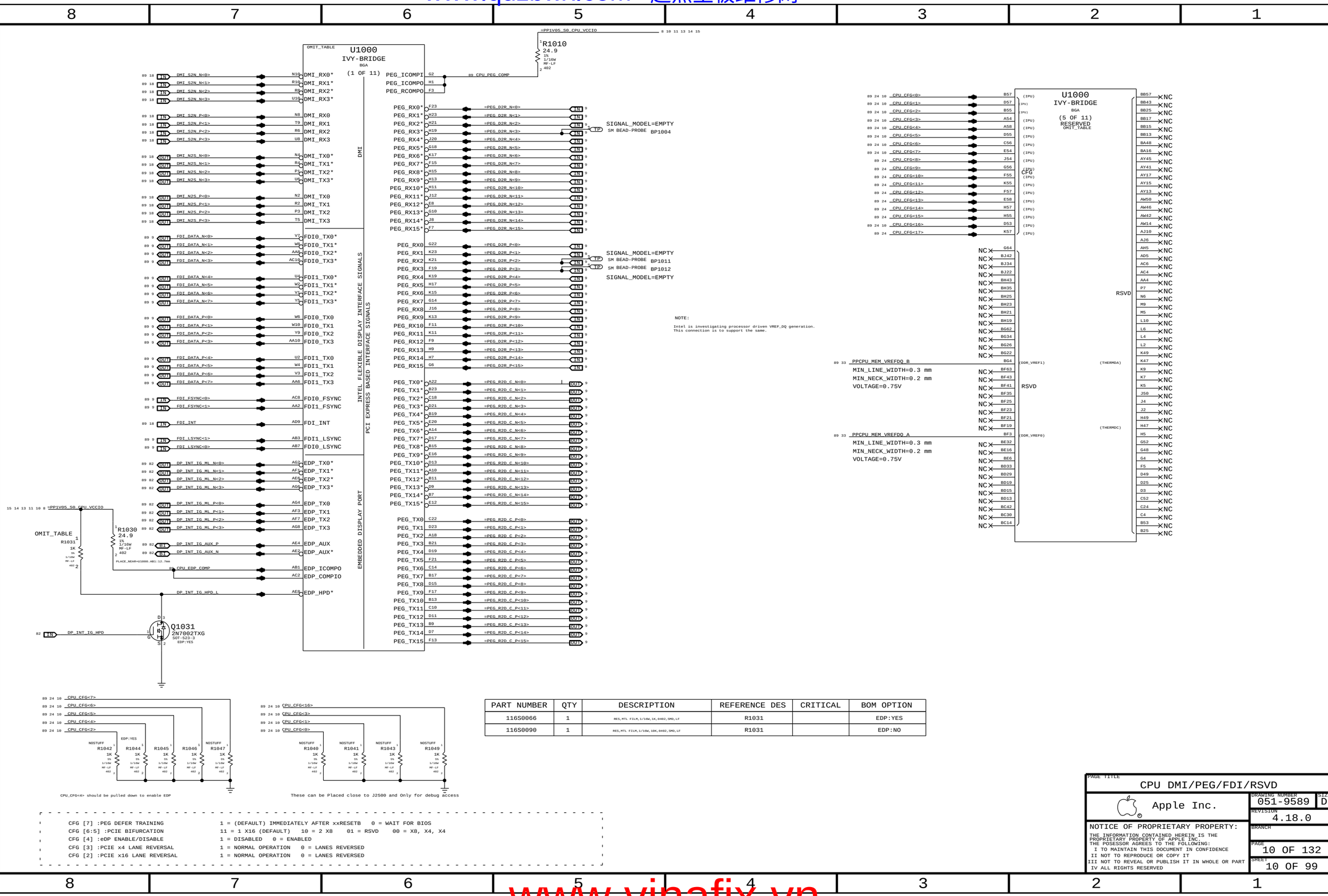

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0066	1	RES,MTL FILM,1/16W,1K,0402,SMD,LF	R1031		EDP:YES
116S0090	1	RES,MTL FILM,1/16W,10K,0402,SMD,LF	R1031		EDP:NO

CFG [7] :PEG DEFER TRAINING	1 = (DEFAULT) IMMEDIATELY AFTER xxRESETB	0 = WAIT FOR BIOS
CFG [6:5] :PCIE BIFURCATION	11 = 1 X16 (DEFAULT)	10 = 2 X8 01 = RSVD 00 = X8, X4, X4
CFG [4] :eDP ENABLE/DISABLE	1 = DISABLED	0 = ENABLED
CFG [3] :PCIE x4 LANE REVERSAL	1 = NORMAL OPERATION	0 = LANES REVERSED
CFG [2] :PCIE x16 LANE REVERSAL	1 = NORMAL OPERATION	0 = LANES REVERSED

PAGE TITLE: CPU DMI/PEG/FDI/RSVD

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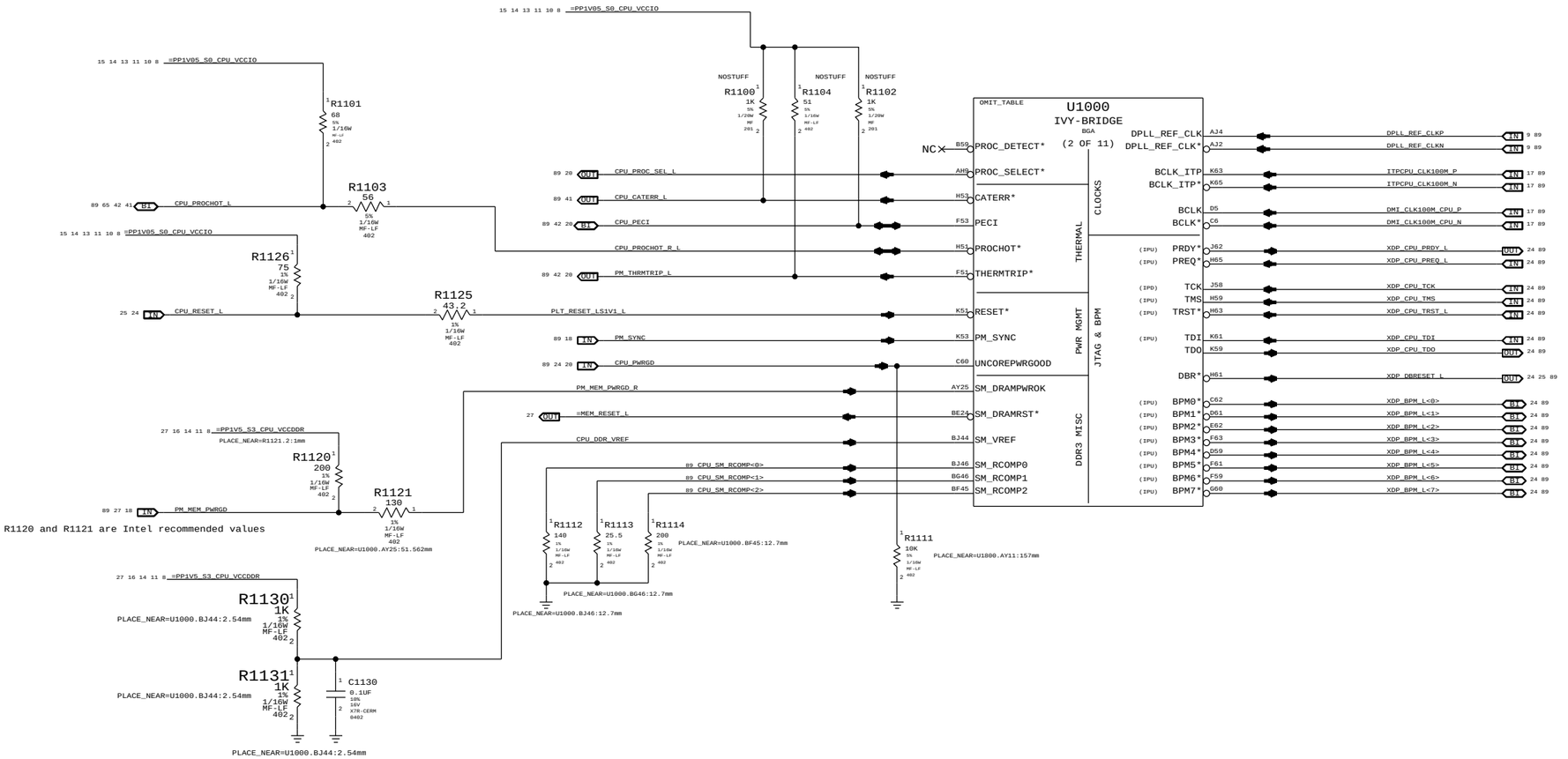

PAGE TITLE
CPU CLOCK/MISC/JTAG

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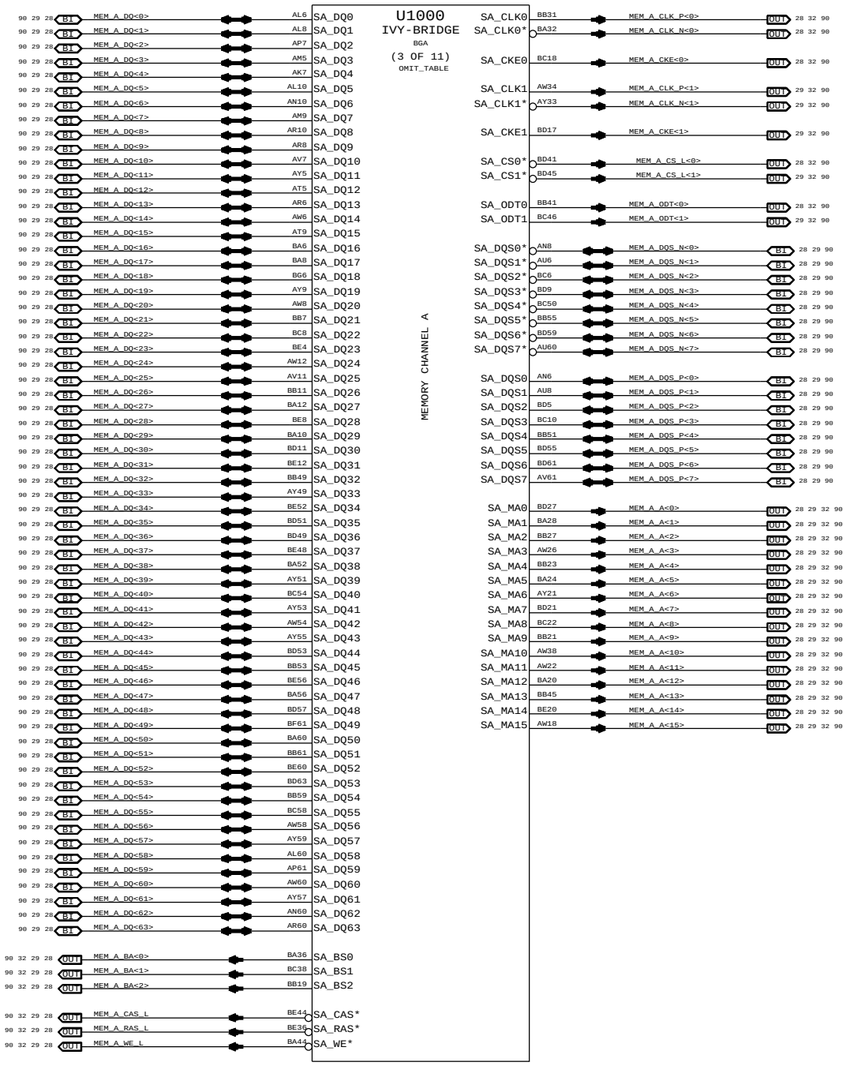

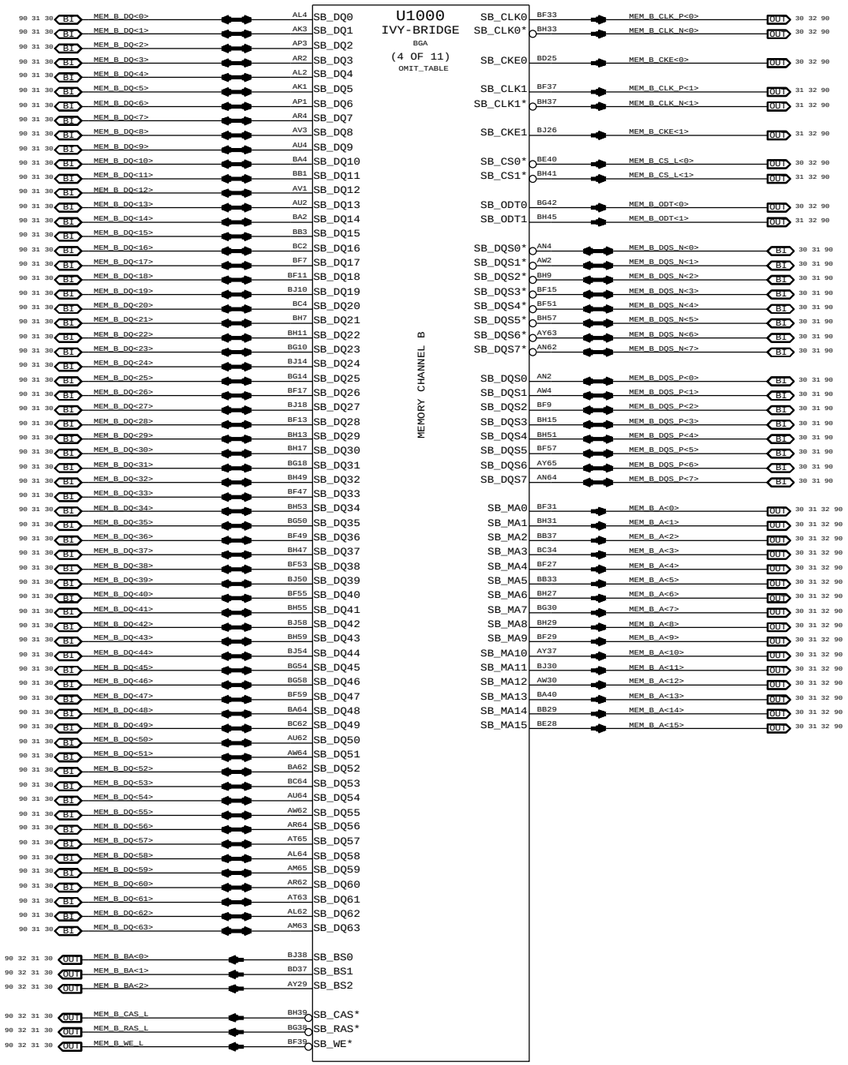

SYNC DATE=01/13/2012

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CPU DDR3 INTERFACES

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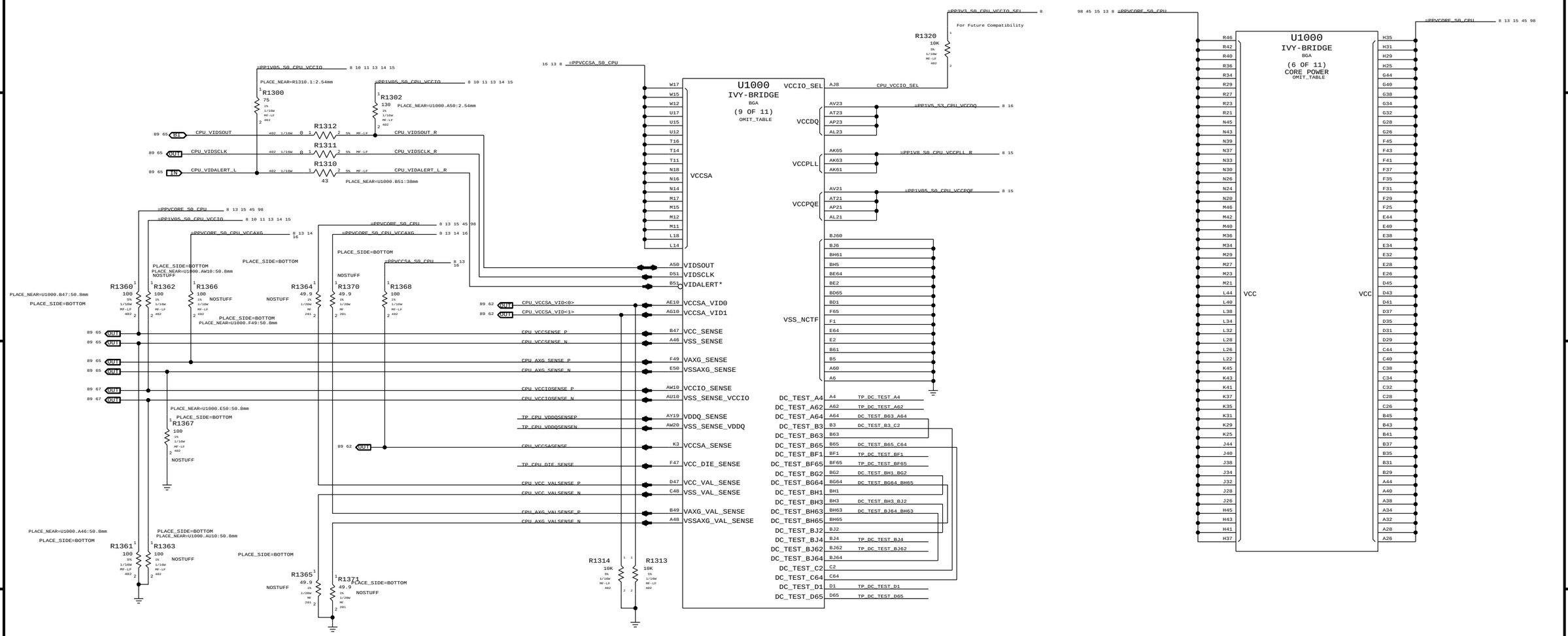

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE: CPU POWER

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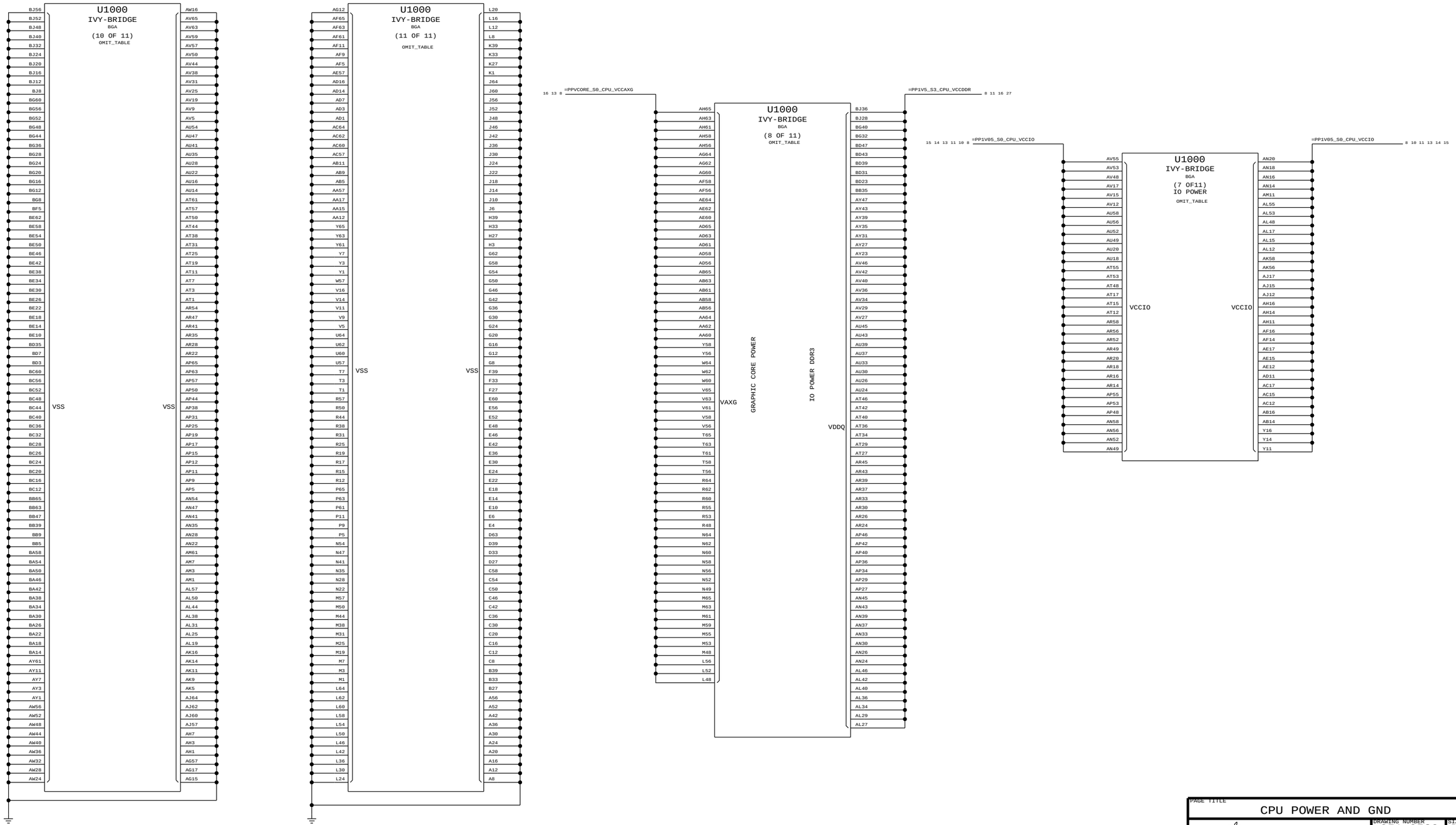

PAGE TITLE	CPU POWER AND GND
	Apple Inc.
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CPU VCORE DECOUPLING

Intel recommendation: 4x 470uF 4mOhm, 2x 470uF 4mOhm (NOSTUFF), 16x 22uF 0805, 4x 10uF 0603, 20x 1uF 0402, 28x 1uF 0402 (NOSTUFF)
Apple Implementation: 8x 270uF 6mOhm, 0x 470uF 4mOhm , 16x 22uF 0402, 4x 10uF 0402, 20x 1uF 0402, 28x 1uF 0201 (NOSTUFF), 4x 22uF 0402 (NOSTUFF)

98 45 13 8 =PPVCORE_S0_CPU

PLACEMENT_NOTE (C1600-C16C7):
Place on bottom side of U1000

C1600 C1601 C1602 C1603 C1604 C1605 C1606 C1607 C1608 C1609 C1610 C1611 C1612 C1613 C1614 C1615 C1616 C1617 C1618 C1619
1UF 10% 10V X6S-CERM 0402

NOSTUFF C16A0 C16A1 C16A2 C16A3 C16A4 C16A5 C16A6 C16A7 C16A8 C16A9 C16B0 C16B1 C16B2 C16B3 C16B4 C16B5 C16B6 C16B7 C16B8 C16B9
1UF 20% 4V CERM-X6S 0201

NOSTUFF C16C0 C16C1 C16C2 C16C3 C16C4 C16C5 C16C6 C16C7
1UF 20% 4V CERM-X6S 0201

PLACEMENT_NOTE (C1620-C1623):
Place near inductors on bottom side.
Place near U1000 on bottom side

C1620 C1621 C1622 C1623
10UF 20% 4V X6S 0402

NOSTUFF CRITICAL C1690 C1691 C1698 C1693 C1694 C1695 C1696 C1699
20UF 20% 2V X6T-CERM 0402

PLACEMENT_NOTE (C1624-C16D5):
Place near inductors on bottom side.

CRITICAL C1624 C1625 C1626 C1627 C1628 C1629 C1630 C1631 C1632 C1633 C1634 C1635 C1636 C1637 C1638 C1639 C16D0 C16D1 C16D2 C16D3 C16D4 C16D5
20UF 20% 2V X6T-CERM 0402
(NOSTUFF: C1628, C1632, C1633, C1634, C1636, C1638, C16D0, C16D1, C16D2, C16D3, C16D4, C16D5)

PLACEMENT_NOTE (C1640-C1645):

CRITICAL C1640 C1641 C1642 C1643 C1644 C1645 C1688 C1689
270UF 20% 2V TANT CASE-B2-SM

CPU VCCIO/VCCPQ DECOUPLING

Intel recommendation: 2x 330uF, 10x 10uF 0603, 26x 1uF 0402
Apple Implementation: 2x 330uF, 10x 10uF 0603, 26x 1uF 0402

PLACEMENT_NOTE (C1646-C1671):
Place on bottom side of U1000

13 11 10 8 14 =PP1V05_S0_CPU_VCCIO

C1646 C1647 C1648 C1649 C1650 C1651 C1652 C1653 C1654 C1655 C1656 C1657 C1658
1UF 10% 10V X6S-CERM 0402

C1659 C1660 C1661 C1662 C1663 C1664 C1665 C1666 C1667 C1668 C1669 C1670 C1671
1UF 10% 10V X6S-CERM 0402

PLACEMENT_NOTE (C1672-C1681):
Place near U1000 on bottom side

C1672 C1673 C1674 C1675 C1676 C1677 C1678 C1679 C1680 C1681
10UF 20% 4V X6S-CERM 0603

CRITICAL C1682 330UF-6MOHM 20% 2.0V POLY-TANT D15T-ECGLT-COMBO
CRITICAL C1683 330UF-6MOHM 20% 2.0V POLY-TANT D15T-ECGLT-COMBO
(Z = 1.5mm, place on tall side next to CPU & under heat pipe)

Intel recommendation: 1x 10mOhn resistor, 1x 1uF 0402

R1601 0.010 2% 1/4W MF 0603
=PP1V05_S0_CPU_VCCPQE 8 13
C1684 1UF 10% 10V X6S-CERM 0402

CPU VCCPLL DECOUPLING

R1600 0 5% 1/10W MF-LF 402
8 =PP1V8_S0_CPU_VCCPLL
=PP1V8_S0_CPU_VCCPLL_R 8 13
PLACE_NEAR=U1000.AK61:5MM
C1685 1UF 10% 10V X6S-CERM 0402
C1686 1UF 10% 10V X6S-CERM 0402
CRITICAL C1687 220UF 20% 2.5V TANT B16 (Z = 1.2mm, place on short side behind CPU)
PLACE_NEAR=U1000.AK63:2.54 mm:NO_VIA
PLACE_NEAR=U1000.AK65:2.54 mm:NO_VIA

CPU VCCPLL Low pass filter

SYNC_MASTER=D2_SEAN SYNC_DATE=03/05/2012

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VAXG DECOUPLING

INTEL RECOMMENDATION: 2X 470UF 4MOHM, 2X 470UF 4MOHM (NOSTUFF), 6X 22UF 0805, 2X 22UF 0805 (NOSTUFF), 6X 10UF 0603, 2X 10UF 0603 (NOSTUFF), 9X 1UF 0402, 9X 1UF 0402 (NOSTUFF)
APPLE IMPLEMENTATION: 0X 470UF 4MOHM, 3X 330UF 9MOHM , 6X 22UF 0603, 2X 22UF 0603 (NOSTUFF), 6X 10UF 0402, 2X 10UF 0402 (NOSTUFF), 9X 1UF 0402, 9X 1UF 0402 (NOSTUFF)

14 13 8 =PPVCORE_S0_CPU_VCCAXG

PLACEMENT_NOTE (C1700-C1708):
Place on bottom side of U1000

C1700 C1701 C1702 C1703 C1704 C1705 C1706 C1707 C1708 NOSTUFF C1709 NOSTUFF C1710 NOSTUFF C1711 NOSTUFF C1712 NOSTUFF C1713 NOSTUFF C1714 NOSTUFF C1715 NOSTUFF C1716 NOSTUFF C1717
1UF 10% 10V X6S-CERM 0402

PLACEMENT_NOTE (C1718-C1723):
Place close to U1000 on bottom side

C1718 C1719 C1720 C1721 C1722 C1723 NOSTUFF C1724 NOSTUFF C1725
10UF 20% 4V X6S 0402

PLACEMENT_NOTE (C1726-C1731):
Place near inductors on bottom side.

C1726 C1727 C1728 C1729 C1730 C1731 NOSTUFF C1732 NOSTUFF C1733
22UF 20% 4V X6S 0603

PLACEMENT_NOTE (C1734-C1735):

CRITICAL C1734 330UF-6MOHM 20% 2.0V POLY-TANT D15T
CRITICAL C1735 330UF-6MOHM 20% 2.0V POLY-TANT D15T
CRITICAL C1737 330UF-6MOHM 20% 2.0V POLY-TANT D15T
(Z = 1.5mm, place on tall side next to CPU & under heat pipe)

CPU VDDQ/VCCDQ DECOUPLING

Intel recommendation: 1x 330uF, 8x 10uF 0603, 10x 1uF 0402
Apple Implementation: 1x 330uF, 8x 10uF 0603, 10x 1uF 0402

27 14 11 8 =PP1V5_S3_CPU_VCCDDR

PLACEMENT_NOTE (C1738-C1747):
Place on bottom side of U1000

C1738 C1739 C1740 C1741 C1742 C1743 C1744 C1745 C1746 C1747
1UF 10% 10V X6S-CERM 0402

Place close to U1000 on bottom side

C1748 C1749 C1750 C1751 C1752 C1753 C1754 C1755
10UF 20% 4V X6S-CERM 0603

Place near inductors on bottom side

C1756 330UF-0.006OHM 20% 2V POLY CASE-D2-SM

Intel recommendation: 1x 10mOhn resistor, 1x 1uF 0402

R1700 0.010 1% 1/4W MF 0603
=PP1V5_S3_CPU_VCCDQ 8 13
C1757 1UF 10% 10V X6S-CERM 0402

CPU VCCSA DECOUPLING

Intel recommendation: 1x 330uF, 5x 10uF 0603, 5x 1uF 0402
Apple Implementation: 1x 330uF, 5x 10uF 0603, 5x 1uF 0402

13 8 =PPVCCSA_S0_CPU

PLACEMENT_NOTE (C1758-C1762):
Place on bottom side of U1000

C1758 C1759 C1760 C1761 C1762
1UF 10% 10V X6S-CERM 0402

C1763 C1764 C1765 C1766 C1767
10UF 20% 4V X6S-CERM 0603

CRITICAL C1768 330UF-6MOHM 20% 2.0V POLY-TANT DIST-ECGLT-COMBO
(Z = 1.5mm, place on tall side next to CPU & under heat pipe)

SYNC_MASTER=D2_SEAN SYNC_DATE=03/05/2012

PAGE TITLE: CPU DECOUPLING-II

Apple Inc.

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OMIT_TABLE

U1800 PANTHERPOINT MOBILE FCBGA (1 OF 10)

SYSCLK_CLK32K_RTC — NCX — RTCX1 / RTCX2

RTC_RESET_L — RTCRST*
PCH_SRTCRST_L — SRTCRST*
PCH_INTRUDER_L — INTRUDER*
PCH_INTVRMEN_L — INTVRMEN

RTC

LPC
- FWH0/LAD0 — LPC_AD_R<0>
- FWH1/LAD1 — LPC_AD_R<1>
- FWH2/LAD2 — LPC_AD_R<2>
- FWH3/LAD3 — LPC_AD_R<3>
- (IPU) FWH4/LFRAME* — LPC_FRAME_R_L
- (IPU) LDRQ0* — TP_LPC_DREQ00_L
- (IPU) LDRQ1*/GPIO23 — TBT_PWR_EN_PCH (OUT 25)
- SERIRQ — LPC_SERIRQ (BI 7 41 43)

=PP3V3_S0_PCH — R1820 10K 5% 1/20W MF 201

IHDA
- HDA_BIT_CLK_R — HDA_BCLK
- HDA_SYNC_R — HDA_SYNC (IPD-BOOT)
- VSel strap not functional (VCCVRM = 1.8V) — PCH_SPKR — SPKR (IPD-PLTRST#)
- HDA_RST_R_L — HDA_RST*
- HDA_SDIN0 — HDA_SDIN0 (IPD)
- TP_HDA_SDIN1 — HDA_SDIN1 (IPD)
- TP_HDA_SDIN2 — HDA_SDIN2 (IPD)
- TP_HDA_SDIN3 — HDA_SDIN3 (IPD)
- HDA_SDOUT_R — HDA_SDO (IPD-BOOT)

JTAG
- JTAG_ISP_TMS — HDA_DOCK_EN*/GPIO33
- ENET_MEDIA_SENSE_RDIV — HDA_DOCK_RST*/GPIO13
- XDP_PCH_TCK — JTAG_TCK (IPD)
- XDP_PCH_TMS — JTAG_TMS (IPU)
- XDP_PCH_TDI — JTAG_TDI (IPU)
- XDP_PCH_TDO — JTAG_TDO

SPI
- SPI_CLK_R — SPI_CLK
- SPI_CS0_R_L — SPI_CS0*
- TP_SPI_CS1_L — SPI_CS1*
- SPI_MOSI_R — SPI_MOSI (IPD-BOOT)
- SPI_MISO — SPI_MISO (IPU)

SATA
- SATA0RXN — SATA_HDD_D2R_N (IN 39 91)
- SATA0RXP — SATA_HDD_D2R_P (IN 39 91)
- SATA0TXN — SATA_HDD_R2D_C_N (OUT 39 91)
- SATA0TXP — SATA_HDD_R2D_C_P (OUT 39 91)
- SATA1RXN — SATA_ODD_D2R_N (IN 9 91)
- SATA1RXP — SATA_ODD_D2R_P (IN 9 91)
- SATA1TXN — SATA_ODD_R2D_C_N (OUT 9 91)
- SATA1TXP — SATA_ODD_R2D_C_P (OUT 9 91)
- SATA2RXN — TP_SATA_C_D2RN
- SATA2RXP — TP_SATA_C_D2RP
- SATA2TXN — TP_SATA_C_R2D_CN
- SATA2TXP — TP_SATA_C_R2D_CP
- SATA3RXN — TP_SATA_D_D2RN (7)
- SATA3RXP — TP_SATA_D_D2RP (7)
- SATA3TXN — TP_SATA_D_R2D_CN (7)
- SATA3TXP — TP_SATA_D_R2D_CP (7)
- SATA4RXN — TP_SATA_E_D2RN (7)
- SATA4RXP — TP_SATA_E_D2RP (7)
- SATA4TXN — TP_SATA_E_R2D_CN (7)
- SATA4TXP — TP_SATA_E_R2D_CP (7)
- SATA5RXN — TP_SATA_F_D2RN (7)
- SATA5RXP — TP_SATA_F_D2RP (7)
- SATA5TXN — TP_SATA_F_R2D_CN (7)
- SATA5TXP — TP_SATA_F_R2D_CP (7)
- SATAICOMPO — PCH_SATAICOMP (91)
- SATAICOMPI
- SATA3RCOMPO
- SATA3COMPI — PCH_SATA3COMP (91)
- SATA3RBIAS — PCH_SATA3RBIAS
- SATALED* — PCH_SATALED_L (17)
- SATA0GP/GPIO21 — XDP_DC2_PCH_GPIO21_DP_AUXCH_ISOL (OUT 24)
- SATA1GP/GPIO19 (IPU) — XDP_DC3_PCH_GPIO19_SATARDRVR_EN (OUT 24)

=PP1V05_S0_PCH_VCCIO_SATA (8 21 23)
PLACE_NEAR=U1800.Y11:2.54mm
R1830 37.4 1% 1/20W MF 201

=PP1V05_S0_PCH (8 23)
R1831 49.9 1% 1/20W MF 201
PLACE_NEAR=U1800.AB12:2.54mm

PLACE_NEAR=U1800.AH1:2.54mm
R1832 750 1% 1/20W MF 201

=PPVRTC_G3_PCH (8 18 21)
R1800 330K 5% 1/20W MF 201
R1801 1M 5% 1/20W MF 201
R1802 20K 5% 1/20W MF 201
R1803 20K 5% 1/20W MF 201
RTC_RESET_L (17)
PCH_SRTCRST_L (17)
PCH_INTRUDER_L (17)
PCH_INTVRMEN_L (17)
C1802 1UF 10% 10V X5R 402
C1803 1UF 10% 10V X5R 402

LPC_AD_R<0> (17)	R1860	33	5%	1/20W	MF	201	LPC_AD<0> (BI 7 41 43 82 92)
LPC_AD_R<1> (17)	R1861	33	5%	1/20W	MF	201	LPC_AD<1> (BI 7 41 43 82 92)
LPC_AD_R<2> (17)	R1862	33	5%	1/20W	MF	201	LPC_AD<2> (BI 7 41 43 82 92)
LPC_AD_R<3> (17)	R1863	33	5%	1/20W	MF	201	LPC_AD<3> (BI 7 41 43 82 92)
LPC_FRAME_R_L (17)	R1864	33	5%	1/20W	MF	201	LPC_FRAME_L (OUT 7 41 43 82 92)
HDA_BIT_CLK_R (92 17)	R1810	33	5%	1/20W	MF	201	HDA_BIT_CLK (OUT 53 92)
HDA_SYNC_R (92 17)	R1811	33	5%	1/20W	MF	201	HDA_SYNC (OUT 53 92)
HDA_RST_R_L (92 17)	R1812	33	5%	1/20W	MF	201	HDA_RST_L (OUT 53 92)
HDA_SDOUT_R (92 25 17)	R1813	33	5%	1/20W	MF	201	HDA_SDOUT (OUT 53 92)

PLACE_NEAR=U1800.N34:1.27mm
PLACE_NEAR=U1800.L34:1.27mm
PLACE_NEAR=U1800.K34:1.27mm
PLACE_NEAR=U1800.A36:1.27mm

=PP3V3_SUS_PCH_GPIO (8 18 19 20)
=PP3V3_S0_PCH_GPIO (8 18 19 20 25 37)

R1877	4.7K	5%	1/20W	MF	201	PCH_SPKR (17)		
R1878	4.7K	5%	1/20W	MF	201	PCH_SATALED_L (17)		
R1834	10K	5%	1/20W	MF	201	DP_AUXCH_ISOL (24 25)		
R1833	10K	5%	1/20W	MF	201	SATARDRVR_EN (24)		
R1842	10K	5%	1/20W	MF	201	FW_CLKREQ_L (17)		
R1869	10K	5%	1/20W	MF	201	AP_CLKREQ_L (17 34)		
R1844	10K	5%	1/20W	MF	201	EXCARD_CLKREQ_L (17)		
R1845	10K	5%	1/20W	MF	201	JTAG_DPMUXUC_TRST_L (17)		
R1847	10K	5%	1/20W	MF	201	ENET_CLKREQ_L (7 17 38)		
R1814	10K	5%	1/20W	MF	201	PEG_CLKREQ_L (9 17)		
R1815	10K	5%	1/20W	MF	201	TBT_CLKREQ_L (17 37)		
R1843	10K	5%	1/20W	MF	201	SSD_CLKREQ_L (17 39)		
R1846	10K	5%	1/20W	MF	201	PEGCLKROA_L_GPIO47 (17)		
GPU:1P R1848	10K	5%	1/20W	MF	201	PEGCLKROB_L_GPIO56 (17)		
R1853	10K	5%	1/20W	MF	201	SMBUS_PCH_ALERT_L (17)		
R1854	10K	5%	1/20W	MF	201	USB_EXTB_SEL_XHCI (17 26)		
R1855	10K	5%	1/20W	MF	201	USB_EXTD_SEL_XHCI (17)		
R1879	10K	5%	1/20W	MF	201	ENET_MEDIA_SENSE_RDIV (17)		

Connect to ENET_MEDIA_SENSE via alias if HDA = 3.3V.
Connect to ENET_MEDIA_SENSE via 12K R if HDA = 1.5V.
If HDA = S0, must also ensure that signal cannot be high in S3.

NO STUFF R1840 0 5% 1/20W MF 201
ITPCPU_CLK100M_N (89 11) — ITPXDP_CLK100M_N (89 24)

NO STUFF R1841 0 5% 1/20W MF 201
ITPCPU_CLK100M_P (89 11) — ITPXDP_CLK100M_P (89 24)

GPU:2P R1880 10K 5% 1/20W MF 201 — PEGCLKROB_L_GPIO56 (17)

OMIT_TABLE

U1800 PANTHERPOINT MOBILE FCBGA (2 OF 10)

PCI-E* / C-LINK
- PCIE_ENET_D2R_N (92 38 7 IN) — PERN1
- PCIE_ENET_D2R_P (92 38 7 IN) — PERP1
- PCIE_ENET_R2D_C_N (92 38 7 OUT) — PETN1
- PCIE_ENET_R2D_C_P (92 38 7 OUT) — PETP1
- PCIE_AP_D2R_N (92 34 IN) — PERN2
- PCIE_AP_D2R_P (92 34 IN) — PERP2
- PCIE_AP_R2D_C_N (92 34 OUT) — PETN2
- PCIE_AP_R2D_C_P (92 34 OUT) — PETP2
- PCIE_FW_D2R_N (9 IN) — PERN3
- PCIE_FW_D2R_P (9 IN) — PERP3
- PCIE_FW_R2D_C_N (9 OUT) — PETN3
- PCIE_FW_R2D_C_P (9 OUT) — PETP3
- PCIE_EXCARD_D2R_N (9 IN) — PERN4
- PCIE_EXCARD_D2R_P (9 IN) — PERP4
- PCIE_EXCARD_R2D_C_N (9 OUT) — PETN4
- PCIE_EXCARD_R2D_C_P (9 OUT) — PETP4
- TP_PCIE_5_D2RN (7) — PERN5
- TP_PCIE_5_D2RP (7) — PERP5
- TP_PCIE_5_R2D_CN (7) — PETN5
- TP_PCIE_5_R2D_CP (7) — PETP5
- TP_PCIE_6_D2RN (7) — PERN6
- TP_PCIE_6_D2RP (7) — PERP6
- TP_PCIE_6_R2D_CN (7) — PETN6
- TP_PCIE_6_R2D_CP (7) — PETP6
- TP_PCIE_7_D2RN (7) — PERN7
- TP_PCIE_7_D2RP (7) — PERP7
- TP_PCIE_7_R2D_CN (7) — PETN7
- TP_PCIE_7_R2D_CP (7) — PETP7
- TP_PCIE_8_D2RN (7) — PERN8
- TP_PCIE_8_D2RP (7) — PERP8
- TP_PCIE_8_R2D_CN (7) — PETN8
- TP_PCIE_8_R2D_CP (7) — PETP8

CLOCKS
- PCIE_CLK100M_ENET_N (92 38 7 OUT) — CLKOUT_PCIE0N
- PCIE_CLK100M_ENET_P (92 38 7 OUT) — CLKOUT_PCIE0P
- SSD_CLKREQ_L (39 17 IN) — PCIECLKRQ0*/GPIO73
- PCIE_CLK100M_FW_N (92 9) — CLKOUT_PCIE1N
- PCIE_CLK100M_FW_P (92 9) — CLKOUT_PCIE1P
- FW_CLKREQ_L (17) — PCIECLKRQ1*/GPIO18
- PCIE_CLK100M_AP_N (92 34 OUT) — CLKOUT_PCIE2N
- PCIE_CLK100M_AP_P (92 34 OUT) — CLKOUT_PCIE2P
- AP_CLKREQ_L (34 17 IN) — PCIECLKRQ2*/GPIO20
- PCIE_CLK100M_EXCARD_N (92 9 OUT) — CLKOUT_PCIE3N
- PCIE_CLK100M_EXCARD_P (92 9 OUT) — CLKOUT_PCIE3P
- EXCARD_CLKREQ_L (17 IN) — PCIECLKRQ3*/GPIO25
- TP_PCIE_CLK100M_PE4N (7) — CLKOUT_PCIE4N
- TP_PCIE_CLK100M_PE4P (7) — CLKOUT_PCIE4P
- JTAG_DPMUXUC_TRST_L (17 OUT) — PCIECLKRQ4*/GPIO26
- PCIE_CLK100M_SSD_N (92 39 OUT) — CLKOUT_PCIE5N
- PCIE_CLK100M_SSD_P (92 39 OUT) — CLKOUT_PCIE5P
- ENET_CLKREQ_L (38 17 7 IN) — PCIECLKRQ5*/GPIO44 (IPU-RSMRST#)
- TP_PCIE_CLK100M_PEBN (7) — CLKOUT_PEG_B_N
- TP_PCIE_CLK100M_PEBP (7) — CLKOUT_PEG_B_P
- PEGCLKRQB_L_GPIO56 (17) — PEG_B_CLKRQ*/GPIO56
- PEG_CLK100M_N (92 71 OUT) — CLKOUT_PCIE6N
- PEG_CLK100M_P (92 71 OUT) — CLKOUT_PCIE6P
- PEG_CLKREQ_L (9 17 IN) — PCIECLKRQ6*/GPIO45
- PCIE_CLK100M_TBT_N (92 35 OUT) — CLKOUT_PCIE7N
- PCIE_CLK100M_TBT_P (92 35 OUT) — CLKOUT_PCIE7P
- TBT_CLKREQ_L (37 17 IN) — PCIECLKRQ7*/GPIO46 (IPU-RSMRST#)
- ITPXDP_CLK100M_N (89 24) — CLKOUT_ITPXDP_N
- ITPXDP_CLK100M_P (89 24) — CLKOUT_ITPXDP_P

Controlled by PCIECLKRQ5#

SMBUS
- SMBALERT*/GPIO11 — SMBUS_PCH_ALERT_L (17)
- SMBCLK — SMBUS_PCH_CLK (OUT 44 92)
- SMBDATA — SMBUS_PCH_DATA (BI 44 92)
- SML0ALERT*/GPIO60 — USB_EXTB_SEL_XHCI (OUT 17 26)
- SML0CLK — SML_PCH_0_CLK (OUT 44 92)
- SML0DATA — SML_PCH_0_DATA (BI 44 92)
- SML1ALERT*/PCHHOT*/GPIO74 — USB_EXTD_SEL_XHCI (OUT 17)
- SML1CLK/GPIO58 — SML_PCH_1_CLK (OUT 44 92)
- SML1DATA/GPIO75 — SML_PCH_1_DATA (BI 44 92)

C-LINK
- (IPU/IPD) CL_CLK1 — TP_CLINK_CLK (7)
- (IPU/IPD) CL_DATA1 — TP_CLINK_DATA (7)
- CL_RST1* — TP_CLINK_RESET_L (7)

CLOCKS
- PEG_A_CLKRQ*/GPIO47 — PEGCLKRQA_L_GPIO47 (17)
- CLKOUT_PEG_A_N — TP_PCIE_CLK100M_PEGAN
- CLKOUT_PEG_A_P — TP_PCIE_CLK100M_PEGAP
- CLKOUT_DMI_N — DMI_CLK100M_CPU_N (OUT 11 89)
- CLKOUT_DMI_P — DMI_CLK100M_CPU_P (OUT 11 89)
- CLKOUT_DP_N — TP_PCH_CLKOUT_DPN (OUT 9)
- CLKOUT_DP_P — TP_PCH_CLKOUT_DPP (OUT 9)
- CLKIN_DMI_N — PCIE_CLK100M_PCH_N (IN 17 92)
- CLKIN_DMI_P — PCIE_CLK100M_PCH_P (IN 17 92)
- CLKIN_GND1_N — PCH_CLKIN_GNDN1 (17)
- CLKIN_GND1_P — PCH_CLKIN_GNDP1 (17)
- CLKIN_DOT_96N — PCH_CLK96M_DOT_N (IN 17 92)
- CLKIN_DOT_96P — PCH_CLK96M_DOT_P (IN 17 92)
- CLKIN_SATA_N — PCH_CLK100M_SATA_N (IN 17 92)
- CLKIN_SATA_P — PCH_CLK100M_SATA_P (IN 17 92)
- REFCLK14IN — PCH_CLK14P3M_REFCLK (IN 17 92)
- CLKIN_PCILOOPBACK — PCH_CLK33M_PCIIN (IN 25 92)

33MHz clocks must be matched within 5"

- XTAL25_IN — SYSCLK_CLK25M_SB_R (17 91)
- XTAL25_OUT — NC
- =PP1V05_S0_PCH_VCCDIFFCLK (23 21 8)
- R1890 90.9 1% 1/20W MF 201
- PLACE_NEAR=U1800.Y47:2.54mm
- XCLK_RCOMP — PCH_XCLK_RCOMP

FLEX CLOCKS
- CLKOUTFLEX0/GPIO64 (IPD-PWROK) — TP_PCH_GPIO64_CLKOUTFLEX0 (9)
- CLKOUTFLEX1/GPIO65 (IPD-PWROK) — TP_PCH_GPIO65_CLKOUTFLEX1 (9)
- CLKOUTFLEX2/GPIO66 (IPD-PWROK) — TP_PCH_GPIO66_CLKOUTFLEX2 (9)
- CLKOUTFLEX3/GPIO67 (IPD-PWROK) — TP_PCH_GPIO67_CLKOUTFLEX3 (9)

SYSCLK_CLK25M_SB (91 25 IN) — R1872 604 1% 1/16W MF-LF 402 — SYSCLK_CLK25M_SB_R (17 91)
1.8V -> 1.1V
R1873 1K 1% 1/20W MF 201

Unused clock terminations for FCIM Mode

PCH_CLK96M_DOT_P (92 17)	R1891	10K	5%	1/20W	MF	201		
PCH_CLK96M_DOT_N (92 17)	R1892	10K	5%	1/20W	MF	201		
PCH_CLK100M_SATA_P (92 17)	R1893	10K	5%	1/20W	MF	201		
PCH_CLK100M_SATA_N (92 17)	R1894	10K	5%	1/20W	MF	201		
PCIE_CLK100M_PCH_P (92 17)	R1895	10K	5%	1/20W	MF	201		
PCIE_CLK100M_PCH_N (92 17)	R1896	10K	5%	1/20W	MF	201		
PCH_CLK14P3M_REFCLK (92 17)	R1897	10K	5%	1/20W	MF	201		
PCH_CLKIN_GNDP1 (17)	R1870	10K	5%	1/20W	MF	201		
PCH_CLKIN_GNDN1 (17)	R1871	10K	5%	1/20W	MF	201		

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE: PCH SATA/PCIe/CLK/LPC/SPI

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=PP3V3_SUS_PCH_GPIO 8 17 18 19 20
=PP1V05_S0_PCH_VCCIO_PCIE 8
PLACE_NEAR=U1800.BJ24:12.7mm
R1905 10K 5% 1/20W MF 201
R1900 49.9 1% 1/20W MF 201

OMIT_TABLE

U1800 PANTHERPOINT MOBILE FCBGA (3 OF 10)

DMI N2S N<0> BC24 DMI0RXN
DMI N2S N<1> BE20 DMI1RXN
DMI N2S N<2> BG18 DMI2RXN
DMI N2S N<3> BG20 DMI3RXN
DMI N2S P<0> BE24 DMI0RXP
DMI N2S P<1> BC20 DMI1RXP
DMI N2S P<2> BJ18 DMI2RXP
DMI N2S P<3> BJ20 DMI3RXP
DMI S2N N<0> AW24 DMI0TXN
DMI S2N N<1> AW20 DMI1TXN
DMI S2N N<2> BB18 DMI2TXN
DMI S2N N<3> AV18 DMI3TXN
DMI S2N P<0> AY24 DMI0TXP
DMI S2N P<1> AY20 DMI1TXP
DMI S2N P<2> AY18 DMI2TXP
DMI S2N P<3> AU18 DMI3TXP

PCH_DMI_COMP BJ24 DMI_ZCOMP
BG25 DMI_IRCOMP
PCH_DMI2RBIAS BH21 DMI2RBIAS

PLACE_NEAR=U1800.BH21:2.54mm
R1920 750 1% 1/20W MF 201

DMI

FDI_RXN0 BJ14 =FDI_DATA_N<0>
FDI_RXN1 AY14 =FDI_DATA_N<1>
FDI_RXN2 BE14 =FDI_DATA_N<2>
FDI_RXN3 BH13 =FDI_DATA_N<3>
FDI_RXN4 BC12 =FDI_DATA_N<4>
FDI_RXN5 BJ12 =FDI_DATA_N<5>
FDI_RXN6 BG10 =FDI_DATA_N<6>
FDI_RXN7 BG9 =FDI_DATA_N<7>
FDI_RXP0 BG14 =FDI_DATA_P<0>
FDI_RXP1 BB14 =FDI_DATA_P<1>
FDI_RXP2 BF14 =FDI_DATA_P<2>
FDI_RXP3 BG13 =FDI_DATA_P<3>
FDI_RXP4 BE12 =FDI_DATA_P<4>
FDI_RXP5 BG12 =FDI_DATA_P<5>
FDI_RXP6 BJ10 =FDI_DATA_P<6>
FDI_RXP7 BH9 =FDI_DATA_P<7>
FDI_INT AW16 FDI_INT
FDI_FSYNC0 AV12 =FDI_FSYNC<0>
FDI_FSYNC1 BC10 =FDI_FSYNC<1>
FDI_LSYNC0 AV14 =FDI_LSYNC<0>
FDI_LSYNC1 BB10 =FDI_LSYNC<1>

FDI

SYSTEM POWER MANAGEMENT

DSWVRMEN A18 PCH_DSWVRMEN
DPWROK E22 PM_DSW_PWRGD
WAKE* B9 PCIE_WAKE_L
CLKRUN*/GPIO32 N3 PM_CLKRUN_L
SUS_STAT*/GPIO61 G8 LPC_PWRDWN_L
SUSCLK/GPIO62 N14 PM_CLK32K_SUSCLK_R
SLP_S5*/GPIO63 D10 PM_SLP_S5_L
SLP_S4* H4 PM_SLP_S4_L
SLP_S3* F4 PM_SLP_S3_L
SLP_A* G10 TP_PM_SLP_A_L
SLP_SUS* G16 PM_SLP_SUS_L
PMSYNCH AP14 PM_SYNC
SLP_LAN*/GPIO29 K14 MEM_VDD_SEL_1V5_L

PCH_SUSACK_L 18 C12 SUSACK* (IPU)
PM_SYSRST_L 41 25 K3 SYS_RESET*
PM_PCH_SYS_PWROK 70 41 24 P12 SYS_PWROK
PM_PCH_PWROK 70 25 L22 PWROK
PM_PCH_APWROK 70 L10 APWROK
PM_MEM_PWRGD 89 27 11 B13 DRAMPWROK
PM_RSMRST_L 70 C21 RSMRST*
PCH_SUSWARN_L 18 K16 SUSWARN*/SUSPWRDNACK/GPIO30
PM_PWRBTN_L 41 24 18 E20 PWRBTN* (IPU)
SMC_ADAPTER_EN 70 42 41 H20 ACPRESENT/GPIO31 (IPD-DeepS4/S5)
PM_BATLOW_L 42 E10 BATLOW*/GPIO72 (IPU)
PCH_RI_L A10 RI*

=PPVRTC_G3_PCH 8 17 21
R1915 390K 5% 1/20W MF 201
R1909 100K 5% 1/20W MF 201

OMIT_TABLE

U1800 PANTHERPOINT MOBILE FCBGA (4 OF 10)

LVDS_IG_BKL_ON 18 9 J47 L_BKLTEN
LVDS_IG_PANEL_PWR 18 9 M45 L_VDD_EN
LVDS_IG_BKL_PWM 7 P45 L_BKLTCTL
LVDS_IG_DDC_CLK 9 T40 L_DDC_CLK
LVDS_IG_DDC_DATA 9 K47 L_DDC_DATA (IPD-PLTRST#)
TP_LVDS_IG_CTRL_CLK 7 T45 L_CTRL_CLK
TP_LVDS_IG_CTRL_DATA 7 P39 L_CTRL_DATA

PLACE_NEAR=U1800.AF37:2.54mm
R1950 2.37K 1% 1/20W MF 201
PCH_LVDS_IBG AF37 LVD_IBG
TP_PCH_LVDS_VBG 7 AF36 LVD_VBG
AE48 LVD_VREFH
AE47 LVD_VREFL

LVDS_IG_A_CLK_N 91 AK39 LVDSA_CLK*
LVDS_IG_A_CLK_P 91 AK40 LVDSA_CLK
LVDS_IG_A_DATA_N<0> 91 AN48 LVDSA_DATA0*
LVDS_IG_A_DATA_N<1> 91 AM47 LVDSA_DATA1*
LVDS_IG_A_DATA_N<2> 91 AK47 LVDSA_DATA2*
LVDS_IG_A_DATA_N<3> 91 AJ48 LVDSA_DATA3*
LVDS_IG_A_DATA_P<0> 91 AN47 LVDSA_DATA0
LVDS_IG_A_DATA_P<1> 91 AM49 LVDSA_DATA1
LVDS_IG_A_DATA_P<2> 91 AK49 LVDSA_DATA2
LVDS_IG_A_DATA_P<3> 91 AJ47 LVDSA_DATA3
LVDS_IG_B_CLK_N 7 AF40 LVDSB_CLK*
LVDS_IG_B_CLK_P 7 AF39 LVDSB_CLK
LVDS_IG_B_DATA_N<0> 91 AH45 LVDSB_DATA0*
LVDS_IG_B_DATA_N<1> 91 AH47 LVDSB_DATA1*
LVDS_IG_B_DATA_N<2> 91 AF49 LVDSB_DATA2*
LVDS_IG_B_DATA_N<3> 91 AF45 LVDSB_DATA3*
LVDS_IG_B_DATA_P<0> 91 AH43 LVDSB_DATA0
LVDS_IG_B_DATA_P<1> 91 AH49 LVDSB_DATA1
LVDS_IG_B_DATA_P<2> 91 AF47 LVDSB_DATA2
LVDS_IG_B_DATA_P<3> 91 AF43 LVDSB_DATA3

LVDS

TP_CRT_IG_BLUE 7 N48 CRT_BLUE
TP_CRT_IG_GREEN 7 P49 CRT_GREEN
TP_CRT_IG_RED 7 T49 CRT_RED
TP_CRT_IG_DDC_CLK 7 T39 CRT_DDC_CLK
TP_CRT_IG_DDC_DATA 7 M40 CRT_DDC_DATA
TP_CRT_IG_HSYNC 7 M47 CRT_HSYNC
TP_CRT_IG_VSYNC 7 M49 CRT_VSYNC
PCH_DAC_IREF T43 DAC_IREF
T42 CRT_IRTN

PLACE_NEAR=U1800.T43:2.54mm
R1951 1K 5% 1/20W MF 201

CRT

DIGITAL DISPLAY INTERFACE

SDVO_TVCLKINN (IPD) AP43 TP_SDVO_TVCLKINN 7
SDVO_TVCLKINP (IPD) AP45 TP_SDVO_TVCLKINP 7
SDVO_STALLN (IPD) AM42 TP_SDVO_STALLN 7
SDVO_STALLP (IPD) AM40 TP_SDVO_STALLP 7
SDVO_INTN (IPD) AP39 TP_SDVO_INTN 7
SDVO_INTP (IPD) AP40 TP_SDVO_INTP 7
SDVO_CTRLCLK P38 DPA_IG_DDC_CLK 83
SDVO_CTRLDATA (IPD-PLTRST#) M39 DPA_IG_DDC_DATA 83
DDPB_AUXN AT49 DPA_IG_AUX_CH_N 83 95
DDPB_AUXP AT47 DPA_IG_AUX_CH_P 83 95
DDPB_HPD AT40 DPA_IG_HPD 9 82
DDPB_0N AV42 TP_DP_IG_B_MLN<0> 9
DDPB_0P AV40 TP_DP_IG_B_MLP<0> 9
DDPB_1N AV45 TP_DP_IG_B_MLN<1> 9
DDPB_1P AV46 TP_DP_IG_B_MLP<1> 9
DDPB_2N AU48 TP_DP_IG_B_MLN<2> 9
DDPB_2P AU47 TP_DP_IG_B_MLP<2> 9
DDPB_3N AV47 TP_DP_IG_B_MLN<3> 9
DDPB_3P AV49 TP_DP_IG_B_MLP<3> 9
DDPC_CTRLCLK P46 DPB_IG_DDC_CLK 83
DDPC_CTRLDATA (IPD-PLTRST#) P42 DPB_IG_DDC_DATA 83
DDPC_AUXN AP47 DPB_IG_AUX_CH_N 83 95
DDPC_AUXP AP49 DPB_IG_AUX_CH_P 83 95
DDPC_HPD AT38 DPB_IG_HPD 9 82
DDPC_0N AY47 TP_DP_IG_C_MLN<0> 7
DDPC_0P AY49 TP_DP_IG_C_MLP<0> 7
DDPC_1N AY43 TP_DP_IG_C_MLN<1> 7
DDPC_1P AY45 TP_DP_IG_C_MLP<1> 7
DDPC_2N BA47 TP_DP_IG_C_MLN<2> 7
DDPC_2P BA48 TP_DP_IG_C_MLP<2> 7
DDPC_3N BB47 TP_DP_IG_C_MLN<3> 7
DDPC_3P BB49 TP_DP_IG_C_MLP<3> 7
DDPD_CTRLCLK M43 TP_DP_IG_D_CTRL_CLK 7
DDPD_CTRLDATA (IPD-PLTRST#) M36 TP_DP_IG_D_CTRL_DATA 7
DDPD_AUXN AT45 TP_DP_IG_D_AUXN 7
DDPD_AUXP AT43 TP_DP_IG_D_AUXP 7
DDPD_HPD BH41 TP_DP_IG_D_HPD 7
DDPD_0N BB43 TP_DP_IG_D_MLN<0> 7
DDPD_0P BB45 TP_DP_IG_D_MLP<0> 7
DDPD_1N BF44 TP_DP_IG_D_MLN<1> 7
DDPD_1P BE44 TP_DP_IG_D_MLP<1> 7
DDPD_2N BF42 TP_DP_IG_D_MLN<2> 7
DDPD_2P BE42 TP_DP_IG_D_MLP<2> 7
DDPD_3N BJ42 TP_DP_IG_D_MLN<3> 7
DDPD_3P BG42 TP_DP_IG_D_MLP<3> 7

20 19 18 17 8 =PP3V3_SUS_PCH_GPIO
R1983 10K 5% 1/20W MF 201
18 PCH_SUSWARN_L
R1986 0 5% 1/20W MF 201
PCH_SUSACK_L 18

=PP3V3_SUS_PCH_GPIO 8 17 18 19 20
=PP3V3_S0_PCH_GPIO 8 17 19 20 25 37
=PP3V3_S5_PCH 8

R1985 1K 5% 1/20W MF 201 PM_PWRBTN_L 18 24 41
R1991 8.2K 5% 1/20W MF 201 PM_CLKRUN_L 7 18 41 43
R1982 10K 5% 1/20W MF 201 MEM_VDD_SEL_1V5_L 18 64
R1925 1K 5% 1/20W MF 201 MAKE_BASE=TRUE PCIE_WAKE_L 7 18 34

NOSTUFF
R1999 0 5% 1/20W MF 201
=TBT_WAKE_L IN 35 42

R1924 100K 5% 1/20W MF 201 PM_SLP_S3_L 7 18 27 38 41 70
R1921 100K 5% 1/20W MF 201 PM_SLP_S4_L 7 18 27 34 38 40 41 70
R1922 100K 5% 1/20W MF 201 PM_SLP_S5_L 18 41 70
R1923 100K 5% 1/20W MF 201 PM_SLP_SUS_L 18 70
R1981 100K 5% 1/20W MF 201 LVDS_IG_BKL_ON 9 18
R1984 100K 5% 1/20W MF 201 LVDS_IG_PANEL_PWR 9 18

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012
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OMIT_TABLE

U1800
PANTHERPOINT
MOBILE
FCBGA
(5 OF 10)

TP_PCH_TP23

USB

PCI

(IPD)

(IPU-PCIERST#)

Ext A (XHCI/EHCI)

Ext B (XHCI)

Ext C (XHCI/EHCI)

Ext D (XHCI) (Mobiles: Trackpad?)

Unused

RSVD: SD

RSVD: WiFi

USB Hub (All LS/FS Devices)

Camera

Ext B (EHCI)

Ext D (EHCI)

RSVD: BT (HS)

Unused

Unused

PLACE_NEAR=U1800.B33:2.54mm

R2070 22.6 1% 1/120W MF 201

NO STUFF

Redundant to pull-up on audio page

NO STUFF

Redundant to pull-up on audio page

SYNC_MASTER=D2_KEPLER	SYNC_DATE=01/13/2012
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BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H

Systems with no chip-down memory should pull all 4 RAMCFG GPIOs high.

Systems with chip-down memory should add pull-downs on another page and set straps per software.

(TBT_CIO_PLUG_EVENT_ISOL)

OMIT_TABLE

U1800 PANTHERPOINT MOBILE FCBGA (6 OF 10)

GPIO

XDP_FC1_PCH_GPIO0	T7	BMBUSY*/GPIO0
FW_PME_L	A42	TACH1/GPIO1
DPMUX_UC_IRQ	H36	TACH2/GPIO6
SMC_RUNTIME_SCI_L	E38	TACH3/GPIO7
TP_PCH_GPIO8	C10	GPIO8 (IPU-RSMRST#)
WOL_EN	C4	LAN_PHY_PWR_CTRL/GPIO12
XDP_FC0_PCH_GPIO15	G2	GPIO15 (IPU)
XDP_DD2_PCH_GPIO16_AUD_IPHS_SWITCH_EN_PCH	U2	SATA4GP/GPIO16
LPCPLUS_GPIO	D40	TACH0/GPIO17
ODD_PWR_EN_L	T5	SCLOCK/GPIO22
TBT_GO2SX_BIDIR	E8	GPIO24
SMC_WAKE_SCI_L	E16	GPIO27 (IPU-DeepS4/S5)
XDP_DC0_PCH_GPIO28_ISOLATE_CPU_MEM_L	P8	GPIO28 (IPU-RSMRST#)
TBT_SW_RESET_R_L	K1	STP_PCI*/GPIO34
XDP_DC1_PCH_GPIO35_MXM_GOOD	K4	GPIO35
XDP_DD0_PCH_GPIO36_DP_GPU_TBT_SEL	V8	SATA2GP/GPIO36 (IPD-PLTRST#)
XDP_DD1_PCH_GPIO37_JTAG_ISP_TCK	M5	SATA3GP/GPIO37 (IPD-PLTRST#)
JTAG_ISP_TDO	N2	SLOAD/GPIO38
JTAG_ISP_TDI	M3	SDATAOUT0/GPIO39
FW_PWR_EN_PCH	V13	SDATAOUT1/GPIO48
XDP_DD3_PCH_GPIO49_ENET_LOW_PWR_PCH	V3	SATA5GP/GPIO49/TEMP_ALERT*
SPIROM_USE_MLB	D6	GPIO57

CPU/MISC

MLB_RAMCFG3	C40	TACH4/GPIO68
MLB_RAMCFG2	B41	TACH5/GPIO69
MLB_RAMCFG1	C41	TACH6/GPIO70
MLB_RAMCFG0	A40	TACH7/GPIO71
PCH_A20GATE	P4	A20GATE
PCH_PECI	AU16	(IPD) PECI
PCH_RCIN_L	P5	RCIN*
PCH_PROCPWRGD	AY11	PROCPWRGD
PM_THRMTRIP_L_R	AY10	THRMTRIP*
PCH_INIT3V3_L	T14	INIT3_3V* (IPU)
PCH_DF_TVS	AY1	DF_TVS (IPD-PLTRST#)
	AH8	TS_VSS1
	AK11	TS_VSS2
	AH10	TS_VSS3
	AK10	TS_VSS4
NC	P37	NC_1

NCTF

	A4	VSS_NCTF_0
	A44	VSS_NCTF_1
	A45	VSS_NCTF_2
	A46	VSS_NCTF_3
	A5	VSS_NCTF_4
	A6	VSS_NCTF_5
	B3	VSS_NCTF_6
	B47	VSS_NCTF_7
	BD1	VSS_NCTF_8
	BD49	VSS_NCTF_9
	BE1	VSS_NCTF_10
	BE49	VSS_NCTF_11
	BF1	VSS_NCTF_12
	BF49	VSS_NCTF_13
	BG2	VSS_NCTF_14
	BG48	VSS_NCTF_15
	BH3	VSS_NCTF_16
	BH47	VSS_NCTF_17
	BJ4	VSS_NCTF_18
	BJ44	VSS_NCTF_19
	BJ45	VSS_NCTF_20
	BJ46	VSS_NCTF_21
	BJ5	VSS_NCTF_22
	BJ6	VSS_NCTF_23
	C2	VSS_NCTF_24
	C48	VSS_NCTF_25
	D1	VSS_NCTF_26
	D49	VSS_NCTF_27
	E1	VSS_NCTF_28
	E49	VSS_NCTF_29
	F1	VSS_NCTF_30
	F49	VSS_NCTF_31

=PP3V3_S0_PCH_GPIO

RAMCFG3:H R2172 10K 5% 1/20W MF 201

RAMCFG2:H R2173 10K 5% 1/20W MF 201

RAMCFG1:H R2174 10K 5% 1/20W MF 201

RAMCFG0:H R2175 10K 5% 1/20W MF 201

R2180 0 5% 1/20W MF 201 — TBT_SW_RESET_L

R2170 43 — NO STUFF — CPU_PECI

R2140 0 — CPU_PWRGD

R2156 390 — PM_THRMTRIP_L

R2130 1K — NO STUFF — This has internal pull up and should not pulled low. THIS SIGNAL IS INTENDED FOR FIRMWARE HUB AND WE ARE NOT USING IT.

=PP1V8_S0_PCH_VCC_DFTERM

R2179 2.2K 5% 1/20W MF 201

R2178 1K 5% 1/20W MF 201 — CPU_PROC_SEL_L

DF_TVS:DMI & FDI Term Voltage
Set to Vss when Low
Set to Vcc when High

=PP3V3_S5_PCH_GPIO
=PP3V3_SUS_PCH_GPIO
=PP3V3_S0_PCH_GPIO

Stuff R2160 or R2574, not both

Must stuff R2197 when R2180 NO STUFFed.

R2160	10K	NO STUFF	XDP_FC1_PCH_GPIO0
R2185	10K		FW_PME_L
R2196	10K		SMC_RUNTIME_SCI_L
R2190	100K		LPCPLUS_GPIO
R2197	10K	NO STUFF	TBT_SW_RESET_R_L
R2184	10K		FW_PWR_EN_PCH
R2150	10K		PCH_A20GATE
R2155	10K		PCH_RCIN_L
R2194	10K		WOL_EN
R2192	10K		TBT_GO2SX_BIDIR
R2193	100K		SPIROM_USE_MLB
R2191	10K		SMC_WAKE_SCI_L
R2111	20K		DPMUX_UC_IRQ
R2195	100K		AUD_IPHS_SWITCH_EN_PCH
R2112	10K		ODD_PWR_EN_L
R2198	10K		XDP_DD0_PCH_GPIO36_DP_GPU_TBT_SEL
R2116	10K		ENET_LOW_PWR_PCH

JTAG Isolation due to glitch in and out of sleep

NOTE: TCK from PCH is Push-Pull CMOS
NOTE: TMS/TDI from PCH is Open Drain
NOTE: TDO from CR is Push-Pull CMOS

CRITICAL — Q2160 SSM6N15AFE SOT563 — R2188 10K — R2163 10K — JTAG_ISP_TMS — JTAG_TBT_TMS

CRITICAL — Q2160 SSM6N15AFE SOT563 — R2199 10K — R2161 10K — JTAG_ISP_TDI — JTAG_TBT_TDI

CRITICAL — Q2162 SSM3K15FV SOD-VESM-HF — R2186 10K — R2162 10K — JTAG_ISP_TDO — JTAG_TBT_TDO

=PP3V3_S0_PCH_GPIO

C2113 0.1UF 10% 16V X5R-CERM 0201

CRITICAL — U2100 SOT833 NLVLVC2G08GT — VCC — GND

TBT_PWR_EN goes high for JTAG Programming

TBT_PWR_EN — JTAG_TBT_TCK
JTAG_ISP_TCK — TBT_CIO_PLUG_EVENT_ISOL
TBT_CIO_PLUG_EVENT

R2113 10K — R2166 10K

Connects to PCH through current limiting 1K resistor R2574

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OMIT_TABLE

U1800
PANTHERPOINT MOBILE
FCBGA
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VCCACLK pin left as NC per DG
=PP3V3_S5_PCH_VCCDSW
TP_PPVOUT_PCH_DCPSUSBYP
PP3V3_S0_PCH_VCC3_3_CLK_F
VCCAPLLDMI2 pin left as NC per DG
=PP1V05_S0_PCH_VCCIO_CLK
AL24 left as NC per DG
=PP1V05_S0_PCH_VCCASW

PCH output, for decoupling only
PLACE_NEAR=U1800.N16:2.54mm
PPVOUT_G3_PCH_DCPRTC
=PP1V8R1V5_S0_PCH_VCCVRM
PP1V05_S0_PCH_VCCADPLLA_F
PP1V05_S0_PCH_VCCADPLLB_F
=PP1V05_S0_PCH_VCCIO_CLK
=PP1V05_S0_PCH_VCCDIFFCLK
55mA Max, 5mA Idle
=PP1V05_S0_PCH_VCCSSC
PPVOUT_S0_PCH_DCPSST
NC-ed per DG
=PP1V05_S0_PCH_V_PROC_IO
=PPVRTC_G3_PCH

C2210 0.1UF 20% 10V CERM 402
C2222 0.1UF 20% 10V CERM 402
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
PLACE_NEAR=U1800.V16:2.54mm
C2231 1UF 10% 6.3V CERM 402
C2232 0.1UF 20% 10V CERM 402
C2233 0.1UF 20% 10V CERM 402
PLACE_NEAR=U1800.A22:2.54mm

AD49	VCCACLK		
T16	VCCDSW3_3		
V12	DCPSUSBYP		
T38	VCC3_3_5_CLK		
BH23	VCCAPLLDMI2		
AL29	VCCIO_14_PLLCLK		
AL24	DCPSUS_3_CLK		
AA19	VCCASW_1_CLK		
AA21	VCCASW_2_CLK		
AA24	VCCASW_3_CLK		
AA26	VCCASW_4_CLK		
AA27	VCCASW_5_CLK		
AA29	VCCASW_6_CLK		
AA31	VCCASW_7_CLK		
AC26	VCCASW_8_CLK		
AC27	VCCASW_9_CLK		
AC29	VCCASW_10_CLK		
AC31	VCCASW_11_CLK		
AD29	VCCASW_12_CLK		
AD31	VCCASW_13_CLK		
W21	VCCASW_14_CLK		
W23	VCCASW_15_CLK		
W24	VCCASW_16_CLK		
W26	VCCASW_17_CLK		
W29	VCCASW_18_CLK		
W31	VCCASW_19_CLK		
W33	VCCASW_20_CLK		
N16	DCPRTC		
Y49	VCCVRM_4_CLK		
BD47	VCCADPLLA		
BF47	VCCADPLLB		
AF17	VCCIO_7_CLK		
AF33	VCCDIFFCLKN		
AF34	VCCDIFFCLKN		
AG34	VCCDIFFCLKN		
AG33	VCCSSC		
V16	DCPSST		
T17	DCPSUS_1_CLK		
V19	DCPSUS_2_CLK		
BJ8	V_PROC_IO		
A22	VCCRTC		
N26	VCCIO_29_USB	USB	=PP1V05_S0_PCH_VCCIO_USB
P26	VCCIO_30_USB		
P28	VCCIO_31_USB		
T27	VCCIO_32_USB		
T29	VCCIO_33_USB		
T23	VCCSUS3_3_7_USB		=PP3V3_SUS_PCH_VCCSUS_USB
T24	VCCSUS3_3_8_USB		
V23	VCCSUS3_3_9_USB		
V24	VCCSUS3_3_10_USB		
P24	VCCSUS3_3_6_USB		
T26	VCCIO_34_PLLUSB		=PP1V05_S0_PCH_VCCIO_PLLUSB
M26	V5REF_SUS		=PP5V_SUS_PCH_V5REFSUS
AN23	DCPSUS_4_USB		NC-ed per DG
AN24	VCCSUS3_3_1_USB		=PP3V3_SUS_PCH_VCCSUS
P34	V5REF	CLK/MISC	=PP5V_S0_PCH_V5REF
N20	VCCSUS3_2_GPIO		=PP3V3_SUS_PCH_VCCSUS_GPIO
N22	VCCSUS3_3_3_GPIO		
P20	VCCSUS3_3_4_GPIO		
P22	VCCSUS3_3_5_GPIO		
AA16	VCC3_3_1_GPIO	PCI/GPIO/LPC	=PP3V3_S0_PCH_VCC3_3_GPIO
W16	VCC3_3_8_GPIO		
T34	VCC3_3_4_GPIO		
AJ2	VCC3_3_2_SATA		=PP3V3_S0_PCH_VCC3_3_SATA
AF13	VCCIO_5_PLLSATA		=PP1V05_S0_PCH_VCCIO_SATA
AH13	VCCIO_12_SATA3		
AH14	VCCIO_13_SATA3		
AF14	VCCIO_6_PLLSATA3		
AK1	VCCAPLLSATA	SATA	NC VCCAPLLSATA pin left as NC per DG
AF11	VCCVRM_1_SATA		=PP1V8R1V5_S0_PCH_VCCVRM
AC16	VCCIO_2_SATA		=PP1V05_S0_PCH_VCCIO_SATA
AC17	VCCIO_3_SATA		
AD17	VCCIO_4_SATA		
T21	VCCASW_22_MISC	MISC	=PP1V05_S0_PCH_VCCASW
V21	VCCASW_23_MISC		
T19	VCCASW_21_MISC		
P32	VCCSUSHDA	HDA	=PP3V3R1V5_S0_PCH_VCCSUSHDA
			10 mA Max, 1mA Idle

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PANTHERPOINT MOBILE
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=PP1V05_S0_PCH_VCC_CORE
1.44 A Max, 474mA Idle

AA23	VCCCORE	VCC CORE	
AC23	VCCCORE		
AD21	VCCCORE		
AD23	VCCCORE		
AF21	VCCCORE		
AF23	VCCCORE		
AG21	VCCCORE		
AG23	VCCCORE		
AG24	VCCCORE		
AG26	VCCCORE		
AG27	VCCCORE		
AG29	VCCCORE		
AJ23	VCCCORE		
AJ26	VCCCORE		
AJ27	VCCCORE		
AJ29	VCCCORE		
AJ31	VCCCORE		
AN19	VCCIO_28_PLLPCIE		=PP1V05_S0_PCH_VCCIO_PLLPCIE
BJ22	VCCAPLLEXP		TP_1V05_S0_PCH_VCCAPLLEXP
AN16	VCCIO_15_FDI		=PP1V05_S0_PCH_VCCIO
AN17	VCCIO_16_FDI		
AN21	VCCIO_17_PCIE	VCCIO	
AN26	VCCIO_18_PCIE		
AN27	VCCIO_19_PCIE		
AP21	VCCIO_20_PCIE		
AP23	VCCIO_21_PCIE		
AP24	VCCIO_22_PCIE		
AP26	VCCIO_23_PCIE		
AT24	VCCIO_24_PCIE		
AN33	VCCIO_25_DP		
AN34	VCCIO_26_DP		
BH29	VCC3_3_3_PCIE		=PP3V3_S0_PCH_VCC3_3_PCI
AP16	VCCVRM_2_FDI		=PP1V8R1V5_S0_PCH_VCCVRM
BG6	VCCAFDIPLL	FDI/DFT/SPI	VCCAFDIPLL pin left as NC per DG
AP17	VCCIO_27_PLLFDI		=PP1V05_S0_PCH_VCCIO_PLLFDI
AU20	VCCDMI_2_FDI		=PP1V05_S0_PCH_VCCDMI_FDI
AG16	VCCDFTERM		=PP1V8_S0_PCH_VCC_DFTERM
AG17	VCCDFTERM		
AJ16	VCCDFTERM		
AJ17	VCCDFTERM		
V1	VCCSPI		=PP3V3_SUS_PCH_VCC_SPI
AK36	VCCALVDS	LVDS	=LVDS_VCCA
AK37	VSSALVDS		
AM37	VCCTX_LVDS		=PP1V8_S0_PCH_VCCTX_LVDS_F
AM38	VCCTX_LVDS		
AP36	VCCTX_LVDS		
AP37	VCCTX_LVDS		
V33	VCC3_3_6_HVCMOS	HVCMOS	=PP3V3_S0_PCH_VCC3_3_HVCMOS
V34	VCC3_3_7_HVCMOS		
AT16	VCCVRM_3_DMI	DMI	=PP1V8R1V5_S0_PCH_VCCVRM
AT20	VCCDMI_1_DMI		=PP1V05_S0_PCH_VCC_DMI
AB36	VCCCLKDMI		=PP1V05_S0_PCH_VCCCLKDMI_F
U48	VCCADAC	CRT	=PP3V3_S0_PCH_VCCA_DAC_F
U47	VSSADAC		

CKPLUS_WAIVE=PwrTerm2Gnd

SYNC_MASTER=D2_CLEAN	SYNC_DATE=03/19/2012
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VSS

H5	VSS	VSS	AK38
AA17	VSS	VSS	AK4
AA2	VSS	VSS	AK42
AA3	VSS	VSS	AK46
AA33	VSS	VSS	AK8
AA34	VSS	VSS	AL16
AB11	VSS	VSS	AL17
AB14	VSS	VSS	AL19
AB39	VSS	VSS	AL2
AB4	VSS	VSS	AL21
AB43	VSS	VSS	AL23
AB5	VSS	VSS	AL26
AB7	VSS	VSS	AL27
AC19	VSS	VSS	AL31
AC2	VSS	VSS	AL33
AC21	VSS	VSS	AL34
AC24	VSS	VSS	AL48
AC33	VSS	VSS	AM11
AC34	VSS	VSS	AM14
AC48	VSS	VSS	AM36
AD10	VSS	VSS	AM39
AD11	VSS	VSS	AM43
AD12	VSS	VSS	AM45
AD13	VSS	VSS	AM46
AD19	VSS	VSS	AM7
AD24	VSS	VSS	AN2
AD26	VSS	VSS	AN29
AD27	VSS	VSS	AN3
AD33	VSS	VSS	AN31
AD34	VSS	VSS	AP12
AD36	VSS	VSS	AP19
AD37	VSS	VSS	AP28
AD38	VSS	VSS	AP30
AD39	VSS	VSS	AP32
AD4	VSS	VSS	AP38
AD40	VSS	VSS	AP4
AD42	VSS	VSS	AP42
AD43	VSS	VSS	AP46
AD45	VSS	VSS	AP8
AD46	VSS	VSS	AR2
AD8	VSS	VSS	AR48
AE2	VSS	VSS	AT11
AE3	VSS	VSS	AT13
AF10	VSS	VSS	AT18
AF12	VSS	VSS	AT22
AD14	VSS	VSS	AT26
AD16	VSS	VSS	AT28
AF16	VSS	VSS	AT30
AF19	VSS	VSS	AT32
AF24	VSS	VSS	AT34
AF26	VSS	VSS	AT39
AF27	VSS	VSS	AT42
AF29	VSS	VSS	AT46
AF31	VSS	VSS	AT7
AF38	VSS	VSS	AU24
AF4	VSS	VSS	AU30
AF42	VSS	VSS	AV11
AF46	VSS	VSS	AV16
AF5	VSS	VSS	AV20
AF7	VSS	VSS	AV24
AF8	VSS	VSS	AV30
AG19	VSS	VSS	AV38
AG2	VSS	VSS	AV4
AG31	VSS	VSS	AV43
AG48	VSS	VSS	AV8
AH11	VSS	VSS	AW14
AH3	VSS	VSS	AW18
AH36	VSS	VSS	AW2
AH39	VSS	VSS	AW22
AH40	VSS	VSS	AW26
AH42	VSS	VSS	AW28
AH46	VSS	VSS	AW32
AH7	VSS	VSS	AW34
AJ19	VSS	VSS	AW36
AJ21	VSS	VSS	AW40
AJ24	VSS	VSS	AW48
AJ33	VSS	VSS	AY12
AJ34	VSS	VSS	AY22
AK12	VSS	VSS	AY28
AK3	VSS		

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U1800
PANTHERPOINT
MOBILE
FCBGA
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VSS

AY4	VSS	VSS	H46
AY42	VSS	VSS	K18
AY46	VSS	VSS	K26
AY8	VSS	VSS	K39
B11	VSS	VSS	K46
B15	VSS	VSS	K7
B19	VSS	VSS	L18
B23	VSS	VSS	L2
B27	VSS	VSS	L20
B31	VSS	VSS	L26
B35	VSS	VSS	L28
B39	VSS	VSS	L36
B7	VSS	VSS	L48
F45	VSS	VSS	M12
BB12	VSS	VSS	P16
BB16	VSS	VSS	M18
BB20	VSS	VSS	M22
BB22	VSS	VSS	M24
BB24	VSS	VSS	M30
BB28	VSS	VSS	M32
BB30	VSS	VSS	M34
BB38	VSS	VSS	M38
BB4	VSS	VSS	M4
BB46	VSS	VSS	M42
BC14	VSS	VSS	M46
BC18	VSS	VSS	M8
BC2	VSS	VSS	N18
BC22	VSS	VSS	P30
BC26	VSS	VSS	N47
BC32	VSS	VSS	P11
BC34	VSS	VSS	P18
BC36	VSS	VSS	T33
BC40	VSS	VSS	P40
BC42	VSS	VSS	P43
BC48	VSS	VSS	P47
BD46	VSS	VSS	P7
BD5	VSS	VSS	R2
BE22	VSS	VSS	R48
BE26	VSS	VSS	T12
BE40	VSS	VSS	T31
BF10	VSS	VSS	T37
BF12	VSS	VSS	T4
BF16	VSS	VSS	W34
BF20	VSS	VSS	T46
BF22	VSS	VSS	T47
BF24	VSS	VSS	T8
BF26	VSS	VSS	V11
BF28	VSS	VSS	V17
BD3	VSS	VSS	V26
BF30	VSS	VSS	V27
BF38	VSS	VSS	V29
BF40	VSS	VSS	V31
BF8	VSS	VSS	V36
BG17	VSS	VSS	V39
BG21	VSS	VSS	V43
BG33	VSS	VSS	V7
BG44	VSS	VSS	W17
BG8	VSS	VSS	W19
BH11	VSS	VSS	W2
BH15	VSS	VSS	W27
BH17	VSS	VSS	W48
BH19	VSS	VSS	Y12
H10	VSS	VSS	Y38
BH27	VSS	VSS	Y4
BH31	VSS	VSS	Y42
BH33	VSS	VSS	Y46
BH35	VSS	VSS	Y8
BH39	VSS		
BH43	VSS	VSS	BG29
BH7	VSS	VSS	N24
D3	VSS	VSS	AJ3
D12	VSS	VSS	AD47
D16	VSS		
D18	VSS	VSS	B43
D22	VSS	VSS	BE10
D24	VSS	VSS	BG41
D26	VSS		
D30	VSS	VSS	G14
D32	VSS	VSS	H16
D34	VSS		
D38	VSS	VSS	T36
D42	VSS		
D8	VSS	VSS	BG22
E18	VSS	VSS	BG24
E26	VSS	VSS	C22
G18	VSS	VSS	AP13
G20	VSS	VSS	M14
G26	VSS	VSS	AP3
G28	VSS	VSS	AP1
G36	VSS	VSS	BE16
G48	VSS	VSS	BC16
H12	VSS	VSS	BG28
H18	VSS	VSS	BJ28
H22	VSS		
H24	VSS		
H26	VSS		
H30	VSS		
H32	VSS		
H34	VSS		
F3	VSS		

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

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PCH GROUNDS

Apple Inc.

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CPU Micro2-XDP

=PPVCCIO_S0_XDP (24 8)

=PP3V3_S0_XDP (8)

NO STUFF
R2540 1K 5% 1/16W MF-LF 402

CRITICAL
XDP_CONN
J2500
DF40RC-60DP-0.4V
M-ST-SM

998-2516

NOTE: This is not the standard XDP pinout. Use with 921-0133 Adapter Flex to support chipset debug.

XDP_CPU:BPM				
XDP_BPM_L<4>	R2560	0		
XDP_BPM_L<5>	R2561	0		
XDP_BPM_L<6>	R2562	0		
XDP_BPM_L<7>	R2563	0		

XDP_CPU:CFG				
CPU_CFG<12>	R2564	0		
CPU_CFG<13>	R2565	0		
CPU_CFG<14>	R2566	0		
CPU_CFG<15>	R2567	0		

CPU_PWRGD	R2500	1K	XDP	PLACE_NEAR=U1000.C60:2.54mm
PM_PWRBTN_L	R2502	0	XDP	PLACE_NEAR=U4900.P17:2.54mm
CPU_CFG<0>	R2501	1K	XDP	PLACE_NEAR=U1000.B57:2.54mm
PM_PCH_SYS_PWROK	R2504	330	XDP	

XDP SIGNALS			PCH SIGNALS
XDP_DA0_USB_EXTA_OC_L	R2520	33	XDP_DA0_PCH_GPIO59_USB_EXTA_OC_L
XDP_DA1_USB_EXTB_OC_L	R2521	33	XDP_DA1_PCH_GPIO40_USB_EXTB_OC_L
XDP_DA2_USB_EXTC_OC_L	R2522	33	XDP_DA2_PCH_GPIO41_USB_EXTC_OC_L
XDP_DA3_USB_EXTD_OC_L	R2523	33	XDP_DA3_PCH_GPIO42_USB_EXTD_OC_L
XDP_DB0_USB_EXTB_OC_EHCI_L	R2524	33	XDP_DB0_PCH_GPIO43_USB_EXTB_OC_EHCI_L
XDP_DB1_USB_EXTD_OC_EHCI_L	R2525	33	XDP_DB1_PCH_GPIO9_USB_EXTD_OC_EHCI_L
XDP_DB2_AP_PWR_EN	R2526	33	XDP_DB2_PCH_GPIO10_AP_PWR_EN
XDP_DB3_SDCONN_STATE_CHANGE	R2527	33	XDP_DB3_PCH_GPIO14_SDCONN_STATE_CHANGE
XDP_FC0	R2528	33	XDP_FC0_PCH_GPIO15
XDP_FC1	R2529	33	XDP_FC1_PCH_GPIO0
XDP_DC0_ISOLATE_CPU_MEM_L	R2530	33	XDP_DC0_PCH_GPIO28_ISOLATE_CPU_MEM_L
XDP_DC1_MXM_GOOD	R2531	33	XDP_DC1_PCH_GPIO35_MXM_GOOD
XDP_DC2_DP_AUXCH_ISOL	R2532	33	XDP_DC2_PCH_GPIO21_DP_AUXCH_ISOL
XDP_DC3_SATARDRVR_EN	R2533	33	XDP_DC3_PCH_GPIO19_SATARDRVR_EN
XDP_DD0_DP_GPU_TBT_SEL	R2534	33	XDP_DD0_PCH_GPIO36_DP_GPU_TBT_SEL
XDP_DD1_JTAG_ISP_TCK	R2535	33	XDP_DD1_PCH_GPIO37_JTAG_ISP_TCK
XDP_DD2_AUD_IPHS_SWITCH_EN	R2536	33	XDP_DD2_PCH_GPIO16_AUD_IPHS_SWITCH_EN_PCH
XDP_DD3_ENET_LOW_PWR	R2537	33	XDP_DD3_PCH_GPIO49_ENET_LOW_PWR_PCH

(R2520-R2537) XDP

ALL_SYS_PWRGD	R2584	1K	XDP	PLACE_NEAR=J2550.39:2.54mm
PM_PWRBTN_L	R2585	0	XDP	PLACE_NEAR=U4900.P17:2.54mm

XDP_CPU_TDO	R2510	51	XDP PLACE_NEAR=J2500.52:2.54mm
XDP_CPU_TDI	R2511	51	XDP PLACE_NEAR=U1000.K61:2.54mm
XDP_CPU_TMS	R2512	51	XDP PLACE_NEAR=U1000.H59:2.54mm
XDP_CPU_TCK	R2513	51	XDP PLACE_NEAR=U1000.J58:2.54mm
XDP_CPU_TRST_L	R2514	51	XDP PLACE_NEAR=U1000.H63:2.54mm

R2515	0	XDP PLACE_NEAR=R1841.1:2.54mm	ITPXDP_CLK100M_P
R2516	0	XDP PLACE_NEAR=R1840.1:2.54mm	ITPXDP_CLK100M_N
R2505	1K	XDP PLACE_NEAR=U1000.G3:2.54mm	CPU_RESET_L

OBSFN_A0	CPU_CFG<16>
OBSFN_A1	CPU_CFG<17>
OBSDATA_A0	CPU_CFG<0>
OBSDATA_A1	CPU_CFG<1>
OBSDATA_A2	CPU_CFG<2>
OBSDATA_A3	CPU_CFG<3>
OBSFN_B0	CPU_CFG<8>
OBSFN_B1	CPU_CFG<9>
OBSDATA_B0	CPU_CFG<4>
OBSDATA_B1	CPU_CFG<5>
OBSDATA_B2	CPU_CFG<6>
OBSDATA_B3	CPU_CFG<7>
PWRGD/HOOK0	XDP_CPU_PWRGD
HOOK1	XDP_CPU_PWRBTN_L
VCC_OBS_AB	
HOOK2	XDP_CPU_CFG<0>
HOOK3	XDP_VR_READY
SDA	=SMBUS_XDP_SDA
SCL	=SMBUS_XDP_SCL
TCK1	
TCK0	XDP_CPU_TCK
NC	

ITPCLK/HOOK4	XDP_CPU_CLK100M_P
ITPCLK#/HOOK5	XDP_CPU_CLK100M_N
VCC_OBS_CD	
RESET#/HOOK6	XDP_CPURST_L
DBR#/HOOK7	XDP_DBRESET_L
XDP_PRESENT#	
TDO	XDP_CPU_TDO
TRSTn	XDP_CPU_TRST_L
TDI	XDP_CPU_TDI
TMS	XDP_CPU_TMS

NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page

XDP C2500 0.1UF 10% 16V X7R-CERM 0402
XDP C2501 0.1UF 10% 16V X7R-CERM 0402

PCH SIGNALS			Non-XDP Signals
XDP_DA0_PCH_GPIO59_USB_EXTA_OC_L	R2590	0	USB_EXTA_OC_L
XDP_DA1_PCH_GPIO40_USB_EXTB_OC_L	R2591	0	USB_EXTB_OC_L
XDP_DB2_PCH_GPIO10_AP_PWR_EN	R2596	0	AP_PWR_EN
XDP_DB3_PCH_GPIO14_SDCONN_STATE_CHANGE	R2597	0	SDCONN_STATE_CHANGE
XDP_DC3_PCH_GPIO19_SATARDRVR_EN	R2573	0	SATARDRVR_EN
XDP_DC0_PCH_GPIO28_ISOLATE_CPU_MEM_L	R2570	0	ISOLATE_CPU_MEM_L
XDP_DC2_PCH_GPIO21_DP_AUXCH_ISOL	R2572	0	DP_AUXCH_ISOL
XDP_FC1_PCH_GPIO0	R2574	1K	TBT_CIO_PLUG_EVENT_ISOL
XDP_DD1_PCH_GPIO37_JTAG_ISP_TCK	R2575	0	JTAG_ISP_TCK
XDP_DD2_PCH_GPIO16_AUD_IPHS_SWITCH_EN_PCH	R2576	0	AUD_IPHS_SWITCH_EN_PCH
XDP_DD3_PCH_GPIO49_ENET_LOW_PWR_PCH	R2577	0	ENET_LOW_PWR_PCH

PCH Micro2-XDP

=PP3V3_S5_XDP (8)

CRITICAL
XDP_CONN
J2550
DF40RC-60DP-0.4V
M-ST-SM

998-2516

OBSFN_A0	OBSFN_C0
OBSFN_A1	OBSFN_C1
OBSDATA_A0	OBSDATA_C0
OBSDATA_A1	OBSDATA_C1
OBSDATA_A2	OBSDATA_C2
OBSDATA_A3	OBSDATA_C3
OBSFN_B0	OBSFN_D0
OBSFN_B1	OBSFN_D1
OBSDATA_B0	OBSDATA_D0
OBSDATA_B1	OBSDATA_D1
OBSDATA_B2	OBSDATA_D2
OBSDATA_B3	OBSDATA_D3
PWRGD/HOOK0	ITPCLK/HOOK4
HOOK1	ITPCLK#/HOOK5
VCC_OBS_AB	VCC_OBS_CD
HOOK2	RESET#/HOOK6
HOOK3	DBR#/HOOK7
SDA	TDO
SCL	TRSTn
TCK1	TDI
TCK0	TMS
NC	XDP_PRESENT#

TP_XDP_PCH_OBSFN_A<0>	XDP_FC0
TP_XDP_PCH_OBSFN_A<1>	XDP_FC1
XDP_DA0_USB_EXTA_OC_L	XDP_DC0_ISOLATE_CPU_MEM_L
XDP_DA1_USB_EXTB_OC_L	XDP_DC1_MXM_GOOD
XDP_DA2_USB_EXTC_OC_L	XDP_DC2_DP_AUXCH_ISOL
XDP_DA3_USB_EXTD_OC_L	XDP_DC3_SATARDRVR_EN
TP_XDP_PCH_OBSFN_B<0>	TP_XDP_PCH_OBSFN_D<0>
TP_XDP_PCH_OBSFN_B<1>	TP_XDP_PCH_OBSFN_D<1>
XDP_DB0_USB_EXTB_OC_EHCI_L	XDP_DD0_DP_GPU_TBT_SEL
XDP_DB1_USB_EXTD_OC_EHCI_L	XDP_DD1_JTAG_ISP_TCK
XDP_DB2_AP_PWR_EN	XDP_DD2_AUD_IPHS_SWITCH_EN
XDP_DB3_SDCONN_STATE_CHANGE	XDP_DD3_ENET_LOW_PWR
XDP_PCH_S5_PWRGD	TP_XDP_PCH_HOOK4
XDP_PCH_PWRBTN_L	TP_XDP_PCH_HOOK5
TP_XDPPCH_HOOK2	XDPPCH_PLTRST_L
TP_XDPPCH_HOOK3	XDP_DBRESET_L
=SMBUS_XDP_SDA	TP_XDP_PCH_TDO
=SMBUS_XDP_SCL	TP_XDP_PCH_TRST_L
	XDP_PCH_TDI
XDP_PCH_TCK	XDP_PCH_TMS

NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page

XDP C2580 0.1UF 10% 16V X7R-CERM 0402
XDP C2581 0.1UF 10% 16V X7R-CERM 0402

XDP_PCH_TDO	R2550	51	XDP PLACE_NEAR=J2550.52:2.54mm
XDP_PCH_TDI	R2551	51	XDP PLACE_NEAR=U1800.K5:2.54mm
XDP_PCH_TMS	R2552	51	XDP PLACE_NEAR=U1800.H7:2.54mm
XDP_PCH_TCK	R2556	51	XDP PLACE_NEAR=U1800.J3:2.54mm

1K series R on PCH Support Page

PCH/XDP Signal Isolation Notes:

- Following Intel's Debug Prot Design Guid for HR and CR v1.3 doc id 404081.
Initially, stuffing both 33 and 0 ohms and validate whether it is functional in that state, else add BOM options.
- For isolated GPIOs:
  - 'Output' non-XDP signals require pulls.
  - 'Output' PCH/XDP signals require pulls.

R252x, R253x, R257x and R259x should be placed where signal path needs to split between route from PCH to J2550 and path to non-XDP signal destination.

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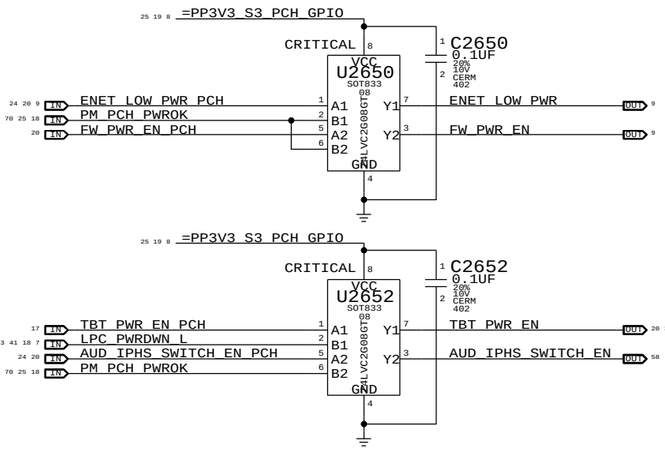
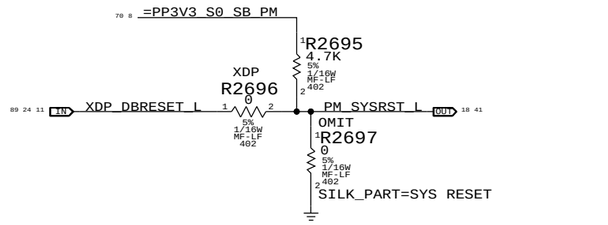
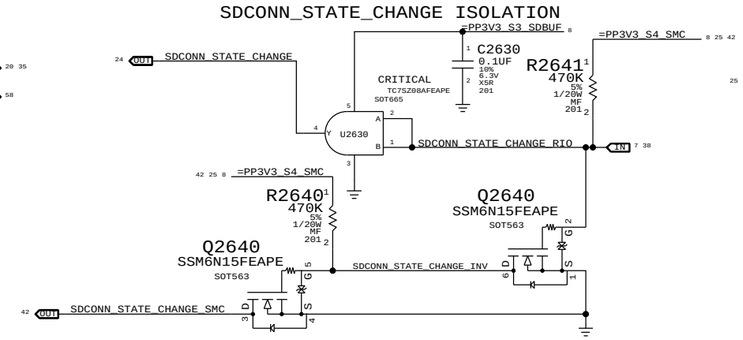
GPIO Glitch Prevention



PCH Reset Button

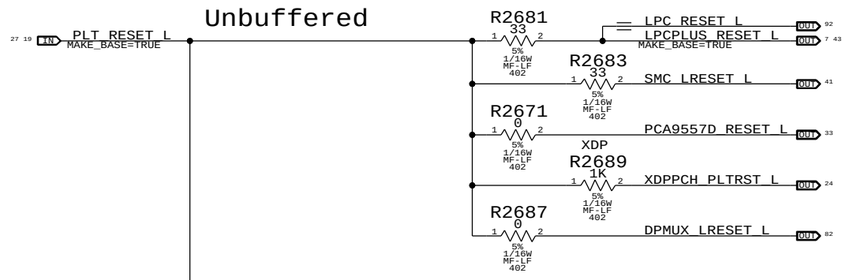


SDCONN_STATE_CHANGE ISOLATION

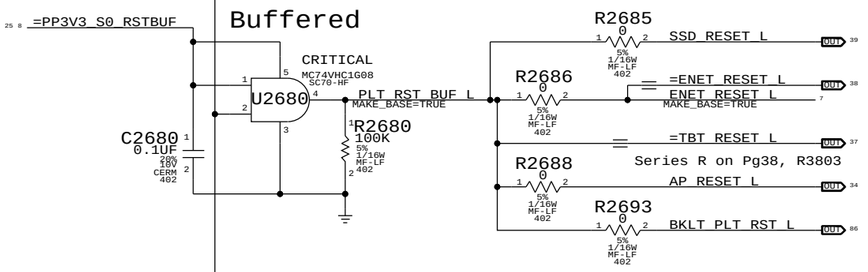


Platform Reset Connections

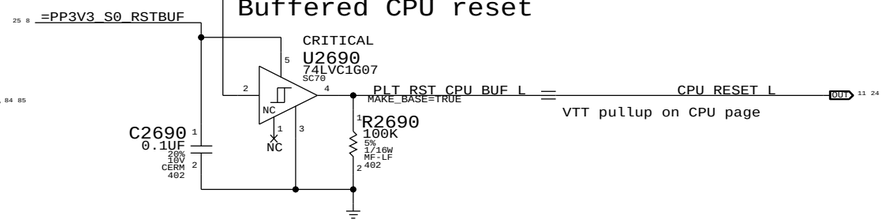
Unbuffered



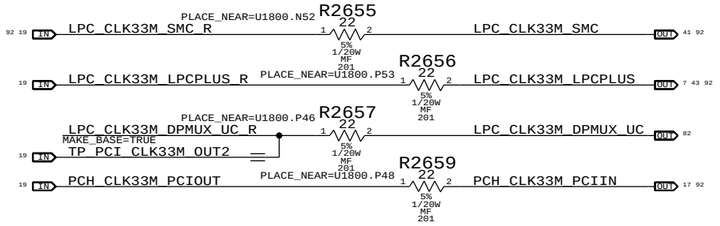
Buffered

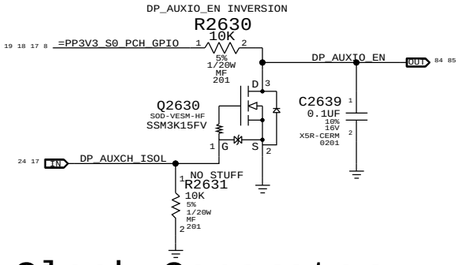


Buffered CPU reset



LPC 33MHz Clock Series Termination

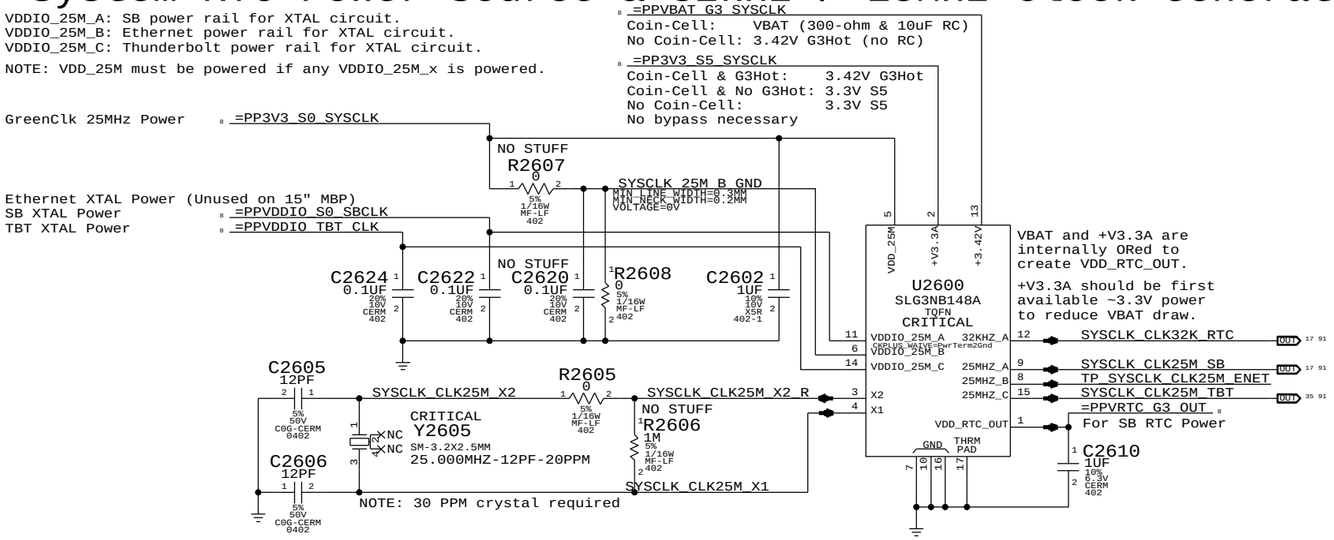




System RTC Power Source & 32kHz / 25MHz Clock Generator

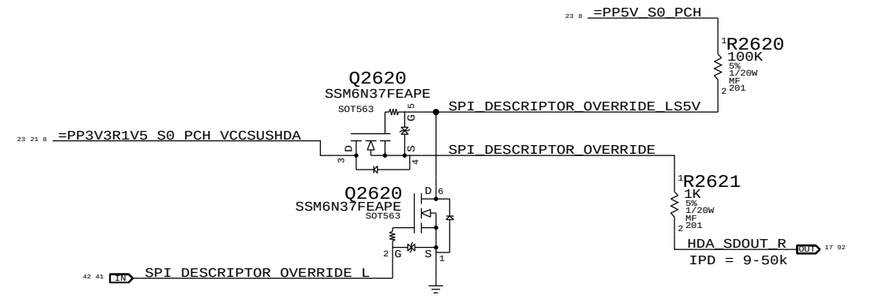
VDDIO_25M_A: SB power rail for XTAL circuit.
VDDIO_25M_B: Ethernet power rail for XTAL circuit.
VDDIO_25M_C: Thunderbolt power rail for XTAL circuit.

NOTE: VDD_25M must be powered if any VDDIO_25M_x is powered.



PCH ME Disable Strap

PCH uses HDA_SDO as a power-up strap. If low, ME functions normally.
If high, ME is disabled. This allows for full re-flashing of SPI ROM.
SMC controls strap enable to allow in-field control of strap setting.
Q2620 & 5V pull-up allows circuit to work regardless of HDA voltage.



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USB MUX FOR LS/FS INTERNAL DEVICES

BOM GROUP	BOM OPTIONS
HUB_ALLREM	HUB_NONREM1_0,HUB_NONREM0_0
HUB_1NONREM	HUB_NONREM1_0,HUB_NONREM0_1
HUB_2NONREM	HUB_NONREM1_1,HUB_NONREM0_0
HUB_3NONREM	HUB_NONREM1_1,HUB_NONREM0_1

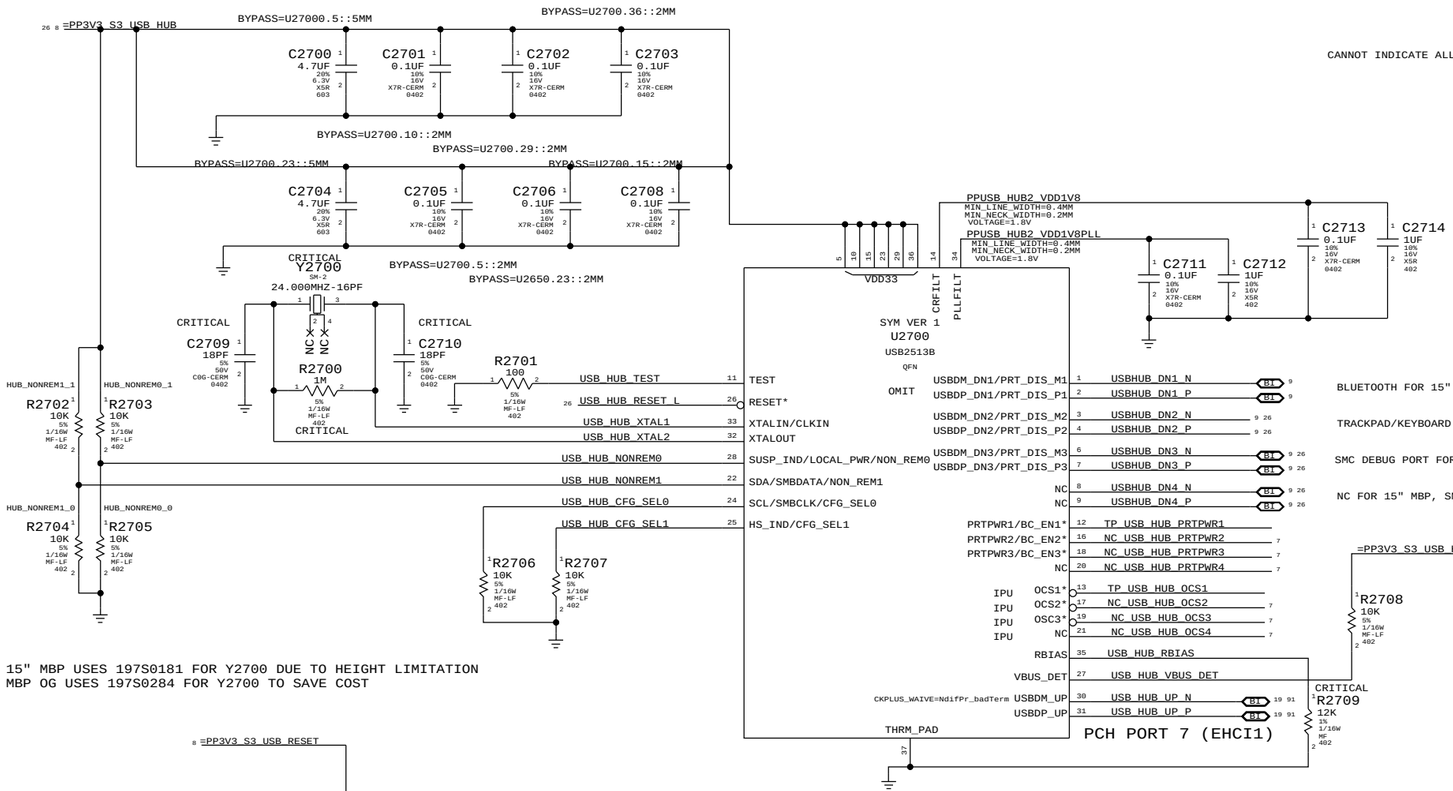
NON_REM 1 :	NON_REM 0	STRAP PIN CFG
0	0	ALL PORTS ARE REMOVABLE
0	1	PORT 1 IS NON REMOVABLE
1	0	PORT 1&2 ARE NON REMOVABLE
1	1	PORT 1&2&3 ARE NON REMOVABLE

CANNOT INDICATE ALL 4 PORTS ARE NON REMOVABLE ON USB2514B VIA STARPPING, PROGRAM NON_REMOVABLE DEVICE REGISTER 09H

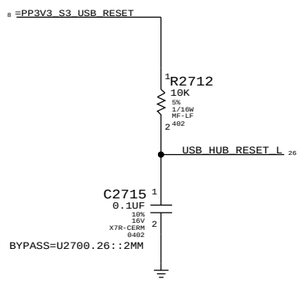
BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0824	1	USB HUB 2514B	U2700	CRITICAL	USBHUB2514B
338S0923	1	USB HUB 2513B	U2700	CRITICAL	USBHUB2513B
338S0983	1	USB HUB 2512B	U2700	CRITICAL	USBHUB2512B

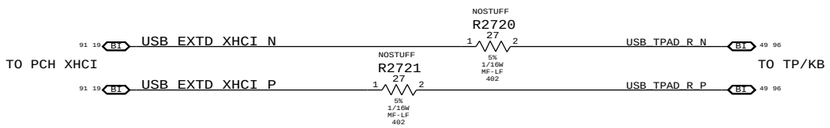
15" MBP ENGINEERING: USE USB2513B PRODUCTION: USE USB2512B
MBP OG ENGINEERING: USE USB2514B PRODUCTION: USE USB2513B



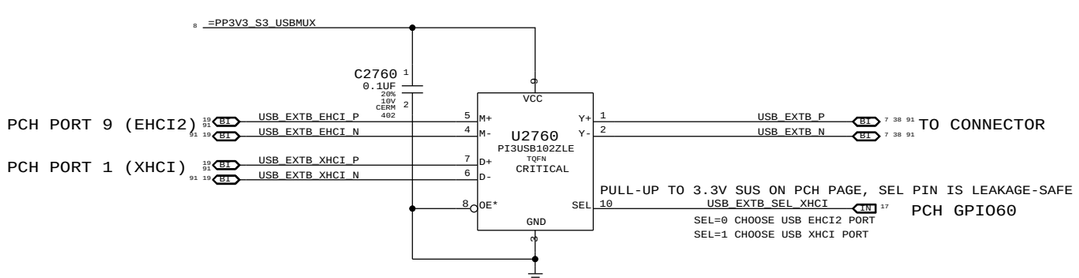
15" MBP USES 197S0181 FOR Y2700 DUE TO HEIGHT LIMITATION
MBP OG USES 197S0284 FOR Y2700 TO SAVE COST



TO CONNECT TP/KB TO PCH XHCI
NOSTUFF R5701 & R5702, STUFF R2720 & R2721



USB XHCI/EHCI2 PORT MUX FOR EXT B



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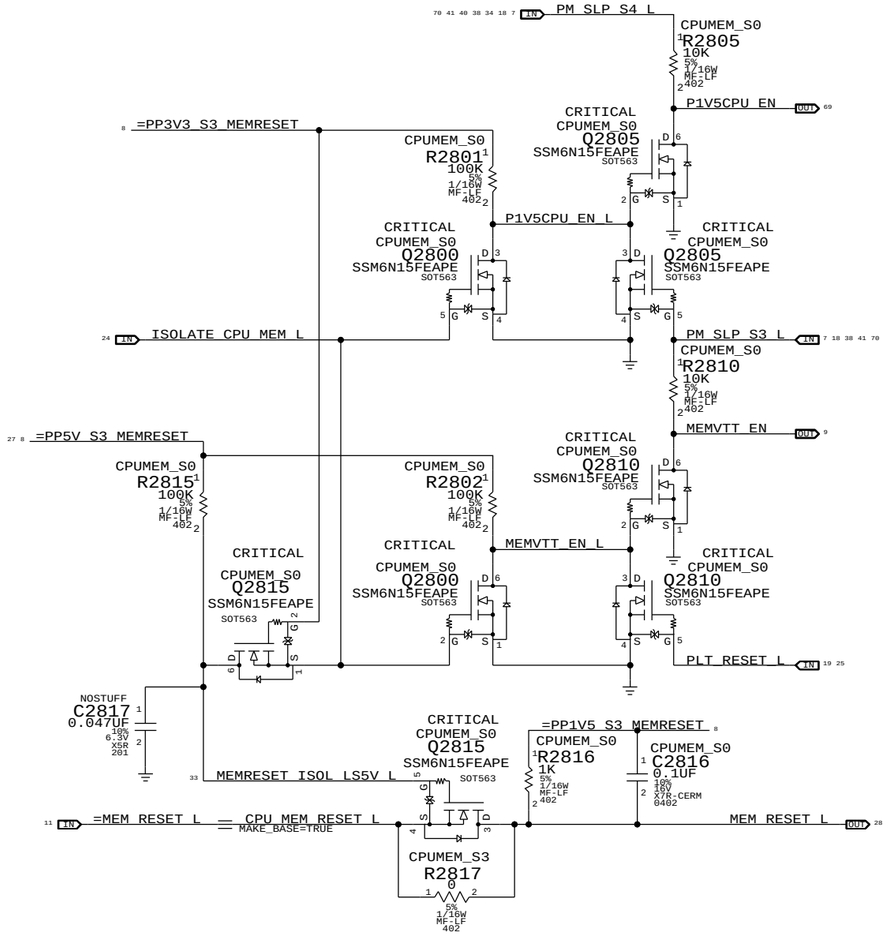
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

P1V5CPU_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L
MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0365	1	RES,MTL FILM,1/16W,33.2K,1,0402,SMD,LF	R2821		PPDDR:1V5
114S0376	1	RES,MTL FILM,1/16W,43.2K,1,0402,SMD,LF	R2821		PPDDR:1V35

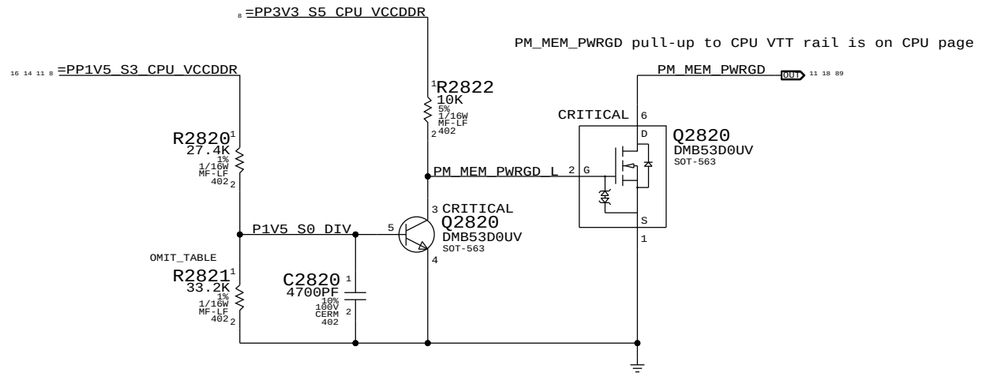


	Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	1	CPU_MEM_RESET_L	1	1
to	1	0	1	1	1	1	1	1	1
S3	2	0	0	1	1	1	1	0	1
	3	0	0	0	1	X	1	0	0
to	4	0	0	1	1	X	1	0	1
S0	5	0	1	1	1	0 (*)	1	1	1
	6	0	1	1	1	1	1	1	1
	7	1	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

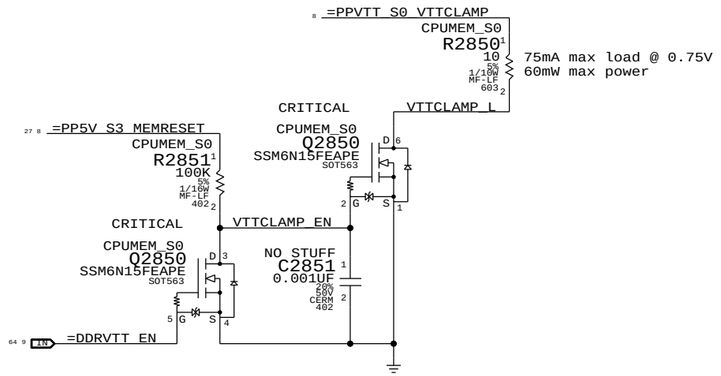
NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

1V5 S0 "PGOOD" for CPU



MEMVTT Clamp

Ensures CKE signals are held low in S3



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8 7 6 5 4 3 2 1

D C B A

PP0V75_S3_MEM_VREFDQ_A
PP0V75_S3_MEM_VREFCA_A
=PP1V5R1V35_S3_MEM_A

C2907 0.47UF 20% 4V CERM-X5R-1 201
C2908 0.47UF 20% 4V CERM-X5R-1 201
C2909 0.47UF 20% 4V CERM-X5R-1 201

U2900 DDR3-1333 FBGA (SYM VER 2) OMIT_TABLE

MEM_A_A<0> MEM_A_A<1> MEM_A_A<2> MEM_A_A<3> MEM_A_A<4> MEM_A_A<5> MEM_A_A<6> MEM_A_A<7> MEM_A_A<8> MEM_A_A<9> MEM_A_A<10> MEM_A_A<11> MEM_A_A<12> MEM_A_A<13> MEM_A_A<14> MEM_A_A<15>
MEM_A_BA<0> MEM_A_BA<1> MEM_A_BA<2>
MEM_A_RAS_L MEM_A_CAS_L MEM_A_WE_L MEM_A_ODT<0> MEM_A_ZQ<0>
MEM_RESET_L

MEM_A_DQ<0> MEM_A_DQ<6> MEM_A_DQ<7> MEM_A_DQ<5> MEM_A_DQ<3> MEM_A_DQ<1> MEM_A_DQ<2> MEM_A_DQ<4>
MEM_A_DQS_P<0> MEM_A_DQS_N<0>
MEM_A_CS_L<0> MEM_A_CKE<0>
MEM_A_CLK_P<0> MEM_A_CLK_N<0>

R2900 240 1% 1/20W MF 201

C2917 0.47UF 20% 4V CERM-X5R-1 201
C2918 0.47UF 20% 4V CERM-X5R-1 201
C2919 0.47UF 20% 4V CERM-X5R-1 201

U2910 DDR3-1333 FBGA (SYM VER 2) OMIT_TABLE

MEM_A_A<0> MEM_A_A<1> MEM_A_A<2> MEM_A_A<3> MEM_A_A<4> MEM_A_A<5> MEM_A_A<6> MEM_A_A<7> MEM_A_A<8> MEM_A_A<9> MEM_A_A<10> MEM_A_A<11> MEM_A_A<12> MEM_A_A<13> MEM_A_A<14> MEM_A_A<15>
MEM_A_BA<0> MEM_A_BA<1> MEM_A_BA<2>
MEM_A_RAS_L MEM_A_CAS_L MEM_A_WE_L MEM_A_ODT<1> MEM_A_ZQ<1>
MEM_RESET_L

MEM_A_DQ<32> MEM_A_DQ<33> MEM_A_DQ<34> MEM_A_DQ<35> MEM_A_DQ<36> MEM_A_DQ<37> MEM_A_DQ<38> MEM_A_DQ<39>
MEM_A_DQS_P<4> MEM_A_DQS_N<4>
MEM_A_CS_L<0> MEM_A_CKE<0>
MEM_A_CLK_P<0> MEM_A_CLK_N<0>

R2910 240 1% 1/20W MF 201

C2927 0.47UF 20% 4V CERM-X5R-1 201
C2928 0.47UF 20% 4V CERM-X5R-1 201
C2929 0.47UF 20% 4V CERM-X5R-1 201

U2920 DDR3-1333 FBGA (SYM VER 2) OMIT_TABLE

MEM_A_A<0> MEM_A_A<1> MEM_A_A<2> MEM_A_A<3> MEM_A_A<4> MEM_A_A<5> MEM_A_A<6> MEM_A_A<7> MEM_A_A<8> MEM_A_A<9> MEM_A_A<10> MEM_A_A<11> MEM_A_A<12> MEM_A_A<13> MEM_A_A<14> MEM_A_A<15>
MEM_A_BA<0> MEM_A_BA<1> MEM_A_BA<2>
MEM_A_RAS_L MEM_A_CAS_L MEM_A_WE_L MEM_A_ODT<2> MEM_A_ZQ<2>
MEM_RESET_L

MEM_A_DQ<14> MEM_A_DQ<9> MEM_A_DQ<10> MEM_A_DQ<15> MEM_A_DQ<11> MEM_A_DQ<13> MEM_A_DQ<8> MEM_A_DQ<12>
MEM_A_DQS_P<1> MEM_A_DQS_N<1>
MEM_A_CS_L<0> MEM_A_CKE<0>
MEM_A_CLK_P<0> MEM_A_CLK_N<0>

R2920 240 1% 1/20W MF 201

C2937 0.47UF 20% 4V CERM-X5R-1 201
C2938 0.47UF 20% 4V CERM-X5R-1 201
C2939 0.47UF 20% 4V CERM-X5R-1 201

U2930 DDR3-1333 FBGA (SYM VER 2) OMIT_TABLE

MEM_A_A<0> MEM_A_A<1> MEM_A_A<2> MEM_A_A<3> MEM_A_A<4> MEM_A_A<5> MEM_A_A<6> MEM_A_A<7> MEM_A_A<8> MEM_A_A<9> MEM_A_A<10> MEM_A_A<11> MEM_A_A<12> MEM_A_A<13> MEM_A_A<14> MEM_A_A<15>
MEM_A_BA<0> MEM_A_BA<1> MEM_A_BA<2>
MEM_A_RAS_L MEM_A_CAS_L MEM_A_WE_L MEM_A_ODT<0> MEM_A_ZQ<3>
MEM_RESET_L

MEM_A_DQ<22> MEM_A_DQ<21> MEM_A_DQ<16> MEM_A_DQ<17> MEM_A_DQ<18> MEM_A_DQ<23> MEM_A_DQ<20> MEM_A_DQ<19>
MEM_A_DQS_P<2> MEM_A_DQS_N<2>
MEM_A_CS_L<0> MEM_A_CKE<0>
MEM_A_CLK_P<0> MEM_A_CLK_N<0>

R2930 240 1% 1/20W MF 201

C2947 0.47UF 20% 4V CERM-X5R-1 201
C2948 0.47UF 20% 4V CERM-X5R-1 201
C2949 0.47UF 20% 4V CERM-X5R-1 201

U2940 DDR3-1333 FBGA (SYM VER 2) OMIT_TABLE

MEM_A_A<0> MEM_A_A<1> MEM_A_A<2> MEM_A_A<3> MEM_A_A<4> MEM_A_A<5> MEM_A_A<6> MEM_A_A<7> MEM_A_A<8> MEM_A_A<9> MEM_A_A<10> MEM_A_A<11> MEM_A_A<12> MEM_A_A<13> MEM_A_A<14> MEM_A_A<15>
MEM_A_BA<0> MEM_A_BA<1> MEM_A_BA<2>
MEM_A_RAS_L MEM_A_CAS_L MEM_A_WE_L MEM_A_ODT<0> MEM_A_ZQ<4>
MEM_RESET_L

MEM_A_DQ<32> MEM_A_DQ<33> MEM_A_DQ<34> MEM_A_DQ<35> MEM_A_DQ<36> MEM_A_DQ<37> MEM_A_DQ<38> MEM_A_DQ<39>
MEM_A_DQS_P<4> MEM_A_DQS_N<4>
MEM_A_CS_L<0> MEM_A_CKE<0>
MEM_A_CLK_P<0> MEM_A_CLK_N<0>

R2940 240 1% 1/20W MF 201

C2957 0.47UF 20% 4V CERM-X5R-1 201
C2958 0.47UF 20% 4V CERM-X5R-1 201
C2959 0.47UF 20% 4V CERM-X5R-1 201

U2950 DDR3-1333 FBGA (SYM VER 2) OMIT_TABLE

MEM_A_A<0> MEM_A_A<1> MEM_A_A<2> MEM_A_A<3> MEM_A_A<4> MEM_A_A<5> MEM_A_A<6> MEM_A_A<7> MEM_A_A<8> MEM_A_A<9> MEM_A_A<10> MEM_A_A<11> MEM_A_A<12> MEM_A_A<13> MEM_A_A<14> MEM_A_A<15>
MEM_A_BA<0> MEM_A_BA<1> MEM_A_BA<2>
MEM_A_RAS_L MEM_A_CAS_L MEM_A_WE_L MEM_A_ODT<0> MEM_A_ZQ<5>
MEM_RESET_L

MEM_A_DQ<40> MEM_A_DQ<41> MEM_A_DQ<42> MEM_A_DQ<43> MEM_A_DQ<44> MEM_A_DQ<45> MEM_A_DQ<46> MEM_A_DQ<47>
MEM_A_DQS_P<5> MEM_A_DQS_N<5>
MEM_A_CS_L<0> MEM_A_CKE<0>
MEM_A_CLK_P<0> MEM_A_CLK_N<0>

R2950 240 1% 1/20W MF 201

C2967 0.47UF 20% 4V CERM-X5R-1 201
C2968 0.47UF 20% 4V CERM-X5R-1 201
C2969 0.47UF 20% 4V CERM-X5R-1 201

U2960 DDR3-1333 FBGA (SYM VER 2) OMIT_TABLE

MEM_A_A<0> MEM_A_A<1> MEM_A_A<2> MEM_A_A<3> MEM_A_A<4> MEM_A_A<5> MEM_A_A<6> MEM_A_A<7> MEM_A_A<8> MEM_A_A<9> MEM_A_A<10> MEM_A_A<11> MEM_A_A<12> MEM_A_A<13> MEM_A_A<14> MEM_A_A<15>
MEM_A_BA<0> MEM_A_BA<1> MEM_A_BA<2>
MEM_A_RAS_L MEM_A_CAS_L MEM_A_WE_L MEM_A_ODT<2> MEM_A_ZQ<6>
MEM_RESET_L

MEM_A_DQ<48> MEM_A_DQ<49> MEM_A_DQ<50> MEM_A_DQ<51> MEM_A_DQ<52> MEM_A_DQ<53> MEM_A_DQ<54> MEM_A_DQ<55>
MEM_A_DQS_P<6> MEM_A_DQS_N<6>
MEM_A_CS_L<0> MEM_A_CKE<0>
MEM_A_CLK_P<0> MEM_A_CLK_N<0>

R2960 240 1% 1/20W MF 201

C2977 0.47UF 20% 4V CERM-X5R-1 201
C2978 0.47UF 20% 4V CERM-X5R-1 201
C2979 0.47UF 20% 4V CERM-X5R-1 201

U2970 DDR3-1333 FBGA (SYM VER 2) OMIT_TABLE

MEM_A_A<0> MEM_A_A<1> MEM_A_A<2> MEM_A_A<3> MEM_A_A<4> MEM_A_A<5> MEM_A_A<6> MEM_A_A<7> MEM_A_A<8> MEM_A_A<9> MEM_A_A<10> MEM_A_A<11> MEM_A_A<12> MEM_A_A<13> MEM_A_A<14> MEM_A_A<15>
MEM_A_BA<0> MEM_A_BA<1> MEM_A_BA<2>
MEM_A_RAS_L MEM_A_CAS_L MEM_A_WE_L MEM_A_ODT<0> MEM_A_ZQ<7>
MEM_RESET_L

MEM_A_DQ<56> MEM_A_DQ<57> MEM_A_DQ<58> MEM_A_DQ<59> MEM_A_DQ<60> MEM_A_DQ<61> MEM_A_DQ<62> MEM_A_DQ<63>
MEM_A_DQS_P<7> MEM_A_DQS_N<7>
MEM_A_CS_L<0> MEM_A_CKE<0>
MEM_A_CLK_P<0> MEM_A_CLK_N<0>

R2970 240 1% 1/20W MF 201

SDRAM Bypassing (NOTE: 2x 2.2uF and 3x 0.1uF per chip)

=PP1V5R1V35_S3_MEM_A

C2900 C2901 C2910 C2911 C2920 C2921 C2930 C2931 2.2UF 20% 10V X5R-CERM 402
C2903 C2904 C2905 C2913 C2914 C2915 C2923 C2924 C2925 C2933 C2934 C2935 0.1UF 10% 6.3V X5R 201
C2940 C2941 C2950 C2951 C2960 C2961 C2970 C2971 2.2UF 20% 10V X5R-CERM 402
C2943 C2944 C2945 C2953 C2954 C2955 C2963 C2964 C2965 C2973 C2974 C2975 0.1UF 10% 6.3V X5R 201

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE: DDR3 SDRAM Bank A (1 OF 2)

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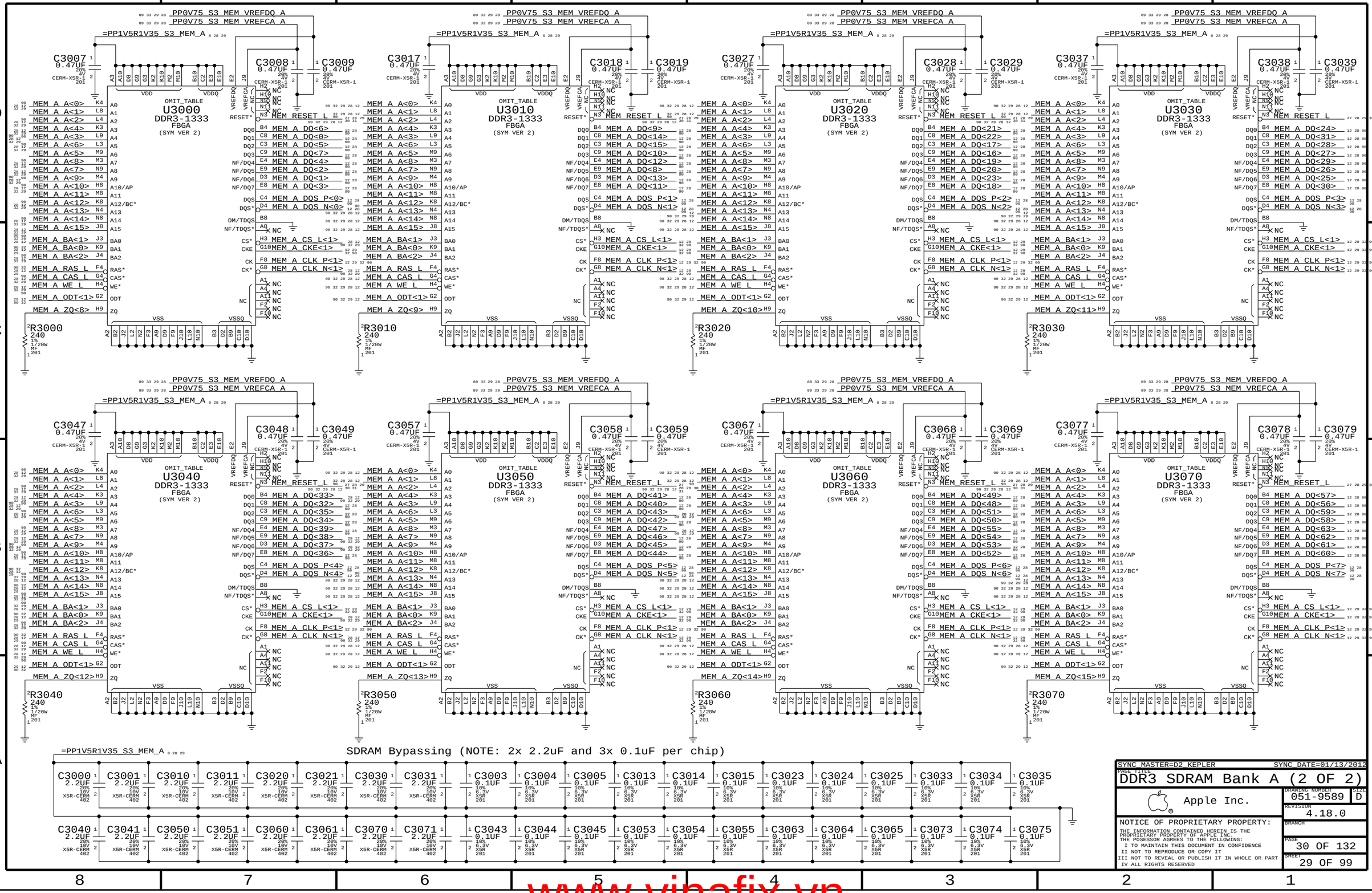

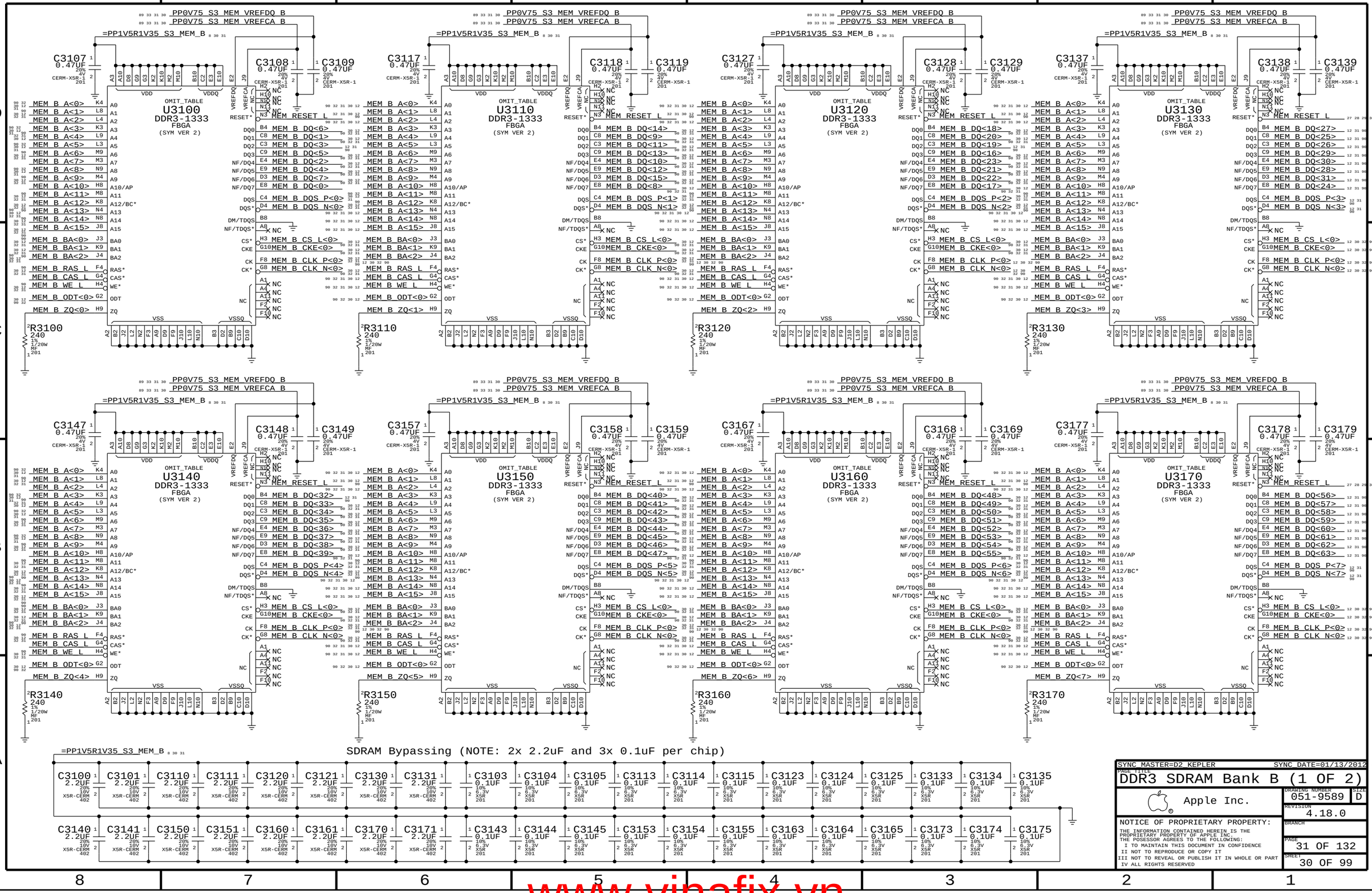

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

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DDR3 SDRAM Bank B (1 OF 2)

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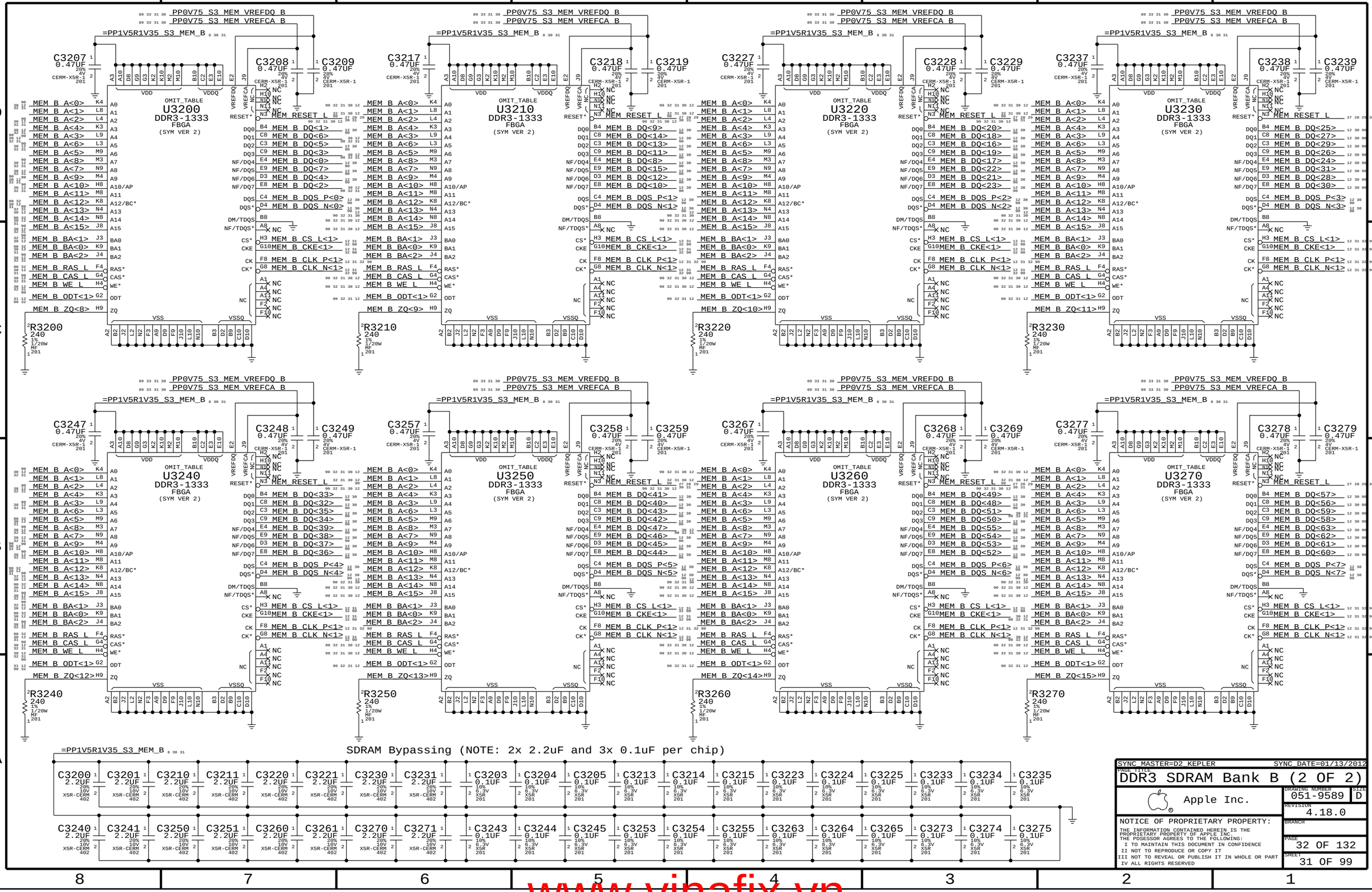

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE
DDR3 SDRAM Bank B (2 OF 2)

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JEDEC 4.20.18 Unbuffered SODIMM Raw Card F spec recommends 36 Ohm term to VTT for CS,CKE,ODT and 36 Ohm for BA,A,RAS,CAS,WE

=PP0V75_S0_MEM_VTT_A

MEM_A_CS_L<1>	RP3305	36	1	8	5% 1/32W	4X0201
MEM_A_CKE<0>	RP3301	36	4	5	5% 1/32W	4X0201
MEM_A_A<0>	RP3302	36	2	7	5% 1/32W	4X0201
MEM_A_A<7>	RP3306	36	2	7	5% 1/32W	4X0201
MEM_A_A<5>	RP3303	36	1	8	5% 1/32W	4X0201
MEM_A_BA<0>	RP3302	36	1	8	5% 1/32W	4X0201
MEM_A_ODT<0>	RP3301	36	2	7	5% 1/32W	4X0201
MEM_A_A<15>	RP3305	36	2	7	5% 1/32W	4X0201
MEM_A_BA<1>	RP3303	36	2	7	5% 1/32W	4X0201
MEM_A_A<14>	RP3307	36	3	6	5% 1/32W	4X0201
MEM_A_A<8>	RP3306	36	1	8	5% 1/32W	4X0201
MEM_A_A<12>	RP3305	36	3	6	5% 1/32W	4X0201
MEM_A_A<9>	RP3306	36	4	5	5% 1/32W	4X0201
MEM_A_BA<2>	RP3302	36	3	6	5% 1/32W	4X0201
MEM_A_ODT<1>	RP3304	36	3	6	5% 1/32W	4X0201
MEM_A_A<4>	RP3303	36	4	5	5% 1/32W	4X0201
MEM_A_RAS_L	RP3304	36	1	8	5% 1/32W	4X0201
MEM_A_A<1>	RP3307	36	2	7	5% 1/32W	4X0201
MEM_A_WE_L	RP3302	36	4	5	5% 1/32W	4X0201
MEM_A_A<6>	RP3303	36	3	6	5% 1/32W	4X0201
MEM_A_A<2>	RP3307	36	1	8	5% 1/32W	4X0201
MEM_A_A<3>	RP3305	36	4	5	5% 1/32W	4X0201
MEM_A_A<13>	RP3307	36	4	5	5% 1/32W	4X0201
MEM_A_CKE<1>	RP3304	36	2	7	5% 1/32W	4X0201
MEM_A_A<10>	RP3304	36	4	5	5% 1/32W	4X0201
MEM_A_CAS_L	RP3301	36	3	6	5% 1/32W	4X0201
MEM_A_CS_L<0>	RP3301	36	1	8	5% 1/32W	4X0201
MEM_A_A<11>	RP3306	36	3	6	5% 1/32W	4X0201

C3300 0.47UF 20% 4V CERM-X5R-1 201
C3302 0.47UF 20% 4V CERM-X5R-1 201
C3303 0.47UF 20% 4V CERM-X5R-1 201
C3304 0.47UF 20% 4V CERM-X5R-1 201
C3305 0.47UF 20% 4V CERM-X5R-1 201
C3306 0.47UF 20% 4V CERM-X5R-1 201
C3307 0.47UF 20% 4V CERM-X5R-1 201
C3308 0.47UF 20% 4V CERM-X5R-1 201
C3310 0.47UF 20% 4V CERM-X5R-1 201

=PP0V75_S0_MEM_VTT_B

MEM_B_ODT<0>	RP3322	36	2	7	5% 1/32W	4X0201
MEM_B_A<13>	RP3325	36	1	8	5% 1/32W	4X0201
MEM_B_A<15>	RP3328	36	1	8	5% 1/32W	4X0201
MEM_B_A<11>	RP3325	36	2	7	5% 1/32W	4X0201
MEM_B_CAS_L	RP3328	36	2	7	5% 1/32W	4X0201
MEM_B_A<1>	RP3325	36	3	6	5% 1/32W	4X0201
MEM_B_CS_L<0>	RP3320	36	2	7	5% 1/32W	4X0201
MEM_B_A<14>	RP3326	36	4	5	5% 1/32W	4X0201
MEM_B_A<0>	RP3330	36	2	7	5% 1/32W	4X0201
MEM_B_BA<2>	RP3320	36	3	6	5% 1/32W	4X0201
MEM_B_BA<1>	RP3330	36	1	8	5% 1/32W	4X0201
MEM_B_A<4>	RP3330	36	3	6	5% 1/32W	4X0201
MEM_B_CS_L<1>	RP3324	36	4	5	5% 1/32W	4X0201
MEM_B_A<6>	RP3326	36	2	7	5% 1/32W	4X0201
MEM_B_A<12>	RP3324	36	1	8	5% 1/32W	4X0201
MEM_B_A<9>	RP3326	36	3	6	5% 1/32W	4X0201
MEM_B_CKE<0>	RP3322	36	3	6	5% 1/32W	4X0201
MEM_B_A<7>	RP3326	36	1	8	5% 1/32W	4X0201
MEM_B_A<5>	RP3330	36	4	5	5% 1/32W	4X0201
MEM_B_A<3>	RP3324	36	3	6	5% 1/32W	4X0201
MEM_B_A<2>	RP3324	36	2	7	5% 1/32W	4X0201
MEM_B_A<8>	RP3325	36	4	5	5% 1/32W	4X0201
MEM_B_BA<0>	RP3320	36	4	5	5% 1/32W	4X0201
MEM_B_A<10>	RP3320	36	1	8	5% 1/32W	4X0201
MEM_B_RAS_L	RP3322	36	1	8	5% 1/32W	4X0201
MEM_B_ODT<1>	RP3328	36	4	5	5% 1/32W	4X0201
MEM_B_CKE<1>	RP3328	36	3	6	5% 1/32W	4X0201
MEM_B_WE_L	RP3322	36	4	5	5% 1/32W	4X0201

C3320 0.47UF 20% 4V CERM-X5R-1 201
C3322 0.47UF 20% 4V CERM-X5R-1 201
C3323 0.47UF 20% 4V CERM-X5R-1 201
C3324 0.47UF 20% 4V CERM-X5R-1 201
C3325 0.47UF 20% 4V CERM-X5R-1 201
C3326 0.47UF 20% 4V CERM-X5R-1 201
C3327 0.47UF 20% 4V CERM-X5R-1 201
C3328 0.47UF 20% 4V CERM-X5R-1 201
C3330 0.47UF 20% 4V CERM-X5R-1 201

MEM Clock Termination

Place RC end termination after last DRAM
Place Source Cterm at neckdown at first DRAM

MEM_A_CLK_N<0>	R3350	30	1	2	5% 1/20W MF	201
MEM_A_CLK0_TERM_R	C3351	0.1UF	1	2	10% 6.3V X5R	201
C3350 3.3PF 5% 25V CERM 201 — PLACE_NEAR=U2900.F7:3.2mm						
MEM_A_CLK_P<0>	R3351	30	1	2	5% 1/20W MF	201
MEM_A_CLK_N<1>	R3355	30	1	2	5% 1/20W MF	201
MEM_A_CLK1_TERM_R	C3356	0.1UF	1	2	10% 6.3V X5R	201
C3355 3.3PF 5% 25V CERM 201 — PLACE_NEAR=U3000.F7:3.2mm						
MEM_A_CLK_P<1>	R3356	30	1	2	5% 1/20W MF	201
MEM_B_CLK_N<0>	R3360	30	1	2	5% 1/20W MF	201
MEM_B_CLK0_TERM_R	C3361	0.1UF	1	2	10% 6.3V X5R	201
C3360 3.3PF 5% 25V CERM 201 — PLACE_NEAR=U3170.F7:3.2mm						
MEM_B_CLK_P<0>	R3361	30	1	2	5% 1/20W MF	201
MEM_B_CLK_N<1>	R3365	30	1	2	5% 1/20W MF	201
MEM_B_CLK1_TERM_R	C3366	0.1UF	1	2	10% 6.3V X5R	201
C3365 3.3PF 5% 25V CERM 201 — PLACE_NEAR=U3270.F7:3.2mm						
MEM_B_CLK_P<1>	R3366	30	1	2	5% 1/20W MF	201

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE: DDR3 Termination

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NOTE: Must not enable more than two SO-DIMM margining buffers at once or VRef source may be overloaded.

Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DDR_BUF
- =PPDDR_S3_MEMVREF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:

DDRVREF_DAC - Stuffs Apple margining circuit.
VREFDQ:LDO - LDO outputs sent to DQ inputs.
VREFDQ:LDO_DAC - Margined LDO outputs sent to DQ inputs.
VREFDQ:M1_M3 - CPU margined DDR voltage divider sent to DQ inputs.
VREFDQ:M1_DAC - DAC margined DDR voltage divider sent to DQ inputs.
VREFCA:LDO - LDO outputs sent to CA inputs.
VREFCA:LDO_DAC - DAC margined LDO outputs sent to CA inputs.

RST* on 'platform reset' so that system watchdog will disable margining.

NOTE: Margining will be disabled across all soft-resets and sleep/wake cycles.

NOTE: CPU DAC output step sizes:
DDR3 (1.5V) 7.70mV per step
DDR3L (1.35V) 6.99mV per step

NOTE: MEMVREG and FRAMEBUF share a DAC output, cannot enable both at the same time!

Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3403,R3405		VREFDQ:LDO
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3409,R3411		VREFCA:LDO

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0218	4	RES,MTL FILM,1K,1%,0402,SM,LF	R3421,R3422,R3441,R3442		VREFDQ:M1_DAC
114S0171	2	RES,MTL FILM,332,1%,0402,SM,LF	R3404,R3406		VREFDQ:M1_DAC

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% VRef)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value	0.75V (DAC: 0x3A)				1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:	0.300V - 1.200V (+/- 450mV)				1.000V - 2.000V (+/- 500mV)	1.056V - 1.442V (+/- 180mV)
DAC range:	0.000V - 1.501V (0x00 - 0x74)				0.000V - 3.000V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
VRef current:	+3.4mA - -3.4mA (- = sourced)				+61uA - -61uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:	7.69mV / step @ output				8.59mV / step @ output	1.51mV / step @ output

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE: DDR3/FRAMEBUF VREF MARGINING

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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0002	4	RES, 00HM, 0201	L3570,L3571,L3573,L3574		

AIRPORT

OMIT_TABLE
L3570
0.6NH+/-0.1NH-0.85A
0201
PLACE_NEAR=J3501.15:2.54MM
C3531 0.1UF 10% 16V X7R-CERM 0402
92 PCIE_AP_R2D_PI_P
PCIE_AP_R2D_C_P IN 17 92
NOSTUFF C3570 0.1UF 10% 16V XSR-CERM 0201
NOSTUFF C3571 0.1UF 10% 16V XSR-CERM 0201
L3571
0.6NH+/-0.1NH-0.85A
0201
92 PCIE_AP_R2D_PI_N
PCIE_AP_R2D_C_N IN 17 92
C3530 0.1UF 10% 16V X7R-CERM 0402
PLACE_NEAR=J3501.17:2.54MM
WIFI_EVENT_L IN 7 41 42
NOSTUFF C3572 0.1UF 10% 16V XSR-CERM 0201
OMIT_TABLE
NOSTUFF C3573 0.1UF 10% 16V XSR-CERM 0201
OMIT_TABLE
L3573
0.6NH+/-0.1NH-0.85A
0201
92 7 PCIE_AP_R2D_P
92 7 PCIE_AP_R2D_N
PCIE_AP_D2R_P OUT 17 92
NOSTUFF C3574 0.1UF 10% 16V XSR-CERM 0201
NOSTUFF C3575 0.1UF 10% 16V XSR-CERM 0201
L3574
0.6NH+/-0.1NH-0.85A
0201
PCIE_AP_D2R_N OUT 17 92
NOSTUFF C3576 0.1UF 10% 16V XSR-CERM 0201
OMIT_TABLE
NOSTUFF C3577 0.1UF 10% 16V XSR-CERM 0201
92 7 PCIE_AP_D2R_PI_P
92 7 PCIE_AP_D2R_PI_N

CRITICAL
514S0335
J3501
SSD-K99
F-RT-SM1

CRITICAL
L3501
90-OHM-100MA
DLP11S
SYM_VER-1
96 7 PCIE_CLK100M_AP_CONN_P
PCIE_CLK100M_AP_P IN 17 92
96 7 PCIE_CLK100M_AP_CONN_N
PCIE_CLK100M_AP_N IN 17 92
PLACE_NEAR=J3501.11:2.54MM

BLUETOOTH

PCIE_WAKE_L OUT 7 18
91 7 USB_BT_CONN_N
91 7 USB_BT_CONN_P
PP3V3_S3RS4_BT_F
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
C3532 0.01UF 10% 16V X7R-CERM 0402
BTPWR:S4 L3505 =PP3V3_S4_BT 8
FERR-120-OHM-1.5A 0402-LF
PLACE_NEAR=J3501.27:2.54MM
BTPWR:S3 L3506 =PP3V3_S3_BT 8
FERR-120-OHM-1.5A 0402-LF
PLACE_NEAR=J3501.27:2.54MM

NOSTUFF R3517 15K 1% 1/20W MF 201
BTPWR:S3 R3518 0 5% 1/20W MF 201
NOSTUFF R3515 15K 1% 1/20W MF 201
NOSTUFF R3516 15K 1% 1/20W MF 201
U3510 PI3USB102ZLE TQFN CRITICAL
VCC
Y+
Y-
SEL
GND
M+
M-
D+
D-
OE*
PP3V3_S3RS4_BT_F 7 34
C3510 0.1UF 10% 6.3V X5R 201
USB_BT_WAKE_P 5 91
USB_BT_WAKE_N 4 91
USB_BT_P BI 9 91
USB_BT_N BI 9 91
NOSTUFF R3514 15K 1% 1/20W MF 201
BTPWR:S4 R3512 15K 1% 1/20W MF 201
NOSTUFF R3513 15K 1% 1/20W MF 201
SIGNAL_MODEL=EMPTY
BTPWR:S4
Q3510 SSM3K15FV SOD-VESM-HF
=BT_WAKE_L OUT 42

BTPWR:S4 R3511 0 5% 1/20W MF 201
PM_SLP_S4_L IN
BTMUX_SEL
NOSTUFF C3511 0.01UF 10% 16V X7R-CERM 0402

SEL	OUTPUT
L	USB_BT_WAKE
H	USB_BT

7 AP_RESET_CONN_L
7 AP_CLKREQ_Q_L

Supervisor & CLKFREG # Isolation
Delay = 130 ms +/- 20%
PP3V3_WLAN_F 34 99
=PP3V3_S3_WLAN 8 34
R3553 100K 1% 1/16W MF-LF 402
R3554 232K 1% 1/16W MF-LF 402
P3V3WLAN_VMON
CRITICAL
VDD
U3540
SLG4AP041V
TDFN
SENSE
VREF
DLY
RESET*
MR*
EN
OUT (OD)
IN
THRM PAD
GND
C3540 0.1uF 20% 10V CERM 402
AP_RESET_L IN 25
AP_PWR_EN IN 19 24 70
AP_CLKREQ_L OUT 17
R3555 100K 1% 1/16W MF-LF 402

ALS CAMERA

OMIT
CRITICAL
J3502
CCR20-6K710S
F-RT-SM
=I2C_ALS_SDA BI 44
=I2C_ALS_SCL IN 44
7 PP5V_S3_ALSCAMERA_F
91 7 USB_CAMERA_CONN_N
91 7 USB_CAMERA_CONN_P
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
CRITICAL
L3507
90-OHM
DLP0NS
SYM_VER-1
USB_CAMERA_N BI 19 91
USB_CAMERA_P BI 19 91
PLACE_NEAR=J3502.3:2.54MM
275 mA peak
206 mA nominal max
PLACE_NEAR=J3502.6:2.54MM
L3508
FERR-120-OHM-1.5A
0402-LF
=PP5V_S3_ALSCAMERA 8
C3552 0.1uF 20% 10V CERM 402

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
518S0767	1	CONN,HDR,TWIN:AX,P=0.4MM,GP,HF	J3502	CRITICAL	

CURRENT SENSE

155S0367
L3504
FERR-120-0HM-3A
0603
1A PEAK
42 7 PP3V3_WLAN
PP3V3_WLAN_F IN 34 99
PP3V3_WLAN_R OUT
MIN_LINE_WIDTH=1 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MIN_LINE_WIDTH=1 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V
C3522 0.1uF 20% 10V CERM 402
C3521 0.1uF 20% 10V CERM 402
PLACE_NEAR=J3501.29:2.54MM
PLACE_NEAR=J3501.29:2.54MM

3V S3 WLAN FET

MOSFET	DMP2018LFK
CHANNEL	P-TYPE
RDS(ON) @ 2.5V	14 mOhm Typ 20 mOhm Max
LOADING	1 A (EDP)

CRITICAL
Q3550
DMP2018LFK
DFN2563-6
=PP3V3_S3_WLAN 8 34
C3551 0.033UF 10% 16V X5R 402
R3551 10K 5% 1/16W MF-LF 402
C3550 0.1UF 10% 16V X7R-CERM 0402
P3V3WLAN_SS
R3550 33K 5% 1/16W MF-LF 402
PM_WLAN_EN_L IN 70

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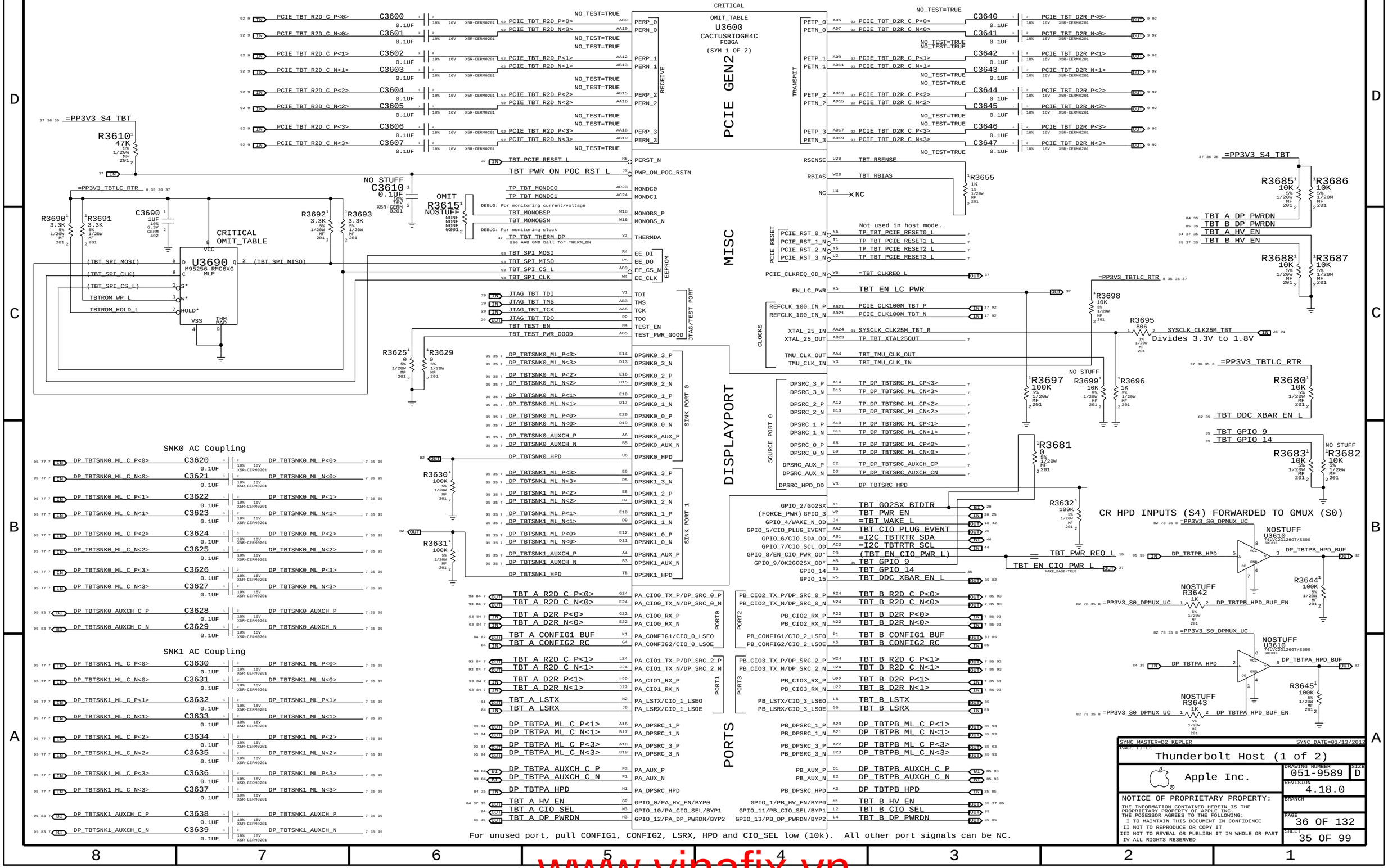

8 =PP1V05_TBTLC_RTR
???? mW (Single Port)
250 mW (Dual Port)
EDP: 1600 mA

C3700 10UF 20% 6.3V CERM-X5R 0402-1
C3710 1.0UF 20% 10V X5R-CERM 0201-1
C3711 1.0UF 20% 10V X5R-CERM 0201-1
C3712 1.0UF 20% 10V X5R-CERM 0201-1
C3713 1.0UF 20% 10V X5R-CERM 0201-1
C3714 1.0UF 20% 10V X5R-CERM 0201-1
C3701 10UF 20% 6.3V CERM-X5R 0402-1
C3715 1.0UF 20% 10V X5R-CERM 0201-1
C3716 1.0UF 20% 10V X5R-CERM 0201-1
C3717 1.0UF 20% 10V X5R-CERM 0201-1

CRITICAL
OMIT_TABLE
U3600
CACTUSRIDGE4C
FCBGA
(SYM 2 OF 2)

VCC
J10 VCC1P0_ON
J12 VCC1P0_ON
J14 VCC1P0_ON
J16 VCC1P0_ON
J8 VCC1P0_ON
K17 VCC1P0_ON
T15 VCC1P0_ON
U14 VCC1P0_ON
V7 VCC1P0_ON
W8 VCC1P0_ON
G10 VCC1P0_PE
G12 VCC1P0_PE
G14 VCC1P0_PE
G16 VCC1P0_PE
G18 VCC1P0_PE
H19 VCC1P0_PE
K19 VCC1P0_PE
M19 VCC1P0_PE
P19 VCC1P0_PE
T19 VCC1P0_PE
V15 VCC1P0_PE
V19 VCC1P0_PE
W12 VCC1P0_PE
W14 VCC1P0_PE
G8 VCC1P0_DPAUX
H9 VCC1P0_DPAUX
K11 VCC1P0
K15 VCC1P0
L10 VCC1P0
L14 VCC1P0
M11 VCC1P0
M15 VCC1P0
N10 VCC1P0
N14 VCC1P0
P11 VCC1P0
P15 VCC1P0
R10 VCC1P0
R14 VCC1P0
T11 VCC1P0
U10 VCC1P0
V11 VCC1P0
W10 VCC1P0
M7 VCC3P3
P7 VCC3P3
T7 VCC3P3
L18 VCC3P3_CIO
N18 VCC3P3_CIO
R18 VCC3P3_CIO
H11 VCC3P3_DP
H13 VCC3P3_DP
H15 VCC3P3_DP
H17 VCC3P3_DP
H7 VCC3P3_DPAUX
K7 VCC3P3_POC

GND
AD1 VSS
K13 VSS
K9 VSS
L12 VSS
L16 VSS
L8 VSS
M13 VSS
M17 VSS
M9 VSS
N12 VSS
N16 VSS
N8 VSS
P13 VSS
P17 VSS
P9 VSS
R12 VSS
R16 VSS
R8 VSS
T13 VSS
T17 VSS
T9 VSS
U12 VSS
U16 VSS
U8 VSS
V9 VSS
A2 VSSPE
A24 VSSPE
AA14 VSSPE
AA20 VSSPE
AA22 VSSPE
AA8 VSSPE
AB11 VSSPE
AB17 VSSPE
AB7 VSSPE
AC10 VSSPE
AC12 VSSPE
AC14 VSSPE
AC16 VSSPE
AC18 VSSPE
AC20 VSSPE
AC22 VSSPE
AC4 VSSPE
AC6 VSSPE
AC8 VSSPE
B1 VSSPE
B7 VSSPE
C10 VSSPE
C12 VSSPE
C14 VSSPE
C16 VSSPE
C18 VSSPE
C20 VSSPE
C22 VSSPE
C24 VSSPE
C4 VSSPE
C6 VSSPE
C8 VSSPE
D21 VSSPE
D23 VSSPE
E4 VSSPE
F11 VSSPE
F13 VSSPE
F15 VSSPE
F17 VSSPE
F19 VSSPE
F21 VSSPE
F23 VSSPE
F5 VSSPE
F7 VSSPE
F9 VSSPE
G20 VSSPE
H21 VSSPE
H23 VSSPE
J18 VSSPE
J20 VSSPE
K21 VSSPE
K23 VSSPE
L20 VSSPE
M21 VSSPE
M23 VSSPE
N20 VSSPE
P21 VSSPE
P23 VSSPE
R20 VSSPE
T21 VSSPE
T23 VSSPE
U18 VSSPE
V13 VSSPE
V17 VSSPE
V21 VSSPE
V23 VSSPE
Y11 VSSPE
Y13 VSSPE
Y15 VSSPE
Y17 VSSPE
Y19 VSSPE
Y21 VSSPE
Y23 VSSPE
Y9 VSSPE

=PP1V05_TBTCIO_RTR 8
???? mW (Single-Port)
2700 mW (Dual-Port)
EDP: 1100 mA

C3740 1.0UF 20% 10V X5R-CERM 0201-1
C3741 1.0UF 20% 10V X5R-CERM 0201-1
C3742 1.0UF 20% 10V X5R-CERM 0201-1
C3743 1.0UF 20% 10V X5R-CERM 0201-1
C3744 1.0UF 20% 10V X5R-CERM 0201-1
C3745 1.0UF 20% 10V X5R-CERM 0201-1
C3705 10UF 20% 6.3V CERM-X5R 0402-1

=PP3V3_TBTLC_RTR 8 35 37
??? mW (Single-Port)
250 mW (Dual-Port)
EDP: 240 mA

C3770 1.0UF 20% 10V X5R-CERM 0201-1
C3771 1.0UF 20% 10V X5R-CERM 0201-1
C3772 1.0UF 20% 10V X5R-CERM 0201-1
C3773 1.0UF 20% 10V X5R-CERM 0201-1
C3774 1.0UF 20% 10V X5R-CERM 0201-1
C3760 10UF 20% 6.3V CERM-X5R 0402-1

PP3V3_S4_TBT
VOLTAGE=3.3V MAKE_BASE=TRUE MIN_LINE_WIDTH=0.6 MM MIN_NECK_WIDTH=0.1 MM
37 35 =PP3V3_S4_TBT
EDP: 10 mA
R3790 0 5% 1/16W MF-LF 402
=PP3V3_S4_TBT_R 8
C3790 1.0UF 20% 10V X5R-CERM 0201-1

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Thunderbolt 15V Boost Regulator

Page Notes

Power aliases required by this page:
- =PPVIN_SW_TBTBST (8-13V Boost Input)
- =PP15V_TBT_REG (15V Boost Output)
- =PP3V3_TBT_P3V3TBTFET (3.3V FET Input)
- =PP3V3_TBTLC_FET (3.3V FET Output)
- =PP3V3_S0_TBTPWRCTL
- =PP1V05_TBT_P1V05TBTFET (1.05V FET Input)
- =PP1V05_TBTLC_FET (1.05V FET Output)

Signal aliases required by this page:
- =TBT_CLKREQ_L
- =TBT_RESET_L

BOM options provided by this page:
TBTBST:Y - Stuffs 15V boost circuitry.

SI8409DB:
Vds(max): -30V
Vgs(max): +/-12V
Vgs(th): -1.4V
Rds(on): 46mOhm @ 4.5V Vgs
Id(max): 3.7A @ 70C

=PPVIN_SW_TBTBST
8-13V Input
Changes required
for 2S.

CRITICAL TBTBST:Y Q3880 SI8409DB 8GA

PPVIN_SW_TBTBST
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
Voltage not specified here, add property on another page.

CRITICAL TBTBST:Y L3895 3.3UH-6.5A PIMB063T-SM

TBTBST_BOOST
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_NODE=TRUE
DIOT=TRUE

TBTBST:Y R3880 470K 5% 1/16W MF-LF 402
TBTBST:Y C3880 0.1UF 10% 16V X5R-CERM 402
TBTBST_PWREN_DIV_L
TBTBST:Y R3881 330K 5% 1/16W MF-LF 402
TBTBST_PWREN_L

TBTBST:Y R3891 200K 1% 1/16W MF-LF 402 <R1>
TBTBST:Y C3860 10UF 20% 25V X5R-CERM 0603
TBTBST:Y C3861 10UF 20% 25V X5R-CERM 0603

TBTBST_EN_UVLO
TBTBST_INTVCC
TBTBST_VC
TBTBST_RT
TBTBST_SS
TBTBST_VC_RC
GND_TBTBST_SGND
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V

CRITICAL TBTBST:Y U3890 LT3957 QFN
25 EN/UVLO
28 INTVCC
30 VC
33 RT
32 SS
34 SYNC
27 VIN
8 9 20 21 38 SW
6 SNS1
3 SNS2
31 FBX
4 SGND
12 13 14 15 16 17 GND

TBTBST_SNS1
TBTBST_SNS2
TBTBST_VSNS
TBTBST_FBX

TBTBST:Y R3889 0 5% 1/20W MF 201
CRITICAL TBTBST:Y D3895 PDS540XF PWRDI5
XW3895 SM
PLACE_NEAR=C3895.1:2 mm
NC
TBTBST:Y C3888 10PF 5% 50V C0G-CERM 0402
TBTBST:Y R3895 137K 1% 1/10W MF-LF 402 <Ra>
NO STUFF C3889 100PF 5% 50V CERM 402
TBTBST:Y R3896 15.8K 1% 1/10W MF-LF 402 <Rb>
TBTBST:Y C3895 10UF 10% 25V X5R 1206-2
TBTBST:Y C3896 20% 25V POLY-TANT CASE-D3L
NO STUFF C3897 10UF 10% 25V X5R 805

=PP15V_TBT_REG
Vout = 15.47V
Max Current = 2A?
Freq = 300KHz
TBTBST:Y C3899 0.001UF 10% 50V X7R-CERM 0402

TBTBST:Y R3892 73.2K 1% 1/16W MF-LF 402 <R2>
TBTBST:Y C3890 2.2UF 20% 10V X5R-CERM 402
TBTBST:Y C3891 2.2UF 20% 10V X5R-CERM 402
TBTBST:Y C3892 2.2UF 20% 10V X5R-CERM 402
TBTBST:Y C3887 68PF 5% 50V C0G-CERM 0402
TBTBST:Y R3893 49.9K 1% 1/10W MF-LF 402
TBTBST:Y C3893 0.0033UF 10% 50V X7R-CERM 0402
TBTBST:Y R3894 28.7K 1% 1/10W MF-LF 402
TBTBST:Y C3894 0.33UF 10% 6.3V CERM-X5R 402

UVLO(falling) = 1.22 * (R1 + R2) / R2
UVLO(rising) = UVLO(falling) + (2uA * R1)
UVLO = 4.55V (falling), 4.95 (rising)

SGND shorted to GND inside package, no XW necessary.

Vout = 1.6V * (1 + Ra / Rb)

TBTBST:Y Q3805 SSM6N37FEAPE SOT563
TBT_A_HV_EN
TBT_B_HV_EN

Supervisor & CLKREQ# Isolation

=PP3V3_S0_TBTPWRCTL
Q3840 SSM3K15FV SOD-VESM-HF
C3800 0.1UF 10% 16V X5R-CERM 0201
R3840 10K 5% 1/20W MF 201
TBT_EN_LC_PWR
Platform (PCIe) Reset
=TBT_RESET_L
TBT_CLKREQ_L
Pull-ups provided by SB page.

CRITICAL U3800 SLG4AP016V TDFN
VDD
SENSE 0.7V
DLY
RESET*
MR*
EN
OUT (OD)
IN
THRM PAD
GND

=PP3V3_TBTLC_RTR
R3807 100K 5% 1/20W MF 201
PP1V05_TBTLC
TBT_PCIE_RESET_L
DLY = 60 ms +/- 20%
=TBT_CLKREQ_L
TBT_CLKREQ_ISOL_L
MAKE_BASE=TRUE

TBTBST:Y Q3888 SSM6N37FEAPE SOT563
Max Vgs: 10V
TBTBST_SHDN_DIV
TBTBST:Y R3888 330K 5% 1/10W MF-LF 402
TBTBST:Y R3887 330K 5% 1/10W MF-LF 402
TBTBST:Y Q3888 SSM6N37FEAPE SOT563
SMC_DELAYED_PWRGD

3.3V TBT "LC" Switch

=PP3V3_S0_P3V3TBTFET
U3810 TPS22924 CSP
VIN VOUT ON GND
CRITICAL
=PP3V3_TBTLC_FET
Max Current = 2A (85C)
R3811 36.5K 1% 1/20W MF 201
C3810 1UF 20% 6.3V X5R 0201
C3811 1UF 10% 6.3V CERM 402
TBT_EN_LC_3V3
TBT_EN_LC_ISOL
R3816 0 5% 1/20W MF 201
TBT_EN_LC_1V05

U3810	
Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.3 mOhm Typ 24 mOhm Max

TBT "POC" Power-up Reset

Intel investigating whether RC is sufficient.

=PP3V3_S4_TBT
CRITICAL U3830 TPS3808 QFN
VDD SENSE CT MR* RESET* GND THRM PAD
Pull-up: R3610
TBTPOCRST_CT
C3831 0.0047UF 10% 25V CERM 0402
C3830 0.1UF 10% 25V X5R 402
TPS3808G25
Vt = 2.33V +/- 2%
Delay = 27.3ms
TBTPOCRST_MR_L
TBT_PWR_ON_POC_RST_L
Q3825 SSM6N37FEAPE SOT563
C3825 330PF 10% 16V X7R-CERM 0201
=PP3V3_S0_PCH_GPIO
R3830 100K 5% 1/20W MF 201
TBT_SW_RESET_L

1.05V TBT "LC" Switch

=PP1V05_S0_P1V05TBTFET
U3815 TPS22924 CSP
VIN VOUT ON GND
CRITICAL
=PP1V05_TBTLC_FET
Max Current = 2A (85C)
C3815 1UF 20% 6.3V X5R 0201
NOSTUFF C3816 1UF 10% 6.3V CERM 402
C3816 must be 10%
RC guarantees minimum 5ms to reach 0.5V

U3815	
Part	TPS22924C
Type	Load Switch
R(on) @ 1.0V	20.3 mOhm Typ 28.6 mOhm Max

1.05V TBT "CIO" Switch

=PP1V05_S0_P1V05TBTFET
=PP3V3_TBTLC_RTR
U3820 TPS22920 CSP
VIN VOUT ON GND
CRITICAL
=PP1V05_TBTCIO_FET
Max Current = 4A (85C)
R3820 100K 5% 1/20W MF 201
TBT_EN_CIO_PWR
Q3825 SSM6N37FEAPE SOT563
C3820 1UF 20% 6.3V X5R 0201
TBT_EN_CIO_PWR_L

U3820	
Part	TPS22920
Type	Load Switch
R(on) @ 1.05V	8 mOhm Typ 11.5 mOhm Max

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J4410
AXK732327G
F-ST-SM

25	IN	=ENET_RESET_L	1	2	PM_SLP_S3_L	IN	7 18 27 41 70
17 7	OUT	ENET_CLKREQ_L	3	4	PM_SLP_S4_L	IN	7 18 27 34 40 41 70
9 7	IN	SD_PWR_EN	5	6	HDMI_EG_DDC_CLK	IN	7 77
25 7	OUT	SDCONN_STATE_CHANGE_RIO	7	8	HDMI_EG_DDC_DATA	BI	7 77
24 7	OUT	USB_EXTB_OC_L	9	10	HDMI_HPD_L	OUT	7 42 82
8		=PP1V5_S0_RIO	11	12			
8		=PP3V3_S3_RIO	13	14			
			15	16			
			17	18			
8		=PP3V3_S4_RIO	19	20			
44		=I2C_HDMIRDRV_SCL	21	22			
44		=I2C_HDMIRDRV_SDA	23	24			
			25	26			
			27	28			
8		=PP5V_S4_RIO	29	30			
			31	32			
				34			

SIGNAL_MODEL=EMPTY
BP4401 BEAD-PROBE SM
BP4402 BEAD-PROBE SM
SIGNAL_MODEL=EMPTY

91 19 IN USB3_EXTB_TX_P
91 19 IN USB3_EXTB_TX_N
91 19 7 OUT USB3_EXTB_RX_P
91 19 7 OUT USB3_EXTB_RX_N

C4402 0.1UF X5R-CERM 0201 10% 16V
GND_VOID=TRUE

C4401 0.1UF X5R-CERM 0201 10% 16V
GND_VOID=TRUE

12 R4403 1/20W 1% MF 201
GND_VOID=TRUE
15PF C4403 5% 25V NP0-CERM 0201
GND_VOID=TRUE

12 R4404 1/20W 1% MF 201
GND_VOID=TRUE
15PF C4404 5% 25V NP0-CERM 0201
GND_VOID=TRUE

SIGNAL_MODEL=EMPTY
BP4405 BEAD-PROBE SM
SIGNAL_MODEL=EMPTY
BP4406 BEAD-PROBE SM

SIGNAL_MODEL=EMPTY
BP4403 BEAD-PROBE SM
BP4404 BEAD-PROBE SM
SIGNAL_MODEL=EMPTY

J4400
20525-130E-01
F-RT-SM

			31				
91 26 7	BI	USB_EXTB_P	1				
91 26 7	BI	USB_EXTB_N	2				
			3				
97 7		USB3_EXTB_TX_C_P	4		GND_VOID=TRUE		
97 7		USB3_EXTB_TX_C_N	5		GND_VOID=TRUE		
			6				
97		USB3_EXTB_RX_RC_P	7		GND_VOID=TRUE		
97		USB3_EXTB_RX_RC_N	8		GND_VOID=TRUE		
			9				
95 77 7	IN	HDMI_EG_DATA_C_P<0>	10		GND_VOID=TRUE		
95 77 7	IN	HDMI_EG_DATA_C_N<0>	11		GND_VOID=TRUE		
			12				
95 77 7	IN	HDMI_EG_DATA_C_P<1>	13		GND_VOID=TRUE		
95 77 7	IN	HDMI_EG_DATA_C_N<1>	14		GND_VOID=TRUE		
			15				
95 77 7	IN	HDMI_EG_DATA_C_P<2>	16		GND_VOID=TRUE		
95 77 7	IN	HDMI_EG_DATA_C_N<2>	17		GND_VOID=TRUE		
			18				
95 77 7	IN	HDMI_EG_CLK_C_P	19				
95 77 7	IN	HDMI_EG_CLK_C_N	20				
			21				
92 17 7	IN	PCIE_CLK100M_ENET_P	22				
92 17 7	IN	PCIE_CLK100M_ENET_N	23				
			24				
92 17 7	OUT	PCIE_ENET_D2R_P	25		GND_VOID=TRUE		
92 17 7	OUT	PCIE_ENET_D2R_N	26		GND_VOID=TRUE		
			27				
92 17 7	IN	PCIE_ENET_R2D_C_P	28		GND_VOID=TRUE		
92 17 7	IN	PCIE_ENET_R2D_C_N	29		GND_VOID=TRUE		
			30				
			33				
			34				
			35				
			36				
			37				
			38				
			39				
			40				
			41				
			32				

518S0829

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

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RIO CONNECTOR

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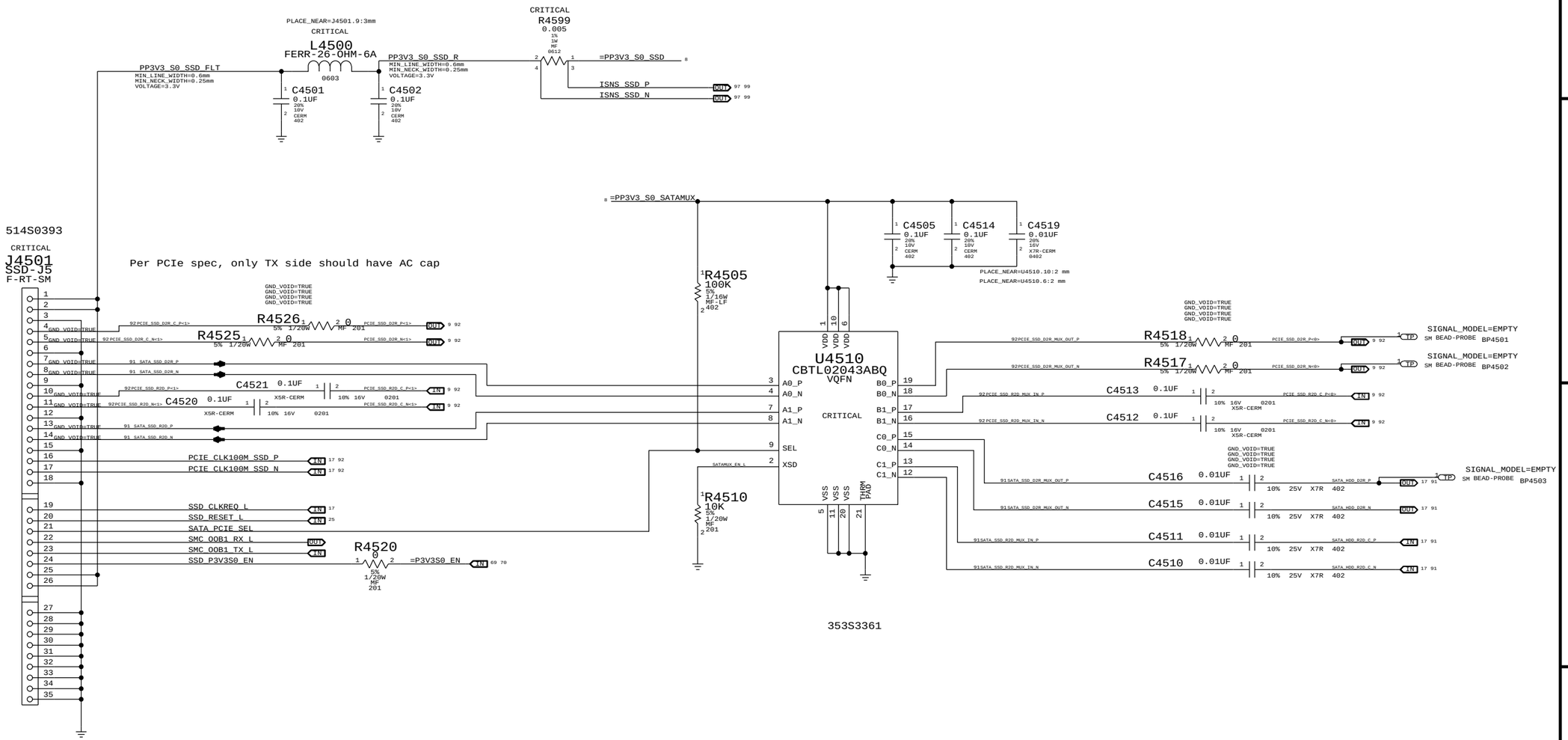

PCIE/SATA GUMSTICK2 CONNECTOR

SYNC_MASTER=D2_KEPLER	SYNC_DATE=01/13/2012
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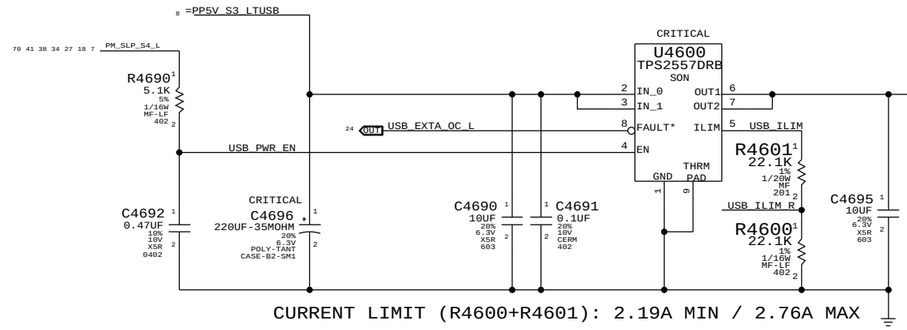
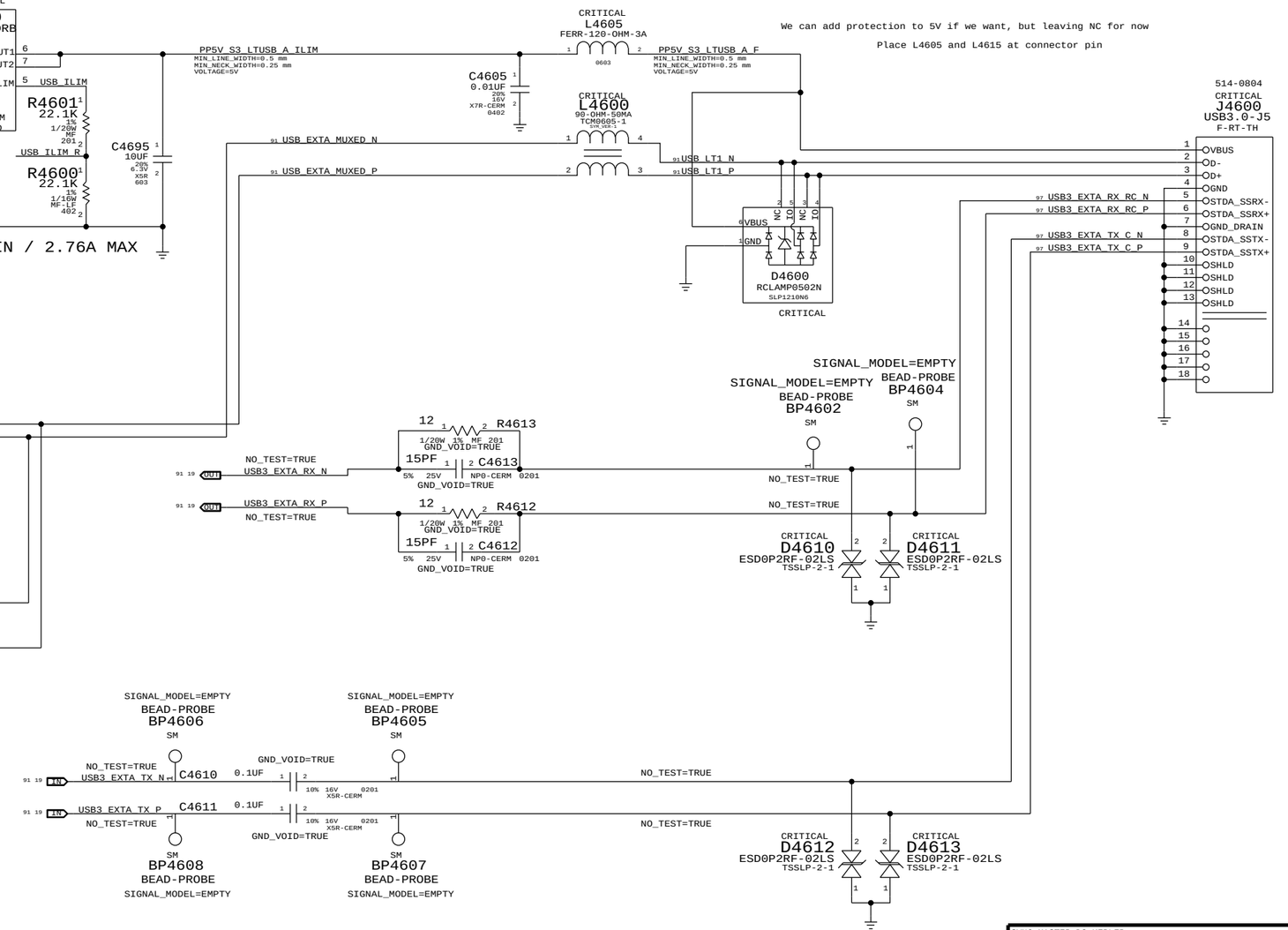
USB Port Power Switch

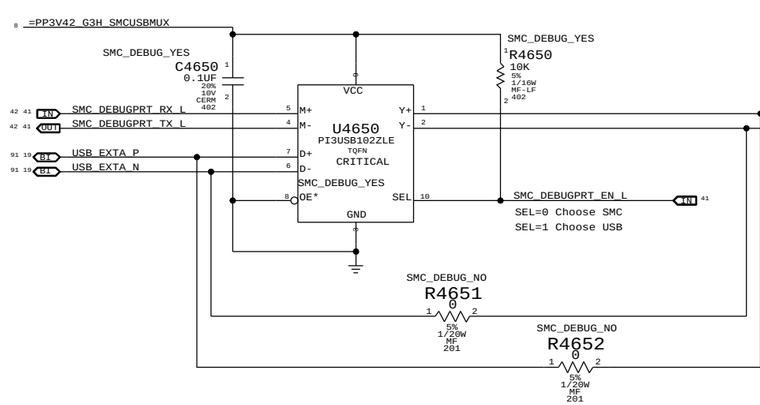


CURRENT LIMIT (R4600+R4601): 2.19A MIN / 2.76A MAX

Left USB Port A



USB/SMC Debug Mux



SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

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USB 3.0 CONNECTORS

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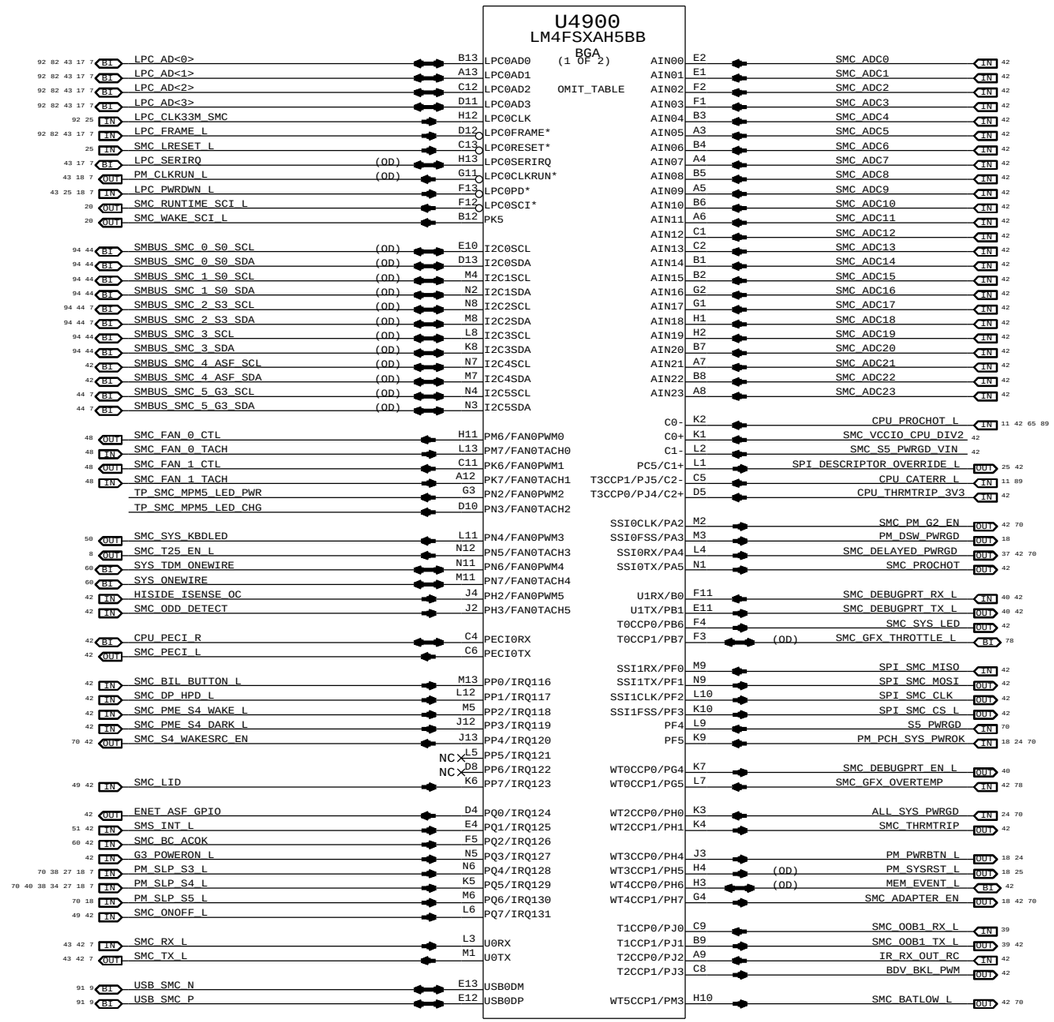
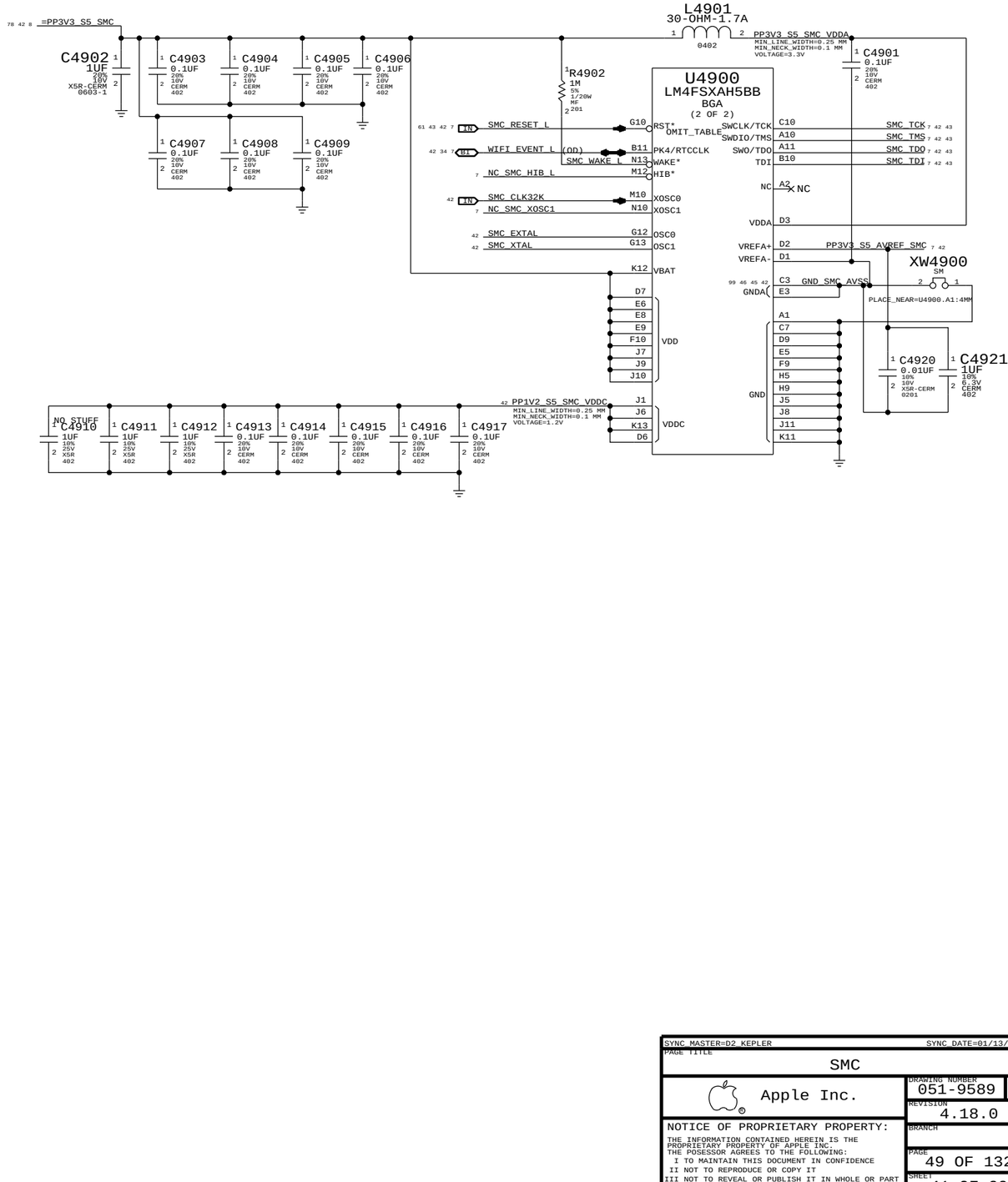
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.



NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.



SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012
PAGE TITLE: SMC
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SMC Reset "Button", Supervisor & AVREF Supply

=PP3V3_S5_SMC — R5027 47 5% 1/16W MF-LF 402 — PP3V42_G3H_SMC_SPVSR (MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.1 mm, VOLTAGE=3.42V)

C5027 4.7UF 20% 6.3V X5R 402

=PPVIN_S5_SMCVREF

Mac Mini: 5V
Mobiles: 3.42V

C5020 0.47UF 10% 6.3V CERM-X5R 402

U5010 VREF-3.3V-VDET-3.0V DFN SN0903048 (V+, VIN, MR1* (IPU), MR2* (IPU), DELAY, CRITICAL, REFOUT, GND, THRM PAD, RESET*)

R5000 100K 5% 1/16W MF-LF 402

R5028 0 5% 1/20W MF 201

SMC_RESET_R_L — SMC_RESET_L (OUT) 7 41 43 61

SMC_TPAD_RST_L (IN) 49
SMC_ONOFF_L (IN) 49 42 41
SMC_MANUAL_RST_L

PP3V3_S5_AVREF_SMC (MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.1 mm, VOLTAGE=3.3V) 7 41

OMIT R5001 0 5% 1/10W MF-LF 603 SILK_PART=SMC_RST

C5001 0.01UF 10% 16V X7R-CERM 0402

C5025 10UF 20% 6.3V X5R 603

C5026 0.01UF 10% 16V X7R-CERM 0402

NOSTUFF C5028 1000PF 5% 25V NP0-C0G 402

GND_SMC_AVSS (MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.1 mm, VOLTAGE=0V) 41 45 46 99

PLACEMENT_NOTE=Place R5001 on BOTTOM side

MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.

NOTE: Internal pull-ups are to VIN, not V+.

Debug Power "Buttons"

SMC_ONOFF_L (OUT) 41 42 49

OMIT R5016 0 5% 1/10W MF-LF 603 PLACE_SIDE=TOP — SILK_PART=PWR_BTN

OMIT R5015 0 5% 1/10W MF-LF 603 PLACE_SIDE=BOTTOM — SILK_PART=PWR_BTN

SMC Crystal Circuit

SMC_XTAL — R5010 2.49K 1% 1/20W MF 201 — SMC_XTAL_R

CRITICAL Y5010 3.2X2.5MM-SM-1 12.000MHZ-30PPM-10PF

SMC_EXTAL

C5010 12PF 5% 50V C0G-CERM 0402 — C5011 12PF 5% 50V C0G-CERM 0402

SMC USB CLOCK REQUIRE THESE CRYSTAL VALUES:5,6,8,10,12,16,18,20,24,25 MHZ

Hall Effect pads

APN: 998-3029
OMIT_TABLE
J5050
HALL-SENSOR-MLB-PADS-K99
SM

NC — NC — =PP3V42_S3_HALL — SMC_LID_R (7) — R5050 0 5% 1/16W MF-LF 402 — SMC_LID 41 42 49

C5050 0.001UF 10% 50V X7R-CERM 0402

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
607-6811	1	SUBASSY,PCBA HALL EFFECT,K99	J5050	CRITICAL	

41 PP1V2_S5_SMC_VDDC — SMC_PACKAGE:ENG R5099 0 5% 1/16W MF-LF 402 — 42 41 SMC_ADC23

ENG PACKAGE REQUIRES 1.2V ON SMC_ADC23 PIN

42 8 =PPVCCIO_S0_SMC — R5097 100K 1% 1/20W MF 201 — 41 SMC_VCCIO_CPU_DIV2 — R5096 100K 1% 1/20W MF 201

HDMI HPD ESD PROTECTION

Inversion now taking place on RIO

=PP3V3_S4_SMC 8 25 42 — R5059 100K 5% 1/20W MF 201

41 SMC_DP_HPD_L (OUT) — R5057 1K 5% 1/20W MF 201 — HDMI_HPD_L (IN) 7 38 82

1K for ESD protection

61 45 =CHGR_ACOK	SMC_BC_ACOK		41 42 60
41 HISIDE_ISENSE_OC	NC_HISIDE_ISENSE_OC		
41 SMC_ADC0	SMC_CPU_VSENSE		45
41 SMC_ADC1	SMC_CPU_ISENSE		46
41 SMC_ADC2	SMC_GPU_HI_ISENSE		46
41 SMC_ADC3	SMC_DCIN_VSENSE		45
41 SMC_ADC4	SMC_DCIN_ISENSE		46
41 SMC_ADC5	SMC_PBUS_VSENSE		45
41 SMC_ADC6	SMC_SSD_ISENSE		99
41 SMC_ADC7	SMC_CHGR_BMON_ISENSE		46
41 SMC_ADC8	SMC_CPU_HI_ISENSE		46
41 SMC_ADC9	SMC_OTHER_HI_ISENSE		46
41 SMC_ADC10	SMC_P1V5MEM_ISENSE		45
41 SMC_ADC11	SMC_CPUVCCIO_ISENSE		45
41 SMC_ADC12	SMC_GFX_VSENSE		45
41 SMC_ADC13	SMC_CPU_SA_ISENSE		45
41 SMC_ADC14	SMC_GPU_CORE_VSENSE		45
41 SMC_ADC15	SMC_GPU_CORE_ISENSE		45
41 SMC_ADC16	SMC_LCDBKLT_VSENSE		99
41 SMC_ADC17	SMC_LCDBKLT_ISENSE		99
41 SMC_ADC18	SMC_CPU_GFX_ISENSE		46
41 SMC_ADC19	SMC_GPU_P1V35_ISENSE		99
41 SMC_ADC20	SMC_CPU_SA_VSENSE		99
41 SMC_ADC21	SMC_PCH_CORE_ISENSE		99
41 SMC_ADC22	SMC_X29_ISENSE		99
42 41 SMC_ADC23	SMC_TBT_ISENSE_R		
41 SMBUS_SMC_4_ASF_SCL	NC_SMBUS_SMC_4_ASF_SCL		7
41 SMBUS_SMC_4_ASF_SDA	NC_SMBUS_SMC_4_ASF_SDA		7
41 BDV_BKL_PWM	NC_BDV_BKL_PWM		
42 41 SMC_PME_S4_DARK_L	SDCONN_STATE_CHANGE_SMC		25
	=TBT_WAKE_L		18 35

SMC_TBT_ISENSE — R5013 0 5% 1/16W MF-LF 402 — SMC_PACKAGE:PROD

R5012 22 5% 1/20W MF 201

18 PM_CLK32K_SUSCLK_R (IN) PLACE_NEAR=U1800.N14:5.1mm — SMC_CLK32K (OUT) 41

41 ENET_ASF_GPIO	NC_ENET_ASF_GPIO		
41 SMC_SYS_LED	NC_SMC_SYS_LED		7
41 MEM_EVENT_L	NC_MEM_EVENT_L		
41 SMC_ODD_DETECT	NC_SMC_ODD_DETECT		7
41 IR_RX_OUT_RC	NC_IR_RX_OUT_RC		

(MAKE_BASE=TRUE)

42 41 CPU_THRMTRIP_3V3 (OUT)

CRITICAL Q5058 MMBT3904LP-7 DFN1006-3 — PM_THRMTRIP_B_L — R5058 3.3K 5% 1/20W MF 201 — PM_THRMTRIP_L (IN) 11 20 89

BATLOW# ISOLATION

8 =PP3V3_S5_SMCBATLOW — R5040 100K 5% 1/20W MF 201 — 70 41 SMC_BATLOW_L (IN)

Q5040 SSM3K15FV SOD-VESM-HF — =PP3V3_SUS_SMC 8 — PM_BATLOW_L (OUT) 18

R5041 0 5% 1/10W MF-LF 402 NOSTUFF

Internal 20K pull-up on PM_BATLOW_L in PCH.

49 =PSOC_WAKE_L (IN)
34 =BT_WAKE_L (IN)

=PP3V3_S4_SMC 8 25 42 — R5082 100K 5% 1/20W MF 201 — SMC_PME_S4_WAKE_L (MAKE_BASE=TRUE) (OUT) 41

SMC12 PECI SUPPORT

=PPVCCIO_S0_SMC 8 42

CRITICAL Q5030 SSM3K15AMFVAPE VESM

41 SMC_PECI_L (IN) — R5032 0 5% 1/16W MF-LF 402 — SMC_PECI_L_R

From SMC

OMIT R5033 NOSTUFF NONE NONE NONE 402

R5031 330 5% 1/16W MF-LF 402

41 CPU_PECI_R (OUT) — R5034 43 5% 1/16W MF-LF 402 — CPU_PECI (BI) 11 20 89

To SMC — From/To CPU/PCH

89 65 41 11 CPU_PROCHOT_L (BI)

Q5059 SSM6N15FEAPE SOT563

ADC10 AND ADC11 ARE SHARED WITH COMPARATORS ON STACK BOARD

SMC_PROCHOT (IN) 41

20 PM_THRMTRIP_L_R (OUT)

Q5059 SSM6N15FEAPE SOT563

SMC_THRMTRIP (IN) 41 42

Q5057 SSM6N15FEAPE SOT563

SMC_GFX_OVERTEMP (IN) 41 78

SMC12 SPI SUPPORT

41 SPI_SMC_MISO (OUT)	R5021	12		SPI_MLB_MISO (IN)	43 52
41 SPI_SMC_MOSI (IN)	R5022	33	PLACE_NEAR=U6100.5:1MM	SPI_MLB_MOSI (OUT)	43 52
41 SPI_SMC_CLK (IN)	R5023	33	PLACE_NEAR=U6100.6:1MM	SPI_MLB_CLK (OUT)	43 52
41 SPI_SMC_CS_L (IN)	R5024	33	PLACE_NEAR=U6100.1:1MM	SPI_MLB_CS_L (OUT)	43 52

(5% 1/10W MF-LF 402)

78 42 41 8 =PP3V3_S5_SMC
42 25 8 =PP3V3_S4_SMC

NO STUFF

41 39 SMC_OOB1_TX_L	R5068	100K	
42 41 SMC_PME_S4_DARK_L	R5069	100K	
49 42 41 SMC_ONOFF_L	R5070	10K	
41 G3_POWERON_L	R5072	10K	
49 42 41 SMC_LID	R5071	100K	
43 41 7 SMC_TX_L	R5073	10K	
43 41 7 SMC_RX_L	R5074	100K	
41 40 SMC_DEBUGPRT_TX_L	R5075	10K	
41 40 SMC_DEBUGPRT_RX_L	R5076	100K	
43 41 7 SMC_TMS	R5077	10K	
43 41 7 SMC_TDO	R5078	10K	
43 41 7 SMC_TDI	R5079	10K	
43 41 7 SMC_TCK	R5080	10K	
41 SMC_BIL_BUTTON_L	R5081	10K	
60 42 41 SMC_BC_ACOK	R5087	470K	
41 SMC_S5_PWRGD_VIN	R5092	100K	
51 41 SMS_INT_L	R5093	10K	
42 41 CPU_THRMTRIP_3V3	R5094	100K	
41 25 SPI_DESCRIPTOR_OVERRIDE_L NOSTUFF	R5095	10K	

(5% 1/20W MF 201)

43 7 SMC_ROMBOOT — R5088 1K 5% 1/20W MF 201

42 41 SMC_THRMTRIP	R5086	10K	
70 41 37 SMC_DELAYED_PWRGD	R5091	100K	
70 41 SMC_PM_G2_EN	R5098	100K	
70 41 18 SMC_ADAPTER_EN	R5085	10K	
70 41 SMC_S4_WAKESRC_EN	R5090	100K	

(5% 1/20W MF 201)

41 34 7 WIFI_EVENT_L — R5089 10K 5% 1/20W MF 201 — 34 7 PP3V3_WLAN

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

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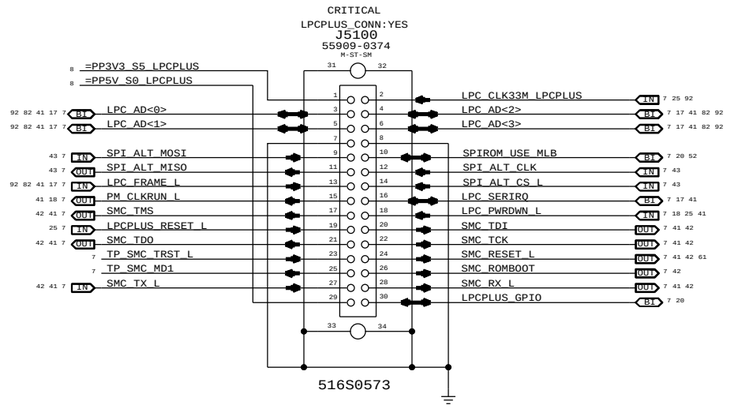
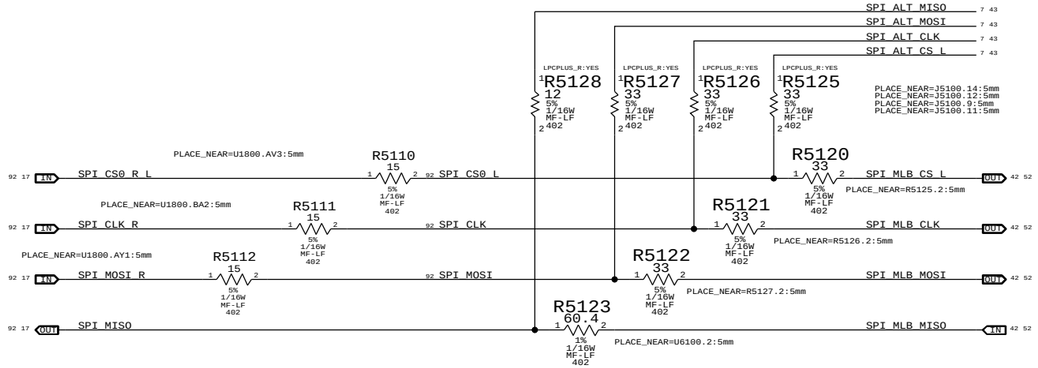
LPC+SPI Connector



SPI Bus Series Termination



SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE

LPC+SPI Debug Connector

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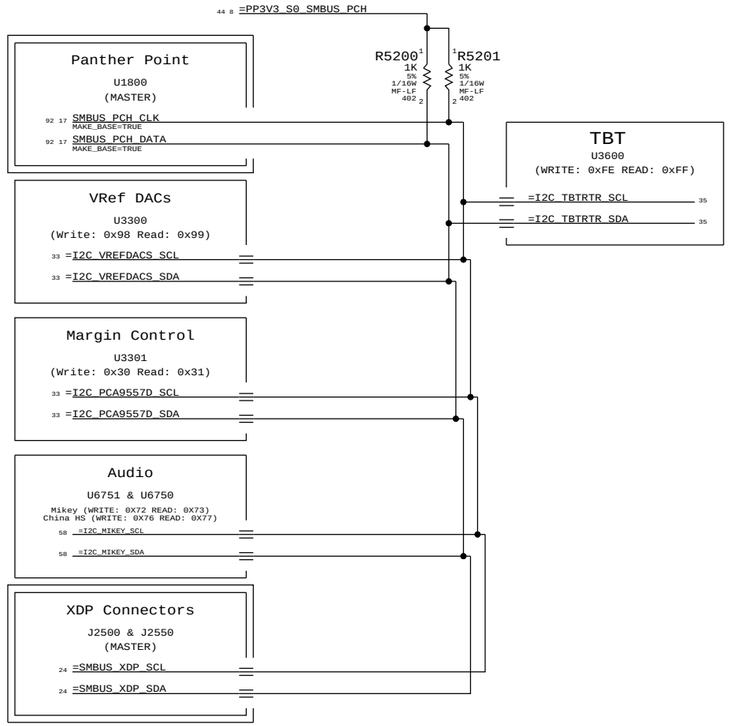
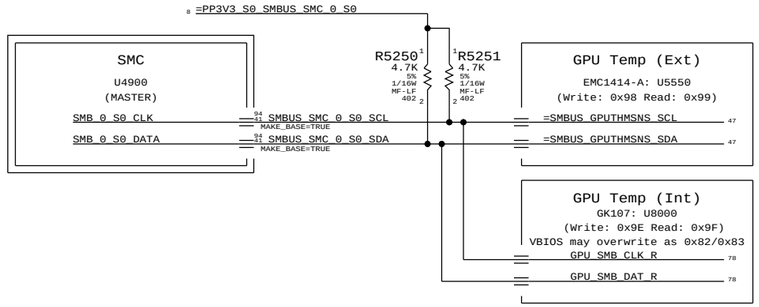
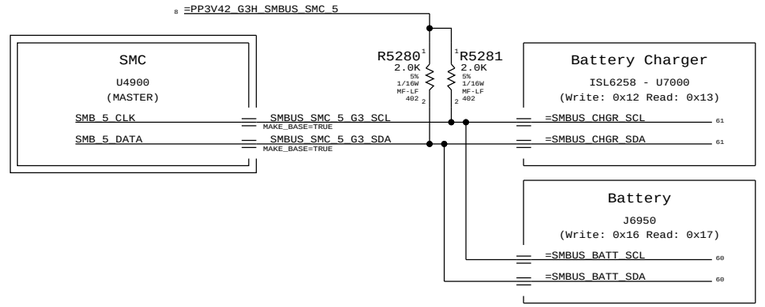
PCH SMBus "0" Connections



SMC "0" SMBus Connections

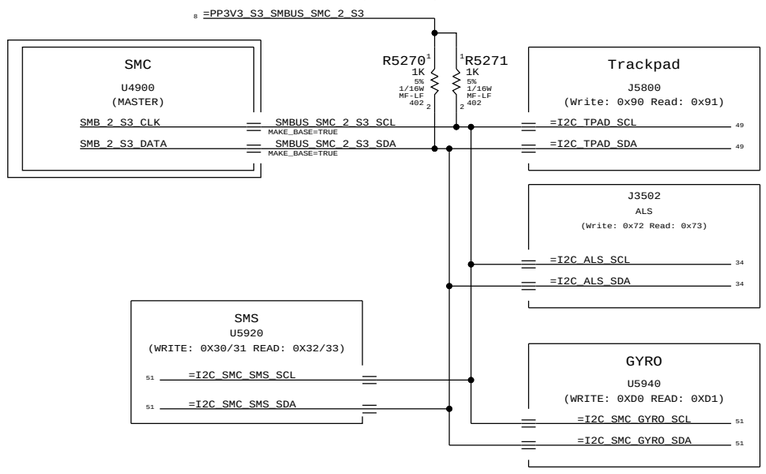


SMC "5" SMBUS CONNECTIONS

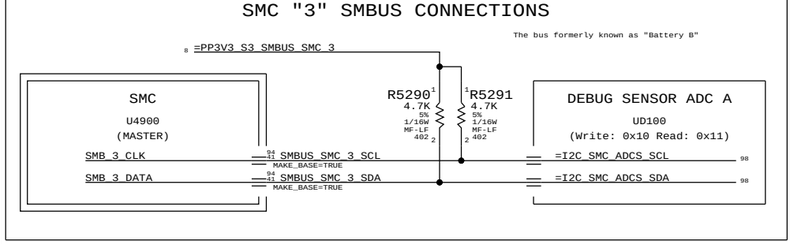


SMC "2" SMBUS CONNECTIONS

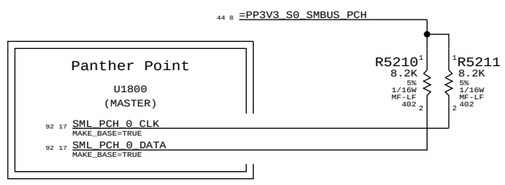
NOTE: SMC RMT bus remains powered and may be active in S3 state



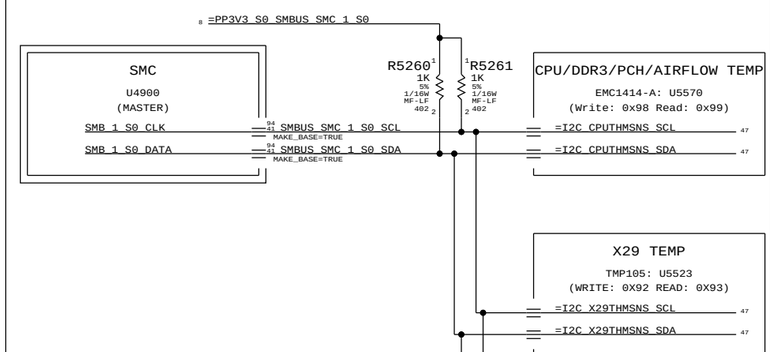
SMC "3" SMBUS CONNECTIONS



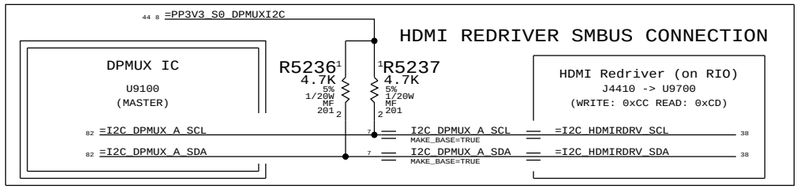
PCH "SMLink 0" Connections



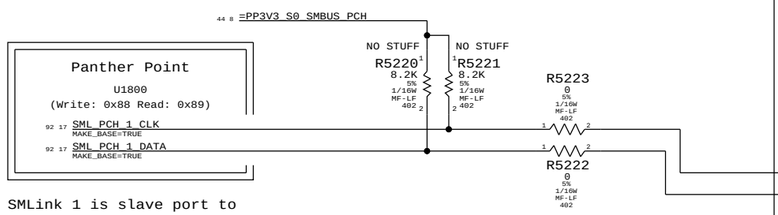
SMC "1" SMBUS CONNECTIONS



HDMI REDRIVER SMBUS CONNECTION

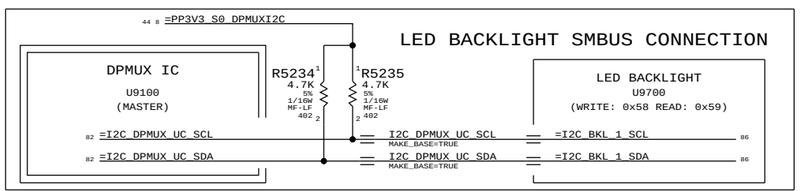


PCH "SMLink 1" Connections



SMLink 1 is slave port to access PCH & CPU via PECI.

LED BACKLIGHT SMBUS CONNECTION



SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

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SMBus Connections

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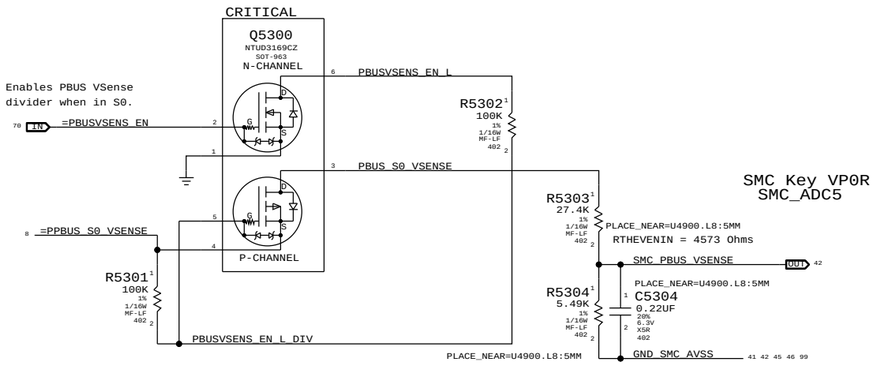
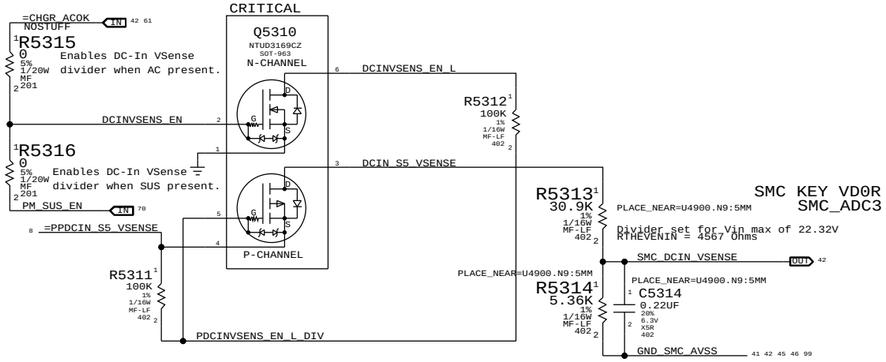
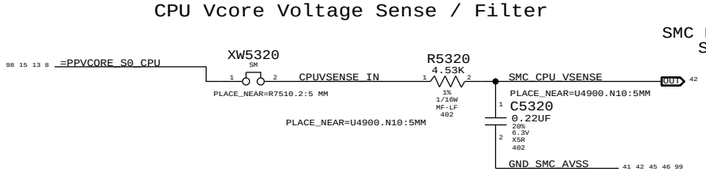
PBUS Voltage Sense Enable & Filter



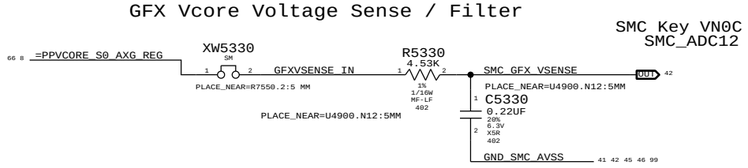
DC-In Voltage Sense Enable & Filter



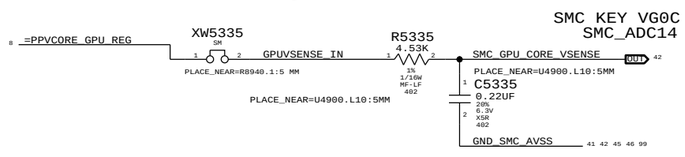
CPU Vcore Voltage Sense / Filter



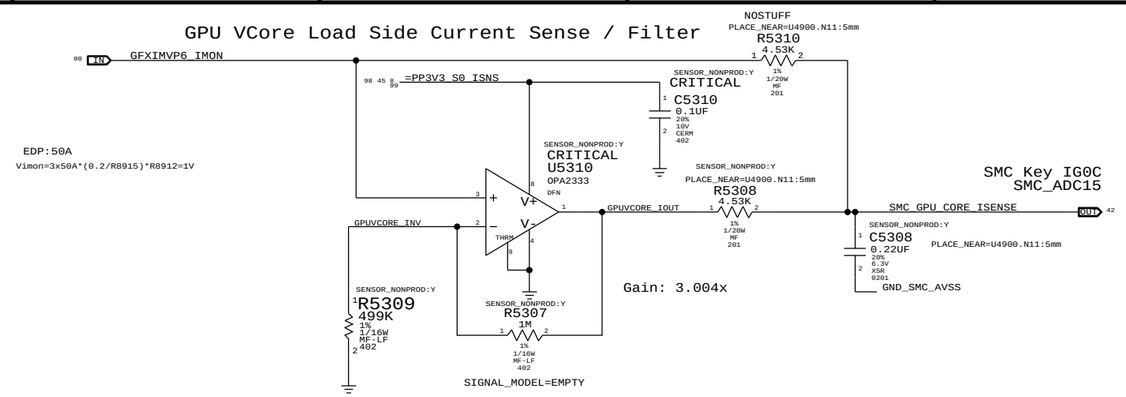
GFX Vcore Voltage Sense / Filter



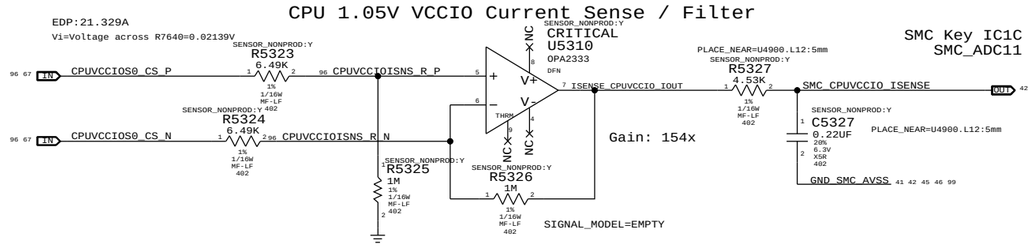
GPU Vcore Voltage Sense / Filter



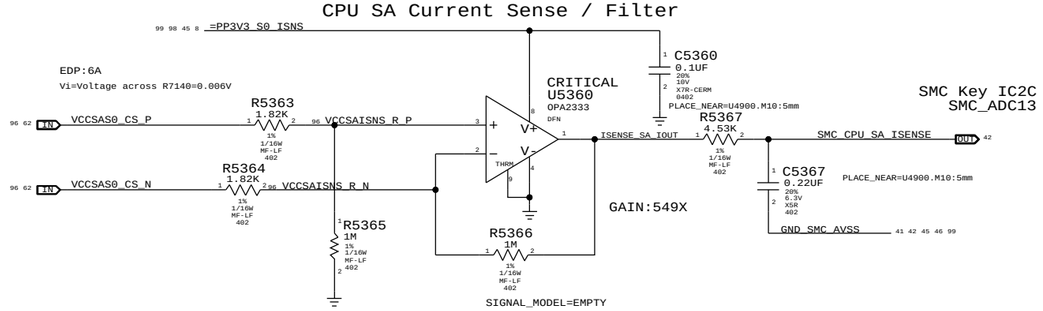
GPU VCore Load Side Current Sense / Filter



CPU 1.05V VCCIO Current Sense / Filter

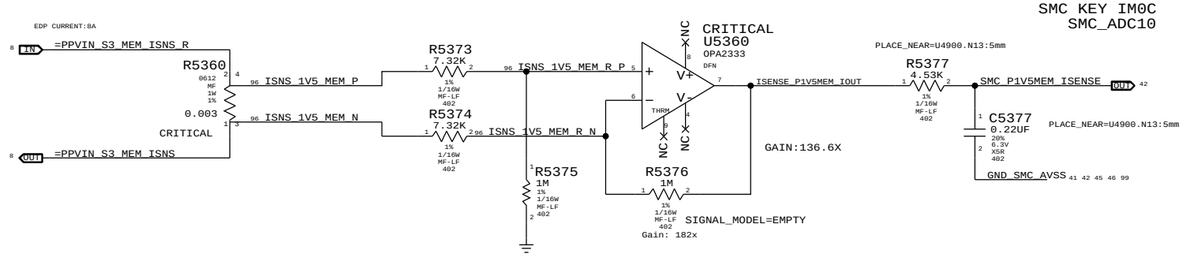


CPU SA Current Sense / Filter



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0114	1	RES,MTL FILM,100K,5,1/16W,0402,SMD,LF	C5327		SENSOR_NONPROD:N
1175O008	1	RES,MF,1/20W,100R OHM,5,0201,SMD	C5308		SENSOR_NONPROD:N

DDR3 1.5V DRAM ONLY CURRENT SENSE / FILTER



SYNC_MASTER=D2_SEAN SYNC_DATE=03/05/2012

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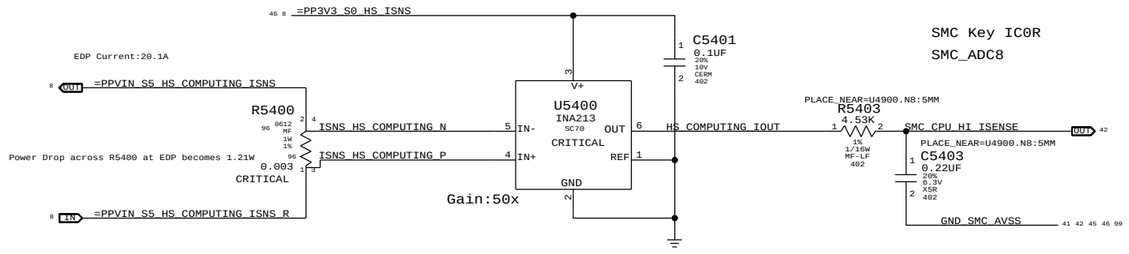
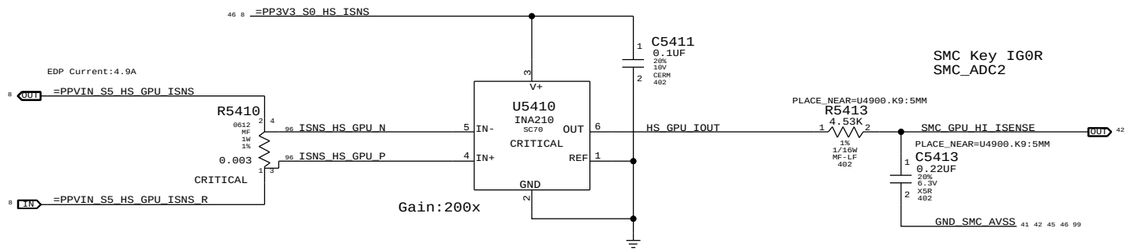
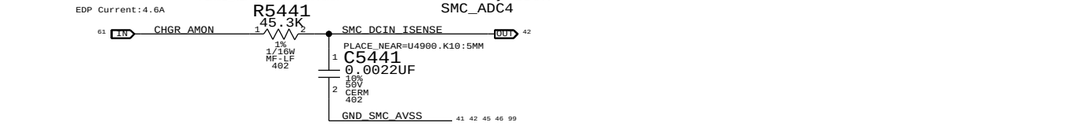
COMPUTING High Side Current Sense / Filter



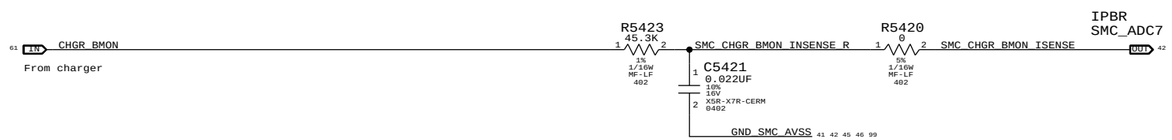
GRAPHICS High Side Current Sense / Filter



OTHER High Side Current Sense / Filter

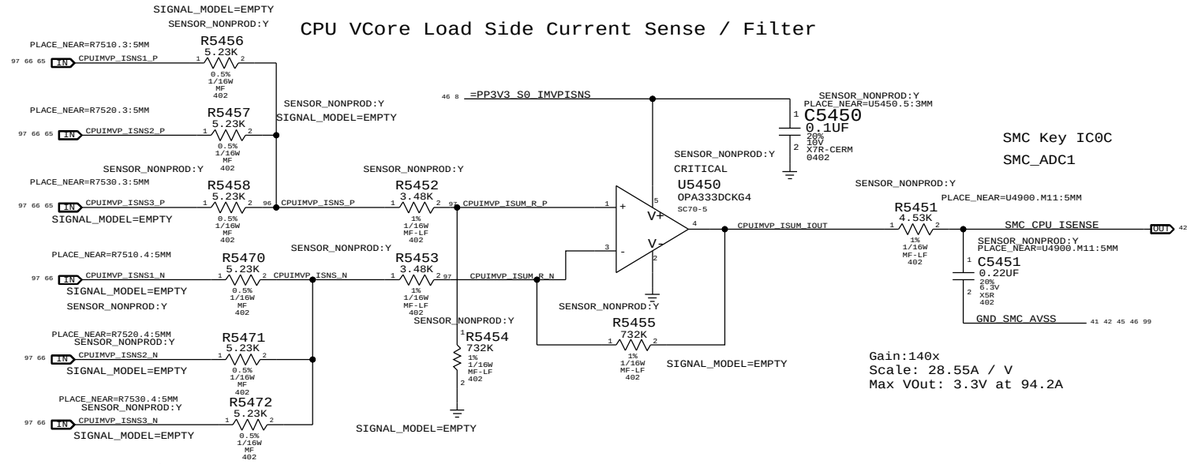


CHARGER BMON HIGH SIDE (BATTERY DISCHARGE) CURRENT SENSE & FILTER

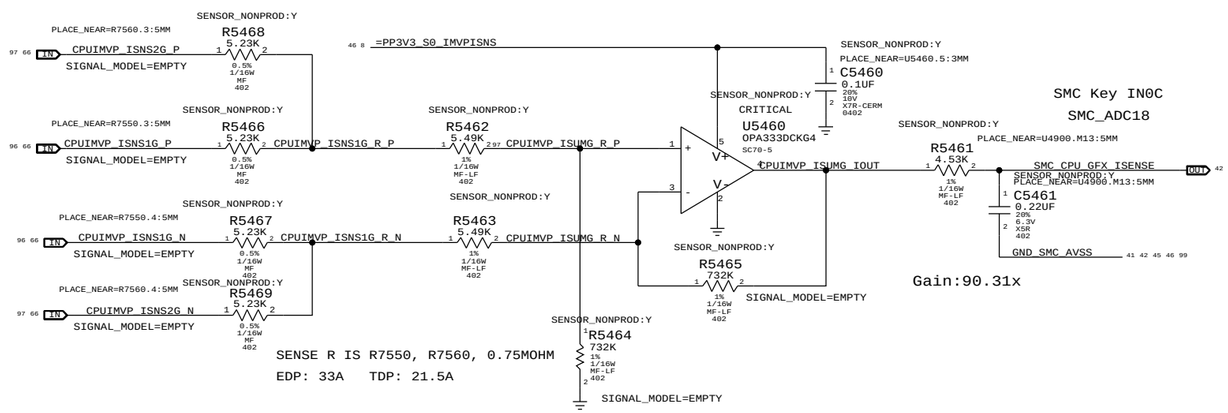


DC-IN (AMON) Current Sense Filter

CPU VCore Load Side Current Sense / Filter



GFX/IG VCore Load Side Current Sense / Filter



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0114	2	RES,MTL FILM,100K,5,1/16W,0402,SMD,LF	C5451,C5461		SENSOR_NONPROD:N

SYNC_MASTER=D2_SEAN SYNC_DATE=03/05/2012

PAGE TITLE: High Side and CPU/AXG Current Sensing

Apple Inc.

DRAWING NUMBER: 051-9589 SIZE: D

REVISION: 4.18.0

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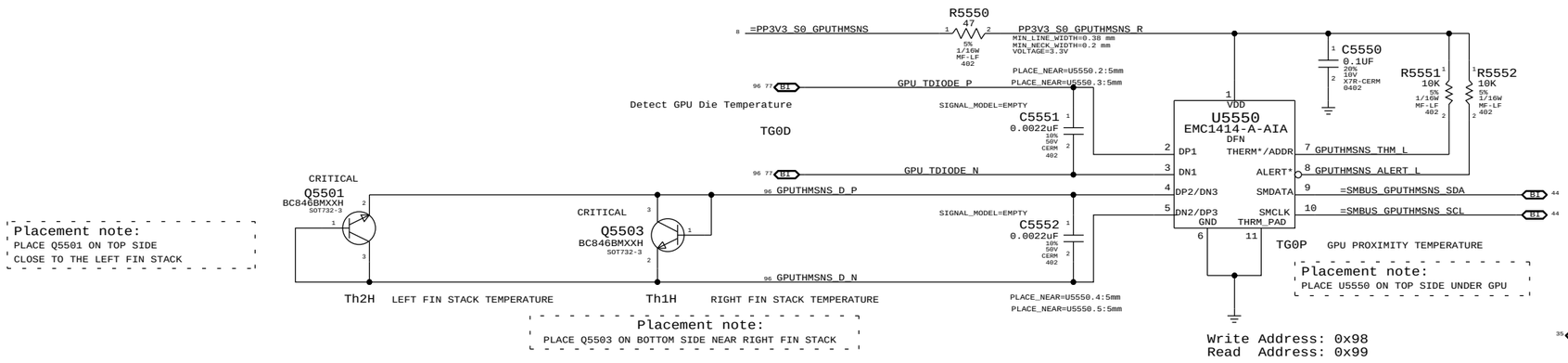
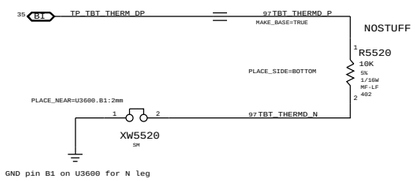
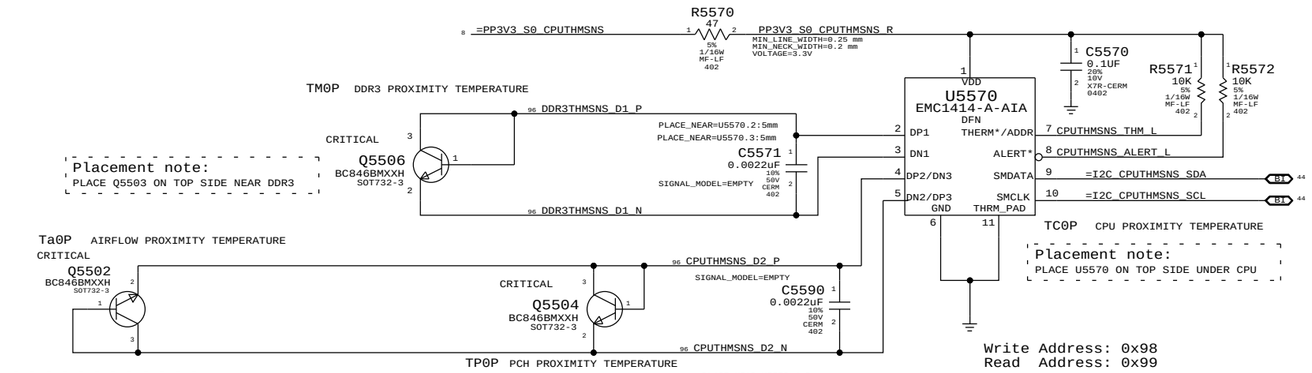
GPU PROXIMITY/GPU DIE/LEFT FIN STACK/RIGHT FIN STACK



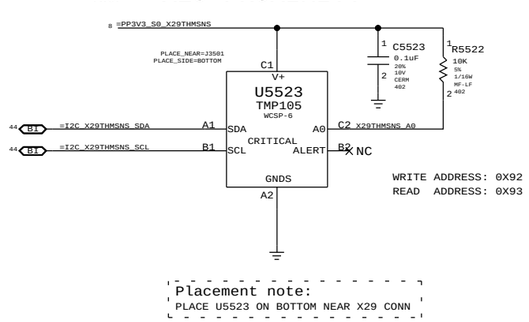
TBT DIE



DDR3 PROXIMITY/CPU PROXIMITY/PCH PROXIMITY/AIRFLOW PROXIMITY



X29 PROXIMITY



SYNC_MASTER=D2_SEAN SYNC_DATE=03/05/2012

PAGE TITLE: Thermal Sensors

Apple Inc.

DRAWING NUMBER: 051-9589 SIZE: D

REVISION: 4.18.0

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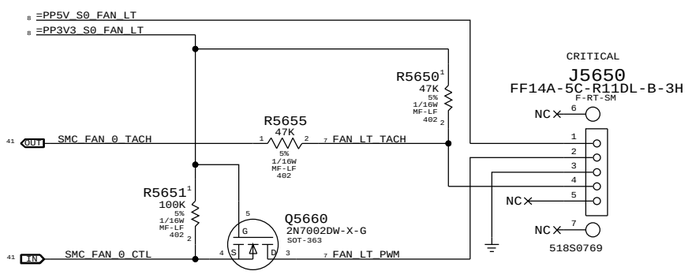
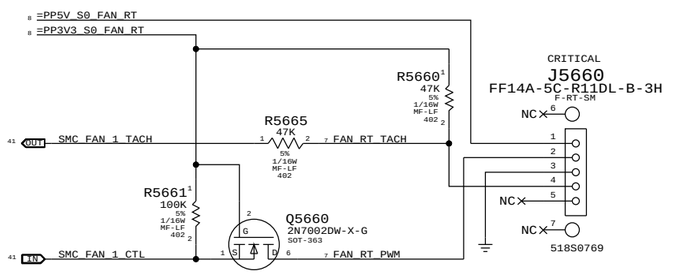
Left Fan



Right Fan



SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE

Fan Connectors

Apple Inc.

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PSOC USB CONTROLLER

- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER

PLACE_SIDE=BOTTOM

=PP3V3_S4_TPAD → R5704 0 5% 1/16W MF-LF 402 → PP3V3_S3_PSOC (MIN_LINE_WIDTH=0.50MM, MIN_NECK_WIDTH=0.20MM, VOLTAGE=3.3V)

BYPASS=U5701.49:50:5 mm

BYPASS=U5701.49:50:8 mm

BYPASS=U5701.49:50:11 mm

R5703 220K 5% 1/20W MF 201

C5704 100PF 5% 50V C0G-CERM 0201

C5705 0.1UF 10% 6.3V X5R 201

C5706 4.7UF 20% 6.3V X5R 402

U5701 CRITICAL OMIT
CY8C24794 MLF (SYM-VER2)
337S2983

=PSOC_WAKE_L	OUT		
PICKB_L			
BUTTON_DISABLE			
Z2_HOST_INTN			
WS_LEFT_SHIFT_KEY			
WS_LEFT_OPTION_KEY			
WS_CONTROL_KEY	P2_3	P2_2	WS_KBD17
Z2_KEY_ACT_L	P2_1	P2_0	WS_KBD16N
	NC P4_7	P4_6	WS_KBD15_C
TPAD_VBUS_EN	IN P4_5	P4_4	WS_KBD14
	NC P4_3	P4_2	WS_KBD13
	NC P4_1	P4_0	WS_KBD12
PSOC_MISO	P3_7	P3_6	WS_KBD11
PSOC_F_CS_L	P3_5	P3_4	WS_KBD10
PSOC_MOSI	P3_3	P3_2	WS_KBD9
PSOC_SCLK	P3_1	P3_0	WS_KBD8
Z2_MISO	P5_7	P5_6	WS_KBD7
Z2_CS_L	P5_5	P5_4	WS_KBD1
Z2_MOSI	P5_3	P5_2	WS_KBD2
Z2_SCLK	P5_1	P5_0	WS_KBD3
		THRML PAD	WS_KBD4
			WS_KBD5
TP_PSOC_SCL			WS_KBD6
TP_PSOC_SDA			
TP_PSOC_P1_3			
TP_ISSP_SCLK_P1_1		TP_ISSP_SDATA_P1_0	
ISSP SCLK/I2C SCL		ISSP SDATA/I2C SDA	
			Z2_CLKIN
			TP_P7_7

R5701 24 5% 1/20W MF 201 — USB_TPAD_P → USB_TPAD_R_P

R5702 24 5% 1/20W MF 201 — USB_TPAD_N → USB_TPAD_R_N

(PP3V3_S3_PSOC)

C5702 100PF 5% 50V C0G-CERM 0201

C5703 0.1UF 10% 6.3V X5R 201

C5701 4.7UF 20% 6.3V X5R 402

BYPASS=U5701.22:19:5 mm

BYPASS=U5701.22:19:8 mm

BYPASS=U5701.22:19:11 mm

IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
		80UA		0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA (MAX)	10 OHM	0.6 V	36E-3 W
	VOUT	60MA (MAX)	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
		14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

IPD Flex Connector

CRITICAL
J5700 516S0689
55560-0228 M-ST-SM

=PP3V3_S4_TPAD → R5708 0 5% 1/20W MF 201 → PP3V3_TPAD_CONN (VOLTAGE=3.3V, MIN_NECK_WIDTH=0.20MM, MIN_LINE_WIDTH=0.50MM)

NOSTUFF C5708 0.1UF 10% 6.3V X5R 201

Z2_CS_L		Z2_KEY_ACT_L
Z2_MOSI	NC	PSOC_F_CS_L
Z2_MISO		PICKB_L
Z2_SCLK		PSOC_MISO
	NC	PSOC_MOSI
Z2_HOST_INTN		PSOC_SCLK
		=I2C_TPAD_SDA
Z2_CLKIN		=I2C_TPAD_SCL
		NC

TPAD_5V_SW_S4 L5700 FERR-120-OHM-1.5A 0402-LF
=PP5V_S4_TPAD → PP5V_S4_CUMULUS (VOLTAGE=5V, MIN_NECK_WIDTH=0.20MM, MIN_LINE_WIDTH=0.50MM)
C5700 0.1UF 10% 10V X5R-CERM 0201 — TPAD_5V_SW_S4, PLACE_NEAR=J5800.18:3MM

TPAD_5V_LDO L5707 FERR-120-OHM-1.5A 0402-LF
PP5V_S5RS4_CUMULUS
C5707 0.1UF 10% 10V X5R-CERM 0201 — TPAD_5V_LDO, PLACE_NEAR=J5800.18:3MM

R5700 220K 5% 1/20W MF 201

SMC Manual Reset & Isolation

Left shift, option & control keys combined with power button cause SMC RESET# assertion.
Keys ANDed with PSoC power to isolate when PSoC is not powered.
No IPD on OE input pin PP3V3_S4 (symbol error).

=PP3V42_G3H_TPAD → C5750 0.1UF 10% 16V X7R-CERM 0402

U5750 SLG4AP021 TQFN

=PP3V3_S4_TPAD	OE (IPD)		
WS_LEFT_SHIFT_KBD	IN_1 (IPD)	OUT_1	WS_LEFT_SHIFT_KEY
WS_LEFT_OPTION_KBD	IN_2 (IPD)	OUT_2	WS_LEFT_OPTION_KEY
WS_CONTROL_KBD	IN_3 (IPD)	OUT_3	WS_CONTROL_KEY
		OUT_ALL#	SMC_TPAD_RST_L → OUT

Pull-up in U5010.

GND, THRM PAD

Keyboard Connector

=PP3V3_S4_TPAD, =PP3V42_G3H_TPAD

	32	
WS_KBD1	30	
WS_KBD2	29	
WS_KBD3	28	
WS_KBD4	27	
WS_KBD5	26	
WS_KBD6	25	
WS_KBD7	24	
WS_KBD8	23	
WS_KBD9	22	
WS_KBD10	21	
WS_KBD11	20	
WS_KBD12	19	
WS_KBD13	18	
WS_KBD14	17	
WS_KBD15_CAP	16	
WS_KBD16_NUM	15	
WS_KBD17	14	
WS_KBD18	13	
WS_KBD19	12	
WS_KBD20	11	
WS_KBD21	10	
WS_KBD22	9	
WS_KBD23	8	
WS_KBD_ONOFF_L	7	
WS_LEFT_SHIFT_KBD	6	
WS_LEFT_OPTION_KBD	5	
WS_CONTROL_KBD	4	
	3	
	2	
	1	
	31	

F-RT-SM
FF14A-30C-R11DL-B-3H
J5713 CRITICAL 518S0752

WS_KBD15_C → CAPS:INT R5714 56.2 1% 1/16W MF-LF 402

WS_KBD16N → R5715 10K 1% 1/16W MF-LF 402

SMC_ONOFF_L → R5710 1K 5% 1/16W MF-LF 402

C5710 0.1UF 20% 10V CERM 402

WS_KBD15_C	CAP_COMP_H	CAP_COMP_L	Q5736	Q5738	LED Current
Z	1	1	off	off	none
1	0	1	on	off	source
0	1	0	off	on	sink

All RC values are TBD

5V TRACKPAD S4 FET

TPAD_5V_NO_FET R5720 0 5% 1/16W MF-LF 402

TPAD_5V_FET CRITICAL Q5720 SIA413DJ SC70-6L

5V TPAD FET	
MOSFET	SiA413
CHANNEL	P-TYPE 12V
RDS(ON)	29 mOhm @4.5V
LOADING	16 mA (EDP)

=PP5V_S5_TPAD

TPAD_5V_FET Q5721 SSM3K15FV SOD-VESM-HF

TPAD_5V_FET R5721 220K 5% 1/20W MF 201

TPAD_5V_FET C5722 0.033UF 10% 16V X5R 402

TPAD_5V_FET R5722 3.3K 5% 1/20W MF 201

TPAD_5V_FET C5723 0.01UF 10% 16V X5R 201

=P5VS4_TPAD_EN (IN) — P5VCUMULUS_EN_L — P5VCUMULUS_SS — PP5V_S5RS4_CUMULUS (VOLTAGE=5V, MIN_NECK_WIDTH=0.20MM, MIN_LINE_WIDTH=0.50MM)

Caps Lock LED Drive

=PP3V3_S4_TPAD

WS_KBD15_C

CAPS:EXT R5730 10K 5% 1/20W MF 201 — CAP_VREF_L
CAPS:EXT R5732 10K 5% 1/20W MF 201
CAPS:EXT R5734 20K 5% 1/20W MF 201

CAPS:EXT R5731 10K 5% 1/20W MF 201 — CAP_VREF_H
CAPS:EXT R5733 20K 5% 1/20W MF 201
CAPS:EXT R5735 10K 5% 1/20W MF 201

CAPS:EXT U5730 LM393ADGKR MSOP (V+, GND) → CAP_COMP_H

CAPS:EXT R5740 10K 5% 1/20W MF 201
CAPS:EXT R5738 10K 5% 1/20W MF 201
CAPS:EXT R5736 10K 5% 1/20W MF 201

CAPS:EXT Q5736 NTZD3152P SOT-563-HF

CAP_SOURCE
CAPS:EXT R5737 113 1% 1/20W MF 201 — MIN_LINE_WIDTH=0.2MM, MIN_NECK_WIDTH=0.1MM
WS_KBD15_CAP
CAPS:EXT R5739 113 1% 1/20W MF 201 — MIN_LINE_WIDTH=0.2MM, MIN_NECK_WIDTH=0.1MM
CAP_SINK

CAPS:EXT Q5738 DMN3730UFB4 DFN1006H4-3

CAP_COMP_L_INV

CAPS:EXT CRITICAL Q5734 SSM3K15AMFVAPE VESM

CAP_COMP_L

TPAD Buttons Disable

BUTTON_DISABLE → Q5701 SSM6N15FEAPE SOT563 → SMC_LID (IN)

PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V

BOM Options available to CSA 5

TPAD_5V:SW_S4	Original implementation off PP5V_S4
TPAD_5V:LDO_S4	PP5V_S5 LDO power in S4 only
TPAD_5V:LDO_S5	PP5V_S5 LDO power

BOM GROUP	BOM OPTIONS
TPAD_5V:SW_S4	TPAD_5V_SW_S4
TPAD_5V:LDO_S4	TPAD_5V_FET,TPAD_5V_LDO
TPAD_5V:LDO_S5	TPAD_5V_NO_FET,TPAD_5V_LDO

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012
PAGE TITLE: KEYBOARD/TRACKPAD (1 OF 2)

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=PP3V3_S0_TPAD
R5853 470K 5% 1/10W MF-LF 402
SMC_SYS_KBDLED
R5854 4.7K 5% 1/10W MF-LF 402
SMC_KBDLED_PRESENT_L

J5815 PIN 4 IS GROUNDED
ON KEYBOARD BACKLIGHT FLEX
CRITICAL

J5815
AA07A-S010-VA1
F-ST-SM

KBDLED_ANODE2
KBDLED_ANODE1
XNC

516S0899

Keyboard Backlight Connector

Keyboard Backlight Driver & Detection

To detect Keyboard backlight, SMC will
tristate and read SMC_SYS_KBDLED:

If LOW, keyboard backlight present
If HIGH, keyboard backlight not present

R5853 always stuffed, R5854 only
grounded when KB BL flex connected.

SMC_SYS_KBDLED
=PP5V_S0_KBDLED
SMC_SYS_KBDLED_FILTER
SMC_SYS_KBDLED_R
SMC_SYS_KBDLED_ANALOG

R5856 0 5% 1/16W MF-LF 402
R5857 10K 5% 1/10W MF-LF 402 NOSTUFF
R5858 120K 5% 1/10W MF-LF 402 NOSTUFF
R5859 100K 5% 1/16W MF-LF 402 NOSTUFF
R5866 0 5% 1/16W MF-LF 402 NOSTUFF

C5859 10UF 20% 10V X5R 0603 NOSTUFF

CRITICAL
L5850
15UH-20%-740MA-0.420HM
VLF403212MT-SM
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.25 MM
SWITCH_NODE=TRUE
KBDLED_SW1

C5850 1UF 10% 10V X5R 402-1

353S3472
DNBT_TABLE
U5850 LT3591 DFN
CTRL VIN LED SW SW CAP CAP GND PAD

KBDLED_ANODE1
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=35V
R5855 10 1% 1/16W MF-LF 402
KBDLED_CAP1
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.2 MM

KBD_BL:SANDWICH CRITICAL C5855 1.0UF 10% 50V X5R 0603
KBD_BL:SANDWICH CRITICAL C5856 1.0UF 10% 50V X5R 0603
KBD_BL:TBONE CRITICAL C5857 1.0UF 10% 50V X7R 0805
KBD_BL:TBONE CRITICAL C5858 1.0UF 10% 50V X7R 0805

CRITICAL
L5860
15UH-20%-740MA-0.420HM
VLF403212MT-SM
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.25 MM
SWITCH_NODE=TRUE
KBDLED_SW2

C5860 1UF 10% 10V X5R 402-1

353S3472
DNBT_TABLE
U5860 LT3591 DFN
CTRL VIN LED SW SW CAP CAP GND PAD

KBDLED_ANODE2
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=35V
R5865 10 1% 1/16W MF-LF 402
KBDLED_CAP2
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.2 MM

KBD_BL:SANDWICH CRITICAL C5865 1.0UF 10% 50V X5R 0603
KBD_BL:SANDWICH CRITICAL C5866 1.0UF 10% 50V X5R 0603
KBD_BL:TBONE CRITICAL C5867 1.0UF 10% 50V X7R 0805
KBD_BL:TBONE CRITICAL C5868 1.0UF 10% 50V X7R 0805

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S1612	2	IC,DC/DC CVTR,BOOST,WHITE LED,1MHZ,DFN8	U5850,U5860	CRITICAL	

SYNC_MASTER=D2_KEPLER
SYNC_DATE=01/13/2012

PAGE TITLE
KEYBOARD/TRACKPAD (2 OF 2)

Apple Inc.

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8 =PP3V3_S3_SMS

BYPASS=U5920.14:13:8 mm

SMS C5926 10UF 20% 6.3V XSR 603

SMS C5922 0.1UF 10% 6.3V X5R 201

BYPASS=U5920.14:13:8 mm

SMS R5924 10K 5% 1/20W MF 201

SMS R5920 10K 5% 1/20W MF 201

NOSTUFF R5925 10K 5% 1/20W MF 201

U5920 LIS331DLH LGA

NC NC NC RESERVED CRITICAL

VDD VDD_IO CS SDO SDA/SDI/SDO SCL/SPC INT1 INT2 GND

SMS_I2C_SEL

SMS_ADDR_SELECT

I2C_SMC_SMS_SDA_R

I2C_SMC_SMS_SCL_R

42 41 OUT SMS_INT_L

TP_SMS_INT2

338S0687

PLACEMENT_NOTE=See schematic for orientation.

SMS R5923 0 5% 1/20W MF 201 =I2C_SMC_SMS_SDA BI 44

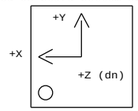
SMS R5922 0 5% 1/20W MF 201 =I2C_SMC_SMS_SCL IN 44

SMS R5921 10K 5% 1/20W MF 201

SMS_ADDR_SELECT=0 Addr: 0x30(Wr)/0x31(Rd)
SMS_ADDR_SELECT=1 Addr: 0x32(Wr)/0x33(Rd)

NOTE: SDA and SCL have internal pull-ups to VDD_IO.

Desired orientation when placed on board bottom-side (view thru top):



Front of system

Circle indicates pin 1 location when placed in correct orientation

8 =PP3V3_S3_GYRO

GYRO C5940 0.1UF 10% 6.3V X5R 201

GYRO C5941 0.1UF 10% 6.3V X5R 201

GYRO C5943 10UF 20% 6.3V CERM-X5R 0402-1

GYRO

(WRITE: 0XD0 READ: 0XD1)

GYRO R5944 10K 5% 1/20W MF 201

CS PU = I2C

338S0927 = 8KHZ

INT ARE PUSH-PULL

GYRO R5946 0 5% 1/20W MF 201 =I2C_SMC_GYRO_SCL IN 44

GYRO R5947 0 5% 1/20W MF 201 =I2C_SMC_GYRO_SDA BI 44

GYRO_CS

TP_IRQ_GYRO_INT2_L

TP_GYRO_SYNC

TP_IRQ_GYRO_INT1_L

U5940 AP3GDL8B LGA

RES/VDDIO VDD VDD_IO CS DRDY/INT2 DEN INT1 PLLFILT SCL_SPC SDA_SDI_SDO SDO_SA0 RES0 RES1 RES2 RES3 GND

I2C_SMC_GYRO_SCL_R

I2C_SMC_GYRO_SDA_R

PLLFILT_GYRO

PLLFILT_GYRO1

GYRO C5942 0.47UF 10% 6.3V CERM-X5R 402

GYRO R5945 10K 5% 1/20W MF 201

GYRO C5945 0.01UF 10% 16V X5R-CERM 0201

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE: DIGITAL ACCELEROMETER & GYRO

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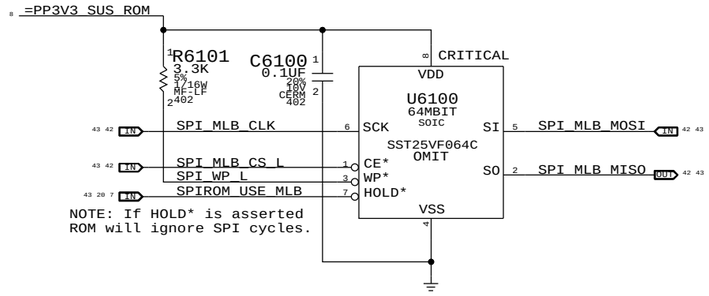

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

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SPI ROM

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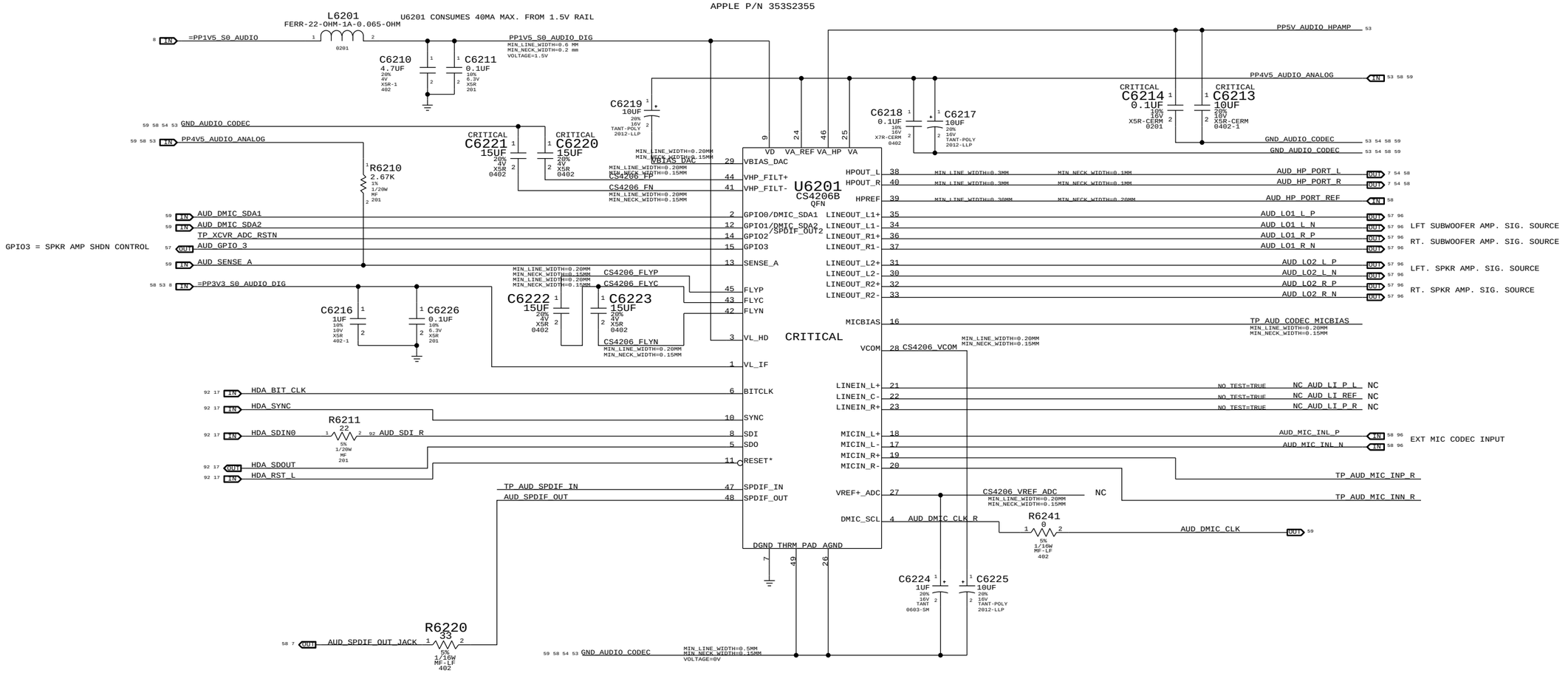
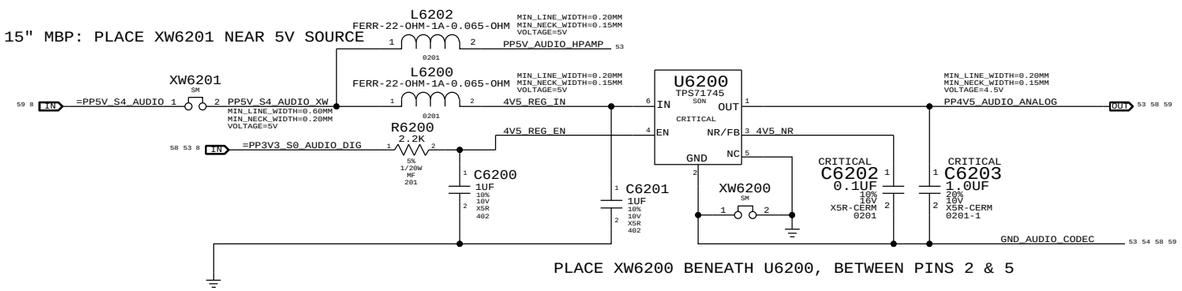
AUDIO CODEC

APPLE P/N 353S2355



4.5V POWER SUPPLY FOR CODEC

APPLE P/N 353S2456



NOTES ON CODEC I/O

DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

SYNC_MASTER=D2_CARA SYNC_DATE=03/16/2012

PAGE TITLE

AUDIO: CODEC/REGULATOR

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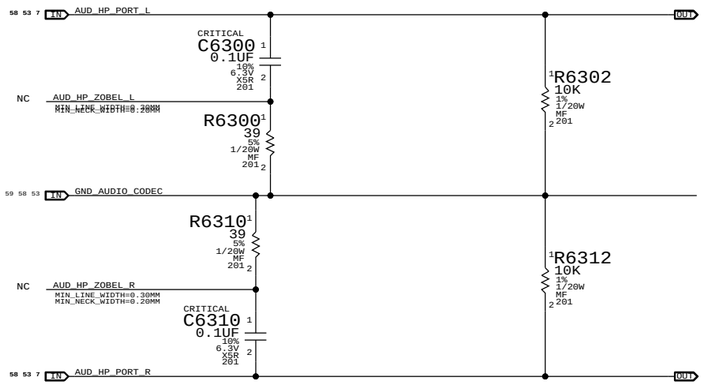
ZOBEL NETWORK & 1ST ORDER DAC FILTER PLACEHOLDER



SYNC_MASTER=D2_CARA SYNC_DATE=03/16/2012

PAGE TITLE

AUDIO: HEADPHONE FILTER

Apple Inc.

DRAWING NUMBER 051-9589 SIZE D

REVISION 4.18.0

BRANCH

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SYNC_MASTER=D2_CARA	SYNC_DATE=03/16/2012
PAGE TITLE: AUDIO: IV SENSE	
Apple Inc.	DRAWING NUMBER: 051-9589 / SIZE: D
	REVISION: 4.18.0
	BRANCH:
	PAGE: 64 OF 132
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8 7 6 5 4 3 2 1

D C B A

SYNC_MASTER=D2_CARA SYNC_DATE=03/16/2012

PAGE TITLE

AUDIO: IV SENSE FILTER

Apple Inc.

DRAWING NUMBER 051-9589 SIZE D

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BRANCH

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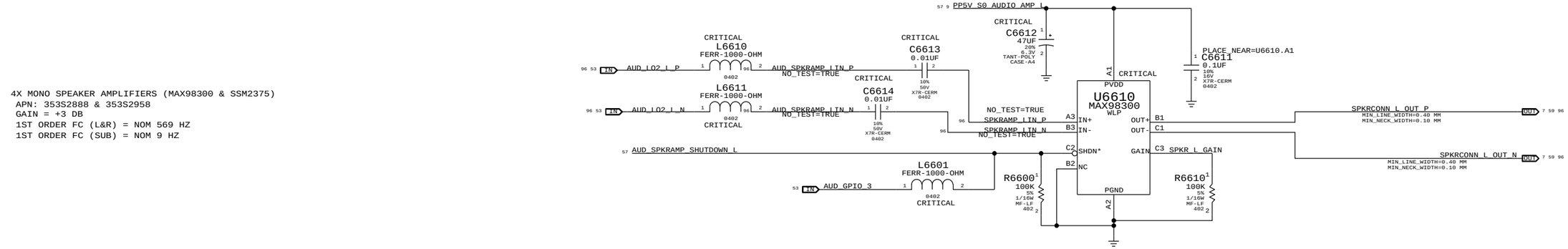
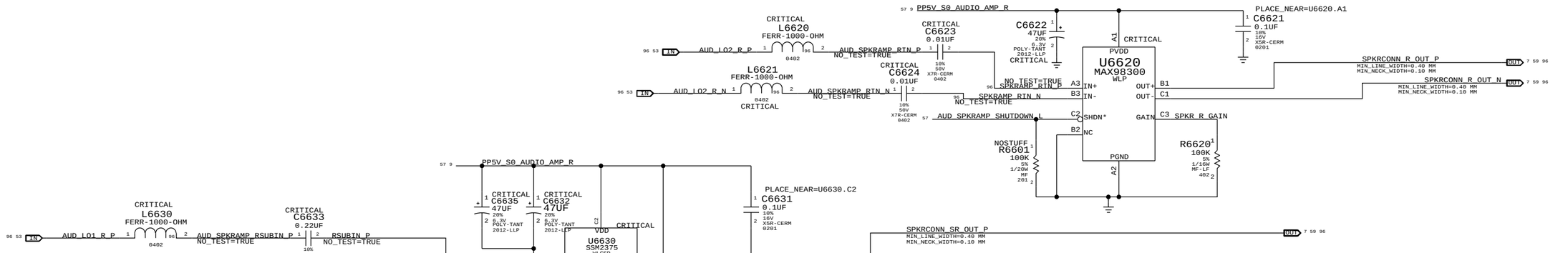
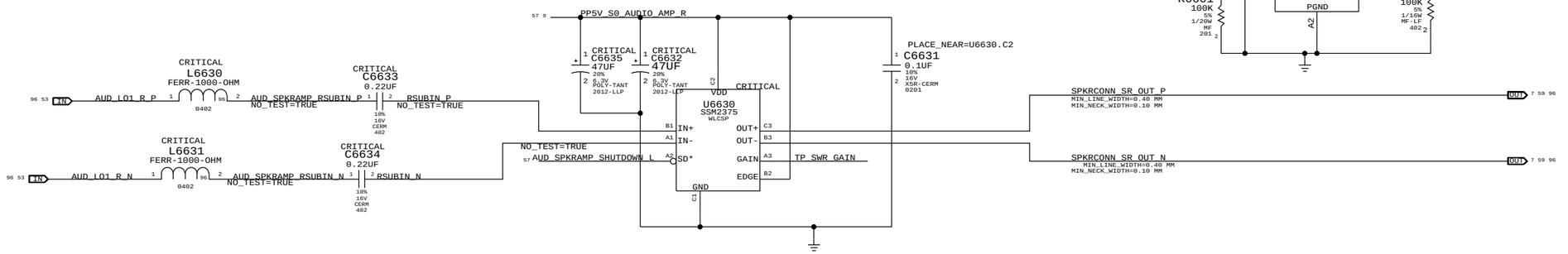
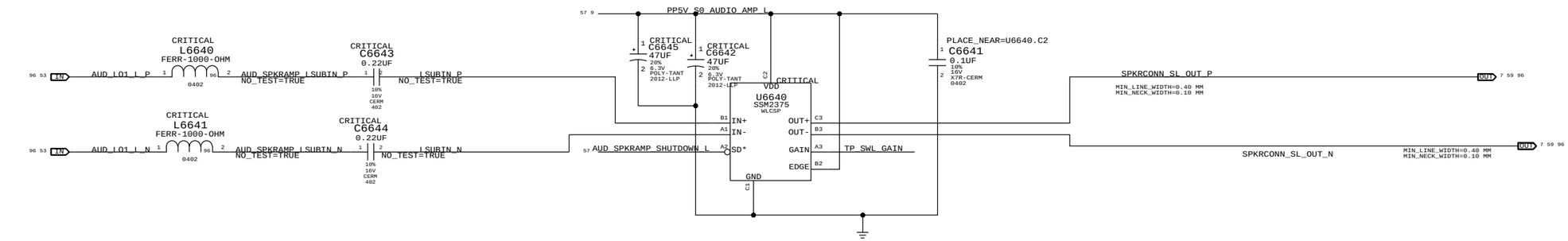
4X MONO SPEAKER AMPLIFIERS (MAX98300 & SSM2375)
APN: 353S2888 & 353S2958
GAIN = +3 DB
1ST ORDER FC (L&R) = NOM 569 HZ
1ST ORDER FC (SUB) = NOM 9 HZ









SYNC MASTER=D2_CARA
SYNC DATE=03/16/2012

PAGE TITLE
AUDIO: SPEAKER AMP

Apple Inc.

DRAWING NUMBER 051-9589
SIZE D
REVISION 4.18.0
BRANCH
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AUDIO JACK: HP CONNECTOR WITH MIKEY & CHS

PORT B LEFT(HEADSET MIC)
HP=80HZ, LP=10.63KHZ

MIKEY 1A
APN:353S2640
MIKEY ADDRESS: WRITE=72H, READ=73H

I2C PULLUPS ON SOUTHBRIDGE PAGE

PP4V5_AUDIO_ANALOG
=PP3V3_S0_AUDIO_DIG
R6762 10K 5% 1/20W MF 201
C6795 1.0UF 20% 10V X5R-CERM 0201-1
C6794 1.0UF 20% 10V X5R-CERM 0201-1
C6755 1.0UF 20% 10V X5R-CERM 0201-1
R6757 33 5% 1/20W MF 201
=I2C_MIKEY_SCL
R6758 33 5% 1/20W MF 201
=I2C_MIKEY_SDA
AUD_I2C_INT_L
AUD_IPHS_SWITCH_EN
NOSTUFF R6761 47K 5% 1/20W MF 201
HS_HDET
NO_TEST=TRUE
AUD_PORTA_DET_L
R6755 100K 5% 1/20W MF 201
GND_AUDIO_CODEC

U6751 CD3282A1 WCSP
AVDD
SCL C3
SDA B3
INT* D3
ENABLE A3
HDET A1
CS B2
MICBIAS C1
DETECT B1
BYPASS D1
DGND C2
AGND D2
AUDIO_SCL
AUDIO_SDA

L6754 FERR-22-OHM-1A-0.065-OHM 0201
=PP3V42_G3H_AUDIO
MIN_LINE_WIDTH=0.20MM
MIN_NECK_WIDTH=0.15MM
VOLTAGE=3.42V
PP3V42_G3H_AUDIO_LC
C6793 1.0UF 20% 10V X5R-CERM 0201-1
C6792 1.0UF 20% 10V X5R-CERM 0201-1
C6790 1.0UF 20% 10V X5R-CERM 0201-1
C6754 0.1UF 10% 16V X5R-CERM 0201
PLACE_NEAR=U6750.A1
GND_AUDIO_CODEC

HS_MIC_BIAS
HS_SW_DET
HS_RX_BP
NO_TEST=TRUE
MIKEY R6754 1K 5% 1/20W MF 201
C6756 0.01UF 10% 16V X5R-CERM 0201

U6750 TS3A8235YFP WCSP CRITICAL
VDD
RAMPI D4
RAMPO D3
CLAMPI C4
CLAMPO B4
MIC D2
REF D1
SCL A3
SDA A4
ADDR A2
GND1 C2
GND2 B2
GND B3
VDD C3
MIC1 B1
MIC2 C1
CHS_CLAMPI
CHS_CLAMPO
HS_MIC_HI
HS_MIC_LO
AUDIO_SCL
AUDIO_SDA
US_HS_GND
CH_HS_GND

R6751 1K 5% 1/20W MF 201
R6752 2.2K 1% 1/20W MF 201
R6753 2.2K 1% 1/20W MF 201
C6751 10UF 20% 10V X5R-CERM 0402-1
C6791 10UF 20% 10V X5R-CERM 0402-1
XW6751 SM
AUD_HP_PORT_REF
PLACE_NEAR=U6750.D1

MIKEY CRITICAL C6752 0.1UF 10% 6.3V X5R 201
MIKEY CRITICAL C6753 0.1UF 10% 6.3V X5R 201
AUD_MIC_INL_P
AUD_MIC_INL_N
HS_MIC_HI_RC
HS_MIC_LO_RC
MIKEY R6756 100K 5% 1/20W MF 201
MIKEY CRITICAL C6750 6800PF 10% 10V X5R-X7R-CERM 0201
MIKEY R6750 2.2K 1% 1/20W MF 201
MIKEY R6759 0 5% 1/20W MF 201
MIKEY CRITICAL C6758 27PF 5% 25V NP0-C0G 0201
R/C6750_FILTER_TO_ADDRESS_OUT-OF-BAND NOISE_ISSUE SEEN ON EARLY HEADSETS (SEE_RADAR_# 6210118)

R6760 47K 5% 1/20W MF 201
NOSTUFF
GND_AUDIO_CODEC

CRITICAL L6701 FERR-33-OHM-0.8A-0.09-OHM 0201
US_HS_MIC
AUD_CONN_MIC
CRITICAL L6700 120-OHM-25%-1.3A 0402
US_HS_GND
AUD_CONN_SLEEVE_XW
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.06MM
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
CRITICAL L6702 120-OHM-25%-1.3A 0402
CH_HS_GND
AUD_CONN_MIC_XW
CRITICAL L6703 FERR-33-OHM-0.8A-0.09-OHM 0201
CH_HS_MIC
AUD_CONN_SLEEVE
CRITICAL L6704 120-OHM-25%-1.3A 0402
AUD_HP_PORT_L
AUD_CONN_HP_LEFT
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.1MM
AUD_CONN_TIPDET_INV
=PP3V3_S0_AUDIO_DIG
AUD_SPDIF_OUT_JACK

APN:510S0009
CRITICAL J6701 51138-0274 F-ST-SM
22 21 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 23 24

CRITICAL L6705 120-OHM-25%-1.3A 0402
AUD_HP_PORT_R
AUD_CONN_HP_RIGHT
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.1MM
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.1MM
CRITICAL L6706 FERR-470-OHM 0201
AUD_TYPEDET
AUD_CONN_TYPEDET

I2C ADDRESSES

MIKEY	U6751	READ	0111 0011	0X73
MIKEY	U6751	WRITE	0111 0010	0X72
CHS	U6750	READ	0111 0111	0X77
CHS	U6750	WRITE	0111 0110	0X76

SYNC_MASTER=D2_CARA SYNC_DATE=03/16/2012

PAGE TITLE: AUDIO: JACK

Apple Inc.

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CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X02 (2)	0X02 (2)	0X09 (9,A)	N/A	0X09 (B)
TWEETERS	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_3	N/A
SUB	0X03 (3)	0X03 (03)	0X0A (10)	GPIO_3	N/A
SPDIF OUT	N/A	0X08 (8)	0X10 (16)	N/A	0X0C (A)

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
DMIC 1	0X06 (6)	0X0E (D,E)	3V3	N/A
DMIC2	0X05 (5)	0X12 (12,C)	3V3	0X0C (12,C)
SPDIF IN	0X07 (7)	0X0F (15)	N/A	N/A
HEADSET MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	MIKEY	MIKEY

SYSTEM INT AND GPIO LINES

FUNCTION	INT	GPIO
MIKEY ENABLE		SATA4GP/GPIO 16
MIKEY INTERRUPT	PIRQ H	GPIO 5
PERIPHERAL DETECT	PIRQ F	GPIO 3

3-MIC CONNECTOR

SPEAKER CONNECTOR HP=80HZ

APN: 518S0627

PORT B DETECT(SPDIF DELEGATE) PORT A DETECT (HEADPHONES)

PORT C DETECT(SPEAKER MISMATCH)

EXTRACTION NOTIFICATION

APN:376S0613

NOM R6892-C6860 FC = 106Hz
SSM6N15FE Vth = 0.8V to 1.5V
SSM6N15FE IGSS = +/-1uA
FLEX-SIDE RPULLDOWN = 100k (TB 49.9k in REV 3)

AUDIO CONNECTOR DETECT STATES

	NOTHING	SPDIF	HEADPHONE
AUD_J1_TYPEDET_R	1	1	0
AUD_J1_TIPDET_R	0	1	1
AUD_OUTJACK_INSERT_L	1	0	0
AUD_SENSE_A	1	20K/2.67K RDIV	39.2K/2.67K RDIV

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S3452	353S1286		U6800	MAXIM ALT TO MICROCHIP

SYNC MASTER=D2_CARA SYNC_DATE=03/16/2012

PAGE TITLE: AUDIO: JACK TRANSLATORS

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MagSafe DC Power Jack

CRITICAL
F6905
6AMP-32V-0.0095OHM
0603

=PP18V5_DCIN_CONN

CRITICAL
J6900
WTB-PWR-M82
M-RT-SM
518S0508

PP18V5_DCIN_FUSE
MIN_LINE_WIDTH=1MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=18.5V

C6905 0.01UF 20% 50V CERM 0603

TDM_ONEWIRE_MPM

=PP3V42_G3H_ONEWIREPROT

C6908 0.1UF 20% 10V CERM 402
PLACEMENT_NOTE=PLACE NEAR U6900 and U6901

CRITICAL
U6901
TC7SZ08FEAPE
SOT665

SMC_BC_ACOK_VCC

C6900 0.1UF 20% 10V CERM 402

R6929 2.0K 5% 1/16W MF-LF 402

SMC_BC_ACOK

ADAPTER_SENSE

U6900
MAX9940
SC70-5
CRITICAL
EXT
INT
VCC
NC GND
NC

SYS_ONEWIRE

1-Wire OverVoltage Protection

The chassis ground will otherwise float and can send transients onto ADAPTER_SENSE when AC is connected.

TDM LEVEL SHIFT

=PP3V42_G3H_TDM

TDM:MPM R6977 22 5% 1/20W MF 201

TDM:MLB R6975 2.21K 1% 1/20W MF 201

TDM:MLB R6976 22 5% 1/20W MF 201

SYS_TDM_ONEWIRE

TDM_ONEWIRE_MLB

R6912 22.1K 1% 1/20W MF 201

Input impedance of 22.1K meets sparkitecture requirements for 15" MBP design only

TDM:MLB
U6970
SLG4AP030
TDFN
CRITICAL
IN_A
IN_B1
IN_B2
OUT_C
OUT_D1
OUT_D2
VDD
GND
THRM PAD

TDM_PD_BASE_R

TDM:MLB CRITICAL D6970 DDZ9694T SOD523

TDM_RX_D

TDM_RX

TDM:MLB R6973 24.9K 1% 1/20W MF 201

TDM:MLB R6974 6.34K 1% 1/20W MF 201

TDM:MLB R6972 54.9 1% 1/20W MF 201

TDM_PD_BASE

TDM:MLB CRITICAL Q6970 ZXTN619MA DFN

TDM:MLB CRITICAL Q6971 MMBT2222AM3T5G SOT723

TDM_PD_DS

TDM:MLB R6971 12.1 1% 1/8W MF-LF 805

TDM:MLB R6970 12.1 1% 1/8W MF-LF 805

LAYOUT NOTE:
Q0220 NEEDS 10 SQ CM
OF 1 OZ CU FOR THERMAL

Q6910
SI5419DU
POWERPAK

R6910 100K 5% 1/20W MF 201

C6912 0.047UF 10% 25V X5R 0402

R6911 10K 5% 1/20W MF 201

DCIN_ISOL_GATE_R

DCIN_ISOL_GATE

When input voltage is 2V the FET will be off blocking the leakage path and 22.1K can be properly detected.

When input voltage is at 16V+, FET will conduct and power charger and 3.42V reg

=PP18V5_DCIN_ISOL

D6910
GDZT2R6.8
GDZ-0201
6.8V Zener

R6920 47 1% 1/3W MF 805

PP18V5_DCIN_CONN_R
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=18.5V

CRITICAL
D6905
BAT30CWFILM
SOT-323

R6905 10 5% 1/8W MF-LF 805

=PPBUS_G3H

PPBUS_G3H_R
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=18.5V

PPVIN_G3H_P3V42G3H
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=18.5V

BATTERY CONNECTOR

518-0376
CRITICAL
J6950
BAT-J5
F-ST-TH

POS 1
POS 2
POS 3
POS 4
SCL 5
SDA 6
SYS_DETECT 7
NEG 8
NEG 9
NEG 10
NEG 11

NC
NC

PPVBAT_G3H_CONN

=SMBUS_BATT_SCL

=SMBUS_BATT_SDA

SYS_DETECT_L

C6950 0.1UF 10% 25V X5R 402

C6960 1UF 10% 25V X5R 603-1

CRITICAL
D6950
RCLAMP2402B
SC-75

R6950 10K 5% 1/16W MF-LF 402

C6990 4.7UF 10% 25V X5R-CERM 0603

C6991 4.7UF 10% 25V X5R-CERM 0603

NOSTUFF
C6992 4.7UF 10% 25V X5R-CERM 0603

C6993 4.7UF 10% 25V X5R-CERM 0603

NOSTUFF
C6996 4.7UF 10% 25V X5R-CERM 0603

NOSTUFF
C6997 4.7UF 10% 25V X5R-CERM 0603

3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator

U6990
LT3470AED
DFN
VIN
BOOST
SHDN*
NC
SW
BIAS
FB
GND PAD
THRM PAD
CRITICAL

P3V42G3H_BOOST
DIDT=TRUE

C6994 0.22UF 10% 10V CERM 402

CRITICAL
L6995
33UH-20%-0.39A-0.435OHM
DP418C-SM

P3V42G3H_SW
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_NODE=TRUE
DIDT=TRUE

P3V42G3H_FB

C6995 22PF 5% 50V NP0-C0G-CERM 0201

<Ra>
R6995 348K 1% 1/20W MF 201

<Rb>
R6996 200K 1% 1/20W MF 201

C6999 22UF 20% 6.3V X5R-CERM-1 603

=PP3V42_G3H_REG

Vout = 3.425V
100MA MAX OUTPUT
(Switcher limit)

Vout = 1.25V * (1 + Ra / Rb)

SYNC_MASTER=D2_KEPLER
SYNC_DATE=01/13/2012

PAGE TITLE
DC-In & Battery Connectors

Apple Inc.

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FROM ADAPTER
=PPDCIN_S5_CHGR
=PPDCIN_S5_CHGR_ISOL
Inrush Limiter
C7085 0.1UF 10% 25V X5R 402
R7085 470K 1% 1/16W MF-LF 402
CRITICAL Q7080 IRF9395TRPBF DIRECTFET-MC
NC NC NC NC NC NC
NO STUFF For EMC C7080 4.7UF 10% 25V X5R-CERM 0603
Reverse-Current Protection
PPDCIN_G3H_INRUSH MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=18.5V
R7080 100K 5% 1/16W MF-LF 402
R7081 62K 5% 1/16W MF-LF 402
CHGR_AGATE_DIV MIN_LINE_WIDTH=0.3 mm MIN_NECK_WIDTH=0.25 mm
CHGR_SGATE_DIV MIN_LINE_WIDTH=0.3 mm MIN_NECK_WIDTH=0.25 mm
R7086 332K 1% 1/16W MF-LF 402
CRITICAL D7005 BAT30CWFILM SOT-323
(CHGR_AGATE) (CHGR_SGATE)
R7005 20 5% 1/16W MF-LF 402
CHGR_DCIN_D_R
(CHGR_DCIN)
ACIN pin threshold is 3.2V, +/- 50mV
Divider sets ACIN threshold at 13.55V
Sparkitecture impedance is set by R6912 in 15" MBP
30mA max load
=PP3V42_G3H_CHGR
PP5V1_CHGR_VDD MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.1 mm VOLTAGE=5.1V
R7001 4.7 5% 1/16W MF-LF 402
PP5V1_CHGR_VDDP MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=5.1V
C7001 1UF 10% 10V X5R 402
C7002 1UF 10% 10V X5R 402
NO STUFF R7002 100K 5% 1/16W MF-LF 402
R7012 1K 1% 1/16W MF-LF 402
GND_CHGR_AGND
R7000 0 5% 1/16W MF-LF 402
R7010 130K 1% 1/16W MF-LF 402
SMC_RESET_L
CHGR_RST_L
=SMBUS_CHGR_SCL
=SMBUS_CHGR_SDA
CHGR_VFRQ
CHGR_CELL
CHGR_ACIN
CHGR_ICOMP
CHGR_VCOMP
CHGR_VNEG
CHGR_CSO_P
CHGR_CSO_N
R7011 40.2K 1% 1/16W MF-LF 402
R7015 330K 5% 1/16W MF-LF 402
C7050 1UF 10% 10V X5R 402
CHGR_VCOMP_R
C7015 220PF 10% 50V X7R-CERM 0402
R7042 0 5% 1/16W MF-LF 402
R7016 3.01K 1% 1/16W MF-LF 402
CHGR_VNEG_R
C7016 470PF 10% 50V CERM 0402
CHGR_ICOMP_RC
C7042 0.068UF 10% 16V X5R-CERM 0402
ISL6259 U7000 TQFN
VDD VDDP
VHST CRITICAL DCIN
SMB_RST_N
SCL
SDA
VFRQ
CELL
ACIN
ICOMP
VCOMP
VNEG
CSOP
CSON
THRM_PAD (AGND)
PGND
SGATE CHGR_SGATE
AGATE CHGR_AGATE
CSIP CHGR_CSI_P
CSIN CHGR_CSI_N
BOOT CHGR_BOOT
UGATE CHGR_UGATE
PHASE CHGR_PHASE
LGATE CHGR_LGATE
BGATE CHGR_BGATE
20V/V AMON CHGR_AMON
36V/V BMON CHGR_BMON
(OD) ACOK =CHGR_ACOK
353S2392
XW7000 SM
PLACE_NEAR=U7000.29:1mm
PLACE_NEAR=U7000.22:1mm
(GND)
C7020 0.047UF 10% 10V X5R-CERM 0402
R7021 10 5% 1/16W MF-LF 402
R7022 10 5% 1/16W MF-LF 402
C7022 0.1UF 10% 25V X5R 402
C7021 0.1UF 10% 25V X5R 402
C7025 0.22UF 10% 10V CERM 402
PLACE_NEAR=U7000.25:2mm
CRITICAL Q7030 RJK0332DPB-01 LFPAK-SM
CRITICAL Q7035 RJK0305DPB LFPAK-HF
CHGR_CSI_R_P
CHGR_CSI_R_N
CRITICAL R7020 0.020 0.5% 1W MF-LF 0612
PPDCIN_G3H_CHGR MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=18.5V
Max Current = 8A
(L7030 limit)
f = 400 kHz
CRITICAL L7030 4.7UH-20%-14.5A-9MOHM PIME173T-SM
152S1466
MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.2 mm SWITCH_NODE=TRUE DIDT=TRUE
CRITICAL C7030 10UF 20% 35V TANT-POLY CASE-D2-SM
CRITICAL C7031 10UF 20% 35V TANT-POLY CASE-D2-SM
CRITICAL C7032 10UF 20% 35V TANT-POLY CASE-D2-SM
CRITICAL C7033 10UF 20% 35V TANT-POLY CASE-D2-SM
CRITICAL C7034 10UF 20% 35V TANT-POLY CASE-D2-SM
CRITICAL C7035 1UF 10% 35V X5R 603
CRITICAL C7036 1UF 10% 35V X5R 603
C7037 0.001UF 10% 50V X7R-CERM 0402
TO SYSTEM
CRITICAL F7040 8AMP-32V-0.006OHM 0603
CRITICAL F7041 8AMP-32V-0.006OHM 0603
=PPBUS_G3H
PPVBAT_G3H_CHGR_REG MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=12.6V
OMIT_TABLE
CRITICAL C7040 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7045 0.001UF 10% 50V X7R-CERM 0402
CRITICAL R7050 0.005 1% 1W MF 0612
PPVBAT_G3H_CHGR_R MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=12.6V
C7055 1UF 10% 25V X5R 603-1
C7056 0.1UF 10% 16V X7R-CERM 0402
C7057 0.01UF 10% 16V X7R-CERM 0402
CRITICAL Q7055 SI7137DP SO-8
TO/FROM BATTERY
PPVBAT_G3H_CONN MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=12.6V
NO STUFF CRITICAL R7055 0.001 1% 1W MF 0612
R7051 2.2 5% 1/16W MF-LF 402
R7052 0 5% 1/16W MF-LF 402
(PPVBAT_G3H_CHGR_R)
(CHGR_BGATE)
CHGR_5V:LDO R7092 0 MF-LF 5% 402 1/16W
P5V1_VIN
C7090 4.7UF 10% 35V X5R-CERM 0805
U7090 LT3470A DFN
VIN BOOST SW BIAS FB THRM GND PAD SHDN*
P5V1_BOOST DIDT=TRUE
C7094 0.22UF 10% 10V CERM 402
CRITICAL L7095 33UH-20%-0.39A-0.435OHM DP418C-SM
P5V1_SW MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm SWITCH_NODE=TRUE DIDT=TRUE
P5V1_BIAS
C7095 22PF 5% 50V NP0-C0G-CERM 0201
P5V1_FB
<Ra> R7095 681K 1% 1/20W MF 201
<Rb> R7096 200K 1% 1/20W MF 201
Vout = 1.25V * (1 + Ra / Rb)
NOSTUFF R7090 (P5V1_BIAS) 0 MF-LF 5% 402 1/16W
CHGR_DCIN
CHGR_5V:LDO R7091 0 MF-LF 5% 402 1/16W
PP5V1_CHGR_VDDP
CRITICAL C7098 10UF 20% 10V X5R 0603
CRITICAL C7099 10UF 20% 10V X5R 0603
Vout = 5.50V
100MA MAX OUTPUT
(Switcher limit)

SYNC_MASTER=D2_KEPLER	SYNC_DATE=01/13/2012
PAGE TITLE	PBus Supply & Battery Charger
Apple Inc.	DRAWING NUMBER 051-9589 SIZE D
	REVISION 4.18.0
	BRANCH
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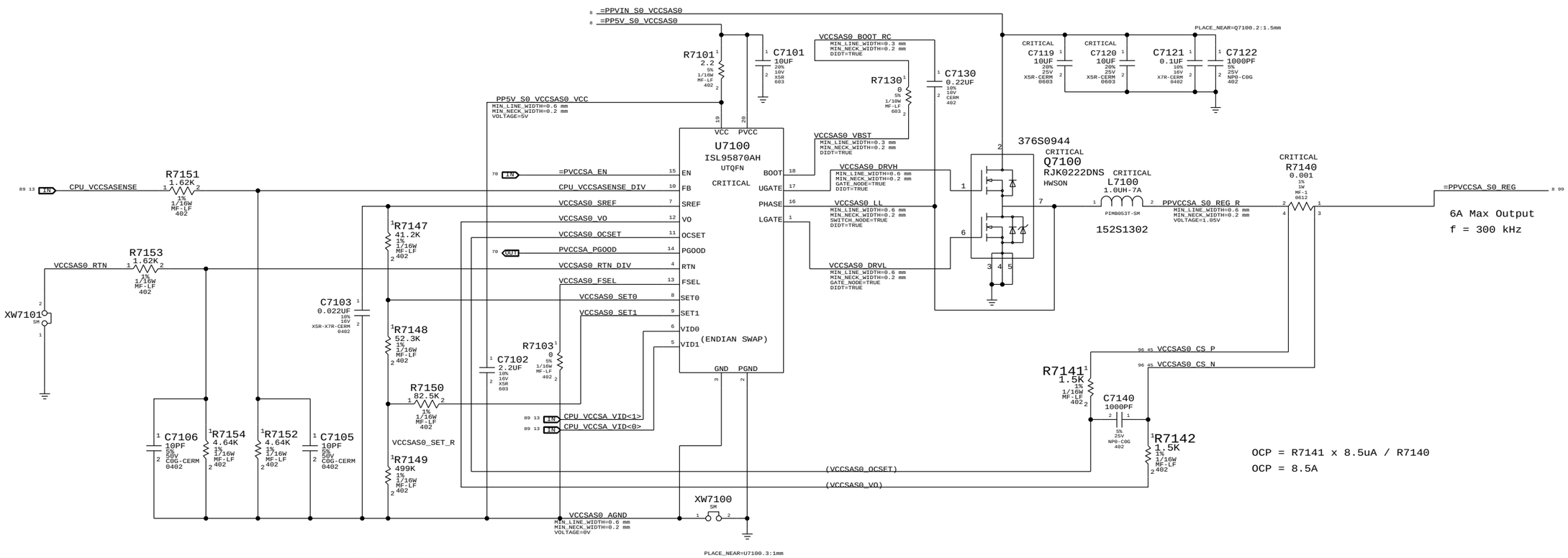

INTEL TABLE:

VID1	VID0	Voltage
0	0	0.9V
1	0	0.8V
0	1	0.725V
1	1	0.675V

fb = (R7151+R7152)/R7152 = 1.349 and Vref = 0.5;

VID1=1, VIC0=1:
Vout<1,1> = Vref x fb;

VID1=0, VID0=1:
Vout<0,1> = Vref x (1+R7147 / (R7148 + R7149)) x fb

VID1=1, VID0=0
Vout<1,0> = Vref x (1+ (R7147 + R7148) / R7149)) x fb

VID1=0, VID0=0
Vout<0,0> = Vref x (1+ (R7147 / (R7148 + R7149 // R7150)) x fb

SYNC MASTER=D2_KEPLER SYNC DATE=01/13/2012

PAGE TITLE

System Agent Supply

Apple Inc.

DRAWING NUMBER 051-9589 SIZE D

REVISION 4.18.0

BRANCH

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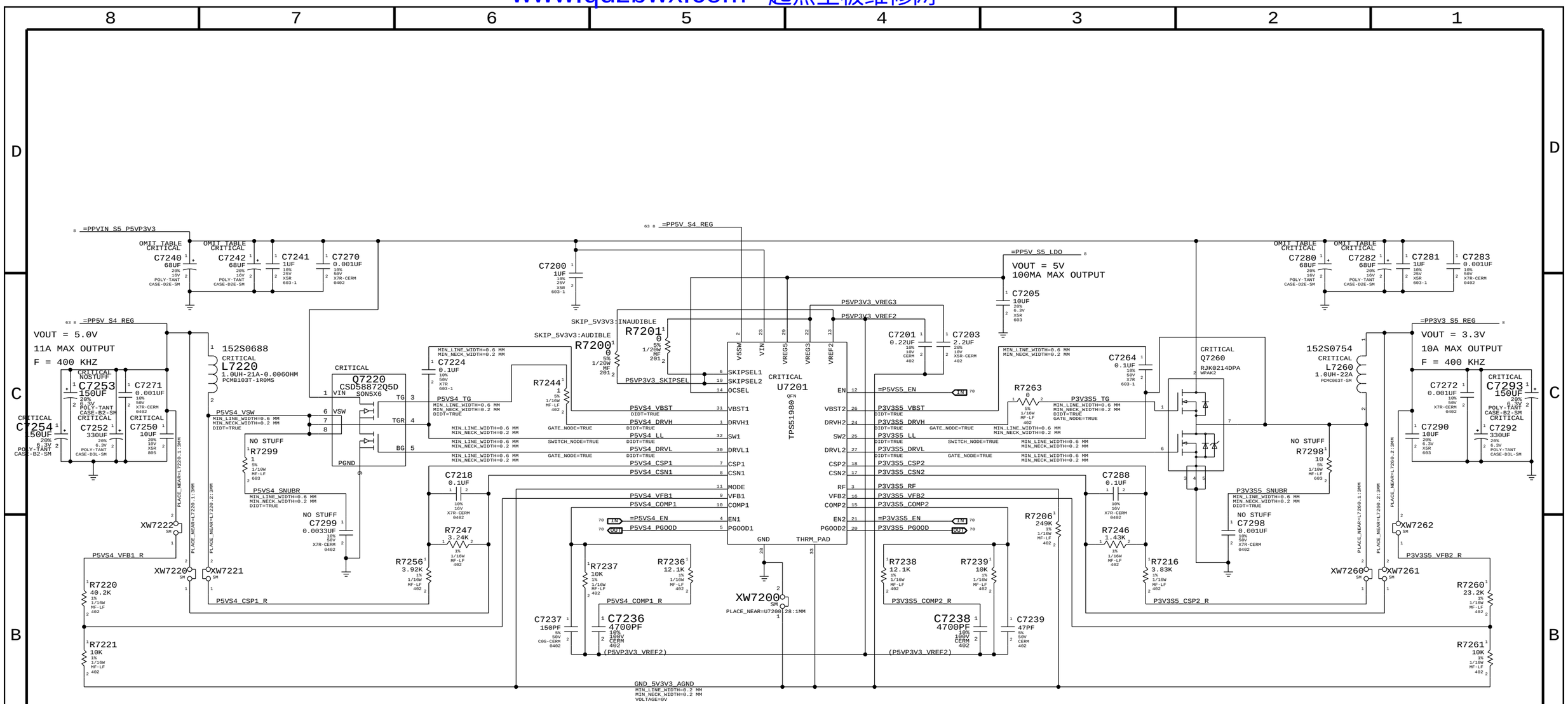

SYNC_MASTER=D2_KEPLER	SYNC_DATE=01/13/2012
PAGE TITLE	5V / 3.3V Power Supply
Apple Inc.	DRAWING NUMBER 051-9589 · SIZE D
	REVISION 4.18.0
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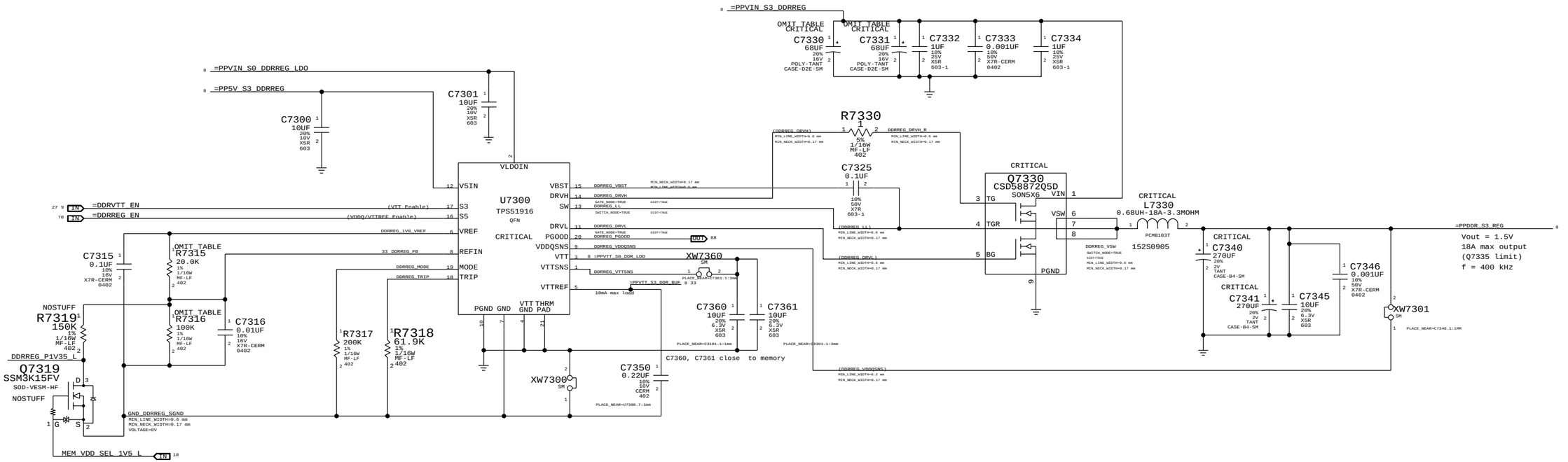
	SHEET 63 OF 99

DDR3 (1V5R1V35 S3) REGULATOR



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0343	1	RES,MTL FILM,1/16W,20.0K,1,0402,SMD,LF	R7315		PPDDR:1V5
114S0342	1	RES,MTL FILM,1/16W,19.6K,1,0402,SMD,LF	R7315		PPDDR:1V35
114S0411	1	RES,MTL FILM,1/16W,100K,1,0402,SMD,LF	R7316		PPDDR:1V5
114S0389	1	RES,MTL FILM,1/16W,57.6K,1,0402,SMD,LF	R7316		PPDDR:1V35

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE

1V5R1V35V DDR3 SUPPLY

Apple Inc.

DRAWING NUMBER 051-9589 SIZE D

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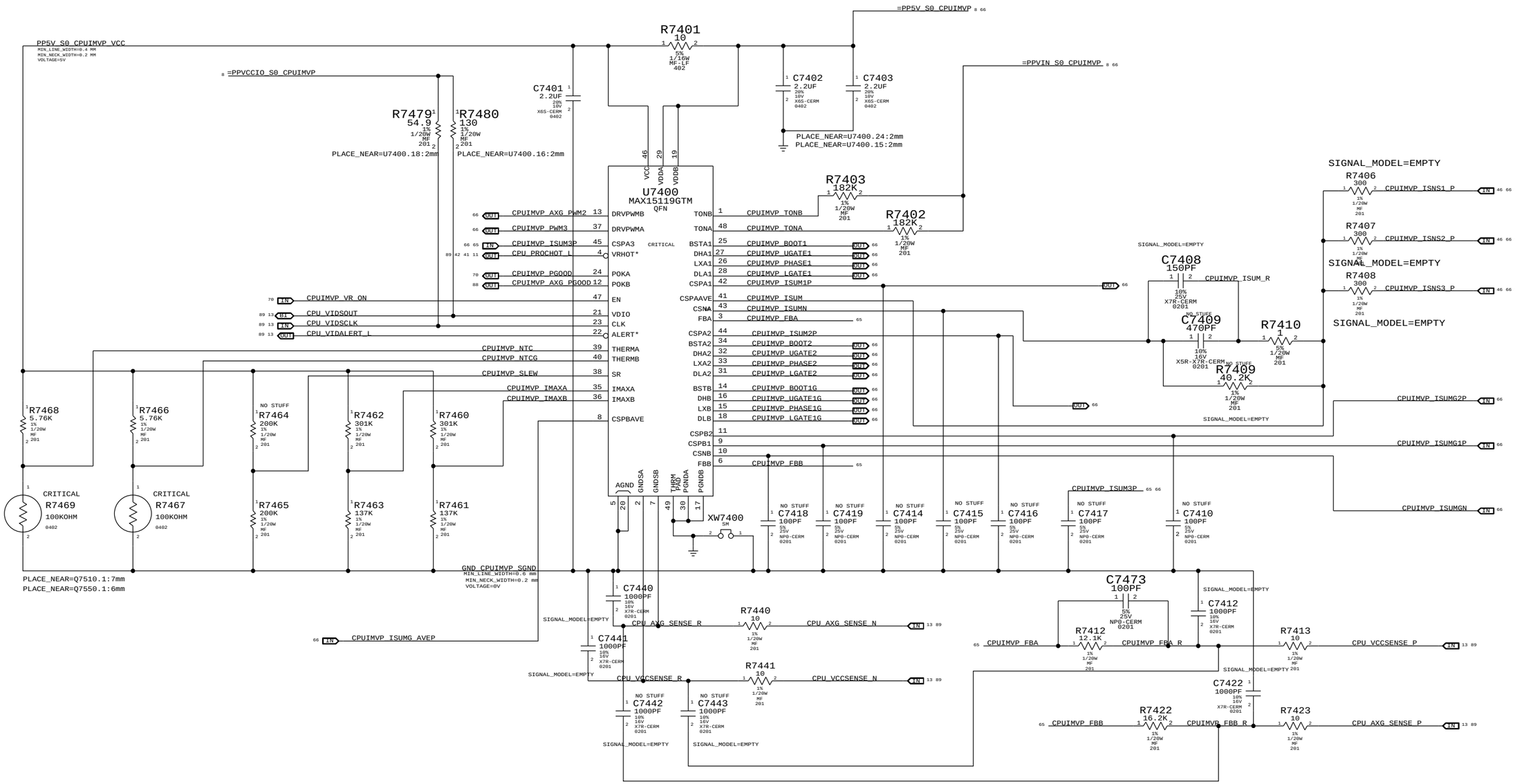

SYNC_MASTER=D2_SEAN SYNC_DATE=03/05/2013

PAGE TITLE

CPU IMVP7 & AXG VCore Regulator

Apple Inc.

DRAWING NUMBER 051-9589 SIZE D

REVISION 4.18.0

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PHASE 1

=PPVIN_S0_CPUIMVP

376S1010

Q7510 IRF6802SDTRPBF DIRECTFET-SA

C7513 68UF (OMIT_TABLE CRITICAL) · C7514 68UF (OMIT_TABLE CRITICAL) · C7515 10UF (NOSTUFF) · C7516 10UF (NOSTUFF CRITICAL) · C7517 1UF · C7518 0.001UF (THESE TWO CAPS ARE FOR EMC) · C7519 0.001UF

R7510 0.00075 (CRITICAL)

L7510 0.36UH-20%-36A-0.001080HM (CRITICAL) PIMS103T-SM 152S1538

PPVCORE_S0_CPU_PH1 — MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=1.25V

=PPVCORE_S0_CPU_REG

R7511 0 · C7511 0.22UF

R7512 2.2 (NOSTUFF) · CPUIMVP_PH1_SNUB · C7512 0.001UF

R7513 46.4 · CPUIMVP_ISNS1_P · R7514 10 · CPUIMVP_ISNS1_N · CPUIMVP_ISUMN · C7581 330PF · CPUIMVP_ISUM1P

Q7515 649135PBF DIRECTFET_S3C 376S1011

CPUIMVP_BOOT1_RC — MIN_LINE_WIDTH=0.25 MM, MIN_NECK_WIDTH=0.25 MM, DIDT=TRUE

CPUIMVP_BOOT1 — MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.2 MM, DIDT=TRUE

CPUIMVP_UGATE1 — MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.2 MM, DIDT=TRUE, GATE_NODE=TRUE

CPUIMVP_PHASE1 — MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.5 MM, DIDT=TRUE, SWITCH_NODE=TRUE

CPUIMVP_LGATE1 — MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.2 MM, DIDT=TRUE, GATE_NODE=TRUE

PHASE 2

376S1010

Q7510 IRF6802SDTRPBF DIRECTFET-SA

C7523 68UF (OMIT_TABLE CRITICAL) · C7524 68UF (OMIT_TABLE CRITICAL) · C7525 10UF (NOSTUFF) · C7526 10UF (CRITICAL) · C7527 1UF · C7528 0.001UF (THESE TWO CAPS ARE FOR EMC) · C7529 0.001UF

R7520 0.00075 (CRITICAL)

L7520 0.36UH-20%-36A-0.001080HM (CRITICAL) PIMS103T-SM 152S1538

PPVCORE_S0_CPU_PH2 — MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=1.25V

=PPVCORE_S0_CPU_REG

R7521 0 · C7521 0.22UF

R7522 2.2 (NOSTUFF) · CPUIMVP_PH2_SNUB · C7522 0.001UF

R7523 46.4 · CPUIMVP_ISNS2_P · R7524 10 · CPUIMVP_ISNS2_N · CPUIMVP_ISUMN · C7582 330PF · CPUIMVP_ISUM2P

Q7525 649135PBF DIRECTFET_S3C 376S1011

CPUIMVP_BOOT2_RC — MIN_LINE_WIDTH=0.25 MM, MIN_NECK_WIDTH=0.25 MM, DIDT=TRUE

CPUIMVP_BOOT2 — MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.2 MM, DIDT=TRUE

CPUIMVP_UGATE2 — MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.2 MM, DIDT=TRUE, GATE_NODE=TRUE

CPUIMVP_PHASE2 — MIN_LINE_WIDTH=1.5 MM, MIN_NECK_WIDTH=0.2 MM, DIDT=TRUE, SWITCH_NODE=TRUE

CPUIMVP_LGATE2 — MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.2 MM, DIDT=TRUE, GATE_NODE=TRUE

PHASE 3

=PP5V_S0_CPUIMVP

U7541 MAX17491 TQFN (CRITICAL) — VDD, PWN, SKIP*, BST, DH, LX, DL, GND, THRM PAD

R7547 10K · C7541 1UF

CPUIMVP_PWM3 · CPUIMVP_SKIP

CPUIMVP_BOOT3_RC — MIN_LINE_WIDTH=0.25 MM, MIN_NECK_WIDTH=0.25 MM, DIDT=TRUE

R7531 3.3 · C7531 0.22UF

CPUIMVP_BOOT3 — MIN_LINE_WIDTH=0.25 MM, MIN_NECK_WIDTH=0.2 MM, DIDT=TRUE

CPUIMVP_UGATE3 — MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.2 MM, DIDT=TRUE, GATE_NODE=TRUE

CPUIMVP_PHASE3 — MIN_LINE_WIDTH=1.5 MM, MIN_NECK_WIDTH=0.2 MM, DIDT=TRUE, SWITCH_NODE=TRUE

CPUIMVP_LGATE3 — MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.2 MM, DIDT=TRUE, GATE_NODE=TRUE

376S1014

Q7530 649136PBF S1 (CRITICAL)

C7533 68UF (OMIT_TABLE CRITICAL) · C7534 68UF (OMIT_TABLE CRITICAL) · C7535 10UF (CRITICAL) · C7536 10UF (CRITICAL) · C7537 1UF · C7538 0.001UF (THESE TWO CAPS ARE FOR EMC) · C7539 0.001UF

R7530 0.00075 (CRITICAL)

L7530 0.36UH-20%-36A-0.001080HM (CRITICAL) PIMS103T-SM 152S1538

CPUIMVP_PHASE3_L — MIN_LINE_WIDTH=1.5 MM, MIN_NECK_WIDTH=0.3 MM, DIDT=TRUE, SWITCH_NODE=TRUE

PPVCORE_S0_CPU_PH3 — MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=1.25V

=PPVCORE_S0_CPU_REG

R7532 2.2 (NOSTUFF) · CPUIMVP_PH3_SNUB · C7532 0.001UF

R7533 46.4 · CPUIMVP_ISNS3_P · R7582 46.4 · R7534 10 · CPUIMVP_ISNS3_N · CPUIMVP_ISUMN · C7583 330PF · CPUIMVP_ISUM3P

Q7535 649135PBF DIRECTFET_S3C 376S1011

Additonal Input Bulk Caps (D SIZE)

C7570 68UF · C7571 68UF · C7572 68UF · C7574 15UF · C7575 68UF · C7578 15UF

(B SIZE)

C7573 15UF · C7576 15UF

AXG PHASE 1

=PPVIN_S0_CPUAXG

376S1010

Q7550 IRF6802SDTRPBF DIRECTFET-SA

C7554 68UF (OMIT_TABLE CRITICAL) · C7555 10UF (NOSTUFF) · C7556 10UF (CRITICAL) · C7557 1UF · C7558 0.001UF (THESE TWO CAPS ARE FOR EMC) · C7559 0.001UF

R7550 0.00075 (CRITICAL)

L7550 0.36UH-20%-36A-0.001080HM (CRITICAL) PIMS103T-SM 152S1538

PPVCORE_S0_AXG1_L — MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.05V

=PPVCORE_S0_AXG_REG

R7556 0 · C7551 0.22UF

R7552 2.2 (NOSTUFF) · CPUIMVP_AXG1_SNUB · C7552 0.001UF

R7553 46.4 · CPUIMVP_ISNS1G_P · R7554 10 · CPUIMVP_ISNS1G_N · CPUIMVP_ISUMGN · C7584 330PF · CPUIMVP_ISUMG1P

Q7551 649135PBF DIRECTFET_S3C 376S1011

CPUIMVP_BOOT1G — MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.2 MM, DIDT=TRUE

CPUIMVP_UGATE1G — MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.2 MM, DIDT=TRUE, GATE_NODE=TRUE

CPUIMVP_PHASE1G — MIN_LINE_WIDTH=1.5 MM, MIN_NECK_WIDTH=0.5 MM, DIDT=TRUE, SWITCH_NODE=TRUE

CPUIMVP_LGATE1G — MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.5 MM, DIDT=TRUE, GATE_NODE=TRUE

=PP5V_S0_CPUIMVP

U7542 MAX17491 TQFN (CRITICAL) — VDD, PWN, SKIP*, BST, DH, LX, DL, GND, THRM PAD

R7540 10K · C7540 1UF

CPUIMVP_AXG_PWM2 · CPUIMVP_SKIP

CPUIMVP_BOOT2G — MIN_LINE_WIDTH=0.25 MM, MIN_NECK_WIDTH=0.25 MM, DIDT=TRUE

CPUIMVP_UGATE2G — MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.2 MM, DIDT=TRUE, GATE_NODE=TRUE

CPUIMVP_PHASE2G — MIN_LINE_WIDTH=1.5 MM, MIN_NECK_WIDTH=0.2 MM, DIDT=TRUE, SWITCH_NODE=TRUE

CPUIMVP_LGATE2G — MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.2 MM, DIDT=TRUE, GATE_NODE=TRUE

CPUIMVP_BOOT2G_RC — MIN_LINE_WIDTH=0.25 MM, MIN_NECK_WIDTH=0.25 MM, DIDT=TRUE

R7535 3.3 · C7530 0.22UF

AXG PHASE 2

376S1010

Q7550 IRF6802SDTRPBF DIRECTFET-SA

C7560 68UF (OMIT_TABLE CRITICAL) · C7561 68UF (OMIT_TABLE CRITICAL) · C7562 10UF (NOSTUFF CRITICAL) · C7563 10UF (NOSTUFF CRITICAL) · C7564 1UF · C7565 0.001UF (THESE TWO CAPS ARE FOR EMC) · C7566 0.001UF

R7560 0.00075 (CRITICAL)

L7560 0.36UH-20%-36A-0.001080HM (CRITICAL) PIMS103T-SM 152S1538

PPVCORE_S0_AXG2_L — MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.05V

=PPVCORE_S0_AXG_REG

R7587 2.2 (NOSTUFF) · CPUIMVP_AXG2_SNUB · C7587 0.001UF

R7561 46.4 · CPUIMVP_ISNS2G_P · R7562 10 · CPUIMVP_ISNS2G_N · CPUIMVP_ISUMGN · C7567 330PF · CPUIMVP_ISUMG2P

Q7561 649135PBF DIRECTFET_S3C 376S1011

R7563 200 · CPUIMVP_ISNS1G_P · R7564 200 · CPUIMVP_ISUMG_AVEP

R7565 0 (NOSTUFF) · R7566 0 · CPUIMVP_ISUMG_AVE_RP · C7568 1000PF · C7569 330PF

CPUIMVP_ISUMGN

SYNC_MASTER=D2_SEAN SYNC_DATE=03/05/2012

PAGE TITLE: CPU IMVP7 & AXG VCore Output

Apple Inc.

DRAWING NUMBER 051-9589 SIZE D

REVISION 4.18.0

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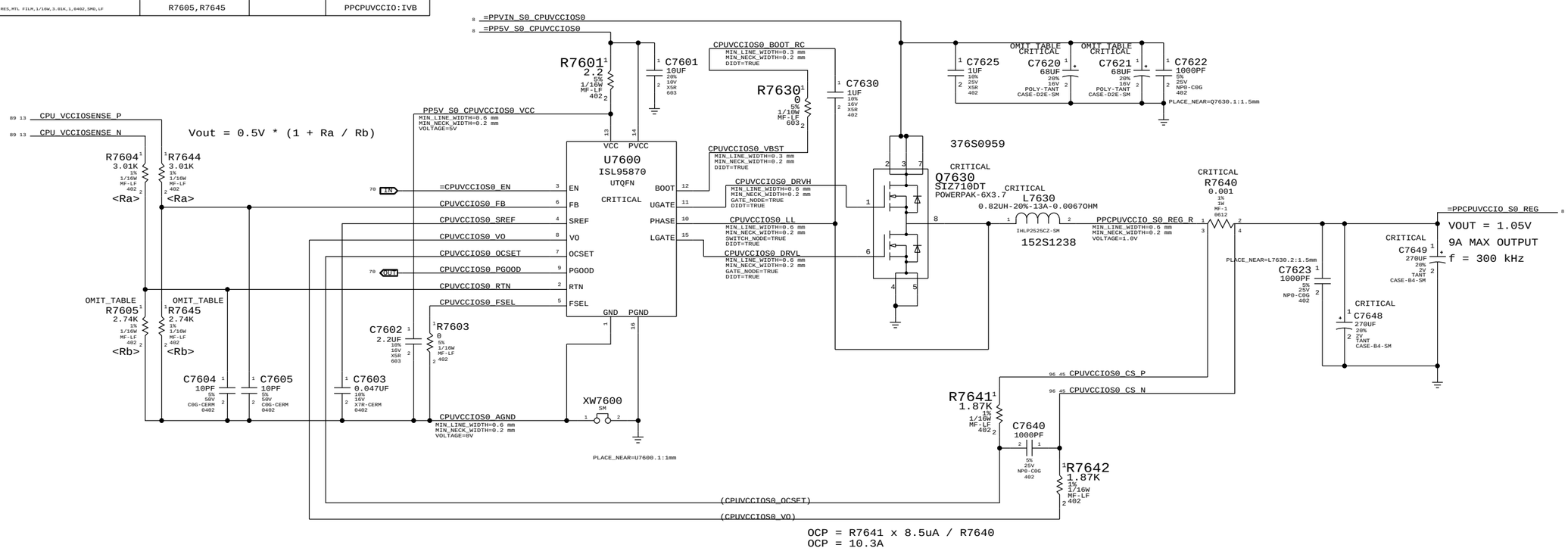
CPU VCCIO (1V0R1V05 S0) REGULATOR

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0260	2	RES,MTL FILM,1/16W,2.74K,1,0402,SMD,LF	R7605,R7645		PPCPUVCCIO:SNB
114S0264	2	RES,MTL FILM,1/16W,3.01K,1,0402,SMD,LF	R7605,R7645		PPCPUVCCIO:IVB



SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE

CPU VCCIO (1V0R1V05 S0) POWER SUPPLY

Apple Inc.

DRAWING NUMBER 051-9589 SIZE D

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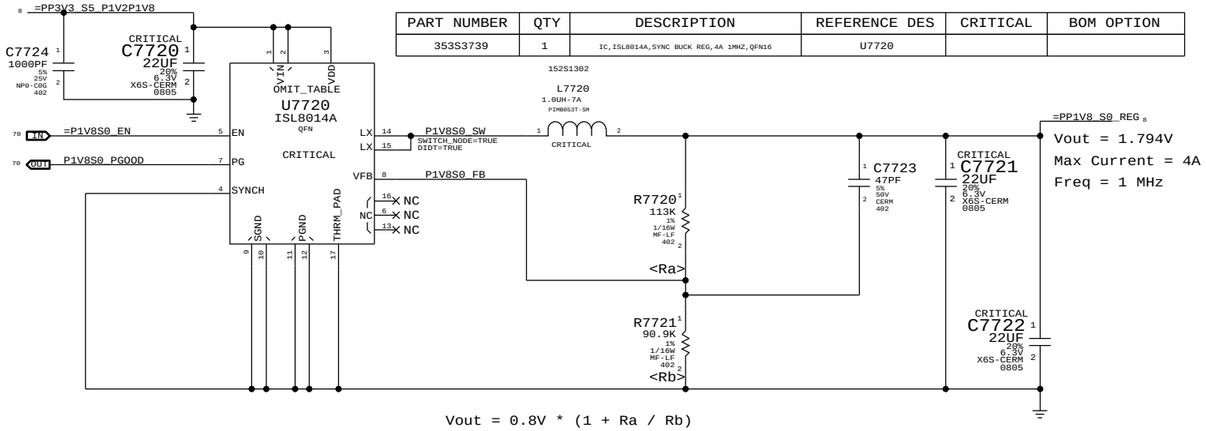
1.8V S0 Regulator

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S3739	1	IC,ISL8014A,SYNC BUCK REG,4A 1MHZ,QFN16	U7720		



Vout = 0.8V * (1 + Ra / Rb)

1.5V S0 Regulator

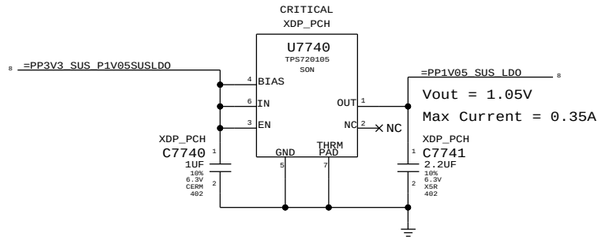
Vout = 0.8V * (1 + Ra / Rb)

1.5V S0 LDO (RIO)

Vout = 0.8V * (1 + Ra / Rb)

1.05V SUS LDO

Panther Point-M requires JTAG pull-ups to be powered at 1.05V in Sus.
Pull-ups (3) must be 51 ohms to support XDP (not required in production).
70mA is required to support pull-ups. Alternative is strong voltage
dividers (200/100) to 3.3V Sus, which burns 100mW in all S-states.



SYNC_MASTER=D2_KEPLER	SYNC_DATE=01/13/2012
PAGE TITLE	Misc Power Supplies
	Apple Inc.
DRAWING NUMBER	051-9589
SIZE	D
REVISION	4.18.0
BRANCH	
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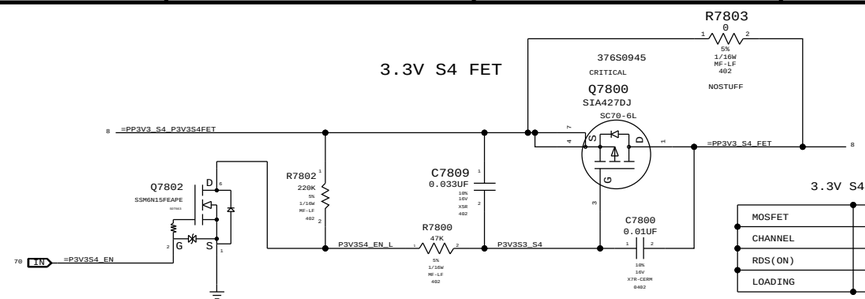
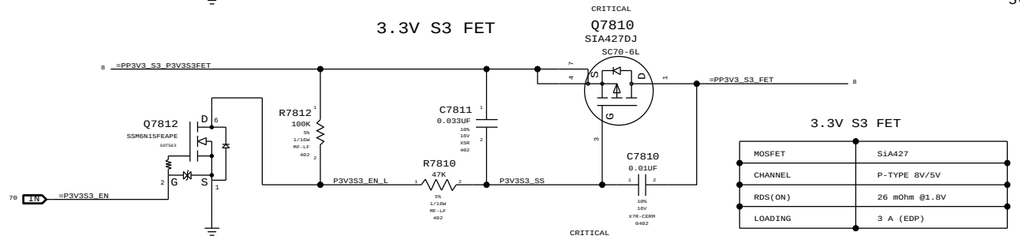
3.3V S4 FET



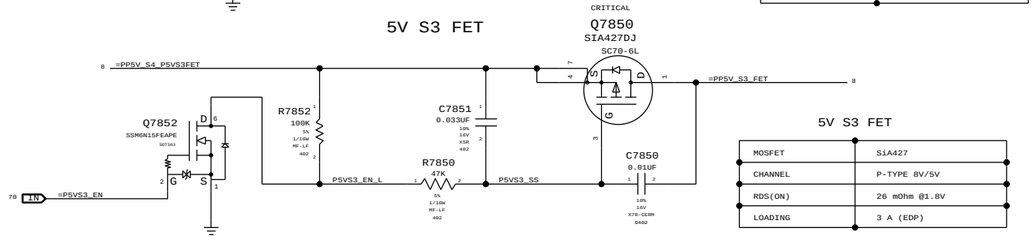
3.3V S4 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.7? A (EDP)

3.3V S3 FET



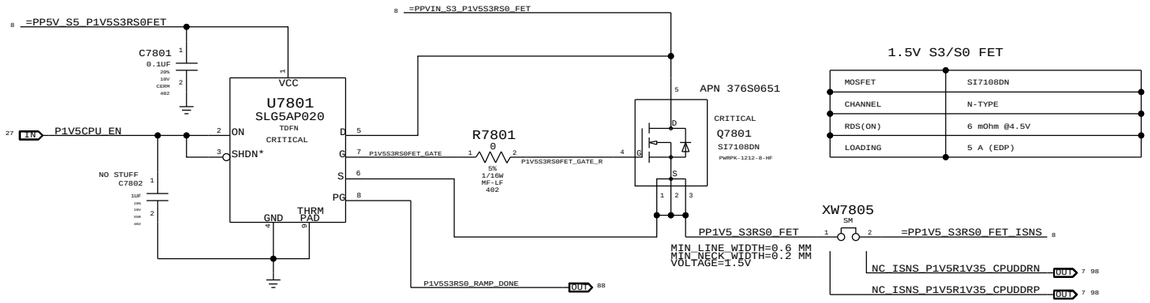
3.3V S3 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	3 A (EDP)

5V S3 FET



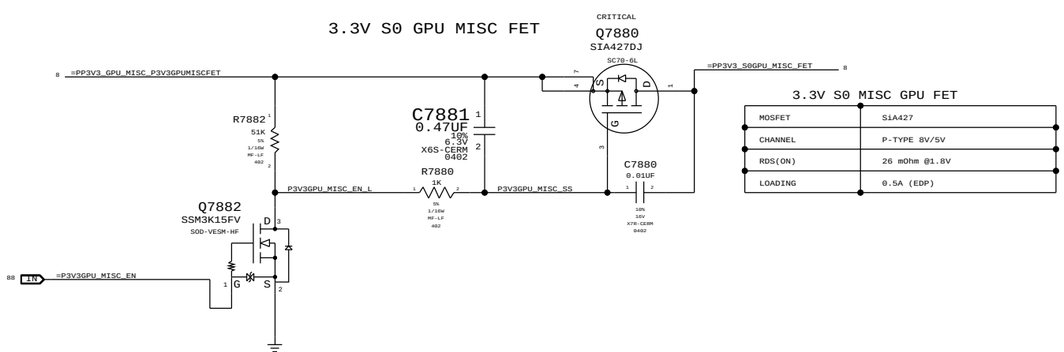
5V S3 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	3 A (EDP)

1.5V S3/S0 FET



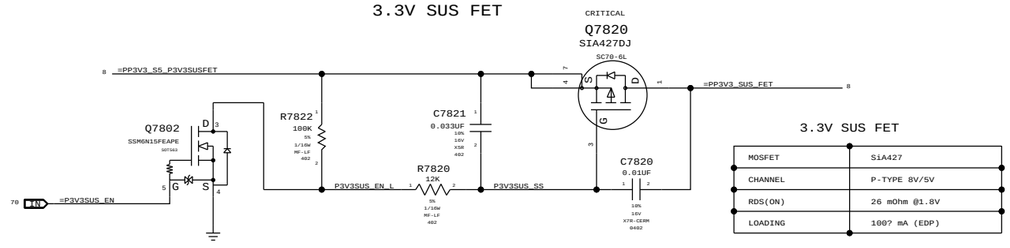
1.5V S3/S0 FET	
MOSFET	SI7108DN
CHANNEL	N-TYPE
RDS(ON)	6 mOhm @4.5V
LOADING	5 A (EDP)

3.3V S0 GPU MISC FET



3.3V S0 MISC GPU FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.5A (EDP)

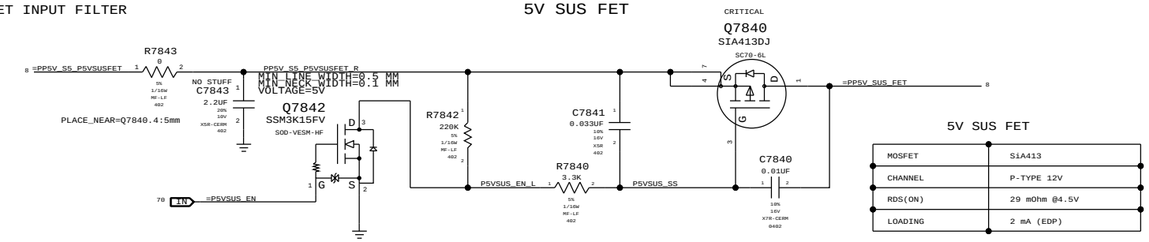
3.3V SUS FET



3.3V SUS FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	100? mA (EDP)

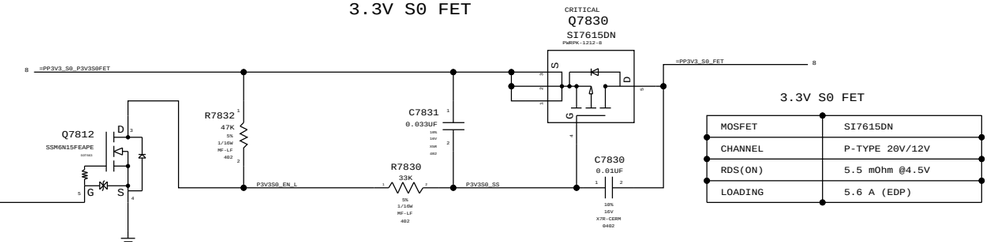
5V_SUS FET INPUT FILTER

5V SUS FET



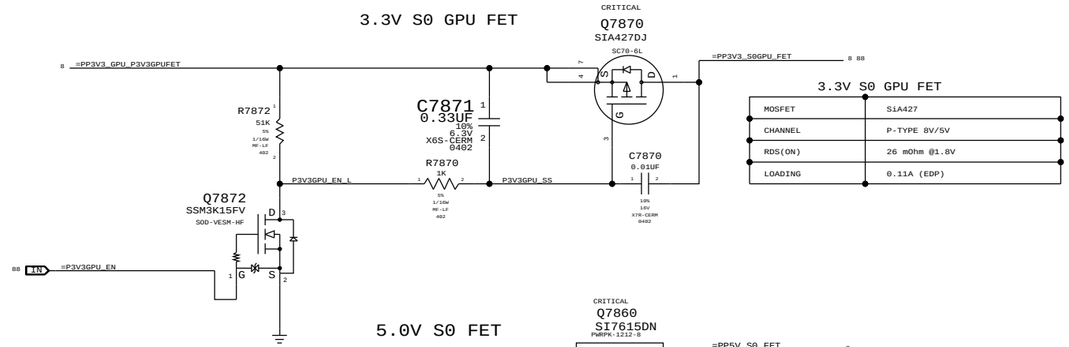
5V SUS FET	
MOSFET	SiA413
CHANNEL	P-TYPE 12V
RDS(ON)	29 mOhm @4.5V
LOADING	2 mA (EDP)

3.3V S0 FET



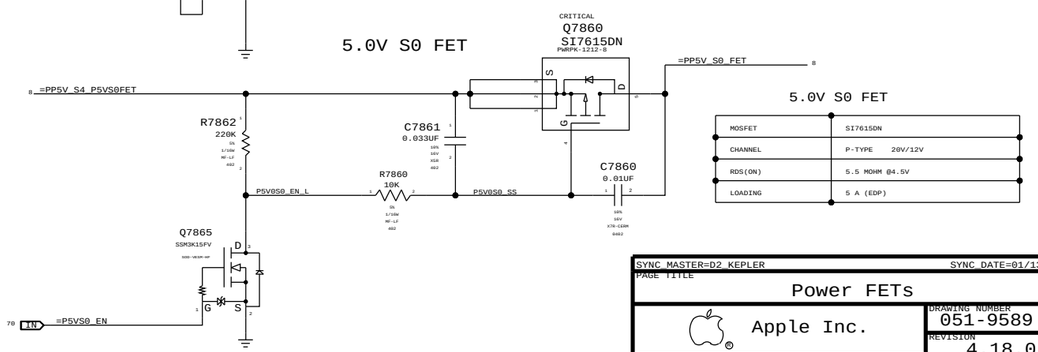
3.3V S0 FET	
MOSFET	SI7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 mOhm @4.5V
LOADING	5.6 A (EDP)

3.3V S0 GPU FET



3.3V S0 GPU FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.11A (EDP)

5.0V S0 FET



5.0V S0 FET	
MOSFET	SI7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 MOHM @4.5V
LOADING	5 A (EDP)

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE

Power FETs

Apple Inc.

DRAWING NUMBER 051-9589 SIZE D

REVISION 4.18.0

BRANCH

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S5 Rail Enables & PGOOD

R7940 100 5% 1/16W MF-LF 402 — PLACE_NEAR=U7201.21:7mm
C7942 0.0033UF 10% 50V X7R-CERM 0402 NO STUFF
=PP3V42_G3H_PWRCTL — PLACE_NEAR=U7201.20:7mm
R7941 100K 5% 1/16W MF-LF 402
P3V3S5_PGOOD — S5_PWRGD (MAKE_BASE=TRUE) — S5_PWRGD (old name RSMRST_PWRGD)-->SMC
SMC_PM_G2_EN (MAKE_BASE=TRUE) — P3V3S5_EN (MAKE_BASE=TRUE) — =P3V3S5_EN

Mobile System Power State Table

State	SMC_ADAPTER_EN	SMC_PM_G2_ENABLE	SMC_S4_WAKESRC_EN	PM_SUS_EN	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	X	1	1	1	1	1	1
Sleep (S3AC)	1	1	1	1	1	1	0
Sleep (S3)	0	1	1	1	1	1	0
Deep Sleep (dS4AC)	1	1	1	0	0	0	0
Deep Sleep (dS4)	0	1	1	0	0	0	0
Deep Sleep (dS5AC)	1	1	0	0	0	0	0
Deep Sleep (dS5)	0	1	0	0	0	0	0
Battery Off (G3HotAC)	toggle 3Hz	0	0	0	0	0	0
Battery Off (G3Hot)	1	0	0	0	0	0	0

3.3V S4 ENABLE

=PP3V3_S5_PWRCTL — PLACE_NEAR=U7940.1:2.3mm
C7970 0.1uF 20% 10V CERM 402
PM_SLP_S5_L:100K pull down on PCH page — PM_SLP_S5_L
U7970 74LVC1G32 SOT891 (NC, NC)
P5V3V3_S4_EN (MAKE_BASE=TRUE)
SMC_S4_WAKESRC_EN (MAKE_BASE=TRUE)
NOSTUFF R7915 0 5% 1/16W MF-LF 402
=P5VS4_TPAD_EN, =P3V3S4_EN, =TBTAPWRSW_EN, =TBTBPWRSW_EN

5V, 3.3V, DDR S3 ENABLE

PM_SLP_S4_L:100K pull down in PCH page — PM_SLP_S4_L
R7911 5.1K 5% 1/16W MF-LF 402 — PLACE_NEAR=U7300.16:6mm
R7912 0 5% 1/16W MF-LF 402 — PLACE_NEAR=Q7812.2:6mm
R7913 0 5% 1/16W MF-LF 402 — PLACE_NEAR=Q7842.2:6MM
R7914 3.3K 5% 1/20W MF 201 — PLACE_NEAR=U5701.4:6MM
C7910 0.47UF 10% 6.3V CERM-X5R 402
C7912 NO STUFF 0.47UF 10% 6.3V CERM-X5R 402
C7913 NO STUFF 0.47UF 10% 6.3V CERM-X5R 402
C7914 NO STUFF 0.47UF 10% 6.3V CERM-X5R 402
TPAD_VBUS_EN, P5VS3_EN, P3V3S3_EN, DDRREG_EN (MAKE_BASE=TRUE)
R7975 0 5% 1/20W MF 201 — P5VS4_EN — =P5VS4_EN
C7975 NO STUFF 0.47UF 10% 6.3V CERM-X5R 402

CPUVCORE ENABLE

R7974 0 5% 1/16W MF-LF 402 — PLACE_NEAR=U7400.7:5mm
ALL_SYS_PWRGD — CPUIMVP_VR_ON

3.3V/5.0V Sus ENABLE

=PP3V3_S5_PWRCTL — PLACE_NEAR=U7940.1:2.3mm
C7940 0.1uF 20% 10V CERM 402
SMC_BATLOW_L:100K pull up on SMC page — SMC_BATLOW_L
PM_SLP_SUS_L:100K pull down on PCH page — PM_SLP_SUS_L
U7940 74AUP1G3208 SOT891 (VCC, A, B, Y, C, GND)
PM_SUS_EN (MAKE_BASE=TRUE) — =P5VSUS_EN, =P3V3SUS_EN
NO STUFF R7917 0 5% 1/16W MF-LF 402

S0 ENABLE

PM_SLP_S3_L — PM_SLP_S3_L:100K pull down in PCH page
R7978 100 5% 1/16W MF-LF 402
(PM_SLP_S3_R_L) — PM_SLP_S3_R_L (MAKE_BASE=TRUE)
R7987 33K 5% 1/16W MF-LF 402 — PLACE_NEAR=U7100.15:6mm
R7981 20K 5% 1/16W MF-LF 402 — PLACE_NEAR=U7600.3:6mm
R7985 20K 5% 1/16W MF-LF 402 — PLACE_NEAR=U7760.4:6mm
R7988 10K 5% 1/16W MF-LF 402 — PLACE_NEAR=U7710.2:6mm
R7986 5.1K 5% 1/16W MF-LF 402 — PLACE_NEAR=U7720.5:6mm
=P5VS0_EN, =P3V3S0_EN, =PBUSVSENS_EN, =TBT_S0_EN
P1V8S0_EN (MAKE_BASE=TRUE) — =P1V8S0_EN
P1V5S0_EN (MAKE_BASE=TRUE) — =P1V5S0_EN
PCHVCCIOS0_EN (MAKE_BASE=TRUE) — =PCHVCCIOS0_EN
CPUVCCIOS0_EN (MAKE_BASE=TRUE) — =CPUVCCIOS0_EN
PVCCSA_EN (MAKE_BASE=TRUE) — =PVCCSA_EN
C7987 0.47UF, C7981 0.47UF, C7985 1UF 10% 6.3V CERM-X5R 402, C7988 0.47UF, C7986 0.47UF 10% 6.3V X6S-CERM 0402

CHGR VFRQ Generation

=PP3V42_G3H_CHGR
R7931 100K 5% 1/16W MF-LF 402
CHGR_VFRQ
Q7931 SSM3K15FV SOD-VESM-HF
VFRQ Low: Fix Frequency
VFRQ High: Variable Frequency

S0 Rail PGOOD (BJT Version)

=PP3V3_S0_VMON — R7951 15.0K 1% 1/16W MF-LF 402
=PP3V3_S5_VMON — R7956 150K 1% 1/16W MF-LF 402
R7953 1K, R7952 7.15K, R7954 1K, R7955 1K 5% 1/16W MF-LF 402
VMON_3V3_DIV, VMON_Q2_BASE, VMON_Q3_BASE, VMON_Q4_BASE
=PP1V5_S3RS0_VMON — PP1V5_S3RS0
=PP1V05_S0_VMON
S0PGD_C — ALL_SYS_PWRGD
Q7950 ASMCC0179 DFN2015H4-8 (Q1, Q2, NC, Q3 CRITICAL, NC, Q4)
353S2809 S0PGD_BJT_GND_R
R7957 100 5% 1/16W MF-LF 402
Worst-Case Thresholds:
Q2: 0.XXXV
Q3: 0.640V
3.3V w/Divider: 2.345V
Q4: 0.660V

3.3V SUS Detect

=PP3V3_S5_PWRCTL — PLACE_NEAR=U7930.6:2.3mm
C7930 0.1uF 20% 10V CERM 402
No stuff C7931, 12ms Min delay time
U7930 Sense input threhold is 3.07V
U7930 TPS3808G33DBVRG4 SOT23-6 (SENSE, CT, VDD, RESET*, MR*, GND)
C7931 0.001UF 20% 50V CERM 402 NO STUFF
Sus_PGOOD_CT — SUS_PGOOD_MR_L — PM_RSMRST_L — PM_RSMRST_L goes to U1800.C21
R7930 0 5% 1/20W MF 201 — =PP3V3_SUS_CNTRL
R7933 100K 5% 1/16W MF-LF 402
Could stuff to satisfy PCH power down timing t235

PCH S0 PWRGD

=PP3V3_S5_PCHPWRGD, =PP3V3_S0_SB_PM
R7950 1K 5% 1/16W MF-LF 402
C7950 0.1UF 20% 10V CERM 402
ALL_SYS_PWRGD, CPUIMVP_PGOOD
U7950 74LVC2G08GT SOT833 (08)
PM_S0_PGOOD
CKPLUS_WAIVE=UNCONNECTED_PINS
U7950 74LVC2G08GT SOT833 (08)
SYS_PWROK_R — R7949 1K 5% 1/16W MF-LF 402 — PM_PCH_SYS_PWROK
PM_PCH_APWROK
SMC_DELAYED_PWRGD — R7948 0 5% 1/16W MF-LF 402 — PM_PCH_PWROK (MAKE_BASE=TRUE)

S0 Rail PGOOD Circuitry (ISL Version in development)

Thresholds:
VDD: 2.734V-3.010V
V2MON: 2.815V-3.099V
V3MON: 0.572V-0.630V
V4MON: 0.572V-0.630V

=PP3V3_S0_PWRCTL — R7967 10K 5% 1/16W MF-LF 402
P1V5S0_PGOOD from U7710
R7968 100, R7966 100, R7965 100, R7964 100, R7969 100, R7963 100 5% 1/16W MF-LF 402
P1V5S0_PGOOD, P1V8S0_PGOOD, P5VS4_PGOOD, CPUVCCIOS0_PGOOD, PCHVCCIOS0_PGOOD, PVCCSA_PGOOD
=PP3V3_S0_VMON — C7960 0.1UF 20% 10V X7R-CERM 0402
R7960 6.04K, R7970 10K, R7972 6.04K, R7961 15.0K, R7971 10K, R7973 15.0K 1% 1/16W MF-LF 402
OMIT_TABLE
U7960 ISL88042IRTEZ TDFN (VDD, V2MON, V3MON, V4MON, GND, THRM_PAD, MR* (IPU), RST*)
S0PGOOD_ISL — R7962 330 5% 1/16W MF-LF 402 — ALL_SYS_PWRGD_R
353S2310

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0315	1	RES,MTL FILM,1/16W,10K,1,0402,SMD,LF	R7971		PPDDR:1V5
114S0323	1	RES,MTL FILM,1/16W,12.4K,1,0402,SMD,LF	R7971		PPDDR:1V35

"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))
NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.

PM_WLAN_EN_L
Q7925 SSM3K15FV SOD-VESM-HF
AP_PWR_EN
AC_EN_L
Q7920 SSM6N15FEAPE SOT563 (x2)
NO STUFF R7929 0 5% 1/16W MF-LF 402
SMC_ADAPTER_EN, PM_SLP_S3_L

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012
PAGE TITLE: Power Control 1/ENABLE
Apple Inc.
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Page Notes

Power aliases required by this page:
- +PP3V3_GPU_VDD33

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

C8020	0.22UF	PEG_R2D_C_P<0>	PEG_R2D_P<0>	89 9	71 88 89
C8021	0.22UF	PEG_R2D_C_N<0>	PEG_R2D_N<0>	89 9	71 88 89
C8022	0.22UF	PEG_R2D_C_P<1>	PEG_R2D_P<1>	89 9	71 89
C8023	0.22UF	PEG_R2D_C_N<1>	PEG_R2D_N<1>	89 9	71 89
C8024	0.22UF	PEG_R2D_C_P<2>	PEG_R2D_P<2>	89 9	71 89
C8025	0.22UF	PEG_R2D_C_N<2>	PEG_R2D_N<2>	89 9	71 89
C8026	0.22UF	PEG_R2D_C_P<3>	PEG_R2D_P<3>	89 9	71 88 89
C8027	0.22UF	PEG_R2D_C_N<3>	PEG_R2D_N<3>	89 9	71 88 89
C8028	0.22UF	PEG_R2D_C_P<4>	PEG_R2D_P<4>	89 9	71 89
C8029	0.22UF	PEG_R2D_C_N<4>	PEG_R2D_N<4>	89 9	71 89
C8030	0.22UF	PEG_R2D_C_P<5>	PEG_R2D_P<5>	89 9	71 88 89
C8031	0.22UF	PEG_R2D_C_N<5>	PEG_R2D_N<5>	89 9	71 88 89
C8032	0.22UF	PEG_R2D_C_P<6>	PEG_R2D_P<6>	89 9	71 89
C8033	0.22UF	PEG_R2D_C_N<6>	PEG_R2D_N<6>	89 9	71 89
C8034	0.22UF	PEG_R2D_C_P<7>	PEG_R2D_P<7>	89 9	71 88 89
C8035	0.22UF	PEG_R2D_C_N<7>	PEG_R2D_N<7>	89 9	71 88 89

C8055	0.22UF	PEG_D2R_C_P<0>	PEG_D2R_P<0>	89 71	9 88 89
C8056	0.22UF	PEG_D2R_C_N<0>	PEG_D2R_N<0>	89 71	9 88 89
C8057	0.22UF	PEG_D2R_C_P<1>	PEG_D2R_P<1>	89 71	9 89
C8058	0.22UF	PEG_D2R_C_N<1>	PEG_D2R_N<1>	89 71	9 89
C8059	0.22UF	PEG_D2R_C_P<2>	PEG_D2R_P<2>	89 71	9 89
C8060	0.22UF	PEG_D2R_C_N<2>	PEG_D2R_N<2>	89 71	9 89
C8061	0.22UF	PEG_D2R_C_P<3>	PEG_D2R_P<3>	89 71	9 89
C8062	0.22UF	PEG_D2R_C_N<3>	PEG_D2R_N<3>	89 71	9 89
C8063	0.22UF	PEG_D2R_C_P<4>	PEG_D2R_P<4>	89 71	9 88 89
C8064	0.22UF	PEG_D2R_C_N<4>	PEG_D2R_N<4>	89 71	9 88 89
C8065	0.22UF	PEG_D2R_C_P<5>	PEG_D2R_P<5>	89 71	9 89
C8066	0.22UF	PEG_D2R_C_N<5>	PEG_D2R_N<5>	89 71	9 89
C8067	0.22UF	PEG_D2R_C_P<6>	PEG_D2R_P<6>	89 71	9 89
C8068	0.22UF	PEG_D2R_C_N<6>	PEG_D2R_N<6>	89 71	9 89
C8069	0.22UF	PEG_D2R_C_P<7>	PEG_D2R_P<7>	89 71	9 88 89
C8070	0.22UF	PEG_D2R_C_N<7>	PEG_D2R_N<7>	89 71	9 88 89

OMIT_TABLE

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PEG_R2D_P<0>	89 88 71	AN12	PEX_RX0	PEX_TX0	AK14	PEG_D2R_C_P<0>	71 89
PEG_R2D_N<0>	89 88 71	AM12	PEX_RX0*	PEX_TX0*	AJ14	PEG_D2R_C_N<0>	71 89
PEG_R2D_P<1>	89 71	AN14	PEX_RX1	PEX_TX1	AH14	PEG_D2R_C_P<1>	71 89
PEG_R2D_N<1>	89 71	AM14	PEX_RX1*	PEX_TX1*	AG14	PEG_D2R_C_N<1>	71 89
PEG_R2D_P<2>	89 71	AP14	PEX_RX2	PEX_TX2	AK15	PEG_D2R_C_P<2>	71 89
PEG_R2D_N<2>	89 71	AP15	PEX_RX2*	PEX_TX2*	AJ15	PEG_D2R_C_N<2>	71 89
PEG_R2D_P<3>	89 88 71	AN15	PEX_RX3	PEX_TX3	AL16	PEG_D2R_C_P<3>	71 89
PEG_R2D_N<3>	89 88 71	AM15	PEX_RX3*	PEX_TX3*	AK16	PEG_D2R_C_N<3>	71 89
PEG_R2D_P<4>	89 71	AN17	PEX_RX4	PEX_TX4	AK17	PEG_D2R_C_P<4>	71 89
PEG_R2D_N<4>	89 71	AM17	PEX_RX4*	PEX_TX4*	AJ17	PEG_D2R_C_N<4>	71 89
PEG_R2D_P<5>	89 88 71	AP17	PEX_RX5	PEX_TX5	AH17	PEG_D2R_C_P<5>	71 89
PEG_R2D_N<5>	89 88 71	AP18	PEX_RX5*	PEX_TX5*	AG17	PEG_D2R_C_N<5>	71 89
PEG_R2D_P<6>	89 71	AN18	PEX_RX6	PEX_TX6	AK18	PEG_D2R_C_P<6>	71 89
PEG_R2D_N<6>	89 71	AM18	PEX_RX6*	PEX_TX6*	AJ18	PEG_D2R_C_N<6>	71 89
PEG_R2D_P<7>	89 88 71	AN20	PEX_RX7	PEX_TX7	AL19	PEG_D2R_C_P<7>	71 89
PEG_R2D_N<7>	89 88 71	AM20	PEX_RX7*	PEX_TX7*	AK19	PEG_D2R_C_N<7>	71 89
NC		AP20	PEX_RX8	PEX_TX8	AK20	NC	
NC		AP21	PEX_RX8*	PEX_TX8*	AJ20	NC	
NC		AN21	PEX_RX9	PEX_TX9	AH20	NC	
NC		AM21	PEX_RX9*	PEX_TX9*	AG20	NC	
NC		AN23	PEX_RX10	PEX_TX10	AK21	NC	
NC		AM23	PEX_RX10*	PEX_TX10*	AJ21	NC	
NC		AP23	PEX_RX11	PEX_TX11	AL22	NC	
NC		AP24	PEX_RX11*	PEX_TX11*	AK22	NC	
NC		AN24	PEX_RX12	PEX_TX12	AK23	NC	
NC		AM24	PEX_RX12*	PEX_TX12*	AJ23	NC	
NC		AN26	PEX_RX13	PEX_TX13	AH23	NC	
NC		AM26	PEX_RX13*	PEX_TX13*	AG23	NC	
NC		AP26	PEX_RX14	PEX_TX14	AK24	NC	
NC		AP27	PEX_RX14*	PEX_TX14*	AJ24	NC	
NC		AN27	PEX_RX15	PEX_TX15	AL25	NC	
NC		AM27	PEX_RX15*	PEX_TX15*	AK25	NC	
PEG_CLK100M_P	92 17	AL13	PEX_REFCLK	PEX_TSTCLK_OUT	AJ26	PEX_TSTCLK_O_P	95 92
PEG_CLK100M_N	92 17	AK13	PEX_REFCLK*	PEX_TSTCLK_OUT*	AK26	PEX_TSTCLK_O_N	95 92
GPU_RESET_L	78 9	AJ12	PEX_RST*	PEX_TERMP	AJ29		
PEX_CLKREQ_L_R	78 71	AK12	PEX_CLKREQ*	PEX_SVDD_3V3	AG12		
NC		AJ11	PEX_WAKE*				

R8000 0 MF 5% 1/20W 201 (GPU_RESET_L → GPU_RESET_R_L)

=PP3V3_GPU_VDD33 79 78 77 8

R8001 10K 1% 1/20W MF 201 (PEX_CLKREQ_L_R 78 71)

NOSTUFF R8002 200 1% 1/20W MF 201 (PEX_TSTCLK_O_P)

R8005 2.49K 1% 1/20W MF 201 (GPU_PEX_TERMP)

PP3V3_GPU_PEX_PLL_HVDD 79

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE: KEPLER PCI-E

Apple Inc.

DRAWING NUMBER: 051-9589 SIZE: D
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OMIT_TABLE

=PP1V35_GPU_FBVDDQ
76 75 72 8

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=PP1V35_GPU_FBVDDQ
8 72 75 76

AA27			H18
AA30			H19
AB27			H20
AB33			H21
AC27			H22
AD27			H23
AE27			H24
AF27			H8
AG27			H9
B13			L27
B16	FBVDDQ	FBVDDQ	M27
B19			N27
E13			P27
E16			R27
E19			T27
H10			T30
H11			T33
H12			V27
H13			W27
H14			W30
H15			W33
H16			Y27

OMIT_TABLE

=PPVCORE_GPU
79 72 8

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=PPVCORE_GPU
8 72 79

AA12			V17
AA14			V18
AA16			V20
AA19			V22
AA21			W12
AA23			W14
AB13			W16
AB15		VDD	W19
AB17			W21
AB18			W23
AB20			Y13
AB22			Y15
AC12			Y17
AC14			Y18
AC16			Y20
AC19			Y22
AC21			U1 NC
AC23			U2 NC
M12			U3 NC
M14			U4 NC
M16			U5 NC
M19			U6 NC
M21			U7 NC
M23			U8 NC
N13			V1 NC
N15			V2 NC
N17		VDD	V3 NC
N18			V4 NC
N20			V5 NC
N22			V6 NC
P12			V7 NC
P14			V8 NC
P16			W2 NC
P19			W3 NC
P21			W4 NC
P23			W5 NC
R13			W7 NC
R15		XVDD	W8 NC
R17			Y1 NC
R18			Y2 NC
R20			Y3 NC
R22			Y4 NC
T12			Y5 NC
T14			Y6 NC
T16			Y7 NC
T19			Y8 NC
T21			AA1 NC
T23			AA2 NC
U13			AA3 NC
U15			AA4 NC
U17			AA5 NC
U18			AA6 NC
U20			AA7 NC
U22			AA8 NC
V13			
V15			

Page Notes

Power aliases required by this page:

- =PPVCORE_GPU
- =PP1V35_GPU_FBVDDQ

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

=PPVCORE_GPU
79 72 8

EDP = 30 A

NOSTUFF C8161 47UF 20% 4V X6S 0805	NOSTUFF CRITICAL C8198 22UF 20% 4V X6S-CERM 0603	NOSTUFF CRITICAL C8199 22UF 20% 4V X6S-CERM 0603	CRITICAL C8162 20UF 20% 2V X6T-CERM 0402	CRITICAL C8163 20UF 20% 2V X6T-CERM 0402	CRITICAL C8164 20UF 20% 2V X6T-CERM 0402	CRITICAL C8165 20UF 20% 2V X6T-CERM 0402	NOSTUFF CRITICAL C8182 20UF 20% 2V X6T-CERM 0402	NOSTUFF CRITICAL C8183 20UF 20% 2V X6T-CERM 0402	C8166 10UF 20% 4V X6S-CERM 0402-1 C8167 10UF 20% 4V X6S-CERM 0402-1
CRITICAL C8145 20UF 20% 2V X6T-CERM 0402	CRITICAL C8146 20UF 20% 2V X6T-CERM 0402	CRITICAL C8147 20UF 20% 2V X6T-CERM 0402	CRITICAL C8148 20UF 20% 2V X6T-CERM 0402	NOSTUFF CRITICAL C8149 20UF 20% 2V X6T-CERM 0402	NOSTUFF CRITICAL C8150 20UF 20% 2V X6T-CERM 0402	NOSTUFF CRITICAL C8151 20UF 20% 2V X6T-CERM 0402			
C8168 10UF 20% 4V X6S-CERM 0402-1	C8169 10UF 20% 4V X6S-CERM 0402-1	C8170 10UF 20% 4V X6S-CERM 0402-1	C8171 10UF 20% 4V X6S-CERM 0402-1	C8172 10UF 20% 4V X6S-CERM 0402-1	C8173 10UF 20% 4V X6S-CERM 0402-1	C8174 10UF 20% 4V X6S-CERM 0402-1	C8175 10UF 20% 4V X6S-CERM 0402-1	C8176 10UF 20% 4V X6S-CERM 0402-1	C8177 10UF 20% 4V X6S-CERM 0402-1
C8178 10UF 20% 4V X6S-CERM 0402-1	C8179 10UF 20% 4V X6S-CERM 0402-1	C8180 10UF 20% 4V X6S-CERM 0402-1	C8181 10UF 20% 4V X6S-CERM 0402-1	C8184 10UF 20% 4V X6S-CERM 0402-1	C8185 10UF 20% 4V X6S-CERM 0402-1	CRITICAL C8186 1UF 20% 4V CERM-X6S 0201	CRITICAL C8187 1UF 20% 4V CERM-X6S 0201	CRITICAL C8188 1UF 20% 4V CERM-X6S 0201	CRITICAL C8189 1UF 20% 4V CERM-X6S 0201
CRITICAL C8190 1UF 20% 4V CERM-X6S 0201	C8191 0.1UF 10% 6.3V X6S 0201	C8192 0.1UF 10% 6.3V X6S 0201	C8193 0.1UF 10% 6.3V X6S 0201	C8194 0.1UF 10% 6.3V X6S 0201	C8195 0.1UF 10% 6.3V X6S 0201	C8196 1000PF 10% 16V X7R-CERM 0201	C8197 1000PF 10% 16V X7R-CERM 0201		

GPU VCORE DE-COUPLING

NOTE: ATLEAST 2 GND VIAS & 2 POWER VIAS PER CAP

=PP1V35_GPU_FBVDDQ
76 75 72 8

GPU FB DE-COUPLING

EDP = 6500 MA

C8125 20UF 20% 2V X6T-CERM 0402	C8126 20UF 20% 2V X6T-CERM 0402	C8127 20UF 20% 2V X6T-CERM 0402	C8128 20UF 20% 2V X6T-CERM 0402	C8101 10UF 20% 4V X6S-CERM 0402-1	C8102 10UF 20% 4V X6S-CERM 0402-1	C8103 10UF 20% 4V X6S-CERM 0402-1	C8104 10UF 20% 4V X6S-CERM 0402-1
C8105 4.7UF 20% 6.3V X6S 0402	C8106 4.7UF 20% 6.3V X6S 0402	C8107 4.7UF 20% 6.3V X6S 0402	C8108 4.7UF 20% 6.3V X6S 0402	C8109 4.7UF 20% 6.3V X6S 0402	C8110 4.7UF 20% 6.3V X6S 0402	C8111 1UF 20% 4V CERM-X6S 0201	C8112 1UF 20% 4V CERM-X6S 0201	C8113 1UF 20% 4V CERM-X6S 0201	C8114 1UF 20% 4V CERM-X6S 0201
C8115 0.1UF 10% 6.3V X6S 0201	C8118 0.1UF 10% 6.3V X6S 0201	C8119 0.1UF 10% 6.3V X6S 0201	C8120 0.1UF 10% 6.3V X6S 0201	C8121 0.1UF 10% 6.3V X6S 0201	C8122 0.1UF 10% 6.3V X6S 0201	C8123 0.1UF 10% 6.3V X6S 0201	C8124 0.1UF 10% 6.3V X6S 0201

SYNC_MASTER=D2_SEAN SYNC_DATE=03/05/2012

PAGE TITLE

KEPLER CORE/FB POWER

Apple Inc.

DRAWING NUMBER 051-9589 SIZE D

REVISION 4.18.0

BRANCH

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NOTE:GDDR5 MODE H MAPPING

OMIT_TABLE

U8000
NV-GK107
BGA
(3 OF 10)
MEM INTERFACE A

FB_A0_DQ<0>	L28	FBA_D0	U30	FB_A0_CS_L	OUT	75 95
FB_A0_DQ<1>	M29	FBA_D1	T31	FB_A0_A<3>	OUT	75 95
FB_A0_DQ<2>	L29	FBA_D2	U29	FB_A0_A<2>	OUT	75 95
FB_A0_DQ<3>	M28	FBA_D3	R34	FB_A0_A<4>	OUT	75 95
FB_A0_DQ<4>	N31	FBA_D4	R33	FB_A0_A<5>	OUT	75 95
FB_A0_DQ<5>	P29	FBA_D5	U32	FB_A0_WE_L	OUT	75 95
FB_A0_DQ<6>	R29	FBA_D6	U33	FB_A0_A<7>	OUT	75 95
FB_A0_DQ<7>	P28	FBA_D7	U28	FB_A0_A<6>	OUT	75 95
FB_A0_DQ<8>	J28	FBA_D8	V28	FB_A0_ABI_L	OUT	75 95
FB_A0_DQ<9>	H29	FBA_D9	V29	FB_A0_A<8>	OUT	75 95
FB_A0_DQ<10>	J29	FBA_D10	V30	FB_A0_A<0>	OUT	75 95
FB_A0_DQ<11>	H28	FBA_D11	U34	FB_A0_A<1>	OUT	75 95
FB_A0_DQ<12>	G29	FBA_D12	U31	FB_A0_RAS_L	OUT	75 95
FB_A0_DQ<13>	E31	FBA_D13	V34	FB_A0_RESET_L	OUT	73 75 95
FB_A0_DQ<14>	E32	FBA_D14	V33	FB_A0_CKE_L	OUT	73 75 95
FB_A0_DQ<15>	F30	FBA_D15	Y32	FB_A0_CAS_L	OUT	75 95
FB_A0_DQ<16>	C34	FBA_D16	AA31	FB_A1_CS_L	OUT	75 95
FB_A0_DQ<17>	D32	FBA_D17	AA29	FB_A1_A<3>	OUT	75 95
FB_A0_DQ<18>	B33	FBA_D18	AA28	FB_A1_A<2>	OUT	75 95
FB_A0_DQ<19>	C33	FBA_D19	AC34	FB_A1_A<4>	OUT	75 95
FB_A0_DQ<20>	F33	FBA_D20	AC33	FB_A1_A<5>	OUT	75 95
FB_A0_DQ<21>	F32	FBA_D21	AA32	FB_A1_WE_L	OUT	75 95
FB_A0_DQ<22>	H33	FBA_D22	AA33	FB_A1_A<7>	OUT	75 95
FB_A0_DQ<23>	H32	FBA_D23	Y28	FB_A1_A<6>	OUT	75 95
FB_A0_DQ<24>	P34	FBA_D24	Y29	FB_A1_ABI_L	OUT	75 95
FB_A0_DQ<25>	P32	FBA_D25	W31	FB_A1_A<8>	OUT	75 95
FB_A0_DQ<26>	P31	FBA_D26	Y30	FB_A1_A<0>	OUT	75 95
FB_A0_DQ<27>	P33	FBA_D27	AA34	FB_A1_A<1>	OUT	75 95
FB_A0_DQ<28>	L31	FBA_D28	Y31	FB_A1_RAS_L	OUT	75 95
FB_A0_DQ<29>	L34	FBA_D29	Y34	FB_A1_RESET_L	OUT	73 75 95
FB_A0_DQ<30>	L32	FBA_D30	Y33	FB_A1_CKE_L	OUT	73 75 95
FB_A0_DQ<31>	L33	FBA_D31	V31	FB_A1_CAS_L	OUT	75 95
FB_A1_DQ<0>	AG28	FBA_D32				
FB_A1_DQ<1>	AF29	FBA_D33				
FB_A1_DQ<2>	AG29	FBA_D34				
FB_A1_DQ<3>	AF28	FBA_D35				
FB_A1_DQ<4>	AD30	FBA_D36				
FB_A1_DQ<5>	AD29	FBA_D37				
FB_A1_DQ<6>	AC29	FBA_D38				
FB_A1_DQ<7>	AD28	FBA_D39				
FB_A1_DQ<8>	AJ29	FBA_D40				
FB_A1_DQ<9>	AK29	FBA_D41				
FB_A1_DQ<10>	AJ30	FBA_D42				
FB_A1_DQ<11>	AK28	FBA_D43				
FB_A1_DQ<12>	AM29	FBA_D44				
FB_A1_DQ<13>	AM31	FBA_D45				
FB_A1_DQ<14>	AN29	FBA_D46				
FB_A1_DQ<15>	AM30	FBA_D47				
FB_A1_DQ<16>	AN31	FBA_D48				
FB_A1_DQ<17>	AN32	FBA_D49				
FB_A1_DQ<18>	AP30	FBA_D50				
FB_A1_DQ<19>	AP32	FBA_D51				
FB_A1_DQ<20>	AM33	FBA_D52				
FB_A1_DQ<21>	AL31	FBA_D53				
FB_A1_DQ<22>	AK33	FBA_D54				
FB_A1_DQ<23>	AK32	FBA_D55				
FB_A1_DQ<24>	AD34	FBA_D56				
FB_A1_DQ<25>	AD32	FBA_D57				
FB_A1_DQ<26>	AC30	FBA_D58				
FB_A1_DQ<27>	AD33	FBA_D59				
FB_A1_DQ<28>	AF31	FBA_D60				
FB_A1_DQ<29>	AG34	FBA_D61				
FB_A1_DQ<30>	AG32	FBA_D62				
FB_A1_DQ<31>	AG33	FBA_D63				
FB_A0_WCLK_P<0>	K31	FBA_WCK01	R30	FB_A0_CLK_P	OUT	75 95
FB_A0_WCLK_N<0>	L30	FBA_WCK01*	R31	FB_A0_CLK_N	OUT	75 95
FB_A1_WCLK_P<1>	H34	FBA_WCK23	AB31	FB_A1_CLK_P	OUT	75 95
FB_A1_WCLK_N<1>	J34	FBA_WCK23*	AC31	FB_A1_CLK_N	OUT	75 95
FB_A1_WCLK_P<0>	AG30	FBA_WCK45				
FB_A1_WCLK_N<0>	AG31	FBA_WCK45*				
FB_A1_WCLK_P<1>	AJ34	FBA_WCK67				
FB_A1_WCLK_N<1>	AK34	FBA_WCK67*				
NC	J30	FBA_WCKB01	P30	FB_A0_DBI_L<0>	BI	75 95
NC	J31	FBA_WCKB01*	F31	FB_A0_DBI_L<1>	BI	75 95
NC	J32	FBA_WCKB23	F34	FB_A0_DBI_L<2>	BI	75 95
NC	J33	FBA_WCKB23*	M32	FB_A0_DBI_L<3>	BI	75 95
NC	AH31	FBA_WCKB45	AD31	FB_A1_DBI_L<0>	BI	75 95
NC	AJ31	FBA_WCKB45*	AL29	FB_A1_DBI_L<1>	BI	75 95
NC	AJ32	FBA_WCKB67	AM32	FB_A1_DBI_L<2>	BI	75 95
NC	AJ33	FBA_WCKB67*	AF34	FB_A1_DBI_L<3>	BI	75 95

FBA_DQS_RN0	M30	NC	
FBA_DQS_RN1	H30	NC	
FBA_DQS_RN2	E34	NC	
FBA_DQS_RN3	M34	NC	
FBA_DQS_RN4	AF30	NC	
FBA_DQS_RN5	AK31	NC	
FBA_DQS_RN6	AM34	NC	
FBA_DQS_RN7	AF32	NC	
FBA_DQS_WP0	M31	FB_A0_EDC<0>	IN 75 95
FBA_DQS_WP1	G31	FB_A0_EDC<1>	IN 75 95
FBA_DQS_WP2	E33	FB_A0_EDC<2>	IN 75 95
FBA_DQS_WP3	M33	FB_A0_EDC<3>	IN 75 95
FBA_DQS_WP4	AE31	FB_A1_EDC<0>	IN 75 95
FBA_DQS_WP5	AK30	FB_A1_EDC<1>	IN 75 95
FBA_DQS_WP6	AN33	FB_A1_EDC<2>	IN 75 95
FBA_DQS_WP7	AF33	FB_A1_EDC<3>	IN 75 95
FB_DLL_AVDD	K27	PP1V05_GPU_FB_DLL_AVDD 73	
FBA_PLL_AVDD	U27	PP1V05_GPU_FB_PLL_AVDD 73	
FBA_DEBUG	R28	GPU_FBA_DEBUG0	
FBA_DEBUG	AC28	GPU_FBA_DEBUG1	
FBA_CAL_PD_VDDQ	J27	FB_CAL_PD_VDDQ 73	
FBA_CAL_PU_GND	H27	FB_CAL_PU_GND 73	
FBA_CAL_TERM_GND	H25	FB_CAL_TERM_GND 1	R8201 2 60.4 1% 1/20W MF 201 PLACE_NEAR=U8000.H25:8.4MM
FB_CLAMP	E1 82	FB_CLAMP	R8261 1 10K 1% 1/20W 201 2 MF
FBA_CMD_RFU	R32	NC	
FBA_CMD_RFU	AC32	NC	
FB_VDDQ_SENSE	F1	GPU_FBVDDQ_SENSE	OUT 74 97
FB_GND_SENSE	F2	GPU_FBGND_SENSE	OUT 74 97

PLACE CLOSE TO BGA

73 FB_CAL_PU_GND — R8204 40.2 1% 1/20W MF 201 — PLACE_NEAR=U8000.H27:8.4MM

=PP1V35_GPU_S0_FB 8 73 — R8205 40.2 1% 1/20W MF 201 — PLACE_NEAR=U8000.J27:8.4MM — FB_CAL_PD_VDDQ 73

R8250 10K 1% 1/20W MF 201 — 95 75 73 FB_A0_RESET_L

R8251 10K 1% 1/20W MF 201 — 95 75 73 FB_A1_RESET_L

FB_A0_CKE_L 73 75 95 — R8252 10K 1% 1/20W MF 201

FB_A1_CKE_L 73 75 95 — R8253 10K 1% 1/20W MF 201

=PP1V35_GPU_S0_FB 8 73

R8203 60.4 1% 1/20W MF 201

R8202 60.4 1% 1/20W MF 201

R8270 100 5% 1/20W MF 201

=PP1V35_GPU_S0_FB 8 73

NOSTUFF R8258 1.33K 1% 1/20W MF 201 — PLACE_NEAR=U8000.H26:8.4MM

FB_VREF 73

NOSTUFF R8259 1.33K 1% 1/20W MF 201 — PLACE_NEAR=U8000.H26:8.4MM

NOSTUFF C8260 0.1UF 10% 6.3V X6S 0201

FB VREF GEN (TEST ONLY)

R8271 100 5% 1/20W MF 201

OMIT_TABLE

U8000
NV-GK107
BGA
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MEM INTRERFACE B

FB_B0_DQ<0>	G9	FBB_D0	D13	FB_B0_CS_L	OUT	76 95
FB_B0_DQ<1>	E9	FBB_D1	E14	FB_B0_A<3>	OUT	76 95
FB_B0_DQ<2>	G8	FBB_D2	F14	FB_B0_A<2>	OUT	76 95
FB_B0_DQ<3>	F9	FBB_D3	A12	FB_B0_A<4>	OUT	76 95
FB_B0_DQ<4>	F11	FBB_D4	B12	FB_B0_A<5>	OUT	76 95
FB_B0_DQ<5>	G11	FBB_D5	C14	FB_B0_WE_L	OUT	76 95
FB_B0_DQ<6>	F12	FBB_D6	B14	FB_B0_A<7>	OUT	76 95
FB_B0_DQ<7>	G12	FBB_D7	G15	FB_B0_A<6>	OUT	76 95
FB_B0_DQ<8>	G6	FBB_D8	F15	FB_B0_ABI_L	OUT	76 95
FB_B0_DQ<9>	F5	FBB_D9	E15	FB_B0_A<8>	OUT	76 95
FB_B0_DQ<10>	E6	FBB_D10	D15	FB_B0_A<0>	OUT	76 95
FB_B0_DQ<11>	F6	FBB_D11	A14	FB_B0_A<1>	OUT	76 95
FB_B0_DQ<12>	F4	FBB_D12	D14	FB_B0_RAS_L	OUT	76 95
FB_B0_DQ<13>	G4	FBB_D13	A15	FB_B0_RESET_L	OUT	73 76 95
FB_B0_DQ<14>	E2	FBB_D14	B15	FB_B0_CKE_L	OUT	73 76 95
FB_B0_DQ<15>	F3	FBB_D15	C17	FB_B0_CAS_L	OUT	76 95
FB_B0_DQ<16>	C2	FBB_D16	D18	FB_B1_CS_L	OUT	76 95
FB_B0_DQ<17>	D4	FBB_D17	E18	FB_B1_A<3>	OUT	76 95 79 73 8
FB_B0_DQ<18>	D3	FBB_D18	F18	FB_B1_A<2>	OUT	76 95
FB_B0_DQ<19>	C1	FBB_D19	A20	FB_B1_A<4>	OUT	76 95
FB_B0_DQ<20>	B3	FBB_D20	B20	FB_B1_A<5>	OUT	76 95
FB_B0_DQ<21>	C4	FBB_D21	C18	FB_B1_WE_L	OUT	76 95
FB_B0_DQ<22>	B5	FBB_D22	B18	FB_B1_A<7>	OUT	76 95
FB_B0_DQ<23>	C5	FBB_D23	G18	FB_B1_A<6>	OUT	76 95
FB_B0_DQ<24>	A11	FBB_D24	G17	FB_B1_ABI_L	OUT	76 95
FB_B0_DQ<25>	C11	FBB_D25	F17	FB_B1_A<8>	OUT	76 95
FB_B0_DQ<26>	D11	FBB_D26	D16	FB_B1_A<0>	OUT	76 95
FB_B0_DQ<27>	B11	FBB_D27	A18	FB_B1_A<1>	OUT	76 95
FB_B0_DQ<28>	D8	FBB_D28	D17	FB_B1_RAS_L	OUT	76 95
FB_B0_DQ<29>	A8	FBB_D29	A17	FB_B1_RESET_L	OUT	73 76 95
FB_B0_DQ<30>	C8	FBB_D30	B17	FB_B1_CKE_L	OUT	73 76 95
FB_B0_DQ<31>	B8	FBB_D31	E17	FB_B1_CAS_L	OUT	76 95
FB_B1_DQ<0>	F24	FBB_D32				
FB_B1_DQ<1>	G23	FBB_D33				
FB_B1_DQ<2>	E24	FBB_D34				
FB_B1_DQ<3>	G24	FBB_D35				
FB_B1_DQ<4>	D21	FBB_D36				
FB_B1_DQ<5>	E21	FBB_D37				
FB_B1_DQ<6>	G21	FBB_D38				
FB_B1_DQ<7>	F21	FBB_D39				
FB_B1_DQ<8>	G27	FBB_D40				
FB_B1_DQ<9>	D27	FBB_D41				
FB_B1_DQ<10>	G26	FBB_D42				
FB_B1_DQ<11>	E27	FBB_D43				
FB_B1_DQ<12>	E29	FBB_D44				
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FB_B1_DQ<25>	C23	FBB_D57				
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FB_B1_DQ<27>	C21	FBB_D59				
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FB_B1_DQ<29>	C24	FBB_D61				
FB_B1_DQ<30>	B26	FBB_D62				
FB_B1_DQ<31>	C26	FBB_D63				
FB_B0_WCLK_P<0>	F8	FBB_WCK01	D12	FB_B0_CLK_P	OUT	76 95
FB_B0_WCLK_N<0>	E8	FBB_WCK01*	E12	FB_B0_CLK_N	OUT	76 95
FB_B0_WCLK_P<1>	A5	FBB_WCK23	E20	FB_B1_CLK_P	OUT	76 95
FB_B0_WCLK_N<1>	A6	FBB_WCK23*	F20	FB_B1_CLK_N	OUT	76 95
FB_B1_WCLK_P<0>	D24	FBB_WCK45				
FB_B1_WCLK_N<0>	D25	FBB_WCK45*				
FB_B1_WCLK_P<1>	B27	FBB_WCK67				
FB_B1_WCLK_N<1>	C27	FBB_WCK67*				
NC	D6	FBB_WCKB01	E11	FB_B0_DBI_L<0>	BI	76 95
NC	D7	FBB_WCKB01*	E3	FB_B0_DBI_L<1>	BI	76 95
NC	C6	FBB_WCKB23	A3	FB_B0_DBI_L<2>	BI	76 95
NC	B6	FBB_WCKB23*	C9	FB_B0_DBI_L<3>	BI	76 95
NC	F26	FBB_WCKB45	F23	FB_B1_DBI_L<0>	BI	76 95
NC	E26	FBB_WCKB45*	F27	FB_B1_DBI_L<1>	BI	76 95
NC	A26	FBB_WCKB67	C30	FB_B1_DBI_L<2>	BI	76 95
NC	A27	FBB_WCKB67*	A24	FB_B1_DBI_L<3>	BI	76 95

FBB_DQS_RN0	D9	NC			
FBB_DQS_RN1	E4	NC			
FBB_DQS_RN2	B2	NC			
FBB_DQS_RN3	A9	NC			
FBB_DQS_RN4	D22	NC			
FBB_DQS_RN5	D28	NC			
FBB_DQS_RN6	A30	NC			
FBB_DQS_RN7	B23	NC			
FBB_DQS_WP0	D10	FB_B0_EDC<0>	IN	76 95	
FBB_DQS_WP1	D5	FB_B0_EDC<1>	IN	76 95	
FBB_DQS_WP2	C3	FB_B0_EDC<2>	IN	76 95	
FBB_DQS_WP3	B9	FB_B0_EDC<3>	IN	76 95	
FBB_DQS_WP4	E23	FB_B1_EDC<0>	IN	76 95	
FBB_DQS_WP5	E28	FB_B1_EDC<1>	IN	76 95	
FBB_DQS_WP6	B30	FB_B1_EDC<2>	IN	76 95	
FBB_DQS_WP7	A23	FB_B1_EDC<3>	IN	76 95	
FBB_PLL_AVDD	H17	73 PP1V05_GPU_FB_PLL_AVDD			
FBB_DEBUG0	G14	GPU_FBB_DEBUG0 73			
FBB_DEBUG1	G20	GPU_FBB_DEBUG1 73			
FB_VREF	H26	FB_VREF 73			
FBB_CMD_RFU0	C12	NC			
FBB_CMD_RFU1	C20	NC			

C8206 1UF 20% 4V CERM-X6S 0201

C8207 0.1UF 10% 6.3V X6S 0201

=PP1V35_GPU_S0_FB 8 73 — R8206 60.4 1% 1/20W MF 201 — GPU_FBB_DEBUG0 73

R8207 60.4 1% 1/20W MF 201 — GPU_FBB_DEBUG1 73

R8254 10K 1% 1/20W MF 201 — 95 76 73 FB_B0_RESET_L

R8255 10K 1% 1/20W MF 201 — 95 76 73 FB_B1_RESET_L

FB_B0_CKE_L 73 76 95 — R8256 10K 1% 1/20W MF 201

FB_B1_CKE_L 73 76 95 — R8257 10K 1% 1/20W MF 201

MEM VREFC & VREFD SWITCH

FB_SW_LEG 76 75 OUT — Q8265 SSM3K15FV SOD-VESM-HF — GPU_ALT_VREF IN 78

L8201 FERR-220-OHM-2A 0603 CRITICAL ESR = 0.050OHM
=PP1V05_GPU_PEX_IOVDD 8 73 79 — PP1V05_GPU_FB_PLL_AVDD 73
MIN_LINE_WIDTH=0.6 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=1.05V

C8201 20UF 20% 2V X6T-CERM 0402

C8202 1UF 20% 4V CERM-X6S 0201

C8203 0.1UF 10% 6.3V X6S 0201

FB PLL & DLL VDD

L8202 FERR-220-OHM-2A 0603 CRITICAL ESR = 0.050OHM
=PP1V05_GPU_PEX_IOVDD — PP1V05_GPU_FB_DLL_AVDD 73
MIN_LINE_WIDTH=0.6 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=1.05V

C8208 20UF 20% 2V X6T-CERM 0402

C8204 1UF 20% 4V CERM-X6S 0201

C8205 0.1UF 10% 6.3V X6S 0201

Page Notes

Power aliases required by this page:
- =PP1V35_GPU_S0_FB
- =PP1V05_GPU_PEX_IOVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

SYNC_MASTER=D2_SEAN	SYNC_DATE=03/05/2012
PAGE TITLE	KEPLER FRAME BUFFER I/F
Apple Inc.	DRAWING NUMBER 051-9589 SIZE D
	REVISION 4.18.0
	BRANCH
	PAGE 82 OF 132
	SHEET 73 OF 99

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GPU FB SUPPLY

VOUT = 1.5V / 1.35V
13A MAX OUTPUT
F = 500 KHZ

GPIO(16)	VID1	VID0	FBVDD
	0	0	1.5V
	1	0	1.35V

GPU 1V05 SUPPLY

VOUT = 1.05V
5.3A MAX OUTPUT
F = 500 KHZ

Vout = 0.5V * (1 + Ra / Rb)

SYNC_MASTER=D2_SEAN	SYNC_DATE=03/05/2012
PAGE TITLE	1V05 GPU / 1V35 FB POWER SUPPLY
Apple Inc.	DRAWING NUMBER 051-9589 SIZE D
	REVISION 4.18.0
	BRANCH
	PAGE 83 OF 132
	SHEET 74 OF 99

Page Notes

Power aliases required by this page:
- =PP1V5R1V35_S0_FB_VDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:

CK TERMINATION - A0

R8401 40.2 1% 1/20W MF 201 — FB_A0_CLK_P — FBA0_CK_MID — R8402 40.2 1% 1/20W MF 201 — FB_A0_CLK_N
C8490 0.01UF 10% 10V X7R-CERM 0201
PLACE_NEAR=U8400.J11:8.4MM
PLACE_NEAR=U8400.J12:8.4MM

CK TERMINATION - A1

R8451 40.2 1% 1/20W MF 201 — FB_A1_CLK_P — FBA1_CK_MID — R8452 40.2 1% 1/20W MF 201 — FB_A1_CLK_N
C8491 0.01UF 10% 10V X7R-CERM 0201
PLACE_NEAR=U8450.J11:8.4MM
PLACE_NEAR=U8450.J12:8.4MM

R8400 120 1% 1/20W MF 201
R8404 120 1% 1/20W MF 201
R8403 120 1% 1/20W MF 201

U8400
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(1 OF 2)

OMIT_TABLE

FB_A0_A<2>	H11	BA0/A2	
FB_A0_A<5>	K10	BA1/A5	
FB_A0_A<4>	K11	BA2/A4	
FB_A0_A<3>	H10	BA3/A3	
FB_A0_A<7>	K4	A8/A7	
FB_A0_A<1>	H5	A9/A1	
FB_A0_A<0>	H4	A10/A0	
FB_A0_A<6>	K5	A11/A6	
FB_A0_CKE_L	J3	CKE*	
FB_A0_CLK_P	J12	CK	
FB_A0_CLK_N	J11	CK*	
FB_A0_CS_L	G12	CS*	
FB_A0_WE_L	L12	WE*	
FB_A0_CAS_L	L3	CAS*	
FB_A0_RAS_L	G3	RAS*	
FB_A0_ZQ	J13	ZQ	
FB_A0_MF	J1	MF (MF=0)	
FB_A0_SEN	J10	SEN	
FB_A0_RESET_L	J2	RESET*	
FB_A0_ABI_L	J4	ABI*	
FB_A0_EDC<0>	C2	EDC0	
FB_A0_EDC<1>	C13	EDC1	
FB_A0_EDC<2>	R13	EDC2	
FB_A0_EDC<3>	R2	EDC3	
FB_A0_WCLK_P<0>	D4	WCK01	
FB_A0_WCLK_N<0>	D5	WCK01*	
FB_A0_WCLK_P<1>	P4	WCK23	
FB_A0_WCLK_N<1>	P5	WCK23*	

DBI0*	D2	FB_A0_DBI_L<0>	
DBI1*	D13	FB_A0_DBI_L<1>	
DBI2*	P13	FB_A0_DBI_L<2>	
DBI3*	P2	FB_A0_DBI_L<3>	
DQ0	A4	FB_A0_DQ<0>	
DQ1	A2	FB_A0_DQ<1>	
DQ2	B4	FB_A0_DQ<2>	
DQ3	B2	FB_A0_DQ<3>	
DQ4	E4	FB_A0_DQ<4>	
DQ5	E2	FB_A0_DQ<5>	
DQ6	F4	FB_A0_DQ<6>	
DQ7	F2	FB_A0_DQ<7>	
DQ8	A11	FB_A0_DQ<8>	
DQ9	A13	FB_A0_DQ<9>	
DQ10	B11	FB_A0_DQ<10>	
DQ11	B13	FB_A0_DQ<11>	
DQ12	E11	FB_A0_DQ<12>	
DQ13	E13	FB_A0_DQ<13>	
DQ14	F11	FB_A0_DQ<14>	
DQ15	F13	FB_A0_DQ<15>	
DQ16	U11	FB_A0_DQ<16>	
DQ17	U13	FB_A0_DQ<17>	
DQ18	T11	FB_A0_DQ<18>	
DQ19	T13	FB_A0_DQ<19>	
DQ20	N11	FB_A0_DQ<20>	
DQ21	N13	FB_A0_DQ<21>	
DQ22	M11	FB_A0_DQ<22>	
DQ23	M13	FB_A0_DQ<23>	
DQ24	U4	FB_A0_DQ<24>	
DQ25	U2	FB_A0_DQ<25>	
DQ26	T4	FB_A0_DQ<26>	
DQ27	T2	FB_A0_DQ<27>	
DQ28	N4	FB_A0_DQ<28>	
DQ29	N2	FB_A0_DQ<29>	
DQ30	M4	FB_A0_DQ<30>	
DQ31	M2	FB_A0_DQ<31>	
NC	A5, J5, U5	NC	FB_A0_A<8>

U8450
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(1 OF 2)

OMIT_TABLE

FB_A1_A<2>	H11	BA0/A2	
FB_A1_A<5>	K10	BA1/A5	
FB_A1_A<4>	K11	BA2/A4	
FB_A1_A<3>	H10	BA3/A3	
FB_A1_A<7>	K4	A8/A7	
FB_A1_A<1>	H5	A9/A1	
FB_A1_A<0>	H4	A10/A0	
FB_A1_A<6>	K5	A11/A6	
FB_A1_CKE_L	J3	CKE*	
FB_A1_CLK_P	J12	CK	
FB_A1_CLK_N	J11	CK*	
FB_A1_CS_L	G12	CS*	
FB_A1_WE_L	L12	WE*	
FB_A1_CAS_L	L3	CAS*	
FB_A1_RAS_L	G3	RAS*	
FB_A1_ZQ	J13	ZQ	
FB_A1_MF	J1	MF (MF=0)	
FB_A1_SEN	J10	SEN	
FB_A1_RESET_L	J2	RESET*	
FB_A1_ABI_L	J4	ABI*	
FB_A1_EDC<0>	C2	EDC0	
FB_A1_EDC<1>	C13	EDC1	
FB_A1_EDC<2>	R13	EDC2	
FB_A1_EDC<3>	R2	EDC3	
FB_A1_WCLK_P<0>	D4	WCK01	
FB_A1_WCLK_N<0>	D5	WCK01*	
FB_A1_WCLK_P<1>	P4	WCK23	
FB_A1_WCLK_N<1>	P5	WCK23*	

DBI0*	D2	FB_A1_DBI_L<0>	
DBI1*	D13	FB_A1_DBI_L<1>	
DBI2*	P13	FB_A1_DBI_L<2>	
DBI3*	P2	FB_A1_DBI_L<3>	
DQ0	A4	FB_A1_DQ<0>	
DQ1	A2	FB_A1_DQ<1>	
DQ2	B4	FB_A1_DQ<2>	
DQ3	B2	FB_A1_DQ<3>	
DQ4	E4	FB_A1_DQ<4>	
DQ5	E2	FB_A1_DQ<5>	
DQ6	F4	FB_A1_DQ<6>	
DQ7	F2	FB_A1_DQ<7>	
DQ8	A11	FB_A1_DQ<8>	
DQ9	A13	FB_A1_DQ<9>	
DQ10	B11	FB_A1_DQ<10>	
DQ11	B13	FB_A1_DQ<11>	
DQ12	E11	FB_A1_DQ<12>	
DQ13	E13	FB_A1_DQ<13>	
DQ14	F11	FB_A1_DQ<14>	
DQ15	F13	FB_A1_DQ<15>	
DQ16	U11	FB_A1_DQ<16>	
DQ17	U13	FB_A1_DQ<17>	
DQ18	T11	FB_A1_DQ<18>	
DQ19	T13	FB_A1_DQ<19>	
DQ20	N11	FB_A1_DQ<20>	
DQ21	N13	FB_A1_DQ<21>	
DQ22	M11	FB_A1_DQ<22>	
DQ23	M13	FB_A1_DQ<23>	
DQ24	U4	FB_A1_DQ<24>	
DQ25	U2	FB_A1_DQ<25>	
DQ26	T4	FB_A1_DQ<26>	
DQ27	T2	FB_A1_DQ<27>	
DQ28	N4	FB_A1_DQ<28>	
DQ29	N2	FB_A1_DQ<29>	
DQ30	M4	FB_A1_DQ<30>	
DQ31	M2	FB_A1_DQ<31>	
NC	A5, J5, U5	NC	FB_A1_A<8>

U8400
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(2 OF 2)

OMIT_TABLE

VDD	C5, C10, D11, G1, G4, G11, G14, L1, L4, L11, L14, P11, R5, R10	
VDDQ	B1, B3, B12, B14, D1, D3, D12, D14, E5, E10, F1, F3, F12, F14, G2, G13, H3, H12, K3, K12, L2, L13, M1, M3, M12, M14, N5, N10, P1, P3, P12, P14, T1, T3, T12, T14	=PP1V35_GPU_FBVDDQ
VSS	B5, B10, D10, G5, G10, H1, H14, K1, K14, L5, L10, P10, T5, T10	
VSSQ	A1, A3, A12, A14, C1, C3, C4, C11, C12, C14, E1, E3, E12, E14, F5, F10, H2, H13, K2, K13, M5, M10, N1, N3, N12, N14, R1, R3, R4, R11, R12, R14, U1, U3, U12, U14	
VREFC	J14	FB_A0_VREFC
VREFD	A10, U10	FB_A0_VREFD

PLACE CLOSE TO U8400

=PP1V35_GPU_FBVDDQ
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.1 MM
R8430 549 1% 1/20W MF 201 — PLACE_NEAR=U8400.J14:8.4MM
FB_A0_VREFC
C8431 820PF 10% 25V X7R-CERM 0201 — PLACE_NEAR=U8400.J14:8.4MM
R8431 1.33K 1% 1/20W MF 201 — PLACE_NEAR=U8400.J14:8.4MM
R8434 931 1% 1/20W MF 201 — PLACE_NEAR=U8400.J14:8.4MM
FB_SW_LEG

=PP1V35_GPU_FBVDDQ
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.1 MM
R8432 549 1% 1/20W MF 201 — PLACE_NEAR=U8400.U10:8.4MM
FB_A0_VREFC
C8432 820PF 10% 25V X7R-CERM 0201
C8433 820PF 10% 25V X7R-CERM 0201
R8433 1.33K 1% 1/20W MF 201 — PLACE_NEAR=U8400.U10:8.4MM
R8435 931 1% 1/20W MF 201 — PLACE_NEAR=U8400.U10:8.4MM
FB_SW_LEG
PLACE_NEAR=U8400.A10:8.4MM
PLACE_NEAR=U8400.U10:8.4MM

U8450
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(2 OF 2)

OMIT_TABLE

VDD	C5, C10, D11, G1, G4, G11, G14, L1, L4, L11, L14, P11, R5, R10	
VDDQ	B1, B3, B12, B14, D1, D3, D12, D14, E5, E10, F1, F3, F12, F14, G2, G13, H3, H12, K3, K12, L2, L13, M1, M3, M12, M14, N5, N10, P1, P3, P12, P14, T1, T3, T12, T14	=PP1V35_GPU_FBVDDQ
VSS	B5, B10, D10, G5, G10, H1, H14, K1, K14, L5, L10, P10, T5, T10	
VSSQ	A1, A3, A12, A14, C1, C3, C4, C11, C12, C14, E1, E3, E12, E14, F5, F10, H2, H13, K2, K13, M5, M10, N1, N3, N12, N14, R1, R3, R4, R11, R12, R14, U1, U3, U12, U14	
VREFC	J14	FB_A1_VREFC
VREFD	A10, U10	FB_A1_VREFD

=PP1V35_GPU_FBVDDQ
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.1 MM
R8480 549 1% 1/20W MF 201 — PLACE_NEAR=U8450.J14:8.4MM
FB_A1_VREFC
C8481 820PF 10% 25V X7R-CERM 0201 — PLACE_NEAR=U8450.J14:8.4MM
R8481 1.33K 1% 1/20W MF 201 — PLACE_NEAR=U8450.J14:8.4MM
R8484 931 1% 1/20W MF 201 — PLACE_NEAR=U8450.J14:8.4MM
FB_SW_LEG
PLACE_NEAR=U8450.J14:8.4MM

PLACE CLOSE TO U8450

=PP1V35_GPU_FBVDDQ
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.1 MM
R8482 549 1% 1/20W MF 201 — PLACE_NEAR=U8450.U10:8.4MM
FB_A1_VREFD
C8482 820PF 10% 25V X7R-CERM 0201 — PLACE_NEAR=U8450.A10:8.4MM
C8483 820PF 10% 25V X7R-CERM 0201 — PLACE_NEAR=U8450.U10:8.4MM
R8483 1.33K 1% 1/20W MF 201 — PLACE_NEAR=U8450.U10:8.4MM
R8485 931 1% 1/20W MF 201 — PLACE_NEAR=U8450.U10:8.4MM
FB_SW_LEG
PLACE_NEAR=U8450.U10:8.4MM

SYNC_MASTER=D2_SEAN SYNC_DATE=03/05/2012

PAGE TITLE: GDDR5 Frame Buffer A

Apple Inc.

DRAWING NUMBER: 051-9589 SIZE: D
REVISION: 4.18.0
BRANCH:
PAGE: 84 OF 132
SHEET: 75 OF 99

Page Notes

Power aliases required by this page:
- =PP1V5R1V35_S0_FB_VDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

CK TERMINATION - B0

R8501 40.2 1% 1/20W MF 201 — FB_B0_CLK_P — FBB0_CK_MID — R8502 40.2 1% 1/20W MF 201 — FB_B0_CLK_N
C8590 0.01UF 10% 10V X7R-CERM 0201
PLACE_NEAR=U8500.J12:8.4MM
PLACE_NEAR=U8500.J11:8.4MM

CK TERMINATION - B1

R8551 40.2 1% 1/20W MF 201 — FB_B1_CLK_P — FBB1_CK_MID — R8552 40.2 1% 1/20W MF 201 — FB_B1_CLK_N
C8591 0.01UF 10% 10V X7R-CERM 0201
PLACE_NEAR=U8550.J12:8.4MM
PLACE_NEAR=U8550.J11:8.4MM

R8500 120 1% 1/20W MF 201
R8504 120 1% 1/20W MF 201
R8503 120 1% 1/20W MF 201

U8500
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(1 OF 2)

FB_B0_A<2>	H11	BA0/A2
FB_B0_A<5>	K10	BA1/A5
FB_B0_A<4>	K11	BA2/A4
FB_B0_A<3>	H10	BA3/A3
FB_B0_A<7>	K4	A8/A7
FB_B0_A<1>	H5	A9/A1
FB_B0_A<0>	H4	A10/A0
FB_B0_A<6>	K5	A11/A6
FB_B0_CKE_L	J3	CKE*
FB_B0_CLK_P	J12	CK
FB_B0_CLK_N	J11	CK*
FB_B0_CS_L	G12	CS*
FB_B0_WE_L	L12	WE*
FB_B0_CAS_L	L3	CAS*
FB_B0_RAS_L	G3	RAS*
FB_B0_ZQ	J13	ZQ
FB_B0_MF	J1	MF (MF=0)
FB_B0_SEN	J10	SEN
FB_B0_RESET_L	J2	RESET*
FB_B0_ABI_L	J4	ABI*
FB_B0_EDC<0>	C2	EDC0
FB_B0_EDC<1>	C13	EDC1
FB_B0_EDC<2>	R13	EDC2
FB_B0_EDC<3>	R2	EDC3
FB_B0_WCLK_P<0>	D4	WCK01
FB_B0_WCLK_N<0>	D5	WCK01*
FB_B0_WCLK_P<1>	P4	WCK23
FB_B0_WCLK_N<1>	P5	WCK23*

DBI0*	D2	FB_B0_DBI_L<0>
DBI1*	D13	FB_B0_DBI_L<1>
DBI2*	P13	FB_B0_DBI_L<2>
DBI3*	P2	FB_B0_DBI_L<3>
DQ0	A4	FB_B0_DQ<0>
DQ1	A2	FB_B0_DQ<1>
DQ2	B4	FB_B0_DQ<2>
DQ3	B2	FB_B0_DQ<3>
DQ4	E4	FB_B0_DQ<4>
DQ5	E2	FB_B0_DQ<5>
DQ6	F4	FB_B0_DQ<6>
DQ7	F2	FB_B0_DQ<7>
DQ8	A11	FB_B0_DQ<8>
DQ9	A13	FB_B0_DQ<9>
DQ10	B11	FB_B0_DQ<10>
DQ11	B13	FB_B0_DQ<11>
DQ12	E11	FB_B0_DQ<12>
DQ13	E13	FB_B0_DQ<13>
DQ14	F11	FB_B0_DQ<14>
DQ15	F13	FB_B0_DQ<15>
DQ16	U11	FB_B0_DQ<16>
DQ17	U13	FB_B0_DQ<17>
DQ18	T11	FB_B0_DQ<18>
DQ19	T13	FB_B0_DQ<19>
DQ20	N11	FB_B0_DQ<20>
DQ21	N13	FB_B0_DQ<21>
DQ22	M11	FB_B0_DQ<22>
DQ23	M13	FB_B0_DQ<23>
DQ24	U4	FB_B0_DQ<24>
DQ25	U2	FB_B0_DQ<25>
DQ26	T4	FB_B0_DQ<26>
DQ27	T2	FB_B0_DQ<27>
DQ28	N4	FB_B0_DQ<28>
DQ29	N2	FB_B0_DQ<29>
DQ30	M4	FB_B0_DQ<30>
DQ31	M2	FB_B0_DQ<31>
NC	A5, J5, U5	NC
		FB_B0_A<8>

OMIT_TABLE

U8550
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(1 OF 2)

FB_B1_A<2>	H11	BA0/A2
FB_B1_A<5>	K10	BA1/A5
FB_B1_A<4>	K11	BA2/A4
FB_B1_A<3>	H10	BA3/A3
FB_B1_A<7>	K4	A8/A7
FB_B1_A<1>	H5	A9/A1
FB_B1_A<0>	H4	A10/A0
FB_B1_A<6>	K5	A11/A6
FB_B1_CKE_L	J3	CKE*
FB_B1_CLK_P	J12	CK
FB_B1_CLK_N	J11	CK*
FB_B1_CS_L	G12	CS*
FB_B1_WE_L	L12	WE*
FB_B1_CAS_L	L3	CAS*
FB_B1_RAS_L	G3	RAS*
FB_B1_ZQ	J13	ZQ
FB_B1_MF	J1	MF (MF=0)
FB_B1_SEN	J10	SEN
FB_B1_RESET_L	J2	RESET*
FB_B1_ABI_L	J4	ABI*
FB_B1_EDC<0>	C2	EDC0
FB_B1_EDC<1>	C13	EDC1
FB_B1_EDC<2>	R13	EDC2
FB_B1_EDC<3>	R2	EDC3
FB_B1_WCLK_P<0>	D4	WCK01
FB_B1_WCLK_N<0>	D5	WCK01*
FB_B1_WCLK_P<1>	P4	WCK23
FB_B1_WCLK_N<1>	P5	WCK23*

DBI0*	D2	FB_B1_DBI_L<0>
DBI1*	D13	FB_B1_DBI_L<1>
DBI2*	P13	FB_B1_DBI_L<2>
DBI3*	P2	FB_B1_DBI_L<3>
DQ0	A4	FB_B1_DQ<0>
DQ1	A2	FB_B1_DQ<1>
DQ2	B4	FB_B1_DQ<2>
DQ3	B2	FB_B1_DQ<3>
DQ4	E4	FB_B1_DQ<4>
DQ5	E2	FB_B1_DQ<5>
DQ6	F4	FB_B1_DQ<6>
DQ7	F2	FB_B1_DQ<7>
DQ8	A11	FB_B1_DQ<8>
DQ9	A13	FB_B1_DQ<9>
DQ10	B11	FB_B1_DQ<10>
DQ11	B13	FB_B1_DQ<11>
DQ12	E11	FB_B1_DQ<12>
DQ13	E13	FB_B1_DQ<13>
DQ14	F11	FB_B1_DQ<14>
DQ15	F13	FB_B1_DQ<15>
DQ16	U11	FB_B1_DQ<16>
DQ17	U13	FB_B1_DQ<17>
DQ18	T11	FB_B1_DQ<18>
DQ19	T13	FB_B1_DQ<19>
DQ20	N11	FB_B1_DQ<20>
DQ21	N13	FB_B1_DQ<21>
DQ22	M11	FB_B1_DQ<22>
DQ23	M13	FB_B1_DQ<23>
DQ24	U4	FB_B1_DQ<24>
DQ25	U2	FB_B1_DQ<25>
DQ26	T4	FB_B1_DQ<26>
DQ27	T2	FB_B1_DQ<27>
DQ28	N4	FB_B1_DQ<28>
DQ29	N2	FB_B1_DQ<29>
DQ30	M4	FB_B1_DQ<30>
DQ31	M2	FB_B1_DQ<31>
NC	A5, J5, U5	NC
		FB_B1_A<8>

OMIT_TABLE

R8550 120 1% 1/20W MF 201
R8554 120 1% 1/20W MF 201
R8553 120 1% 1/20W MF 201

U8500
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(2 OF 2)

VDD	C5, C10, D11, G1, G4, G11, G14, L1, L4, L11, L14, P11, R5, R10	
VDDQ	B1, B3, B12, B14, D1, D3, D12, D14, E5, E10, F1, F3, F12, F14, G2, G13, H3, H12, K3, K12, L2, L13, M1, M3, M12, M14, N5, N10, P1, P3, P12, P14, T1, T3, T12, T14	
VSS	B5, B10, D10, G5, G10, H1, H14, K1, K14, L5, L10, P10, T5, T10	
VSSQ	A1, A3, A12, A14, C1, C3, C4, C11, C12, C14, E1, E3, E12, E14, F5, F10, H2, H13, K2, K13, M5, M10, N1, N3, N12, N14, R1, R3, R4, R11, R12, R14, U1, U3, U12, U14	
VREFC	J14	FB_B0_VREFC
VREFD	A10, U10	FB_B0_VREFD

OMIT_TABLE

=PP1V35_GPU_FBVDDQ

C8500 4.7UF 20% 6.3V X6S 0402
C8501 4.7UF 20% 6.3V X6S 0402
C8502 4.7UF 20% 6.3V X6S 0402
C8503 4.7UF 20% 6.3V X6S 0402
C8504 4.7UF 20% 6.3V X6S 0402
C8505 4.7UF 20% 6.3V X6S 0402
C8506 1UF 20% 4V CERM-X6S 0201
C8507 1UF 20% 4V CERM-X6S 0201
C8508 1UF 20% 4V CERM-X6S 0201
C8509 1UF 20% 4V CERM-X6S 0201
C8510 1UF 20% 4V CERM-X6S 0201
C8511 1UF 20% 4V CERM-X6S 0201
C8512 1UF 20% 4V CERM-X6S 0201
C8513 1UF 20% 4V CERM-X6S 0201
C8514 1UF 20% 4V CERM-X6S 0201
C8515 1UF 20% 4V CERM-X6S 0201
C8516 0.1UF 10% 6.3V X6S 0201
C8517 0.1UF 10% 6.3V X6S 0201
C8518 0.1UF 10% 6.3V X6S 0201
C8519 0.1UF 10% 6.3V X6S 0201
C8520 0.1UF 10% 6.3V X6S 0201
C8521 0.1UF 10% 6.3V X6S 0201
C8522 0.1UF 10% 6.3V X6S 0201
C8523 0.1UF 10% 6.3V X6S 0201
C8524 0.1UF 10% 6.3V X6S 0201
C8525 0.1UF 10% 6.3V X6S 0201

=PP1V35_GPU_FBVDDQ

C8550 4.7UF 20% 6.3V X6S 0402
C8551 4.7UF 20% 6.3V X6S 0402
C8552 4.7UF 20% 6.3V X6S 0402
C8553 4.7UF 20% 6.3V X6S 0402
C8554 4.7UF 20% 6.3V X6S 0402
C8555 4.7UF 20% 6.3V X6S 0402
C8556 1UF 20% 4V CERM-X6S 0201
C8557 1UF 20% 4V CERM-X6S 0201
C8558 1UF 20% 4V CERM-X6S 0201
C8559 1UF 20% 4V CERM-X6S 0201
C8560 1UF 20% 4V CERM-X6S 0201
C8561 1UF 20% 4V CERM-X6S 0201
C8562 1UF 20% 4V CERM-X6S 0201
C8563 1UF 20% 4V CERM-X6S 0201
C8564 1UF 20% 4V CERM-X6S 0201
C8565 1UF 20% 4V CERM-X6S 0201
C8566 0.1UF 10% 6.3V X6S 0201
C8567 0.1UF 10% 6.3V X6S 0201
C8568 0.1UF 10% 6.3V X6S 0201
C8569 0.1UF 10% 6.3V X6S 0201
C8570 0.1UF 10% 6.3V X6S 0201
C8571 0.1UF 10% 6.3V X6S 0201
C8572 0.1UF 10% 6.3V X6S 0201
C8573 0.1UF 10% 6.3V X6S 0201
C8574 0.1UF 10% 6.3V X6S 0201
C8575 0.1UF 10% 6.3V X6S 0201

U8550
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(2 OF 2)

VDD	C5, C10, D11, G1, G4, G11, G14, L1, L4, L11, L14, P11, R5, R10	
VDDQ	B1, B3, B12, B14, D1, D3, D12, D14, E5, E10, F1, F3, F12, F14, G2, G13, H3, H12, K3, K12, L2, L13, M1, M3, M12, M14, N5, N10, P1, P3, P12, P14, T1, T3, T12, T14	
VSS	B5, B10, D10, G5, G10, H1, H14, K1, K14, L5, L10, P10, T5, T10	
VSSQ	A1, A3, A12, A14, C1, C3, C4, C11, C12, C14, E1, E3, E12, E14, F5, F10, H2, H13, K2, K13, M5, M10, N1, N3, N12, N14, R1, R3, R4, R11, R12, R14, U1, U3, U12, U14	
VREFC	J14	FB_B1_VREFC
VREFD	A10, U10	FB_B1_VREFD

OMIT_TABLE

=PP1V35_GPU_FBVDDQ

R8530 549 1% 1/20W MF 201
R8531 1.33K 1% 1/20W MF 201
R8534 931 1% 1/20W MF 201
C8531 820PF 10% 25V X7R-CERM 0201
FB_B0_VREFC
FB_SW_LEG
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.1 MM
PLACE_NEAR=U8500.J14:8.4MM

PLACE CLOSE TO U8500

=PP1V35_GPU_FBVDDQ

R8532 549 1% 1/20W MF 201
R8533 1.33K 1% 1/20W MF 201
R8535 931 1% 1/20W MF 201
C8532 820PF 10% 25V X7R-CERM 0201
C8533 820PF 10% 25V X7R-CERM 0201
FB_B0_VREFD
FB_SW_LEG
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.1 MM
PLACE_NEAR=U8500.U10:8.4MM
PLACE_NEAR=U8500.A10:8.4MM

=PP1V35_GPU_FBVDDQ

R8580 549 1% 1/20W MF 201
R8581 1.33K 1% 1/20W MF 201
R8584 931 1% 1/20W MF 201
C8581 820PF 10% 25V X7R-CERM 0201
FB_B1_VREFC
FB_SW_LEG
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.1 MM
PLACE_NEAR=U8550.J14:8.4MM

PLACE CLOSE TO U8550

=PP1V35_GPU_FBVDDQ

R8582 549 1% 1/20W MF 201
R8583 1.33K 1% 1/20W MF 201
R8585 931 1% 1/20W MF 201
C8582 820PF 10% 25V X7R-CERM 0201
C8583 820PF 10% 25V X7R-CERM 0201
FB_B1_VREFD
FB_SW_LEG
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.1 MM
PLACE_NEAR=U8550.U10:8.4MM
PLACE_NEAR=U8550.A10:8.4MM

SYNC_MASTER=D2_SEAN	SYNC_DATE=03/05/2012
PAGE TITLE	GDDR5 Frame Buffer B
Apple Inc.	DRAWING NUMBER 051-9589 SIZE D
	REVISION 4.18.0
	BRANCH
	PAGE 85 OF 132
	SHEET 76 OF 99

PD FOR AUX CHANNELS (FOR NVIDIA)

DP_INT_EG_AUX_P
DP_INT_EG_AUX_N
DP_TBTSNK0_EG_AUXCH_P
DP_TBTSNK0_EG_AUXCH_N
DP_TBTSNK1_EG_AUXCH_P
DP_TBTSNK1_EG_AUXCH_N
HDMI_EG_DDC_CLK_Q
HDMI_EG_DDC_DATA_Q

R8614 100K 1% 1/20W MF 201
R8613 100K 1% 1/20W MF 201
R8615 100K 1% 1/20W MF 201
R8616 100K 1% 1/20W MF 201
R8617 100K 1% 1/20W MF 201
R8618 100K 1% 1/20W MF 201
R8627 100K 1% 1/20W MF 201 NO STUFF
R8628 100K 1% 1/20W MF 201 NO STUFF

=PP3V3_GPU_VDD33
R8623 4.7K 1% 1/20W MF 201
R8624 4.7K 1% 1/20W MF 201

DPA_EG_DDC_CLK R4 I2CA_SCL
DPA_EG_DDC_DATA R5 I2CA_SDA
GPU_SSC_SMB_CLK R2 I2CC_SCL
GPU_SSC_SMB_DAT R3 I2CC_SDA
GPU_SMB_CLK T4 I2CS_SCL
GPU_SMB_DAT T3 I2CS_SDA
DPB_EG_DDC_CLK R7 I2CB_SCL
DPB_EG_DDC_DATA R6 I2CB_SDA

DDC MAPPING
I2CA -> IFPE
I2CB -> IFPF
I2CC -> SSC CLK GEN

CRITICAL
L8604 330-OHM-1.2A 0603
=PP3V3_GPU_IFPX_PLLVDD
PP3V3_GPU_IFPX_PLLVDD
IFPX PLLVDD
C8610 10UF 20% 10V X6S-CERM 0603
C8611 1UF 10% 25V X6S-CERM 0402
C8612 0.1UF 20% 16V X6S-CERM 0201

PLACE BELOW GPU NEAR DISPLAY SECTION
C8613 10UF 20% 10V X6S-CERM 0603
C8619 4.7UF 20% 6.3V X6S-CERM 0603
C8615 1UF 10% 25V X6S-CERM 0402
C8616 1UF 10% 25V X6S-CERM 0402
C8617 0.1UF 20% 16V X6S-CERM 0201
C8618 0.1UF 20% 16V X6S-CERM 0201

L8605 FERR-220-OHM-2A 0603 CRITICAL ESR = 0.050OHM
=PP1V05_GPU_IFPCD_IOVDD
PP1V05_GPU_IFPCD_IOVDD
IFP CD IOVDD
C8625 4.7UF 20% 6.3V X6S 0402
C8626 1UF 20% 4V CERM-X6S 0201
C8627 0.1UF 20% 16V X6S-CERM 0201
C8628 0.1UF 20% 16V X6S-CERM 0201
C8655 10UF 20% 4V X6S-CERM 0402-1
C8656 1UF 20% 4V CERM-X6S 0201
C8657 0.1UF 20% 16V X6S-CERM 0201
C8658 0.1UF 20% 16V X6S-CERM 0201

L8606 FERR-220-OHM-2A 0603 CRITICAL ESR = 0.050OHM
=PP1V05_GPU_IFPEF_IOVDD
PP1V05_GPU_IFPEF_IOVDD
IFP EF IOVDD
C8629 10UF 20% 4V X6S-CERM 0402-1
C8630 1UF 20% 4V CERM-X6S 0201
C8631 0.1UF 20% 16V X6S-CERM 0201
C8632 0.1UF 20% 16V X6S-CERM 0201
C8633 4.7UF 20% 6.3V X6S 0402
C8634 4.7UF 20% 6.3V X6S 0402
C8635 1UF 20% 4V CERM-X6S 0201
C8636 1UF 20% 4V CERM-X6S 0201
C8637 0.1UF 20% 16V X6S-CERM 0201
C8638 0.1UF 20% 16V X6S-CERM 0201

OMIT_TABLE
CRITICAL
U8000 NV-GK107 BGA (5 OF 10)

PP1V8_GPU_IFPA_IOVDD	AG8	IFPA_IOVDD	IFPA_TXC AM6 NC
PP3V3_GPU_IFPB_IOVDD	AG9	IFPB_IOVDD	IFPA_TXC* AN6 NC
PP1V05_GPU_IFPCD_IOVDD	AF6	IFPC_IOVDD	AP3
PP1V05_GPU_IFPCD_IOVDD	AG6	IFPD_IOVDD	IFPA_TXD0 AN3 NC
PP1V05_GPU_IFPEF_IOVDD	AC7	IFPE_IOVDD	IFPA_TXD0* AN5 NC
PP1V05_GPU_IFPEF_IOVDD	AC8	IFPF_IOVDD	IFPA_TXD1 AM5 NC
PP1V05_GPU_IFPAB_PLLVDD	AH8	IFPAB_PLLVDD	IFPA_TXD1* AL6 NC
NC	AJ8	IFPAB_RSET	IFPA_TXD2 AK6 NC
PP3V3_GPU_IFPX_PLLVDD	AF7	IFPC_PLLVDD	IFPA_TXD2* AJ6 NC
IFPC_RSET	AF8	IFPC_RSET	IFPA_TXD3 AH6 NC
PP3V3_GPU_IFPX_PLLVDD	AG7	IFPD_PLLVDD	IFPA_TXD3*
IFPD_RSET	AN2	IFPD_RSET	IFPB_TXC AJ9
PP3V3_GPU_IFPX_PLLVDD	AB8	IFPEF_PLLVDD	IFPB_TXC* AH9 NC
IFPEF_RSET	AD6	IFPEF_RSET	IFPB_TXD4 AP6 NC
			IFPB_TXD4* AP5 NC
			IFPB_TXD5 AM7 NC
			IFPB_TXD5* AL7 NC
			IFPB_TXD6 AN8 NC
			IFPB_TXD6* AM8 NC
			IFPB_TXD7 AK8 NC
			IFPB_TXD7* AL8 NC
		IFPC_AUX_I2CW_SCL	AG3 HDMI_EG_DDC_CLK_Q
		IFPC_AUX_I2CW_SDA*	AG2 HDMI_EG_DDC_DATA_Q
		IFPC_L0	AK1 HDMI_EG_DATA_C_P<2>
		IFPC_L0*	AJ1 HDMI_EG_DATA_C_N<2>
		IFPC_L1	AJ3 HDMI_EG_DATA_C_P<1>
		IFPC_L1*	AJ2 HDMI_EG_DATA_C_N<1>
		IFPC_L2	AH3 HDMI_EG_DATA_C_P<0>
		IFPC_L2*	AH4 HDMI_EG_DATA_C_N<0>
		IFPC_L3	AG5 HDMI_EG_CLK_C_P
		IFPC_L3*	AG4 HDMI_EG_CLK_C_N
		IFPD_AUX_I2CX_SCL	AK3 DP_INT_EG_AUX_P
		IFPD_AUX_I2CX_SDA*	AK2 DP_INT_EG_AUX_N
		IFPD_L0	AM1 DP_INT_EG_ML_P<0>
		IFPD_L0*	AM2 DP_INT_EG_ML_N<0>
		IFPD_L1	AM3 DP_INT_EG_ML_P<1>
		IFPD_L1*	AM4 DP_INT_EG_ML_N<1>
		IFPD_L2	AL3 DP_INT_EG_ML_P<2>
		IFPD_L2*	AL4 DP_INT_EG_ML_N<2>
		IFPD_L3	AK4 DP_INT_EG_ML_P<3>
		IFPD_L3*	AK5 DP_INT_EG_ML_N<3>
		IFPE_AUX_I2CY_SCL	AB3 DP_TBTSNK0_EG_AUXCH_P
		IFPE_AUX_I2CY_SDA*	AB4 DP_TBTSNK0_EG_AUXCH_N
		IFPE_L0	AD2 DP_TBTSNK0_ML_C_P<0>
		IFPE_L0*	AD3 DP_TBTSNK0_ML_C_N<0>
		IFPE_L1	AD1 DP_TBTSNK0_ML_C_P<1>
		IFPE_L1*	AC1 DP_TBTSNK0_ML_C_N<1>
		IFPE_L2	AC2 DP_TBTSNK0_ML_C_P<2>
		IFPE_L2*	AC3 DP_TBTSNK0_ML_C_N<2>
		IFPE_L3	AC4 DP_TBTSNK0_ML_C_P<3>
		IFPE_L3*	AC5 DP_TBTSNK0_ML_C_N<3>
		IFPF_AUX_I2CZ_SCL	AF3 DP_TBTSNK1_EG_AUXCH_P
		IFPF_AUX_I2CZ_SDA*	AF2 DP_TBTSNK1_EG_AUXCH_N
		IFPF_L0	AE3 DP_TBTSNK1_ML_C_P<0>
		IFPF_L0*	AE4 DP_TBTSNK1_ML_C_N<0>
		IFPF_L1	AF4 DP_TBTSNK1_ML_C_P<1>
		IFPF_L1*	AF5 DP_TBTSNK1_ML_C_N<1>
		IFPF_L2	AD4 DP_TBTSNK1_ML_C_P<2>
		IFPF_L2*	AD5 DP_TBTSNK1_ML_C_N<2>
		IFPF_L3	AG1 DP_TBTSNK1_ML_C_P<3>
		IFPF_L3*	AF1 DP_TBTSNK1_ML_C_N<3>
DAC_AVDD	AG10	DACA_VDD	
		DACA_RED	AK9 NC
		DACA_GREEN	AL10 NC
		DACA_BLUE	AL9 NC
	AP9	DACA_VREF	
	AP8	DACA_RSET	
		DACA_HSYNC	AM9 NC
		DACA_VSYNC	AN9 NC
		CEC	L3 NC

R8600 10K 1% 1/20W MF 201

DISABLE PHY A & B FOR 15" MBP

PP1V8_GPU_IFPA_IOVDD
MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.2 mm VOLTAGE=1.8V
R8601 10K 1% 1/20W MF 201

PP3V3_GPU_IFPB_IOVDD
MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.2 mm VOLTAGE=3.3V
R8602 10K 1% 1/20W MF 201

PP1V05_GPU_IFPAB_PLLVDD
MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.2 mm VOLTAGE=1.05V
R8603 10K 1% 1/20W MF 201

GPU_TESTMODE
R8608 10K 1% 1/20W MF 201

PD FOR RSET
IFPC_RSET PLACE_NEAR=U8000.AF8:5MM R8621 1K 1% 1/20W MF 201
IFPD_RSET PLACE_NEAR=U8000.AN2:5MM R8606 1K 1% 1/20W MF 201
IFPEF_RSET PLACE_NEAR=U8000.AD6:5MM R8607 1K 1% 1/20W MF 201

Page Notes

Power aliases required by this page:
- =PP3V3_GPU_IFPB_IOVDD
- =PP1V8_GPU_IFPA_IOVDD
- =PP1V8_GPU_DPLL
- =PP1V05_GPU_DPLL
- =PP3V3_GPU_IFPX_PLLVDD
- =PP1V05_GPU_IFPCD_IOVDD
- =PP1V05_GPU_IFPEF_IOVDD
- =PP3V3_GPU_VDD33

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- J31:YES
- D2:YES

PP1V05_GPU_SP_PLLVDD = PP1V05_GPU_VID_PLLVDD (MAKE_BASE=TRUE)

GPU_OSC_27M_XTAL_BUFFOUT_R PLACE_NEAR=U8000.J4:8.4MM R8611 10K 1% 1/20W MF 201
GPU_OSC_27M_SSIN PLACE_NEAR=U8000.H1:8.4MM R8612 10K 1% 1/20W MF 201

=PP3V3_GPU_VDD33
R8625 4.7K 1% 1/20W MF 201
R8626 4.7K 1% 1/20W MF 201

DDC 3.3V/5V LEVEL TRANSLATOR
SSM6N37FEAPE SOT563 Q8600
HDMI_EG_DDC_CLK
HDMI_EG_DDC_DATA

OMIT_TABLE
U8000 NV-GK107 BGA (6 OF 10)

GPIO0	P6	GPU_GPIO_0
GPIO1	M3	GPU_GPIO_1
GPIO2	L6	GPU_GPIO_2
GPIO3	P5	GPU_GPIO_3
GPIO4	P7	GPU_GPIO_4
GPIO5	L7	GPU_GPIO_5
GPIO6	M7	GPU_GPIO_6
GPIO7	N8	GPU_GPIO_7
GPIO8	M1	GPU_GPIO_8
GPIO9	M2	GPU_GPIO_9
GPIO10	L1	GPU_GPIO_10
GPIO11	M5	GPU_GPIO_11
GPIO12	N3	GPU_GPIO_12
GPIO13	M4	GPU_GPIO_13
GPIO14	N4	GPU_GPIO_14
GPIO15	P2	GPU_GPIO_15
GPIO16	R8	GPU_GPIO_16
GPIO17	M6	GPU_GPIO_17
GPIO18	R1	GPU_GPIO_18
GPIO19	P3	GPU_GPIO_19
GPIO20	P4	GPU_GPIO_20
GPIO21	P1	GPU_GPIO_21
JTAG_TCK	AM10	GPU_JTAG_TCK
JTAG_TDI	AM11	GPU_JTAG_TDI
JTAG_TDO	AP12	GPU_JTAG_TDO
JTAG_TMS	AP11	GPU_JTAG_TMS
JTAG_TRST*	AN11	GPU_JTAG_TRST_L
THERMDP	K3	GPU_TDIODE_P
THERMDN	K4	GPU_TDIODE_N

=PP3V3_GPU_MISC
=PP3V3_GPU_VDD33
VDD33 J8 K8 L8 M8
ROM_CS* H6 GPU_ROM_CS_L
ROM_SCLK H4 GPU_ROM_SCLK
ROM_SI H5 GPU_ROM_SI
ROM_SO H7 GPU_ROM_SO
R8609 40.2K 0.1% 1/20W MF 0201
MULTI_STRAP_REF_GND J1 MULTI_STRAP_REF
TESTMODE AK11 GPU_TESTMODE
SP_PLLVDD AE8 PP1V05_GPU_SP_PLLVDD
PLLVDD AD8 PP1V05_GPU_PLLVDD
VID_PLLVDD AD7 PP1V05_GPU_VID_PLLVDD
XTAL_IN H3 GPU_OSC_27M_XTALIN
XTAL_OUT H2 GPU_OSC_27M_XTALOUT
XTAL_OUTBUFF J4 GPU_OSC_27M_XTAL_BUFFOUT_R
XTAL_SSIN H1 GPU_OSC_27M_SSIN
STRAP0 J2 GPU_MLS_STRAP0
STRAP1 J7 GPU_MLS_STRAP1
STRAP2 J6 GPU_MLS_STRAP2
STRAP3 J5 GPU_MLS_STRAP3
STRAP4 J3 GPU_MLS_STRAP4

GPU PLL VDD
L8607 FERR-220-OHM-2A 0603 CRITICAL ESR = 0.050OHM
=PP1V05_GPU_PEX_PLLVDD
PP1V05_GPU_PLLVDD
MIN_LINE_WIDTH=0.41 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=1.05V
C8651 20UF 20% 2V X6T-CERM 0402
C8652 1UF 20% 4V CERM-X6S 0201
C8653 0.1UF 20% 16V X6S-CERM 0201
C8654 0.1UF 20% 16V X6S-CERM 0201

GPU 3V3 VDD
=PP3V3_GPU_VDD33
C8640 10UF 20% 10V X6S-CERM 0603
C8641 1UF 10% 25V X6S-CERM 0402
C8642 1UF 10% 25V X6S-CERM 0402
C8643 0.1UF 20% 16V X6S-CERM 0201
C8644 0.1UF 20% 16V X6S-CERM 0201
=PP3V3_GPU_MISC
C8645 4.7UF 20% 6.3V X6S 0402
C8646 4.7UF 20% 6.3V X6S 0402
C8649 0.1UF 20% 16V X6S-CERM 0201
C8650 0.1UF 20% 16V X6S-CERM 0201

SYNC_MASTER=D2_SEAN SYNC_DATE=03/05/2012
PAGE TITLE: KEPLER EDP/DP/GPIO
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GPIOs

77	GPU_GPIO_0	GFXIMVP_VID<4>	80
77	GPU_GPIO_1	GFXIMVP_VID<3>	80
77	GPU_GPIO_2	GFXIMVP_PSI_R_L	80
77	GPU_GPIO_3	EG_LCD_PWR_EN	78 82
77	GPU_GPIO_4	EG_BKLT_EN	78 82
77	GPU_GPIO_5	GFXIMVP_VID<1>	80
77	GPU_GPIO_6	GFXIMVP_VID<2>	80
77	GPU_GPIO_7	FB_CLAMP_TOGGLE_REQ_L	78 82
77	GPU_GPIO_8	SMC_GFX_OVERTEMP_R_L	78
77	GPU_GPIO_9	SMC_GFX_THROTTLE_R_L	78
77	GPU_GPIO_10	GPU_ALT_VREF	73
77	GPU_GPIO_11	GFXIMVP_VID<0>	80
77	GPU_GPIO_12	HDMI_EG_HPD	82
77	GPU_GPIO_13	GFXIMVP_VID<5>	80

GPIOs

77	GPU_GPIO_14	DP_EXTA_CA_DET_EG	82
77	GPU_GPIO_15	DP_EXTB_CA_DET_EG	82
77	GPU_GPIO_16	FBVDD_ALTVO	74 78
77	GPU_GPIO_17	DP_INT_EG_HPD	82
77	GPU_GPIO_18	DP_TBTSNK0_HPD_EG	82
77	GPU_GPIO_19	DP_TBTSNK1_HPD_EG	82
77	GPU_GPIO_20	NC_GPU_GPIO_20_RSVD (NO_TEST=TRUE)	
77	GPU_GPIO_21	NC_GPU_GPIO_21_RSVD (NO_TEST=TRUE)	

77 PEX_CLKREQ_L_R — R8795 0 5% 1/20W MF 201 — EG_CLKREQ_IN_L OUT 9 82

GPU internal Temp isolation

=PP3V3_GPU_VDD33

R8755 10K 5% 1/20W MF 201

Q8702 SSM6N37FEAPE SOT563

77 B1 GPU_SMB_DAT — GPU_SMB_DAT_R B1 44

R8780 0 5% 1/20W MF 201 NOSTUFF

=PP3V3_GPU_VDD33

R8754 10K 5% 1/20W MF 201

Q8702 SSM6N37FEAPE SOT563

77 OUT GPU_SMB_CLK — GPU_SMB_CLK_R IN 44

R8781 0 5% 1/20W MF 201 NOSTUFF

Unused signals

TP_GPU_JTAG_TCK (MAKE_BASE=TRUE)	GPU_JTAG_TCK	77
TP_GPU_JTAG_TDI (MAKE_BASE=TRUE)	GPU_JTAG_TDI	77
TP_GPU_JTAG_TDO (MAKE_BASE=TRUE)	GPU_JTAG_TDO	77
	GPU_JTAG_TMS	77
	GPU_JTAG_TRST_L	77

Note: PU to non GPU_S0 3v3 source

82 35 8 =PP3V3_S0_DPMUX_UC — R8753 10K 5% 1/20W MF 201 NOSTUFF GC6 SUPPORT

82 78 FB_CLAMP_TOGGLE_REQ_L

R8751 10K 5% 1/20W MF 201 NOSTUFF

R8758 10K 5% 1/20W MF 201 NOSTUFF

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0013	1	RES, 10KOHM, 0201	R8711		FB_2G_SAMSUNG
118S0414	1	RES,5.1KOHM, 0201	R8711		FB_2G_HYNIX_M_DIE
118S0230	1	RES,MF,24.9KOHM,1/20W,0201	R8711		FB_2G_HYNIX_A_DIE

Die Rev	Strap
D-DIE	0x1
M-DIE	0x0
A-DIE	0x4

Straps for GK107. GF108 support has been removed.

CONFIG STRAPS - MLPS

=PP3V3_GPU_VDD33

R8700 45.3K 1% 1/20W MF 201

OUT 77 GPU_MLS_STRAP0

R8701 5.62K 1% 1/20W MF 201 NOSTUFF

=PP3V3_GPU_VDD33

NOSTUFF R8708 3.24K 1% 1/20W MF 201

OUT 77 GPU_MLS_STRAP4

R8709 45.3K 1% 1/20W MF 201

=PP3V3_GPU_VDD33

NOSTUFF R8702 3.24K 1% 1/20W MF 201

OUT 77 GPU_MLS_STRAP1

R8703 45.3K 1% 1/20W MF 201

=PP3V3_GPU_VDD33

NOSTUFF R8710 3.24K 1% 1/20W MF 201

OUT 77 78 GPU_ROM_SI

R8711 25.5K 1% 1/20W MF 201 OMIT_TABLE

=PP3V3_GPU_VDD33

NOSTUFF R8704 15K 1% 1/20W MF 201

OUT 77 GPU_MLS_STRAP2

R8705 30K 1% 1/20W MF 201

=PP3V3_GPU_VDD33

R8712 10K 1% 1/20W MF 201

OUT 77 78 GPU_ROM_SO

NOSTUFF R8713 10K 1% 1/20W MF 201

=PP3V3_GPU_VDD33

R8706 20K 1% 1/20W MF 201

OUT 77 GPU_MLS_STRAP3

R8707 5.62K 1% 1/20W MF 201 NOSTUFF

=PP3V3_GPU_VDD33

R8714 24.9K 1% 1/20W MF 201

OUT 77 78 GPU_ROM_SCLK

NOSTUFF R8715 34.8K 1% 1/20W MF 201

GPU GC6 ROM

=PP3V3_GPU_VDD33

77 78 GPU_ROM_SI — R8723 33 5% 1/20W MF 201 — GPU_ROM:YES

GPU_ROM:YES R8720 10K 5% 1/20W MF 201 OMIT_TABLE 8 VCC

GPU_ROM:YES R8721 0 5% 1/20W MF 201 GPU_ROM:YES C8721 0.1UF 10% 6.3V X6S 0201

U8701 1MBIT USON MX25L1005CMI-12G CRITICAL

GPU_ROM_SI_R 5 SI — SCLK 6 — GPU_ROM_SCLK_R — R8724 33 5% 1/20W MF 201 — GPU_ROM_SCLK — GPU_ROM:YES 77 78

77 78 GPU_ROM_SO — R8726 33 5% 1/20W MF 201 — GPU_ROM_SO_R 2 SO

CS* 1 — GPU_ROM_CS_L_R — R8725 33 5% 1/20W MF 201 — GPU_ROM_CS_L — GPU_ROM:YES 77

WP* 3 — GPU_ROM_WP_L

HOLD* 7

THRM PAD 9 — GND 4

NO STUFF R8722 0 5% 1/20W MF 201

GPU XTAL 27 MHZ

GPU_OSC_27M_XTALIN OUT 77 95

GPU_OSC_27M_XTALOUT IN 77 95

CRITICAL Y8700 2.50X2.00MM-SM 27MHZ-30PPM-18PF-60OHM

C8700 18PF 5% 25V NPO-C0G-CERM 0201 NCX

C8701 18PF 5% 25V NPO-C0G-CERM 0201 NCX

STRAP NOTES:

CURRENTLY STUFFED FOR GF108a/GK107-GTX

STUFF R8704 FOR THICK DIE

STUFF R8705 FOR THIN DIE

GPU overtemp masking

=PP3V3_GPU_VDD33

=PP3V3_S5_SMC 42 41 8

=PP3V3_GPU_VDD33

R8756 0 5% 1/20W MF 201

NOSTUFF R8757 0 5% 1/20W MF 201

R8752 10K 5% 1/20W MF 201

VOLTAGE=3.3V MIN_LINE_WIDTH=0.2 MM MIN_NECK_WIDTH=0.1 MM

PP3V3_GPU_OVERTEMP

U8702 74LVC1G08 SOT891

SMC_GFX_OVERTEMP_Q 2 — 1 — 08 — 4 — SMC_GFX_OVERTEMP OUT 78 41 42

NC 5 — 3

Q8701 SSM3K15FV SOD-VESM-HF D 3 G 1 S 2

78 SMC_GFX_OVERTEMP_R_L

GPU_RESET_L IN

=PP3V3_GPU_VDD33

R8796 10K 5% 1/20W MF 201

R8797 10K 5% 1/20W MF 201

78 SMC_GFX_OVERTEMP_R_L — R8798 0 NO STUFF 5% 1/20W MF 201 — SMC_GFX_OVERTEMP OUT 41 42 78

78 SMC_GFX_THROTTLE_R_L — R8799 0 5% 1/20W MF 201 — SMC_GFX_THROTTLE_L B1 41

EG_LCD_PWR_EN OUT 78 82

EG_BKLT_EN OUT 78 82

FBVDD_ALTVO OUT 74 78

R8792 10K 5% 1/20W MF 201

R8793 10K 5% 1/20W MF 201

R8794 10K 5% 1/20W MF 201

NO STUFF R8790 10K 5% 1/20W MF 201

NOSTUFF R8791 10K 5% 1/20W MF 201

SYNC_MASTER=D2_SEAN SYNC_DATE=03/05/2012

PAGE TITLE: KEPLER GPIOS,CLK & STRAPS

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Page Notes

Power aliases required by this page:

- =PP3V3_GPU_VDD33
- =PP1V05_GPU_PEX_IOVDD
- =PP1V05_GPU_PEX_PLLVDD

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

GPU SP PLLVDD

L8804 FERR-220-OHM-2A 0603 CRITICAL ESR = 0.050OHM

=PP1V05_GPU_PEX_PLLVDD → C8830 20UF 20% 2V X6T-CERM 0402 → C8831 4.7UF 20% 6.3V X6S 0402 → C8832 1UF 20% 4V CERM-X6S 0201 → C8833 1UF 20% 4V CERM-X6S 0201 → C8834 0.1UF 20% 16V X6S-CERM 0201 → C8835 0.1UF 20% 16V X6S-CERM 0201 → C8836 0.1UF 20% 16V X6S-CERM 0201 → C8837 0.1UF 20% 16V X6S-CERM 0201 → PP1V05_GPU_SP_PLLVDD

MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=1.05V

XW8801 SM — MIN_LINE_WIDTH=0.3 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=0V — GND_GPU_SP_PLLVDD

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OMIT_TABLE

NC P8	PEX_IOVDD	AG19
NC AC6	PEX_IOVDD	AG21
NC AJ28	PEX_IOVDD	AG22
NC AJ4	PEX_IOVDD	AG24
NC AJ5	PEX_IOVDD	AH21
NC AL11	PEX_IOVDD	AH25
NC C15		
NC D19		
NC D20	PEX_IOVDDQ	AG13
NC D23	PEX_IOVDDQ	AG15
NC D26	PEX_IOVDDQ	AG16
NC H31	PEX_IOVDDQ	AG18
NC T8	PEX_IOVDDQ	AG25
NC V32	PEX_IOVDDQ	AH15
	PEX_IOVDDQ	AH18
	PEX_IOVDDQ	AH26
	PEX_IOVDDQ	AH27
	PEX_IOVDDQ	AJ27
	PEX_IOVDDQ	AK27
	PEX_IOVDDQ	AL27
	PEX_IOVDDQ	AM28
	PEX_IOVDDQ	AN28
C16	GND_OPT	
W32	GND_OPT	
L4	VDD_SENSE	
L5	GND_SENSE	
GPU_BUFRSTN L2	BUFRST*	
	PEX_PLLVDD	AG26
	PEX_PLL_HVDD	AH12

=PP1V05_GPU_PEX_IOVDD (8 73 79) → PEX_IOVDD rails

=PP1V05_GPU_PEX_IOVDD (8 73 79) → PEX_IOVDDQ rails

=PPVCORE_GPU (72 8) → R8810 100 5% 1/20W MF 201 → C16, W32 GND_OPT

GPUVCORE_SENSE_P (97 80 OUT) → L4 VDD_SENSE

GPUVCORE_SENSE_N (97 80 OUT) → L5 GND_SENSE

GPU_BUFRSTN L2 BUFRST* — R8811 100 5% 1/20W MF 201; R8800 10K 1% 1/20W MF 201

PP1V05_GPU_PEX_PLLVDD

MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.05V

PP1V05_GPU_PEX_PLLVDD → R8803 0 5% 1/10W MF-LF 603 → =PP1V05_GPU_PEX_PLLVDD (8 77 79)

C8826 4.7UF 20% 6.3V X6S 0402; C8827 4.7UF 20% 6.3V X6S 0402; C8828 1UF 20% 4V CERM-X6S 0201; C8829 0.1UF 10% 6.3V X6S 0201

GND_GPU_PEX_PLLVDD — XW8802 SM — MIN_LINE_WIDTH=0.3 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=0V

PP3V3_GPU_PEX_PLL_HVDD

MIN_LINE_WIDTH=0.8 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=3.3V

PP3V3_GPU_PEX_PLL_HVDD → R8802 0 5% 1/16W MF-LF 402 → =PP3V3_GPU_VDD33 (8 71 77 78)

C8822 4.7UF 20% 6.3V X6S 0402; C8823 4.7UF 20% 6.3V X6S 0402; C8824 1UF 20% 4V CERM-X6S 0201; C8825 0.1UF 10% 6.3V X6S 0201

GND_GPU_PEX_PLL_HVDD — XW8803 SM — MIN_LINE_WIDTH=0.3 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=0V

PEX IOVDD & PEX IOVDDQ

XW8804 SM — PLACE XW8800 & XW8804 CLOSE TO C8803 — P1V05_GPU_PEX_IOVDD_SNS_P (OUT 74 97) — PLACE_NEAR=C8803.1:2MM

=PP1V05_GPU_PEX_IOVDD (79 73 8)

C8803 20UF 20% 2V X6T-CERM 0402; C8804 20UF 20% 2V X6T-CERM 0402; C8805 4.7UF 20% 6.3V X6S 0402

XW8800 SM — P1V05_GPU_PEX_IOVDD_SNS_N (OUT 74 97) — PLACE_NEAR=C8803.2:2MM

C8815 10UF 20% 4V X6S-CERM 0402-1; C8816 1UF 20% 4V CERM-X6S 0201; C8817 0.1UF 10% 6.3V X6S 0201; C8818 100PF 5% 25V NP0-CERM 0201

C8809 10UF 20% 4V X6S-CERM 0402-1; C8810 1UF 20% 4V CERM-X6S 0201; C8811 0.1UF 10% 6.3V X6S 0201; C8819 100PF 5% 25V NP0-CERM 0201

EDP = 2000 MA

C8800 20UF 20% 2V X6T-CERM 0402; C8801 20UF 20% 2V X6T-CERM 0402; C8802 4.7UF 20% 6.3V X6S 0402

C8812 10UF 20% 4V X6S-CERM 0402-1; C8813 1UF 20% 4V CERM-X6S 0201; C8814 0.1UF 10% 6.3V X6S 0201; C8821 100PF 5% 25V NP0-CERM 0201

C8806 10UF 20% 4V X6S-CERM 0402-1; C8807 1UF 20% 4V CERM-X6S 0201; C8808 0.1UF 10% 6.3V X6S 0201; C8820 100PF 5% 25V NP0-CERM 0201

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OMIT_TABLE

AG11	AK7
A2	AL12
A33	AL14
AA13	AL15
AA15	AL17
AA17	AL18
AA18	AL2
AA20	AL20
AA22	AL21
AB12	AL23
AB14	AL24
AB16	AL26
AB19	AL28
AB2	AL30
AB21	AL32
AB23	AL33
AB28	AL5
AB30	AM13
AB32	AM16
AB5	AM19
AB7	AM22
AC13	AM25
AC15	AN1
AC17	AN10
AC18	AN13
AC20	AN16
AC22	AN19
AE2	AN22
AE28	AN25
AE30	AN30
AE32	AN34
AE33	AN4
AE5	AN7
AE7	AP2
AH10	AP33
AH13	B1
AH16	B10
AH19	B22
AH2	B25
AH22	B28
AH24	B31
AH28	B34
AH29	B4
AH30	B7
AH32	C10
AH33	C13
AH5	C19
AH7	C22
AJ7	C25
AK10	C28

GND

U8000 NV-GK107 BGA (9 OF 10)

OMIT_TABLE

C7	N7
D2	P13
D31	P15
D33	P17
E10	P18
E22	P20
E25	P22
E5	R12
E7	R14
F28	R16
F7	R19
G10	R21
G13	R23
G16	T13
G19	T15
G2	T17
G22	T18
G25	T2
G28	T20
G3	T22
G30	T28
G32	T32
G33	T5
G5	T7
G7	U12
K2	U14
K28	U16
K30	U19
K32	U21
K33	U23
K5	V12
K7	V14
M13	V16
M15	V19
M17	V21
M18	V23
M20	W13
M22	W15
N12	W17
N14	W18
N16	W20
N19	W22
N2	W28
N21	Y12
N23	Y14
N28	Y16
N30	Y19
N32	Y21
N33	Y23
N5	AH11

GND

SYNC_MASTER=D2_SEAN SYNC_DATE=03/05/2012

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=PPVIN_S0_GFXIMVP

=PP5V_S0_GFXIMVP

PLACE_NEAR=Q8900.25:1mm
C8902 1UF 10% 25V X6S-CERM 0402

R8901 1 5% 1/20W MF 201
MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM VOLTAGE=5V
PP5V_S0_GFXIMVP_VDD

PLACE_NEAR=Q8900.16:1mm
C8901 1UF 10% 25V X6S-CERM 0402

R8900 10 5% 1/20W MF 201
MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM VOLTAGE=12.8V
PPVIN_S0_GFXIMVP_R

PLACE_NEAR=Q8900.17:1mm
C8900 0.22UF 10% 25V X7R 0402

(GND_GFXIMVP_AGND)

R8940 147K 1% 1/20W MF 201

R8918 30.1K 1% 1/20W MF 201

C8916 560PF 10% 50V X7R-CERM 0201 GFXIMVP_COMP_R

R8913 8.06K 1% 1/20W MF 201

C8917 330PF 10% 16V X7R-CERM 0201

C8918 NOSTUFF 22PF 5% 50V NP0-C0G-CERM 0201

R8914 5.11K 1% 1/20W MF 201

C8919 1000PF 10% 16V X7R-CERM 0201

R8916 49.9 1% 1/20W MF 201 GFXIMVP_FB_SNS_R

R8915 SIGNAL_MODEL=EMPTY 301 1% 1/20W MF 201

C8940 SIGNAL_MODEL=EMPTY 3300PF 10% 16V X7R 201

R8917 NOSTUFF 49.9 1% 1/20W MF 201 GFXIMVP_FB_GND_R

C8941 NOSTUFF 5600PF 10% 16V CERM 201

C8915 SIGNAL_MODEL=EMPTY 1000PF 10% 16V X7R-CERM 0201

C8914 SIGNAL_MODEL=EMPTY 1000PF 10% 16V X7R-CERM 0201

R8912 SIGNAL_MODEL=EMPTY 10K 1% 1/20W MF 201

C8913 SIGNAL_MODEL=EMPTY 0.1UF 10% 6.3V X6S 0201

U8900 ISL62882C TQFN
VDD VCCP VIN (16 25 17)
Line Width & DIDT on all DIDT nets

GFXIMVP_RBIAS	3	RBIAS 353S3679	
GFXIMVP_NTC	5	NTC	
GPUVCORE_PGOOD (OUT)	1	PGOOD	
GFXIMVP_VR_TT_L	4	VR_TT*	
	40	CLK_EN*	
GFXIMVP_VID<0> (IN)	31	VID0	
GFXIMVP_VID<1> (IN)	32	VID1	
GFXIMVP_VID<2> (IN)	33	VID2	
GFXIMVP_VID<3> (IN)	34	VID3	
GFXIMVP_VID<4> (IN)	35	VID4	
GFXIMVP_VID<5> (IN)	36	VID5	
GFXIMVP_VID<6> (IN)	37	VID6	
GFXIMVP_PSI_L	2	PSI*	
GFXIMVP_DPSLP_EN	39	DPRSLPVR	
=GPUVCORE_EN (IN)	38	VR_ON	
GFXIMVP_VW	6	VW	
GFXIMVP_COMP	7	COMP	
GFXIMVP_FB2	9	FB2	
GFXIMVP_FB	8	FB	
CKPLUS_WAIVE=PdifPr_badTerm	12	VSEN	
GPUVCORE_SENSE_P (IN)	13	RTN	
GPUVCORE_SENSE_N (IN)	18	IMON	
GFXIMVP6_IMON (OUT)			
	41	THRM PAD	
	30	BOOT2	GFXIMVP_BOOT2 GATE_NODE=TRUE
	29	UGATE2	GFXIMVP_UGATE2 SWITCH_NODE=TRUE
	28	PHASE2	GFXIMVP_PHASE2 GATE_NODE=TRUE
	26	LGATE2	GFXIMVP_LGATE2 GATE_NODE=TRUE
	27	VSSP2	GFXIMVP_VSSP2 MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM VOLTAGE=0V
	10	ISEN2	GFXIMVP_ISEN2
	19	BOOT1	GFXIMVP_BOOT1 GATE_NODE=TRUE
	20	UGATE1	GFXIMVP_UGATE1 SWITCH_NODE=TRUE
	21	PHASE1	GFXIMVP_PHASE1 GATE_NODE=TRUE
	23	LGATE1A	GFXIMVP_LGATE1
	24	LGATE1B	NC MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM VOLTAGE=0V
	22	VSSP1	GFXIMVP_VSSP1
	11	ISEN1	GFXIMVP_ISEN1
	15	ISUM+	GFXIMVP_ISUMP
	14	ISUM-	GFXIMVP_ISUMN_R

XW8900 SM PLACE_NEAR=U8900.41:1mm

GND_GFXIMVP_AGND MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM VOLTAGE=0V

MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM DIDT=TRUE GFXIMVP_BOOT2_R

C8930 0.22UF 10% 16V CERM 402

R8930 0 5% 1/10W MF-LF 603

Q8930 IRF6802SDTRPBF DIRECTFET-SA

CRITICAL L8930 0.2UH-20%-24A-0.003OHM PIMB063T-SM
MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM VOLTAGE=1.05V

PPVCORE_S0_GFX_PH2

R8998 0.00075 1% 1W MF 0612

25A max per phase

=PPVCORE_S0_GFX_REG

C8928 0.001UF 10% 50V X7R-CERM 0402

C8927 0.001UF 10% 50V X7R-CERM 0402

OMIT_TABLE CRITICAL C8926 68UF 20% 16V POLY-TANT CASE-D2E-SM

OMIT_TABLE CRITICAL C8920 68UF 20% 16V POLY-TANT CASE-D2E-SM

OMIT_TABLE CRITICAL C8921 68UF 20% 16V POLY-TANT CASE-D2E-SM

OMIT_TABLE CRITICAL C8922 68UF 20% 16V POLY-TANT CASE-D2E-SM

C8923 1UF 10% 25V X6S-CERM 0402

C8924 1UF 10% 25V X6S-CERM 0402

CRITICAL C8925 150UF 20% 16V TANT SM

CRITICAL C8961 270UF 20% 2V TANT CASE-B2-SM

CRITICAL C8962 270UF 20% 2V TANT CASE-B2-SM

CRITICAL C8963 270UF 20% 2V TANT CASE-B2-SM

CRITICAL C8964 270UF 20% 2V TANT CASE-B2-SM

GFXIMVP_ISNS2_P

GFXIMVP_ISNS2_N

R8931 10K 1% 1/20W MF 201

R8933 1K 1% 1/20W MF 201

R8934 1.00 1% 1/20W MF 201

GFXIMVP_ISUMN

GFXIMVP_ISUMP

R8932 10K 1% 1/20W MF 201

C8931 0.22UF 20% 6.3V X6S-CERM 0201

GFXIMVP_ISNS1_N

PLACE_NEAR=Q8931.3:1mm XW8930 SM

=PPVIN_S0_GFXIMVP

MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM DIDT=TRUE GFXIMVP_BOOT1_R

C8965 0.22UF 10% 16V CERM 402

R8960 0 5% 1/10W MF-LF 603

Q8930 IRF6802SDTRPBF DIRECTFET-SA

CRITICAL L8960 0.2UH-20%-24A-0.003OHM PIMB063T-SM
MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM VOLTAGE=1.05V

PPVCORE_S0_GFX_PH1

R8999 0.00075 1% 1W MF 0612

GFXIMVP_ISNS1_P

GFXIMVP_ISNS1_N

R8961 10K 1% 1/20W MF 201

R8963 1K 1% 1/20W MF 201

R8964 1.00 1% 1/20W MF 201

GFXIMVP_ISUMN

GFXIMVP_ISUMP

R8962 10K 1% 1/20W MF 201

C8966 0.22UF 20% 6.3V X6S-CERM 0201

GFXIMVP_ISNS2_N

PLACE_NEAR=Q8961.3:1mm XW8931 SM

C8910 5600PF 10% 16V CERM 201

R8910 1.24K 1% 1/20W MF 201

C8912 NOSTUFF 0.1UF 10% 6.3V X6S 0201

R8911 1.15K 1% 1/20W MF 201

C8911 0.1UF 10% 6.3V X6S 0201

GFXIMVP_ISUMP_C

GFXIMVP_ISUMN

GPU VCORE VID STRAPS
DEFAULT = 0.9 V

=PP3V3_S0_GFX3V3BIAS

R8943 NOSTUFF 10K 1% 1/20W MF 201 GFXIMVP_VID<0>

R8944 NOSTUFF 10K 1% 1/20W MF 201 GFXIMVP_VID<1>

R8945 NOSTUFF 10K 1% 1/20W MF 201 GFXIMVP_VID<2>

R8946 NOSTUFF 10K 1% 1/20W MF 201 GFXIMVP_VID<3>

R8947 NOSTUFF 10K 1% 1/20W MF 201 GFXIMVP_VID<4>

R8948 NOSTUFF 10K 1% 1/20W MF 201 GFXIMVP_VID<5>

R8949 NOSTUFF 10K 1% 1/20W MF 201 GFXIMVP_VID<6>

R8950 10K 1% 1/20W MF 201

R8951 10K 1% 1/20W MF 201

R8952 10K 1% 1/20W MF 201

R8953 10K 1% 1/20W MF 201

R8954 NOSTUFF 10K 1% 1/20W MF 201

R8955 NOSTUFF 10K 1% 1/20W MF 201

R8956 10K 1% 1/20W MF 201

Stuff option for GPIO control

R8981 = PSI Control
R8982 = VID6 control (old connection)
R8982 = DPSLP Control

GFXIMVP_PSI_R_L (IN)

R8981 0 5% 1/20W MF 201 GFXIMVP_PSI_L

R8982 NOSTUFF 0 5% 1/20W MF 201 GFXIMVP_VID<6>

R8983 NOSTUFF 0 5% 1/20W MF 201 GFXIMVP_DPSLP_EN

=PP3V3_S0_GFX3V3BIAS

R8970 NOSTUFF 499 1% 1/20W MF 201

R8971 100K 5% 1/20W MF 201

R8974 NOSTUFF 100K 5% 1/20W MF 201

R8972 NOSTUFF 100K 5% 1/20W MF 201

R8973 100K 5% 1/20W MF 201

GFXIMVP_VR_TT_L
GFXIMVP_PSI_L
GFXIMVP_DPSLP_EN

Do not config

PSI_L = HIGH & DPSLP_EN = HIGH

SYNC_MASTER=D2_SEAN SYNC_DATE=03/05/2012

PAGE TITLE: GFX IMVP VCore Regulator

Apple Inc.

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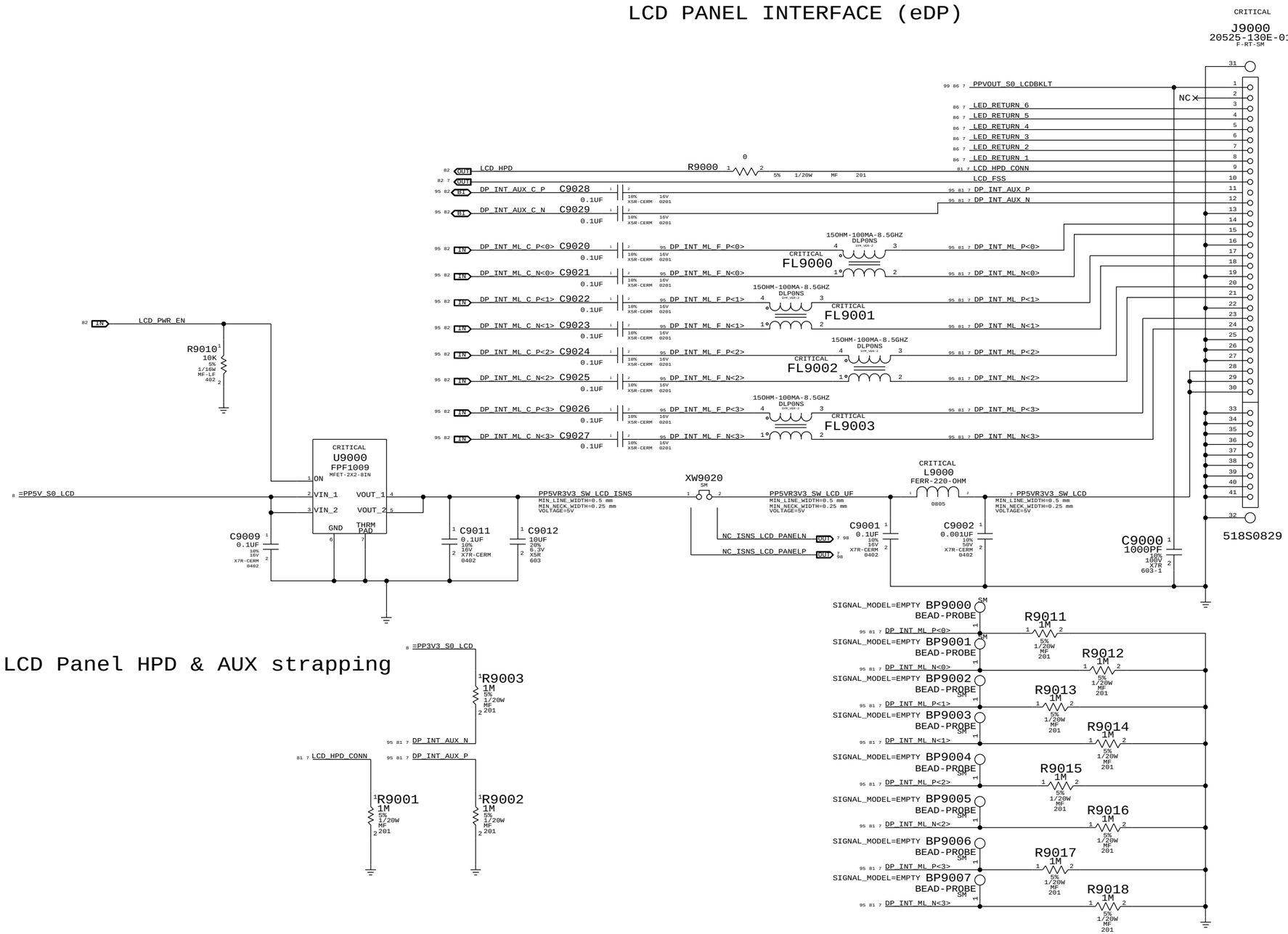
LCD PANEL INTERFACE (eDP)



SYNC MASTER=D2_KEPLER	SYNC DATE=01/13/2012
PAGE TITLE	eDP Display Connector
Apple Inc.	DRAWING NUMBER 051-9589 SIZE D
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OMIT_TABLE

TP_DPMUX_UC_P10	B12	P10/WUE0*	
TP_DPMUX_UC_P11	A13	P11/WUE1*	
TP_DPMUX_UC_P12	A12	P12/WUE2*	
TP_DPMUX_UC_P13	B13	P13/WUE3*	
TP_DPMUX_UC_P14	D11	P14/WUE4*	
TP_DPMUX_UC_P15	C13	P15/WUE5*	
TP_DPMUX_UC_P16	C12	P16/WUE6*	
TP_DPMUX_UC_P17	D10	P17/WUE7*	
EG_RAIL1_EN	D13	P20	
EG_RAIL2_EN	E11	P21	
EG_RAIL3_EN	D12	P22	
EG_RAIL4_EN	F11	P23	
EG_RAIL5_EN	E13	P24	
EG_CLKREQ_OUT_L	E12	P25	
EG_RESET_L	F13	P26	
FB_CLAMP	E10	P27	
LPC_AD<0>	A9	P30/LAD0	
LPC_AD<1>	D9	P31/LAD1	
LPC_AD<2>	C8	P32/LAD2	
LPC_AD<3>	B7	P33/LAD3	
LPC_FRAME_L	A8	P34/LFRAM*	
DPMUX_LRESET_L	D8	P35/LRESET*	
LPC_CLK33M_DPMUX_UC	D7	P36/LCLK	
TP_DPMUX_UC_P37	D6	P37/SERIRQ	
TP_DPMUX_UC_P40	D4	P40/TMI0/TCMCYI0	
TP_DPMUX_UC_P41	A5	P41/TMO0/TCMCKI0/TCMMCI0	
TP_DPMUX_UC_P42	B4	P42/TCMCYI1	
LCD_FSS	A1	P43/TMI1/TCMCKI1/TCMMCI1	
LCD_MUX_SEL	C2	P44/TMO1/PWMU2B/TCMCYI2	
TP_DPMUX_UC_P45	B2	P45/PWMU3B/TCMCKI2/TCMMCI2	
TP_DPMUX_UC_P46	C1	P46/PWMU4B	
TP_DPMUX_UC_P47	C3	P47/PWMU5B	
DPMUX_UC_TX	G2	P50/FTXD	
DPMUX_UC_RX	F3	P51/FRXD	
TP_DPMUX_UC_P52	E4	P52/SCL0	
P60/KIN0*	L13	DP_EXTA_MUX_EN	OUT
P61/KIN1*	K12	DP_EXTA_MUX_SEL_EG	OUT
P62/KIN2*	K11	TP_DPMUX_UC_P62	
P63/KIN3*	J12	TP_DPMUX_UC_P63	
P64/KIN4*	K13	DP_EXTB_MUX_EN	OUT
P65/KIN5*	J10	DP_EXTB_MUX_SEL_EG	OUT
P66/KIN6*	J11	TP_DPMUX_UC_P66	
P67/IRQ7*/KIN7*	H12	TP_DPMUX_UC_P67	
P70/AN0	N10	DPMUX_UC_UNUSED	
P71/AN1	M11	DPMUX_UC_UNUSED	
P72/AN2	L10	DPMUX_UC_UNUSED	
P73/AN3	N11	DPMUX_UC_UNUSED	
P74/AN4	N12	DPMUX_UC_UNUSED	
P75/AN5	M13	DPMUX_UC_UNUSED	
P76/AN6	N13	DPMUX_UC_UNUSED	
P77/AN7	L12	DPMUX_UC_UNUSED	
P80/PME*	A7	TP_DPMUX_UC_P80	
P81/GA20	B6	TP_DPMUX_UC_P81	
P82/CLKRUN*	C7	TP_DPMUX_UC_P82	
P83/LPCPD*	D5	TP_DPMUX_UC_P83	
P84/IRQ3*/TXD1	A6	DPMUX_UC_BOOT_TX	OUT
P85/IRQ4*/RXD1	B5	DPMUX_UC_BOOT_RX	IN
P86/IRQ5*/SCK1	C6	TP_LCD_IRQ	
P90/IRQ2*	J4	DP_TBTPA_HPD_BUF	IN
P91/IRQ1*	G3	DP_TBTPB_HPD_BUF	IN
P92/IRQ0*	H2	DP_TBTSNK0_HPD	IN
P93/IRQ12*	G1	DP_TBTSNK1_HPD	IN
P94/IRQ13*	H4	DP_A_CA_DET_BUF	IN
P95/IRQ14*	G4	DP_B_CA_DET_BUF	IN
P96/EXCL	F4	TP_DPMUX_UC_P96	
P97/SDA0/IRQ15*	F1	TBT_DDC_XBAR_EN_L	IN

CONNECT I2C TO LCD BKLT IC

U9100 R4F2113NLG TLP-145V SYM 2 OF 3

OMIT_TABLE

=I2C_DPMUX_UC_SDA	N3	PA0/KIN8*/SDA1	
=I2C_DPMUX_UC_SCL	N1	PA1/KIN9*/SCL1	
DPMUX_UC_IRQ	M3	PA2/KIN10*/PS2AC	
DPMUX_UC_UNUSED	M2	PA3/KIN11*/PS2AD	
DPMUX_UC_UNUSED	N2	PA4/KIN12*/PS2BC	
DPMUX_UC_UNUSED	L1	PA5/KIN13*/PS2BD	
DPMUX_UC_UNUSED	K3	PA6/KIN14*/PS2CC	
FB_CLAMP_TOGGLE_REQ_L	L2	PA7/KIN15*/PS2CD	
TP_DPA_EG_HPD	B8	PB0/LSMI*	
TP_DPB_EG_HPD	C9	PB1/LSCI	
DP_TBTSNK0_HPD_EG	B9	PB2/RI*/PWMU0B	
DP_TBTSNK1_HPD_EG	A10	PB3/DCD*/PWMU1B	
DP_EXTA_CA_DET_EG	C10	PB4/DSR*/FSIDO	
DP_EXTB_CA_DET_EG	B10	PB5/DTR*/FSIDI	
HDMI_EG_HPD	C11	PB6/CTS*/FSICK	
DP_INT_EG_HPD	A11	PB7/RTS*/FSISS	
LCD_PWR_EN	G11	PC0/TIOCA0/WUE8*	
LCD_BKLT_EN	G13	PC1/TIOCB0/WUE9*	
TP_DPMUX_UC_PC2	F12	PC2/TIOCC0/TCLKA/WUE10*	
TP_DPMUX_UC_PC3	H13	PC3/TIOCD0/TCLKB/WUE11*	
LCD_MUX_EN	G10	PC4/TIOCA1/WUE12*	
TP_LCD_MUX_REQ	G12	PC5/TIOCB1/TCLKC/WUE13*	
LCD_BKLT_PWM	H11	PC6/TIOCA2/WUE14*	
DP_DDC_MUX_CROSSBAR_L	J13	PC7/TIOCB2/TCLKD/WUE15*	
TP_DPA_IG_HPD	M10	PD0/AN8	
TP_DPB_IG_HPD	N9	PD1/AN9	
DP_TBTSNK0_HPD_IG	K10	PD2/AN10	
DP_TBTSNK1_HPD_IG	L8	PD3/AN11	
TP_DP_EXTA_CA_DET_IG	M9	PD4/SSO	
TP_DP_EXTB_CA_DET_IG	N8	PD5/SSI	
TP_HDMI_IG_HPD	K9	PD6/SSCK	
DP_INT_IG_HPD	L7	PD7/SCS	
PE0/EXEXCL	K1	DPMUX_UC_CLK32K	
PE1/ETCK	J3	DPMUX_UC_TCK	
PE2/ETDI	K2	DPMUX_UC_TDI	
PE3/ETDO	J1	DPMUX_UC_TDO	
PE4/ETMS	K4	DPMUX_UC_TMS	
PE5/ETRST*	H3	DPMUX_UC_TRST_L	
PF0/IRQ8*/PWMU0A	K5	EG_LCD_PWR_EN	IN
PF1/IRQ9*/PWMU1A	N5	EG_BKLT_EN	IN
PF2/IRQ10*/TMOY	M6	PM_ALL_GPU_PGOOD	IN
PF3/IRQ11*/TMOX	L5	EG_CLKREQ_IN_L	IN
PF4/PWMU2A/EXDSR	M5	GPU_PGOOD4	IN
PF5/PWMU3A/EXDTR	N4	GPU_PGOOD3	IN
PF6/PWMU4A/EXCTS	L4	GPU_PGOOD2	IN
PF7/PWMU5A/EXRTS	M4	GPU_PGOOD1	IN
PG0/EXIRQ8*/TMIX/SDAA	M8	=I2C_DPMUX_A_SDA	BI
PG1/EXIRQ9*/TMIY/SCLA	N7	=I2C_DPMUX_A_SCL	OUT
PG2/EXIRQ10*/SDAB	K8	DPMUX_UC_UNUSED	
PG3/EXIRQ11*/SCLB	K7	DPMUX_UC_UNUSED	
PG4/EXIRQ12*/SDAC	K6	DPMUX_UC_UNUSED	
PG5/EXIRQ13*/SCLC	N6	DPMUX_LRESET_L	IN
PG6/EXIRQ14*/SDAD	M7	HDMI_HPD_BUF	IN
PG7/EXIRQ15*/SCLD	L6	LCD_HPD	IN
PH0/IRQ6*	E2	IG_LCD_PWR_EN	IN
PH1/EXIRQ7*	F2	IG_BKLT_EN	IN
PECI	A4	DPMUX_UC_PECI	
PEVREF	B3	DPMUX_UC_PEVREF	

PU OFFPAGE

J9100 1909782 M-RT-SM

DPMUX_DEBUG

DPMUX UC DEBUG HEADER

Q9190 SSM3K15FV SOD-VESM-HF

DPMUX UC PULL-UPS

DPMUX_UC_NMI	R9110	10K	NOSTUFF
DPMUX_UC_TRST_L	R9111	10K	NOSTUFF
DPMUX_UC_MD1	R9112	10K	NOSTUFF
DPMUX_UC_MD2	R9113	10K	NOSTUFF
DPMUX_UC_CLK32K	R9114	10K	NOSTUFF
DPMUX_UC_TCK	R9115	10K	NOSTUFF
DPMUX_UC_TDI	R9116	10K	NOSTUFF
DPMUX_UC_TDO	R9117	10K	NOSTUFF
DPMUX_UC_TMS	R9118	10K	NOSTUFF
EG_CLKREQ_OUT_L	R9119	100K	NOSTUFF PU on PCH Page
DPMUX_UC_RESET_L	R9140	100K	NOSTUFF

HDMI HPD INVERSION & ISOLATION

U9110 74LVC1G00GF SOT891

HDMI_HPD_L → HDMI_HPD_BUF

CA_DET ISOLATION

Q9110 SSM6N37FEAPE SOT563

TBT_A_CONFIG1_BUF → DP_A_CA_DET_BUF (R9160 100K)

TBT_B_CONFIG1_BUF → DP_B_CA_DET_BUF (R9161 100K)

DP 2:1 ANALOG MUX

U9150 CBTL06142EEE TFBGA CRITICAL

DP_INT_IG_ML_P<0>	B4	DIN1_0+	
DP_INT_IG_ML_N<0>	A4	DIN1_0-	
DP_INT_IG_ML_P<1>	B5	DIN1_1+	
DP_INT_IG_ML_N<1>	A5	DIN1_1-	
DP_INT_IG_ML_P<2>	B6	DIN1_2+	
DP_INT_IG_ML_N<2>	A6	DIN1_2-	
DP_INT_IG_ML_P<3>	A8	DIN1_3+	
DP_INT_IG_ML_N<3>	A9	DIN1_3-	
DP_INT_IG_AUX_P	H9	DAUX1+	
DP_INT_IG_AUX_N	J9	DAUX1-	
NC	H8	DDC_CLK1	
NC	J8	DDC_DAT1	
NC	J2	HPD_1	
DP_INT_EG_ML_P<0>	B8	DIN2_0+	
DP_INT_EG_ML_N<0>	B9	DIN2_0-	
DP_INT_EG_ML_P<1>	D8	DIN2_1+	
DP_INT_EG_ML_N<1>	D9	DIN2_1-	
DP_INT_EG_ML_P<2>	E8	DIN2_2+	
DP_INT_EG_ML_N<2>	E9	DIN2_2-	
DP_INT_EG_ML_P<3>	F8	DIN2_3+	
DP_INT_EG_ML_N<3>	F9	DIN2_3-	
DP_INT_EG_AUX_P	H6	DAUX2+	
DP_INT_EG_AUX_N	J6	DAUX2-	
NC	H5	DDC_CLK2	
NC	J5	DDC_DAT2	
NC	H3	HPD_2	
LCD_MUX_SEL	A1	GPU_SEL	
LCD_MUX_EN	B7	XSD*	
		DDC_AUX_SEL	C2
DOUT_0+	B2	DP_INT_ML_C_P<0>	OUT
DOUT_0-	B1	DP_INT_ML_C_N<0>	OUT
DOUT_1+	D2	DP_INT_ML_C_P<1>	OUT
DOUT_1-	D1	DP_INT_ML_C_N<1>	OUT
DOUT_2+	E2	DP_INT_ML_C_P<2>	OUT
DOUT_2-	E1	DP_INT_ML_C_N<2>	OUT
DOUT_3+	F2	DP_INT_ML_C_P<3>	OUT
DOUT_3-	F1	DP_INT_ML_C_N<3>	OUT
AUX+	H2	DP_INT_AUX_C_P	BI
AUX-	H1	DP_INT_AUX_C_N	BI
HPDIN	J1	DPMUX_HPD_PD	R9162 100K

DPMUX UC PULL-DOWNS

DPMUX_UC_RESET_L	R9120	10K	NOSTUFF
EG_RAIL1_EN	R9121	10K	
EG_RAIL2_EN	R9122	10K	
EG_RAIL3_EN	R9123	10K	
EG_RAIL4_EN	R9124	10K	
EG_RAIL5_EN	R9125	10K	
LCD_PWR_EN	R9126	10K	NOSTUFF PD on LCD Page
LCD_BKLT_EN	R9127	10K	
LCD_BKLT_PWM	R9128	10K	
DPMUX_UC_NMI	R9129	10K	NOSTUFF
DPMUX_UC_MD1	R9130	10K	NOSTUFF
DPMUX_UC_MD2	R9131	10K	NOSTUFF
DPMUX_UC_PECI	R9132	10K	
DPMUX_UC_PEVREF	R9133	10K	
DPMUX_UC_UNUSED	R9134	10K	
EG_RESET_L	R9135	100K	
DPA_IG_HPD	R9136	100K	
DP_TBTSNK0_HPD_EG	R9137	100K	
DPB_IG_HPD	R9138	100K	
DP_TBTSNK1_HPD_EG	R9139	100K	
DP_INT_IG_HPD	R9145	100K	
DP_INT_EG_HPD	R9146	100K	

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OMIT_TABLE

DPMUX_UC_XTAL	A3	XTAL	
DPMUX_UC_EXTAL	A2	EXTAL	
DPMUX_UC_RESET_L	D3	RES*	
DPMUX_UC_MD1	D1	MD1	
DPMUX_UC_MD2	H1	MD2	
DPMUX_UC_NMI	E3	NMI	
NC	E5	NC	
MDCKN	C4		

DPMUX:XTAL Y9100 2.50X2.00MM-SM

DPMUX:XTAL R9151 0

DPMUX:XTAL C9140 15PF, C9141 15PF

DPMUX:HOCO R9150 10K

C9100 / C9101 / C9102 / C9103 0.1UF 20% 10V X7R-CERM 0402

C9104 0.1UF 20% 10V X7R-CERM 0402

C9105 0.47UF 10% 6.3V X6S-CERM 0402

C9150 / C9151 0.1UF 20% 10V X7R-CERM 0402

R9100 / R9101 0 5% 1/16W MF-LF 402

R9102 0 NOSTUFF

SYNC_MASTER=D2_SEAN	SYNC_DATE=03/05/2012
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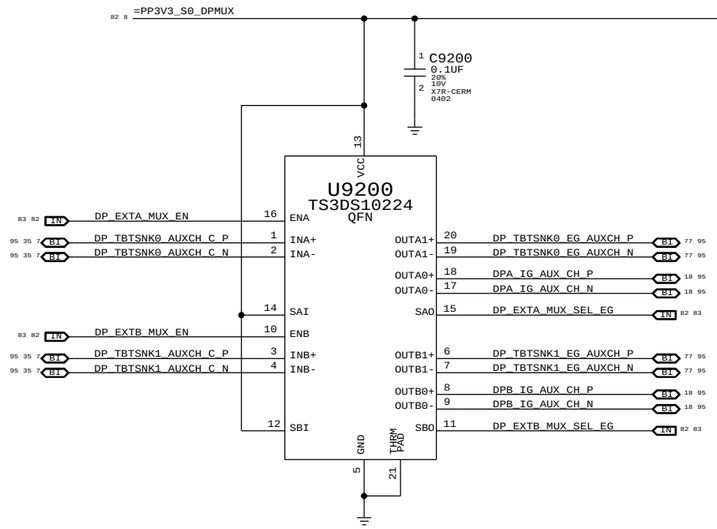
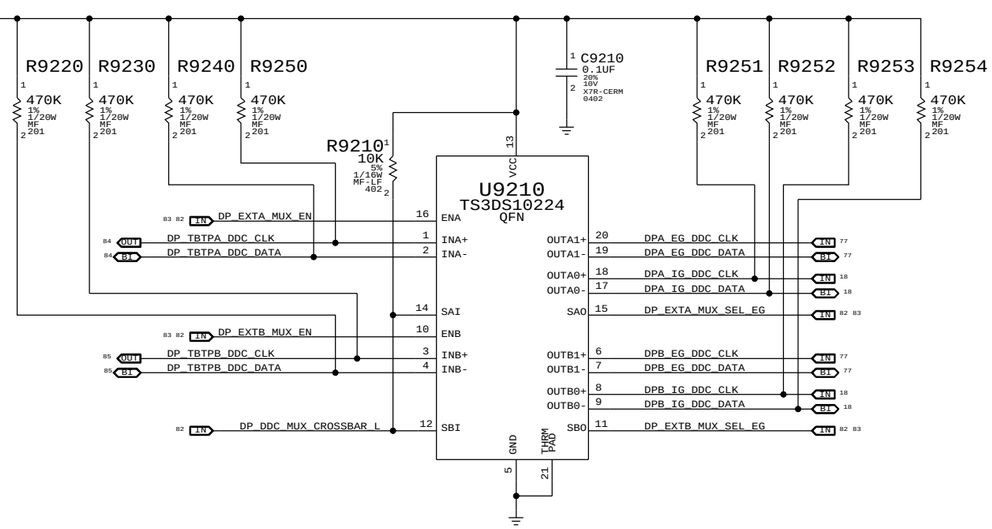
DP A & DP B AUX MUX



DP A & DP B DDC MUX



MUX TRUTH TABLE

SAI/SBI	SAO	SBO	INA	INB
0	0	0	OUTB0	OUTA0
0	0	1	OUTB1	OUTA0
0	1	0	OUTB0	OUTA1
0	1	1	OUTB1	OUTA1
1	0	0	OUTA0	OUTB0
1	0	1	OUTA0	OUTB1
1	1	0	OUTA1	OUTB0
1	1	1	OUTA1	OUTB1

SYNC_MASTER=D2_SEAN SYNC_DATE=03/05/2012

PAGE TITLE: eDP Muxed Graphics Support

Apple Inc.

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3.3V/HV Power MUX

V3P3 must be S4 to support wake from Thunderbolt devices.

	Nominal	Min	Max
IV3P3	1100mA	1030mA	1200mA
IHVS0	890mA	830mA	930mA (assumes 15V, 12W minimum)
IHVS3	890mA	830mA	930mA (assumes 3S, 9-12.6V, 7.5-11.7W)

=PP3V3_S4_TBTAPWRSW

CRITICAL C9487 100UF 20% 6.3V POLY-TANT CASE-B2-SM; C9480 22UF 20% 6.3V X5R-CERM-1 603; C9481 0.1UF 10% 16V X5R-CERM 0201

=PPHV_SW_TBTAPWRSW 18.9V Max

C9415 4.7UF 10% 25V X5R-CERM 0603; C9410 0.1UF 10% 25V X5R 402

U9410 CRITICAL CD3210A0RGP QFN

V3P3 (19, 20); VHV (6, 7); RSVD (16); EN (5); HV_EN (11); S0 (17); GND; THRM PAD

=TBTAPWRSW_EN; TBT_A_HV_EN; =TBT_S0_EN

V3P3OUT (18); OUT (12); RSVD (15); ISET_V3P3 (8); ISET_S0 (10); ISET_S3 (9)

C9485 0.1UF 10% 16V X5R-CERM 0201; C9486 10UF 20% 6.3V CERM-X5R 0402; C9411 0.1UF 10% 25V X5R 402

PP3V3_SW_TBTAPWR (MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=3.3V)

PPHV_SW_TBTAPWR (MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=15V)

TBTAPWRSW_ISET_V3P3; TBTAPWRSW_ISET_S0; TBTAPWRSW_ISET_S3

TBTHV:P15V R9410 22.6K 1% 1/20W MF 201; R9411 22.6K 1% 1/20W MF 201; R9412 36.5K 1% 1/20W MF 201 <RV3P3>

12V: See below

TBTAPWRSW_ISET_S3_R; TBTAPWRSW_ISET_S0_R

R9413 22.6K 1% 1/20W MF 201 <RHVS3>; R9414 22.6K 1% 1/20W MF 201 <RHVS0>

Single-fault protection requires two R_S_per HV ISET_SX with tps3210. Single R on ISET_V3P3 OK.

ILIM = 40000 / RISET

For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R9410,R9413		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R9411,R9414		TBTHV:P12V

	Nominal	Min	Max
IHVS0/S3	1120mA	1090mA	1170mA (12W minimum)

Thunderbolt Connector A

PP3V3_SW_TBTAPWR

C9420 0.1UF 10% 16V X5R-CERM 0201; C9421 0.1UF 10% 16V X5R-CERM 0201

R9427 10K 5% 1/20W MF 201; R9429 100K 5% 1/20W MF 201

VDD

CRITICAL U9420 CBTL05023 HVQFN

SIGNAL_MODEL=TBT_MUX

TBT_A_CIO_SEL	35 IN	1	BIASIN
DP_AUXIO_EN	85 25 IN	2	AUXIO_EN
DP_TBTPA_AUXCH_C_N	93 35 BI	7	AUX-
DP_TBTPA_AUXCH_C_P	93 35 BI	8	AUX+
DP_TBTPA_DDC_DATA	83 BI	4	DDC_DAT
DP_TBTPA_DDC_CLK	83 IN	5	DDC_CLK
TBT_A_CONFIG1_BUF	82 35 OUT	16	CA_DETOUT
DP_TBTPA_ML_C_P<1>	93 IN	11	DP+
DP_TBTPA_ML_C_N<1>	93 IN	10	DP-
TBT_A_LSTX	35 IN	14	LSTX
TBT_A_LSRX_UNBUF		13	LSRX
TBT_A_DP_PWRDN	35 IN	6	DP_PD
DP_TBTPA_HPD	35 OUT	12	HPDOUT

BIASOUT	24	TBT_A_BIAS	VOLTAGE=3.3V
AUXIO-	23	DP_A_AUXCH_DDC_N	84 93
AUXIO+	22	DP_A_AUXCH_DDC_P	84 93
CA_DET	18	TBT_A_CONFIG1_RC	84
DPML0+	19	DP_A_LSX_ML_P<1>	84 93
DPML0-	20	DP_A_LSX_ML_N<1>	84 93
HPD	17	TBT_A_HPD	84

GND_THMPAD (9, 21, 25)

C9425 0.1UF 10% 16V X5R-CERM 0201

TBT: RX_1 Bias Sink

TBT: LSX_A_R2P/P2R (P/N)

R9426 1M 5% 1/20W MF 201; R9428 100K 5% 1/20W MF 201

C9430 0.1UF 10% 16V X5R-CERM 0201; C9431 0.1UF 10% 16V X5R-CERM 0201

C9432 0.22UF 20% 6.3V X5R 0201; C9433 0.22UF 20% 6.3V X5R 0201

PP3V3_SW_TBTAPWR

CRITICAL U9460 74AUP1T97 SOT891 5

TBT_A_LSRX; Y = B

C9460 0.1UF 10% 16V X5R-CERM 0201

CRITICAL L9400 FERR-120-OHM-3A 0603

PP3V3RHV_SW_TBTAPWR (MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=15V)

C9400 0.01UF 10% 50V X7R-CERM 0402

TBTACONN_20_RC (MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=18V)

R9401 12 5% 1/20W MF 201

C9401 0.01UF 10% 50V X7R-CERM 0402

For J9400 TBT SMT pads (3, 5, 17 & 19):

TBTACONN_1_C (MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=18.9V)

GND_VOID=TRUE C9405 0.01UF 10% 25V X5R-CERM 0201

TBTACONN_7_C (MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=18.9V)

GND_VOID=TRUE C9406 0.01UF 10% 25V X5R-CERM 0201

J9400 MDP-D2 F-RT-TH

SHIELD PINS S16 S15 S14 S13 S12

B2	HPD	GND0	B1
B4	CONFIG1	ML_LANE0P	B3
B6	CONFIG2	ML_LANE0N	B5
B8	GND2	GND1	B7
B10	ML_LANE3P	ML_LANE1P	B9
B12	ML_LANE3N	ML_LANE1N	B11
B14	GND4	GND3	B13
B16	AUX_CHP	ML_LANE2P	B15
B18	AUX_CHN	ML_LANE2N	B17
B20	DP_PWR	RETURN	B19

PORT B

SHIELD PINS S22 S21 S20 S19 S18 S17

514-0803

TBT Dir; DP Dir

(0-18.9V)

TBT_A_R2D_P<0>; TBT_A_R2D_N<0>

TBT: TX_0

C9470 0.22UF; C9471 0.22UF (GND_VOID=TRUE (Both C's))

R9470 470K; R9471 470K

TBT_A_R2D_C_P<0>; TBT_A_R2D_C_N<0>

(0-18.9V)

DP_A_LSX_ML_P<1>; DP_A_LSX_ML_N<1>

TBT: LSX_R2P/P2R (P/N)

TBT_A_R2D_P<1>; TBT_A_R2D_N<1>

TBT: TX_1

C9472 0.22UF; C9473 0.22UF (GND_VOID=TRUE (Both C's))

R9472 470K; R9473 470K

TBT_A_R2D_C_P<1>; TBT_A_R2D_C_N<1>

470K R's for ESD protection on AC-coupled signals.

C9474 0.47UF; C9475 0.47UF (GND_VOID=TRUE (Both C's))

TBT_A_D2R_P<0>; TBT_A_D2R_N<0>

TBT_A_D2R_C_P<0>; TBT_A_D2R_C_N<0>

R9494 1K 5% 1/20W MF 201 SIGNAL_MODEL=EMPTY; R9495 1K 5% 1/20W MF 201 SIGNAL_MODEL=EMPTY

R9478 470K 5% 1/20W MF 201; R9479 470K 5% 1/20W MF 201

C9478 0.22UF; C9479 0.22UF

DP_TBTPA_ML_C_P<3>; DP_TBTPA_ML_C_N<3>

TBT: Unused

TBT_A_BIAS

R9498 2.2K 5% 1/20W MF 201; R9499 2.2K 5% 1/20W MF 201

C9476 0.47UF; C9477 0.47UF (GND_VOID=TRUE (Both C's))

TBT_A_D2R_P<1>; TBT_A_D2R_N<1>

TBT_A_D2R_C_P<1>; TBT_A_D2R_C_N<1>

CRITICAL SIGNAL_MODEL=TBTPIN GND_VOID=TRUE (Both D's)

D9498 BAR90-02LRH TSLP-2-7; D9499 BAR90-02LRH TSLP-2-7

TBT_A_D2R1_AUXDDC_P; TBT_A_D2R1_AUXDDC_N

CRITICAL L9498 650NH-5%-0.430MA-0.52OHM 0603 SIGNAL_MODEL=EMPTY

CRITICAL L9499 650NH-5%-0.430MA-0.52OHM 0603 SIGNAL_MODEL=EMPTY

DP_A_AUXCH_DDC_P; DP_A_AUXCH_DDC_N

C9498 30PF 5% 50V C0G-NP0 0402; C9499 30PF 5% 50V C0G-NP0 0402

TBT_A_HPD; TBT_A_CONFIG1_RC; TBT_A_CONFIG2_RC

R9452 1M 5% 1/20W MF 201; R9451 1M 5% 1/20W MF 201

C9494 330PF 10% 16V X7R-CERM 0201; C9495 330PF 10% 16V X7R-CERM 0201

R9441 100K 5% 1/20W MF 201

C9402 0.01UF 10% 16V X5R-CERM 0201

DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

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3.3V/HV Power MUX

V3P3 must be S4 to support wake from Thunderbolt devices.

	Nominal	Min	Max
IV3P3	1100mA	1030mA	1200mA
IHVS0	890mA	830mA	930mA (assumes 15V, 12W minimum)
IHVS3	890mA	830mA	930mA (assumes 3S, 9-12.6V, 7.5-11.7W)

=PP3V3_S4_TBTBPWRSW
CRITICAL C9687 100UF 20% 6.3V POLY-TANT CASE-B2-SM; C9680 22UF 20% 6.3V X5R-CERM-1 603; C9681 0.1UF 10% 16V X5R-CERM 0201
=PPHV_SW_TBTBPWRSW
18V Max
C9615 4.7UF 10% 25V X5R-CERM 0603; C9610 0.1UF 10% 25V X5R 402
CRITICAL U9610 CD3210A0RGP QFN
V3P3 (19, 20); VHV (6, 7); RSVD (16); EN (5); HV_EN (11); S0 (17); S3 (9); GND; THRM PAD
V3P3OUT (18); OUT (12); RSVD (15); ISET_V3P3 (8); ISET_S0 (10); ISET_S3 (9)
C9685 0.1UF 10% 16V X5R-CERM 0201; C9686 10UF 20% 6.3V CERM-X5R 0402; C9611 0.1UF 10% 25V X5R 402
PP3V3_SW_TBTBPWR — MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=3.3V
PPHV_SW_TBTBPWR — MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=15V
=TBTBPWRSW_EN
TBT_B_HV_EN
=TBT_S0_EN
TBTBPWRSW_ISET_V3P3
TBTBPWRSW_ISET_S0
TBTBPWRSW_ISET_S3
12V: See below
TBTHV:P15V R9610 22.6K 1% 1/20W MF 201
TBTHV:P15V R9611 22.6K 1% 1/20W MF 201
R9612 36.5K 1% 1/20W MF 201 <RV3P3>
TBTBPWRSW_ISET_S3_R
TBTBPWRSW_ISET_S0_R
TBTHV:P15V R9613 22.6K 1% 1/20W MF 201 <RHVS3>
TBTHV:P15V R9614 22.6K 1% 1/20W MF 201 <RHVS0>
Single-fault protection requires two R's per HV ISET_SX with CD3210. Single R on ISET_V3P3 OK.
ILIM = 40000 / RISET

For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R9610,R9613		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R9611,R9614		TBTHV:P12V

	Nominal	Min	Max
IHVS0/S3	1120mA	1090mA	1170mA (12W minimum)

Thunderbolt Connector B

PP3V3_SW_TBTBPWR
C9620 0.1UF 10% 16V X5R-CERM 0201; C9621 0.1UF 10% 16V X5R-CERM 0201
R9627 10K 5% 1/20W MF 201; R9629 100K 5% 1/20W MF 201
SIGNAL_MODEL=TBT_MUX
CRITICAL U9620 CBTL05023 HVQFN — VDD; GND_THMPAD
TBT_B_BIAS — VOLTAGE=3.3V; C9625 0.1UF 10% 16V X5R-CERM 0201
TBT_B_CIO_SEL
DP_AUXIO_EN
DP_TBTPB_AUXCH_C_N; DP_TBTPB_AUXCH_C_P
C9630 0.1UF 10% 16V X5R-CERM 0201; C9631 0.1UF 10% 16V X5R-CERM 0201
DP_TBTPB_DDC_DATA
DP_TBTPB_DDC_CLK
TBT_B_CONFIG1_BUF
DP_TBTPB_ML_C_P<1>; DP_TBTPB_ML_C_N<1>
C9632 0.22UF 20% 6.3V X5R 0201; C9633 0.22UF 20% 6.3V X5R 0201
TBT_B_LSTX
TBT_B_LSRX_UNBUF
TBT_B_DP_PWRDN
DP_TBTPB_HPD
R9626 1M 5% 1/20W MF 201
R9628 100K 5% 1/20W MF 201
BIASIN, AUXIO_EN, AUX-, AUX+, DDC_DAT, DDC_CLK, CA_DETOUT, DP+, DP-, LSTX, LSRX, DP_PD, HPDOUT; BIASOUT, AUXIO-, AUXIO+, CA_DET, DPMLO+, DPMLO-, HPD
TBT_B_AUXCH_DDC_N; TBT_B_AUXCH_DDC_P — TBT: RX_1 Bias Sink
TBT_B_CONFIG1_RC
TBT_B_LSX_ML_P<1>; TBT_B_LSX_ML_N<1> — TBT: LSX_A_R2P/P2R (P/N)
TBT_B_HPD
PP3V3_SW_TBTBPWR
CRITICAL U9660 74AUP1T97 SOT891 5
TBT_B_LSRX — Y = B
C9660 0.1UF 10% 16V X5R-CERM 0201

CRITICAL L9600 FERR-120-OHM-3A 0603
PP3V3RHV_SW_TBTBPWR — MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=15V
C9600 0.01UF 10% 50V X7R-CERM 0402
TBTBCONN_20_RC — MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=18V
R9601 12 5% 1/20W MF 201
C9601 0.01UF 10% 50V X7R-CERM 0402

TBTBCONN_1_C — MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=18.9V
C9605 0.01UF 10% 25V X5R-CERM 0201
GND_VOID=TRUE
(0-18.9V)
DP Dir; TBT Dir
TBT: TX_0
TBTBCONN_7_C — MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=18.9V
C9606 0.01UF 10% 16V X5R-CERM 0201
(0-18.9V)
TBT: LSX_R2P/P2R (P/N)
TBT: TX_1

For J9600 TBT SMT pads (3, 5, 17 & 19):
TBT Dir; DP Dir
SHIELD PINS S5 S4 S3 S2 S1
J9400 MDP-D2 F-RT-TH
PORT A
HPD, CONFIG1, CONFIG2, GND2, ML_LANE3P, ML_LANE3N, GND4, AUX_CHP, AUX_CHN, DP_PWR
GND0, ML_LANE0P, ML_LANE0N, GND1, ML_LANE1P, ML_LANE1N, GND3, ML_LANE2P, ML_LANE2N, RETURN
SHIELD PINS S11 S10 S9 S8 S7 S6
514-0803

C9670 0.22UF; C9671 0.22UF — GND_VOID=TRUE (Both C's)
TBT_B_R2D_C_P<0>; TBT_B_R2D_C_N<0>
R9670 470K; R9671 470K
C9672 0.22UF; C9673 0.22UF — GND_VOID=TRUE (Both C's)
TBT_B_R2D_C_P<1>; TBT_B_R2D_C_N<1>
R9672 470K; R9673 470K
470K R's for ESD protection on AC-coupled signals.

C9674 0.47UF; C9675 0.47UF — GND_VOID=TRUE (Both C's)
TBT_B_D2R_P<0>; TBT_B_D2R_N<0>
R9694 1K; R9695 1K — SIGNAL_MODEL=EMPTY
R9678 470K; R9679 470K
C9678 0.22UF; C9679 0.22UF
DP_TBTPB_ML_C_P<3>; DP_TBTPB_ML_C_N<3>
TBT: Unused
TBT_B_BIAS
R9698 2.2K; R9699 2.2K
C9676 0.47UF; C9677 0.47UF — GND_VOID=TRUE (Both C's)
TBT_B_D2R_P<1>; TBT_B_D2R_N<1>
CRITICAL SIGNAL_MODEL=TBTPIN GND_VOID=TRUE (Both D's)
D9698 BAR90-02LRH TSLP-2-7; D9699 BAR90-02LRH TSLP-2-7
TBT_B_D2R1_AUXDDC_P; TBT_B_D2R1_AUXDDC_N
CRITICAL L9698 650NH-5%-0.430MA-0.52OHM 0603 — GND_VOID=TRUE; SIGNAL_MODEL=EMPTY
CRITICAL L9699 650NH-5%-0.430MA-0.52OHM 0603 — GND_VOID=TRUE; SIGNAL_MODEL=EMPTY
DP_B_AUXCH_DDC_P; DP_B_AUXCH_DDC_N
C9698 30PF 5% 50V C0G-NP0 0402; C9699 30PF 5% 50V C0G-NP0 0402
TBT_B_HPD
TBT_B_CONFIG1_RC
TBT_B_CONFIG2_RC
R9652 1M 5% 1/20W MF 201; R9651 1M 5% 1/20W MF 201
C9694 330PF 10% 16V X7R-CERM 0201; C9695 330PF 10% 16V X7R-CERM 0201
R9641 100K 5% 1/20W MF 201
C9602 0.01UF 10% 16V X5R-CERM 0201

DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

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PPBUS S0 LCDBkLT FET

MOSFET	FDC638APZ
CHANNEL	P-TYPE
RDS(ON)	43 mOhm @4.5V
LOADING	0.715 A (EDP)

THERE IS A SENSE RESISTOR BETWEEN PPBUS_SW_LCDBKLT_PWR AND PPBUS_SW_BKL ON THE SENSOR PAGE

NEED VALUE CHANGES FOR 55V AND 96 LEDS !!!

*L9710, Q9701, D9701, C9715-C9719 SHOULD ALL BE PLACED NEAR EACH OTHER.

C9715, C9716 SHOULD BE PLACED IN T-BONE. SAME FOR C9718,C9719

C9715, C9716 SHOULD BE PLACED ON TOP SIDE. PLACE C9718,C9719 ON BOTTOM SIDE

PPBUS_S0_LCDBKLT_PWR_SW SHOULD BE KEPT AS SHORT AS POSSIBLE

R9753 AND R9757 NEED TO BE 402 PACK FOR LAB ACCESS

LCD_BKLT_PWM SHOULD BE KEPT AWAY FROM BOOST CIRCUIT

PLACE XW9710 AWAY FROM U9701.1 AND U9701.15
ADD VIAS IN TPAD OF U9701

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	6	RES, 0OHM, 0402	R9717,R9718,R9719,R9720,R9721,R9722		D_BKL:PROD

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE: LCD Backlight Driver (LP8545)

Apple Inc.

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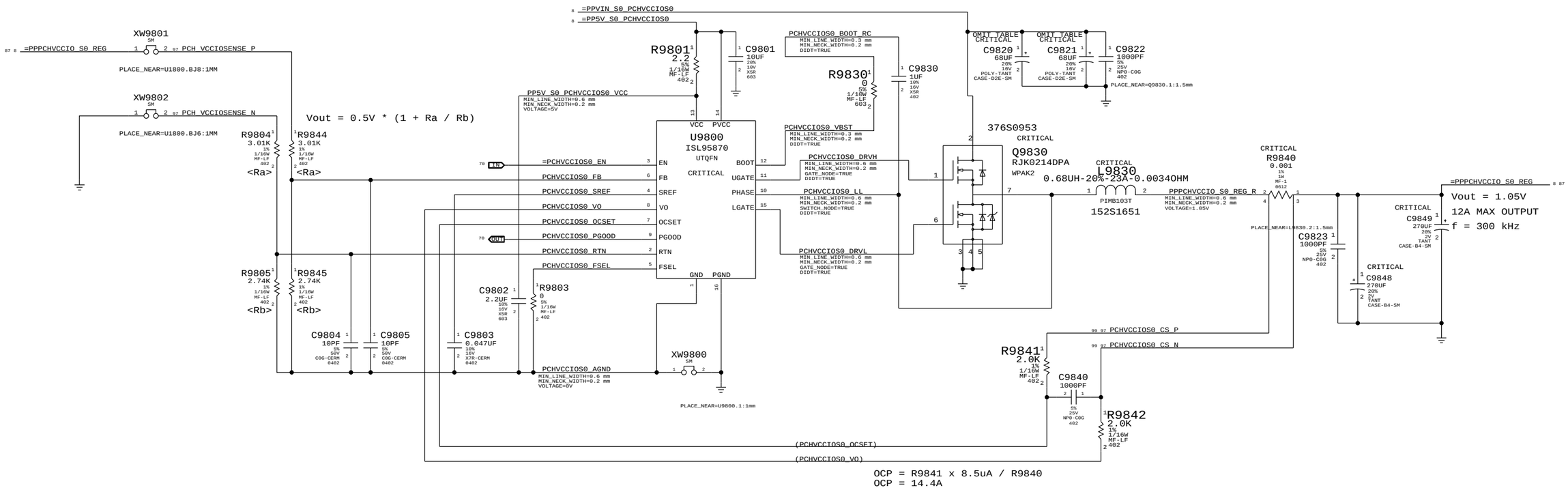
PCH VCCIO (1.05V S0) REGULATOR



SYNC_MASTER=D2_KEPLER	SYNC_DATE=01/13/2012
PAGE TITLE	PCH VCCIO (1.05V) POWER SUPPLY
Apple Inc.	DRAWING NUMBER 051-9589 · SIZE D
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GPU Rail Sequencing

KEPLER GPU REQUIRES RAILS TO COME
up in the following order:

1) GPU_3.3V
2) IFPX IOVDD - 1.8V
3) GPUVCORE
4) FBVDDQ/GDDR5 1.35V
5) PEXVDD/Q OR IFPY IOVDD - 1.05V

EG_RAIL1_EN	P3V3GPU_EN (MAKE_BASE=TRUE)	=P3V3GPU_MISC_EN	OUT	69
EG_RAIL2_EN	P1V8GPU_EN (MAKE_BASE=TRUE)	=P3V3GPU_EN	OUT	69
EG_RAIL3_EN	GPUVCORE_EN (MAKE_BASE=TRUE)	=P1V8GPU_EN	OUT	8
EG_RAIL4_EN	P1V35GPUFB_EN (MAKE_BASE=TRUE)	=GPUVCORE_EN	OUT	80
EG_RAIL5_EN	P1V05_S0GPU_EN (MAKE_BASE=TRUE)	=P1V35FB_EN	OUT	74
		=P1V05_GPU_EN	OUT	74

NOTE: 1V8 MAY NOT BE REQUIRED FOR KEPLER IF THERE IS NO LVDS

EXT GPU PWRGD Pullup

=PP3V3_S0_PWRCTL (88 70 8)

R9900 100K 5% 1/20W MF 201
R9901 100K 5% 1/20W MF 201
R9902 100K 5% 1/20W MF 201

69 8	=PP3V3_S0GPU_FET	GPU_PGOOD1	82
8	=PP1V8_GPU_FET	GPU_PGOOD2	82
80	GPUVCORE_PGOOD (MAKE_BASE=TRUE)	GPU_PGOOD3	82
74	GPUFB_PGOOD (MAKE_BASE=TRUE)	GPU_PGOOD4	82
74	P1V05_S0GPU_PGOOD (MAKE_BASE=TRUE)	PM_ALL_GPU_PGOOD	82

NOTE: NO PU ON 3V3 AND 1V8 PGOODS SINCE THEY ARE SYNTHETIC.

NOTE 2: CHECK IF 1V8 IS READ AS LOGIC HIGH BY GMUX

Unused PGOOD signal

=PP3V3_S0_PWRCTL (88 70 8)

NO STUFF
R9991 10K 5% 1/16W MF-LF 402

		CPUIMVP_AXG_PGOOD	IN 65
TP_DDRREG_PGOOD (MAKE_BASE=TRUE)	DDRREG_PGOOD	DDRREG_PGOOD	IN 64
TP_P1V5S3RS0_RAMP_DONE (MAKE_BASE=TRUE)	P1V5S3RS0_RAMP_DONE		IN 69

PEG_R2D_P<0> (71 89) — R9910 82 5% 1/20W MF 201 — NOSTUFF — PEG_R2D_N<0> (71 89)
PEG_R2D_P<5> (71 89) — R9915 82 5% 1/20W MF 201 — NOSTUFF — PEG_R2D_N<5> (71 89)
PEG_R2D_P<3> (71 89) — R9913 82 5% 1/20W MF 201 — NOSTUFF — PEG_R2D_N<3> (71 89)
PEG_R2D_P<7> (71 89) — R9917 82 5% 1/20W MF 201 — NOSTUFF — PEG_R2D_N<7> (71 89)

PLACE R9910 - R9917 CLOSE TO U8000

PCIE TEST STRUCTURES (FOR LAB USE)

PEG_D2R_P<0> (9 71 89) — R9920 82 5% 1/20W MF 201 — NOSTUFF — PEG_D2R_N<0> (9 71 89)
PEG_D2R_P<4> (9 71 89) — R9924 82 5% 1/20W MF 201 — NOSTUFF — PEG_D2R_N<4> (9 71 89)
PEG_D2R_P<7> (9 71 89) — R9927 82 5% 1/20W MF 201 — NOSTUFF — PEG_D2R_N<7> (9 71 89)

PLACE R9920 - R9927 CLOSE TO U1000

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE: Power Sequencing EG/PCH S0

Apple Inc.

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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	20 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_VID	*	0.457 MM	?
CPU_VREF	*	12 MIL	?

Most CPU signals with impedance requirements are 50-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: IVB PLATFORM DG , Tables 205-207

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	15 MIL	?
CLK_PCIE	*	20 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	15 MIL	?

PEG

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PEG_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PEG_RXRX	*	=4X_DIELECTRIC	?
PEG_TXTX	*	=4X_DIELECTRIC	?
PEG_TXRX	*	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PEG_D2R	PEG_D2R	*	PEG_RXRX
PEG_R2D	PEG_R2D	*	PEG_TXTX
PEG_D2R	PEG_R2D	*	PEG_TXRX

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DMI_S2N	PCIE_85D	PCIE	DMI_S2N_P<3:0>	10 18
DMI_S2N	PCIE_85D	PCIE	DMI_S2N_N<3:0>	10 18
DMI_N2S	PCIE_85D	PCIE	DMI_N2S_P<3:0>	10 18
DMI_N2S	PCIE_85D	PCIE	DMI_N2S_N<3:0>	10 18
FDI_DATA	PCIE_85D	PCIE	FDI_DATA_P<7:0>	9 10
FDI_DATA	PCIE_85D	PCIE	FDI_DATA_N<7:0>	9 10
FDI_FSYNC	CPU_50S	CPU_AGTL	FDI_FSYNC<1..0>	9 10
FDI_LSYNC	CPU_50S	CPU_AGTL	FDI_LSYNC<1..0>	9 10
FDI_INT	CPU_50S	CPU_AGTL	FDI_INT	10 18
1125 DMI_CLK100M	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_P	11 17
1126 DMI_CLK100M	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_N	11 17
1127 DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_IG_ML_P<3:0>	10 82
1128 DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_IG_ML_N<3:0>	10 82
1129 DP_INT_AUX	DP_85D	DISPLAYPORT	DP_INT_IG_AUX_P	10 82
1131 DP_INT_AUX	DP_85D	DISPLAYPORT	DP_INT_IG_AUX_N	10 82
1132 CPU_EDP_COMP	CPU_27P4S	CPU_COMP	CPU_EDP_COMP	10
1130 CPU_PEG_COMP	CPU_27P4S	CPU_COMP	CPU_PEG_COMP	10
1133 CPU_CFG	CPU_50S	CPU_ITP	CPU_CFG<17..0>	10 24
XDP_CLK_CPU	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_P	11 17
XDP_CLK_CPU	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_N	11 17
XDP_CLK_PCH	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_P	17 24
XDP_CLK_PCH	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_N	17 24
1138 DPLL_REF_CLK120M	CLK_PCIE_90D	CLK_PCIE	DPLL_REF_CLKP	9 11
1139 DPLL_REF_CLK120M	CLK_PCIE_90D	CLK_PCIE	DPLL_REF_CLKN	9 11
XDP_TDI	CPU_50S	CPU_ITP	XDP_CPU_TDI	11 24
XDP_TDO	CPU_50S	CPU_ITP	XDP_CPU_TDO	11 24
XDP_TMS	CPU_50S	CPU_ITP	XDP_CPU_TMS	11 24
XDP_TCK	CPU_50S	CPU_ITP	XDP_CPU_TCK	11 24
XDP_TRST_L	CPU_50S	CPU_ITP	XDP_CPU_TRST_L	11 24
XDP_BPM	CPU_50S	CPU_ITP	XDP_BPM_L<3..0>	11 24
XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<7..4>	11 24
1134 XDP_RESET_L	CPU_50S	CPU_ITP	XDP_DBRESET_L	11 24 25
1135 XDP_PRDY_L	CPU_50S	CPU_ITP	XDP_CPU_PRDY_L	11 24
1135 XDP_PREQ_L	CPU_50S	CPU_ITP	XDP_CPU_PREQ_L	11 24
CPU_CATERR_L	CPU_50S	CPU_AGTL	CPU_CATERR_L	11 41
1115 CPU_PROC_SEL_L	CPU_50S	CPU_AGTL	CPU_PROC_SEL_L	11 20
CPU_PECI	CPU_50S	CPU_VID	CPU_PECI	11 20 42
CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L	11 41 42 65
XDP_CPU_PWRGD	CPU_50S	CPU_ITP	XDP_CPU_PWRGD	24
PM_THRMTRIP_L	CPU_50S	CPU_BMIL	PM_THRMTRIP_L	11 20 42
PM_SYNC	CPU_50S	CPU_AGTL	PM_SYNC	11 18
PM_MEM_PWRGD	CPU_50S	CPU_AGTL	PM_MEM_PWRGD	11 18 27
1150 CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD	11 20 24
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<2..0>	11
	CPU_50S	CPU_VID	CPU_VIDSOUT	13 65
	CPU_50S	CPU_VID	CPU_VIDSCLK	13 65
	CPU_50S	CPU_VID	CPU_VIDALERT_L	13 65
	CPU_55S	CPU_VID	CPU_VCCSA_VID<1..0>	13 62
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	13 65
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	13 65
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCIOSENSE_P	13 67
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCIOSENSE_N	13 67
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_SENSE_P	13 65
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_SENSE_N	13 65
1120 CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_P	13
1121 CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_N	13
1122 CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_P	13
1123 CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_N	13
1137 CPU_VCCSASENSE	CPU_50S	CPU_AGTL	CPU_VCCSASENSE	13 62
1140 CPU_MEM_VREF		CPU_VREF	PPCPU_MEM_VREFDQ_A	10 33
1141 CPU_MEM_VREF		CPU_VREF	PPCPU_MEM_VREFDQ_B	10 33
1144 CPU_MEM_VREF		CPU_VREF	PP0V75_S3_MEM_VREFDQ_A	28 29 33
1145 CPU_MEM_VREF		CPU_VREF	PP0V75_S3_MEM_VREFDQ_B	30 31 33
1146 CPU_MEM_VREF		CPU_VREF	PP0V75_S3_MEM_VREFCA_A	28 29 33
1147 CPU_MEM_VREF		CPU_VREF	PP0V75_S3_MEM_VREFCA_B	30 31 33
1148 XDP_CLK_ITP	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_P	24
1149 XDP_CLK_ITP	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_N	24
	PEG_80D	PEG_R2D	PEG_R2D_P<7..0>	71 88
	PEG_80D	PEG_R2D	PEG_R2D_N<7..0>	71 88
PEG_R2D	PEG_80D	PEG_R2D	PEG_R2D_C_P<7..0>	9 71
	PEG_80D	PEG_R2D	PEG_R2D_C_N<7..0>	9 71
PEG_D2R	PEG_80D	PEG_D2R	PEG_D2R_P<7..0>	9 71 88
	PEG_80D	PEG_D2R	PEG_D2R_N<7..0>	9 71 88
	PEG_80D	PEG_D2R	PEG_D2R_C_P<7..0>	71
	PEG_80D	PEG_D2R	PEG_D2R_C_N<7..0>	71

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_37S	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=STANDARD	=STANDARD
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=3:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MILS	?
MEM_DQBL2BL	*	16 MILS	?
MEM_DQCH2CH	*	25 MILS	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_*	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_*	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_*	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DQ_BYTE*	MEM_*	*	MEM_DATA2MEM
MEM_*_DQ_BYTE*	=SAME	*	MEM_DATA2DATA
MEM_A_DQ_BYTE*	MEM_A_DQ_BYTE*	*	MEM_DQBL2BL
MEM_B_DQ_BYTE*	MEM_B_DQ_BYTE*	*	MEM_DQBL2BL
MEM_A_DQ_BYTE*	MEM_B_DQ_BYTE*	*	MEM_DQCH2CH

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_*	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*	*	*	MEM_2OTHER

DDR3 (Memory Down):
DQ signals should be matched within 0.508mm of associated DQS pair
DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.
DQS to clock matching should be within [CLK-139.73mm] and [CLK-30.48mm].
CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.508mm.
CONTROL signals should be matched within [CLK-2.54mm] to [CLK+0mm] of CLK pairs.
A/BA/CMD signals should be matched within [CLK-2.54mm] to [CLK+2.54mm] of CLK pairs.
DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.
Maximum length of any signal from die pad to first DRAM device is 139.7mm max, to last DRAM device is 194.31mm max.

SOURCE: Chief River SFF Platform DG, Rev 0.7 (#460452), Section 2.6.3

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_P<5..0>	12 28 29 32
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_N<5..0>	12 28 29 32
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_CKE<3..0>	12 28 29 32
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_CS_L<3..2>	
T101 MEM_A_CNTL1	MEM_37S	MEM_CTRL	MEM_A_CS_L<1>	12 29 32
T102 MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_CS_L<0>	12 28 32
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_ODT<3..2>	
T103 MEM_A_CNTL1	MEM_37S	MEM_CTRL	MEM_A_ODT<1>	12 29 32
T104 MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_ODT<0>	12 28 32
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_A<15..0>	12 28 29 32
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_BA<2..0>	12 28 29 32
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_RAS_L	12 28 29 32
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_CAS_L	12 28 29 32
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_WE_L	12 28 29 32
MEM_A_DQ_BYTE0	MEM_50S	MEM_A_DQ_BYTE0	MEM_A_DQ<7..0>	12 28 29
MEM_A_DQ_BYTE1	MEM_50S	MEM_A_DQ_BYTE1	MEM_A_DQ<15..8>	12 28 29
MEM_A_DQ_BYTE2	MEM_50S	MEM_A_DQ_BYTE2	MEM_A_DQ<23..16>	12 28 29
MEM_A_DQ_BYTE3	MEM_50S	MEM_A_DQ_BYTE3	MEM_A_DQ<31..24>	12 28 29
MEM_A_DQ_BYTE4	MEM_50S	MEM_A_DQ_BYTE4	MEM_A_DQ<39..32>	12 28 29
MEM_A_DQ_BYTE5	MEM_50S	MEM_A_DQ_BYTE5	MEM_A_DQ<47..40>	12 28 29
MEM_A_DQ_BYTE6	MEM_50S	MEM_A_DQ_BYTE6	MEM_A_DQ<55..48>	12 28 29
T105 MEM_A_DQ_BYTE7	MEM_50S	MEM_A_DQ_BYTE7	MEM_A_DQ<63..56>	12 28 29
T106 MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_P<0>	12 28 29
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_N<0>	12 28 29
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_P<1>	12 28 29
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_N<1>	12 28 29
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_P<2>	12 28 29
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_N<2>	12 28 29
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_P<3>	12 28 29
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_N<3>	12 28 29
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_P<4>	12 28 29
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_N<4>	12 28 29
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_P<5>	12 28 29
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_N<5>	12 28 29
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_P<6>	12 28 29
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_N<6>	12 28 29
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_P<7>	12 28 29
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_N<7>	12 28 29
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_P<5..0>	12 30 31 32
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_N<5..0>	12 30 31 32
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_CKE<3..2>	
T110 MEM_B_CNTL1	MEM_37S	MEM_CTRL	MEM_B_CKE<1>	12 31 32
T111 MEM_B_CNTL0	MEM_37S	MEM_CTRL	MEM_B_CKE<0>	12 30 32
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_CS_L<3..0>	12 30 31 32
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_ODT<3..1>	12 31 32
T109 MEM_B_CNTL0	MEM_37S	MEM_CTRL	MEM_B_ODT<0>	12 30 32
T108 MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_A<15..7>	12 30 31 32
T107 MEM_B_CMD6	MEM_40S	MEM_CMD	MEM_B_A<6>	12 30 31 32
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_A<5..0>	12 30 31 32
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_BA<2..0>	12 30 31 32
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_RAS_L	12 30 31 32
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_CAS_L	12 30 31 32
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_WE_L	12 30 31 32
MEM_B_DQ_BYTE0	MEM_50S	MEM_B_DQ_BYTE0	MEM_B_DQ<7..0>	12 30 31
MEM_B_DQ_BYTE1	MEM_50S	MEM_B_DQ_BYTE1	MEM_B_DQ<15..8>	12 30 31
MEM_B_DQ_BYTE2	MEM_50S	MEM_B_DQ_BYTE2	MEM_B_DQ<23..16>	12 30 31
MEM_B_DQ_BYTE3	MEM_50S	MEM_B_DQ_BYTE3	MEM_B_DQ<31..24>	12 30 31
MEM_B_DQ_BYTE4	MEM_50S	MEM_B_DQ_BYTE4	MEM_B_DQ<39..32>	12 30 31
MEM_B_DQ_BYTE5	MEM_50S	MEM_B_DQ_BYTE5	MEM_B_DQ<47..40>	12 30 31
MEM_B_DQ_BYTE6	MEM_50S	MEM_B_DQ_BYTE6	MEM_B_DQ<55..48>	12 30 31
MEM_B_DQ_BYTE7	MEM_50S	MEM_B_DQ_BYTE7	MEM_B_DQ<63..56>	12 30 31
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_P<0>	12 30 31
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_N<0>	12 30 31
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_P<1>	12 30 31
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_N<1>	12 30 31
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_P<2>	12 30 31
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_N<2>	12 30 31
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_P<3>	12 30 31
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_N<3>	12 30 31
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_P<4>	12 30 31
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_N<4>	12 30 31
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_P<5>	12 30 31
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_N<5>	12 30 31
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_P<6>	12 30 31
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_N<6>	12 30 31
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_P<7>	12 30 31
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_N<7>	12 30 31

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

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Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_DP_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
LVDS_85D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_DISPLAYPORT	TOP,BOTTOM	=4:1_SPACING	?
LVDS	TOP,BOTTOM	=4:1_SPACING	?

SOURCE: HR PLATFORM DESIGN GUIDE, TABLES 191,193

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
SATA_37SE	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE
SATA_50SE	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=5:1_SPACING	?

SOURCE: HR PLATFORM DESIGN GUIDE, TABLES 191,193

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4:1_SPACING	?

SOURCE: HR PLATFORM DESIGN GUIDE, TABLES 191,193

USB 3.0 INTERFACE CONSTRAINTS

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3	TOP,BOTTOM	=5:1_SPACING	?

SOURCE: CR SFF PLATFORM DESIGN GUIDE V0.7, TABLE 4-211, 1X1+

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_25M_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=2x_DIELECTRIC	?
CLK_25M	*	=5x_DIELECTRIC	?

NOTE: 25MHz system clocks very sensitive to noise.

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
LVDS_IG_A_CLK	LVDS_85D	LVDS	LVDS_IG_A_CLK_P	9 18
LVDS_IG_A_CLK	LVDS_85D	LVDS	LVDS_IG_A_CLK_N	9 18
LVDS_IG_A_DATA	LVDS_85D	LVDS	LVDS_IG_A_DATA_P<2..0>	9 18
LVDS_IG_A_DATA	LVDS_85D	LVDS	LVDS_IG_A_DATA_N<2..0>	9 18
LVDS_IG_A_DATA3	LVDS_85D	LVDS	LVDS_IG_A_DATA_P<3>	9 18
LVDS_IG_A_DATA3	LVDS_85D	LVDS	LVDS_IG_A_DATA_N<3>	9 18
LVDS_IG_B_DATA	LVDS_85D	LVDS	LVDS_IG_B_DATA_P<2..0>	9 18
LVDS_IG_B_DATA	LVDS_85D	LVDS	LVDS_IG_B_DATA_N<2..0>	9 18
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_C_P	17 39
	SATA_90D	SATA	SATA_HDD_R2D_C_N	17 39
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_P	17 39
	SATA_90D	SATA	SATA_HDD_D2R_N	17 39
SATA_HDD_D2R	SATA_90D	SATA	SATA_SSD_D2R_MUX_OUT_P	39
	SATA_90D	SATA	SATA_SSD_D2R_MUX_OUT_N	39
SATA_HDD_R2D	SATA_90D	SATA	SATA_SSD_R2D_MUX_IN_P	39
	SATA_90D	SATA	SATA_SSD_R2D_MUX_IN_N	39
T237 SATA_HDD_D2R	SATA_90D	SATA	SATA_SSD_D2R_P	39
T238	SATA_90D	SATA	SATA_SSD_D2R_N	39
T239 SATA_HDD_R2D	SATA_90D	SATA	SATA_SSD_R2D_P	39
T240	SATA_90D	SATA	SATA_SSD_R2D_N	39
T218 SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_UF_P	
T219	SATA_90D	SATA	SATA_HDD_R2D_UF_N	
SATA_ODD_R2D	SATA_90D	SATA	SATA_ODD_R2D_C_P	9 17
	SATA_90D	SATA	SATA_ODD_R2D_C_N	9 17
SATA_ODD_R2D	SATA_90D	SATA	SATA_ODD_R2D_P	
	SATA_90D	SATA	SATA_ODD_R2D_N	
SATA_ODD_D2R	SATA_90D	SATA	SATA_ODD_D2R_P	9 17
	SATA_90D	SATA	SATA_ODD_D2R_N	9 17
SATA_ODD_D2R	SATA_90D	SATA	SATA_ODD_D2R_UF_P	
	SATA_90D	SATA	SATA_ODD_D2R_UF_N	
T213 PCH_SATA3_TCOMP	SATA_50SE	SATA_TCOMP	PCH_SATA3COMP	17
PCH_SATA_TCOMP	SATA_37SE	SATA_TCOMP	PCH_SATAICOMP	17
T235 USB_HUB1_UP	USB_85D	USB	USB_EXTB_XHCI_P	19 26
T236	USB_85D	USB	USB_EXTB_XHCI_N	19 26
USB_HUB1_UP	USB_85D	USB	USB_EXTB_EHCI_P	19 26
	USB_85D	USB	USB_EXTB_EHCI_N	19 26
USB_HUB2_UP	USB_85D	USB	USB_HUB_UP_P	19 26
	USB_85D	USB	USB_HUB_UP_N	19 26
USB_EXTA	USB_85D	USB	USB_EXTA_P	19 40
	USB_85D	USB	USB_EXTA_N	19 40
USB_EXTB	USB_85D	USB	USB_EXTB_P	7 26 38
	USB_85D	USB	USB_EXTB_N	7 26 38
USB_EXTC	USB_85D	USB	USB_EXTC_P	9 19
	USB_85D	USB	USB_EXTC_N	9 19
USB_CAMERA	USB_85D	USB	USB_CAMERA_CONN_P	7 34
	USB_85D	USB	USB_CAMERA_CONN_N	7 34
USB_BT	USB_85D	USB	USB_BT_P	9 34
	USB_85D	USB	USB_BT_N	9 34
USB_BT	USB_85D	USB	USB_BT_CONN_P	7 34
	USB_85D	USB	USB_BT_CONN_N	7 34
T249 USB_BT	USB_85D	USB	USB_BT_WAKE_P	34
T250	USB_85D	USB	USB_BT_WAKE_N	34
USB_TPAD	USB_85D	USB	USB_TPAD_P	9 49
	USB_85D	USB	USB_TPAD_N	9 49
USB_IR	USB_85D	USB	USB_SMC_P	9 41
	USB_85D	USB	USB_SMC_N	9 41
PCH_USB_RBIAS	PCH_USB_RBIAS	USB_RBIAS	PCH_USB_RBIAS	19
T230 USB_T29A	USB_85D	USB	USB_EXTD_XHCI_P	19 26
T231	USB_85D	USB	USB_EXTD_XHCI_N	19 26
T241 USB_EXTA	USB_85D	USB	USB_EXTA_MUXED_P	40
T242	USB_85D	USB	USB_EXTA_MUXED_N	40
T247 USB_CAMERA	USB_85D	USB	USB_CAMERA_P	19 34
T248	USB_85D	USB	USB_CAMERA_N	19 34
T243 USB_EXTA	USB_85D	USB	USB_LT1_P	40
T244	USB_85D	USB	USB_LT1_N	40
T220 USB3_EXTB_TX	USB_85D	USB3	USB3_EXTB_TX_P	19 38
T221	USB_85D	USB3	USB3_EXTB_TX_N	19 38
T227 USB3_EXTB_RX	USB_85D	USB3	USB3_EXTB_RX_P	7 19 38
T228	USB_85D	USB3	USB3_EXTB_RX_N	7 19 38
T224 USB3_EXTC_TX	USB_85D	USB3	USB3_EXTC_TX_P	9 19
T225	USB_85D	USB3	USB3_EXTC_TX_N	9 19
T226 USB3_EXTC_RX	USB_85D	USB3	USB3_EXTC_RX_P	9 19
T227	USB_85D	USB3	USB3_EXTC_RX_N	9 19
T232 USB3_EXTA_TX	USB_85D	USB3	USB3_EXTA_TX_P	19 40
T233	USB_85D	USB3	USB3_EXTA_TX_N	19 40
T229 USB3_EXTA_RX	USB_85D	USB3	USB3_EXTA_RX_P	19 40
T234	USB_85D	USB3	USB3_EXTA_RX_N	19 40

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
T255 SYSCLK_CLK32K_RTC	CLK_SLOW_55S	CLK_SLOW	SYSCLK_CLK32K_RTC	17 25
T256 SYSCLK_CLK25M_SB	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_SB	17 25
T254	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_SB_R	17
T253 SYSCLK_CLK25M_ENET	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_ENET	
T252	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_ENET_R	
T251 SYSCLK_CLK25M_TBT	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_TBT	25 35
T250	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_TBT_R	35

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
LPC_AD	LPC_50S	LPC	LPC_AD<3..0>	7 17 41 43 82
LPC_FRAME_L	LPC_50S	LPC	LPC_FRAME_L	7 17 41 43 82
LPC_RESET_L	LPC_50S	LPC	LPC_RESET_L	25
PCH_LPC_CLK0	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC_R	19 25
	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC	25 41
	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_LPCPLUS	7 25 43
SMBUS_PCH_CLK	SMB_50S	SMB	SMBUS_PCH_CLK	17 44
SMBUS_PCH_DATA	SMB_50S	SMB	SMBUS_PCH_DATA	17 44
SMBUS_PCH_0_CLK	SMB_50S	SMB	SML_PCH_0_CLK	17 44
SMBUS_PCH_0_DATA	SMB_50S	SMB	SML_PCH_0_DATA	17 44
SMBUS_PCH_1_CLK	SMB_50S	SMB	SML_PCH_1_CLK	17 44
SMBUS_PCH_1_DATA	SMB_50S	SMB	SML_PCH_1_DATA	17 44
HDA_BIT_CLK	HDA_50S	HDA	HDA_BIT_CLK	17 53
	HDA_50S	HDA	HDA_BIT_CLK_R	17
HDA_SYNC	HDA_50S	HDA	HDA_SYNC	17 53
	HDA_50S	HDA	HDA_SYNC_R	17
HDA_RST_L	HDA_50S	HDA	HDA_RST_R_L	17
	HDA_50S	HDA	HDA_RST_L	17 53
HDA_SDIN0	HDA_50S	HDA	HDA_SDIN0	17 53
	HDA_50S	HDA	AUD_SDI_R	53
HDA_SDOUT	HDA_50S	HDA	HDA_SDOUT	17 53
	HDA_50S	HDA	HDA_SDOUT_R	17 25
SPI_CLK	SPI_55S	SPI	SPI_CLK_R	17 43
	SPI_55S	SPI	SPI_CLK	43
SPI_MOSI	SPI_55S	SPI	SPI_MOSI_R	17 43
	SPI_55S	SPI	SPI_MOSI	43
SPI_MISO	SPI_55S	SPI	SPI_MISO	17 43
SPI_CS0	SPI_55S	SPI	SPI_CS0_R_L	17 43
	SPI_55S	SPI	SPI_CS0_L	43
	PCIE_85D	PCIE	PCIE_ENET_R2D_P	
	PCIE_85D	PCIE	PCIE_ENET_R2D_N	
PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE_ENET_R2D_C_P	7 17 38
	PCIE_85D	PCIE	PCIE_ENET_R2D_C_N	7 17 38
PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE_ENET_D2R_P	7 17 38
	PCIE_85D	PCIE	PCIE_ENET_D2R_N	7 17 38
	PCIE_85D	PCIE	PCIE_ENET_D2R_C_P	
	PCIE_85D	PCIE	PCIE_ENET_D2R_C_N	
	PCIE_85D	PCIE	PCIE_AP_R2D_P	7 34
	PCIE_85D	PCIE	PCIE_AP_R2D_N	7 34
PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_C_P	17 34
	PCIE_85D	PCIE	PCIE_AP_R2D_C_N	17 34
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_D2R_P	17 34
	PCIE_85D	PCIE	PCIE_AP_D2R_N	17 34
1275 PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_D2R_PI_P	7 34
1276	PCIE_85D	PCIE	PCIE_AP_D2R_PI_N	7 34
1275 PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_R2D_PI_P	34
1277	PCIE_85D	PCIE	PCIE_AP_R2D_PI_N	34
PCIE_TBT_D2R	PCIE_85D	PCIE	PCIE_SSD_D2R_MUX_OUT_P	39
	PCIE_85D	PCIE	PCIE_SSD_D2R_MUX_OUT_N	39
PCIE_TBT_R2D	PCIE_85D	PCIE	PCIE_SSD_R2D_C_P<1..0>	9 39
	PCIE_85D	PCIE	PCIE_SSD_R2D_C_N<1..0>	9 39
PCIE_TBT_D2R	PCIE_85D	PCIE	PCIE_SSD_D2R_P<1..0>	9 39
	PCIE_85D	PCIE	PCIE_SSD_D2R_N<1..0>	9 39
PCIE_TBT_R2D	PCIE_85D	PCIE	PCIE_SSD_R2D_MUX_IN_P	39
	PCIE_85D	PCIE	PCIE_SSD_R2D_MUX_IN_N	39
1274 PCIE_TBT_D2R	PCIE_85D	PCIE	PCIE_SSD_D2R_C_P<1>	39
1275	PCIE_85D	PCIE	PCIE_SSD_D2R_C_N<1>	39
1274 PCIE_TBT_R2D	PCIE_85D	PCIE	PCIE_SSD_R2D_P<1>	39
1277	PCIE_85D	PCIE	PCIE_SSD_R2D_N<1>	39
1253 PCIE_CLK100M	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_P	17
1254	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_N	17
1262 PCIE_CLK100M_TBT_	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_TBT_P	17 35
1261	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_TBT_N	17 35
1255	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_P	17
1257	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_N	17
1256 PCIE_CLK100M_TBT_	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_P	17
1260	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_N	17
1258	CPU_50S	CLK_PCIE	PCH_CLK14P3M_REFCLK	17
1266	CPU_50S	CLK_PCIE	PCH_CLK33M_PCIIN	17 25
1270 PCIE_CLK100M	1:1_DIFFPAIR	CLK_PCIE	PEX_TSTCLK_O_P	71 95
1280	1:1_DIFFPAIR	CLK_PCIE	PEX_TSTCLK_O_N	71 95
PCIE_CLK100M	CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_P	17 71
	CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_N	17 71
PCIE_CLK100M_ENET	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_P	7 17 38
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_N	7 17 38
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_P	17 34
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_N	17 34
PCIE_CLK100M_FW	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_P	9 17
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_N	9 17
1281 PCIE_CLK100M_FW	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_SSD_P	17 39
1282	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_SSD_N	17 39
PCIE_CLK100M_EXCARD	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_EXCARD_P	9 17
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_EXCARD_N	9 17
1263 PCIE_TBT_R2D	PCIE_85D	PCIE	PCIE_TBT_R2D_C_P<3..0>	9 35
1264 PCIE_TBT_R2D	PCIE_85D	PCIE	PCIE_TBT_R2D_C_N<3..0>	9 35
1265 PCIE_TBT_R2D	PCIE_85D	PCIE	PCIE_TBT_R2D_P<3..0>	35
1267 PCIE_TBT_R2D	PCIE_85D	PCIE	PCIE_TBT_R2D_N<3..0>	35
1268 PCIE_TBT_D2R	PCIE_85D	PCIE	PCIE_TBT_D2R_P<3..0>	9 35
1269 PCIE_TBT_D2R	PCIE_85D	PCIE	PCIE_TBT_D2R_N<3..0>	9 35
1270 PCIE_TBT_D2R	PCIE_85D	PCIE	PCIE_TBT_D2R_C_P<3..0>	35
1269 PCIE_TBT_D2R	PCIE_85D	PCIE	PCIE_TBT_D2R_C_N<3..0>	35

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DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

Thunderbolt SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_SPI	*	=2x_DIELECTRIC	?

Thunderbolt/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
TBTDP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
TBTDP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP	*	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP	TOP,BOTTOM	=7x_DIELECTRIC	?

NOTE: Thunderbolt high-speed nets are NOT directly assigned to TBTDP_*D physical rules.
TABLE_PHYSICAL_ASSIGNMENT symbols must be used to create the assignments.
Proper differential impedance depends on mDP connector used.
For 514-0637: R2D nets (SMT pins) = 80D, D2R nets (TH pins) = 100D

SOURCE: Bill Cornelius’s Thunderbolt Routing Notes

Thunderbolt/DP Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
TBT_A_R2D	TBTDP_85D	TBTDP	TBT_A_R2D_C_P<1..0>	7 35 84
TBT_A_R2D	TBTDP_85D	TBTDP	TBT_A_R2D_C_N<1..0>	7 35 84
	TBTDP_85D	TBTDP	TBT_A_R2D_P<1..0>	7 84
	TBTDP_85D	TBTDP	TBT_A_R2D_N<1..0>	7 84
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<3..1:2>	35 84
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<3..1:2>	35 84
	DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<3..1:2>	84
	DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<3..1:2>	84
	DP_85D	DISPLAYPORT	DP_A_LSX_ML_P<1>	84
	DP_85D	DISPLAYPORT	DP_A_LSX_ML_N<1>	84
	TBTDP_85D	TBTDP	TBT_A_D2R_C_P<1..0>	7 84
	TBTDP_85D	TBTDP	TBT_A_D2R_C_N<1..0>	7 84
TBT_A_D2R	TBTDP_85D	TBTDP	TBT_A_D2R_P<1..0>	7 35 84
TBT_A_D2R	TBTDP_85D	TBTDP	TBT_A_D2R_N<1..0>	7 35 84
TBT_A_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_C_P	35 84
TBT_A_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_C_N	35 84
	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_P	84
	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_N	84
	DP_85D	DISPLAYPORT	DP_A_AUXCH_DDC_P	84
	DP_85D	DISPLAYPORT	DP_A_AUXCH_DDC_N	84
	TBTDP_85D	TBTDP	TBT_A_D2R1_AUXDDC_P	84
	TBTDP_85D	TBTDP	TBT_A_D2R1_AUXDDC_N	84
TBT_B_R2D	TBTDP_85D	TBTDP	TBT_B_R2D_C_P<1..0>	7 35 85
TBT_B_R2D	TBTDP_85D	TBTDP	TBT_B_R2D_C_N<1..0>	7 35 85
	TBTDP_85D	TBTDP	TBT_B_R2D_P<1..0>	7 85
	TBTDP_85D	TBTDP	TBT_B_R2D_N<1..0>	7 85
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<3..1:2>	35 85
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<3..1:2>	35 85
	DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<3..1:2>	85
	DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<3..1:2>	85
	DP_85D	DISPLAYPORT	DP_B_LSX_ML_P<1>	85
	DP_85D	DISPLAYPORT	DP_B_LSX_ML_N<1>	85
	TBTDP_85D	TBTDP	TBT_B_D2R_C_P<1..0>	7 85
	TBTDP_85D	TBTDP	TBT_B_D2R_C_N<1..0>	7 85
TBT_B_D2R	TBTDP_85D	TBTDP	TBT_B_D2R_P<1..0>	7 35 85
TBT_B_D2R	TBTDP_85D	TBTDP	TBT_B_D2R_N<1..0>	7 35 85
TBT_B_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_C_P	35 85
TBT_B_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_C_N	35 85
	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_P	85
	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_N	85
	DP_85D	DISPLAYPORT	DP_B_AUXCH_DDC_P	85
	DP_85D	DISPLAYPORT	DP_B_AUXCH_DDC_N	85
TBT_B_D2R	TBTDP_85D	TBTDP	TBT_B_D2R1_AUXDDC_P	85
	TBTDP_85D	TBTDP	TBT_B_D2R1_AUXDDC_N	85

Only used on dual-port hosts.

Thunderbolt IC Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_P<3..0>	
	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_N<3..0>	
	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_C_P	
	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_C_N	
TBT_SPI_CLK	TBT_SPI_5SS	TBT_SPI	TBT_SPI_CLK	35
TBT_SPI_MOSI	TBT_SPI_5SS	TBT_SPI	TBT_SPI_MOSI	35
TBT_SPI_MISO	TBT_SPI_5SS	TBT_SPI	TBT_SPI_MISO	35
TBT_SPI_CS_L	TBT_SPI_5SS	TBT_SPI	TBT_SPI_CS_L	35

Only used on hosts supporting Thunderbolt video-in

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE: Thunderbolt Constraints

Apple Inc.

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
SMBUS_SMC_2_S3_SCL	SMB_50S	SMB	SMBUS_SMC_2_S3_SCL	7 41 44
SMBUS_SMC_2_S3_SDA	SMB_50S	SMB	SMBUS_SMC_2_S3_SDA	7 41 44
SMBUS_SMC_1_S0_SCL	SMB_50S	SMB	SMBUS_SMC_1_S0_SCL	41 44
SMBUS_SMC_1_S0_SDA	SMB_50S	SMB	SMBUS_SMC_1_S0_SDA	41 44
SMBUS_SMC_0_S0_SCL	SMB_50S	SMB	SMBUS_SMC_0_S0_SCL	41 44
SMBUS_SMC_0_S0_SDA	SMB_50S	SMB	SMBUS_SMC_0_S0_SDA	41 44
SMBUS_SMC_5_SCL	SMB_50S	SMB	SMBUS_SMC_5_SCL	
SMBUS_SMC_5_SDA	SMB_50S	SMB	SMBUS_SMC_5_SDA	
SMBUS_SMC_3_SCL	SMB_50S	SMB	SMBUS_SMC_3_SCL	41 44
SMBUS_SMC_3_SDA	SMB_50S	SMB	SMBUS_SMC_3_SDA	41 44

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P	61
	1TO1_DIFFPAIR		CHGR_CSI_N	61
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P	61
	1TO1_DIFFPAIR		CHGR_CSO_N	61

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE: SMC Constraints

Apple Inc.

DRAWING NUMBER: 051-9589 SIZE: D

REVISION: 4.18.0

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GDDR5 Frame Buffer Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR5_45R50SE	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	12.7 MM	=STANDARD	=STANDARD
GDDR5_45SE	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
GDDR5_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR5_CLK	*	=5x_DIELECTRIC	?
GDDR5_CMD	*	=3x_DIELECTRIC	?
GDDR5_DATA	*	=3x_DIELECTRIC	?
GDDR5_EDC	*	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR5_CLK	TOP,BOTTOM	=5x_DIELECTRIC	?
GDDR5_CMD	TOP,BOTTOM	=4x_DIELECTRIC	?
GDDR5_DATA	TOP,BOTTOM	=5x_DIELECTRIC	?
GDDR5_EDC	TOP,BOTTOM	=5x_DIELECTRIC	?

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
HDMI_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
HDMI	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
HDMI	TOP,BOTTOM	=4x_DIELECTRIC	?

DisplayPort/TMDS intra-pair matching should be 0.127mm. Inter-pair matching should be within 2.54cm. Max Length 241.3mm.
DIsplayPort AUX CH intra-pair matching should be 0.127mm. Max length 330.2mm.
MAX LENGTH OF DISPLAYPORT/TMDS TRACES: 13 INCHES.
SOURCE: Calpella SFF DG Rev 1.5 (407364) and Family GPU DG-04202-001-v04.

GDDR5 FB A Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
FB_A0_CLK	GDDR5_80D	GDDR5_CLK	FB_A0_CLK_P
FB_A0_CLK	GDDR5_80D	GDDR5_CLK	FB_A0_CLK_N
FB_A1_CLK	GDDR5_80D	GDDR5_CLK	FB_A1_CLK_P
FB_A1_CLK	GDDR5_80D	GDDR5_CLK	FB_A1_CLK_N
FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB_A0_A<8..0>
FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB_A1_A<8..0>
FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB_A0_ABI_L
FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB_A1_ABI_L
FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB_A0_RAS_L
FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB_A1_RAS_L
FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB_A0_CAS_L
FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB_A1_CAS_L
FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB_A0_WE_L
FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB_A1_WE_L
FB_A0_CMD_R	GDDR5_45SE	GDDR5_CMD	FB_A0_CKE_L
FB_A1_CMD_R	GDDR5_45SE	GDDR5_CMD	FB_A1_CKE_L
FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB_A0_CS_L
FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB_A1_CS_L
FB_A0_EDC0	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<0>
FB_A0_EDC1	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<1>
FB_A0_EDC2	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<2>
FB_A0_EDC3	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<3>
FB_A1_EDC0	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<0>
FB_A1_EDC1	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<1>
FB_A1_EDC2	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<2>
FB_A1_EDC3	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<3>
FB_A0_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<0>
FB_A0_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<1>
FB_A0_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<2>
FB_A0_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<3>
FB_A1_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<0>
FB_A1_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<1>
FB_A1_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<2>
FB_A1_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<3>
FB_A0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_A0_WCLK_P<0>
FB_A0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_A0_WCLK_N<0>
FB_A0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_A0_WCLK_P<1>
FB_A0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_A0_WCLK_N<1>
FB_A1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_A1_WCLK_P<0>
FB_A1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_A1_WCLK_N<0>
FB_A1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_A1_WCLK_P<1>
FB_A1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_A1_WCLK_N<1>
FB_A0_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<7..0>
FB_A0_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<15..8>
FB_A0_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<23..16>
FB_A0_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<31..24>
FB_A1_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<7..0>
FB_A1_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<15..8>
FB_A1_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<23..16>
FB_A1_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<31..24>
FB_A0_CMD_R	GDDR5_45SE	GDDR5_CMD	FB_A0_RESET_L
FB_A1_CMD_R	GDDR5_45SE	GDDR5_CMD	FB_A1_RESET_L

GDDR5 FB B Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
FB_B0_CLK	GDDR5_80D	GDDR5_CLK	FB_B0_CLK_P
FB_B0_CLK	GDDR5_80D	GDDR5_CLK	FB_B0_CLK_N
FB_B1_CLK	GDDR5_80D	GDDR5_CLK	FB_B1_CLK_P
FB_B1_CLK	GDDR5_80D	GDDR5_CLK	FB_B1_CLK_N
FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB_B0_A<8..0>
FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB_B1_A<8..0>
FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB_B0_ABI_L
FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB_B1_ABI_L
FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB_B0_RAS_L
FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB_B1_RAS_L
FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB_B0_CAS_L
FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB_B1_CAS_L
FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB_B0_WE_L
FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB_B1_WE_L
FB_B0_CMD_R	GDDR5_45SE	GDDR5_CMD	FB_B0_CKE_L
FB_B1_CMD_R	GDDR5_45SE	GDDR5_CMD	FB_B1_CKE_L
FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB_B0_CS_L
FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB_B1_CS_L
FB_B0_EDC0	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<0>
FB_B0_EDC1	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<1>
FB_B0_EDC2	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<2>
FB_B0_EDC3	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<3>
FB_B1_EDC0	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<0>
FB_B1_EDC1	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<1>
FB_B1_EDC2	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<2>
FB_B1_EDC3	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<3>
FB_B0_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<0>
FB_B0_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<1>
FB_B0_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<2>
FB_B0_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<3>
FB_B1_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<0>
FB_B1_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<1>
FB_B1_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<2>
FB_B1_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<3>
FB_B0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_P<0>
FB_B0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_N<0>
FB_B0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_P<1>
FB_B0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_N<1>
FB_B1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_P<0>
FB_B1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_N<0>
FB_B1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_P<1>
FB_B1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_N<1>
FB_B0_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<7..0>
FB_B0_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<15..8>
FB_B0_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<23..16>
FB_B0_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<31..24>
FB_B1_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<7..0>
FB_B1_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<15..8>
FB_B1_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<23..16>
FB_B1_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<31..24>
FB_B0_CMD_R	GDDR5_45SE	GDDR5_CMD	FB_B0_RESET_L
FB_B1_CMD_R	GDDR5_45SE	GDDR5_CMD	FB_B1_RESET_L

MUXGFX & DP AUX MUX NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_C_P<3..0>
	DP_85D	DISPLAYPORT	DP_INT_ML_C_N<3..0>
DP_INT_AUXCH	DP_85D	DISPLAYPORT	DP_INT_AUX_C_P
	DP_85D	DISPLAYPORT	DP_INT_AUX_C_N
DP_INT_AUXCH	DP_85D	DISPLAYPORT	DP_INT_AUX_P
	DP_85D	DISPLAYPORT	DP_INT_AUX_N
DP_INT_AUXCH	DP_85D	DISPLAYPORT	DP_INT_EG_AUX_P
	DP_85D	DISPLAYPORT	DP_INT_EG_AUX_N
DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_P<3..0>
	DP_85D	DISPLAYPORT	DP_INT_ML_N<3..0>
DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_F_P<3..0>
	DP_85D	DISPLAYPORT	DP_INT_ML_F_N<3..0>
DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_EG_ML_P<3..0>
	DP_85D	DISPLAYPORT	DP_INT_EG_ML_N<3..0>
DP_INT_AUXCH	DP_85D	DISPLAYPORT	DPA_IG_AUX_CH_P
	DP_85D	DISPLAYPORT	DPA_IG_AUX_CH_N
DP_INT_AUXCH	DP_85D	DISPLAYPORT	DPB_IG_AUX_CH_P
	DP_85D	DISPLAYPORT	DPB_IG_AUX_CH_N
DP_INT_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK0_EG_AUXCH_P
	DP_85D	DISPLAYPORT	DP_TBTSNK0_EG_AUXCH_N
DP_INT_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK1_EG_AUXCH_P
	DP_85D	DISPLAYPORT	DP_TBTSNK1_EG_AUXCH_N
TBT_A_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_C_P
	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_C_N
TBT_B_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_C_P
	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_C_N
DP_INT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_P<3..0>
	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_N<3..0>
DP_INT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_P<3..0>
	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_N<3..0>
TBT_A_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_P
	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_N
TBT_B_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_P
	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_N
DP_INT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_P<3..0>
	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_N<3..0>
DP_INT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_P<3..0>
	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_N<3..0>

Kepler Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
GPU_CLK27M	CLK_SLOW_555	CLK_SLOW	GPU_OSC_27M_XTALIN
GPU_CLK27M	CLK_SLOW_555	CLK_SLOW	GPU_OSC_27M_XTALOUT
GPU_CLK27M	CLK_SLOW_555	CLK_SLOW	GPU_OSC_27M_XTAL_BUFFOUT
GPU_CLK27M	CLK_SLOW_555	CLK_SLOW	GPU_OSC_27M_SSIN
	1:1_DIFFPAIR		PEX_TSTCLK_O_P
	1:1_DIFFPAIR		PEX_TSTCLK_O_N
HDMI_DATA	HDMI_90D	HDMI	HDMI_EG_DATA_C_P<2..0>
	HDMI_90D	HDMI	HDMI_EG_DATA_C_N<2..0>
HDMI_CLK	HDMI_90D	HDMI	HDMI_EG_CLK_C_P
	HDMI_90D	HDMI	HDMI_EG_CLK_C_N

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

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GPU (Kepler) CONSTRAINTS

Apple Inc.

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_5SS	*	=1:1_DIFFPAIR	=5S_OHM_SE	=5S_OHM_SE	=5S_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_5SS	*	=1:1_DIFFPAIR	=5S_OHM_SE	=5S_OHM_SE	=5S_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR
AUDIODIFF	*	=1:1_DIFFPAIR	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM
THERM_5SS_CPUIMVPISNS1	*	=1:1_DIFFPAIR	=5S_OHM_SE	=5S_OHM_SE	=5S_OHM_SE	0.2 MM	0.2 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_CLK	*	GND_P2MM
GND	MEM_CMD	*	GND_P2MM
GND	MEM_CTRL	*	GND_P2MM
GND	MEM_*_DQ_BYTE*	*	GND_P2MM
GND	MEM_DQS	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_37S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	10 mm OVERRIDE	OVERRIDE	OVERRIDE
USB_85D OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
CPU_27P4S OVERRIDE	BOTTOM OVERRIDE	OVERRIDE	OVERRIDE	0.23 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE

Graphics ,SATA Constraint Relaxations

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS_85D	BGA	LVDS_85D
DP_85D	BGA	100_DIFF_BGA
SATA_90D	BGA	100_DIFF_BGA
CLK_PCIE_90D	BGA	100_DIFF_BGA

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for ARD fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_72D	BOTTOM			0.127 MM	6.35 MM		
MEM_85D	TOP			0.1 MM	6.35 MM		

D2 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SENSE_DIFFPAIR	THERM_1TO1_5SS	THERM	CPUTHMSNS_D2_P	47
	THERM_1TO1_5SS	THERM	CPUTHMSNS_D2_N	47
SENSE_DIFFPAIR	THERM_1TO1_5SS	THERM	DDR3THMSNS_D1_P	47
	THERM_1TO1_5SS	THERM	DDR3THMSNS_D1_N	47
SENSE_DIFFPAIR	THERM_1TO1_5SS	THERM	GPUTHMSNS_D_P	47
	THERM_1TO1_5SS	THERM	GPUTHMSNS_D_N	47
SENSE_DIFFPAIR	THERM_1TO1_5SS	THERM	GPU_TDIODE_P	47 77
	THERM_1TO1_5SS	THERM	GPU_TDIODE_N	47 77
SENSE_DIFFPAIR	SENSE_1TO1_5SS	SENSE	VCCSAS0_CS_P	45 62
	SENSE_1TO1_5SS	SENSE	VCCSAS0_CS_N	45 62
SENSE_DIFFPAIR	SENSE_1TO1_5SS	SENSE	VCCSAISNS_R_P	45
	SENSE_1TO1_5SS	SENSE	VCCSAISNS_R_N	45
SENSE_DIFFPAIR	SENSE_1TO1_5SS	SENSE	ISNS_1V5_MEM_R_P	45
	SENSE_1TO1_5SS	SENSE	ISNS_1V5_MEM_R_N	45
SENSE_DIFFPAIR	SENSE_1TO1_5SS	SENSE	CPUVCCIOS0_CS_P	45 67
	SENSE_1TO1_5SS	SENSE	CPUVCCIOS0_CS_N	45 67
SENSE_DIFFPAIR	SENSE_1TO1_5SS	SENSE	CPUVCCIOISNS_R_P	45
	SENSE_1TO1_5SS	SENSE	CPUVCCIOISNS_R_N	45
SENSE_DIFFPAIR	SENSE_1TO1_5SS	SENSE	GPUISENS_N	
	SENSE_1TO1_5SS	SENSE	GPUISENS_P	
SENSE_DIFFPAIR	SENSE_1TO1_5SS	SENSE	ISNS_1V5_MEM_N	45
	SENSE_1TO1_5SS	SENSE	ISNS_1V5_MEM_P	45
SENSE_DIFFPAIR	SENSE_1TO1_5SS	SENSE	ISNS_AIRPORT_N	96
	SENSE_1TO1_5SS	SENSE	ISNS_AIRPORT_N	96
SENSE_DIFFPAIR	SENSE_1TO1_5SS	SENSE	ISNS_AIRPORT_P	96
	SENSE_1TO1_5SS	SENSE	ISNS_AIRPORT_P	96
SENSE_DIFFPAIR	SENSE_1TO1_5SS	SENSE	ISNS_AIRPORT_R_N	99
	SENSE_1TO1_5SS	SENSE	ISNS_AIRPORT_R_P	99
SENSE_DIFFPAIR	SENSE_1TO1_5SS	SENSE	ISNS_LCDBKLT_N	
	SENSE_1TO1_5SS	SENSE	ISNS_LCDBKLT_P	
	SENSE_1TO1_5SS	SENSE	GPUFB_CS_P	74 99
	SENSE_1TO1_5SS	SENSE	GPUFB_CS_N	74 99
SENSE_DIFFPAIR	SENSE_1TO1_5SS	SENSE	ISNS_PP1V0_S0GPU_R_P	98
	SENSE_1TO1_5SS	SENSE	ISNS_PP1V0_S0GPU_R_N	98
SENSE_DIFFPAIR	SENSE_1TO1_5SS	SENSE	ISNS_PP1V8_S0GPU_P	
	SENSE_1TO1_5SS	SENSE	ISNS_PP1V8_S0GPU_N	
SENSE_DIFFPAIR	SENSE_1TO1_5SS	SENSE	ISNS_PP1V8_S0GPU_R_P	
	SENSE_1TO1_5SS	SENSE	ISNS_PP1V8_S0GPU_R_N	
	SENSE_1TO1_5SS	SENSE	P1V05_GPU_CS_P	74 98
	SENSE_1TO1_5SS	SENSE	P1V05_GPU_CS_N	74 98
SENSE_DIFFPAIR	SENSE_1TO1_5SS	SENSE	ISNS_PP1V5_S0GPU_R_P	99
	SENSE_1TO1_5SS	SENSE	ISNS_PP1V5_S0GPU_R_N	99
SENSE_DIFFPAIR_42	SENSE_1TO1_5SS	SENSE	CPUIMVP_ISNS1G_P	46 66
SENSE_DIFFPAIR_42	SENSE_1TO1_5SS	SENSE	CPUIMVP_ISNS1G_N	46 66
SENSE_DIFFPAIR	SENSE_1TO1_5SS	SENSE	CPUIMVP_ISNS1G_R_P	46
	SENSE_1TO1_5SS	SENSE	CPUIMVP_ISNS1G_R_N	46
SENSE_DIFFPAIR	SENSE_1TO1_5SS	SENSE	ISNS_HS_OTHER_P	46
	SENSE_1TO1_5SS	SENSE	ISNS_HS_OTHER_N	46
SENSE_DIFFPAIR	SENSE_1TO1_5SS	SENSE	ISNS_HS_GPU_P	46
	SENSE_1TO1_5SS	SENSE	ISNS_HS_GPU_N	46
SENSE_DIFFPAIR	SENSE_1TO1_5SS	SENSE	ISNS_HS_COMPUTING_P	46
	SENSE_1TO1_5SS	SENSE	ISNS_HS_COMPUTING_N	46
SENSE_DIFFPAIR	SENSE_1TO1_5SS	SENSE	CPUIMVP_ISNS_P	46
	SENSE_1TO1_5SS	SENSE	CPUIMVP_ISNS_N	46
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	ADC1_VSENSE_P	
	AUDIODIFF	AUDIO	ADC1_VSENSE_N	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	ADC2_VSENSE_P	
	AUDIODIFF	AUDIO	ADC2_VSENSE_N	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	ADC2_ISENSE_P	96
	AUDIODIFF	AUDIO	ADC2_ISENSE_N	96
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	ADC2_ISENSE_P	96
	AUDIODIFF	AUDIO	ADC2_ISENSE_N	96
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKR_R_RSENSE_P	
	AUDIODIFF	AUDIO	SPKR_R_RSENSE_N	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKR_L_RSENSE_P	
	AUDIODIFF	AUDIO	SPKR_L_RSENSE_N	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_P	53 57
	AUDIODIFF	AUDIO	AUD_LO1_L_N	53 57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_P	53 57
	AUDIODIFF	AUDIO	AUD_LO1_R_N	53 57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_P	53 57
	AUDIODIFF	AUDIO	AUD_LO2_L_N	53 57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_P	53 57
	AUDIODIFF	AUDIO	AUD_LO2_R_N	53 57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_INL_P	53 58
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_INL_N	53 58
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_LIN_P	57
	AUDIODIFF	AUDIO	AUD_SPKRAMP_LIN_N	57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_RIN_P	57
	AUDIODIFF	AUDIO	AUD_SPKRAMP_RIN_N	57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_LSUBIN_P	57
	AUDIODIFF	AUDIO	AUD_SPKRAMP_LSUBIN_N	57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_RSUBIN_P	57
	AUDIODIFF	AUDIO	AUD_SPKRAMP_RSUBIN_N	57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	LSPKR_INTIV_RSENSE_P	
	AUDIODIFF	AUDIO	LSPKR_INTIV_RSENSE_N	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	RSPKR_INTIV_RSENSE_P	
	AUDIODIFF	AUDIO	RSPKR_INTIV_RSENSE_N	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	LSPKR_INTIV_P	
	AUDIODIFF	AUDIO	LSPKR_INTIV_N	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	RSPKR_INTIV_P	
	AUDIODIFF	AUDIO	RSPKR_INTIV_N	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	ISNS_TBT_N	99
	AUDIODIFF	AUDIO	ISNS_TBT_P	99
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	ISNS_TBT_R_N	99
	AUDIODIFF	AUDIO	ISNS_TBT_R_P	99

D2 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_P	7 34
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_N	7 34
	1TO1_DIFFPAIR		CHGR_CSI_R_P	61
	1TO1_DIFFPAIR		CHGR_CSI_R_N	61
	1TO1_DIFFPAIR		CHGR_CSO_R_P	61
	1TO1_DIFFPAIR		CHGR_CSO_R_N	61
(USB_EXTA)	USB_85D	USB	USB2_EXTA_MUXED_P	
(USB_EXTA)	USB_85D	USB	USB2_EXTA_MUXED_N	
(USB_EXTA)	USB_85D	USB	USB2_LT1_P	
(USB_EXTA)	USB_85D	USB	USB2_LT1_N	
	USB_85D	USB	CONN_USB2_BT_P	
	USB_85D	USB	CONN_USB2_BT_N	
	USB_85D	USB	USB_LT2_P	
	USB_85D	USB	USB_LT2_N	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRAMP_LIN_P	57
	AUDIODIFF	AUDIO	SPKRAMP_LIN_N	57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRAMP_RIN_P	57
	AUDIODIFF	AUDIO	SPKRAMP_RIN_N	57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SSM2375SL_P	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SSM2375SL_N	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SSM2375SR_P	
	AUDIODIFF	AUDIO	SSM2375SR_N	
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SL_OUT_P_R	
	DIFFPAIR	AUDIO	SPKRCONN_SL_OUT_N_R	
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SL_OUT_P	7 57 59
	DIFFPAIR	AUDIO	SPKRCONN_SL_OUT_N	7 57 59
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	LSPKR_VSENSE_FILT_P	
	DIFFPAIR	AUDIO	LSPKR_VSENSE_FILT_N	
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	RSPKR_VSENSE_FILT_P	
	DIFFPAIR	AUDIO	RSPKR_VSENSE_FILT_N	
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SR_OUT_P_R	
	DIFFPAIR	AUDIO	SPKRCONN_SR_OUT_N_R	
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SR_OUT_P	7 57 59
	DIFFPAIR	AUDIO	SPKRCONN_SR_OUT_N	7 57 59
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_L_OUT_P	7 57 59
	DIFFPAIR	AUDIO	SPKRCONN_L_OUT_N	7 57 59
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_R_OUT_P	7 57 59
	DIFFPAIR	AUDIO	SPKRCONN_R_OUT_N	7 57 59
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_S_OUT_P	
	DIFFPAIR	AUDIO	SPKRCONN_S_OUT_N	
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	LSPKR_ISENSE_FILT_P	
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	LSPKR_ISENSE_FILT_N	
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	RSPKR_ISENSE_FILT_P	
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	RSPKR_ISENSE_FILT_N	
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	RSUBIN_P	57
	DIFFPAIR	AUDIO	RSUBIN_N	57
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	LSUBIN_P	57
	DIFFPAIR	AUDIO	LSUBIN_N	57
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SSM4321SR_P	
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SSM4321SR_N	
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SSM4321SL_P	
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SSM4321SL_N	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	LSPKR_VSENSE_IN_P	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	LSPKR_VSENSE_IN_N	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	RSPKR_VSENSE_IN_P	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	RSPKR_VSENSE_IN_N	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	LSPKR_ISENSE_RDIVIDE_P	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	LSPKR_ISENSE_RDIVIDE_N	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	RSPKR_ISENSE_RDIVIDE_P	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	RSPKR_ISENSE_RDIVIDE_N	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	LSPKR_VSENSE_RDIVIDE_P	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	LSPKR_VSENSE_RDIVIDE_N	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	RSPKR_VSENSE_RDIVIDE_P	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	RSPKR_VSENSE_RDIVIDE_N	
	USB_85D	USB	USB_TPAD_R_P	26 49
	USB_85D	USB	USB_TPAD_R_N	26 49
	SB_POWER		PP3V3_S5	7 8
	SB_POWER		PP3V3_S0	7 8
	SB_POWER		PP1V5_S3RS0_CPUDDR	8
	GND		GND	

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Project Specific Constraints

Apple Inc.

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15" MBP BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	16.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
50_OHM_SE	*	Y	0.070 MM	0.070 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.116 MM	0.116 MM			
45_OHM_SE	*	Y	0.085 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.145 MM	0.095 MM			
40_OHM_SE	*	Y	0.105 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.095 MM			
37_OHM_SE	*	Y	0.120 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.265 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.190 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.124 MM	0.124 MM		0.200 MM	0.200 MM
72_OHM_DIFF	ISL2,ISL11	Y	0.124 MM	0.124 MM		0.200 MM	0.200 MM
72_OHM_DIFF	TOP,BOTTOM	Y	0.140 MM	0.140 MM		0.120 MM	0.120 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.096 MM	0.096 MM		0.126 MM	0.126 MM
80_OHM_DIFF	ISL2,ISL11	Y	0.096 MM	0.096 MM		0.126 MM	0.126 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.120 MM	0.120 MM		0.160 MM	0.160 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.089 MM	0.089 MM		0.180 MM	0.180 MM
85_OHM_DIFF	ISL2,ISL11	Y	0.089 MM	0.089 MM		0.180 MM	0.180 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.110 MM	0.110 MM		0.180 MM	0.180 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.081 MM	0.081 MM		0.200 MM	0.200 MM
90_OHM_DIFF	ISL2,ISL11	Y	0.081 MM	0.081 MM		0.200 MM	0.200 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.099 MM	0.090 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.065 MM	0.065 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL2,ISL11	Y	0.065 MM	0.065 MM		0.200 MM	0.200 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.079 MM	0.079 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	P072_SPACE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	0.1 MM	?
BGA_P2MM	*	0.2 MM	?
P072_SPACE	*	0.071 MM	?

15" MBP Specific Net Properties

	ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE	
1	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	ADC1_ISENSE_P	
2		AUDIODIFF	AUDIO	ADC1_ISENSE_N	
3	SENSE_DIFFPAIR_42	THERM_55S_CPUIMVPISNS1	THERM	CPUIMVP_ISNS1_P	46 65 66
4		THERM_55S_CPUIMVPISNS1	THERM	CPUIMVP_ISNS1_N	46 66
5	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPUIMVP_ISNS2G_P	46 66
6		THERM_1TO1_55S	THERM	CPUIMVP_ISNS2G_N	46 66
7	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPUIMVP_ISNS2_P	46 65 66
8		THERM_1TO1_55S	THERM	CPUIMVP_ISNS2_N	46 66
9	SENSE_DIFFPAIR	THERM_55S_CPUIMVPISNS1	THERM	CPUIMVP_ISNS3_P	46 65 66
10		THERM_55S_CPUIMVPISNS1	THERM	CPUIMVP_ISNS3_N	46 66
11	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPUIMVP_ISUM_R_P	46
12		THERM_1TO1_55S	THERM	CPUIMVP_ISUM_R_N	46
13	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPUIMVP_ISUMG_R_P	46
14		THERM_1TO1_55S	THERM	CPUIMVP_ISUMG_R_N	46
15	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GFXIMVP_ISNS1_P	80
16		THERM_1TO1_55S	THERM	GFXIMVP_ISNS1_N	80
17	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GFXIMVP_ISNS2_P	80
18		THERM_1TO1_55S	THERM	GFXIMVP_ISNS2_N	80
19	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	ISNS_CPU_DDR_R_P	98
20		THERM_1TO1_55S	THERM	ISNS_CPU_DDR_R_N	98
21	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	ISNS_LCD_PANEL_P	
22		THERM_1TO1_55S	THERM	ISNS_LCD_PANEL_N	
23	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	ISNS_P1V5R1V35_CPUDDR_P	
24		THERM_1TO1_55S	THERM	ISNS_P1V5R1V35_CPUDDR_N	
26	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	ISNS_SSD_P	39 99
25		THERM_1TO1_55S	THERM	ISNS_SSD_N	39 99
28	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	ISNS_SSD_R_P	99
27		THERM_1TO1_55S	THERM	ISNS_SSD_R_N	99
30	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	PCHVCCIOS0_CS_P	87 99
29		THERM_1TO1_55S	THERM	PCHVCCIOS0_CS_N	87 99
32	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	PCH_VCCIOSENSE_P	87
31		THERM_1TO1_55S	THERM	PCH_VCCIOSENSE_N	87
67	SENSE_DIFFPAIR	40_OHM_SE	THERM	GPUVCORE_SENSE_P	79 80
68	SENSE_DIFFPAIR	40_OHM_SE	THERM	GPUVCORE_SENSE_N	79 80
64		THERM_1TO1_55S	THERM	GPU_FBVDDQ_SENSE	73 74
63		THERM_1TO1_55S	THERM	GPU_FBGND_SENSE	73 74
65		THERM_1TO1_55S	THERM	P1V05_GPU_PEX_IOVDD_SNS_P	74 79
66		THERM_1TO1_55S	THERM	P1V05_GPU_PEX_IOVDD_SNS_N	74 79
33	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	SPKRL_THMSNS_D2_P	
34		THERM_1TO1_55S	THERM	SPKRL_THMSNS_D2_N	
35	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	SPKR_THMSNS_D2_P	
36		THERM_1TO1_55S	THERM	SPKR_THMSNS_D2_N	
37	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	TBT_THERMD_P	47
38		THERM_1TO1_55S	THERM	TBT_THERMD_N	47
39	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	X29THMSNS_D2_P	
40		THERM_1TO1_55S	THERM	X29THMSNS_D2_N	
57	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	VDDCIS0_CS_P	
58	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	VDDCIS0_CS_N	
59	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GFXIMVP6_VSEN_P	
60	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GFXIMVP6_VSEN_N	
41		USB_85D	USB3	USB3_EXTA_TX_F_P	
42		USB_85D	USB3	USB3_EXTA_TX_F_N	
43		USB_85D	USB3	USB3_EXTA_RX_F_P	
44		USB_85D	USB3	USB3_EXTA_RX_F_N	
45		USB_85D	USB3	USB3_EXTA_TX_C_P	40
46		USB_85D	USB3	USB3_EXTA_TX_C_N	40
47		USB_85D	USB3	USB3_EXTB_TX_C_P	7 38
48		USB_85D	USB3	USB3_EXTB_TX_C_N	7 38
49		USB_85D	USB3	USB3_EXTB_RX_RC_P	38
50		USB_85D	USB3	USB3_EXTB_RX_RC_N	38
70		USB_85D	USB3	USB3_EXTA_RX_RC_P	40
69		USB_85D	USB3	USB3_EXTA_RX_RC_N	40
61			CLK_25M	P1V5_GPU_VSNS	
62			CLK_25M	P1V0S0_VSNS	

Stackup-Defined Spacing Rules

Note: Outer dielectric is 0.058 mm nominal,
Inner dielectric is 0.053 mm nominal.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	TOP,BOTTOM	0.058 MM	?
2:1_SPACING	TOP,BOTTOM	0.116 MM	?
3:1_SPACING	TOP,BOTTOM	0.174 MM	?
4:1_SPACING	TOP,BOTTOM	0.232 MM	?
5:1_SPACING	TOP,BOTTOM	0.290 MM	?
1:1_SPACING	ISL3,ISL4,ISL9,ISL10	0.053 MM	?
2:1_SPACING	ISL3,ISL4,ISL9,ISL10	0.106 MM	?
3:1_SPACING	ISL3,ISL4,ISL9,ISL10	0.159 MM	?
4:1_SPACING	ISL3,ISL4,ISL9,ISL10	0.212 MM	?
5:1_SPACING	ISL3,ISL4,ISL9,ISL10	0.265 MM	?
1:1_SPACING	ISL2,ISL5,ISL6,ISL7,ISL8,ISL11	0.101 MM	?
2:1_SPACING	ISL2,ISL5,ISL6,ISL7,ISL8,ISL11	0.202 MM	?
3:1_SPACING	ISL2,ISL5,ISL6,ISL7,ISL8,ISL11	0.303 MM	?
4:1_SPACING	ISL2,ISL5,ISL6,ISL7,ISL8,ISL11	0.404 MM	?
5:1_SPACING	ISL2,ISL5,ISL6,ISL7,ISL8,ISL11	0.505 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1x_DIELECTRIC	TOP,BOTTOM	0.058 MM	?
2x_DIELECTRIC	TOP,BOTTOM	0.116 MM	?
3x_DIELECTRIC	TOP,BOTTOM	0.174 MM	?
4x_DIELECTRIC	TOP,BOTTOM	0.232 MM	?
5x_DIELECTRIC	TOP,BOTTOM	0.290 MM	?
1x_DIELECTRIC	ISL3,ISL4,ISL9,ISL10	0.053 MM	?
2x_DIELECTRIC	ISL3,ISL4,ISL9,ISL10	0.106 MM	?
3x_DIELECTRIC	ISL3,ISL4,ISL9,ISL10	0.159 MM	?
4x_DIELECTRIC	ISL3,ISL4,ISL9,ISL10	0.212 MM	?
5x_DIELECTRIC	ISL3,ISL4,ISL9,ISL10	0.265 MM	?
1x_DIELECTRIC	ISL2,ISL5,ISL6,ISL7,ISL8,ISL11	0.101 MM	?
2x_DIELECTRIC	ISL2,ISL5,ISL6,ISL7,ISL8,ISL11	0.202 MM	?
3x_DIELECTRIC	ISL2,ISL5,ISL6,ISL7,ISL8,ISL11	0.303 MM	?
4x_DIELECTRIC	ISL2,ISL5,ISL6,ISL7,ISL8,ISL11	0.404 MM	?
5x_DIELECTRIC	ISL2,ISL5,ISL6,ISL7,ISL8,ISL11	0.505 MM	?

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE: PCB Rule Definitions

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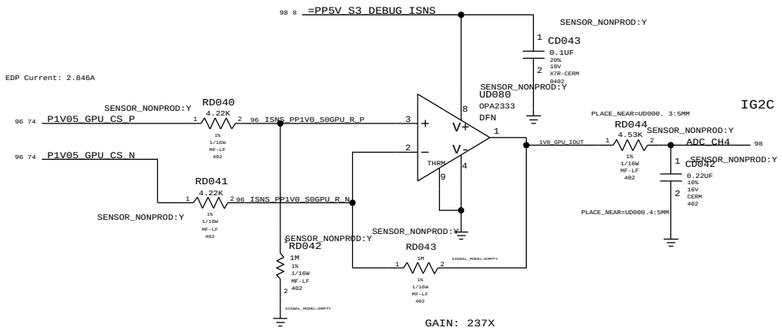
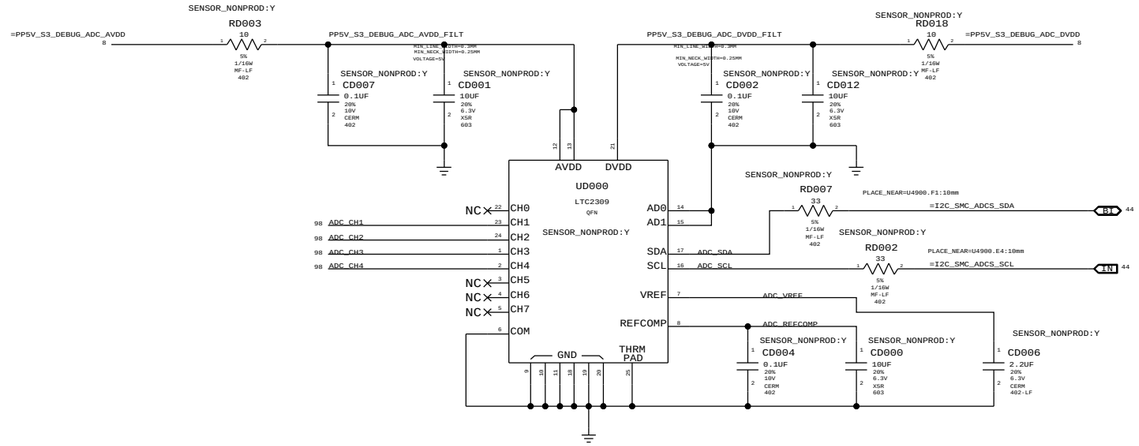
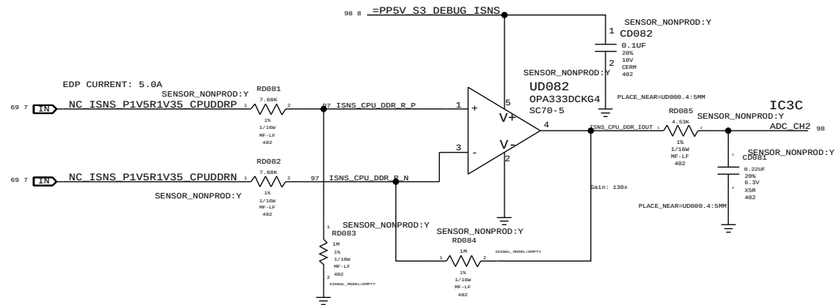
GPU 1.0V CURRENT SENSE

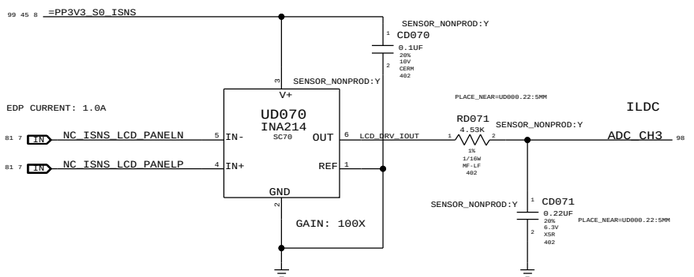


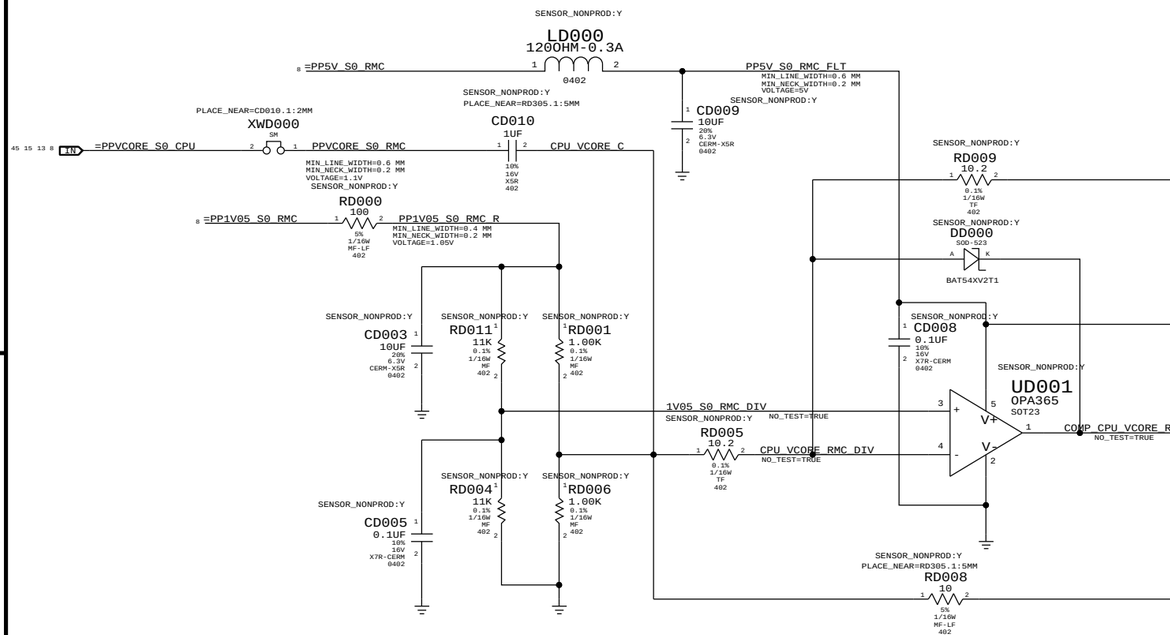


CPU DDR CURRENT SENSE



LCD PANEL CURRENT SENSE





SYNC_MASTER=D2_SEAN	SYNC_DATE=03/05/2017
PAGE TITLE	DEBUG SENSORS AND ADC
Apple Inc.	DRAWING NUMBER 051-9589
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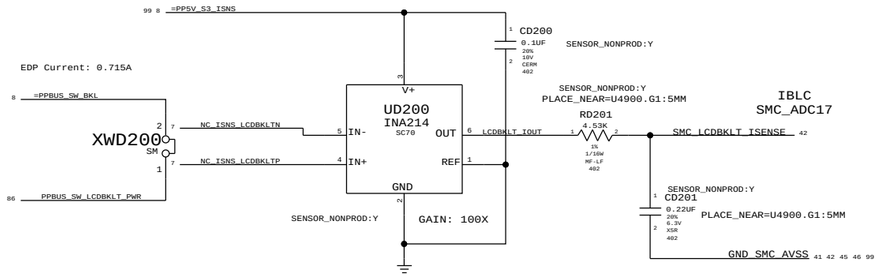
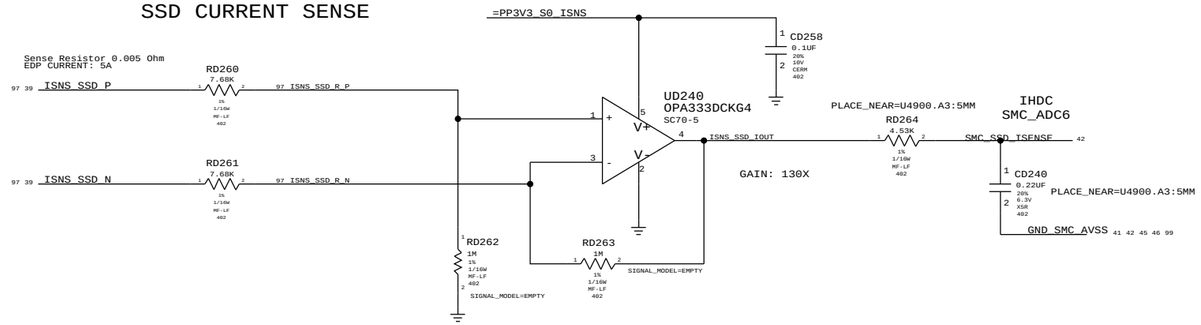
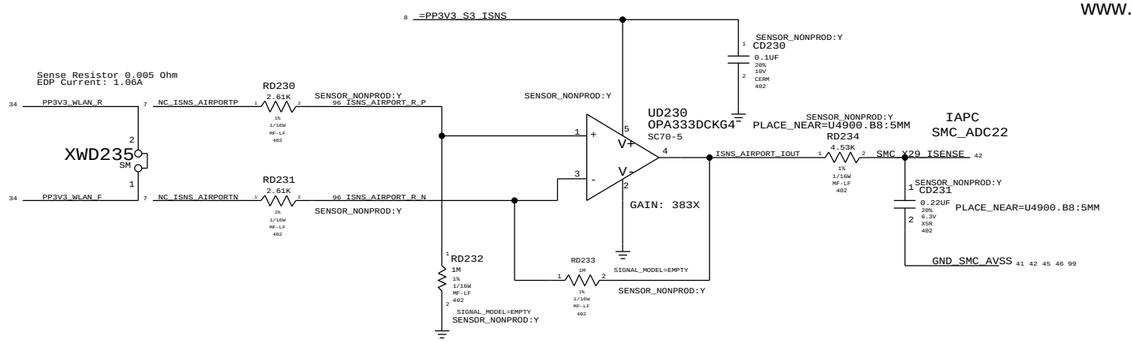
LCD BKLT Current Sense



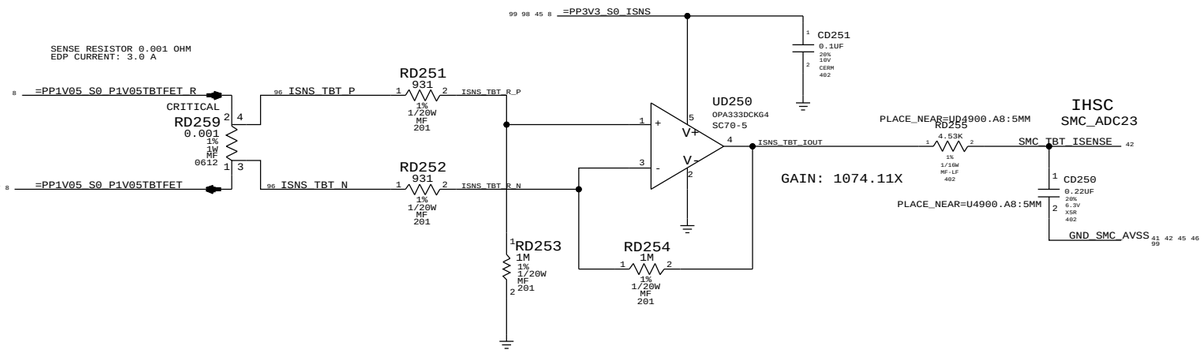
SSD CURRENT SENSE



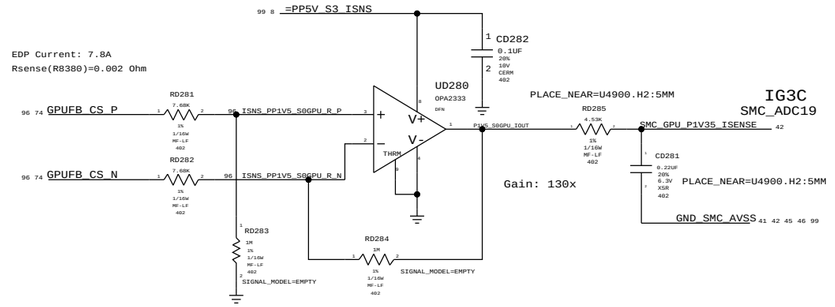
X29 AIRPORT CURRENT SENSE



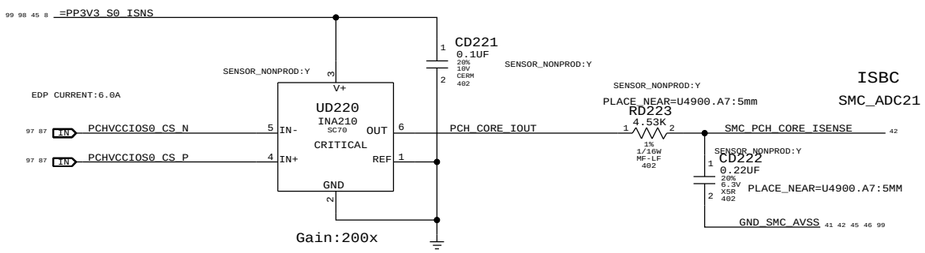
TBT (T29) CURRENT SENSE



GPU FB (1.35V/1.5V) CURRENT SENSE

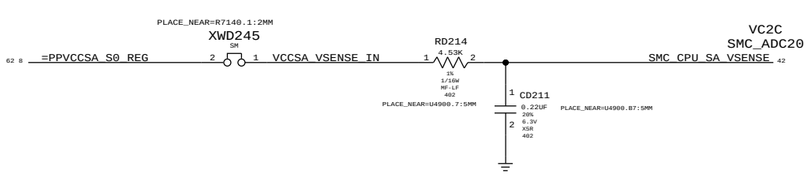


PCH VCORE CURRENT SENSE

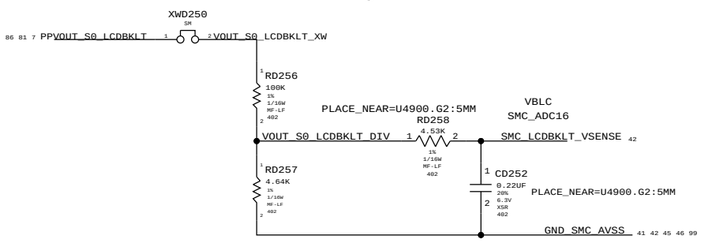


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0114	4	RES,MTL FILM,100K,5,1/16W,0402,SMD,LF	CD201,CD222,CD231		SENSOR_NONPROD:N

CPU VCCSA VOLTAGE SENSE



LCD BKLT Voltage Sense



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PAGE TITLE: SMC12 SENSORS EXTENDED

Apple Inc.

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