1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

X2407 MLB

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
5	0045688612	ENGINEERING RELEASED	2023-07-11

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4	5	SOC: CONFIG STRAPS	T585_REF_SOC_H15C_0.10.0	
5	6	SOC: RESETS, CLOCKS, SWD	T585_REF_SOC_H15C_0.10.0	
6	8	SOC: GPIO, I2C, I2S, SPI, UART	T585_REF_SOC_H15C_0.10.0	
7	10	SOC: LPDP, ISP	T585_REF_SOC_H15C_0.10.0	
8	12	SOC: PCIE	T585_REF_SOC_H15C_0.10.0	
9	14	SOC: CIO, USB	T585_REF_SOC_H15C_0.10.0	
10	16	SOC: AOP, SMC, NUB	T585_REF_SOC_H15C_0.10.0	
11	19	SOC: QSPI ROM, SEP ROM, VSNS	T585_REF_SOC_H15C_0.10.0	
12	20	SOC: SHARED SUPPORT 1	T585_REF_SOC_H15C_0.10.0	
13	21	SOC: SHARED SUPPORT 2	T585_REF_SOC_H15C_0.10.0	
14	22	SOC: SHARED SUPPORT 3	T585_REF_SOC_H15C_0.10.0	
15	23	SOC: POWER (CPU, GPU)	T585_REF_SOC_H15C_0.10.0	
16	25	SOC: POWER (SRAM, DISP, DCS)	T585_REF_SOC_H15C_0.10.0	
17	27	SOC: POWER (VDD1)	T585_REF_SOC_H15C_0.10.0	
18	29	SOC: POWER (VDDQ)	T585_REF_SOC_H15C_0.10.0	
19	31	SOC: POWER (AFR, ANE, CIO)	T585_REF_SOC_H15C_0.10.0	
20	33	SOC: POWER (FABRIC, FIXED)	T585_REF_SOC_H15C_0.10.0	
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22	37	SOC: POWER (VDD2H0)	T585_REF_SOC_H15C_0.10.0	
23	39	SOC: POWER (VDD2H1)	T585_REF_SOC_H15C_0.10.0	
24	41	SOC: GND-1	T585_REF_SOC_H15C_0.10.0	
25	42	SOC: GND-2	T585_REF_SOC_H15C_0.10.0	
26	43	SOC: GND-3	T585_REF_SOC_H15C_0.10.0	
27	50	Secure Element	T585_REF_SE_JUNO_0.1.3	
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30	53	CHARGER:SUPPORT	T585_REF_CHARGER_MANDOLA_28V_0.5.17	
31	54	MAGSAFE: CONNECTOR	T585_REF_MAGSAFE_ACE3_0.4.3	
32	55	MAGSAFE: PORT CONTROLLER	T585_REF_MAGSAFE_ACE3_0.4.3	
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34	57	POWER: 3V8 AON (1/2)	T585_REF_VR_ICEMAN_HP_0.33.10	
35	58	POWER: 3V8 AON (2/2)	T585_REF_VR_ICEMAN_HP_0.33.10	
36	59	page59	S-replace	04/28/2022
37	60	POWER: 3V8 AON OUTPUT THROTTLE	T585_REF_VR_ICEMAN_HP_0.33.10	
38	74	PMU PROJECT-SPECIFIC SUPPORT	T585_REF_PMU_CHAPEL_H15_0.42.0	
39	76	PMU OUTPUT DESENSE CAPS	T585_REF_PMU_CHAPEL_H15_0.42.0	
40	77	FPMU VIN/LDO/SW/GND	T585_REF_PMU_CHAPEL_H15_0.42.0	
41	78	FPMU BUCKS 0-7	T585_REF_PMU_CHAPEL_H15_0.42.0	
42	79	FPMU GPIO & BUCKS 8-9	T585_REF_PMU_CHAPEL_H15_0.42.0	
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44	81	LPMU VIN/LDO/SW/GND	T585_REF_PMU_CHAPEL_H15_0.42.0	
45	82	LPMU BUCKS 0-7	T585_REF_PMU_CHAPEL_H15_0.42.0	
46	83	LPMU GPIO & BUCKS 8-9	T585_REF_PMU_CHAPEL_H15_0.42.0	
47	84	LPMU BUCK IN/OUT CAPS	T585_REF_PMU_CHAPEL_H15_0.42.0	
48	85	PMU PROJECT-SPECIFIC SUPPORT 2	GAREN_MLB_C_0.5.1	07/25/2022
49	92	VDDH VR: Project Support	MLB_C_0.108.0	
50	93	VDDH VR: VDD, GND, Digital	T585_REF_VR_SPITFIRE_EKARA_H15C_0.18.7	
51	94	VDDH VR: Buck Controller	T585_REF_VR_SPITFIRE_EKARA_H15C_0.18.7	
52	95	VDDH VR: External Phases 0,1	T585_REF_VR_SPITFIRE_EKARA_H15C_0.18.7	
53	96	VDDH VR: External Phases 2,3	T585_REF_VR_SPITFIRE_EKARA_H15C_0.18.7	
54	97	VDDH VR: External Phase 5	T585_REF_VR_SPITFIRE_EKARA_H15C_0.18.7	
55	99	VDDH VR: Output Caps	T585_REF_VR_SPITFIRE_EKARA_H15C_0.18.7	
56	101	CLVR0	T585_REF_CLVR_SEBRING_0.33.0	
57	102	CLVR1	T585_REF_CLVR_SEBRING_0.33.0	
58	103	CLVR2	T585_REF_CLVR_SEBRING_0.33.0	
59	104	CLVR3	T585_REF_CLVR_SEBRING_0.33.0	
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61	120	CLVR PROJECT SUPPORT	T585_REF_CLVR_SEBRING_0.33.0	
62	122	POWER: 5V S2 TPS62130	T585_REF_VR_5V_TPS62130_0.22.0	
63	128	SPF 27UF Caps	MLB_C_0.108.0	
64	130	I2C Connections - AP	MLB_S_0.64.4	09/11/2022
65	131	I2C Connections - SMC	MLB_S_0.64.4	09/11/2022
66	132	I2C Connections - Other	X2682_JIAPENG_WANG2_MLB_S_0.86.4	09/11/2022
67	135	SENSORS: HIGH-SIDE (1/3)	update_sensor_for_mp	06/04/2023
68	136	SENSORS: HIGH-SIDE (2/3)	update_sensor_for_mp	06/04/2023
69	137	SENSORS: HIGH-SIDE(3/3)	update_sensor_for_mp	06/04/2023
70	138	SENSORS: LOW-SIDE (1/3)	update_sensor_for_mp	06/04/2023
71	139	SENSORS: LOW-SIDE (2/3)	update_sensor_for_mp	06/04/2023
72	140	SENSORS: LOW-SIDE (3/3)	sense_res_change_to_shortupdate_sensor_for_mp	06/04/2023
73	141	SENSORS:THERMAL	MLB_C_0.108.0	11/24/2022
74	142	SENSORS: ALIASES	MLB_C_0.108.0	11/14/2022
75	144	SENSORS: MOTION	T585_REF_IMU_SOVEREIGN_0.17.0	
76	145	FANS	MLB_S_0.64.4	11/14/2022
77	147	USB-C: Left Connectors	MLB_S_0.61.0	
78	148	USB-C: Alt Flipped Connector(s)	MLB_S_0.64.4	
79	149	USB-C: Connector(s)	MLB_S_0.64.4	
80	150	USB-C: High Speed ATC0	T585_REF_USBC_LFKA_3PRT_ACE3_0.45.0	
81	151	USB-C: High Speed ATC1	T585_REF_USBC_LFKA_3PRT_ACE3_0.45.0	
82	152	USB-C: Support 1 ATC01	T585_REF_USBC_LFKA_3PRT_ACE3_0.45.0	
83	153	USB-C: Support 2 ATC01	T585_REF_USBC_LFKA_3PRT_ACE3_0.45.0	
84	154	USB-C: Port Controller ATC0	T585_REF_USBC_LFKA_3PRT_ACE3_0.45.0	
85	155	USB-C: Port Controller ATC1	T585_REF_USBC_LFKA_3PRT_ACE3_0.45.0	
86	156	USB-C: USB2 RPT	T585_REF_USBC_LFKA_3PRT_ACE3_0.45.0	
87	157	USB-C: Support 3 ATC01	T585_REF_USBC_LFKA_3PRT_ACE3_0.45.0	
88	158	USB-C: 5V Regulator	T585_REF_USBC_VR_LT8642_1_0.11.0	
89	159	USB-C: ATC01 REGULATORS	T585_REF_USBC_LFKA_3PRT_ACE3_0.45.0	
90	160	USB-C: High Speed ATC2	T585_REF_USBC_LFKA_3PRT_ACE3_0.45.0	
91	162	USB-C: Support 1 ATC2	T585_REF_USBC_LFKA_3PRT_ACE3_0.45.0	
92	163	USB-C: Support 2 ATC2	T585_REF_USBC_LFKA_3PRT_ACE3_0.45.0	
93	164	USB-C: Port Controller ATC2	T585_REF_USBC_LFKA_3PRT_ACE3_0.45.0	
94	166	USB-C: USB2 RPT2	T585_REF_USBC_LFKA_3PRT_ACE3_0.45.0	
95	167	USB-C: HS Level Shifters ATC2	T585_REF_USBC_LFKA_3PRT_ACE3_0.45.0	
96	168	USB-C: 5V Regulator	T585_REF_USBC_VR_TPS62180_0.9.0	
97	169	USB-C: ATC2 REGULATORS	T585_REF_USBC_LFKA_3PRT_ACE3_0.45.0	
98	170	USB-C: SUPPORT	MLB_S_0.61.0	
99	175	HDMI: CONNECTOR	T585_REF_HDMI_COBRA_0.61.0	
100	176	HDMI: DESENSE FILTERS	T585_REF_HDMI_COBRA_0.61.0	
101	177	HDMI: COBRA	T585_REF_HDMI_COBRA_0.61.0	
102	178	HDMI: Project Support 1	T585_REF_HDMI_COBRA_0.61.0	
103	179	HDMI: Project Support 2	T585_REF_HDMI_COBRA_0.61.0	
104	181	USB-C: CIO Redrivers 2/3	T585_REF_CIO_RDVR_COLUMBUS_0.19.0	
105	182	USB-C: CIO Redrivers 4/5	T585_REF_CIO_RDVR_COLUMBUS_0.19.0	
106	195	SDCARD CONTROLLER	T585_REF_SDCARD_GL9755_V2_0.13.0	
107	196	SDCARD CONNECTOR	T585_REF_SDCARD_GL9755_V2_0.13.0	
108	197	SDCARD IO LS/BUF SUPPORT	T585_REF_SDCARD_GL9755_V2_0.13.0	
109	198	SDCARD POWER SUPPORT	T585_REF_SDCARD_GL9755_V2_0.13.0	
110	200	WIFI/BT: MODULE	T585_REF_WIRELESS_WILLAMETTE_0.35.0	
111	201	WIFI/BT: ANTENNA and GND	T585_REF_WIRELESS_WILLAMETTE_0.35.0	
112	220	STORAGE: SSD0 S5E MK2 <0>	T585_REF_STORAGE_S5E_MARK2_0.26.0	
113	221	STORAGE: SSD0 S5E MK2 <1>	T585_REF_STORAGE_S5E_MARK2_0.26.0	
114	222	STORAGE: SSD0 S5E MK2 <2>	T585_REF_STORAGE_S5E_MARK2_0.26.0	
115	223	STORAGE: SSD0 S5E MK2 <3>	T585_REF_STORAGE_S5E_MARK2_0.26.0	
116	224	STORAGE: SSD0 OCARINA & NAND VCC	T585_REF_STORAGE_S5E_MARK2_0.26.0	
117	225	STORAGE: SSD1 S5E MK2 <0>	T585_REF_STORAGE_S5E_MARK2_0.26.0	
118	226	STORAGE: SSD1 S5E MK2 <1>	T585_REF_STORAGE_S5E_MARK2_0.26.0	
119	227	STORAGE: SSD1 S5E MK2 <2>	T585_REF_STORAGE_S5E_MARK2_0.26.0	
120	228	STORAGE: SSD1 S5E MK2 <3>	T585_REF_STORAGE_S5E_MARK2_0.26.0	

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122	230	STORAGE: SSD SUPPORT	MLB_C_0.108.0	
123	232	CAMERA-SUPPORT	MLB_S_0.64.4	
124	234	CAMERA: FLEX CONNECTOR	MLB_S_0.62.0	
125	236	DISPLAY CONNECTOR	MLB_S_0.64.4	
126	237	DISPLAY POWER SEQUENCER	T585_REF_PANELPWR_2D_0.9.0	
127	238	LUXE LCD Backlight Driver	T585_REF_BLC_LUXE_0.36.0	
128	239	BCON CONNECTOR	MLB_S_0.61.0	
129	242	SECDIS: LID ANGLE SENSOR	T585_REF_SECDIS_LAS_H14X_0.3.0	
130	243	SECDIS: SAK	T585_REF_SECDIS_H14X_0.9.0	
131	245	AUDIO JACK CODEC	T585_REF_CODEC_CARLOW_1.6.0	
132	246	AUDIO AMPLIFIERS (1/2)	T585_REF_SPKRAMP_SN012776_3.10.0	
133	247	AUDIO AMPLIFIERS (2/2)	T585_REF_SPKRAMP_SN012776_3.10.0	
134	248	AUDIO CONNECTORS: AMPS	MLB_S_0.64.4	
135	249	AUDIO FLEX CONNECTORS	MLB_C_0.108.0	
136	250	BEN: KEYBD BKLT	T585_REF_BLC_BEN_KBD_ONLY_0.10.0	
137	251	KEYBOARD IOX, SUPPORT	T585_REF_KBD_34PIN_0.7.0	
138	252	KEYBOARD SIGNAL CONNECTOR, ESD	MLB_C_0.108.0	
139	253	TRACKPAD SUPPORT	T585_REF_TPAD_IF_PKG_LARGE_0.15.0	
140	254	TRACKPAD SUPPORT 2	MLB_C_0.108.0	
141	255	TOUCHID CONN	MLB_S_0.64.4	
142	256	TOUCHID SUPPORT	MLB_S_0.64.4	
143	266	FCT 1	MLB_S_0.56.0	
144	267	FCT 2	MLB_S_0.49.0	
145	268	FCT 3 and PMU TPs	SAKKOC_MLB_C_0.28.2	
146	270	Debug: LEDs	MLB_S_0.64.4	
147	271	Debug: Buttons	MLB_S_0.62.0	
148	281	DESENSE CAPS	MLB_C_0.108.0	
149	294	DEBUG: VITAMIN-C	MLB_C_0.118.0	
150	400	POWER ALIASES 1	MLB_S_0.62.0	
151	401	POWER ALIASES 2	MLB_S_0.61.1	
152	402	POWER ALIASES CLVR	MLB_C_0.108.0	
153	403	POWER ALIASES PMU (C)	T585_REF_PMU_CHAPEL_H15_0.42.0	
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155	406	SIGNAL ALIASES 2	MLB_S_0.64.4	
156	407	SIGNAL ALIASES 3	MLB_S_0.61.0	
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158	410	SIGNAL ALIASES-T724	MLB_S_0.61.0	
159	411	ALIASES FIXUP FOR PALMA	Patch S to C	04/30/2022
160	420	Signal Aliases - SGA/CGA Diffs	Raymond	06/08/2022
161	500	17.2 RULES		
162	600	BOM OPTION - SOC,NAND	MLB_S_0.64.4	02/27/2023
163	601	BOM OPTION TABLES	MLB_S_0.64.4	02/27/2023
164	602	BOM GROUPS	MLB_S_0.64.4	02/27/2023
165	603	BOM VARIANT TABLES	SKAIPRATH_MLB_C_0.36.2	02/27/2023
166	610	BOM ALTERNATES 1	MLB_S_0.64.4	02/27/2023
167	611	BOM ALTERNATES 2	MLB_S_0.64.4	02/27/2023
168	700	PACK OPTIONS	S-replace	04/28/2022

Schematic / PCB #'s

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-08286	1	SCHEM,MLB-C,X2407	SCH	CRITICAL	SCH
820-02935	1	PCBF,MLB-C,X2407	PCB	CRITICAL	PCB

CHECKPLUS RULE CONFIGURATIONS	
CHECK VOLTAGE IC - LEVELS	?
PCB TESTPOINTS ALLOWED	YES
CHECK FATAL PACK_OPTION	YES
CHECK RESISTOR VOLTAGE	NO

SCHEM, MLB, X2407

DRAWING TITLE: SCHEM,MLB-C,X2407

Apple Inc.

DRAWING NUMBER: 051-08286 SIZE: D
REVISION: 5.0.3
BRANCH:
PAGE: 1 OF 700
SHEET: 1 OF 168

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C MLB Support Pages

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Reference Design Pages

SOURCE PROJECT	SUB-DESIGN NAME	SUB-DESIGN PAGES	VERSION	HARD/SOFT	SYNC_DATE/TIME
T585	REF_SOC_H15C	5,6,8,10,12,14,16,19,20,21,22,23,25,27,29,31,33,35,37,39,41-43	0.10.0	S	2023_03_20_12:21:41
T585	REF_SE_JUNO	50	0.1.3	S	2023_05_29_07:43:40
T585	REF_DEADBATTERY_SAK	51	0.20.13	S	2023_05_29_08:37:07
T585	REF_CHARGER_MANDOLA_28V	52-53	0.5.17	S	2023_03_20_16:29:16
T585	REF_MAGSAFE_ACE3	54-56	0.4.3	S	2023_03_28_12:05:55
T585	REF_VR_ICEMAN_HP	57,58,60	0.33.10	H	2023_02_27_14:35:44
T585	REF_PMU_CHAPEL_H15	74,76,77-84,403	0.42.0	S	2023_03_30_15:45:28
T585	REF_VR_SPITFIRE_EKARA_H15C	93-97,99	0.18.7	S	2023_04_01_18:58:11
T585	REF_CLVR_SEBRING	101-105,120	0.33.0	S	2023_04_18_12:09:56
T585	REF_VR_5V_TPS62130	122	0.22.0	S	2022_08_09_10:59:10
T585	REF_IMU_SOVEREIGN	144	0.17.0	S	2023_05_28_23:27:43
T585	REF_USBC_VR_LT8642_1	158	0.11.0	S	2022_05_25_20:14:08
T585	REF_USBC_VR_TPS62180	168	0.9.0	S	2022_05_25_20:14:17
T585	REF_USBC_LFKA_3PRT_ACE3	150-157,159-160,162-164,166-167,169	0.45.0	S	2023_03_20_10:30:44
T585	REF_HDMI_COBRA	175-179	0.61.0	S	2023_02_27_14:56:09
T585	REF_CIO_RDVR_COLUMBUS	181,182	0.19.0	S	2022_09_14_12:27:44
T585	REF_SDCARD_GL9755_V2	195-198	0.13.0	S	2022_05_25_20:14:25
T585	REF_WIRELESS_WILLAMETTE	200-201	0.35.0	S	2023_03_27_11:51:36
T585	REF_STORAGE_S5E_MARK2	220-229	0.26.0	S	2022_08_12_17:22:42
T585	REF_PANELPWR_2D	237	0.9.0	S	2022_06_16_19:48:19
T585	REF_BLC_LUXE	238	0.36.0	S	2022_07_01_23:08:00
T585	REF_SECDIS_LAS_H14X	242	0.3.0	S	2022_05_25_20:16:02
T585	REF_SECDIS_H14X	243	0.9.0	S	2022_07_11_10:02:31
T585	REF_CODEC_CARLOW	245	1.6.0	S	2022_05_25_20:16:10
T585	REF_SPKRAMP_SN012776	246,247	3.10.0	S	2023_03_27_22:29:36
T585	REF_BLC_BEN_KBD_ONLY	250	0.10.0	S	2023_01_03_21:57:49
T585	REF_KBD_34PIN	251	0.7.0	S	2022_08_31_11:15:35
T585	REF_TPAD_IF_PKG_LARGE	253	0.15.0	S	2023_01_23_23:15:18

Pages Not Synced from Anywhere

Page Name	Reasoning
CSA 004: PD Parts	Unique PD design for SOC region
CSA 019: SOC Shared Support	Extra content relative to SGA
CSA 021: SOC Project Support	Extra content relative to SGA
CSA 120: CLVR Support	Extra CLVRs compared to SGA MLB
CSA 402: CLVR Aliases	Extra CLVRs compared to SGA MLB
CSA 407: Signal Aliases 3	Signals NC'd on SGA are connected on CGA
CSA 408: NC Aliases	Signals NC'd on SGA are connected on CGA
CSA 420: SGA/CGA Aliases	Fix net name diffs between SGA and CGA
CSA 60x: BOM Configuration	Each design has unique APNs
CSA 7xx: Pack Options	Unique combination of pack options

Reference Design Overrides

Page Name	Changes made
CSA196 : REF_SDCARD_GL9755_V2	JK600 SDCARD Connector replaced with 514-00180 to match the MCO for X2407.Also added GND_VOID=TRUE for pin 11,12,15 and 16.
CSA200 : REF_WIRELESS_WILLIAMETTE	Removed OFFPAGE ports from BT_I2C_DATA/CLK to satisfy ckplus
CSA157 : REF_USBC_LFKA_3PRT_ACE3	Added CKPLUS_WAIVE=NC_CHECKS for the net NC_UPC0_AID_ALERT
CSA053 : REF_CHARGER_MANDOLA_28V	Changed the bomoption on R5201 from OMIT_TABLE to AUX_SHORT
CSA053 : REF_CHARGER_MANDOLA_28V	Added CKPLUS_WAIVE=NO_VOLT to PP5V_VHGR_SW to satisfy ckplus
CSA250 : REF_BLC_BEN_KBD_ONLY	Changed MIN_NECK_WIDTH for KBDBKLT_SW2 net from 0.250 to 0.200
CSA253 : REF_TPAD_IF_PKG_LARGE	Added CKPLUS_WAIVE=NO_VOLT to PP3V3_S2_HOLD_IPD_FUNC1 to satisfy ckplus
CSA153 : REF_USBC_LFKA_3PRT_ACE3	Removed PPF300, UPC0/1_SOC_REQUEST_DFU path and the SOC_FORCE_DFU:NO pack options to fix the layout error
CSA093 : REF_VR_SPITFIRE_EKARA_H15c	Added dummy resistors R93B0 and R93B1 for UF boundary after pack option VPP:GND removed R93A0 and R93A1.

!DEF TBL_PINDELAY_REFDES=U0600 !DEF TBL_PINDELAY_CSVFILE_NAME=CGA_PINDELAY_2020-05-01.CSV

Pin delay table removed due to pin delay import error causing fatal checkplus error
Recommend adding the table entry back once error is resolved

SYNC_DATE=

PAGE TITLE
REFERENCE DESIGN TABLE

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MAGSAFE BOSS

BS0450
2.7X1.8R-1.4ID-1.7H-SM
860-01714

BS0451
2.7X1.8R-1.4ID-1.7H-SM
860-01714

L USBC BOSS

BS04F0
2.7X1.8R-1.4ID-1.7H-SM
860-01714

BS04F1
2.7X1.8R-1.4ID-1.7H-SM
860-01714

BS04F2
2.7X1.8R-1.4ID-1.7H-SM
860-01714

R USBC BOSS

BS04G0
2.7X1.8R-1.4ID-1.7H-SM
860-01714

BS04G1
2.7X1.8R-1.4ID-1.7H-SM
860-01714

ANTENNA BOSS

BS04L0
2.7X1.8R-1.4ID-1.7H-SM
860-01714

BS04L1
2.7X1.8R-1.4ID-1.7H-SM
860-01714

BS04L2
BOSS-2.9X4.7-2.1H-SM
860-01841

DISP, CAM BOSS

BS04P0
2.7X1.8R-1.4ID-1.7H-SM
860-01714

BS04P1
2.7X1.8R-1.4ID-1.7H-SM
860-01714

BKLT BOSS

BS04P2
2.7X1.8R-1.4ID-1.7H-SM
860-01714

BS04P3
2.7X1.8R-1.4ID-1.7H-SM
860-01714

LAS BOSS

BS04R0
2.7X1.8R-1.4ID-1.7H-SM
860-01714

BS04R1
2.7X1.8R-1.4ID-1.7H-SM
860-01714

L SPEAKER BOSS

BS04R2
2.7X1.8R-1.4ID-1.7H-SM
860-01714

R SPEAKER BOSS

BS04R3
2.7X1.8R-1.4ID-1.7H-SM
860-01714

AUDIO JACK BOSS

BS04R4
2.7X1.8R-1.4ID-1.7H-SM
860-01714

BS04R5
2.7X1.8R-1.4ID-1.7H-SM
860-01714

TRACKPAD BOSS

BS04T0
3.4OD1.75ID-2.01H-SM
860-01805

BS04T1
3.4OD1.75ID-2.01H-SM
860-01805

TOUCHID BOSS

BS04T2
2.7X1.8R-1.34H-SM
860-01936

BS04T3
2.7X1.8R-1.34H-SM
860-01936

DFM DUMMY CAPS

C0400 15UF 20% 2.5V X6S 0402-1
C0401 15UF 20% 2.5V X6S 0402-1
C0402 15UF 20% 2.5V X6S 0402-1

BUMPERS

860-01715

BM0400 2.8OD1.2ID-2.0H-SM
BM0401 2.8OD1.2ID-2.0H-SM
BM0402 2.8OD1.2ID-2.0H-SM
BM0403 2.8OD1.2ID-2.0H-SM
BM0404 2.8OD1.2ID-2.0H-SM
BM0405 2.8OD1.2ID-2.0H-SM
BM0406 2.8OD1.2ID-2.0H-SM
BM0410 2.8OD1.2ID-2.0H-SM
BM0413 2.8OD1.2ID-2.0H-SM
BM0407 2.8OD1.2ID-4.6H-SM
BM0408 2.8OD1.2ID-4.6H-SM

BOTTOM BUMPERS

860-01839

BM0430 2.8OD1.2ID-4.0H-SM
BM0431 2.8OD1.2ID-4.0H-SM
BM0432 2.8OD1.2ID-4.0H-SM
BM0412 2.8OD1.2ID-4.0H-SM
BM0411 2.8OD1.2ID-4.0H-SM
BM0433 2.8OD1.2ID-4.0H-SM
BM0434 2.8OD1.2ID-4.0H-SM
BM0435 2.8OD1.2ID-4.0H-SM
BM0436 2.8OD1.2ID-4.0H-SM
BM0437 2.8OD1.2ID-4.0H-SM
BM0438 2.8OD1.2ID-4.0H-SM

POGO PINS

870-12862

PG0400 POGO-2.3OD-4.88-LOW FORCE SM
PG0401 POGO-2.3OD-4.88-LOW FORCE SM
PG0402 POGO-2.3OD-4.88-LOW FORCE SM
PG0403 POGO-2.3OD-4.88-LOW FORCE SM
PG0404 POGO-2.3OD-4.88-LOW FORCE SM
PG0405 POGO-2.3OD-4.88-LOW FORCE SM
PG0406 POGO-2.3OD-4.88-LOW FORCE SM
PG0407 POGO-2.3OD-4.88-LOW FORCE SM
PG0408 POGO-2.3OD-4.88-LOW FORCE SM
PG0409 POGO-2.3OD-4.88-LOW FORCE SM
PG0410 POGO-2.3OD-4.88-LOW FORCE SM

SHIELD CAN SLOTS

998-04440

SH0400 TH-NSP SL-1.2X0.4-1.5X0.7 OMIT_TABLE	SH0401 TH-NSP SL-1.2X0.4-1.5X0.7	Left 2 Burnside USBC Ports
SH0402 TH-NSP SL-1.2X0.4-1.5X0.7 OMIT_TABLE	SH0403 TH-NSP SL-1.2X0.4-1.5X0.7	Left Spitfire
SH0404 TH-NSP SL-1.2X0.4-1.5X0.7 OMIT_TABLE	SH0407 TH-NSP SL-1.2X0.4-1.5X0.7	Right Spitfire
SH0405 TH-NSP SL-1.2X0.4-1.5X0.7 OMIT_TABLE	SH0406 TH-NSP SL-1.2X0.4-1.5X0.7	Columbus Retimer
SH0408 TH-NSP SL-1.2X0.4-1.5X0.7 OMIT_TABLE	SH0409 TH-NSP SL-1.2X0.4-1.5X0.7	SDCARD
SH0410 TH-NSP SL-1.2X0.4-1.5X0.7 OMIT_TABLE	SH0411 TH-NSP SL-1.2X0.4-1.5X0.7	Right 1 Burnside USBC Port
SH0412 TH-NSP SL-1.2X0.4-1.5X0.7 OMIT_TABLE	SH0413 TH-NSP SL-1.2X0.4-1.5X0.7	HDMI Madea HDMI Madea
SH0414 TH-NSP SL-1.2X0.4-1.5X0.7 OMIT_TABLE	SH0415 TH-NSP SL-1.2X0.4-1.5X0.7	North Chapel Slave
SH0416 TH-NSP SL-1.2X0.4-1.5X0.7 OMIT_TABLE	SH0417 TH-NSP SL-1.2X0.4-1.5X0.7	Iceman
SH0418 TH-NSP SL-1.2X0.4-1.5X0.7 OMIT_TABLE	SH0419 TH-NSP SL-1.2X0.4-1.5X0.7	Top Left Spitfire
SH0422 TH-NSP SL-1.2X0.4-1.5X0.7 OMIT_TABLE	SH0423 TH-NSP SL-1.2X0.4-1.5X0.7	Top Right Spitfire

BOTTOM 1 TP TP-P4 WSHR01
BOTTOM 1 TP TP-P4 WSHR02
BOTTOM 1 TP TP-P4 WSHR03
BOTTOM 1 TP TP-P4 WSHR04
TOP 1 TP TP-P4 SOCFNC01

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
806-34812	1	Left 2 Burnside USBC Ports	SH0400	CRITICAL	
806-39753	1	Bottom Left Spitfire	SH0402	CRITICAL	
806-39752	1	Bottom Right Spitfire	SH0404	CRITICAL	
806-37364	1	Top Left Spitfire	SH0418	CRITICAL	
806-37365	1	Top Right Spitfire	SH0422	CRITICAL	
806-34809	1	Columbus Retimer Fence	SH0405	CRITICAL	
806-34667	1	SDCARD Fence	SH0408	CRITICAL	
806-34811	1	Right 1 Burnside USBC Port Fence	SH0410	CRITICAL	
806-34810	1	HDMI Cobrs Fence	SH0412	CRITICAL	
806-34685	1	North Maverick Slave Fence	SH0414	CRITICAL	
806-34813	1	Iceman Fence	SH0416	CRITICAL	
806-41466	1	SOC STIFFENER	SOCFNC01	CRITICAL	
860-02624	4	WASHER, SMT	WSHR01,WSHR02,WSHR03,WSHR04	CRITICAL	

PAGE TITLE
PD PARTS

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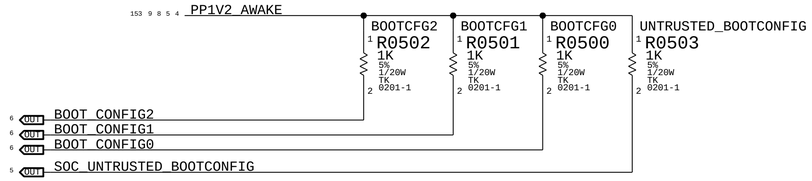
BOOT CONFIG

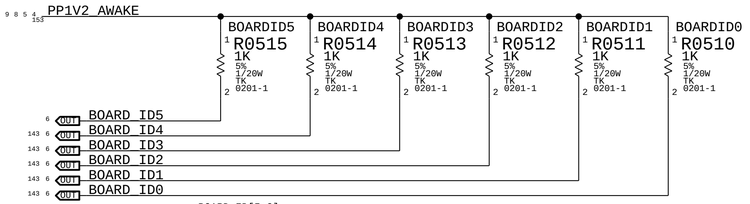


BOOT_CONFIGFG[2:0]	MODE
000	RESERVED
001	RESERVED
BACKUP ---> 010	QSPI NOR (24MHZ)
011	RESERVED
100	SPI NOR (6MHZ)
101	SPI NOR (12MHZ)
POR ---> 110	QSPI NOR (40MHZ)
111	SPI NOR (40MHZ)

SW READ FLOW

1. SET GPIO AS INPUT
2. ENABLE IPD
3. WAIT 100 MILLISECONDS
4. READ VALUES
5. DISABLE GPIOS

BOARD ID

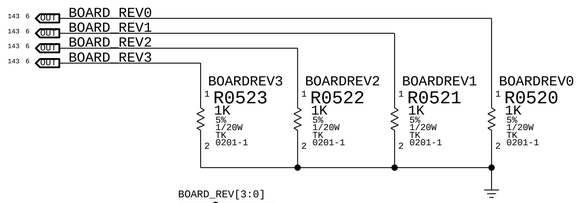


BOARD_ID[5:0]
000100 X2406 FF
000101 X2406 DEV
000110 X2407 FF
000111 X2407 DEV

HW READ FLOW

- HARDWARE SAMPLED BEFORE AP TAKEN OUT OF RESET
- SEE CHIPPADS INTEGRATION SPEC, SECTION 2.4.7

BOARD REV



BOARD_REV[3:0]	
0000	0x0
0001	0x1
0010	0x2
0011	0x3
0100	0x4
0101	0x5
0110	0x6
0111	0x7
1000	0x8
1001	0x9
1010	0xA
1011	0xB
1100	0xC
1101	0xD
1110	0xE
1111	0xF

SW READ FLOW

- SAMPLED IN IBOOT ONCE AP IS RUNNING

BOM_COST_GROUP=SOC

PAGE TITLE
SOC: CONFIG STRAPS

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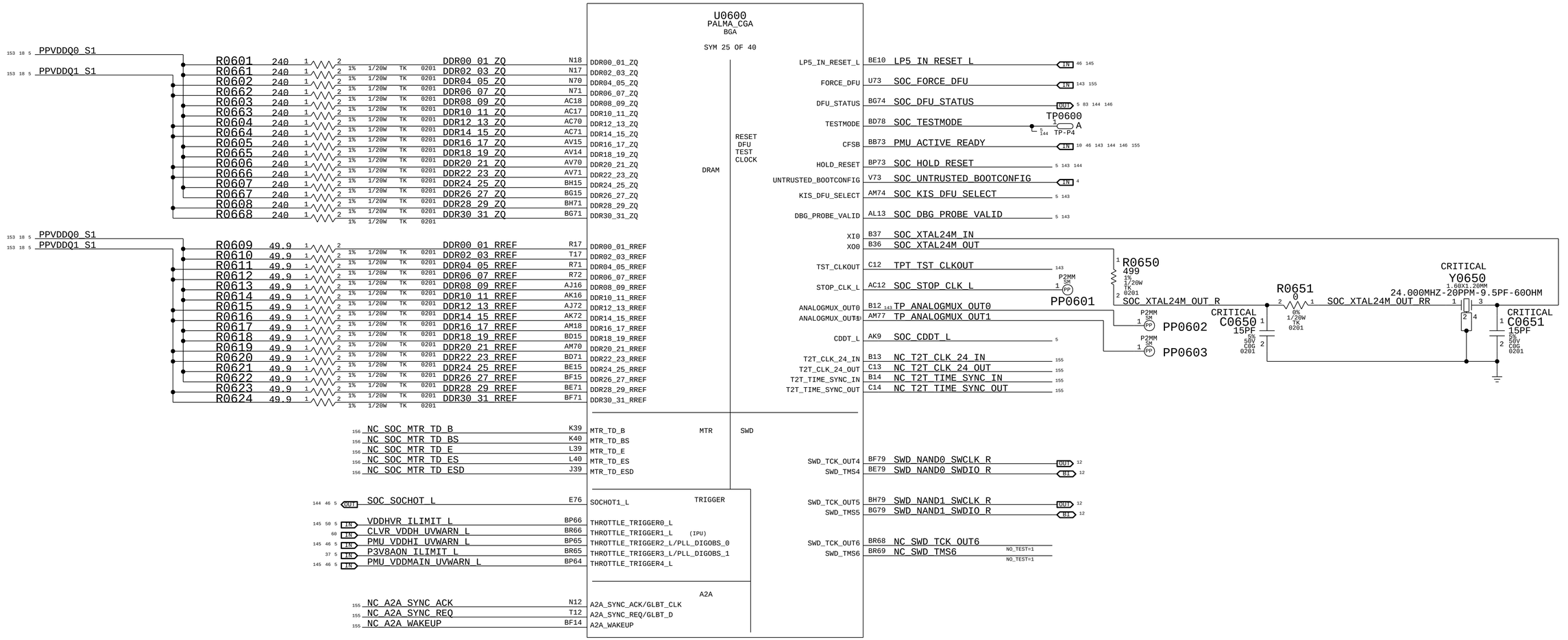

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PAGE TITLE	SOC: RESETS, CLOCKS, SWD
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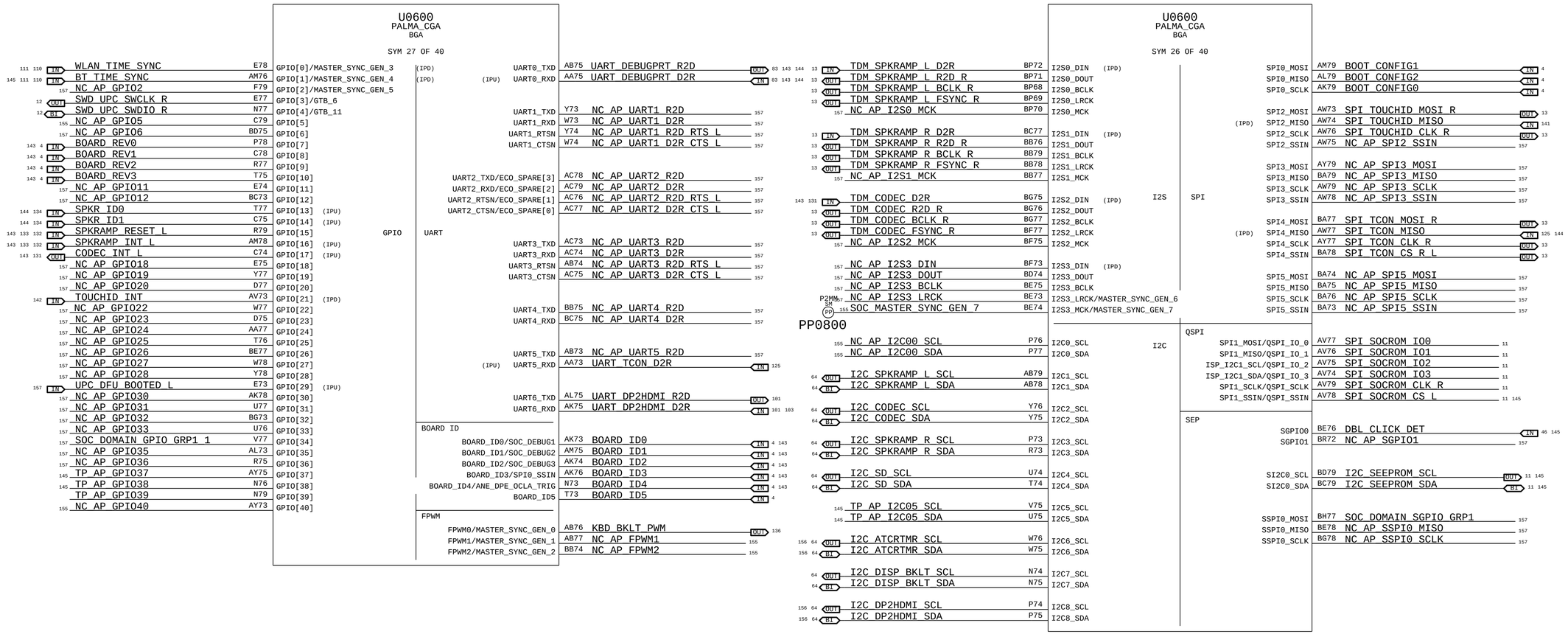

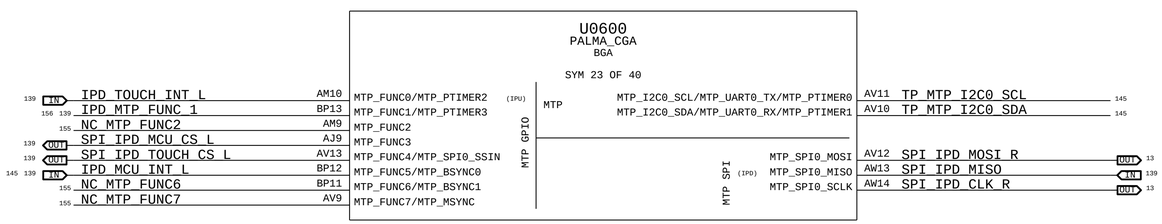

BOM_COST_GROUP=SOC

PAGE TITLE
SOC: GPIO, I2C, I2S, SPI, UART

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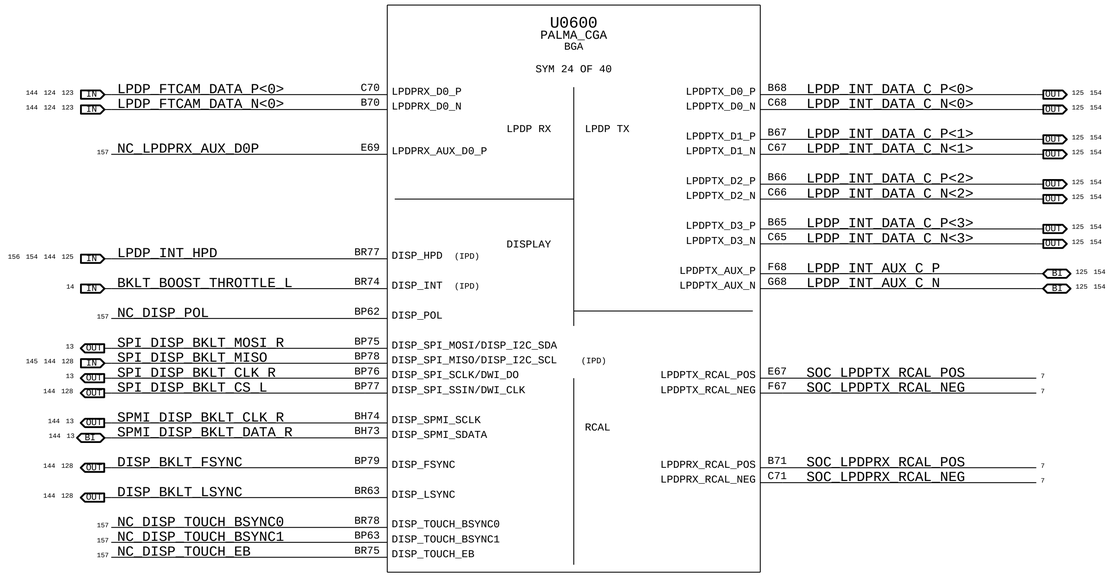

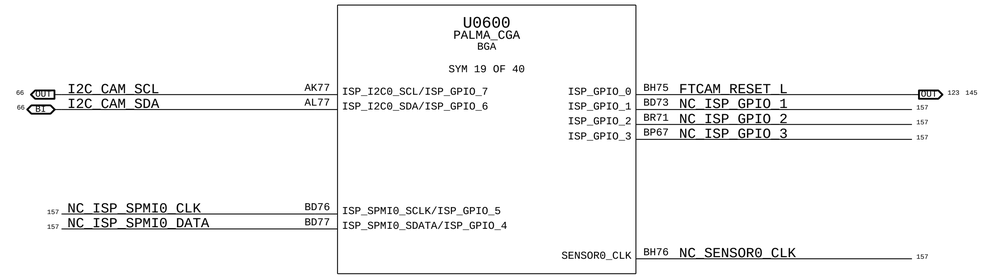

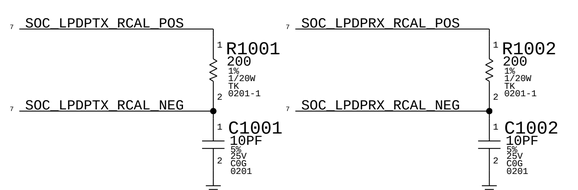

PAGE TITLE
SOC: LPDP, ISP

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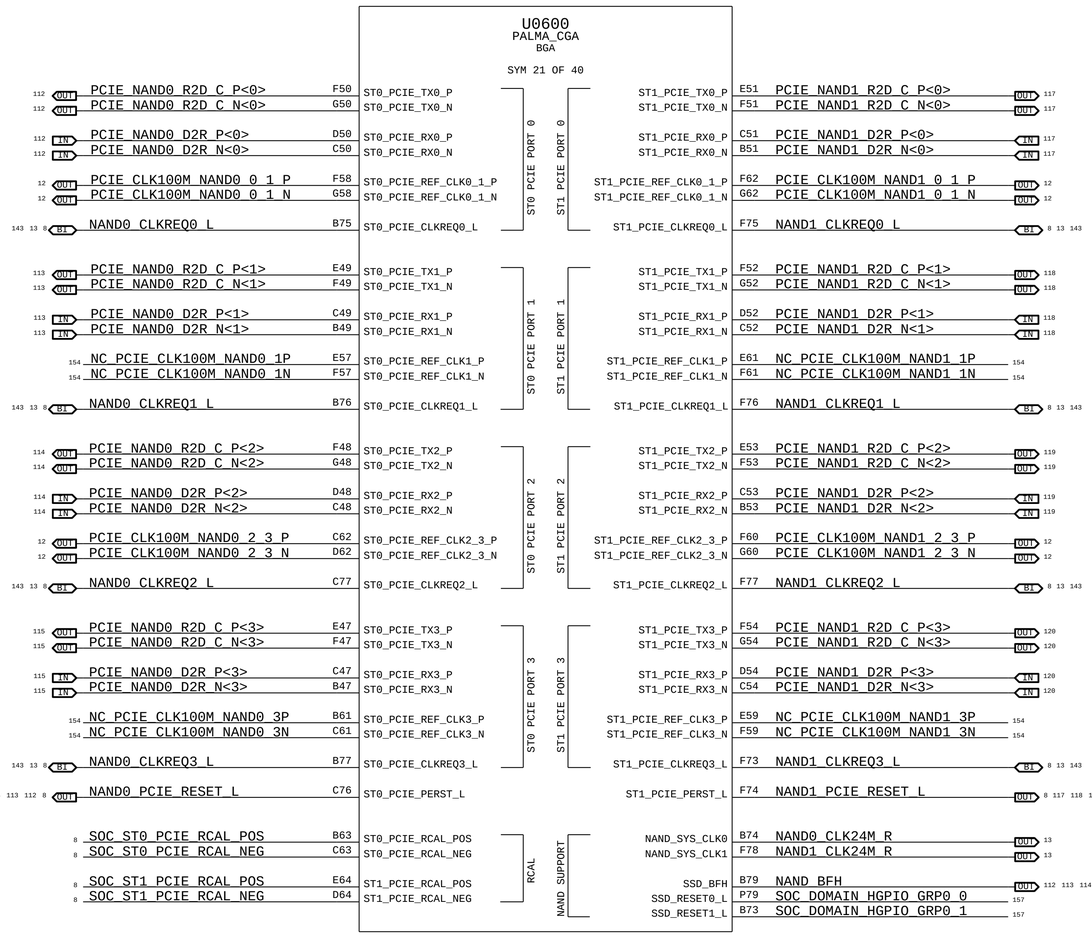

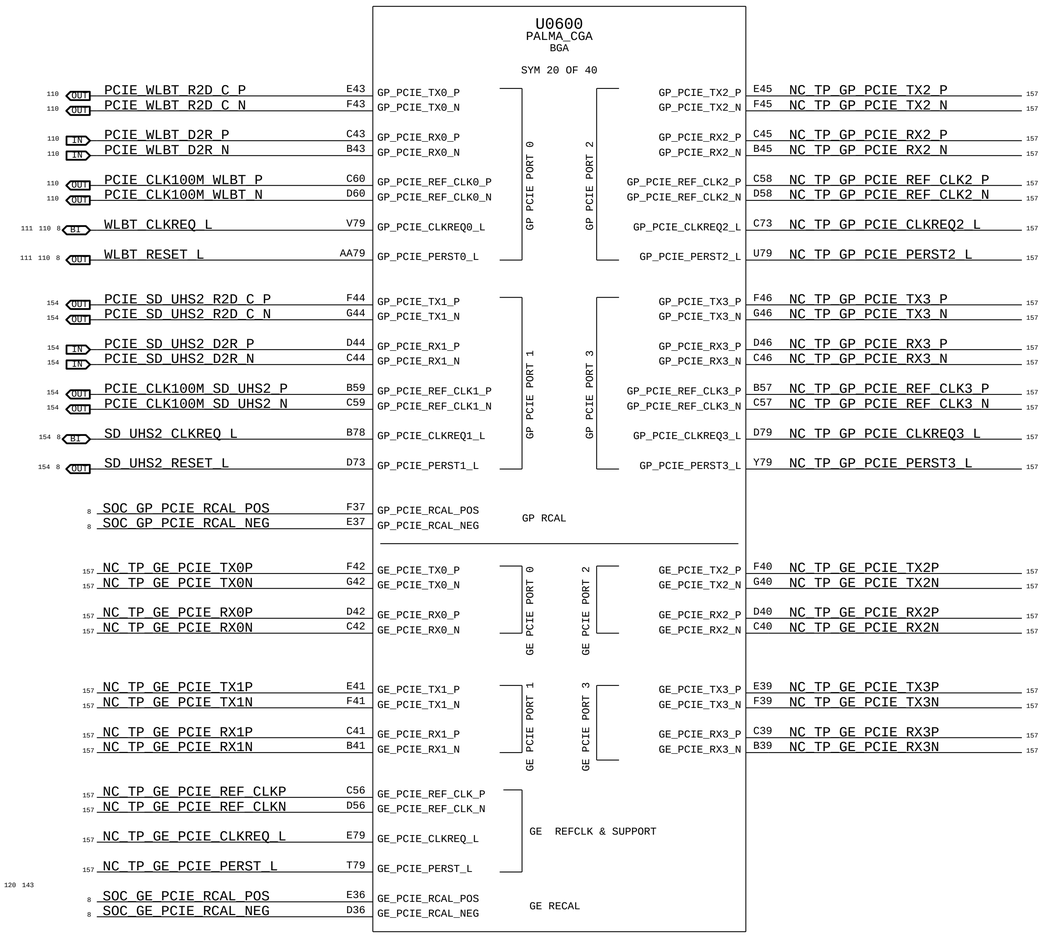

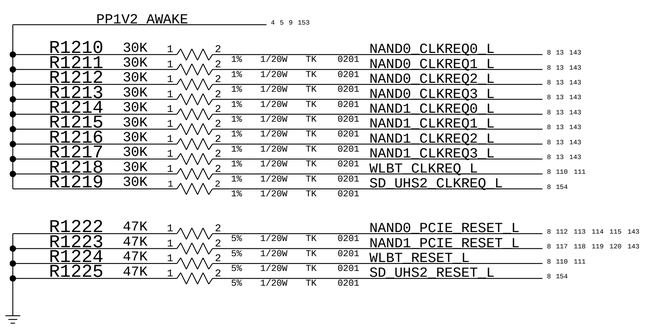

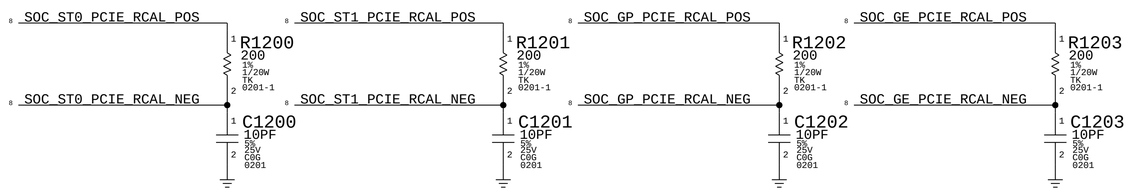

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PAGE TITLE: SOC: PCIE

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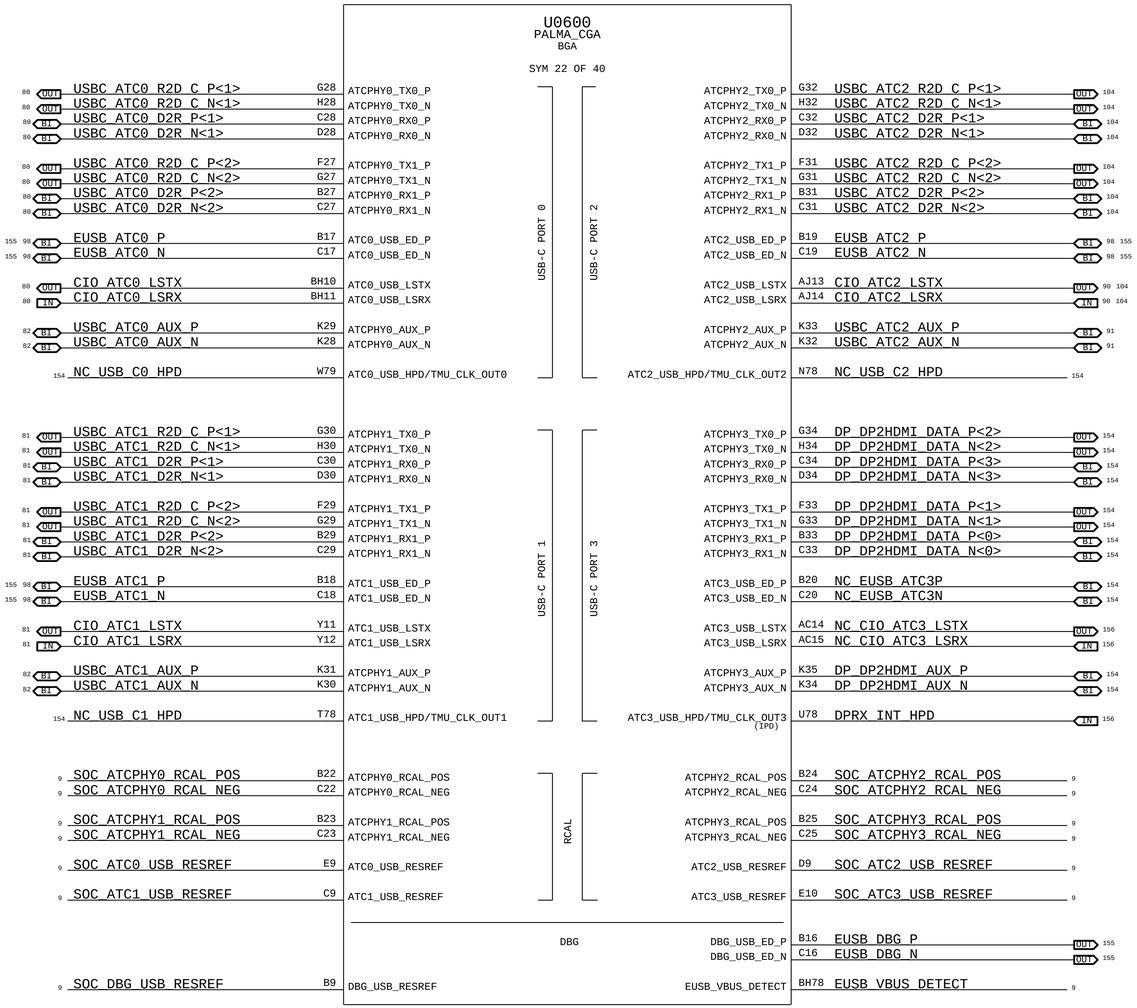

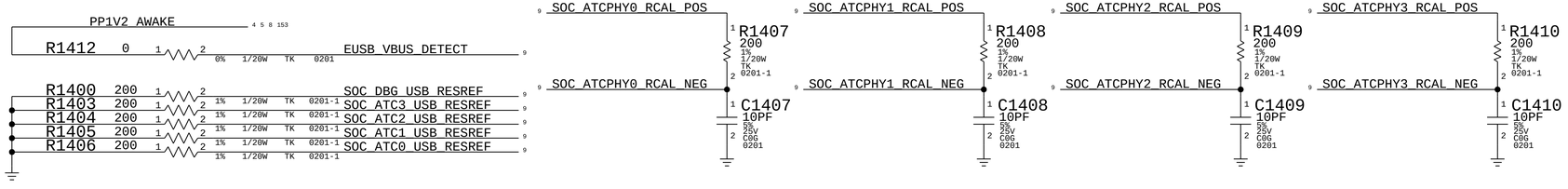

BOM_COST_GROUP=SOC

PAGE TITLE
SOC: CIO, USB

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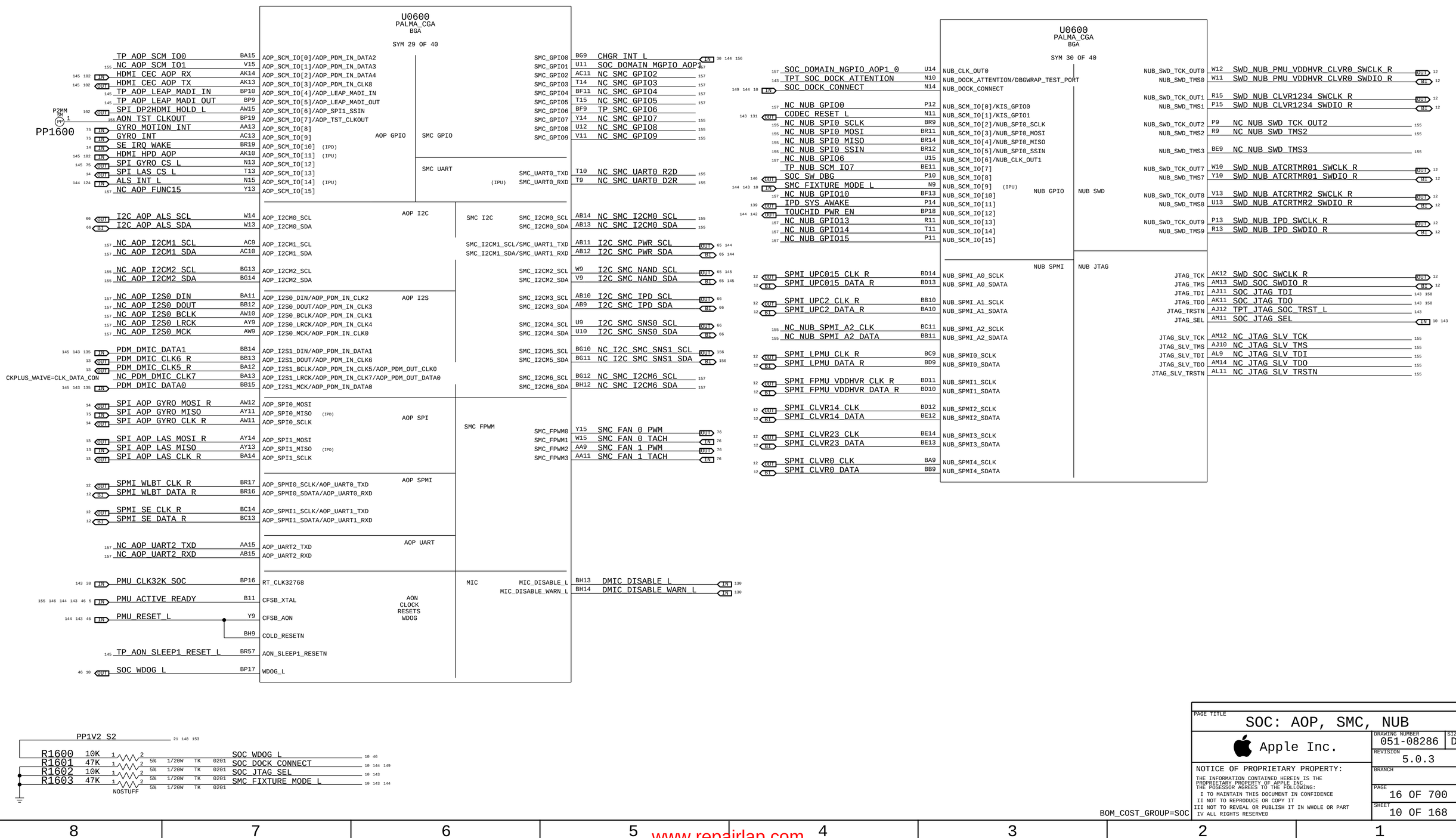
U0600
PALMA_CGA
BGA
SYM 29 OF 40
AOP GPIO
SMC GPIO
SMC UART
AOP I2C
SMC I2C
AOP I2S
AOP SPI
SMC FPWM
AOP SPMI
AOP UART
MIC
AON CLOCK RESETS WDOG
TP_AOP_SCM_IO0
NC_AOP_SCM_IO1
HDMI_CEC_AOP_RX
HDMI_CEC_AOP_TX
TP_AOP_LEAP_MADI_IN
TP_AOP_LEAP_MADI_OUT
SPI_DP2HDMI_HOLD_L
AON_TST_CLKOUT
GYRO_MOTION_INT
GYRO_INT
SE_IRQ_WAKE
HDMI_HPD_AOP
SPI_GYRO_CS_L
SPI_LAS_CS_L
ALS_INT_L
NC_AOP_FUNC15
I2C_AOP_ALS_SCL
I2C_AOP_ALS_SDA
NC_AOP_I2CM1_SCL
NC_AOP_I2CM1_SDA
NC_AOP_I2CM2_SCL
NC_AOP_I2CM2_SDA
NC_AOP_I2S0_DIN
NC_AOP_I2S0_DOUT
NC_AOP_I2S0_BCLK
NC_AOP_I2S0_LRCK
NC_AOP_I2S0_MCK
PDM_DMIC_DATA1
PDM_DMIC_CLK6_R
PDM_DMIC_CLK5_R
NC_PDM_DMIC_CLK7
PDM_DMIC_DATA0
SPI_AOP_GYRO_MOSI_R
SPI_AOP_GYRO_MISO
SPI_AOP_GYRO_CLK_R
SPI_AOP_LAS_MOSI_R
SPI_AOP_LAS_MISO
SPI_AOP_LAS_CLK_R
SPMI_WLBT_CLK_R
SPMI_WLBT_DATA_R
SPMI_SE_CLK_R
SPMI_SE_DATA_R
NC_AOP_UART2_TXD
NC_AOP_UART2_RXD
PMU_CLK32K_SOC
PMU_ACTIVE_READY
PMU_RESET_L
TP_AON_SLEEP1_RESET_L
SOC_WDOG_L
CHGR_INT_L
SOC_DOMAIN_MGPIO_AOP1
NC_SMC_GPIO2
NC_SMC_GPIO3
NC_SMC_GPIO4
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TP_SMC_GPIO6
NC_SMC_GPIO7
NC_SMC_GPIO8
NC_SMC_GPIO9
NC_SMC_UART0_R2D
NC_SMC_UART0_D2R
NC_SMC_I2CM0_SCL
NC_SMC_I2CM0_SDA
I2C_SMC_PWR_SCL
I2C_SMC_PWR_SDA
I2C_SMC_NAND_SCL
I2C_SMC_NAND_SDA
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I2C_SMC_IPD_SDA
I2C_SMC_SNS0_SCL
I2C_SMC_SNS0_SDA
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NC_SMC_I2CM6_SDA
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SMC_FAN_0_TACH
SMC_FAN_1_PWM
SMC_FAN_1_TACH
DMIC_DISABLE_L
DMIC_DISABLE_WARN_L
PP1600
P2MM SM PP 1
PP1V2_S2
R1600 10K
R1601 47K
R1602 10K
R1603 47K
5% 1/20W TK 0201
NOSTUFF
SOC_DOCK_CONNECT
SOC_JTAG_SEL
SOC_FIXTURE_MODE_L
U0600
PALMA_CGA
BGA
SYM 30 OF 40
NUB GPIO
NUB SWD
NUB SPMI
NUB JTAG
SOC_DOMAIN_NGPIO_AOP1_0
TPT_SOC_DOCK_ATTENTION
SOC_DOCK_CONNECT
NC_NUB_GPIO0
CODEC_RESET_L
NC_NUB_SPI0_SCLK
NC_NUB_SPI0_MOSI
NC_NUB_SPI0_MISO
NC_NUB_SPI0_SSIN
NC_NUB_GPIO6
TP_NUB_SCM_IO7
SOC_SW_DBG
SMC_FIXTURE_MODE_L
NC_NUB_GPIO10
IPD_SYS_AWAKE
TOUCHID_PWR_EN
NC_NUB_GPIO13
NC_NUB_GPIO14
NC_NUB_GPIO15
SPMI_UPC015_CLK_R
SPMI_UPC015_DATA_R
SPMI_UPC2_CLK_R
SPMI_UPC2_DATA_R
NC_NUB_SPMI_A2_CLK
NC_NUB_SPMI_A2_DATA
SPMI_LPMU_CLK_R
SPMI_LPMU_DATA_R
SPMI_FPMU_VDDHVR_CLK_R
SPMI_FPMU_VDDHVR_DATA_R
SPMI_CLVR14_CLK
SPMI_CLVR14_DATA
SPMI_CLVR23_CLK
SPMI_CLVR23_DATA
SPMI_CLVR0_CLK
SPMI_CLVR0_DATA
SWD_NUB_PMU_VDDHVR_CLVR0_SWCLK_R
SWD_NUB_PMU_VDDHVR_CLVR0_SWDIO_R
SWD_NUB_CLVR1234_SWCLK_R
SWD_NUB_CLVR1234_SWDIO_R
NC_NUB_SWD_TCK_OUT2
NC_NUB_SWD_TMS2
NC_NUB_SWD_TMS3
SWD_NUB_ATCRTMR01_SWCLK_R
SWD_NUB_ATCRTMR01_SWDIO_R
SWD_NUB_ATCRTMR2_SWCLK_R
SWD_NUB_ATCRTMR2_SWDIO_R
SWD_NUB_IPD_SWCLK_R
SWD_NUB_IPD_SWDIO_R
SWD_SOC_SWCLK_R
SWD_SOC_SWDIO_R
SOC_JTAG_TDI
SOC_JTAG_TDO
TPT_JTAG_SOC_TRST_L
SOC_JTAG_SEL
NC_JTAG_SLV_TCK
NC_JTAG_SLV_TMS
NC_JTAG_SLV_TDI
NC_JTAG_SLV_TDO
NC_JTAG_SLV_TRSTN
BOM_COST_GROUP=SOC
PAGE TITLE
SOC: AOP, SMC, NUB
Apple Inc.
DRAWING NUMBER 051-08286
SIZE D
REVISION 5.0.3
BRANCH
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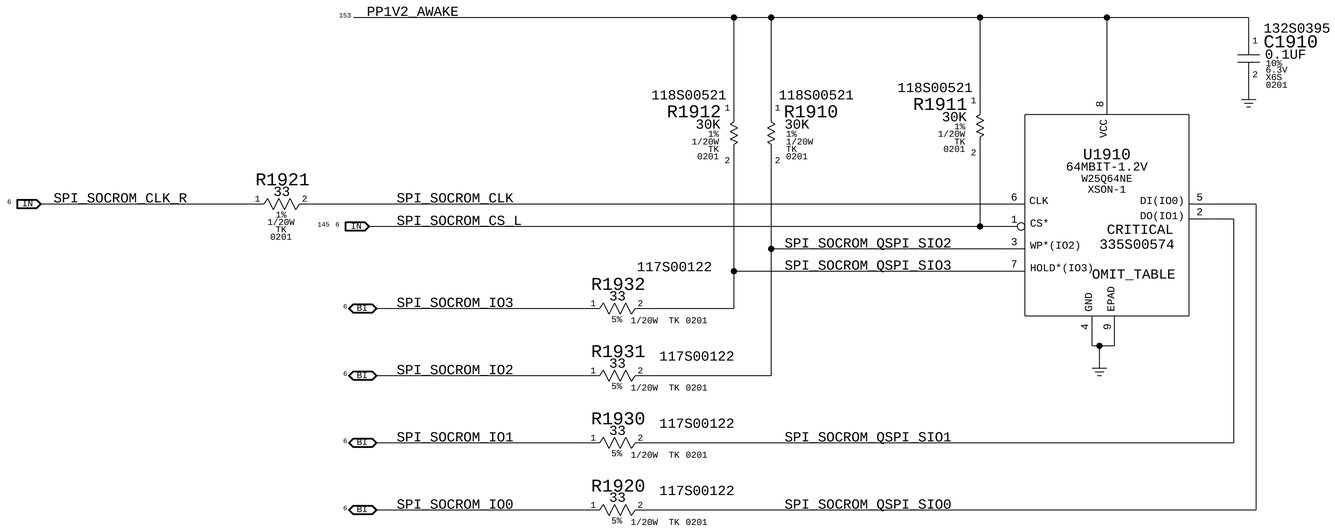
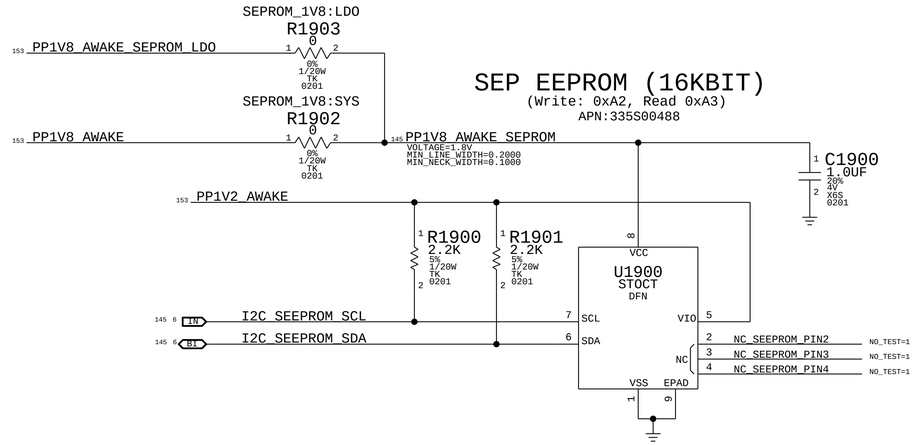
SPI NOR



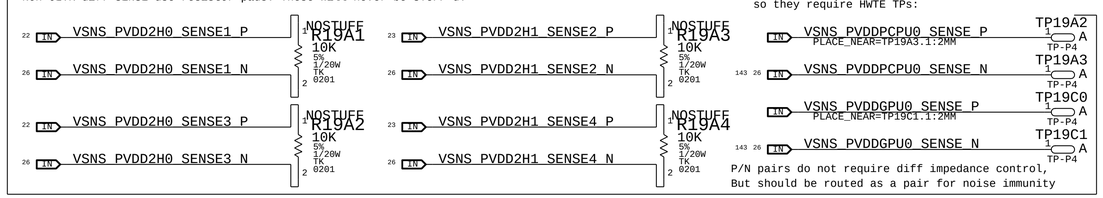


VDD/VSS SENSE BREAKOUT PADS

All SOC/DRAM VSNS traces to attempt to be 50ohm SE-impedance
45ohm SE-impedance will work but may impact measurement accuracy

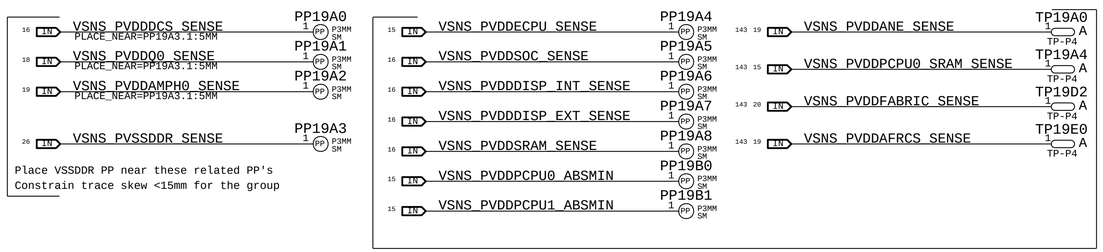
Non-CLVR SENSE points are only for debug/characterization access

Non-CLVR diff SENSE use resistor pads. These will never be STUFF'd:



CLVR rail SENSE points are used in Factory
in place of fixture probe access on PP* net,
so they require HWTE TPs:

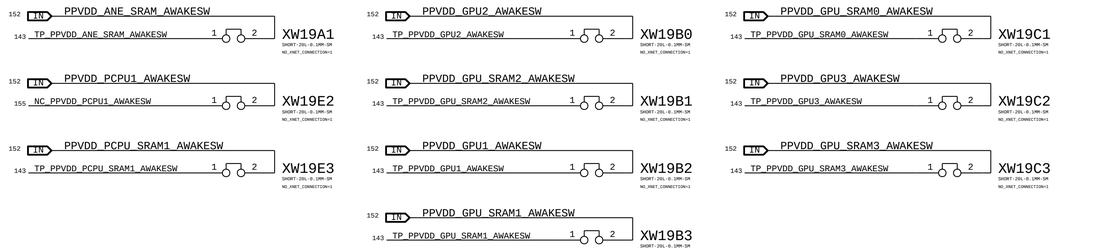
P/N pairs do not require diff impedance control,
But should be routed as a pair for noise immunity



Place VSSDDR PP near these related PP's
Constrain trace skew <15mm for the group

HWTE access to CLVR outputs

TP20** SENSE TPs can be used in place of output nets. Below are the CLVR outputs that don't have a SENSE TP
Place XWs under CLVRs, to breakout to HWTE-accessible test vias
TP_PPVDD nets require special spacing constraints to all nets except GND



BOM_COST_GROUP=SOC

PAGE TITLE
SOC: QSPI ROM, SEP ROM, VSNS

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SPMI SERIES TERMINATION

10 IN	SPMI_UPC015_CLK_R	R2070	20	PLACE_NEAR=U0600:25MM	SPMI_UPC015_CLK	R2071	33	PLACE_NEAR=UE400:25MM	SPMI_UPC0_CLK	OUT	155
						R2072	33	PLACE_NEAR=UE500:25MM	SPMI_UPC1_CLK	OUT	155
						R2073	33	PLACE_NEAR=U5500:25MM	SPMI_UPC5_CLK	OUT	144 155
10 BI	SPMI_UPC015_DATA_R	R2074	20	PLACE_NEAR=U0600:25MM	SPMI_UPC015_DATA	R2075	33	PLACE_NEAR=UE400:25MM	SPMI_UPC0_DATA	BI	155
						R2076	33	PLACE_NEAR=UE500:25MM	SPMI_UPC1_DATA	BI	155
						R2077	33	PLACE_NEAR=U5500:25MM	SPMI_UPC5_DATA	BI	144 155
10 IN	SPMI_UPC2_CLK_R	R2078	20	PLACE_NEAR=U0600:25MM	SPMI_UPC2_CLK_R2	R2016	20	PLACE_NEAR=UG400:25MM	SPMI_UPC2_CLK	OUT	155
10 BI	SPMI_UPC2_DATA_R	R2079	20	PLACE_NEAR=U0600:25MM	SPMI_UPC2_DATA_R2	R2017	20	PLACE_NEAR=UG400:25MM	SPMI_UPC2_DATA	BI	155
10 IN	SPMI_LPMU_CLK_R	R2008	33	PLACE_NEAR=U0600:25MM					SPMI_LPMU_CLK	OUT	46
10 BI	SPMI_LPMU_DATA_R	R2009	33	PLACE_NEAR=U0600:25MM					SPMI_LPMU_DATA	BI	46
		C2009 10PF 5% 25V C0G 0201 PLACE_NEAR=U0600:25MM									
10 IN	SPMI_FPMU_VDDHVR_CLK_R	R2014	20	PLACE_NEAR=U0600:25MM	SPMI_FPMU_VDDHVR_CLK	R2010	49.9	PLACE_NEAR=U7700:25MM	SPMI_FPMU_CLK	OUT	42
						R2011	49.9	PLACE_NEAR=U9300:25MM	SPMI_VDDHVR_CLK	OUT	50 145
10 BI	SPMI_FPMU_VDDHVR_DATA_R	R2015	20	PLACE_NEAR=U0600:25MM	SPMI_FPMU_VDDHVR_DATA	R2012	49.9	PLACE_NEAR=U7700:25MM	SPMI_FPMU_DATA	BI	42
						R2013	49.9	PLACE_NEAR=U9300:25MM	SPMI_VDDHVR_DATA	BI	50 145
10 IN	SPMI_CLVR14_CLK							MAKE_BASE=TRUE	SPMI_CLVR14_CLK		
									SPMI_CLVR14_CLK	OUT	57
									SPMI_CLVR14_CLK	OUT	60
10 BI	SPMI_CLVR14_DATA							MAKE_BASE=TRUE	SPMI_CLVR14_DATA		
									SPMI_CLVR14_DATA	BI	57
									SPMI_CLVR14_DATA	BI	60
10 IN	SPMI_CLVR23_CLK							MAKE_BASE=TRUE	SPMI_CLVR23_CLK		
									SPMI_CLVR23_CLK	OUT	58
									SPMI_CLVR23_CLK	OUT	59
10 BI	SPMI_CLVR23_DATA							MAKE_BASE=TRUE	SPMI_CLVR23_DATA		
									SPMI_CLVR23_DATA	BI	58
									SPMI_CLVR23_DATA	BI	59
10 IN	SPMI_CLVR0_CLK							MAKE_BASE=TRUE	SPMI_CLVR0_CLK	OUT	56
10 BI	SPMI_CLVR0_DATA							MAKE_BASE=TRUE	SPMI_CLVR0_DATA	BI	56
10 IN	SPMI_WLBT_CLK_R	R2068	33						SPMI_WLBT_CLK	OUT	110
10 BI	SPMI_WLBT_DATA_R	R2069	33						SPMI_WLBT_DATA	BI	110
10 IN	SPMI_SE_CLK_R	R2000	33						SPMI_SE_CLK	OUT	27
10 BI	SPMI_SE_DATA_R	R2001	33						SPMI_SE_DATA	BI	27

NAND PCIE CLK SHARING

8 IN	PCIE_CLK100M_NAND0_0_1_P	MAKE_BASE=TRUE	PCIE_CLK100M_NAND0_0_1_P OUT 112 122
			PCIE_CLK100M_NAND0_0_1_P OUT 113
8 IN	PCIE_CLK100M_NAND0_0_1_N	MAKE_BASE=TRUE	PCIE_CLK100M_NAND0_0_1_N OUT 112 122
			PCIE_CLK100M_NAND0_0_1_N OUT 113
8 IN	PCIE_CLK100M_NAND0_2_3_P	MAKE_BASE=TRUE	PCIE_CLK100M_NAND0_2_3_P OUT 114 122
			PCIE_CLK100M_NAND0_2_3_P OUT 115
8 IN	PCIE_CLK100M_NAND0_2_3_N	MAKE_BASE=TRUE	PCIE_CLK100M_NAND0_2_3_N OUT 114 122
			PCIE_CLK100M_NAND0_2_3_N OUT 115
8 IN	PCIE_CLK100M_NAND1_0_1_P	MAKE_BASE=TRUE	PCIE_CLK100M_NAND1_0_1_P OUT 117 122
			PCIE_CLK100M_NAND1_0_1_P OUT 118
8 IN	PCIE_CLK100M_NAND1_0_1_N	MAKE_BASE=TRUE	PCIE_CLK100M_NAND1_0_1_N OUT 117 122
			PCIE_CLK100M_NAND1_0_1_N OUT 118
8 IN	PCIE_CLK100M_NAND1_2_3_P	MAKE_BASE=TRUE	PCIE_CLK100M_NAND1_2_3_P OUT 119 122
			PCIE_CLK100M_NAND1_2_3_P OUT 120
8 IN	PCIE_CLK100M_NAND1_2_3_N	MAKE_BASE=TRUE	PCIE_CLK100M_NAND1_2_3_N OUT 119 122
			PCIE_CLK100M_NAND1_2_3_N OUT 120

SWD SERIES TERMINATION

5 IN	SWD_NAND0_SWCLK_R	R2032	15	PLACE_NEAR=U0600:25MM	SWD_NAND0_SWCLK	R2082	49.9		SWD_NAND0_S5E0_S5E1_SWCLK	OUT	154
					SSD_BRANCH_2L	R2083	49.9		SWD_NAND0_S5E2_S5E3_SWCLK	OUT	154
5 BI	SWD_NAND0_SWDIO_R	R2033	15	PLACE_NEAR=U0600:25MM	SWD_NAND0_SWDIO	R2084	49.9		SWD_NAND0_S5E0_S5E1_SWDIO	BI	154
	SSD_BRANCH_2L				SSD_BRANCH_2L	R2085	49.9		SWD_NAND0_S5E2_S5E3_SWDIO	BI	154
5 IN	SWD_NAND1_SWCLK_R	R2034	15	PLACE_NEAR=U0600:25MM	SWD_NAND1_SWCLK	R2086	49.9		SWD_NAND1_S5E0_S5E1_SWCLK	OUT	154
	SSD_BRANCH_2L				SSD_BRANCH_2L	R2087	49.9		SWD_NAND1_S5E2_S5E3_SWCLK	OUT	154
5 BI	SWD_NAND1_SWDIO_R	R2035	15	PLACE_NEAR=U0600:25MM	SWD_NAND1_SWDIO	R2088	49.9		SWD_NAND1_S5E0_S5E1_SWDIO	BI	154
					SSD_BRANCH_2L	R2089	49.9		SWD_NAND1_S5E2_S5E3_SWDIO	BI	154
10 IN	SWD_NUB_PMU_VDDHVR_CLVR0_SWCLK_R	R2036	15	PLACE_NEAR=U0600:25MM	SWD_NUB_PMU_VDDHVR_CLVR0_SWCLK	R2040	49.9	PLACE_NEAR=U8100:25MM	SWD_LPMU_SWCLK	OUT	46
						R2042	49.9	PLACE_NEAR=U7700:25MM	SWD_FPMU_SWCLK	OUT	42
						R2030	49.9	PLACE_NEAR=U9300:25MM	SWD_VDDHVR_SWCLK	OUT	50
						R2090	49.9	PLACE_NEAR=UA100:25MM	SWD_CLVR0_SWCLK	OUT	56
10 BI	SWD_NUB_PMU_VDDHVR_CLVR0_SWDIO_R	R2037	15	PLACE_NEAR=U0600:25MM	SWD_NUB_PMU_VDDHVR_CLVR0_SWDIO	R2041	49.9	PLACE_NEAR=U8100:25MM	SWD_LPMU_SWDIO	BI	46
						R2043	49.9	PLACE_NEAR=U7700:25MM	SWD_FPMU_SWDIO	OUT	42
						R2031	49.9	PLACE_NEAR=U9300:25MM	SWD_VDDHVR_SWDIO	OUT	50
						R2092	49.9	PLACE_NEAR=UA100:25MM	SWD_CLVR0_SWDIO	BI	56
10 IN	SWD_NUB_CLVR1234_SWCLK_R	R2044	15	PLACE_NEAR=U0600:25MM	SWD_NUB_CLVR1234_SWCLK	R2091	49.9	PLACE_NEAR=UA200:25MM	SWD_CLVR1_SWCLK	OUT	57
						R2094	49.9	PLACE_NEAR=UA300:25MM	SWD_CLVR2_SWCLK	OUT	58
						R2096	49.9	PLACE_NEAR=UA400:25MM	SWD_CLVR3_SWCLK	OUT	59
						R2097	49.9	PLACE_NEAR=UA500:25MM	SWD_CLVR4_SWCLK	OUT	60
10 BI	SWD_NUB_CLVR1234_SWDIO_R	R2045	15	PLACE_NEAR=U0600:25MM	SWD_NUB_CLVR1234_SWDIO	R2093	49.9	PLACE_NEAR=UA200:25MM	SWD_CLVR1_SWDIO	BI	57
						R2095	49.9	PLACE_NEAR=UA300:25MM	SWD_CLVR2_SWDIO	BI	58
						R2098	49.9	PLACE_NEAR=UA400:25MM	SWD_CLVR3_SWDIO	BI	59
						R2099	49.9	PLACE_NEAR=UA500:25MM	SWD_CLVR4_SWDIO	BI	60
10 OUT	SWD_SOC_SWCLK_R					R2038	0		SWD_SOC_SWCLK	IN	83 143 144
10 BI	SWD_SOC_SWDIO_R					R2039	0		SWD_SOC_SWDIO	BI	83 143 144
6 IN	SWD_UPC_SWCLK_R	R2050	20	SWD_UPC_SWCLK	R2046	49.9		SWD_UPC_SWCLK015	R2051	20	SWD_UPC_SWCLK0	MAKE_BASE=TRUE	SWD_UPC_SWCLK0 OUT 84 155
									R2052	20	SWD_UPC_SWCLK1	MAKE_BASE=TRUE	SWD_UPC_SWCLK1 OUT 85
									R2053	49.9	SWD_UPC_SWCLK5	MAKE_BASE=TRUE	SWD_UPC_SWCLK5 OUT 32 33
					R2060	20	SWD_UPC_SWCLK2					MAKE_BASE=TRUE	SWD_UPC_SWCLK2 OUT 93 155
6 BI	SWD_UPC_SWDIO_R	R2054	20	SWD_UPC_SWDIO	R2055	49.9		SWD_UPC_SWDIO015	R2047	20	SWD_UPC_SWDIO0	MAKE_BASE=TRUE	SWD_UPC_SWDIO0 BI 84 155
									R2049	20	SWD_UPC_SWDIO1	MAKE_BASE=TRUE	SWD_UPC_SWDIO1 BI 85
									R2056	49.9	SWD_UPC_SWDIO5	MAKE_BASE=TRUE	SWD_UPC_SWDIO5 BI 32 33
					R2048	20	SWD_UPC_SWDIO2					MAKE_BASE=TRUE	SWD_UPC_SWDIO2 BI 93 155
10 IN	SWD_NUB_ATCRTMR01_SWCLK_R					R2061	49.9		SWD_NUB_ATCRTMR01_SWCLK	OUT	145 156
10 BI	SWD_NUB_ATCRTMR01_SWDIO_R					R2062	49.9		SWD_NUB_ATCRTMR01_SWDIO	BI	156
10 IN	SWD_NUB_ATCRTMR2_SWCLK_R					R2063	49.9		SWD_NUB_ATCRTMR2_SWCLK	OUT	156
10 BI	SWD_NUB_ATCRTMR2_SWDIO_R					R2064	49.9		SWD_NUB_ATCRTMR2_SWDIO	BI	156
10 IN	SWD_NUB_IPD_SWCLK_R					R2065	0		SWD_IPD_CLK_R	OUT	156
10 BI	SWD_NUB_IPD_SWDIO_R					R2066	0		SWD_IPD_DATA_R	BI	156

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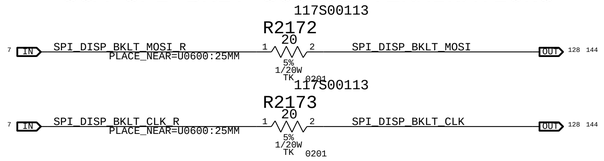
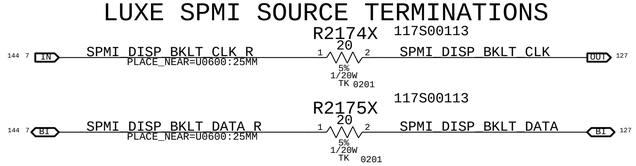
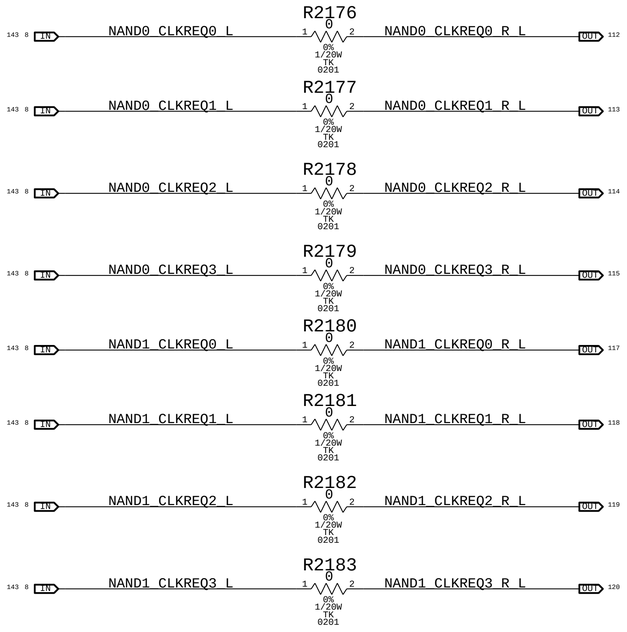
SGA SPI BKLT SOURCE TERMINATIONS



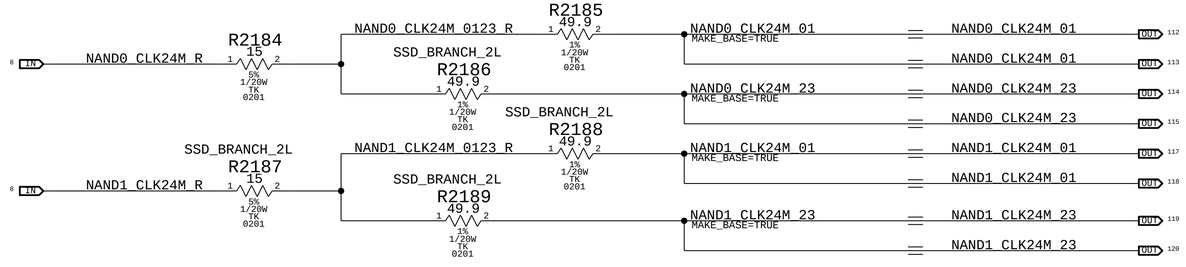
LUXE SPMI SOURCE TERMINATIONS



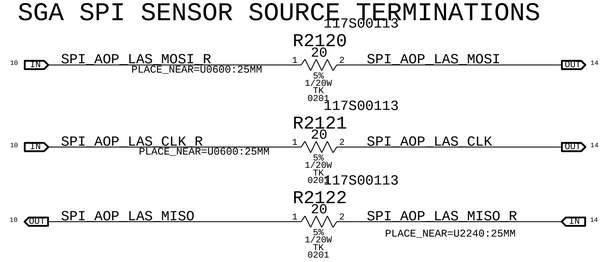
NAND CLKREQ SERIES RESISTORS



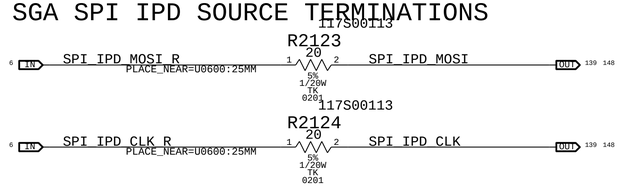
SSD 24M CLOCK TERMINATIONS



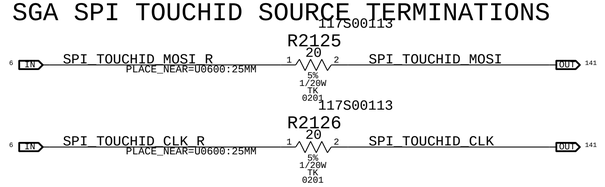
SGA SPI SENSOR SOURCE TERMINATIONS



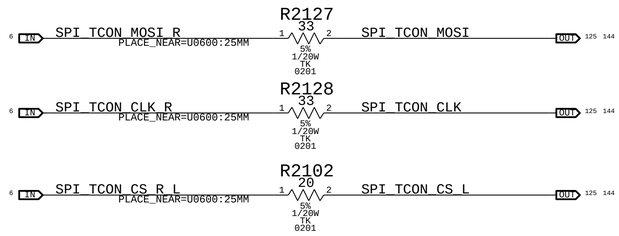
SGA SPI IPD SOURCE TERMINATIONS



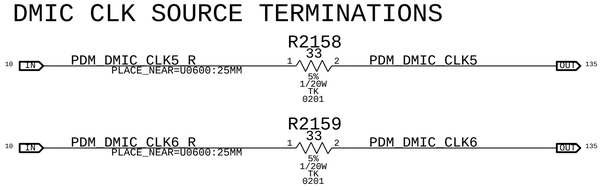
SGA SPI TOUCHID SOURCE TERMINATIONS



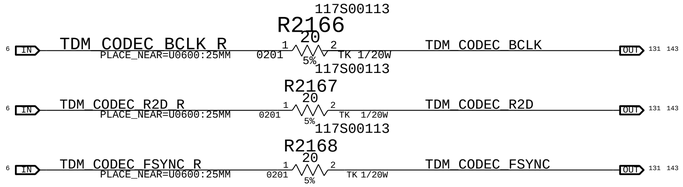
SGA SPI TCON SOURCE TERMINATIONS



DMIC CLK SOURCE TERMINATIONS



SGA TDM SOURCE TERMINATIONS



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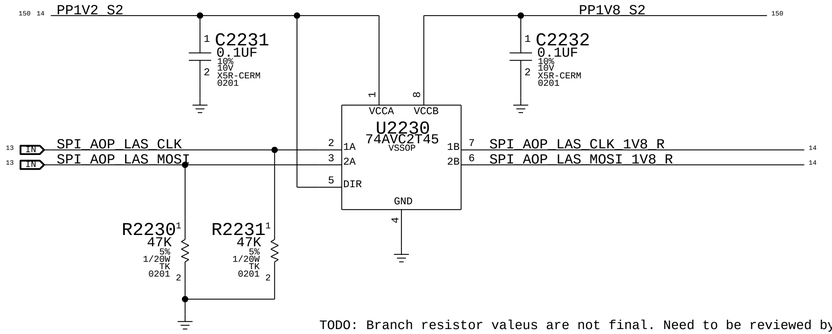
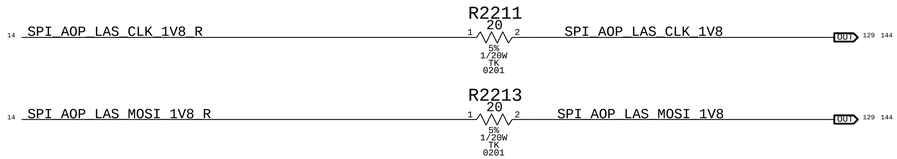
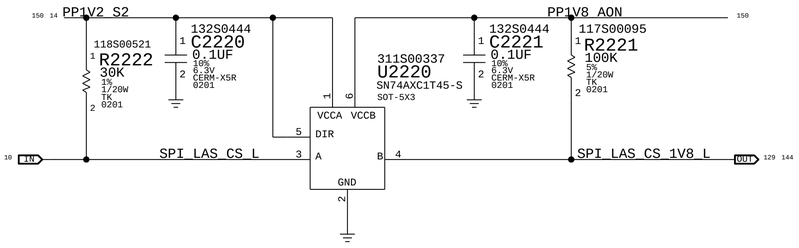
SPI AOP Sensor LS and Branch Resistors

TODO: Reference designators need to be updated once layout has imported latest netlist

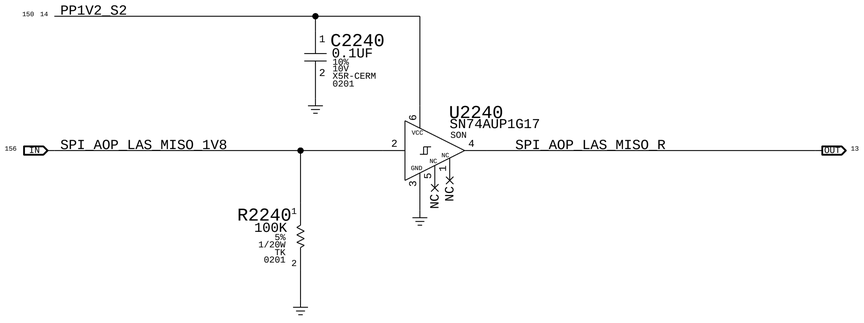


TODO: Branch resistor valeus are not final. Need to be reviewed by SI once routed

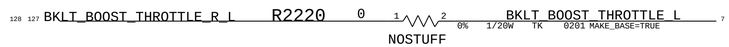




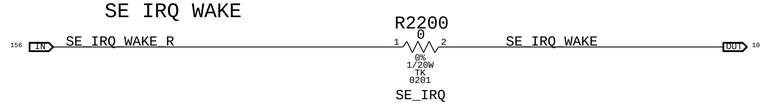
SPI LEVEL TRANSLATION



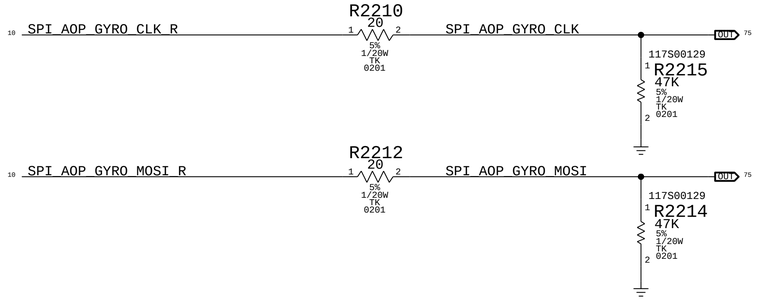
DISPLAY BACKLIGHT



SE IRQ WAKE



KEEP STUFFED UNTIL POR SE IS BROUGHT UP WITHOUT IRQ



BOM_COST_GROUP=SOC

PAGE TITLE: SOC: SHARED SUPPORT 3

Apple Inc.

DRAWING NUMBER: 051-08286 SIZE: D

REVISION: 5.0.3

BRANCH:

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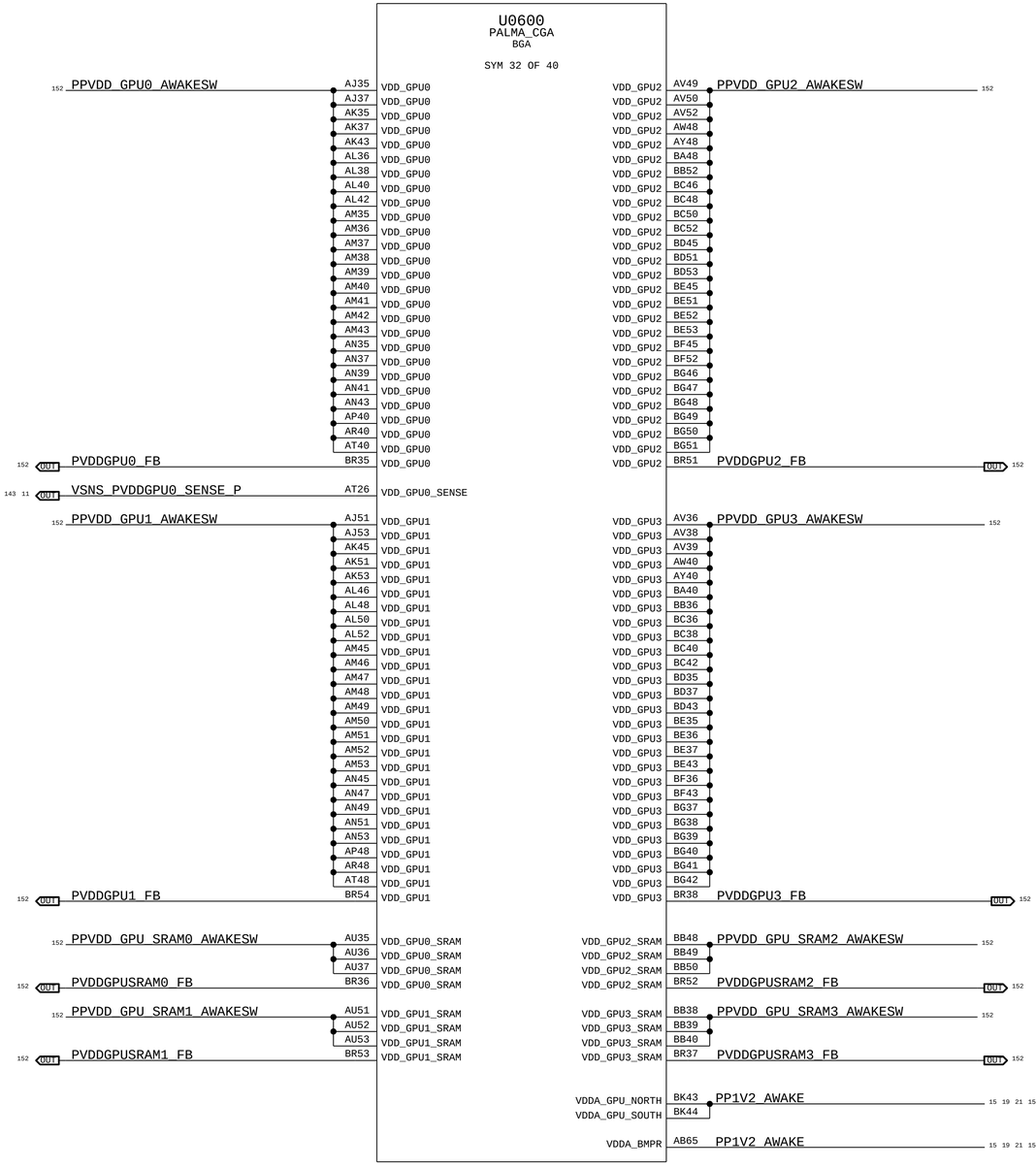

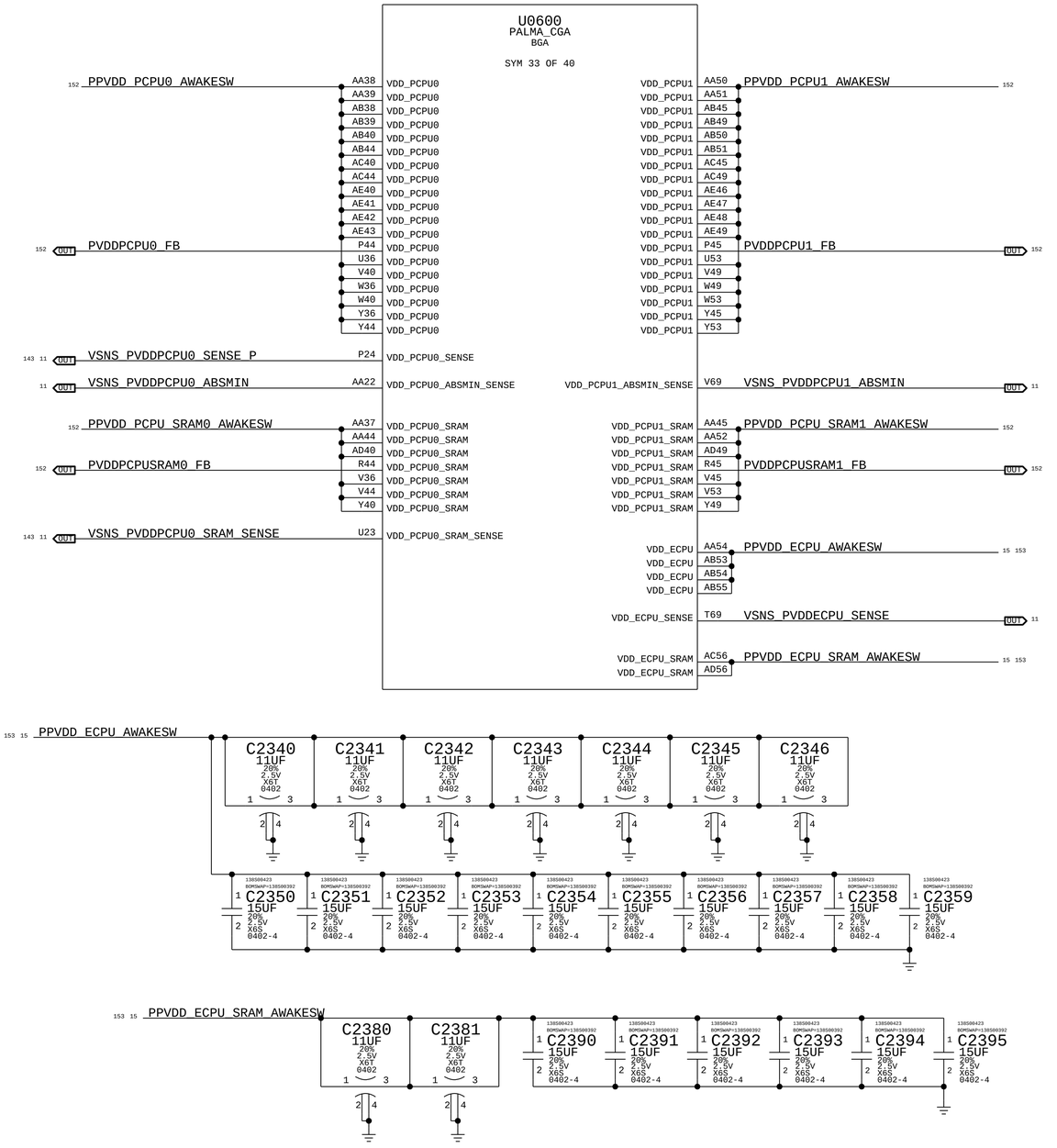

BOM_COST_GROUP=SOC

PAGE TITLE
SOC: POWER (CPU, GPU)

Apple Inc.

DRAWING NUMBER 051-08286
SIZE D
REVISION 5.0.3
BRANCH
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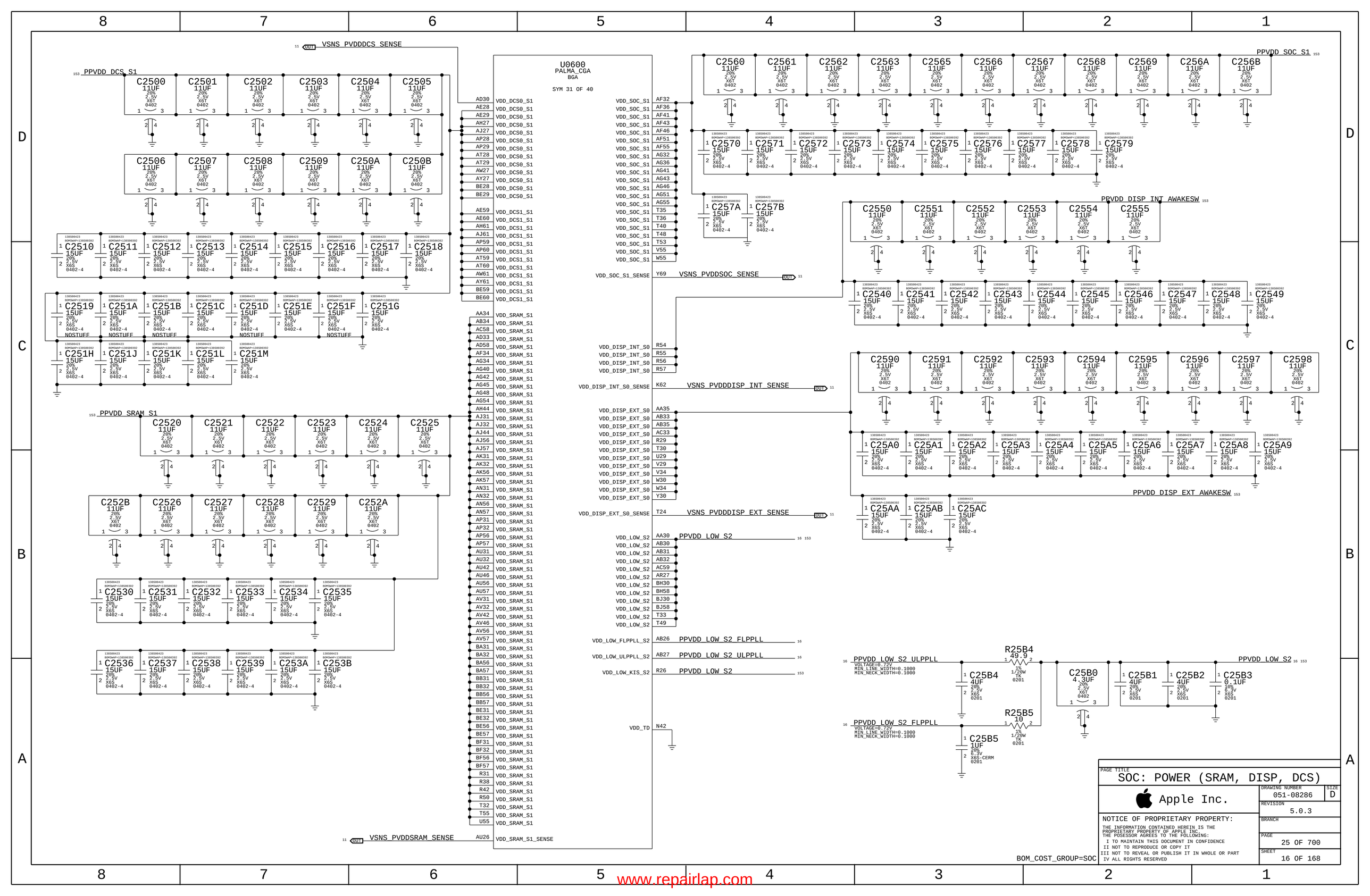
VSNS_PVDDDCS_SENSE
PPVDD_DCS_S1
PPVDD_SRAM_S1
U0600
PALMA_CGA
BGA
SYM 31 OF 40
VDD_DCS0_S1
VDD_DCS1_S1
VDD_SRAM_S1
VDD_SRAM_S1_SENSE
VSNS_PVDDSRAM_SENSE
VDD_SOC_S1
VDD_SOC_S1_SENSE
VSNS_PVDDSOC_SENSE
PPVDD_SOC_S1
PPVDD_DISP_INT_AWAKESW
VDD_DISP_INT_S0
VDD_DISP_INT_S0_SENSE
VSNS_PVDDDISP_INT_SENSE
VDD_DISP_EXT_S0
VDD_DISP_EXT_S0_SENSE
VSNS_PVDDDISP_EXT_SENSE
PPVDD_DISP_EXT_AWAKESW
VDD_LOW_S2
PPVDD_LOW_S2
VDD_LOW_FLPPLL_S2
PPVDD_LOW_S2_FLPPLL
VDD_LOW_ULPPLL_S2
PPVDD_LOW_S2_ULPPLL
VDD_LOW_KIS_S2
VDD_TD
R25B4 49.9
R25B5 10
C25B0 4.3UF
C25B1 4UF
C25B2 4UF
C25B3 0.1UF
C25B4 4UF
C25B5 1UF
BOM_COST_GROUP=SOC
PAGE TITLE
SOC: POWER (SRAM, DISP, DCS)
Apple Inc.
DRAWING NUMBER
051-08286
SIZE
D
REVISION
5.0.3
BRANCH
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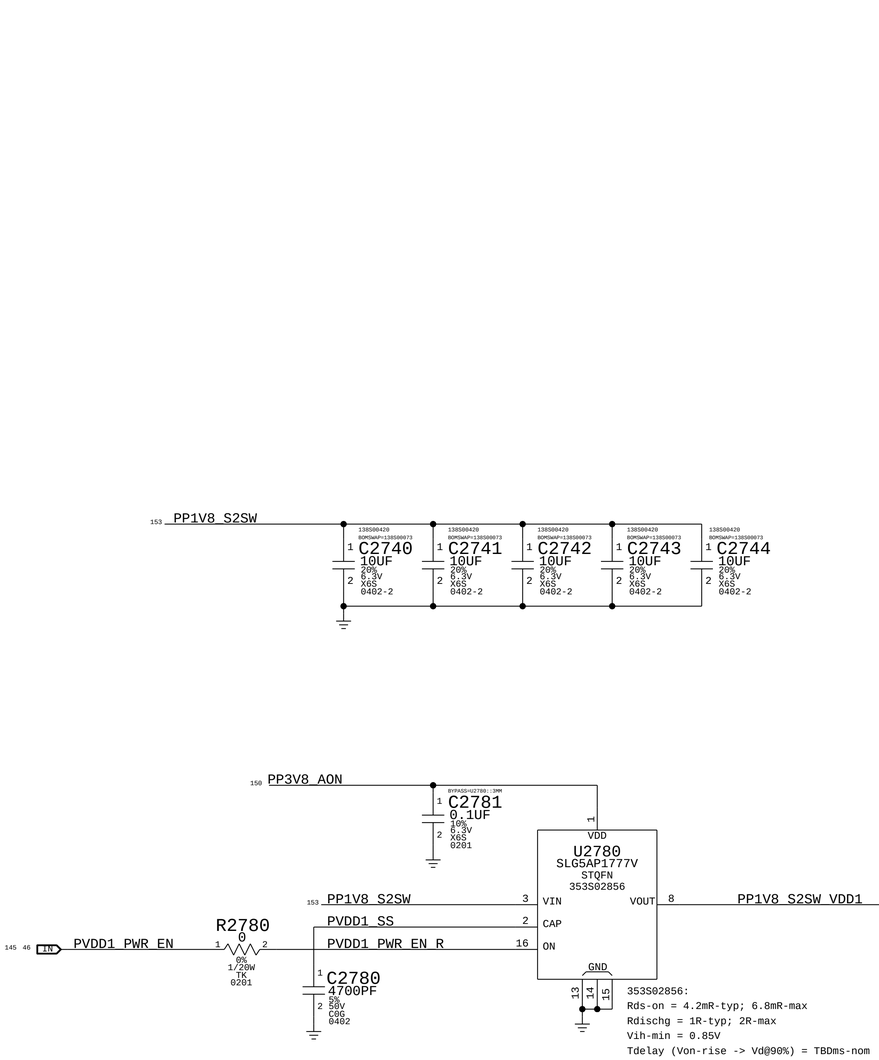

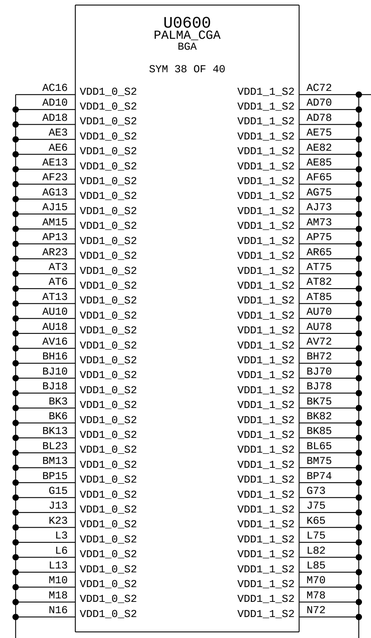

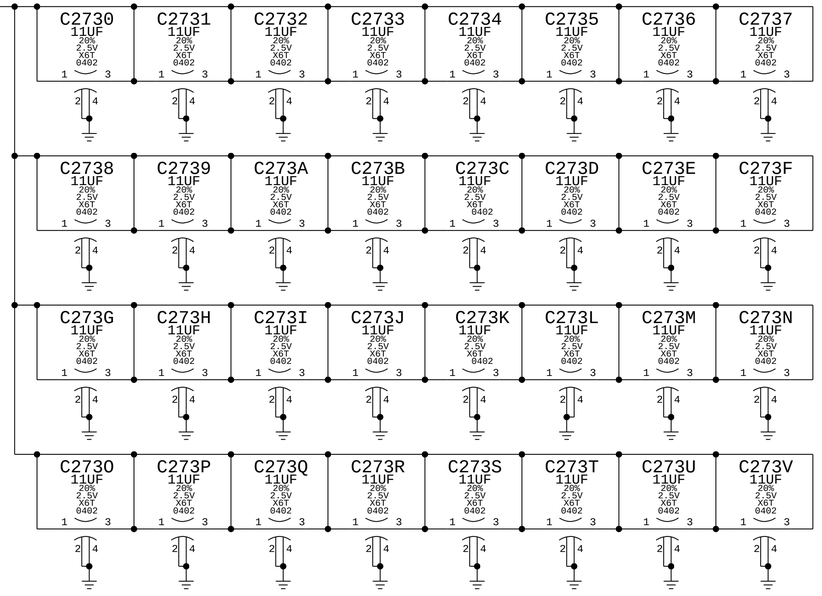

BOM_COST_GROUP=SOC

PAGE TITLE
SOC: POWER (VDD1)

Apple Inc.

DRAWING NUMBER 051-08286
SIZE D
REVISION 5.0.3
BRANCH
PAGE 27 OF 700
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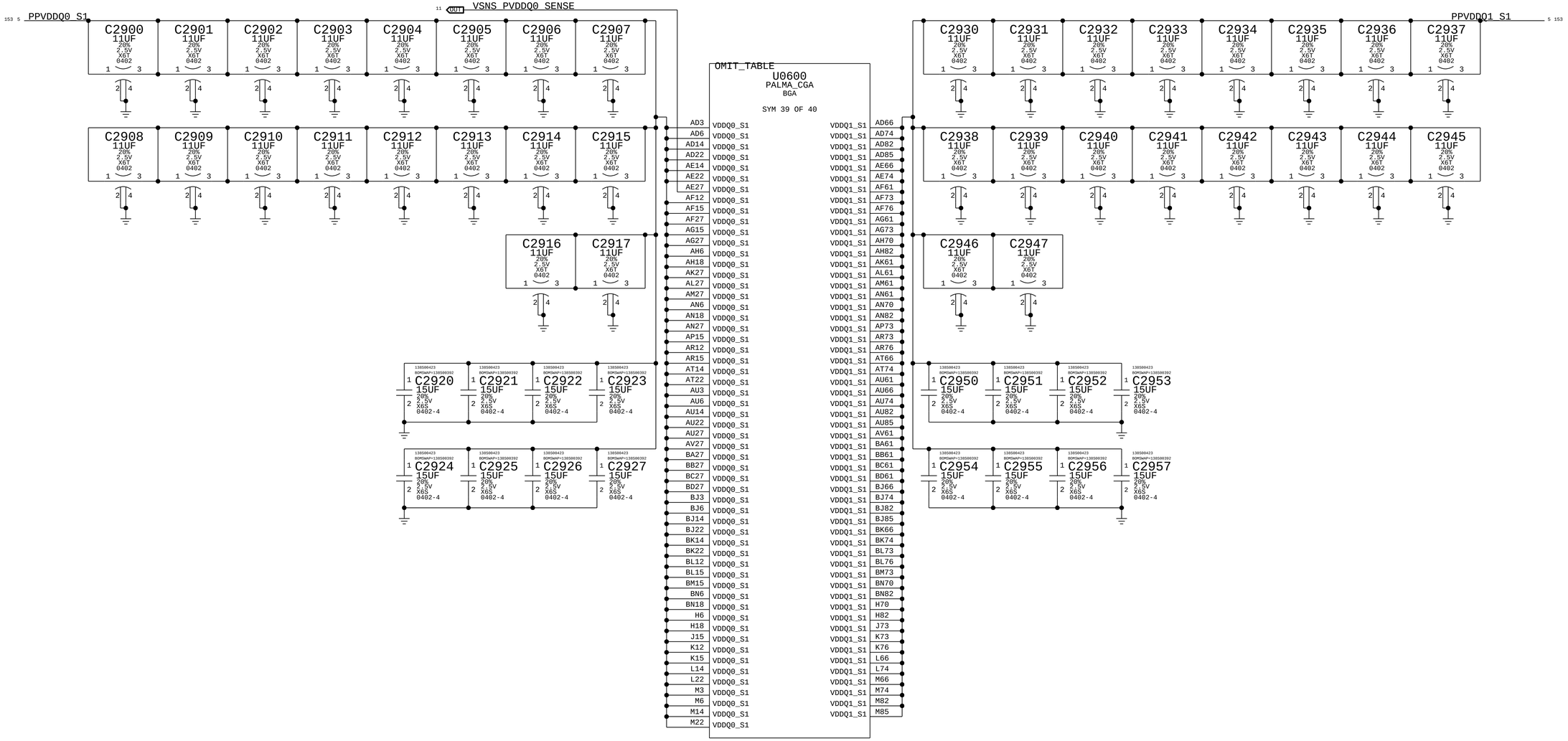

PAGE TITLE
SOC: POWER (VDDQ)

Apple Inc.

DRAWING NUMBER 051-08286
SIZE D
REVISION 5.0.3
BRANCH
PAGE 29 OF 700
SHEET 18 OF 168

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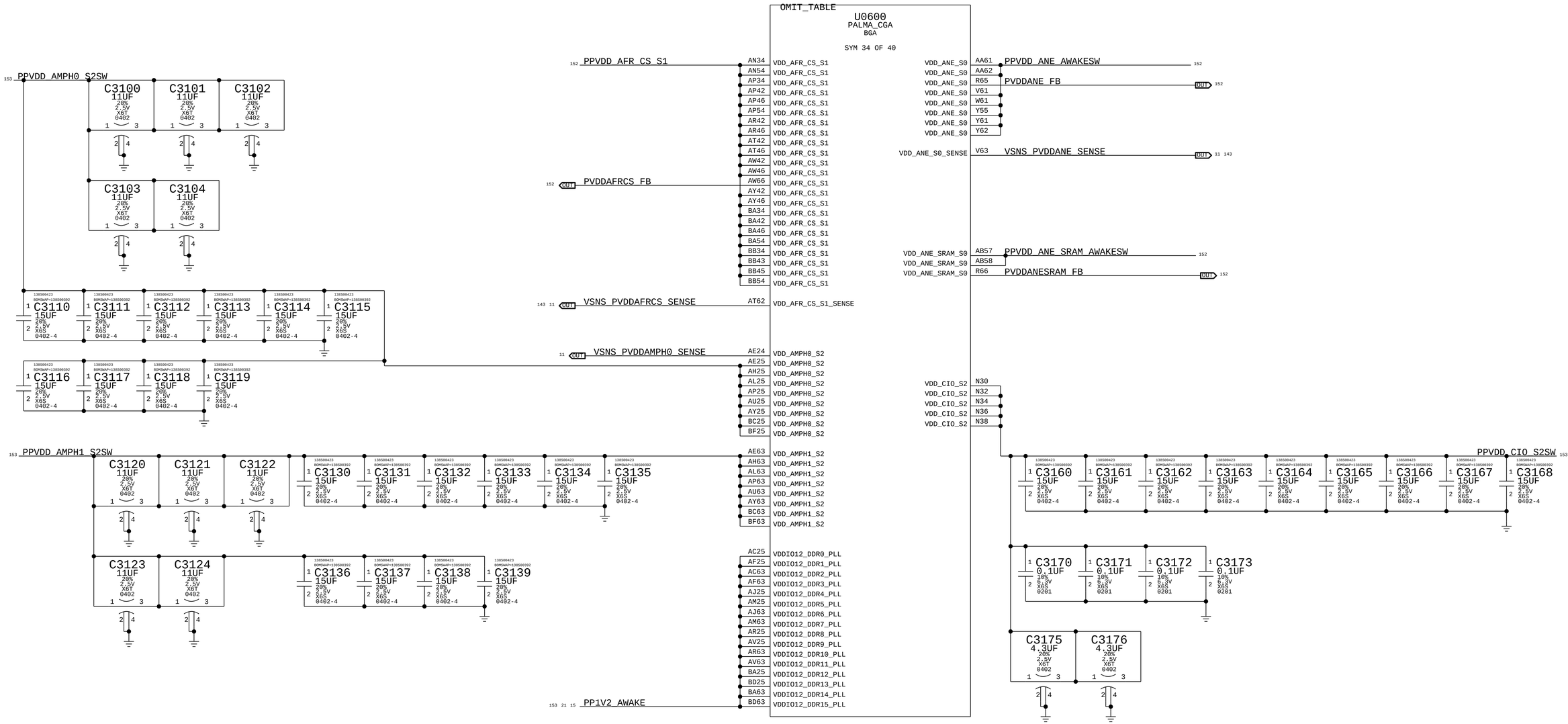

BOM_COST_GROUP=SOC

PAGE TITLE: SOC: POWER (AFR, ANE, CIO)

Apple Inc.

DRAWING NUMBER: 051-08286 | SIZE: D

REVISION: 5.0.3

BRANCH:

PAGE: 31 OF 700

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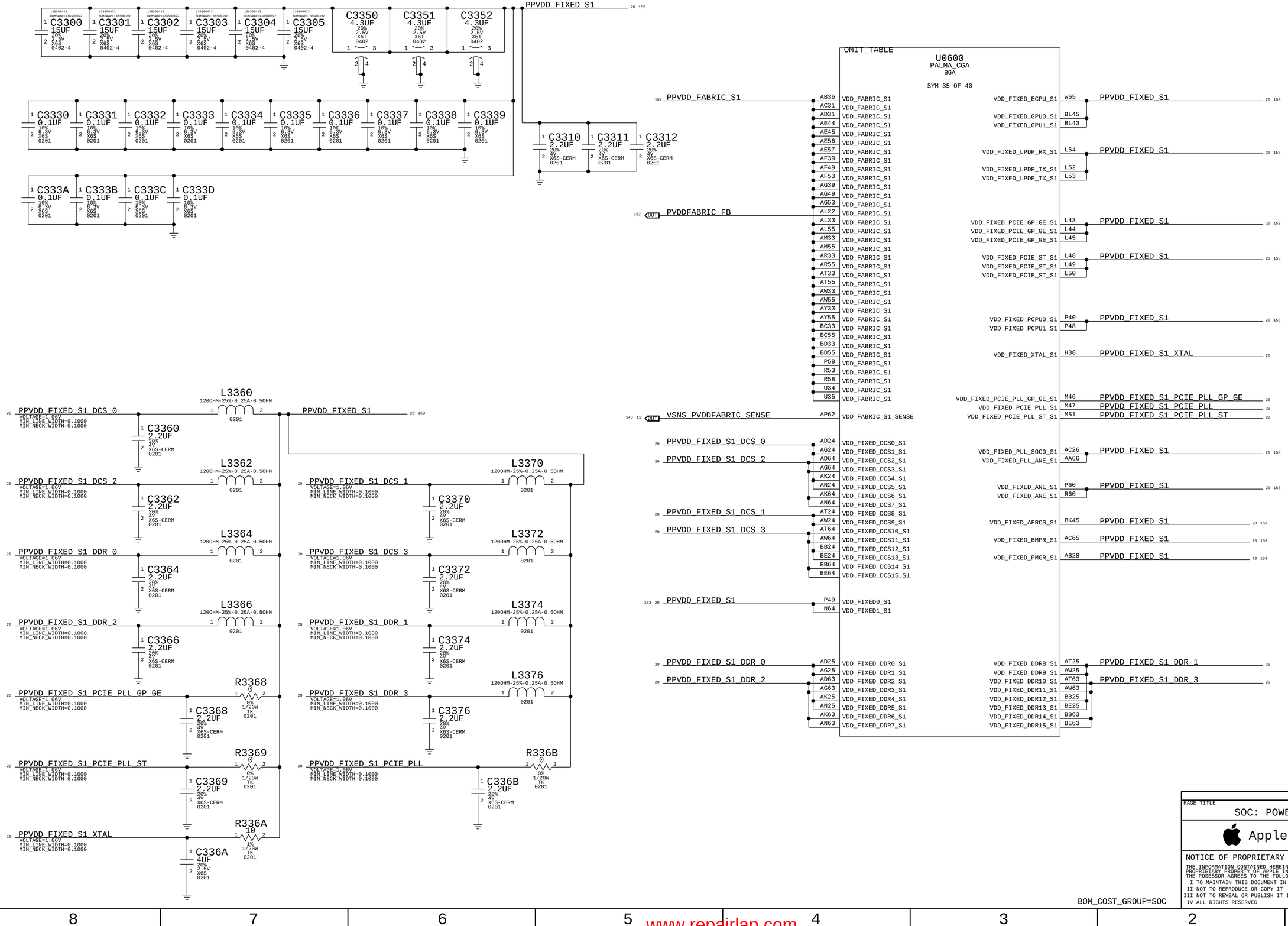

PAGE TITLE

SOC: POWER (FABRIC, FIXED)

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DRAWING NUMBER 051-08286

SIZE D

REVISION 5.0.3

BRANCH

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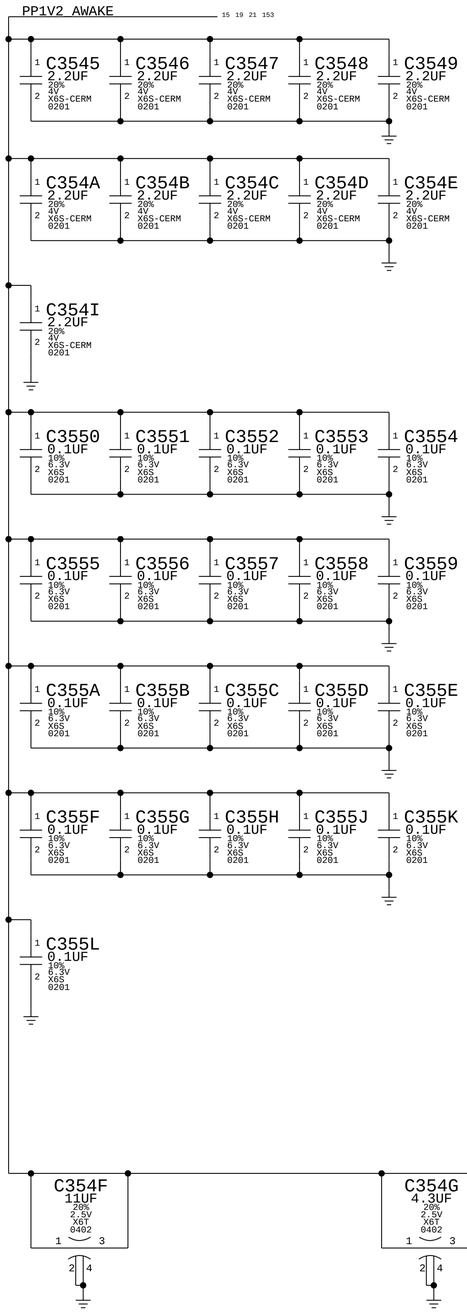

OMIT_TABLE

U0600
PALMA_CGA
BGA

SYM 40 OF 40

PP1V2_S2_AOP0_S2	AA28	VDDIO12_AOP0_S2
	W28	VDDIO12_AOP0_S2
	Y28	VDDIO12_AOP0_S2
PP1V2_S2_AOP1_S2	T28	VDDIO12_AOP1_S2
	U28	VDDIO12_AOP1_S2
	V28	VDDIO12_AOP1_S2
PP1V2_S2	L30	VDDIO12_CIO_S2
	L32	VDDIO12_CIO_S2
	L34	VDDIO12_CIO_S2
	M29	VDDIO12_CIO_S2
	M31	VDDIO12_CIO_S2
	M33	VDDIO12_CIO_S2
	M35	VDDIO12_CIO_S2
PP1V2_AWAKE	AC24	VDDIO12_DCS0_PLL
	AF24	VDDIO12_DCS1_PLL
	AC64	VDDIO12_DCS2_PLL
	AF64	VDDIO12_DCS3_PLL
	AJ24	VDDIO12_DCS4_PLL
	AM24	VDDIO12_DCS5_PLL
	AJ64	VDDIO12_DCS6_PLL
	AM64	VDDIO12_DCS7_PLL
	AR24	VDDIO12_DCS8_PLL
	AV24	VDDIO12_DCS9_PLL
	AR64	VDDIO12_DCS10_PLL
	AV64	VDDIO12_DCS11_PLL
	BA24	VDDIO12_DCS12_PLL
	BD24	VDDIO12_DCS13_PLL
	BA64	VDDIO12_DCS14_PLL
	BD64	VDDIO12_DCS15_PLL
PP1V2_AWAKE_GRP0	M55	VDDIO12_GRP0
	M56	VDDIO12_GRP0
	M57	VDDIO12_GRP0
	M58	VDDIO12_GRP0
PP1V2_AWAKE_GRP1	P62	VDDIO12_GRP1
	R62	VDDIO12_GRP1
	T62	VDDIO12_GRP1
	U62	VDDIO12_GRP1
PP1V2_AWAKE_T2T	M41	VDDIO12_T2T

VDD12_AMUX0_S2	M42	PP1V2_S2
VDD12_AMUX1_S2	L64	
VDD18_EFUSE1	P42	
VDD18_EFUSE_SEP	U63	
VDD12_FMON	T64	PP1V2_AWAKE_FMON
VDD12_HSCDFT0	K37	PP1V2_S2
VDD12_HSCDFT1	N63	
VDD12_LPDP_RX	K54	PP1V2_AWAKE
VDD12_LPDP_TX	K52	
VDD12_LPDP_TX	K53	
VDD12_MTR1	Y64	PP1V2_AWAKE
VDD12_MTR2	Y22	
VDD12_MTR3	U65	
VDD12_MTR4	AA23	
VDD12_XTAL	H37	PP1V2_AWAKE_XTAL
VDD12_PCIE_GE_GP	K43	PP1V2_AWAKE
VDD12_PCIE_GE_GP	K44	
VDD12_PCIE_GE_GP	K45	
VDD12_PCIE_ST_S1	K48	PP1V2_AWAKE
VDD12_PCIE_ST_S1	K49	
VDD12_PCIE_ST_S1	K50	
VDD12_PCIE_PLL	L47	PP1V2_AWAKE_PCIE_PLL
VDD12_PLL_ANE	Y66	PP1V2_AWAKE
VDD12_PLL_PCPU0_AFX	AB21	
VDD12_PLL_PCPU1_ECPU_FAB	AA64	
VDD12_PLL_SOC0	AC27	
VDD12_TSADC_PCPU0_S2	AB23	PP1V2_S2
VDD12_TSADC_PCPU1_S2	W66	
VDD12_TSADC_ECPU_S2	W64	
VDD12_TSADC_SOC0	J37	PP1V2_AWAKE
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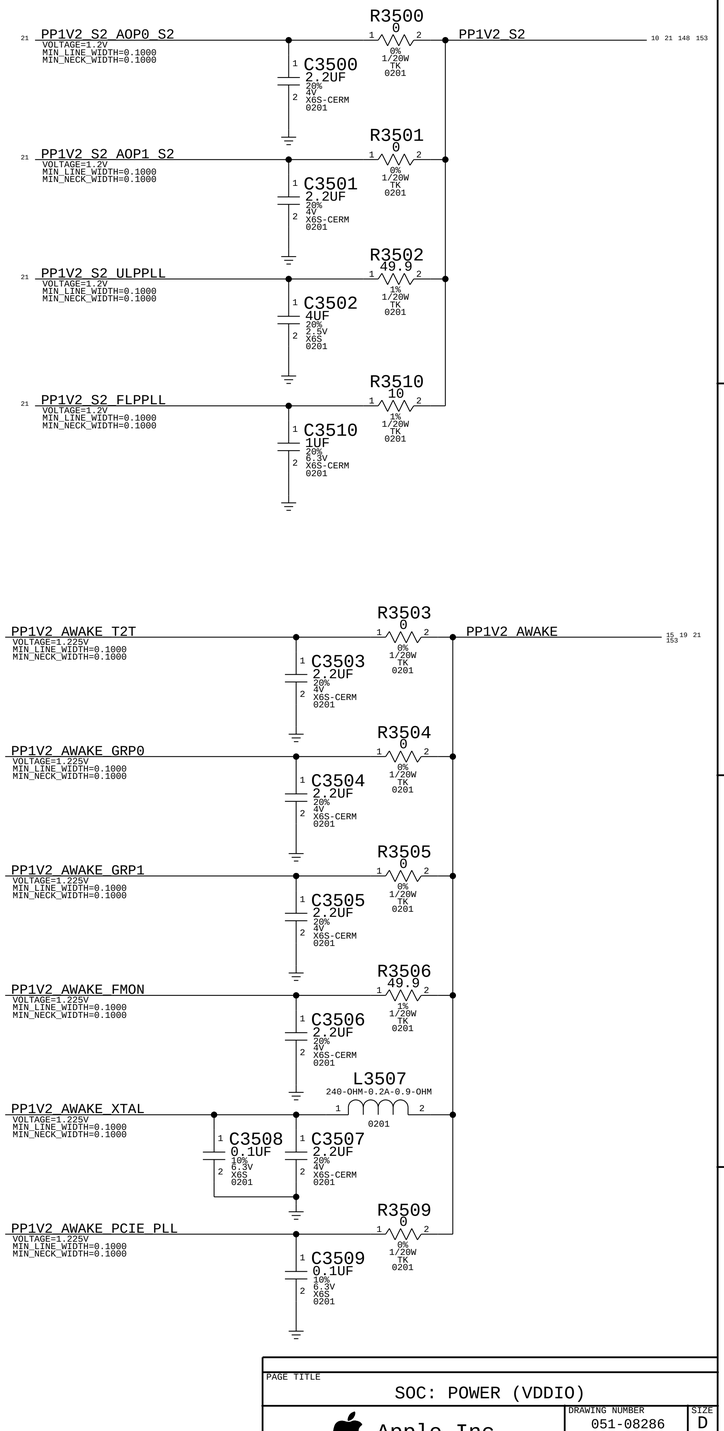
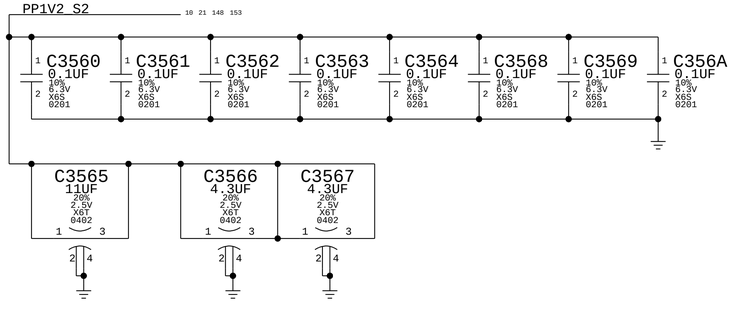
VDD12_ULPPLL_S2	Y25	PP1V2_S2_ULPPLL





BOM_COST_GROUP=SOC

PAGE TITLE
SOC: POWER (VDDIO)

Apple Inc.

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SIZE D
REVISION 5.0.3
BRANCH
PAGE 35 OF 700
SHEET 21 OF 168

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PPVDD2H0_S2SW 153

OMIT_TABLE

U0600
PALMA_CGA
BGA

SYM 36 OF 40

AD4	VDD2H0_S2	VDD2H0_S2	BL9
AD8	VDD2H0_S2	VDD2H0_S2	BL17
AD12	VDD2H0_S2	VDD2H0_S2	BL19
AD16	VDD2H0_S2	VDD2H0_S2	BL21
AD20	VDD2H0_S2	VDD2H0_S2	BM3
AE4	VDD2H0_S2	VDD2H0_S2	BM5
AE8	VDD2H0_S2	VDD2H0_S2	BM7
AE10	VDD2H0_S2	VDD2H0_S2	BM9
AE16	VDD2H0_S2	VDD2H0_S2	BM11
AE18	VDD2H0_S2	VDD2H0_S2	BM17
AE20	VDD2H0_S2	VDD2H0_S2	BM19
AF5	VDD2H0_S2	VDD2H0_S2	BM21
AF7	VDD2H0_S2	VDD2H0_S2	BN3
AF9	VDD2H0_S2	VDD2H0_S2	BN4
AF17	VDD2H0_S2	VDD2H0_S2	BN8
AF19	VDD2H0_S2	VDD2H0_S2	BN10
AF21	VDD2H0_S2	VDD2H0_S2	BN12
AG3	VDD2H0_S2	VDD2H0_S2	BN14
AG5	VDD2H0_S2	VDD2H0_S2	BN16
AG7	VDD2H0_S2	VDD2H0_S2	BN20
AG9	VDD2H0_S2	VDD2H0_S2	BN22
AG11	VDD2H0_S2	VDD2H0_S2	BP7
AG17	VDD2H0_S2	VDD2H0_S2	G7
AG19	VDD2H0_S2	VDD2H0_S2	H3
AG21	VDD2H0_S2	VDD2H0_S2	H4
AH3	VDD2H0_S2	VDD2H0_S2	H8
AH4	VDD2H0_S2	VDD2H0_S2	H10
AH8	VDD2H0_S2	VDD2H0_S2	H12
AH10	VDD2H0_S2	VDD2H0_S2	H14
AH12	VDD2H0_S2	VDD2H0_S2	H16
AH14	VDD2H0_S2	VDD2H0_S2	H20
AH16	VDD2H0_S2	VDD2H0_S2	H22
AH20	VDD2H0_S2	VDD2H0_S2	J3
AH22	VDD2H0_S2	VDD2H0_S2	J5
AJ7	VDD2H0_S2	VDD2H0_S2	J7
AM7	VDD2H0_S2	VDD2H0_S2	J9
AN3	VDD2H0_S2	VDD2H0_S2	J11
AN4	VDD2H0_S2	VDD2H0_S2	J17
AN8	VDD2H0_S2	VDD2H0_S2	J19
AN10	VDD2H0_S2	VDD2H0_S2	J21
AN12	VDD2H0_S2	VDD2H0_S2	K5
AN14	VDD2H0_S2	VDD2H0_S2	K7
AN16	VDD2H0_S2	VDD2H0_S2	K9
AN20	VDD2H0_S2	VDD2H0_S2	K17
AN22	VDD2H0_S2	VDD2H0_S2	K19
AP3	VDD2H0_S2	VDD2H0_S2	K21
AP5	VDD2H0_S2	VDD2H0_S2	L4
AP7	VDD2H0_S2	VDD2H0_S2	L8
AP9	VDD2H0_S2	VDD2H0_S2	L10
AP11	VDD2H0_S2	VDD2H0_S2	L16
AP17	VDD2H0_S2	VDD2H0_S2	L18
AP19	VDD2H0_S2	VDD2H0_S2	L20
AP21	VDD2H0_S2	VDD2H0_S2	M4
AR5	VDD2H0_S2	VDD2H0_S2	M8
AR7	VDD2H0_S2	VDD2H0_S2	M12
AR9	VDD2H0_S2	VDD2H0_S2	M16
AR17	VDD2H0_S2	VDD2H0_S2	M20
AR19	VDD2H0_S2		
AR21	VDD2H0_S2	VDD2H0_S2_SENSE1	G13 VSNS_PVDD2H0_SENSE1_P OUT 11
AT4	VDD2H0_S2	VDD2H0_S2_SENSE3	AL17 VSNS_PVDD2H0_SENSE3_P OUT 11
AT8	VDD2H0_S2		
AT10	VDD2H0_S2		
AT16	VDD2H0_S2		
AT18	VDD2H0_S2		
AT20	VDD2H0_S2		
AU4	VDD2H0_S2		
AU8	VDD2H0_S2		
AU12	VDD2H0_S2		
AU16	VDD2H0_S2		
AU20	VDD2H0_S2		
BJ4	VDD2H0_S2		
BJ8	VDD2H0_S2		
BJ12	VDD2H0_S2		
BJ16	VDD2H0_S2		
BJ20	VDD2H0_S2		
BK4	VDD2H0_S2		
BK8	VDD2H0_S2		
BK10	VDD2H0_S2		
BK16	VDD2H0_S2		
BK18	VDD2H0_S2		
BK20	VDD2H0_S2		
BL5	VDD2H0_S2		
BL7	VDD2H0_S2		

C3700 C3701 C3702 C3703 C3704 C3705 C3706 C3707
11UF 20% 2.5V X6T 0402

C3708 C3709 C3710 C3711 C3712 C3713 C3714 C3715
11UF 20% 2.5V X6T 0402

C3716 C3717 C3718 C3719 C3720 C3721 C3722 C3723
11UF 20% 2.5V X6T 0402

C3724 C3725 C3726 C3727 C3728 C3729 C3730 C3731
11UF 20% 2.5V X6T 0402

C3750 C3751 C3752 C3753 C3754 C3755 C3756 C3757 C3758 C3759
15UF 20% 2.5V X6S 0402-4

BOM_COST_GROUP=SOC

PAGE TITLE
SOC: POWER (VDD2H0)

Apple Inc.

DRAWING NUMBER 051-08286
SIZE D
REVISION 5.0.3
BRANCH
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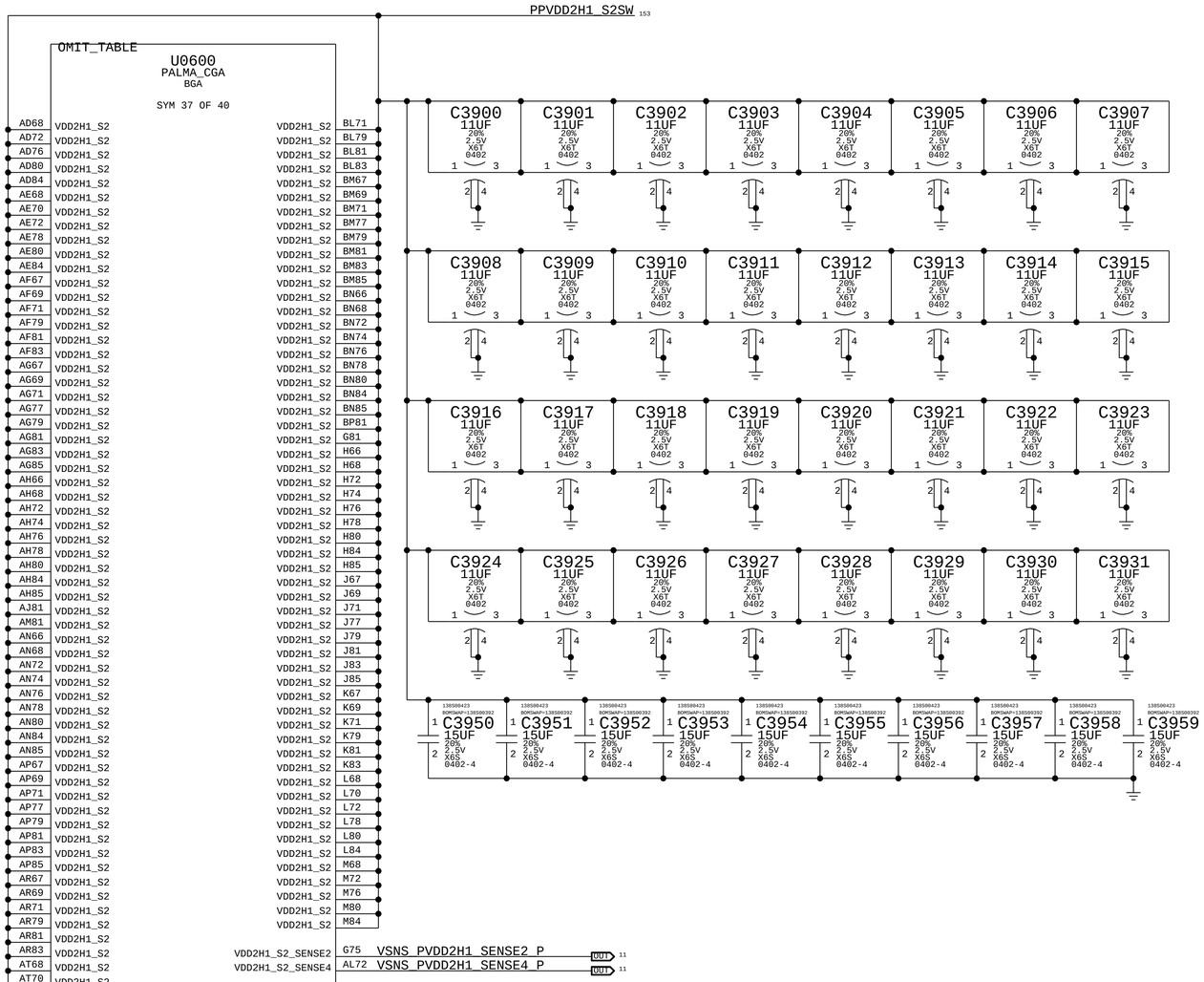

BOM_COST_GROUP=SOC

PAGE TITLE
SOC: POWER (VDD2H1)

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DRAWING NUMBER 051-08286
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PAGE 39 OF 700
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TODO_DT: GND symbols and pin alignment is still in flux with CAD. We will have some floating wires in the meantime

Ready for initial placement

OMIT_TABLE
U0600
PALMA_CGA
BGA

SYM 1 OF 40

A2	VSS	VSS	B1
A4	VSS	VSS	B3
A5	VSS	VSS	B4
A6	VSS	VSS	B5
A7	VSS	VSS	B6
A8	VSS	VSS	B7
A9	VSS	VSS	B8
A10	VSS	VSS	B10
A11	VSS	VSS	B15
A12	VSS	VSS	B21
A13	VSS	VSS	B26
A14	VSS	VSS	B28
A15	VSS	VSS	B30
A16	VSS	VSS	B32
A17	VSS	VSS	B34
A18	VSS	VSS	B35
A19	VSS	VSS	B38
A20	VSS	VSS	B40
A21	VSS	VSS	B42
A22	VSS	VSS	B44
A23	VSS	VSS	B46
A24	VSS	VSS	B48
A25	VSS	VSS	B50
A26	VSS	VSS	B52
A27	VSS	VSS	B54
A28	VSS	VSS	B55
A29	VSS	VSS	B56
A30	VSS	VSS	B58
A31	VSS	VSS	B60
A32	VSS	VSS	B62
A33	VSS	VSS	B64
A34	VSS	VSS	B69
A35	VSS	VSS	B72
A36	VSS	VSS	B80
A37	VSS	VSS	B81
A38	VSS	VSS	B82
A39	VSS	VSS	B83
A40	VSS	VSS	B84
A41	VSS	VSS	B85
A42	VSS	VSS	B87
A43	VSS	VSS	C2
A44	VSS	VSS	C3
A45	VSS	VSS	C4
A46	VSS	VSS	C5
A47	VSS	VSS	C6
A48	VSS	VSS	C7
A49	VSS	VSS	C8
A50	VSS	VSS	C10
A51	VSS	VSS	C11
A52	VSS	VSS	C15
A53	VSS	VSS	C21
A54	VSS	VSS	C26
A55	VSS	VSS	C35
A56	VSS	VSS	C36
A57	VSS	VSS	C37
A58	VSS	VSS	C38
A59	VSS	VSS	C55
A60	VSS	VSS	C64
A61	VSS	VSS	C69
A62	VSS	VSS	C72
A63	VSS	VSS	C80
A64	VSS	VSS	C81
A65	VSS	VSS	C82
A66	VSS	VSS	C83
A67	VSS	VSS	C84
A68	VSS	VSS	C85
A69	VSS	VSS	C86
A70	VSS	VSS	D1
A71	VSS	VSS	D2
A72	VSS	VSS	D3
A73	VSS	VSS	D4
A74	VSS	VSS	D5
A75	VSS	VSS	D6
A76	VSS	VSS	D7
A77	VSS	VSS	D8
A78	VSS	VSS	D10
A79	VSS	VSS	D11
A80	VSS	VSS	D12
A81	VSS	VSS	D13
A82	VSS	VSS	D14
A83	VSS	VSS	D15
A84	VSS	VSS	D16
A86	VSS	VSS	D17

OMIT_TABLE
U0600
PALMA_CGA
BGA

SYM 2 OF 40

D18	VSS	VSS	E42
D19	VSS	VSS	E44
D20	VSS	VSS	E46
D21	VSS	VSS	E48
D22	VSS	VSS	E50
D23	VSS	VSS	E52
D24	VSS	VSS	E54
D25	VSS	VSS	E55
D26	VSS	VSS	E56
D27	VSS	VSS	E58
D29	VSS	VSS	E60
D31	VSS	VSS	E62
D33	VSS	VSS	E63
D35	VSS	VSS	E65
D37	VSS	VSS	E66
D38	VSS	VSS	E68
D39	VSS	VSS	E70
D41	VSS	VSS	E71
D43	VSS	VSS	E72
D45	VSS	VSS	E80
D47	VSS	VSS	E81
D49	VSS	VSS	E82
D51	VSS	VSS	E83
D53	VSS	VSS	E84
D55	VSS	VSS	E85
D57	VSS	VSS	E86
D59	VSS	VSS	E87
D61	VSS	VSS	F1
D63	VSS	VSS	F2
D65	VSS	VSS	F3
D66	VSS	VSS	F4
D67	VSS	VSS	F5
D68	VSS	VSS	F6
D69	VSS	VSS	F7
D70	VSS	VSS	F8
D71	VSS	VSS	F9
D72	VSS	VSS	F10
D74	VSS	VSS	F11
D76	VSS	VSS	F12
D78	VSS	VSS	F13
D80	VSS	VSS	F14
D81	VSS	VSS	F15
D82	VSS	VSS	F16
D83	VSS	VSS	F17
D84	VSS	VSS	F18
D85	VSS	VSS	F19
D86	VSS	VSS	F20
D87	VSS	VSS	F21
E1	VSS	VSS	F22
E2	VSS	VSS	F23
E3	VSS	VSS	F24
E4	VSS	VSS	F25
E5	VSS	VSS	F26
E6	VSS	VSS	F28
E7	VSS	VSS	F30
E8	VSS	VSS	F32
E11	VSS	VSS	F34
E12	VSS	VSS	F35
E13	VSS	VSS	F36
E14	VSS	VSS	F38
E15	VSS	VSS	F55
E16	VSS	VSS	F56
E17	VSS	VSS	F63
E18	VSS	VSS	F64
E19	VSS	VSS	F65
E20	VSS	VSS	F66
E21	VSS	VSS	F69
E22	VSS	VSS	F70
E23	VSS	VSS	F71
E24	VSS	VSS	F72
E25	VSS	VSS	F80
E26	VSS	VSS	F81
E27	VSS	VSS	F82
E28	VSS	VSS	F83
E29	VSS	VSS	F84
E30	VSS	VSS	F85
E31	VSS	VSS	F86
E32	VSS	VSS	F87
E33	VSS	VSS	G1
E34	VSS	VSS	G2
E35	VSS	VSS	G3
E38	VSS	VSS	G4
E40	VSS	VSS	G5

OMIT_TABLE
U0600
PALMA_CGA
BGA

SYM 3 OF 40

G6	VSS	VSS	H47
G8	VSS	VSS	H48
G9	VSS	VSS	H49
G10	VSS	VSS	H50
G11	VSS	VSS	H51
G14	VSS	VSS	H52
G16	VSS	VSS	H53
G17	VSS	VSS	H54
G18	VSS	VSS	H55
G19	VSS	VSS	H56
G20	VSS	VSS	H57
G21	VSS	VSS	H58
G22	VSS	VSS	H59
G23	VSS	VSS	H60
G24	VSS	VSS	H61
G25	VSS	VSS	H62
G26	VSS	VSS	H63
G35	VSS	VSS	H64
G36	VSS	VSS	H65
G37	VSS	VSS	H67
G38	VSS	VSS	H69
G39	VSS	VSS	H71
G41	VSS	VSS	H73
G43	VSS	VSS	H75
G45	VSS	VSS	H77
G47	VSS	VSS	H79
G49	VSS	VSS	H81
G51	VSS	VSS	H83
G53	VSS	VSS	H86
G55	VSS	VSS	H87
G56	VSS	VSS	J1
G57	VSS	VSS	J2
G59	VSS	VSS	J4
G61	VSS	VSS	J6
G63	VSS	VSS	J8
G64	VSS	VSS	J10
G65	VSS	VSS	J12
G66	VSS	VSS	J14
G67	VSS	VSS	J16
G69	VSS	VSS	J18
G70	VSS	VSS	J20
G71	VSS	VSS	J22
G72	VSS	VSS	J23
G76	VSS	VSS	J24
G77	VSS	VSS	J25
G78	VSS	VSS	J26
G79	VSS	VSS	J27
G80	VSS	VSS	J28
G82	VSS	VSS	J29
G83	VSS	VSS	J30
G84	VSS	VSS	J31
G85	VSS	VSS	J32
G86	VSS	VSS	J33
G87	VSS	VSS	J34
H1	VSS	VSS	J35
H2	VSS	VSS	J36
H5	VSS	VSS	J38
H7	VSS	VSS	J40
H9	VSS	VSS	J41
H11	VSS	VSS	J42
H13	VSS	VSS	J43
H15	VSS	VSS	J44
H17	VSS	VSS	J45
H19	VSS	VSS	J46
H21	VSS	VSS	J47
H23	VSS	VSS	J48
H24	VSS	VSS	J49
H25	VSS	VSS	J50
H26	VSS	VSS	J51
H27	VSS	VSS	J52
H29	VSS	VSS	J53
H31	VSS	VSS	J54
H33	VSS	VSS	J55
H35	VSS	VSS	J56
H36	VSS	VSS	J57
H39	VSS	VSS	J58
H40	VSS	VSS	J59
H41	VSS	VSS	J60
H42	VSS	VSS	J61
H43	VSS	VSS	J62
H44	VSS	VSS	J63
H45	VSS	VSS	J64
H46	VSS	VSS	J65

OMIT_TABLE
U0600
PALMA_CGA
BGA

SYM 4 OF 40

J66	VSS	VSS	L38
J68	VSS	VSS	L41
J70	VSS	VSS	L42
J72	VSS	VSS	L46
J74	VSS	VSS	L51
J76	VSS	VSS	L55
J78	VSS	VSS	L56
J80	VSS	VSS	L57
J82	VSS	VSS	L58
J84	VSS	VSS	L59
J86	VSS	VSS	L60
J87	VSS	VSS	L61
K1	VSS	VSS	L62
K2	VSS	VSS	L63
K3	VSS	VSS	L65
K4	VSS	VSS	L67
K6	VSS	VSS	L69
K8	VSS	VSS	L71
K10	VSS	VSS	L73
K11	VSS	VSS	L76
K13	VSS	VSS	L77
K14	VSS	VSS	L79
K16	VSS	VSS	L81
K18	VSS	VSS	L83
K20	VSS	VSS	L86
K22	VSS	VSS	L87
K24	VSS	VSS	M1
K25	VSS	VSS	M2
K26	VSS	VSS	M5
K27	VSS	VSS	M7
K36	VSS	VSS	M9
K38	VSS	VSS	M11
K41	VSS	VSS	M13
K42	VSS	VSS	M15
K46	VSS	VSS	M17
K47	VSS	VSS	M19
K51	VSS	VSS	M21
K55	VSS	VSS	M23
K56	VSS	VSS	M24
K57	VSS	VSS	M25
K58	VSS	VSS	M26
K59	VSS	VSS	M27
K60	VSS	VSS	M28
K61	VSS	VSS	M30
K63	VSS	VSS	M32
K64	VSS	VSS	M34
K66	VSS	VSS	M36
K68	VSS	VSS	M37
K70	VSS	VSS	M38
K72	VSS	VSS	M39
K74	VSS	VSS	M40
K75	VSS	VSS	M43
K77	VSS	VSS	M44
K78	VSS	VSS	M45
K80	VSS	VSS	M48
K82	VSS	VSS	M49
K84	VSS	VSS	M50
K85	VSS	VSS	M52
K86	VSS	VSS	M53
K87	VSS	VSS	M54
L1	VSS	VSS	M59
L2	VSS	VSS	M60
L5	VSS	VSS	M61
L7	VSS	VSS	M62
L9	VSS	VSS	M63
L11	VSS	VSS	M64
L12	VSS	VSS	M65
L15	VSS	VSS	M67
L17	VSS	VSS	M69
L19	VSS	VSS	M71
L21	VSS	VSS	M73
L23	VSS	VSS	M75
L24	VSS	VSS	M77
L25	VSS	VSS	M79
L26	VSS	VSS	M81
L27	VSS	VSS	M83
L28	VSS	VSS	M86
L29	VSS	VSS	M87
L31	VSS	VSS	N1
L33	VSS	VSS	N2
L35	VSS	VSS	N3
L36	VSS	VSS	N4
L37	VSS	VSS	N5

OMIT_TABLE
U0600
PALMA_CGA
BGA

SYM 5 OF 40

N6	VSS	VSS	P39
N7	VSS	VSS	P41
N8	VSS	VSS	P43
N19	VSS	VSS	P46
N20	VSS	VSS	P47
N21	VSS	VSS	P50
N22	VSS	VSS	P51
N23	VSS	VSS	P52
N24	VSS	VSS	P53
N25	VSS	VSS	P54
N26	VSS	VSS	P55
N27	VSS	VSS	P56
N28	VSS	VSS	P57
N29	VSS	VSS	P59
N31	VSS	VSS	P61
N33	VSS	VSS	P63
N35	VSS	VSS	P64
N37	VSS	VSS	P65
N39	VSS	VSS	P66
N40	VSS	VSS	P67
N41	VSS	VSS	P68
N43	VSS	VSS	P69
N44	VSS	VSS	P70
N45	VSS	VSS	P71
N46	VSS	VSS	P72
N47	VSS	VSS	P80
N48	VSS	VSS	P81
N49	VSS	VSS	P82
N50	VSS	VSS	P83
N51	VSS	VSS	P84
N52	VSS	VSS	P85
N53	VSS	VSS	P86
N54	VSS	VSS	P87
N55	VSS	VSS	R1
N56	VSS	VSS	R2
N57	VSS	VSS	R3
N58	VSS	VSS	R4
N59	VSS	VSS	R5
N60	VSS	VSS	R6
N61	VSS	VSS	R7
N62	VSS	VSS	R8
N65	VSS	VSS	R10
N66	VSS	VSS	R12
N67	VSS	VSS	R14
N68	VSS	VSS	R16
N69	VSS	VSS	R18
N80	VSS	VSS	R19
N81	VSS	VSS	R20
N82	VSS	VSS	R21
N83	VSS	VSS	R22
N84	VSS	VSS	R23
N85	VSS	VSS	R24
N86	VSS	VSS	R25
N87	VSS	VSS	R27
P1	VSS	VSS	R28
P2	VSS	VSS	R30
P3	VSS	VSS	R32
P4	VSS	VSS	R33
P5	VSS	VSS	R34
P6	VSS	VSS	R35
P7	VSS	VSS	R36
P8	VSS	VSS	R37
P16	VSS	VSS	R39
P17	VSS	VSS	R40
P18	VSS	VSS	R41
P19	VSS	VSS	R43
P20	VSS	VSS	R46
P21	VSS	VSS	R47
P22	VSS	VSS	R48
P25	VSS	VSS	R49
P26	VSS	VSS	R51
P27	VSS	VSS	R52
P28	VSS	VSS	R59
P29	VSS	VSS	R61
P30	VSS	VSS	R63
P31	VSS	VSS	R64
P32	VSS	VSS	R67
P33	VSS	VSS	R68
P34	VSS	VSS	R69
P35	VSS	VSS	R70
P36	VSS	VSS	R74
P37	VSS	VSS	R76
P38	VSS	VSS	R78

OMIT_TABLE
U0600
PALMA_CGA
BGA

SYM 6 OF 40

R80	VSS	VSS	U68
R81	VSS	VSS	U69
R82	VSS	VSS	U70
R83	VSS	VSS	U71
R84	VSS	VSS	U72
R85	VSS	VSS	U80
R86	VSS	VSS	U81
R87	VSS	VSS	U82
T1	VSS	VSS	U83
T2	VSS	VSS	U84
T3	VSS	VSS	U85
T4	VSS	VSS	U86
T5	VSS	VSS	U87
T6	VSS	VSS	V1
T7	VSS	VSS	V2
T8	VSS	VSS	V3
T16	VSS	VSS	V4
T18	VSS	VSS	V5
T19	VSS	VSS	V6
T20	VSS	VSS	V7
T21	VSS	VSS	V8
T22	VSS	VSS	V10
T23	VSS	VSS	V12
T25	VSS	VSS	V14
T26	VSS	VSS	V16
T27	VSS	VSS	V17
T29	VSS	VSS	V18
T31	VSS	VSS	V19
T34	VSS	VSS	V20
T41	VSS	VSS	V21
T42	VSS	VSS	V22
T43	VSS	VSS	V23
T44	VSS	VSS	V24
T45	VSS	VSS	V25
T46	VSS	VSS	V26
T47	VSS	VSS	V27
T54	VSS	VSS	V30
T61	VSS	VSS	V35
T63	VSS	VSS	V54
T65	VSS	VSS	V62
T66	VSS	VSS	V64
T67	VSS	VSS	V65
T68	VSS	VSS	V66
T70	VSS	VSS	V67
T71	VSS	VSS	V68
T72	VSS	VSS	V70
T80	VSS	VSS	V71
T81	VSS	VSS	V72
T82	VSS	VSS	V74
T83	VSS	VSS	V76
T84	VSS	VSS	V78
T85	VSS	VSS	V80
T86	VSS	VSS	V81
T87	VSS	VSS	V82
U1	VSS	VSS	V83
U2	VSS	VSS	V84
U3	VSS	VSS	V85
U4	VSS	VSS	V86
U5	VSS	VSS	V87
U6	VSS	VSS	W1
U7	VSS	VSS	W2
U8	VSS	VSS	W3
U16	VSS	VSS	W4
U17	VSS	VSS	W5
U18	VSS	VSS	W6
U19	VSS	VSS	W7
U20	VSS	VSS	W8
U21	VSS	VSS	W16
U22	VSS	VSS	W17
U24	VSS	VSS	W18
U25	VSS	VSS	W19
U26	VSS	VSS	W20
U27	VSS	VSS	W21
U30	VSS	VSS	W22
U40	VSS	VSS	W23
U44	VSS	VSS	W24
U45	VSS	VSS	W25
U49	VSS	VSS	W26
U54	VSS	VSS	W27
U61	VSS	VSS	W29
U64	VSS	VSS	W35
U66	VSS	VSS	W44
U67	VSS	VSS	W45

BOM_COST_GROUP=SOC

PAGE TITLE
SOC: GND-1

Apple Inc.

DRAWING NUMBER 051-08286
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BRANCH
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TODO_DT: GND symbols and pin alignment is still in flux with CAD. We will have some floating wires in the meantime

Ready for initial placement

OMIT_TABLE
U0600
PALMA_CGA
BGA
SYM 7 OF 40

W54	VSS	VSS	AA68
W62	VSS	VSS	AA69
W63	VSS	VSS	AA70
W67	VSS	VSS	AA71
W68	VSS	VSS	AA72
W69	VSS	VSS	AA74
W70	VSS	VSS	AA76
W71	VSS	VSS	AA78
W72	VSS	VSS	AA80
W80	VSS	VSS	AA81
W81	VSS	VSS	AA82
W82	VSS	VSS	AA83
W83	VSS	VSS	AA84
W84	VSS	VSS	AA85
W85	VSS	VSS	AA86
W86	VSS	VSS	AA87
W87	VSS	VSS	AB1
Y1	VSS	VSS	AB2
Y2	VSS	VSS	AB3
Y3	VSS	VSS	AB4
Y4	VSS	VSS	AB5
Y5	VSS	VSS	AB6
Y6	VSS	VSS	AB7
Y7	VSS	VSS	AB8
Y8	VSS	VSS	AB16
Y16	VSS	VSS	AB17
Y17	VSS	VSS	AB18
Y18	VSS	VSS	AB19
Y19	VSS	VSS	AB20
Y20	VSS	VSS	AB22
Y21	VSS	VSS	AB24
Y23	VSS	VSS	AB25
Y24	VSS	VSS	AB29
Y26	VSS	VSS	AB37
Y27	VSS	VSS	AB52
Y29	VSS	VSS	AB56
Y34	VSS	VSS	AB59
Y35	VSS	VSS	AB60
Y54	VSS	VSS	AB61
Y63	VSS	VSS	AB62
Y65	VSS	VSS	AB63
Y67	VSS	VSS	AB64
Y68	VSS	VSS	AB66
Y70	VSS	VSS	AB67
Y71	VSS	VSS	AB68
Y72	VSS	VSS	AB69
Y80	VSS	VSS	AB70
Y81	VSS	VSS	AB71
Y82	VSS	VSS	AB72
Y83	VSS	VSS	AB80
Y84	VSS	VSS	AB81
Y85	VSS	VSS	AB82
Y86	VSS	VSS	AB83
Y87	VSS	VSS	AB84
AA1	VSS	VSS	AB85
AA2	VSS	VSS	AB86
AA3	VSS	VSS	AB87
AA4	VSS	VSS	AC1
AA5	VSS	VSS	AC2
AA6	VSS	VSS	AC3
AA7	VSS	VSS	AC4
AA8	VSS	VSS	AC5
AA10	VSS	VSS	AC6
AA12	VSS	VSS	AC7
AA14	VSS	VSS	AC8
AA16	VSS	VSS	AC19
AA17	VSS	VSS	AC20
AA18	VSS	VSS	AC21
AA19	VSS	VSS	AC22
AA20	VSS	VSS	AC23
AA21	VSS	VSS	AC28
AA24	VSS	VSS	AC29
AA26	VSS	VSS	AC30
AA27	VSS	VSS	AC32
AA29	VSS	VSS	AC39
AA36	VSS	VSS	AC50
AA40	VSS	VSS	AC57
AA49	VSS	VSS	AC60
AA53	VSS	VSS	AC61
AA55	VSS	VSS	AC62
AA63	VSS	VSS	AC66
AA65	VSS	VSS	AC67
AA67	VSS	VSS	AC68

OMIT_TABLE
U0600
PALMA_CGA
BGA
SYM 8 OF 40

AC69	VSS	VSS	AF3
AC80	VSS	VSS	AF4
AC81	VSS	VSS	AF6
AC82	VSS	VSS	AF8
AC83	VSS	VSS	AF10
AC84	VSS	VSS	AF11
AC85	VSS	VSS	AF13
AC86	VSS	VSS	AF14
AC87	VSS	VSS	AF16
AD1	VSS	VSS	AF18
AD2	VSS	VSS	AF20
AD5	VSS	VSS	AF22
AD7	VSS	VSS	AF26
AD9	VSS	VSS	AF31
AD11	VSS	VSS	AF33
AD13	VSS	VSS	AF35
AD15	VSS	VSS	AF37
AD17	VSS	VSS	AF38
AD19	VSS	VSS	AF40
AD21	VSS	VSS	AF42
AD23	VSS	VSS	AF44
AD26	VSS	VSS	AF45
AD27	VSS	VSS	AF47
AD28	VSS	VSS	AF48
AD32	VSS	VSS	AF50
AD39	VSS	VSS	AF52
AD44	VSS	VSS	AF54
AD45	VSS	VSS	AF56
AD50	VSS	VSS	AF57
AD57	VSS	VSS	AF62
AD59	VSS	VSS	AF66
AD60	VSS	VSS	AF68
AD61	VSS	VSS	AF70
AD62	VSS	VSS	AF72
AD65	VSS	VSS	AF74
AD67	VSS	VSS	AF75
AD69	VSS	VSS	AF77
AD71	VSS	VSS	AF78
AD73	VSS	VSS	AF80
AD75	VSS	VSS	AF82
AD77	VSS	VSS	AF84
AD79	VSS	VSS	AF85
AD81	VSS	VSS	AF86
AD83	VSS	VSS	AF87
AD86	VSS	VSS	AG1
AD87	VSS	VSS	AG2
AE1	VSS	VSS	AG4
AE2	VSS	VSS	AG6
AE5	VSS	VSS	AG8
AE7	VSS	VSS	AG10
AE9	VSS	VSS	AG12
AE11	VSS	VSS	AG14
AE12	VSS	VSS	AG16
AE15	VSS	VSS	AG18
AE17	VSS	VSS	AG20
AE19	VSS	VSS	AG22
AE21	VSS	VSS	AG23
AE23	VSS	VSS	AG26
AE26	VSS	VSS	AG31
AE30	VSS	VSS	AG33
AE31	VSS	VSS	AG35
AE32	VSS	VSS	AG37
AE33	VSS	VSS	AG38
AE39	VSS	VSS	AG44
AE50	VSS	VSS	AG47
AE58	VSS	VSS	AG50
AE61	VSS	VSS	AG52
AE62	VSS	VSS	AG56
AE64	VSS	VSS	AG57
AE65	VSS	VSS	AG62
AE67	VSS	VSS	AG65
AE69	VSS	VSS	AG66
AE71	VSS	VSS	AG68
AE73	VSS	VSS	AG70
AE76	VSS	VSS	AG72
AE77	VSS	VSS	AG74
AE79	VSS	VSS	AG76
AE81	VSS	VSS	AG78
AE83	VSS	VSS	AG80
AE86	VSS	VSS	AG82
AE87	VSS	VSS	AG84
AF1	VSS	VSS	AG86
AF2	VSS	VSS	AG87

OMIT_TABLE
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PALMA_CGA
BGA
SYM 9 OF 40

AH1	VSS	VSS	AJ83
AH2	VSS	VSS	AJ84
AH5	VSS	VSS	AJ85
AH7	VSS	VSS	AJ86
AH9	VSS	VSS	AJ87
AH11	VSS	VSS	AK1
AH13	VSS	VSS	AK2
AH15	VSS	VSS	AK3
AH17	VSS	VSS	AK4
AH19	VSS	VSS	AK5
AH21	VSS	VSS	AK6
AH23	VSS	VSS	AK7
AH24	VSS	VSS	AK8
AH26	VSS	VSS	AK15
AH31	VSS	VSS	AK17
AH32	VSS	VSS	AK18
AH33	VSS	VSS	AK19
AH34	VSS	VSS	AK20
AH35	VSS	VSS	AK21
AH36	VSS	VSS	AK22
AH37	VSS	VSS	AK23
AH43	VSS	VSS	AK26
AH45	VSS	VSS	AK33
AH51	VSS	VSS	AK34
AH52	VSS	VSS	AK36
AH53	VSS	VSS	AK44
AH54	VSS	VSS	AK52
AH55	VSS	VSS	AK54
AH56	VSS	VSS	AK55
AH57	VSS	VSS	AK62
AH62	VSS	VSS	AK65
AH64	VSS	VSS	AK66
AH65	VSS	VSS	AK67
AH67	VSS	VSS	AK68
AH69	VSS	VSS	AK69
AH71	VSS	VSS	AK70
AH73	VSS	VSS	AK71
AH75	VSS	VSS	AK80
AH77	VSS	VSS	AK81
AH79	VSS	VSS	AK82
AH81	VSS	VSS	AK83
AH83	VSS	VSS	AK84
AH86	VSS	VSS	AK85
AH87	VSS	VSS	AK86
AJ1	VSS	VSS	AK87
AJ2	VSS	VSS	AL1
AJ3	VSS	VSS	AL2
AJ4	VSS	VSS	AL3
AJ5	VSS	VSS	AL4
AJ6	VSS	VSS	AL5
AJ8	VSS	VSS	AL6
AJ17	VSS	VSS	AL7
AJ18	VSS	VSS	AL8
AJ19	VSS	VSS	AL10
AJ20	VSS	VSS	AL12
AJ21	VSS	VSS	AL14
AJ22	VSS	VSS	AL15
AJ23	VSS	VSS	AL18
AJ26	VSS	VSS	AL19
AJ33	VSS	VSS	AL20
AJ34	VSS	VSS	AL21
AJ36	VSS	VSS	AL23
AJ43	VSS	VSS	AL24
AJ45	VSS	VSS	AL26
AJ52	VSS	VSS	AL31
AJ54	VSS	VSS	AL32
AJ55	VSS	VSS	AL34
AJ62	VSS	VSS	AL35
AJ65	VSS	VSS	AL37
AJ66	VSS	VSS	AL39
AJ67	VSS	VSS	AL41
AJ68	VSS	VSS	AL43
AJ69	VSS	VSS	AL44
AJ70	VSS	VSS	AL45
AJ71	VSS	VSS	AL47
AJ74	VSS	VSS	AL49
AJ75	VSS	VSS	AL51
AJ76	VSS	VSS	AL53
AJ77	VSS	VSS	AL54
AJ78	VSS	VSS	AL56
AJ79	VSS	VSS	AL57
AJ80	VSS	VSS	AL62
AJ82	VSS	VSS	AL64

OMIT_TABLE
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PALMA_CGA
BGA
SYM 10 OF 40

AL65	VSS	VSS	AN73
AL66	VSS	VSS	AN75
AL67	VSS	VSS	AN77
AL68	VSS	VSS	AN79
AL69	VSS	VSS	AN81
AL70	VSS	VSS	AN83
AL74	VSS	VSS	AN86
AL76	VSS	VSS	AN87
AL78	VSS	VSS	AP1
AL80	VSS	VSS	AP2
AL81	VSS	VSS	AP4
AL82	VSS	VSS	AP6
AL83	VSS	VSS	AP8
AL84	VSS	VSS	AP10
AL85	VSS	VSS	AP12
AL86	VSS	VSS	AP14
AL87	VSS	VSS	AP16
AM1	VSS	VSS	AP18
AM2	VSS	VSS	AP20
AM3	VSS	VSS	AP22
AM4	VSS	VSS	AP23
AM5	VSS	VSS	AP24
AM6	VSS	VSS	AP26
AM8	VSS	VSS	AP27
AM16	VSS	VSS	AP30
AM17	VSS	VSS	AP33
AM19	VSS	VSS	AP41
AM20	VSS	VSS	AP47
AM21	VSS	VSS	AP55
AM22	VSS	VSS	AP58
AM23	VSS	VSS	AP61
AM26	VSS	VSS	AP64
AM31	VSS	VSS	AP65
AM32	VSS	VSS	AP66
AM34	VSS	VSS	AP68
AM44	VSS	VSS	AP70
AM54	VSS	VSS	AP72
AM56	VSS	VSS	AP74
AM57	VSS	VSS	AP76
AM62	VSS	VSS	AP78
AM65	VSS	VSS	AP80
AM66	VSS	VSS	AP82
AM67	VSS	VSS	AP84
AM68	VSS	VSS	AP86
AM69	VSS	VSS	AP87
AM71	VSS	VSS	AR1
AM72	VSS	VSS	AR2
AM80	VSS	VSS	AR3
AM82	VSS	VSS	AR4
AM83	VSS	VSS	AR6
AM84	VSS	VSS	AR8
AM85	VSS	VSS	AR10
AM86	VSS	VSS	AR11
AM87	VSS	VSS	AR13
AN1	VSS	VSS	AR14
AN2	VSS	VSS	AR16
AN5	VSS	VSS	AR18
AN7	VSS	VSS	AR20
AN9	VSS	VSS	AR22
AN11	VSS	VSS	AR28
AN13	VSS	VSS	AR29
AN15	VSS	VSS	AR30
AN17	VSS	VSS	AR31
AN19	VSS	VSS	AR32
AN21	VSS	VSS	AR34
AN23	VSS	VSS	AR41
AN26	VSS	VSS	AR47
AN33	VSS	VSS	AR54
AN36	VSS	VSS	AR56
AN38	VSS	VSS	AR57
AN40	VSS	VSS	AR58
AN42	VSS	VSS	AR59
AN44	VSS	VSS	AR60
AN46	VSS	VSS	AR61
AN48	VSS	VSS	AR62
AN50	VSS	VSS	AR66
AN52	VSS	VSS	AR68
AN55	VSS	VSS	AR70
AN62	VSS	VSS	AR72
AN65	VSS	VSS	AR74
AN67	VSS	VSS	AR75
AN69	VSS	VSS	AR77
AN71	VSS	VSS	AR78

OMIT_TABLE
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PALMA_CGA
BGA
SYM 11 OF 40

AR80	VSS	VSS	AV3
AR82	VSS	VSS	AV4
AR84	VSS	VSS	AV5
AR85	VSS	VSS	AV6
AR86	VSS	VSS	AV7
AR87	VSS	VSS	AV8
AT1	VSS	VSS	AV17
AT2	VSS	VSS	AV18
AT5	VSS	VSS	AV19
AT7	VSS	VSS	AV20
AT9	VSS	VSS	AV21
AT11	VSS	VSS	AV22
AT12	VSS	VSS	AV23
AT15	VSS	VSS	AV26
AT17	VSS	VSS	AV33
AT19	VSS	VSS	AV34
AT21	VSS	VSS	AV35
AT23	VSS	VSS	AV37
AT27	VSS	VSS	AV40
AT30	VSS	VSS	AV41
AT31	VSS	VSS	AV47
AT32	VSS	VSS	AV48
AT34	VSS	VSS	AV51
AT41	VSS	VSS	AV53
AT47	VSS	VSS	AV54
AT54	VSS	VSS	AV55
AT56	VSS	VSS	AV62
AT57	VSS	VSS	AV65
AT58	VSS	VSS	AV66
AT61	VSS	VSS	AV67
AT65	VSS	VSS	AV68
AT67	VSS	VSS	AV69
AT69	VSS	VSS	AV80
AT71	VSS	VSS	AV81
AT73	VSS	VSS	AV82
AT76	VSS	VSS	AV83
AT77	VSS	VSS	AV84
AT79	VSS	VSS	AV85
AT81	VSS	VSS	AV86
AT83	VSS	VSS	AV87
AT86	VSS	VSS	AW1
AT87	VSS	VSS	AW2
AU1	VSS	VSS	AW3
AU2	VSS	VSS	AW4
AU5	VSS	VSS	AW5
AU7	VSS	VSS	AW6
AU9	VSS	VSS	AW7
AU11	VSS	VSS	AW8
AU13	VSS	VSS	AW16
AU15	VSS	VSS	AW17
AU17	VSS	VSS	AW18
AU19	VSS	VSS	AW19
AU21	VSS	VSS	AW20
AU23	VSS	VSS	AW21
AU24	VSS	VSS	AW22
AU33	VSS	VSS	AW23
AU34	VSS	VSS	AW26
AU38	VSS	VSS	AW31
AU39	VSS	VSS	AW32
AU40	VSS	VSS	AW34
AU41	VSS	VSS	AW41
AU47	VSS	VSS	AW47
AU48	VSS	VSS	AW54
AU49	VSS	VSS	AW56
AU50	VSS	VSS	AW57
AU54	VSS	VSS	AW62
AU55	VSS	VSS	AW65
AU62	VSS	VSS	AW67
AU64	VSS	VSS	AW68
AU65	VSS	VSS	AW69
AU67	VSS	VSS	AW70
AU69	VSS	VSS	AW71
AU71	VSS	VSS	AW72
AU73	VSS	VSS	AW80
AU75	VSS	VSS	AW81
AU77	VSS	VSS	AW82
AU79	VSS	VSS	AW83
AU81	VSS	VSS	AW84
AU83	VSS	VSS	AW85
AU86	VSS	VSS	AW86
AU87	VSS	VSS	AW87
AV1	VSS	VSS	AY1
AV2	VSS	VSS	AY2

OMIT_TABLE
U0600
PALMA_CGA
BGA
SYM 12 OF 40

AY3	VSS	VSS	BA85
AY4	VSS	VSS	BA86
AY5	VSS	VSS	BA87
AY6	VSS	VSS	BB1
AY7	VSS	VSS	BB2
AY8	VSS	VSS	BB3
AY10	VSS	VSS	BB4
AY12	VSS	VSS	BB5
AY15	VSS	VSS	BB6
AY16	VSS	VSS	BB7
AY17	VSS	VSS	BB8
AY18	VSS	VSS	BB16
AY19	VSS	VSS	BB17
AY20	VSS	VSS	BB18
AY21	VSS	VSS	BB19
AY22	VSS	VSS	BB20
AY23	VSS	VSS	BB21
AY24	VSS	VSS	BB22
AY26	VSS	VSS	BB23
AY31	VSS	VSS	BB26
AY32	VSS	VSS	BB33
AY34	VSS	VSS	BB35
AY41	VSS	VSS	BB37
AY47	VSS	VSS	BB41
AY54	VSS	VSS	BB42
AY56	VSS	VSS	BB44
AY57	VSS	VSS	BB46
AY62	VSS	VSS	BB47
AY64	VSS	VSS	BB51
AY65	VSS	VSS	BB53
AY66	VSS	VSS	BB55
AY67	VSS	VSS	BB62
AY68	VSS	VSS	BB65
AY69	VSS	VSS	BB66
AY70	VSS	VSS	BB67
AY71	VSS	VSS	BB68
AY72	VSS	VSS	BB69
AY74	VSS	VSS	BB70
AY76	VSS	VSS	BB71
AY78	VSS	VSS	BB72
AY80	VSS	VSS	BB80
AY81	VSS	VSS	BB81
AY82	VSS	VSS	BB82
AY83	VSS	VSS	BB83
AY84	VSS	VSS	BB84
AY85	VSS	VSS	BB85
AY86	VSS	VSS	BB86
AY87	VSS	VSS	BB87
BA1	VSS	VSS	BC1
BA2	VSS	VSS	BC2
BA3	VSS	VSS	BC3
BA4	VSS	VSS	BC4
BA5	VSS	VSS	BC5
BA6	VSS	VSS	BC6
BA7	VSS	VSS	BC7
BA8	VSS	VSS	BC8
BA16	VSS	VSS	BC10
BA17	VSS	VSS	BC12
BA18	VSS	VSS	BC15
BA19	VSS	VSS	BC16
BA20	VSS	VSS	BC17
BA21	VSS	VSS	BC18
BA22	VSS	VSS	BC19
BA23	VSS	VSS	BC20
BA26	VSS	VSS	BC21
BA33	VSS	VSS	BC22
BA41	VSS	VSS	BC23
BA47	VSS	VSS	BC24
BA55	VSS	VSS	BC26
BA62	VSS	VSS	BC31
BA65	VSS	VSS	BC32
BA66	VSS	VSS	BC34
BA67	VSS	VSS	BC35
BA68	VSS	VSS	BC37
BA69	VSS	VSS	BC39
BA70	VSS	VSS	BC41
BA71	VSS	VSS	BC43
BA72	VSS	VSS	BC44
BA80	VSS	VSS	BC45
BA81	VSS	VSS	BC47
BA82	VSS	VSS	BC49
BA83	VSS	VSS	BC51
BA84	VSS	VSS	BC53

BOM_COST_GROUP=SOC

PAGE TITLE
SOC: GND-2

Apple Inc.

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Ready for initial placement

TODO_DT: GND symbols and pin alignment is still in flux with CAD. We will have some floating wires in the meantime

OMIT_TABLE
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PALMA_CGA
BGA
SYM 13 OF 40

BC54	VSS	VSS	BE27
BC56	VSS	VSS	BE30
BC57	VSS	VSS	BE33
BC62	VSS	VSS	BE34
BC64	VSS	VSS	BE44
BC65	VSS	VSS	BE54
BC66	VSS	VSS	BE55
BC67	VSS	VSS	BE58
BC68	VSS	VSS	BE61
BC69	VSS	VSS	BE62
BC70	VSS	VSS	BE65
BC71	VSS	VSS	BE66
BC72	VSS	VSS	BE67
BC74	VSS	VSS	BE68
BC76	VSS	VSS	BE69
BC78	VSS	VSS	BE70
BC80	VSS	VSS	BE72
BC81	VSS	VSS	BE80
BC82	VSS	VSS	BE81
BC83	VSS	VSS	BE82
BC84	VSS	VSS	BE83
BC85	VSS	VSS	BE84
BC86	VSS	VSS	BE85
BC87	VSS	VSS	BE86
BD1	VSS	VSS	BE87
BD2	VSS	VSS	BF1
BD3	VSS	VSS	BF2
BD4	VSS	VSS	BF3
BD5	VSS	VSS	BF4
BD6	VSS	VSS	BF5
BD7	VSS	VSS	BF6
BD8	VSS	VSS	BF7
BD16	VSS	VSS	BF8
BD17	VSS	VSS	BF10
BD18	VSS	VSS	BF12
BD19	VSS	VSS	BF16
BD20	VSS	VSS	BF17
BD21	VSS	VSS	BF18
BD22	VSS	VSS	BF19
BD23	VSS	VSS	BF20
BD26	VSS	VSS	BF21
BD31	VSS	VSS	BF22
BD32	VSS	VSS	BF23
BD34	VSS	VSS	BF24
BD36	VSS	VSS	BF26
BD44	VSS	VSS	BF27
BD52	VSS	VSS	BF28
BD54	VSS	VSS	BF29
BD56	VSS	VSS	BF30
BD57	VSS	VSS	BF33
BD62	VSS	VSS	BF34
BD65	VSS	VSS	BF35
BD66	VSS	VSS	BF37
BD67	VSS	VSS	BF44
BD68	VSS	VSS	BF51
BD69	VSS	VSS	BF53
BD70	VSS	VSS	BF54
BD72	VSS	VSS	BF55
BD80	VSS	VSS	BF58
BD81	VSS	VSS	BF59
BD82	VSS	VSS	BF60
BD83	VSS	VSS	BF61
BD84	VSS	VSS	BF62
BD85	VSS	VSS	BF64
BD86	VSS	VSS	BF65
BD87	VSS	VSS	BF66
BE1	VSS	VSS	BF67
BE2	VSS	VSS	BF68
BE3	VSS	VSS	BF69
BE4	VSS	VSS	BF70
BE5	VSS	VSS	BF72
BE6	VSS	VSS	BF74
BE7	VSS	VSS	BF76
BE8	VSS	VSS	BF78
BE16	VSS	VSS	BF80
BE17	VSS	VSS	BF81
BE18	VSS	VSS	BF82
BE19	VSS	VSS	BF83
BE20	VSS	VSS	BF84
BE21	VSS	VSS	BF85
BE22	VSS	VSS	BF86
BE23	VSS	VSS	BF87
BE26	VSS	VSS	BG1

OMIT_TABLE
U0600
PALMA_CGA
BGA
SYM 14 OF 40

BG2	VSS	VSS	BH34
BG3	VSS	VSS	BH35
BG4	VSS	VSS	BH36
BG5	VSS	VSS	BH37
BG6	VSS	VSS	BH38
BG7	VSS	VSS	BH39
BG8	VSS	VSS	BH40
BG16	VSS	VSS	BH41
BG17	VSS	VSS	BH42
BG18	VSS	VSS	BH43
BG19	VSS	VSS	BH44
BG20	VSS	VSS	BH45
BG21	VSS	VSS	BH46
BG22	VSS	VSS	BH47
BG23	VSS	VSS	BH48
BG24	VSS	VSS	BH49
BG25	VSS	VSS	BH50
BG26	VSS	VSS	BH51
BG27	VSS	VSS	BH52
BG28	VSS	VSS	BH53
BG29	VSS	VSS	BH54
BG30	VSS	VSS	BH55
BG31	VSS	VSS	BH56
BG32	VSS	VSS	BH57
BG33	VSS	VSS	BH59
BG34	VSS	VSS	BH60
BG35	VSS	VSS	BH61
BG36	VSS	VSS	BH62
BG43	VSS	VSS	BH63
BG44	VSS	VSS	BH64
BG45	VSS	VSS	BH65
BG52	VSS	VSS	BH66
BG53	VSS	VSS	BH67
BG54	VSS	VSS	BH68
BG55	VSS	VSS	BH69
BG56	VSS	VSS	BH70
BG57	VSS	VSS	BH80
BG58	VSS	VSS	BH81
BG59	VSS	VSS	BH82
BG60	VSS	VSS	BH83
BG61	VSS	VSS	BH84
BG62	VSS	VSS	BH85
BG63	VSS	VSS	BH86
BG64	VSS	VSS	BH87
BG65	VSS	VSS	BJ1
BG66	VSS	VSS	BJ2
BG67	VSS	VSS	BJ5
BG68	VSS	VSS	BJ7
BG69	VSS	VSS	BJ9
BG70	VSS	VSS	BJ11
BG72	VSS	VSS	BJ13
BG80	VSS	VSS	BJ15
BG81	VSS	VSS	BJ17
BG82	VSS	VSS	BJ19
BG83	VSS	VSS	BJ21
BG84	VSS	VSS	BJ23
BG85	VSS	VSS	BJ24
BG86	VSS	VSS	BJ25
BG87	VSS	VSS	BJ26
BH1	VSS	VSS	BJ27
BH2	VSS	VSS	BJ28
BH3	VSS	VSS	BJ29
BH4	VSS	VSS	BJ31
BH5	VSS	VSS	BJ32
BH6	VSS	VSS	BJ33
BH7	VSS	VSS	BJ34
BH8	VSS	VSS	BJ35
BH17	VSS	VSS	BJ36
BH18	VSS	VSS	BJ37
BH19	VSS	VSS	BJ38
BH20	VSS	VSS	BJ39
BH21	VSS	VSS	BJ40
BH22	VSS	VSS	BJ41
BH23	VSS	VSS	BJ42
BH24	VSS	VSS	BJ43
BH25	VSS	VSS	BJ44
BH26	VSS	VSS	BJ45
BH27	VSS	VSS	BJ46
BH28	VSS	VSS	BJ47
BH29	VSS	VSS	BJ48
BH31	VSS	VSS	BJ49
BH32	VSS	VSS	BJ50
BH33	VSS	VSS	BJ51

OMIT_TABLE
U0600
PALMA_CGA
BGA
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BJ52	VSS	VSS	BK83
BJ53	VSS	VSS	BK86
BJ54	VSS	VSS	BK87
BJ55	VSS	VSS	BL1
BJ56	VSS	VSS	BL2
BJ57	VSS	VSS	BL3
BJ59	VSS	VSS	BL4
BJ60	VSS	VSS	BL6
BJ61	VSS	VSS	BL8
BJ62	VSS	VSS	BL10
BJ63	VSS	VSS	BL11
BJ64	VSS	VSS	BL13
BJ65	VSS	VSS	BL14
BJ67	VSS	VSS	BL16
BJ69	VSS	VSS	BL18
BJ71	VSS	VSS	BL20
BJ73	VSS	VSS	BL22
BJ75	VSS	VSS	BL24
BJ77	VSS	VSS	BL25
BJ79	VSS	VSS	BL26
BJ81	VSS	VSS	BL27
BJ83	VSS	VSS	BL28
BJ86	VSS	VSS	BL29
BJ87	VSS	VSS	BL30
BK1	VSS	VSS	BL31
BK2	VSS	VSS	BL32
BK5	VSS	VSS	BL33
BK7	VSS	VSS	BL34
BK9	VSS	VSS	BL35
BK11	VSS	VSS	BL36
BK12	VSS	VSS	BL37
BK15	VSS	VSS	BL38
BK17	VSS	VSS	BL39
BK19	VSS	VSS	BL40
BK21	VSS	VSS	BL41
BK23	VSS	VSS	BL42
BK24	VSS	VSS	BL44
BK25	VSS	VSS	BL46
BK26	VSS	VSS	BL52
BK27	VSS	VSS	BL53
BK28	VSS	VSS	BL54
BK29	VSS	VSS	BL55
BK30	VSS	VSS	BL56
BK31	VSS	VSS	BL57
BK32	VSS	VSS	BL58
BK33	VSS	VSS	BL59
BK34	VSS	VSS	BL60
BK35	VSS	VSS	BL61
BK36	VSS	VSS	BL62
BK37	VSS	VSS	BL63
BK38	VSS	VSS	BL64
BK39	VSS	VSS	BL66
BK40	VSS	VSS	BL68
BK41	VSS	VSS	BL70
BK42	VSS	VSS	BL72
BK46	VSS	VSS	BL74
BK47	VSS	VSS	BL75
BK48	VSS	VSS	BL77
BK49	VSS	VSS	BL78
BK50	VSS	VSS	BL80
BK51	VSS	VSS	BL82
BK52	VSS	VSS	BL84
BK53	VSS	VSS	BL85
BK54	VSS	VSS	BL86
BK55	VSS	VSS	BL87
BK56	VSS	VSS	BM1
BK57	VSS	VSS	BM2
BK58	VSS	VSS	BM4
BK59	VSS	VSS	BM6
BK60	VSS	VSS	BM8
BK61	VSS	VSS	BM10
BK62	VSS	VSS	BM12
BK63	VSS	VSS	BM14
BK64	VSS	VSS	BM16
BK65	VSS	VSS	BM18
BK67	VSS	VSS	BM20
BK69	VSS	VSS	BM22
BK71	VSS	VSS	BM23
BK73	VSS	VSS	BM24
BK76	VSS	VSS	BM25
BK77	VSS	VSS	BM26
BK79	VSS	VSS	BM27
BK81	VSS	VSS	BM28

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PALMA_CGA
BGA
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BM29	VSS	VSS	BN51
BM30	VSS	VSS	BN52
BM31	VSS	VSS	BN53
BM32	VSS	VSS	BN54
BM33	VSS	VSS	BN55
BM34	VSS	VSS	BN56
BM35	VSS	VSS	BN57
BM36	VSS	VSS	BN58
BM37	VSS	VSS	BN59
BM38	VSS	VSS	BN60
BM39	VSS	VSS	BN61
BM40	VSS	VSS	BN62
BM41	VSS	VSS	BN63
BM42	VSS	VSS	BN64
BM43	VSS	VSS	BN65
BM44	VSS	VSS	BN67
BM45	VSS	VSS	BN69
BM46	VSS	VSS	BN71
BM52	VSS	VSS	BN73
BM53	VSS	VSS	BN75
BM54	VSS	VSS	BN77
BM55	VSS	VSS	BN79
BM56	VSS	VSS	BN81
BM57	VSS	VSS	BN83
BM58	VSS	VSS	BN86
BM59	VSS	VSS	BN87
BM60	VSS	VSS	BP1
BM61	VSS	VSS	BP2
BM62	VSS	VSS	BP3
BM63	VSS	VSS	BP4
BM64	VSS	VSS	BP5
BM65	VSS	VSS	BP6
BM66	VSS	VSS	BP8
BM68	VSS	VSS	BP14
BM70	VSS	VSS	BP20
BM72	VSS	VSS	BP21
BM74	VSS	VSS	BP22
BM76	VSS	VSS	BP23
BM78	VSS	VSS	BP24
BM80	VSS	VSS	BP25
BM82	VSS	VSS	BP26
BM84	VSS	VSS	BP27
BM86	VSS	VSS	BP28
BM87	VSS	VSS	BP29
BN1	VSS	VSS	BP30
BN2	VSS	VSS	BP31
BN5	VSS	VSS	BP32
BN7	VSS	VSS	BP33
BN9	VSS	VSS	BP34
BN11	VSS	VSS	BP35
BN13	VSS	VSS	BP36
BN15	VSS	VSS	BP37
BN17	VSS	VSS	BP38
BN19	VSS	VSS	BP39
BN21	VSS	VSS	BP40
BN23	VSS	VSS	BP41
BN24	VSS	VSS	BP42
BN25	VSS	VSS	BP43
BN26	VSS	VSS	BP44
BN27	VSS	VSS	BP45
BN28	VSS	VSS	BP46
BN29	VSS	VSS	BP47
BN30	VSS	VSS	BP48
BN31	VSS	VSS	BP49
BN32	VSS	VSS	BP50
BN33	VSS	VSS	BP51
BN34	VSS	VSS	BP52
BN35	VSS	VSS	BP53
BN36	VSS	VSS	BP54
BN37	VSS	VSS	BP55
BN38	VSS	VSS	BP56
BN39	VSS	VSS	BP57
BN40	VSS	VSS	BP58
BN41	VSS	VSS	BP59
BN42	VSS	VSS	BP60
BN43	VSS	VSS	BP61
BN44	VSS	VSS	BP80
BN45	VSS	VSS	BP82
BN46	VSS	VSS	BP83
BN47	VSS	VSS	BP84
BN48	VSS	VSS	BP85
BN49	VSS	VSS	BP86
BN50	VSS	VSS	BP87

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PALMA_CGA
BGA
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BR2	VSS	VSS	BT27
BR3	VSS	VSS	BT28
BR4	VSS	VSS	BT29
BR5	VSS	VSS	BT30
BR6	VSS	VSS	BT31
BR7	VSS	VSS	BT32
BR8	VSS	VSS	BT33
BR10	VSS	VSS	BT34
BR13	VSS	VSS	BT35
BR15	VSS	VSS	BT36
BR18	VSS	VSS	BT37
BR20	VSS	VSS	BT38
BR21	VSS	VSS	BT39
BR22	VSS	VSS	BT40
BR23	VSS	VSS	BT41
BR24	VSS	VSS	BT42
BR25	VSS	VSS	BT43
BR26	VSS	VSS	BT44
BR27	VSS	VSS	BT45
BR28	VSS	VSS	BT46
BR29	VSS	VSS	BT47
BR30	VSS	VSS	BT48
BR31	VSS	VSS	BT49
BR32	VSS	VSS	BT50
BR33	VSS	VSS	BT51
BR34	VSS	VSS	BT52
BR39	VSS	VSS	BT53
BR40	VSS	VSS	BT54
BR41	VSS	VSS	BT55
BR42	VSS	VSS	BT56
BR43	VSS	VSS	BT57
BR44	VSS	VSS	BT58
BR45	VSS	VSS	BT59
BR46	VSS	VSS	BT60
BR47	VSS	VSS	BT61
BR48	VSS	VSS	BT62
BR49	VSS	VSS	BT63
BR50	VSS	VSS	BT64
BR55	VSS	VSS	BT65
BR56	VSS	VSS	BT66
BR58	VSS	VSS	BT67
BR59	VSS	VSS	BT68
BR60	VSS	VSS	BT69
BR61	VSS	VSS	BT70
BR62	VSS	VSS	BT71
BR64	VSS	VSS	BT72
BR67	VSS	VSS	BT73
BR70	VSS	VSS	BT74
BR73	VSS	VSS	BT75
BR76	VSS	VSS	BT76
BR79	VSS	VSS	BT77
BR80	VSS	VSS	BT78
BR81	VSS	VSS	BT79
BR82	VSS	VSS	BT80
BR83	VSS	VSS	BT81
BR84	VSS	VSS	BT82
BR85	VSS	VSS	BT83
BR86	VSS	VSS	BT84
BT1	VSS	VSS	BT85
BT3	VSS	VSS	BT87
BT4	VSS	VSS	BU2
BT5	VSS	VSS	BU4
BT6	VSS	VSS	BU5
BT7	VSS	VSS	BU6
BT8	VSS	VSS	BU7
BT9	VSS	VSS	BU8
BT10	VSS	VSS	BU9
BT11	VSS	VSS	BU10
BT12	VSS	VSS	BU11
BT13	VSS	VSS	BU12
BT14	VSS	VSS	BU13
BT15	VSS	VSS	BU14
BT16	VSS	VSS	BU15
BT17	VSS	VSS	BU16
BT18	VSS	VSS	BU17
BT19	VSS	VSS	BU18
BT20	VSS	VSS	BU19
BT21	VSS	VSS	BU20
BT22	VSS	VSS	BU21
BT23	VSS	VSS	BU22
BT24	VSS	VSS	BU23
BT25	VSS	VSS	BU24
BT26	VSS	VSS	BU25

OMIT_TABLE
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PALMA_CGA
BGA
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BU26	VSS	VSS	BU67
BU27	VSS	VSS	BU68
BU28	VSS	VSS	BU69
BU29	VSS	VSS	BU70
BU30	VSS	VSS	BU71
BU31	VSS	VSS	BU72
BU32	VSS	VSS	BU73
BU33	VSS	VSS	BU74
BU34	VSS	VSS	BU75
BU35	VSS	VSS	BU76
BU36	VSS	VSS	BU77
BU37	VSS	VSS	BU78
BU38	VSS	VSS	BU79
BU39	VSS	VSS	BU80
BU40	VSS	VSS	BU81
BU41	VSS	VSS	BU82
BU42	VSS	VSS	BU83
BU43	VSS	VSS	BU84
BU44	VSS	VSS	BU86
BU45	VSS	VSS	
BU46	VSS	VSS	
BU47	VSS	VSS	
BU48	VSS	VSS	
BU49	VSS	VSS	
BU50	VSS	VSS	
BU51	VSS	VSS	
BU52	VSS	VSS	
BU53	VSS	VSS	
BU54	VSS	VSS	
BU55	VSS	VSS	
BU56	VSS	VSS	
BU57	VSS	VSS	
BU58	VSS	VSS	
BU59	VSS	VSS	
BU60	VSS	VSS	
BU61	VSS	VSS	
BU62	VSS	VSS	
BU63	VSS	VSS	
BU64	VSS	VSS	
BU65	VSS	VSS	
BU66	VSS	VSS	

VSS_DDR_SENSE	AD29	VSNS_PVSSDDR_SENSE
VSS_GPU0_SENSE	AR26	VSNS_PVDDGPU0_SENSE_N
VSS_PCPU0_SENSE	P23	VSNS_PVDDPCPU0_SENSE_N
VSS_SENSE1	G12	VSNS_PVDD2H0_SENSE1_N
VSS_SENSE2	G74	VSNS_PVDD2H1_SENSE2_N
VSS_SENSE3	AL16	VSNS_PVDD2H0_SENSE3_N
VSS_SENSE4	AL71	VSNS_PVDD2H1_SENSE4_N

OUT 11
OUT 11 143
OUT 11 143
OUT 11
OUT 11
OUT 11
OUT 11

VSS_DDR_SENSE is a shared VSS for DCS/VDDQ/AMPH VSENSE

BOM_COST_GROUP=SOC

PAGE TITLE
SOC: GND-3

Apple Inc.

DRAWING NUMBER 051-08286
SIZE D
REVISION 5.0.3
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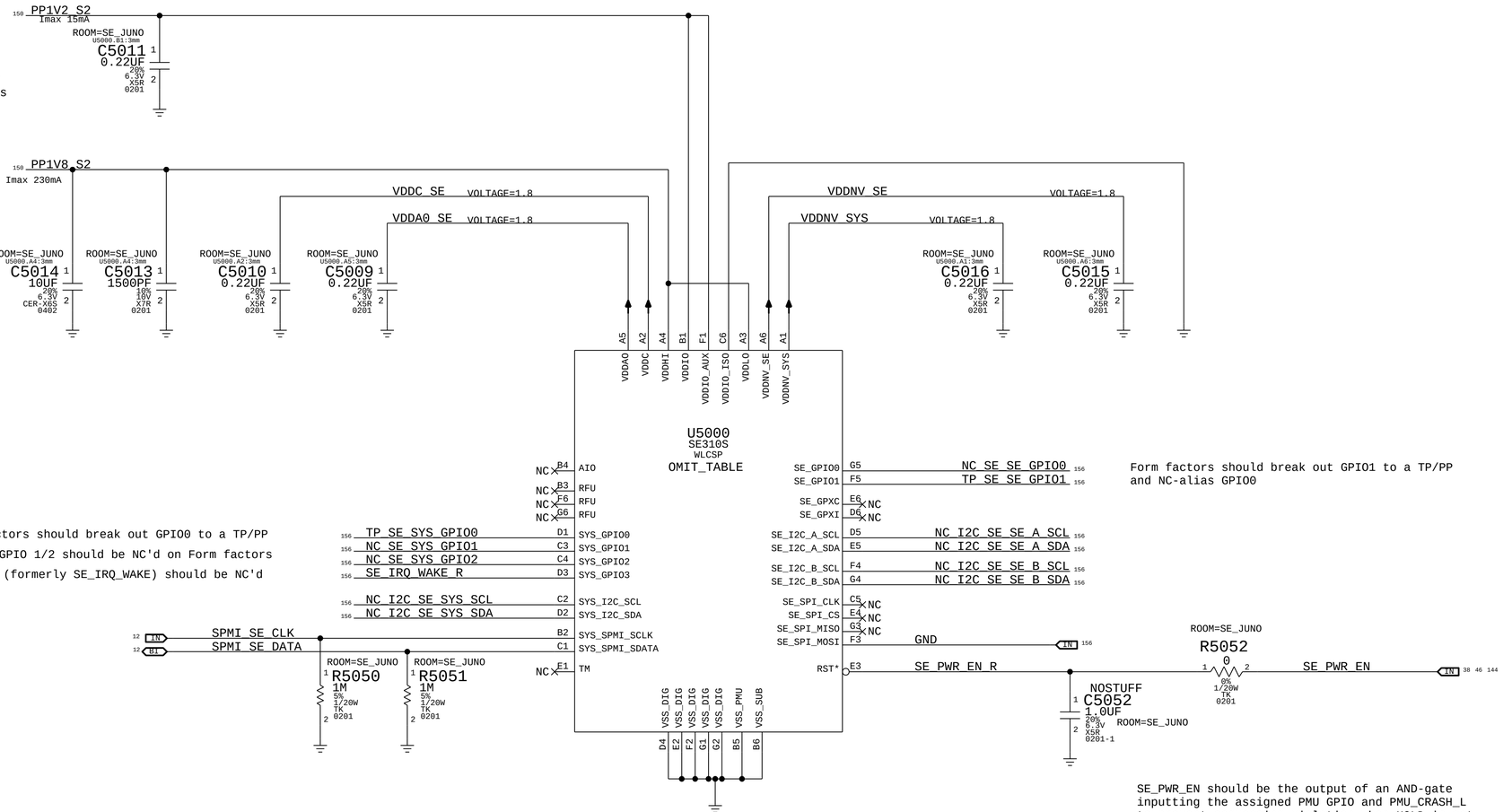
Juno - Secure Element

AONSW nets will connect to either AON LDOs or dedicated AONSW rails. Consult power arch docs to determine appropriate connectivity.



Form factors should break out GPIO0 to a TP/PP
GPIO 1/2 should be NC'd on Form factors
=SE_SYS_GPIO3 (formerly SE_IRQ_WAKE) should be NC'd

Form factors should break out GPIO1 to a TP/PP and NC-alias GPIO0

SE_PWR_EN should be the output of an AND-gate inputting the assigned PMU GPIO and PMU_CRASH_L to prevent sequencing violation when HOLD is set

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
338S00941	1	IC,JUNO,SE310S,A0,DEV,10C,WLCSP42	U5000	JUNO:A0_DEV
338S00956	1	IC,JUNO,SE310S,A0,PROD,1PB,WLCSP42	U5000	JUNO:A0_PROD
338S01012	1	IC,JUNO,SE310S,A0,DEV,10C1,WLCSP42	U5000	JUNO:A0_DEV_DLY
338S01013	1	IC,JUNO,SE310S,A0,PROD,1PB1,WLCSP42	U5000	JUNO:A0_PROD_DLY

<rdar://problem/89368110> [SE310S] Data Sheet
<rdar://problem/90105225> [SE310S] Juno Reference Schematic

BOM_COST_GROUP=SECURE ELEMENT

PAGE TITLE: Secure Element

Apple Inc.

DRAWING NUMBER: 051-08286 SIZE: D
REVISION: 5.0.3
BRANCH:
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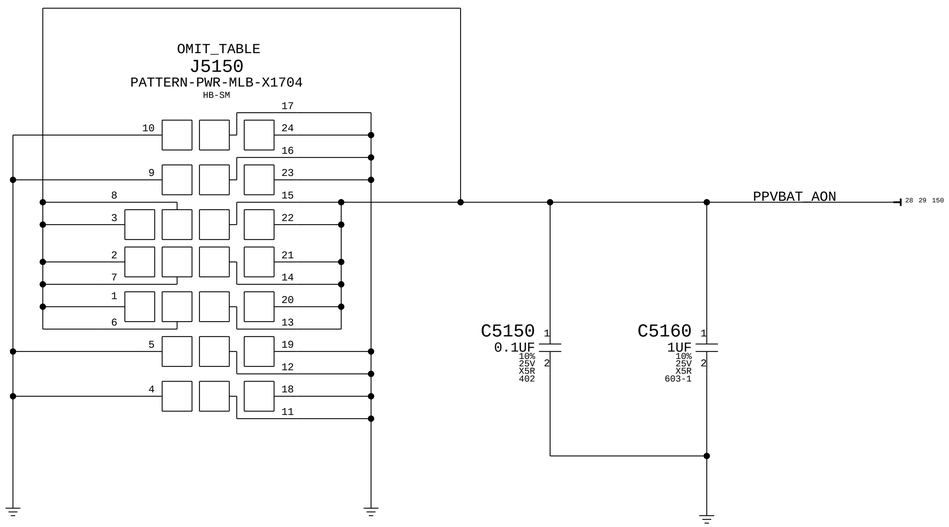
Battery Sub-System Debug Connector

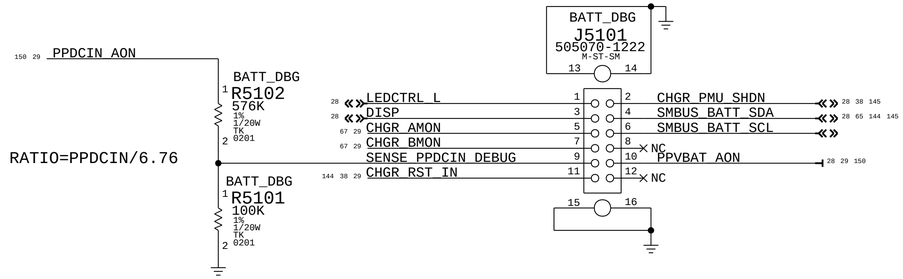
ARKANOID CONN

BMU POWER FLEX HOTBAR'd TO THE MLB:

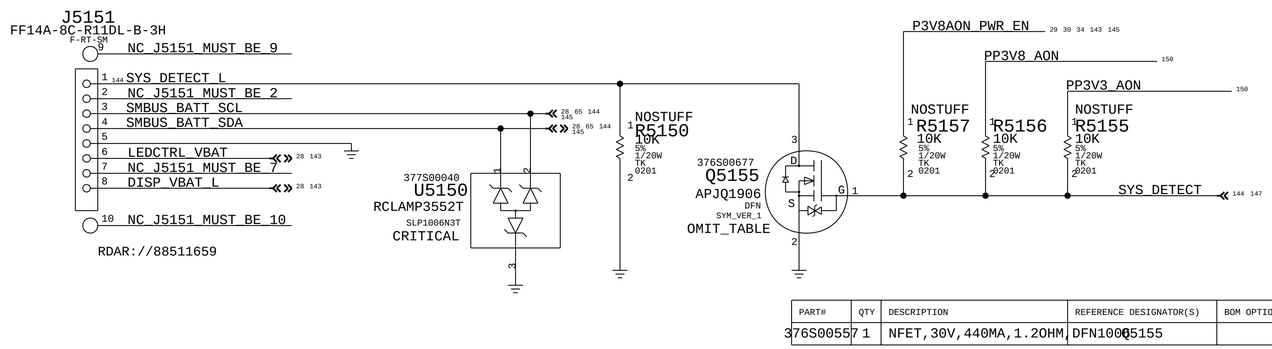
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
632-04146	1	PCBA,FLEX,BMU-POWER,X1703	J5150	CRITICAL	

ARKANOID	MLB Connector / Signals		Saleae
J0301 - 1	6	SMBUS_BATT_SCL (= I2C_SMC_PWR_SCL)	0
J0301 - 3	4	SMBUS_BATT_SDA (= I2C_SMC_PWR_SDA)	1
J0301 - 5	2	CHGR_PMU_SHDN	2
J0301 - 7	1	LEDCTRL_L	3
J0302 - 1	3	DISP	4
J0302 - 3	5	CHGR_AMON	5
J0302 - 5	7	CHGR_BMON	6
J0302 - 7	9	1 / 6.76 * PPDCIN_AON	7
J0303 - 1	11	CHGR_RST_IN	8
J0303 - 3	12	—	9
J0303 - 5	10	PPVBAT_AON	10
J0303 - 7	8	—	11

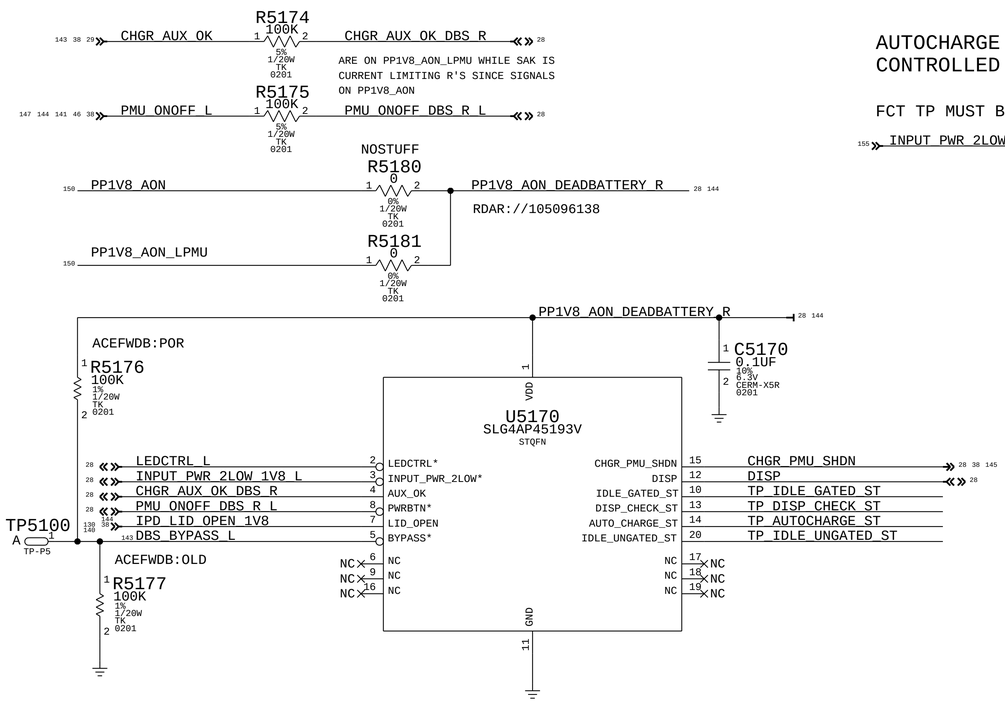


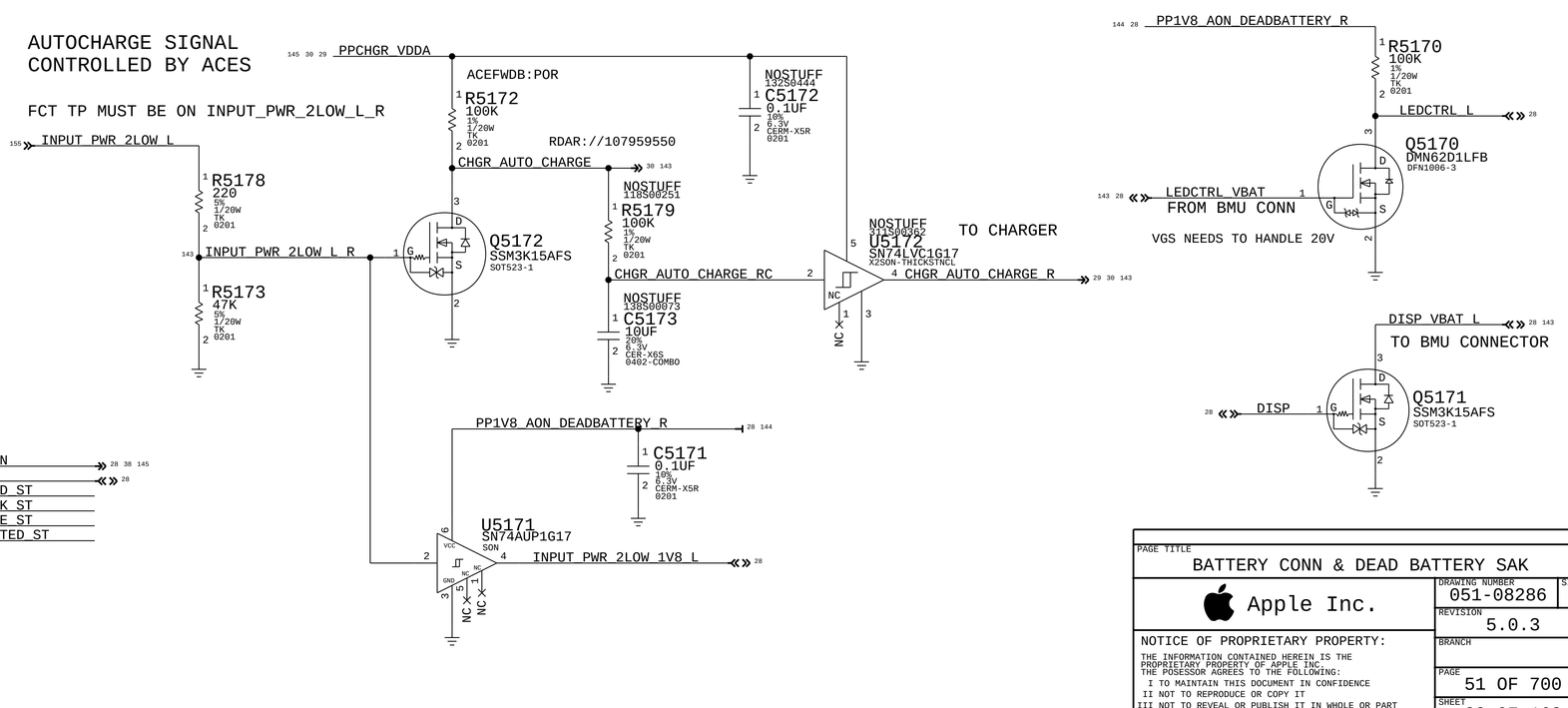


MLB CONNECTOR APN# 518S00164



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
376S00557	1	NFET,30V,440MA,1.2OHM,DFN1006	Q5155	





BOM_COST_GROUP=BATTERY

PAGE TITLE: BATTERY CONN & DEAD BATTERY SAK

Apple Inc.

DRAWING NUMBER: 051-08286 SIZE: D

REVISION: 5.0.3

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*** OK2PLACE ***

PPDCIN_AON_CHGR_R

C5201 CRITICAL 10UF 20% 50V TANT-POLY 7343-31 CAPMAT=POLY-TANT
C5202 CRITICAL 10UF 20% 50V TANT-POLY 7343-31 CAPMAT=POLY-TANT
C5203 CRITICAL 10UF 20% 50V TANT-POLY 7343-31 CAPMAT=POLY-TANT
C520A 0.1UF 10% 50V CERM-X7R 0402
C520B 0.1UF 10% 50V CERM-X7R 0402
C520C 0.1UF 10% 50V CERM-X7R 0402
C520D 0.1UF 10% 50V CERM-X7R 0402
C520E 0.1UF 10% 50V CERM-X7R 0402

MIN_NECK_WIDTH=0.1500
MIN_LINE_WIDTH=0.6000

C5204 CRITICAL 10UF 20% 50V TANT-POLY 7343-31 CAPMAT=POLY-TANT
C5205 CRITICAL 10UF 20% 50V TANT-POLY 7343-31 CAPMAT=POLY-TANT
C520F 0.1UF 10% 50V CERM-X7R 0402
C520G 0.1UF 10% 50V CERM-X7R 0402
C520H 0.1UF 10% 50V CERM-X7R 0402

VOLTAGE=28V

L5230 1UH-20%-23A-0.00290HM PIMB103E-SM CRITICAL
L5231 1UH-20%-23A-0.00290HM PIMB103E-SM CRITICAL

CKPLUS_WAIVE=CAPDERATE

C5250 CRITICAL 27UF 20% 18V TANT-POLY CASE-B12
C5251 CRITICAL 27UF 20% 18V TANT-POLY CASE-B12
C5252 CRITICAL 27UF 20% 18V TANT-POLY CASE-B12
C5253 CRITICAL 27UF 20% 18V TANT-POLY CASE-B12
C5254 CRITICAL 27UF 20% 18V TANT-POLY CASE-B12
C5255 CRITICAL 27UF 20% 18V TANT-POLY CASE-B12
C5256 CRITICAL 27UF 20% 18V TANT-POLY CASE-B12
C5257 CRITICAL 27UF 20% 18V TANT-POLY CASE-B12

27UF_CAPS
PACK_OPTION=27UF_CAPS

PACK_IGNORE=TRUE
PACK_OPTION=33UF_CAPS

C5250 CRITICAL 33UF 20% 16V TANT CASE-T
C5251 CRITICAL 33UF 20% 16V TANT CASE-T
C5252 CRITICAL 33UF 20% 16V TANT CASE-T
C5253 CRITICAL 33UF 20% 16V TANT CASE-T
C5254 CRITICAL 33UF 20% 16V TANT CASE-T
C5255 CRITICAL 33UF 20% 16V TANT CASE-T
C5256 CRITICAL 33UF 20% 16V TANT CASE-T
C5257 CRITICAL 33UF 20% 16V TANT CASE-T

33UF_CAPS

107S00044
NO_XNET_CONNECTION=1
R5220 CRITICAL 0.01 0.5% 1W MF 0612-1-COMBO
(AMON) 2-CELL: 0.02 OHM 3-CELL: 0.01 OHM

FROM USB-C SOURCE
PPDCIN_AON

C5208 2.2UF 10% 50V X5R 0603
C5209 2.2UF 10% 50V X5R 0603
C5206 CRITICAL 10UF 20% 50V TANT-POLY 7343-31 CAPMAT=POLY-TANT
C5207 CRITICAL 10UF 20% 50V TANT-POLY 7343-31 CAPMAT=POLY-TANT

Q5230 CRITICAL NTMFS5H431NL DFN-COMBO-1
Q5231 CRITICAL NTMFS5H431NL DFN-COMBO-1

Q5240 SIZF5300DT POWERPAIR-3X3--THICKSTNGL

TO SYSTEM
PPBUS_AON

C5290 CRITICAL 2.2UF 20% 25V X5R 0402-1
C5291 CRITICAL 2.2UF 20% 25V X5R 0402-1
C5292 1000PF 10% 25V X7R 0201

Consult DCDC DRI before removing PP

PP5201 P2MM SM CHGR_GATE_Q1
PP5202 P2MM SM CHGR_GATE_Q2
PP5203 P2MM SM CHGR_GATE_Q3
PP5204 P2MM SM CHGR_GATE_Q4
PP5205 P2MM SM CHGR_PHASE1
PP5206 P2MM SM CHGR_PHASE2
PP5207 P2MM SM P3V8AON_PWR_EN
PP5208 P2MM SM CHGR_INT_1V8_L
PP5211 P2MM SM PLACE_SIDE=BOTTOM
PP5212 P2MM SM PLACE_SIDE=BOTTOM
PP5213 P2MM SM PLACE_SIDE=BOTTOM
PP5214 P2MM SM PLACE_SIDE=BOTTOM
PP5215 P2MM SM PLACE_SIDE=BOTTOM
PP5216 P2MM SM PLACE_SIDE=BOTTOM
PLACE_SIDE=TOP

CHGR_CSI_P
CHGR_CSI_N
PLACE_NEAR=U5200.D5:2MM
PLACE_NEAR=U5200.C5:2MM
R5221 1 1% 1/20W TK 0201
R5222 1 1% 1/20W TK 0201
CHGR_CSI_FILT_P
CHGR_CSI_FILT_N
C5221 CRITICAL 0.1UF 10% 25V CERM-X7R 0402
C5222 CRITICAL 0.047UF 10% 25V CER-X7R 0402
C5220 CRITICAL 0.47UF 20% 4V CERM-X5R-1 201
NO_XNET_CONNECTION=1

PACK_IGNORE=TRUE
PACK_OPTION=WHAMOLA_OPTION:YES
R5200 116S00014 0 5% 1/20W MF 0402
PP5V_CHGR_SW
PP5V_R_CHG
R5275 117S00062 4.7 5% 1/20W TK 0201
R5276 1 117S00109 5% 1/20W TK 0201
VOLTAGE=5V

PPBUS_AON
C5278 2.2UF 20% 35V X5R-CERM 0402
PPCHGR_VDDA
PPCHGR_VDDP
C5275 CRITICAL 2.2UF 20% 25V X5R-CERM 0402-1
C5277 CRITICAL 10UF 20% 25V X5R-CERM 0603
C5223 1.0UF 10% 50V CERM-X7R 0603
PLACE_NEAR=U5200.B5:5MM

U5200 RAA489901 WLCSP 998-28081 CRITICAL
OMIT_TABLE

B5	P_IN	GATE_Q1	H1
C5	CSIN	BOOT1	F1
D5	CSIP	LX1	G1
A5	PBUS_PWR	GATE_Q2	E1
D3	AUX_DET	GATE_Q3	D1
		LX2	B1
		BOOT2	C1
		GATE_Q4	A1
		PBUS_Q4SNS	A3
		CSOP	A4
		CSON	B4
		BGATE	B3
		VBAT	C3
		EN_VR1	F2
		SMC_RST*	H4
		IRQ*	H3
		TEST	H2
		(5V) EN_MVR	F4
		(OD) AUX_OK	F3
		AMON	D4
		BMON	C4
F5	VDDIO1P8		
G5	SDA		
H5	SCL		
G2	SMC_RST_IN		
G3	HPWR_EN*		
E5	COMP		
G4	CELL		
B2	AUTO_CHARGE		
C2	SYS_5V		
E4	AUX_SHORT		
E3	AGND		
E2	PGND		

CHGR_GATE_Q1 DIDT=TRUE SWITCH_NODE=TRUE
CHGR_GATE_Q2 DIDT=TRUE GATE_NODE=TRUE
CHGR_GATE_Q3 GATE_NODE=TRUE DIDT=TRUE
CHGR_BOOT2 SWITCH_NODE=TRUE DIDT=TRUE
CHGR_GATE_Q4 DIDT=TRUE GATE_NODE=TRUE
CHGR_PHASE1 DIDT=TRUE SWITCH_NODE=TRUE
CHGR_PHASE2 DIDT=TRUE SWITCH_NODE=TRUE

C5230 CRITICAL 0.1UF 10% 25V X7R-CERM-1 0402
CHGR_BOOT1_RC DIDT=TRUE SWITCH_NODE=TRUE
R5230 0 0% 1/16W TK 0402
CHGR_BOOT1 DIDT=TRUE SWITCH_NODE=TRUE

C5240 CRITICAL 0.1UF 10% 25V X7R-CERM-1 0402
CHGR_BOOT2_RC DIDT=TRUE SWITCH_NODE=TRUE
R5240 0 0% 1/16W TK 0402

CHGR_PBUS_SNS
XW5260 SM PLACE_NEAR=Q5240.1:2MM

(BMON) 2-CELL: 0.010 OHM 3-CELL: 0.005 OHM
NO_XNET_CONNECTION=1
R5265 CRITICAL 107S00392 .01 1% 1.5W MF 0612
CHGR_CSO1_P CHGR_CSO1_N
R5260 CRITICAL 107S00392 .01 1% 1.5W MF 0612
CHGR_CSO_P CHGR_CSO_N
R5261 2 1% 1/20W TK 0201
R5262 2 1% 1/20W TK 0201
PLACE_NEAR=U5200.A4:2MM
PLACE_NEAR=U5200.B4:2MM
MIN_NECK_WIDTH=0.6000
MIN_LINE_WIDTH=0.1500
R5291 0 0% 1/10W TK 0201
R5266 2 1% 1/20W TK 0201
R5267 2 1% 1/20W TK 0201
CHGR_CSO_FILT_P CHGR_CSO_FILT_N
C5261 CRITICAL 0.047UF 10% 50V CER-X7R 0402
C5262 CRITICAL 0.047UF 10% 50V CER-X7R 0402
C5260 CRITICAL 0.47UF 20% 4V CERM-X5R-1 201
NO_XNET_CONNECTION=1

PPVBAT_AON_CHGR_R
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1500

C5265 CRITICAL 2.2UF 20% 25V X5R 0402-1
C5266 CRITICAL 2.2UF 20% 25V X5R 0402-1
C5267 CRITICAL 0.1UF 10% 25V X5R 0201
C5268 0.01UF 10% 25V X5R-CERM 0201

Q5265 CRITICAL SI7137DP SO-8-COMBO
C5264 1000PF 10% 25V X7R 0201
VOLTAGE=13.2V

TO/FROM BATTERY
PPVBAT_AON
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
VOLTAGE=13.2V

C5269 0.1UF 10% 25V X5R 0201
C5263 4700PF 10% 25V CER-X5R 0201-1

XW5263 SM PLACE_NEAR=J5150:5MM
CHGR_VBAT_XW
<RDAR://37259372&39763505&84523221>

Q5270 NTNS4CS69N XDFN SYM_VER_1
PACK_IGNORE=TRUE WHAMOLA_OPTION:YES

PPDCIN_AON
R5271 118S00364 200K 1% 1/20W TK 0201
SAVE_BAT_S
SAVE_BAT_G
R5263 1K 5% 1/20W TK 0201-1
R5270 117S00119 24K 5% 1/20W TK 0201
D5270 CRITICAL 371S00307 DZD5V6L2P3-55 SOD-923-2 ALLOW_APPLE_PREFIX=D

PACK_IGNORE=TRUE WHAMOLA_OPTION:YES

Q5216 SSM3K15AFS SOT523-1
R5217 10K 1% 1/20W TK 0201
PACK_IGNORE=TRUE PACK_OPTION=WHAMOLA_OPTION:YES

C5280 1.0UF 20% 6.3V X5R 0201-1
I2C_SMC_PWR_1V8_SDA
I2C_SMC_PWR_1V8_SCL
CHGR_RST_IN
GND
CHGR_COMP
H:3-CELL L:2-CELL

CRITICAL C5270 0.12UF 10% 10V X5R 0402
CRITICAL C5271 0.12UF 10% 10V X5R 0402
CHGR_AUTO_CHARGE_R
PP5V_CHGR_VDDA_R
AUX_DET_SHORT_R
C5279 2.2UF 20% 25V X5R-CERM 0402-1
OMIT_TABLE
R5201 10K 1% 1/20W TK 0201
Mandola has a 200K ohm pull-down on AUX_SHORT

R5290 0 0% 1/20W TK 0201
CHGR_AUX_DET_SHORT

R5215 787K 1% 1/20W TK 0201
CHGR_AUX_DET
NOSTUFF C5216 0.01UF 10% 25V X5R-CERM 0201
R5216 158K 1% 1/20W TK 0201

Whamola ID Register 0xFF => 0x001C

BOM_COST_GROUP=BATTERY

PAGE TITLE	CHARGER:MANDOLA
Apple Inc.	DRAWING NUMBER 051-08286 SIZE D
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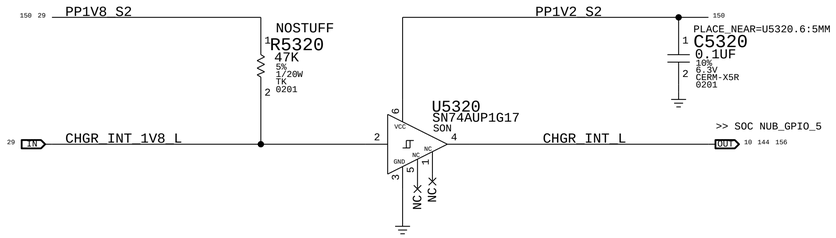
*** OK2PLACE ***

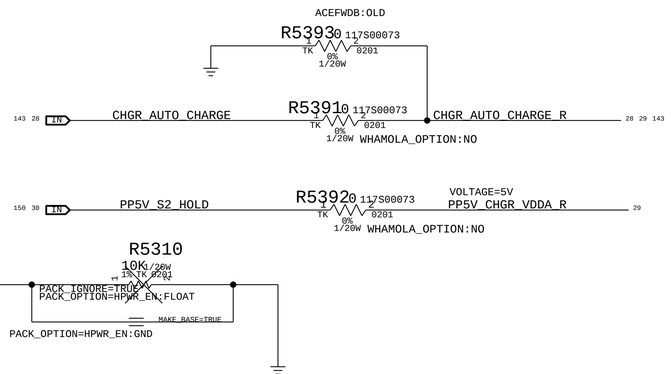
CHGR I2C Level Translation

SMBUS_CHGR_1V8_[SCL/SDA]: Level translation circuit to be placed in project specific I2C page.

CHGR_INT_L Level Translation

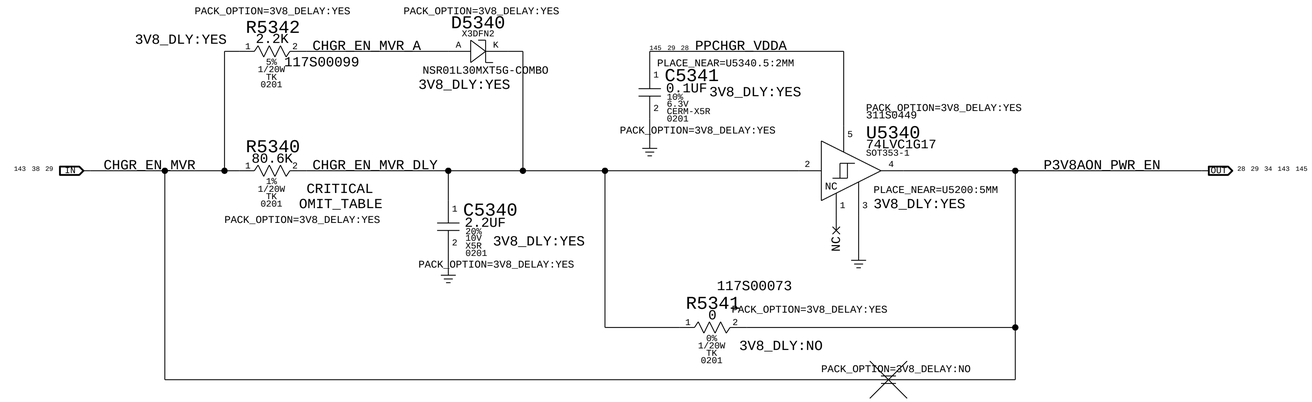
Stuff R5320 in case, glitch during power sequencing is a concern.





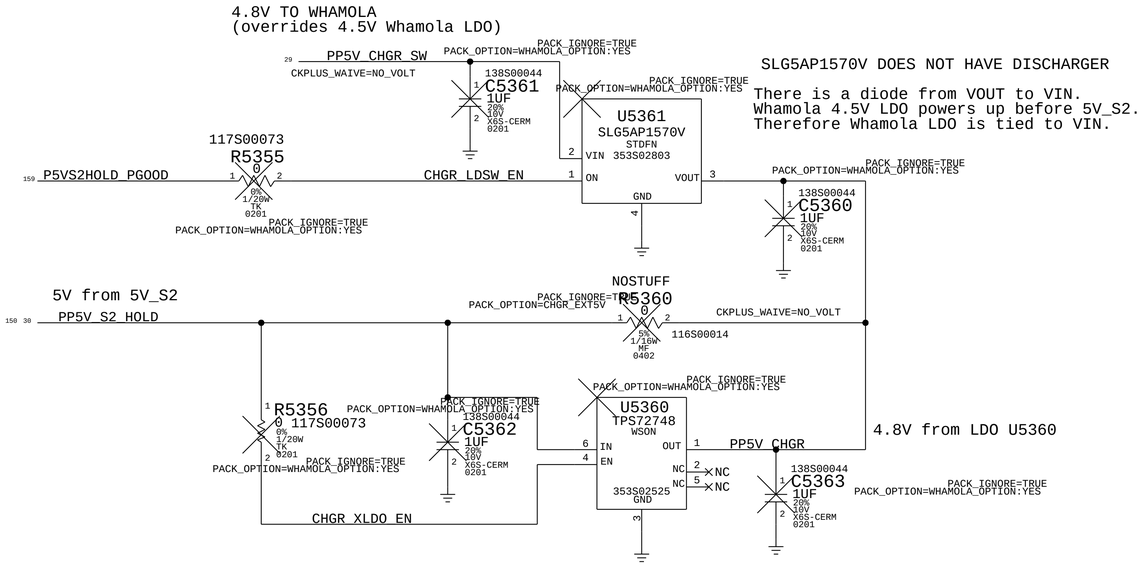
DELAY FOR 3.8V VR ENABLE

R5340 and C5340 updated per rdar://62686034



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
118S00505	1	RES,TK,80.6KOHM,1%,1/20W,0201	R5340	CRITICAL	3V8_DLY:YES
117S0201	1	RES,MF,1A MAX,0.0 OHM,5%,0201,BLACK	R5340	CRITICAL	3V8_DLY:NO

SWITCHOVER TO EXTERNAL 5V



BOM_COST_GROUP=BATTERY

PAGE TITLE: CHARGER:SUPPORT

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DRAWING NUMBER: 051-08286 SIZE: D
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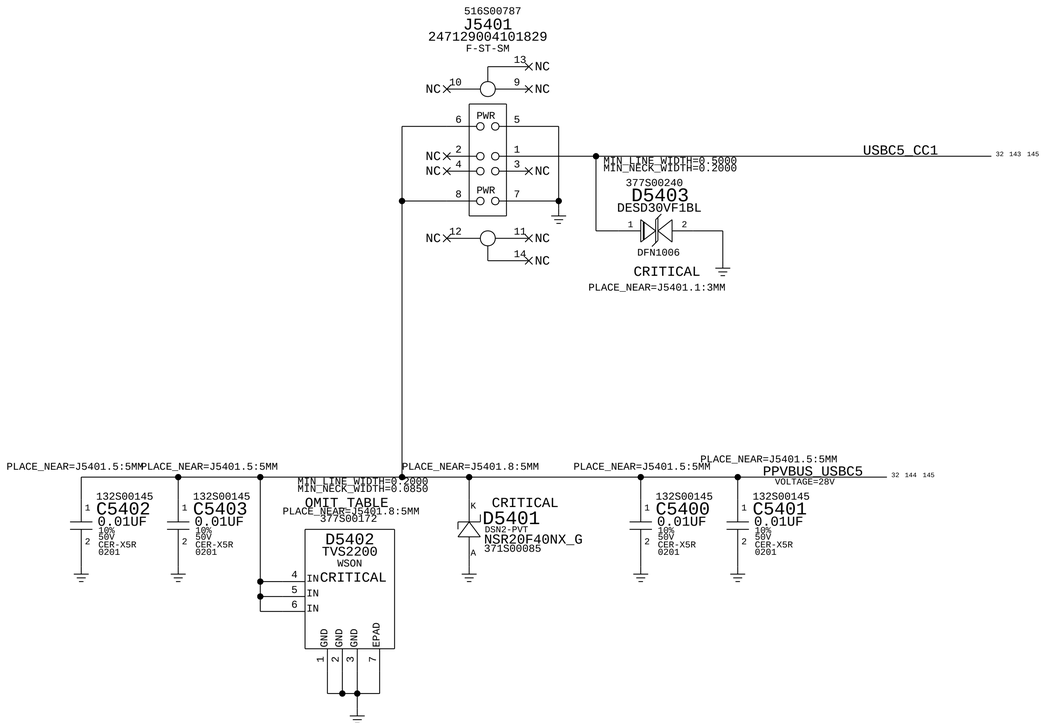
** OK2PLACE **

MAGSAFE B2B connector and VBUS protection



TVS PROTECTION

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
377S00172	1	IC,TVS,UNIDIR,22VRWM,28VCL@40A,2X2,SON6	D5402	ACE3:20V
377S00251	1	IC,TVS,UNIDIR,33VRWM,40VCL@35A,2X2,SON6	D5402	ACE3:28V

BOM_COST_GROUP=MAGSAFE

PAGE TITLE: MAGSAFE: CONNECTOR

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REVISION: 5.0.3

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*** IN PROGRESS ***

33 PPHV_INT5_AONSW
MAX 100uF TOTAL ON RAIL

ACE5_VCONN
ACE5_VCONN

R5500 1K 1% 1/16W TK 0402
VOLTAGE=0V MAKE_BASE=TRUE
ACE5_VCONN MAKE_BASE=TRUE

PP_5V0 PP_CABLE PP_HV VBUS

PPVBUS_USBC5 31 144 145
C5501 1UF 20% 50V X5R 0402

PP3V3_S2 150
C5500 10UF 20% 6.3V CERM 0402

PP1V2_S2 33 150
C5502 1.0UF 20% 6.3V X5R 0201-1
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.0750
VOLTAGE=3.3V

PP3V3_UPC5_LDO 32 33
C5503 10UF 20% 6.3V CERM 0402
C5504 10UF 20% 6.3V CERM 0402

Either a Testpoint or Arkanoid connector
must be present for GPIO0
(EVEN IN PRODUCTION)

1M R5501 1% 1/20W TK 0201 — PD_UART_UPC5_RX_TX 32
100K R5502 5% 1/20W TK 0201 — PD_UPC5_MRESET 32 145
100K R5503 5% 1/20W TK 0201 — PD_UPC5_HPD 32
100K R5521 5% 1/20W TK 0201 — UPC5_GPIO21 32
100K R5522 5% 1/20W TK 0201 — UPC5_GPIO18 32
MAKE_BASE=TRUE

GND 32
PACK_OPTION=UPC5_STRAP3:GND
NOSTUFF
0 R5515 0% 1/20W TK 0201 — UPC5_STRAP3_I2C_ADDR0 32
PACK_OPTION=UPC5_STRAP3:RPD
NOSTUFF
140K R5516 1% 1/20W TK 0201 — UPC5_STRAP4_I2C_ADDR1 32
UPC5 ADDRESS: ADDR0=NC ADDR1=NC
GND 32
GND 32
MAKE_BASE=TRUE

USE INTERNAL LAYER
LIMIT BOARD LEAKAGE
R5504 15K 0.1% 1/20W TK 0201
CRITICAL

PP3V3_UPC5_LDO 32 33
1M R5517 1% 1/20W TK 0201 — UPC5_I2CC_SDA 32
1M R5518 1% 1/20W TK 0201 — UPC5_I2CC_SCL 32
NOSTUFF
1.5K R5519 1% 1/20W TK 0201 — I2C_UPC015_3V3_SDA 33 145 155
1.5K R5520 1% 1/20W TK 0201 — I2C_UPC015_3V3_SCL 33 145 155
NOSTUFF

R5505 100K 5% 1/20W TK 0201 — UPC5_RP MAKE_BASE=TRUE
R5506 100K 5% 1/20W TK 0201 — UPC5_AUX MAKE_BASE=TRUE
R5507 100K 5% 1/20W TK 0201 — UPC5_DBG MAKE_BASE=TRUE

U5500
SN2012024
BGA
353S02973
OMIT_TABLE

POWER
DIGITAL CORE I/O & CONTROL
TYPE-C
PORT MUX

M22	HRESET	
H18	GPIO14_MRESET	145 32 PD_UPC5_MRESET
B4	GPIO15_RESETZ	NC_UPC5_RESET_L
F26	GPIO0	145 33 OUT UPC5_SER_DBG
D18	GPIO1	33 BI UPC5_GPIO1
K24	GPIO2	33 BI UPC5_GPIO2
L21	GPIO3	33 BI UPC5_GPIO3
J25	GPIO4	33 BI UPC5_GPIO4
J9	GPIO5	33 BI UPC5_GPIO5
C1	GPIO6	33 BI UPC5_GPIO6
C5	GPIO7	33 BI UPC5_GPIO7
F10	GPIO8	33 BI UPC5_GPIO8
H10	GPIO9	33 BI UPC5_GPIO9
A3	GPIO10	33 BI UPC5_GPIO10
L25	GPIO11	33 BI UPC5_GPIO11
E11	GPIO12	155 BI INPUT_PWR_2LOW_L
M26	GPIO16_DFU_BOOTED_L	33 BI UPC5_GPIO16
G19	GPIO17_FORCE_RST_REQ	33 BI UPC5_GPIO17
L13	GPIO18_LSTXRX	32 UPC5_GPIO18
C3	GPIO19_LSRX	32 UPC5_GPIO18
N23	GPIO20_SS_HOLD	98 OUT UPC5_AUX_DET_SHORT
G25	GPIO21_LSX_DIR	32 UPC5_GPIO21
J17	STRAP0_BUSPOWER	32 GND
L27	STRAP1_I2C_SPMI_SEL	32 GND
J13	STRAP2_DFU_EN	33 IN UPC0_SOC_FORCE_DFU_3V3
M20	STRAP3_I2C_ADDR0	32 UPC5_STRAP3_I2C_ADDR0
N21	STRAP4_I2C_ADDR1	32 UPC5_STRAP4_I2C_ADDR1
J21	STRAP5_VDDIO_CFG	32 GND
B10	R_OSC	UPC5_R_OSC
F14	AID0	NC_UPC5_AID0
G15	AID1	NC_UPC5_AID1
H14	AID2	NC_UPC5_AID2
E15	AID3	NC_UPC5_AID3
A25	I2CC_SDA	32 UPC5_I2CC_SDA
B26	I2CC_SCL	32 UPC5_I2CC_SCL
K28	I2C1_SDA_GPIO23	155 145 33 32 BI I2C_UPC015_3V3_SDA
J27	I2C1_SCL_GPIO22	155 145 33 32 IN I2C_UPC015_3V3_SCL
H26	I2C_IRQ1Z	NC_INT_I2C_UPC5_L
N25	SPMI_I2C2_DATA 1V25	155 BI SPMI_UPC5_DATA
M24	SPMI_I2C2_CLK 1V25	155 IN SPMI_UPC5_CLK
K26	I2C_IRQ2Z	NC_INT_I2C_SMC_UPC5_L
G27	SPI_CLK	33 OUT SPI_UPC5_R_CLK
H28	SPI_COPI	33 OUT SPI_UPC5_R_MOSI
F28	SPI_CIPO	33 IN SPI_UPC5_R_MISO
E27	SPI_CSZ	145 33 OUT SPI_UPC5_R_CS_L
E25	SWD_DATA IPU	33 12 BI SWD_UPC_SWDIO5
E23	SWD_CLK IPU	33 12 BI SWD_UPC_SWCLK5
D28	UART_RX	32 PD_UART_UPC5_RX_TX
C27	UART_TX	
A15	USB_RP1_P	UPC5_RP
B16	USB_RP1_N	UPC5_RP
A17	USB_RP2_P	UPC5_RP
B18	USB_RP2_N	UPC5_RP
A19	USB_RP3_P	UPC5_RP
B20	USB_RP3_N	UPC5_RP
D14	AUX_P	UPC5_AUX
C15	AUX_N	UPC5_AUX
G11	GPIO13_HPDTXRX	32 PD_UPC5_HPD
E19	DEBUG0_GPIO24	UPC5_DBG
F18	DEBUG1_GPIO25	UPC5_DBG
H22	DEBUG2_GPIO26	UPC5_DBG
D22	DEBUG3_GPIO27	UPC5_DBG
G23	DEBUG4_GPIO28	UPC5_DBG
F22	DEBUG5_GPIO29	UPC5_DBG
C23	DEBUG6_GPIO30	UPC5_DBG
D26	DEBUG7_GPIO31	UPC5_DBG

C19	VIN_3V3	
C25	VDDIO	
B22	LDO_3V3	
A23	LDO_1V8	PP1V8_UPC5_LDO
		VOLTAGE=1.8
A27		UPC5_LV
B28	VIN_LV	
B24	VOUT_LV	
A5	SS	UPC5_SS
A21	LDO_CORE	PP1V5_UPC5_LDO_CORE
		VOLTAGE=1.5V MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.0750
M16	C_CC1	USBC5_CC1 MAKE_BASE=TRUE
N15		
M18	C_CC2	USBC5_CC2
N17		CKPLUS_WAIVE=SINGLE_COMP_NET
L17	RPD_G1	USBC5_CC1
L19	RPD_G2	GND MAKE_BASE=TRUE
A11	C_USB_TP	USBC5_WPD
A13	C_USB_TN	USBC5_WPD
B12	C_USB_BP	USBC5_WPD
B14	C_USB_BN	USBC5_WPD
C11	C_SBU1	USBC5_WPD
D10	C_SBU2	USBC5_WPD
B8	3V3 LDCM	NC_USBC5_LDCM
C7	3V3 LDCM_LB	NC_USBC5_LDCM_LB
A7	3V3 LDCM_SENSE	USBC5_LDCM_SENSE
B6	3V3 LDCM_COMP	USBC5_LDCM_COMP
A9	3V3 LDCM_SW	USBC5_LDCM_SW

C5505 10UF 20% 6.3V CERM 0402
C5511 0.68UF 5% 6.3V X6S 0402
MIN_LINE_WIDTH=0.5000
MIN_NECK_WIDTH=0.2000
C5506 220PF 5% 50V C0G 0201-1
R5510 10K 1% 1/16W TK 0402-3 — USBC5_WPD MAKE_BASE=TRUE
R5512 1K 1% 1/20W TK 0201
R5509 10K 1% 1/20W TK 0201
R5508 100K 5% 1/20W TK 0201

GROUND
GND
A1 B2 K16 K20 M28 N19 N27

BOM_COST_GROUP=MAGSAFE

ACE3 PART

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
353S03508	1	IC,SN2012025,ACE3,A1,USBPD W/20HV,BGA149	U5500	ACE3:20V
353S03507	1	IC,SN2012024,ACE3,A1,USBPD W/28HV,BGA149	U5500	ACE3:28V

PAGE TITLE
MAGSAFE: PORT CONTROLLER

Apple Inc.

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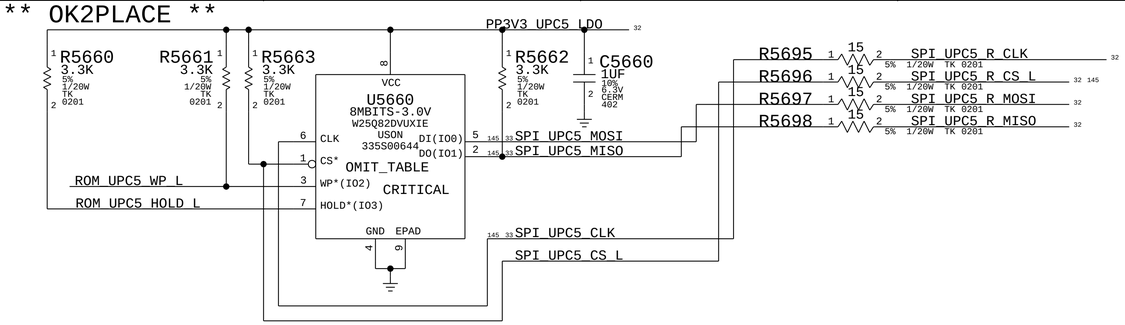
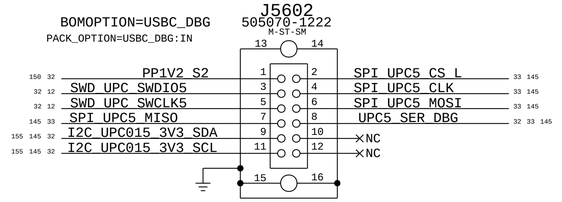
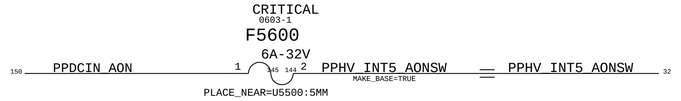


AARDVARKANOID CONN

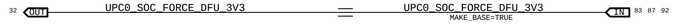


Either a Testpoint or Arkanoid connector
must be present for GPIO0
(EVEN IN PRODUCTION)

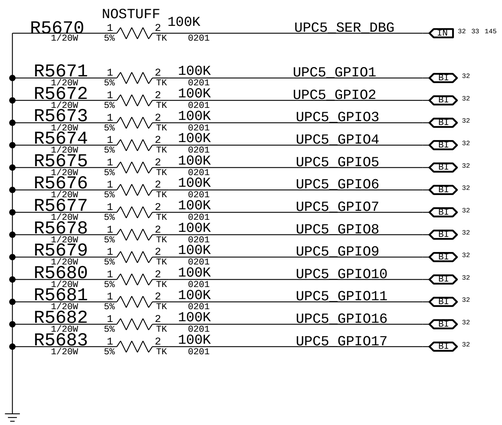
CONNECTION TO DCIN



UPC5 FUSE



Unused ports and GPIOs



BOM_COST_GROUP=MAGSAFE

PAGE TITLE
MAGSAFE: CONTROLLER SUPPORT

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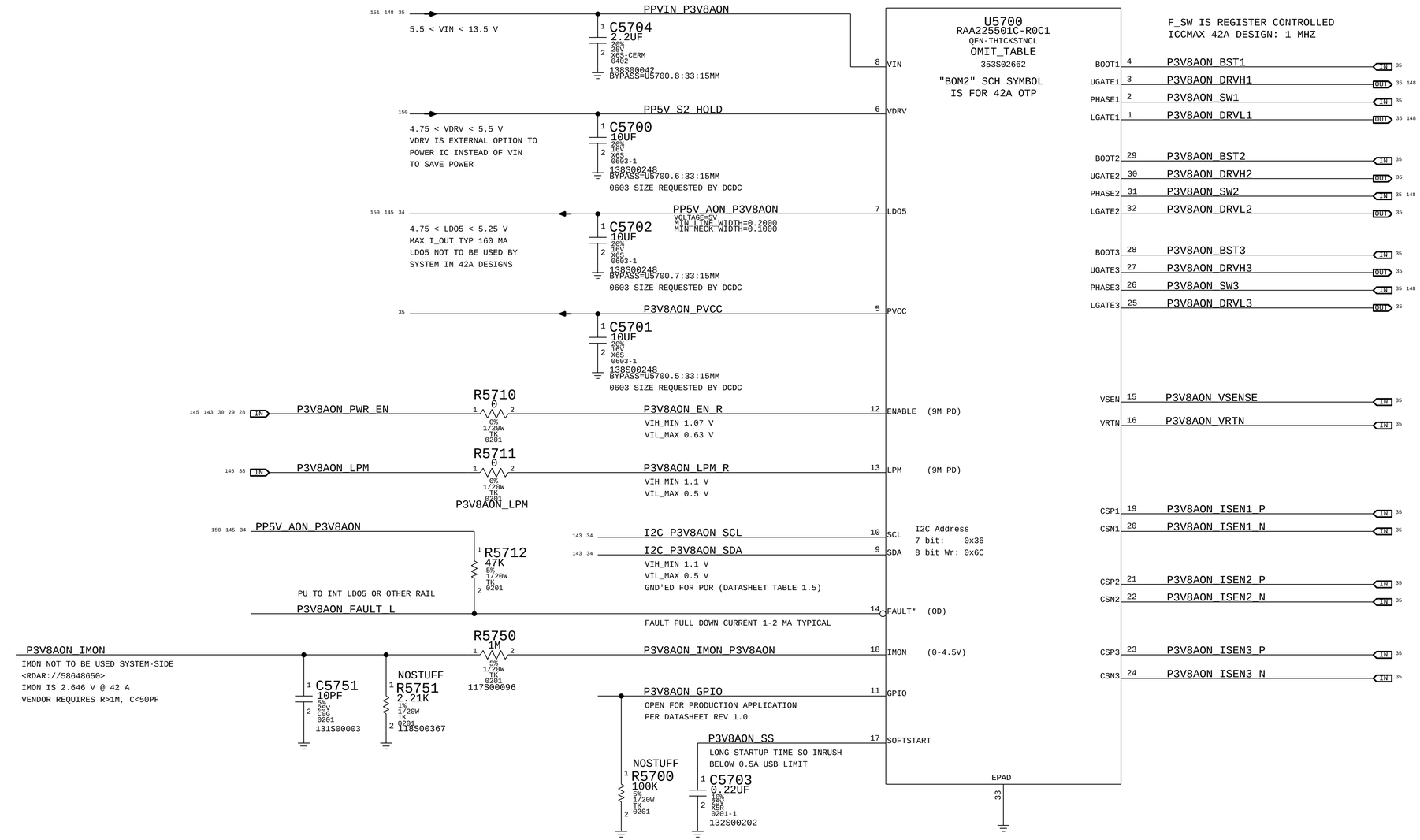
*** OK2INTEGRATE ***

3V8 AON CONTROLLER
42A DESIGN



rdar://70382922 J129: Iceman BOM2 OTP Tracker

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S02662	1	IC,RAA225501B,ICE,BOM2,A2,OTP-R0C1,QFN32	U5700	CRITICAL	P3V8AON_IC:A2_BOM2_R0C1
353S02604	1	IC,RAA225501B,ICE,BOM2,A2,OTP-R0C0,QFN32	U5700	CRITICAL	P3V8AON_IC:A2_BOM2_R0C0
353S02473	1	IC,RAA225501C,ICE,BOM2,A1,OTP-R0C0,QFN32	U5700	CRITICAL	P3V8AON_IC:A1_BOM2_R0C0

BOM_COST_GROUP=SOC POWER

PAGE TITLE: POWER: 3V8 AON (1/2)

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*** OK2INTEGRATE ***

42A DESIGN

PPVIN P3V8AON

P3V8AON_DRVH1 — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, GATE_NODE=TRUE, DIDT=TRUE

R5803 0 NA 0.05W TK 0402-1 116S00021 (3V8_AON_RG402, PACK_IGNORE=TRUE)

R5804 2.2 5% 1/20W TK 0201 117S00116 (3V8_AON_RG201)

R5804 2.2 5% 1/16W TK 0402 116S00043 (3V8_AON_RG402, PACK_IGNORE=TRUE)

P3V8AON_DRVH1_R — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, GATE_NODE=TRUE, DIDT=TRUE

P3V8AON_BST1 — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, DIDT=TRUE, SWITCH_NODE=TRUE

R5803 0 0% 1/20W TK 0201 117S00073 (3V8_AON_RG201)

P3V8AON_BST1_RC — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, DIDT=TRUE, SWITCH_NODE=TRUE

C5811 0.1UF 10% 25V CERM-X7R 0402 132S0578

P3V8AON_SW1 — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, SWITCH_NODE=TRUE, DIDT=TRUE

NOSTUFF D5800 SBR1A30T5 SOD523 (IGNORE=TRUE, PACK_OPTION=3V8_EXT_DIODE)

P3V8AON_PVCC

CRITICAL Q5800 CSD58889Q3D Q3D 376S00012 (VIN, TG, TGR, VSW, BG, PGND)

CRITICAL C5800 33UF 20% 16V TANT CASE-T 128S00009 (OPLUS_WCIVE=CAPEMITE, 3V8_AON_PBUS-16V, PACK_IGNORE=TRUE)

CRITICAL C5801 33UF 20% 16V TANT CASE-T 128S00009

CRITICAL C5800 27UF 20% 18V TANT-POLY CASE-B12 128S00107 (OPLUS_WCIVE=CAPEMITE, 3V8_AON_PBUS-18V)

CRITICAL C5801 27UF 20% 18V TANT-POLY CASE-B12 128S00107

C5804 2.2UF 20% 25V X6S-CERM 0402 138S00042

C5805 2.2UF 20% 25V X6S-CERM 0402 138S00042 (MIRROR_WITH=C5804)

P3V8AON_VSW1

CRITICAL L5800 1UH-20%-11A-0.01270HM PIHA052D-SM 152S00265

PP3V8AON_PH1 — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, VOLTAGE=5V

3V8_AON_RPH1_ORIG — CRITICAL R5800 107S00056 0.003 1% 1/2W MF 0306 (NO_XNET_CONNECTION=1)

PACK_IGNORE=TRUE, 3V8_AON_RPH1_MIRR — CRITICAL R5800 107S00056 0.003 1% 1/2W MF 0306 (NO_XNET_CONNECTION=1)

ICCMAX = 42 A

PP3V8_AON (148 150)

CRITICAL C5890 150UF 20% 6.3V TANT-POLY CASE-B3-1 128S00094 (OPLUS_WCIVE=CAPEMITE)

CRITICAL C5891 150UF 20% 6.3V TANT-POLY CASE-B3-1 128S00094

CRITICAL C5892 150UF 20% 6.3V TANT-POLY CASE-B3-1 128S00094

P3V8AON_DRVL1 — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, GATE_NODE=TRUE, DIDT=TRUE

R5805 1 5% 1/16W TK 0402 116S00025

P3V8AON_DRVL1_R — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, GATE_NODE=TRUE, DIDT=TRUE

R5809 1.5 5% 1/16W TK 0402 116S00026

P3V8AON_SNUB1 — SWITCH_NODE=TRUE, DIDT=TRUE

C5809 150PF 5% 50V C0G-CERM 0402 131S0514

NOSTUFF C5814 220PF 5% 50V C0G 0201-1

C5810 5600PF 10% 10V CERM-X7R 0201 132S0370 (NO_XNET_CONNECTION=1)

R5801 1 1% 1/20W TK 0201 118S00397 — P3V8AON_ISNS1_P

R5802 1 1% 1/20W TK 0201 118S00397 — P3V8AON_ISNS1_N

NOSTUFF C5815 220PF 5% 50V C0G 0201-1

P3V8AON_ISEN1_P

P3V8AON_ISEN1_N

CRITICAL C5893 150UF 20% 6.3V TANT-POLY CASE-B3-1 128S00094

CRITICAL C5894 150UF 20% 6.3V TANT-POLY CASE-B3-1 128S00094

CRITICAL C5895 150UF 20% 6.3V TANT-POLY CASE-B3-1 128S00094

PPVIN P3V8AON

CRITICAL C5820 27UF 20% 18V TANT-POLY CASE-B12 128S00107 (OPLUS_WCIVE=CAPEMITE, 3V8_AON_PBUS-18V)

CRITICAL C5821 27UF 20% 18V TANT-POLY CASE-B12 128S00107

CRITICAL C5822 27UF 20% 18V TANT-POLY CASE-B12 128S00107

CRITICAL C582A 27UF 20% 18V TANT-POLY CASE-B12 128S00107

CRITICAL C582B 27UF 20% 18V TANT-POLY CASE-B12 128S00107

R5824 0 1% 1/5W TK 0603 104S00135

P3V8AON_DRVH2 — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, GATE_NODE=TRUE, DIDT=TRUE

P3V8AON_DRVH2_R — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, GATE_NODE=TRUE, DIDT=TRUE

CRITICAL Q5820 376S00328 SISA14DN-T1-GE3-A PWRPAK-SM-COMBO-2 ALLOW_APPLE_PREFIX=Q

CRITICAL C5820 33UF 20% 16V TANT CASE-T 128S00009 (OPLUS_WCIVE=CAPEMITE, 3V8_AON_PBUS-16V, PACK_IGNORE=TRUE)

CRITICAL C5821 33UF 20% 16V TANT CASE-T 128S00009

CRITICAL C5822 33UF 20% 16V TANT CASE-T 128S00009

CRITICAL C582A 33UF 20% 16V TANT CASE-T 128S00009

CRITICAL C582B 33UF 20% 16V TANT CASE-T 128S00009

C5824 2.2UF 20% 25V X6S-CERM 0402 138S00042

C5825 2.2UF 20% 25V X6S-CERM 0402 138S00042 (MIRROR_WITH=C5824)

CRITICAL C5886 2.2UF 20% 25V X6S-CERM 0402 138S00042 (MIRROR_WITH=C5887)

CRITICAL C5887 2.2UF 20% 25V X6S-CERM 0402 138S00042

CRITICAL C5888 2.2UF 20% 25V X6S-CERM 0402 138S00042 (MIRROR_WITH=C5889)

CRITICAL C5889 2.2UF 20% 25V X6S-CERM 0402 138S00042

CRITICAL C5896 150UF 20% 6.3V TANT-POLY CASE-B3-1 128S00094 (OPLUS_WCIVE=CAPEMITE)

CRITICAL C5897 150UF 20% 6.3V TANT-POLY CASE-B3-1 128S00094

P3V8AON_BST2 — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, DIDT=TRUE, SWITCH_NODE=TRUE

R5823 0 NA 0.05W TK 0402-1 116S00021

P3V8AON_BST2_RC — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, DIDT=TRUE, SWITCH_NODE=TRUE

C5831 0.1UF 10% 25V CERM-X7R 0402 132S0578

P3V8AON_SW2 — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, SWITCH_NODE=TRUE, DIDT=TRUE

NOSTUFF D5820 SBR1A30T5 SOD523 (IGNORE=TRUE, PACK_OPTION=3V8_EXT_DIODE)

P3V8AON_PVCC

CRITICAL Q5821 376S00397 SISS66DN POWERPAK1212-COMBO ALLOW_APPLE_PREFIX=Q

R5825 0 1% 1/5W TK 0603 104S00135

R5826 0 1% 1/5W TK 0603 104S00135

P3V8AON_DRVL2_R — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, GATE_NODE=TRUE, DIDT=TRUE

SAME_SW NET ON BOTH SIDES — P3V8AON_SW2 — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, SWITCH_NODE=TRUE, DIDT=TRUE

R5829 2.2 5% 1/10W TK 0603 — DIDT=TRUE, SWITCH_NODE=TRUE — P3V8AON_SNUB2

NOSTUFF C5829 100PF 5% 50V C0G 0402

CRITICAL L5820 0.4UH-20%-30A-0.0033OHM PILS062D-SM 152S01300

PP3V8AON_PH2 — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, VOLTAGE=5V

3V8_AON_RPH2_ORIG — CRITICAL R5820 107S00011 0.00075 1% 1W MF 0612-1 (NO_XNET_CONNECTION=1)

PACK_IGNORE=TRUE, 3V8_AON_RPH2_MIRR — CRITICAL R5820 107S00011 0.00075 1% 1W MF 0612-1 (NO_XNET_CONNECTION=1)

R5821 1 1% 1/20W TK 0201 118S00397 — P3V8AON_ISNS2_P

R5822 1 1% 1/20W TK 0201 118S00397 — P3V8AON_ISNS2_N

NOSTUFF C5834 220PF 5% 50V C0G 0201-1

C5830 5600PF 10% 10V CERM-X7R 0201 132S0370 (NO_XNET_CONNECTION=1)

NOSTUFF C5835 220PF 5% 50V C0G 0201-1

P3V8AON_ISEN2_P

P3V8AON_ISEN2_N

PPVIN P3V8AON

CRITICAL C5840 27UF 20% 18V TANT-POLY CASE-B12 128S00107 (OPLUS_WCIVE=CAPEMITE, 3V8_AON_PBUS-18V)

CRITICAL C5841 27UF 20% 18V TANT-POLY CASE-B12 128S00107

CRITICAL C5842 27UF 20% 18V TANT-POLY CASE-B12 128S00107

CRITICAL C584A 27UF 20% 18V TANT-POLY CASE-B12 128S00107

CRITICAL C584B 27UF 20% 18V TANT-POLY CASE-B12 128S00107

R5844 0 1% 1/5W TK 0603 104S00135

P3V8AON_DRVH3 — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, GATE_NODE=TRUE, DIDT=TRUE

P3V8AON_DRVH3_R — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, GATE_NODE=TRUE, DIDT=TRUE

CRITICAL Q5840 376S00328 SISA14DN-T1-GE3-A PWRPAK-SM-COMBO-2 ALLOW_APPLE_PREFIX=Q

CRITICAL C5840 33UF 20% 16V TANT CASE-T 128S00009 (OPLUS_WCIVE=CAPEMITE, 3V8_AON_PBUS-16V, PACK_IGNORE=TRUE)

CRITICAL C5841 33UF 20% 16V TANT CASE-T 128S00009

CRITICAL C5842 33UF 20% 16V TANT CASE-T 128S00009

CRITICAL C584A 33UF 20% 16V TANT CASE-T 128S00009

CRITICAL C584B 33UF 20% 16V TANT CASE-T 128S00009

C5844 2.2UF 20% 25V X6S-CERM 0402 138S00042

C5845 2.2UF 20% 25V X6S-CERM 0402 138S00042 (MIRROR_WITH=C5844)

NO_XNET_CONNECTION=1 — XW5870 (SM) — P3V8AON_VSNS_XW_P

R5870 0 0% 1/20W TK 0201 117S00073 (NO_XNET_CONNECTION=1) — P3V8AON_VSENSE

NOSTUFF C5870 1UF 20% 10V X6S-CERM 0201 138S00044 (NO_XNET_CONNECTION=1) — P3V8AON_VRTN

NO_XNET_CONNECTION=1 — XW5871 (SM) — P3V8AON_VSNS_XW_N

R5871 0 0% 1/20W TK 0201 117S00073 (NO_XNET_CONNECTION=1)

P3V8AON_BST3 — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, DIDT=TRUE, SWITCH_NODE=TRUE

R5843 0 NA 0.05W TK 0402-1 116S00021

P3V8AON_BST3_RC — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, DIDT=TRUE, SWITCH_NODE=TRUE

C5851 0.1UF 10% 25V CERM-X7R 0402 132S0578

P3V8AON_SW3 — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, SWITCH_NODE=TRUE, DIDT=TRUE

NOSTUFF D5840 SBR1A30T5 SOD523 (IGNORE=TRUE, PACK_OPTION=3V8_EXT_DIODE)

P3V8AON_PVCC

CRITICAL Q5841 376S00397 SISS66DN POWERPAK1212-COMBO ALLOW_APPLE_PREFIX=Q

R5845 0 1% 1/5W TK 0603 104S00135

R5846 0 1% 1/5W TK 0603 104S00135

P3V8AON_DRVL3_R — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, GATE_NODE=TRUE, DIDT=TRUE

SAME_SW NET ON BOTH SIDES — P3V8AON_SW3 — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, SWITCH_NODE=TRUE, DIDT=TRUE

R5849 2.2 5% 1/10W TK 0603 — DIDT=TRUE, SWITCH_NODE=TRUE — P3V8AON_SNUB3

NOSTUFF C5849 100PF 5% 50V C0G 0402

CRITICAL L5840 0.4UH-20%-30A-0.0033OHM PILS062D-SM 152S01300

PP3V8AON_PH3 — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, VOLTAGE=5V

3V8_AON_RPH3_ORIG — CRITICAL R5840 107S00011 0.00075 1% 1W MF 0612-1 (NO_XNET_CONNECTION=1)

PACK_IGNORE=TRUE, 3V8_AON_RPH3_MIRR — CRITICAL R5840 107S00011 0.00075 1% 1W MF 0612-1 (NO_XNET_CONNECTION=1)

R5841 1 1% 1/20W TK 0201 118S00397 — P3V8AON_ISNS3_P

R5842 1 1% 1/20W TK 0201 118S00397 — P3V8AON_ISNS3_N

NOSTUFF C5854 220PF 5% 50V C0G 0201-1

C5850 5600PF 10% 10V CERM-X7R 0201 132S0370 (NO_XNET_CONNECTION=1)

NOSTUFF C5855 220PF 5% 50V C0G 0201-1

P3V8AON_ISEN3_P

P3V8AON_ISEN3_N

BOM_COST_GROUP=SOC POWER

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PAGE TITLE

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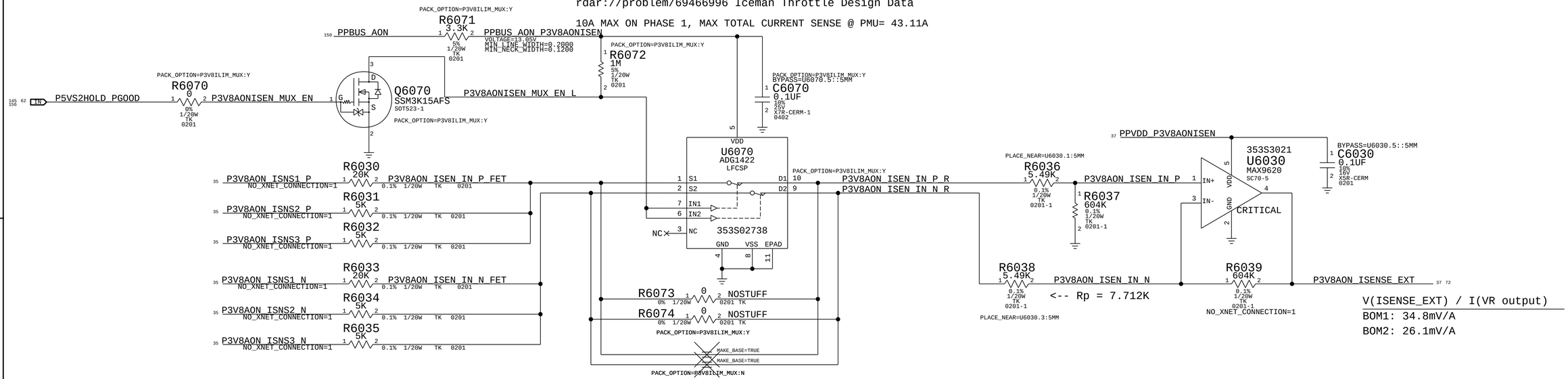
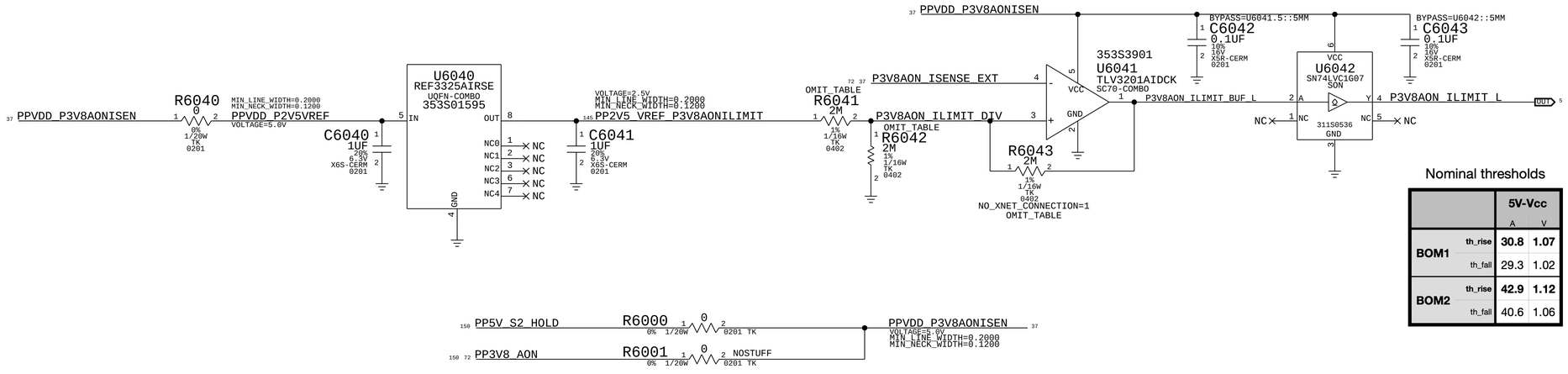
P3V8 LOW SIDE ISENSE AND ILIMIT (SUMMING AMP FOR 3 PHASES)

rdar://problem/69466996 Iceman Throttle Design Data

10A MAX ON PHASE 1, MAX TOTAL CURRENT SENSE @ PMU= 43.11A



PHASE 1 VSENSE GAIN: 8.75
PHASE 2/3 VSENSE GAIN: 35
4:1 WEIGHT FOR PHASE 1 RTREE



Nominal thresholds

		5V-Vcc	
		A	V
BOM1	th_rise	**30.8**	**1.07**
	th_fall	29.3	1.02
BOM2	th_rise	**42.9**	**1.12**
	th_fall	40.6	1.06

Call one of these BOM GROUPs in the main BOM:

BOM GROUP	BOM OPTIONS
P3V8ILIM:BOM1_5V	P3V8ILIM_RT:22K,P3V8ILIM_RB:15K4,P3V8ILIM_RF:866K
P3V8ILIM:BOM2_5V	P3V8ILIM_RT:20K,P3V8ILIM_RB:15K,P3V8ILIM_RF:715K

Don't Call these OPTIONs directly:

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S00178	1	RES,0402,1%,1/16W,20K	R6041	P3V8ILIM_RT:20K
114S00277	1	RES,0402,1%,1/16W,22K	R6041	P3V8ILIM_RT:22K
114S00177	1	RES,0402,1%,1/16W,15K	R6042	P3V8ILIM_RB:15K
114S00201	1	RES,0402,1%,1/16W,15.4K	R6042	P3V8ILIM_RB:15K4
114S00179	1	RES,0402,1%,1/16W,715K	R6043	P3V8ILIM_RF:715K
114S00202	1	RES,0402,1%,1/16W,866K	R6043	P3V8ILIM_RF:866K

BOM_COST_GROUP=SOC POWER

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42 NC_FPMU_GPIO1 ==  MAKE_BASE=TRUE  NC_FPMU_GPIO1
42 NC_FPMU_GPIO2 ==  MAKE_BASE=TRUE  NC_FPMU_GPIO2
42 NC_FPMU_GPIO3 ==  MAKE_BASE=TRUE  NC_FPMU_GPIO3
42 NC_FPMU_GPIO4 ==  MAKE_BASE=TRUE  NC_FPMU_GPIO4
42 NC_FPMU_GPIO5 ==  MAKE_BASE=TRUE  NC_FPMU_GPIO5
42 NC_FPMU_GPIO6 ==  MAKE_BASE=TRUE  NC_FPMU_GPIO6
42 NC_FPMU_GPIO7 ==  MAKE_BASE=TRUE  NC_FPMU_GPIO7
42 NC_FPMU_GPIO8 ==  MAKE_BASE=TRUE  NC_FPMU_GPIO8
42 NC_FPMU_GPIO9 ==  MAKE_BASE=TRUE  NC_FPMU_GPIO9
42 NC_FPMU_GPIO10 ==  MAKE_BASE=TRUE  NC_FPMU_GPIO10
42 NC_FPMU_GPIO11 ==  MAKE_BASE=TRUE  NC_FPMU_GPIO11

42 NC_FPMU_GPIO13 ==  MAKE_BASE=TRUE  NC_FPMU_GPIO13
42 NC_FPMU_GPIO14 ==  MAKE_BASE=TRUE  NC_FPMU_GPIO14
42 NC_FPMU_GPIO15 ==  MAKE_BASE=TRUE  NC_FPMU_GPIO15
42 NC_FPMU_GPIO16 ==  MAKE_BASE=TRUE  NC_FPMU_GPIO16
42 NC_FPMU_GPIO17 ==  MAKE_BASE=TRUE  NC_FPMU_GPIO17
42 NC_FPMU_GPIO18 ==  MAKE_BASE=TRUE  NC_FPMU_GPIO18
42 NC_FPMU_GPIO19 ==  MAKE_BASE=TRUE  NC_FPMU_GPIO19
42 NC_FPMU_GPIO20 ==  MAKE_BASE=TRUE  NC_FPMU_GPIO20
42 NC_FPMU_GPIO21 ==  MAKE_BASE=TRUE  NC_FPMU_GPIO21
42 NC_FPMU_GPIO22 ==  MAKE_BASE=TRUE  NC_FPMU_GPIO22
42 NC_FPMU_GPIO23 ==  MAKE_BASE=TRUE  NC_FPMU_GPIO23
42 NC_FPMU_GPIO24 ==  MAKE_BASE=TRUE  NC_FPMU_GPIO24
42 NC_FPMU_GPIO27 ==  MAKE_BASE=TRUE  NC_FPMU_GPIO27

46 NC_DP2HDMI_CEC_IRQ ==  MAKE_BASE=TRUE  NC_DP2HDMI_CEC_IRQ
46 NC_LPMU_GPIO8_RSVD ==  MAKE_BASE=TRUE  NC_LPMU_GPIO8_RSVD
46 NC_LPMU_GPIO12_RSVD ==  MAKE_BASE=TRUE  NC_LPMU_GPIO12_RSVD
46 NC_SD_MAIN_PWR_EN ==  MAKE_BASE=TRUE  NC_SD_MAIN_PWR_EN

46 NC_ENET_LOM_RESET ==  MAKE_BASE=TRUE  NC_ENET_LOM_RESET
46 NC_PMU_PSU_12V_PGOOD ==  MAKE_BASE=TRUE  NC_PMU_PSU_12V_PGOOD
46 NC_PMU2_SHDN ==  MAKE_BASE=TRUE  NC_PMU2_SHDN
46 NC_PMU_WAKE2LF ==  MAKE_BASE=TRUE  NC_PMU_WAKE2LF
42 NC_FPMU_AMUX_AY ==  MAKE_BASE=TRUE  NC_FPMU_AMUX_AY
42 NC_FPMU_AMUX_BY ==  MAKE_BASE=TRUE  NC_FPMU_AMUX_BY
46 NC_LPMU_AMUX_AY ==  MAKE_BASE=TRUE  NC_LPMU_AMUX_AY
46 NC_LPMU_AMUX_BY ==  MAKE_BASE=TRUE  NC_LPMU_AMUX_BY
44 NC_LPMU_LDOX_EN ==  MAKE_BASE=TRUE  NC_LPMU_LDOX_EN

46 IPD_LID_OPEN_1V8 ==  MAKE_BASE=TRUE  IPD_LID_OPEN_1V8  IN 28 130 140 144
46 SDCONN_STATE_CHANGE ==  MAKE_BASE=TRUE  SDCONN_STATE_CHANGE  IN 108 144
46 CHGR_AUX_OK ==  MAKE_BASE=TRUE  CHGR_AUX_OK  IN 28 29 143
46 IPD_WAKE_L ==  MAKE_BASE=TRUE  IPD_WAKE_L  IN 139 144
46 SD_PWR_EN ==  MAKE_BASE=TRUE  SD_PWR_EN  OUT 109
46 IPD_PWR_EN ==  MAKE_BASE=TRUE  IPD_PWR_EN  OUT 137 140 145
46 P3V8AON_LPM ==  MAKE_BASE=TRUE  P3V8AON_LPM  OUT 34 38 145
46 LCD_PWR_EN ==  MAKE_BASE=TRUE  LCD_PWR_EN  OUT 126
46 BL_PWR_EN ==  MAKE_BASE=TRUE  BL_PWR_EN  OUT 127 144
46 BL_PMIC_PWR_EN ==  MAKE_BASE=TRUE  BL_PMIC_PWR_EN  OUT 128 144
46 PMU_CLK32K_IPD_R ==  MAKE_BASE=TRUE  PMU_CLK32K_IPD_R  38
40 EDP_BKLT_1V29_EN ==  MAKE_BASE=TRUE  EDP_BKLT_1V29_EN  IN 126 145
144 46 145 P5VS2HOLD_PWR_EN ==  MAKE_BASE=TRUE  P5VS2HOLD_PWR_EN  38
                             ==  P5VS2HOLD_PWR_EN  OUT 62 103 145
```

```
46 IN SGPIO_CLK0_R ── 131S00003 C7400 10PF 5% 25V C0G 0201 ── 2
R7400 10 5% 1/20W TK 0201  PLACE_NEAR=U8100.M11:15MM
SGPIO_SCLK0
R7406 10 5% 1/20W TK 0201  PACK_OPTION=SOC:C  PLACE_NEAR=U9300.A6:15MM  SGPIO_VDDHVR_CLK  OUT 50
R7408 10 5% 1/20W TK 0201  PACK_OPTION=SOC:C  PLACE_NEAR=UA200.L1:15MM  SGPIO_CLVR1_CLK  OUT 57
R7409 10 5% 1/20W TK 0201  PACK_OPTION=SOC:C  PLACE_NEAR=UA300.L1:15MM  SGPIO_CLVR2_CLK  OUT 58
R740B 10 5% 1/20W TK 0201  PACK_OPTION=SOC:C  PLACE_NEAR=UA500.L1:15MM  SGPIO_CLVR4_CLK  OUT 60
R7404 10 5% 1/20W TK 0201  PACK_IGNORE=TRUE  PACK_OPTION=SOC:S  PLACE_NEAR=U7700.M11:15MM  SGPIO_FPMU_CLK  OUT 38 42
R7405 10 5% 1/20W TK 0201  PACK_IGNORE=TRUE  PACK_OPTION=SOC:S  PLACE_NEAR=U9300.A6:15MM  SGPIO_PCPUVR_CLK  OUT

R740F 10 5% 1/20W TK 0201  PACK_OPTION=SOC:C  PLACE_NEAR=U9300.B6:15MM  SGPIO_VDDHVR_DATA  BI 50
R740H 10 5% 1/20W TK 0201  PACK_OPTION=SOC:C  PLACE_NEAR=UA200.K1:15MM  SGPIO_CLVR1_DATA  BI 57
R740I 10 5% 1/20W TK 0201  PACK_OPTION=SOC:C  PLACE_NEAR=UA300.K1:15MM  SGPIO_CLVR2_DATA  BI 58
R740K 10 5% 1/20W TK 0201  PACK_OPTION=SOC:C  PLACE_NEAR=UA500.K1:15MM  SGPIO_CLVR4_DATA  BI 60
R740C 10 5% 1/20W TK 0201  PACK_IGNORE=TRUE  PACK_OPTION=SOC:S  PLACE_NEAR=U7700.L11:15MM  SGPIO_FPMU_DATA  BI 42
R740D 10 5% 1/20W TK 0201  PACK_IGNORE=TRUE  PACK_OPTION=SOC:S  PLACE_NEAR=U9300.B6:15MM  SGPIO_PCPUVR_DATA  BI

46 IN SGPIO_CLK1_R ── 131S00003 C7401 10PF 5% 25V C0G 0201 ── 2
R7401 10 5% 1/20W TK 0201  PLACE_NEAR=U8100.M10:15MM  PACK_OPTION=SOC:C
SGPIO_SCLK1
R7403 10 5% 1/20W TK 0201  PACK_OPTION=SOC:C  PLACE_NEAR=U7700.M11:15MM  SGPIO_FPMU_CLK  OUT 38 42
R7407 10 5% 1/20W TK 0201  PACK_OPTION=SOC:C  PLACE_NEAR=UA100.L1:15MM  SGPIO_CLVR0_CLK  OUT 56
R740A 10 5% 1/20W TK 0201  PACK_OPTION=SOC:C  PLACE_NEAR=UA400.L1:15MM  SGPIO_CLVR3_CLK  OUT 59
R74A1 10 5% 1/20W TK 0201  PACK_IGNORE=TRUE  PACK_OPTION=SOC:S  PLACE_NEAR=U8200.M11:15MM  SGPIO_GPUVR_CLK  OUT

R740G 10 5% 1/20W TK 0201  PACK_OPTION=SOC:C  PLACE_NEAR=UA100.K1:15MM  SGPIO_CLVR0_DATA  BI 56
R740J 10 5% 1/20W TK 0201  PACK_OPTION=SOC:C  PLACE_NEAR=UA400.K1:15MM  SGPIO_CLVR3_DATA  BI 59
R740E 10 5% 1/20W TK 0201  PACK_IGNORE=TRUE  PACK_OPTION=SOC:S  PLACE_NEAR=U9600.B6:15MM  SGPIO_GPUVR_DATA  BI

46 BI SGPIO_DATA_R ── 131S00003 C7402 10PF 5% 25V C0G 0201 ── 2
R7402 10 5% 1/20W TK 0201  PLACE_NEAR=U8100.L11:15MM  SGPIO_DATA
```

```
143 46 44 PP1V2_AON_LPMU ── R7425 10K 5% 1/20W 0201 TK NOSTUFF ── R7420 0 0% 1/20W 0201 TK ── 46 BI LPMU_CRASH0_L
FPMU_CRASH0_L  BI 38 42 145

46 BI LPMU_CRASH1_L ── R7426 10K 5% 1/20W 0201 TK NOSTUFF ── R7421 0 0% 1/20W 0201 TK
VDDHVR_SCRASH_L  BI 50 145

BI LPMU_CRASH2_L ── R7427 1K 5% 1/20W 0201-1 TK NOSTUFF ── R7422 0 0% 1/20W 0201 TK
CLVR_CRASH_L  BI 56 57 58 59 60 145

150 40 38 PP1V8_AON_FPMU
PLACE_NEAR=U7470.5:5MM
C7470 0.1UF 10% 6.3V X5R 0201
IN CHGR_EN_MVR ── 2
U7470 74LVC1617 SOT353-1 311S0449
NC 1 ── NC
5 ── 4 CHGR_EN_MVR_1V8_R
R7470 1K 5% 1/20W 0201-1 TK
CHGR_EN_MVR_1V8 ── R7475 0 0% 1/20W 0201 TK ── FPMU_CRASH1_L  BI 42 145
NOSTUFF R7471 1K 5% 1/20W TK 0201-1

150 40 38 PP1V8_AON_FPMU
C7471 0.1UF 10% 6.3V CERM-X5R 0201  132S0444
BYPASS=U7471::3MM
U7471 SN74AUP1G07 X2SON-THICKSTNCL
VCC  GND  NC ── 1  2 A  Y 4 ── FPMU_CRASH0_L  BI 38 42 145
```

32K Series R values all tbd from SIPI

```
38 IN PMU_CLK32K_IPD_R ── R7413 22 5% 1/20W TK 0201 ── IPD_TOUCH_CLK_CONN  OUT 139
46 IN PMU_CLK32K_SOC_R ── R7412 22 5% 1/20W TK 0201 ── PMU_CLK32K_SOC  OUT 10 143
46 IN PMU_CLK32K_WLBT_R ── R7411 22 5% 1/20W TK 0201 ── PMU_CLK32K_WLBT  OUT 110 111 145
46 IN PMU_CLK32K_CLVR_R ── R7410 22 5% 1/20W TK 0201 ── PMU_CLK32K_CLVR  OUT 56 57 58 59 60 145
PACK_OPTION=SOC:C

46 IN PMU_FORCE_DFU ── R7415 680 5% 1/20W 0201 TK ── PMU_UPC_FORCE_DFU  OUT 143 147 155
```

Series R to allow the debug button to overdrive PMU_FORCE_DFU high

IPD_PWR_EN and P5VS2HOLD_PWR_EN stay high through all Software-controlled Resets
...so IPD rails and PP5V_S2 only disable during ship-mode, and unuexpected resets
(SOCHOT, SPF, astris reset, etc)

```
44 PP3V8_AON_LPMU ==  PP3V8_AON_LPMU  44 46 47 48 151 153
40 PP3V8_AON_FPMU ==  PP3V8_AON_FPMU  38 40 42 43 48 151 153

46 44 NC_LPMU_VLDORTC ==  NC_LPMU_VLDORTC  MAKE_BASE=TRUE
46 44 NC_LPMU_VLDORTC2 ==  NC_LPMU_VLDORTC2  MAKE_BASE=TRUE

40 PP3V8_AON_FPMU ==  PP3V8_AON_FPMU  38 40 42 43 48 151 153
40 NC_FPMU_LDO2 ==  NC_FPMU_LDO2  MAKE_BASE=TRUE
40 PP3V8_AON_FPMU ==  PP3V8_AON_FPMU  38 40 42 43 48 151 153
40 NC_FPMU_LDO4 ==  NC_FPMU_LDO4  MAKE_BASE=TRUE
```

```
150 PP1V8_AON
PLACE_NEAR=U7440.1:5MM
C7440 0.1UF 10% 25V X5R 0201
U7440 SLG4AP43601 STQFN
VDD  GND  BTN1  BTN2  RESET 10 CHGR_RST_IN  OUT 28 29 144
CRITICAL 343S00387
NC NC NC NC NC NC NC NC NC

147 144 141 46 28 IN PMU_ONOFF_L ── R7472 100K 5% 1/20W 0201 TK ── PMU_ONOFF_R_L 3
147 144 137 46 IN PMU_RSLOC_RST_L ── R7473 100K 5% 1/20W 0201 TK ── PMU_RSLOC_RST_R_L 4

145 28 IN CHGR_PMU_SHDN ── 2
U7441 SN74AUP1G32 SOT553
PLACE_NEAR=U7441.1:5MM
C7441 0.1UF 10% 25V X5R 0201
PMU_SHDN_R ── R7441 1K 5% 1/20W TK 0201-1 ── PMU_SHDN  OUT 46 144 147
```

For ICs powered by 3V8 or PBUS (** items are known necessary)

```
145 38 34 P3V8AON_LPM ── R7485 100K 5% 1/20W 0201 TK
144 46 27 SE_PWR_EN ── R7480 47K 5% 1/20W 0201 TK
145 111 110 46 WLBT_PWR_EN ── R7486 100K 5% 1/20W 0201 TK
38 P5VS2HOLD_PWR_EN ── NOSTUFF R7483 100K 5% 1/20W 0201 TK
```

Scrub these APNs as the build approaches

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
998-32235	1	Chapel,Portables,LPMU,OTP-APJ	U8100	CRITICAL	SOC:S
998-32236	1	Chapel,Portables,FPMU,OTP-BPJ	U7700	CRITICAL	SOC:S
998-32237	1	Chapel,Portables,LPMU,OTP-CPJ	U8100	CRITICAL	SOC:C
998-32238	1	Chapel,Portables,FPMU,OTP-DPJ	U7700	CRITICAL	SOC:C

PACK_OPTIONS TO INCLUDE IN NETLIST
PMU_COINCELL:N
PMUOSC:QRTZ
PMU_CFGOTP:GND
VPP:GND
FPMU_SW0
FPMU_LDO3

<- Change :R options to :GND for DVT and beyond
(VPP applies to Spitfire design too)

BOM GROUP	BOM OPTIONS
CHAPEL_PORTABLES	PBUS:3S,PMUOSC:QRTZ

BOM_COST_GROUP=SOC POWER

PAGE TITLE
PMU PROJECT-SPECIFIC SUPPORT

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Desense Caps for every rail

1 set for 1- and 2- phase BUCKs
2 set for 3- and 4- phase BUCKs

LPMU

153 47 45 PPVDD_SOC_S1
0
C7600 1 2 12PF 25V NP0-C0G 5% 0201
C7601 1 2 3.0PF 25V NP0-C0G +/-0.1PF 0201
C7602 1 2 1.8PF 25V C0G +/-0.1PF 201
C7603 1 2 12PF 25V NP0-C0G 5% 0201
C7604 1 2 3.0PF 25V NP0-C0G +/-0.1PF 0201
C7605 1 2 1.8PF 25V C0G +/-0.1PF 201

153 148 47 45 PPVDD_SRAM_S1
1
C7610 1 2 12PF 25V NP0-C0G 5% 0201
C7611 1 2 3.0PF 25V NP0-C0G +/-0.1PF 0201
C7612 1 2 1.8PF 25V C0G +/-0.1PF 201
C7613 1 2 12PF 25V NP0-C0G 5% 0201
C7614 1 2 3.0PF 25V NP0-C0G +/-0.1PF 0201
C7615 1 2 1.8PF 25V C0G +/-0.1PF 201

153 47 45 PPVDD2H1_S2SW
2
C7620 1 2 12PF 25V NP0-C0G 5% 0201
C7621 1 2 3.0PF 25V NP0-C0G +/-0.1PF 0201
C7622 1 2 1.8PF 25V C0G +/-0.1PF 201
C7623 1 2 12PF 25V NP0-C0G 5% 0201
C7624 1 2 3.0PF 25V NP0-C0G +/-0.1PF 0201
C7625 1 2 1.8PF 25V C0G +/-0.1PF 201

153 47 45 PP1V8_S2SW
3
C7630 1 2 12PF 25V NP0-C0G 5% 0201
C7631 1 2 3.0PF 25V NP0-C0G +/-0.1PF 0201
C7632 1 2 1.8PF 25V C0G +/-0.1PF 201

153 150 47 45 PPVDD_ECPU_AWAKESW
PACK_OPTION=LBUCK5:Y
5
C7650 1 2 12PF 25V NP0-C0G 5% 0201
C7651 1 2 3.0PF 25V NP0-C0G +/-0.1PF 0201
C7652 1 2 1.8PF 25V C0G +/-0.1PF 201
C7653 1 2 12PF 25V NP0-C0G 5% 0201
C7654 1 2 3.0PF 25V NP0-C0G +/-0.1PF 0201
C7655 1 2 1.8PF 25V C0G +/-0.1PF 201

153 47 45 PPVDDQ1_S1
6
C7660 1 2 12PF 25V NP0-C0G 5% 0201
C7661 1 2 3.0PF 25V NP0-C0G +/-0.1PF 0201
C7662 1 2 1.8PF 25V C0G +/-0.1PF 201

153 47 45 PPVDD_AMPH1_S2SW
7
C7670 1 2 12PF 25V NP0-C0G 5% 0201
C7671 1 2 3.0PF 25V NP0-C0G +/-0.1PF 0201
C7672 1 2 1.8PF 25V C0G +/-0.1PF 201

153 47 46 PP1V2_S2
8
C7680 1 2 12PF 25V NP0-C0G 5% 0201
C7681 1 2 3.0PF 25V NP0-C0G +/-0.1PF 0201
C7682 1 2 1.8PF 25V C0G +/-0.1PF 201

153 47 46 PPVDD_ECPU_SRAM_AWAKESW
9
C7690 1 2 12PF 25V NP0-C0G 5% 0201
C7691 1 2 3.0PF 25V NP0-C0G +/-0.1PF 0201
C7692 1 2 1.8PF 25V C0G +/-0.1PF 201

153 44 PP1V2_S2SW_CLVR_VDDIO
PACK_OPTION=LPMU_SW2
SW2
C76M0 1 2 12PF 25V NP0-C0G 5% 0201
C76M1 1 2 3.0PF 25V NP0-C0G +/-0.1PF 0201
C76M2 1 2 1.8PF 25V C0G +/-0.1PF 201

FPMU

153 43 41 PPVDD_DCS_S1
0
C76A0 1 2 12PF 25V NP0-C0G 5% 0201
C76A1 1 2 3.0PF 25V NP0-C0G +/-0.1PF 0201
C76A2 1 2 1.8PF 25V C0G +/-0.1PF 201
C76A3 1 2 12PF 25V NP0-C0G 5% 0201
C76A4 1 2 3.0PF 25V NP0-C0G +/-0.1PF 0201
C76A5 1 2 1.8PF 25V C0G +/-0.1PF 201

153 43 41 PPVDD_DISP_EXT_AWAKESW
1
C76B0 1 2 12PF 25V NP0-C0G 5% 0201
C76B1 1 2 3.0PF 25V NP0-C0G +/-0.1PF 0201
C76B2 1 2 1.8PF 25V C0G +/-0.1PF 201
C76B3 1 2 12PF 25V NP0-C0G 5% 0201
C76B4 1 2 3.0PF 25V NP0-C0G +/-0.1PF 0201
C76B5 1 2 1.8PF 25V C0G +/-0.1PF 201

153 43 41 PPVDD2H0_S2SW
2
C76C0 1 2 12PF 25V NP0-C0G 5% 0201
C76C1 1 2 3.0PF 25V NP0-C0G +/-0.1PF 0201
C76C2 1 2 1.8PF 25V C0G +/-0.1PF 201
C76C3 1 2 12PF 25V NP0-C0G 5% 0201
C76C4 1 2 3.0PF 25V NP0-C0G +/-0.1PF 0201
C76C5 1 2 1.8PF 25V C0G +/-0.1PF 201

153 43 41 PP1V8_S2
3
C76D0 1 2 12PF 25V NP0-C0G 5% 0201
C76D1 1 2 3.0PF 25V NP0-C0G +/-0.1PF 0201
C76D2 1 2 1.8PF 25V C0G +/-0.1PF 201

153 43 41 PPVDDQ0_S1
4
C76E0 1 2 12PF 25V NP0-C0G 5% 0201
C76E1 1 2 3.0PF 25V NP0-C0G +/-0.1PF 0201
C76E2 1 2 1.8PF 25V C0G +/-0.1PF 201

153 43 41 PPVDD_DISP_INT_AWAKESW
PACK_OPTION=FBUCK5:Y
5
C76F0 1 2 12PF 25V NP0-C0G 5% 0201
C76F1 1 2 3.0PF 25V NP0-C0G +/-0.1PF 0201
C76F2 1 2 1.8PF 25V C0G +/-0.1PF 201
C76F3 1 2 12PF 25V NP0-C0G 5% 0201
C76F4 1 2 3.0PF 25V NP0-C0G +/-0.1PF 0201
C76F5 1 2 1.8PF 25V C0G +/-0.1PF 201

153 148 43 41 PPVDD_CIO_S2SW
6
C76G0 1 2 12PF 25V NP0-C0G 5% 0201
C76G1 1 2 3.0PF 25V NP0-C0G +/-0.1PF 0201
C76G2 1 2 1.8PF 25V C0G +/-0.1PF 201

153 43 41 PPVDD_FIXED_S1
7
C76H0 1 2 12PF 25V NP0-C0G 5% 0201
C76H1 1 2 3.0PF 25V NP0-C0G +/-0.1PF 0201
C76H2 1 2 1.8PF 25V C0G +/-0.1PF 201

153 43 42 PP1V2_AWAKE
8
C76I0 1 2 12PF 25V NP0-C0G 5% 0201
C76I1 1 2 3.0PF 25V NP0-C0G +/-0.1PF 0201
C76I2 1 2 1.8PF 25V C0G +/-0.1PF 201

153 43 42 PPVDD_AMPH0_S2SW
9
C76J0 1 2 12PF 25V NP0-C0G 5% 0201
C76J1 1 2 3.0PF 25V NP0-C0G +/-0.1PF 0201
C76J2 1 2 1.8PF 25V C0G +/-0.1PF 201

BOM_COST_GROUP=WIRELESS

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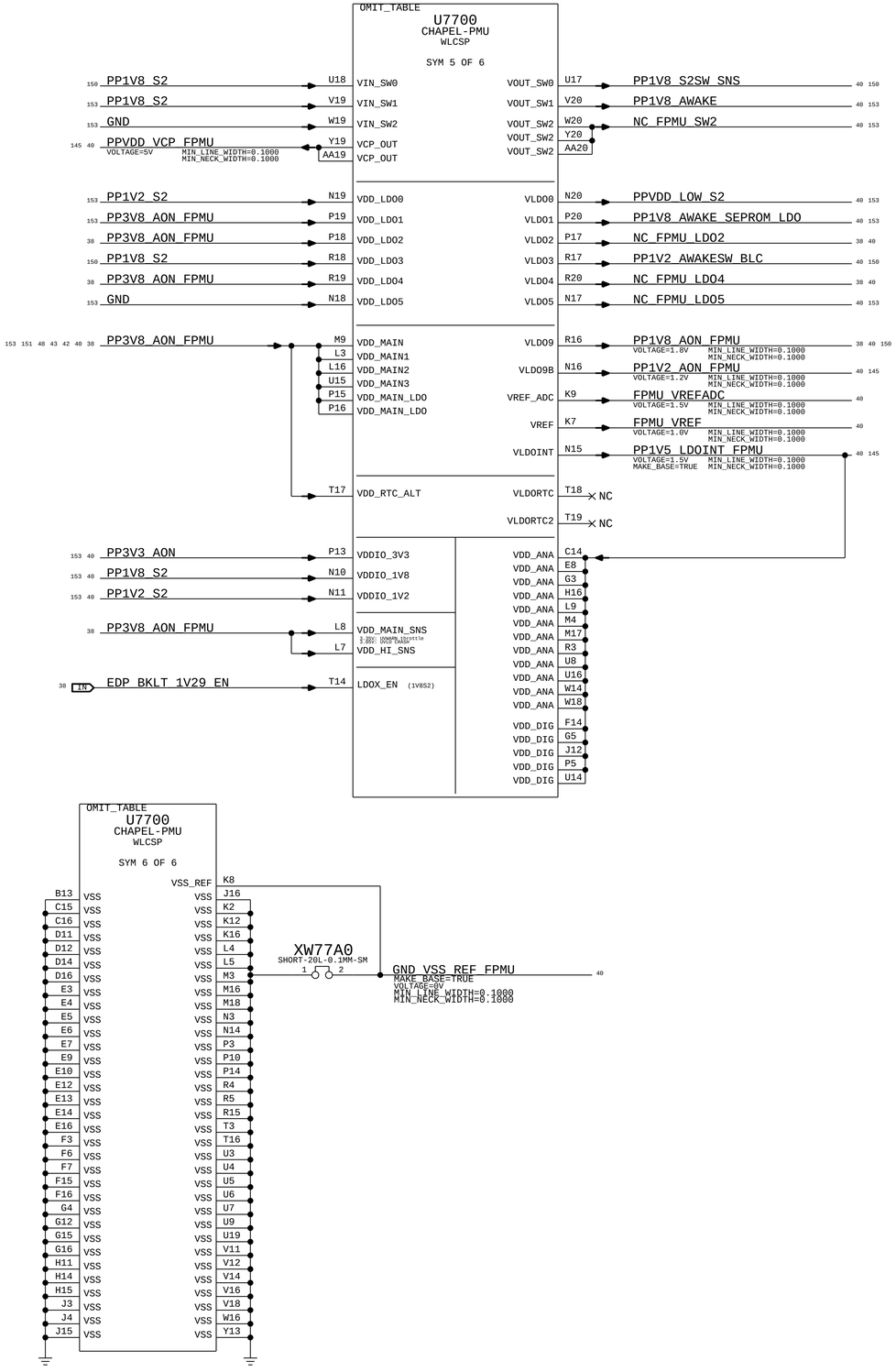

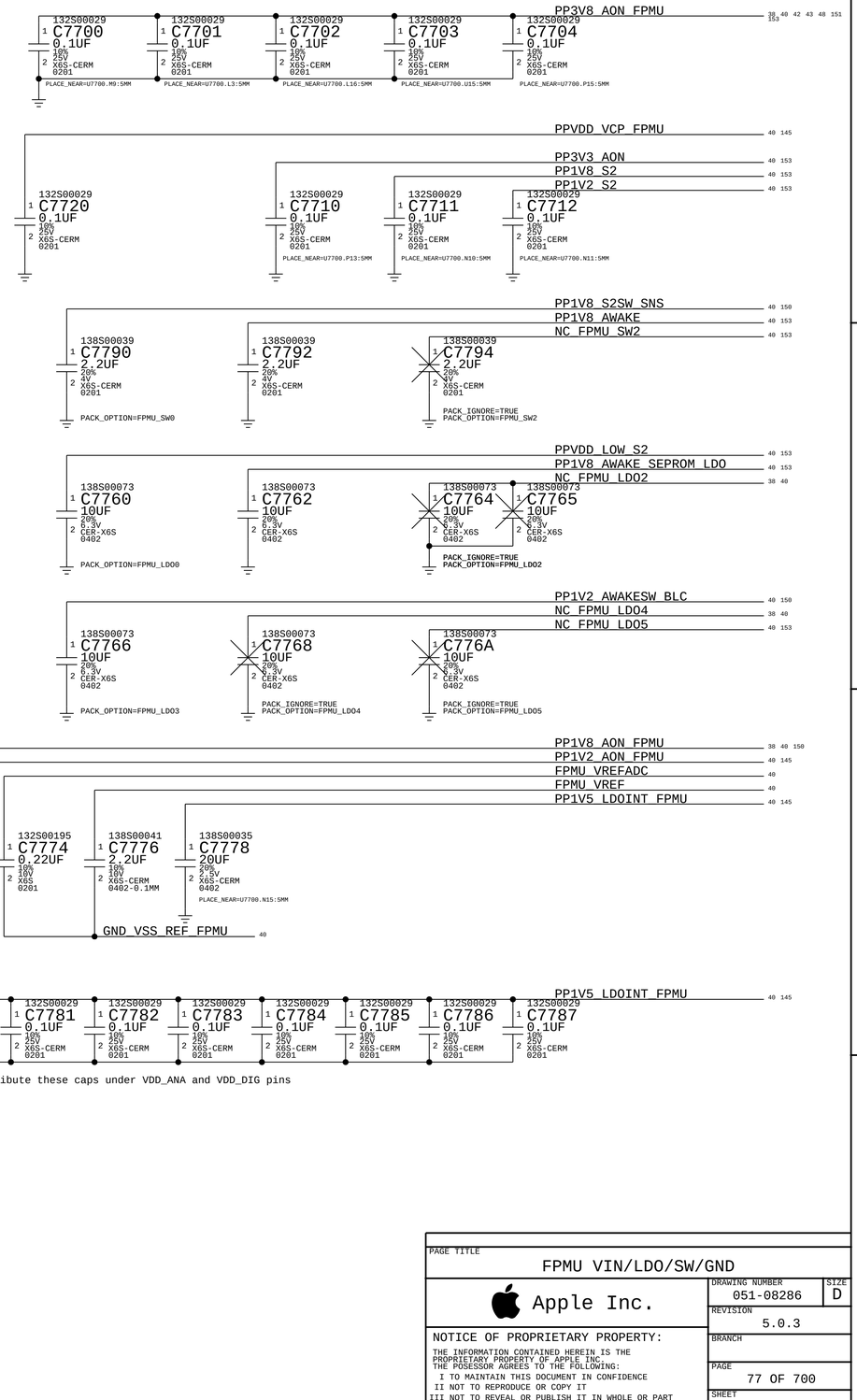

BOM_COST_GROUP=SOC POWER

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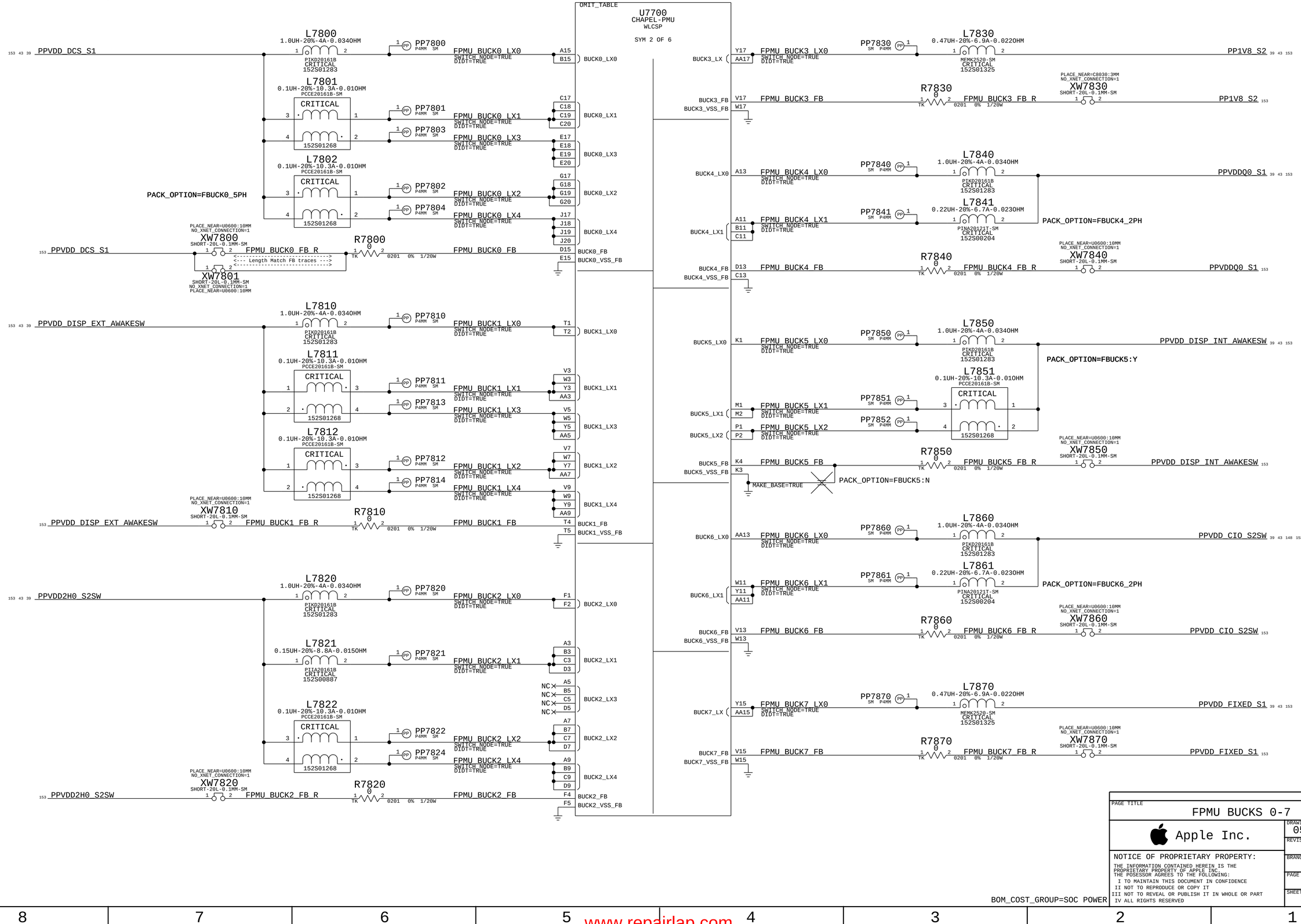

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(Pin Notes) are based on OTP version xPD: https://seg-docs.csg.apple.com/projects/chapel/release/OTP/A0/
[Pin Notes] are based on iBoot overrides: rdar://96232826

GPIO without (OTP notes) are Input/PD/1V8AON
GPIO without [iBoot overrides notes] are left in their OTP config
GPIO that are unused (NC) in a given project are left in their OTP config

OMIT_TABLE
U7700
CHAPEL-PMU
WLCSP
SYM 4 OF 6

74	P1V8VDDH_HS_ISENSE	G8	AMUX_A<0>	GPIO1	H12	NC_FPMU_GPIO1	38
74	P1V8VDDH_VSENSE	F13	AMUX_A<1>	GPIO2	J11	NC_FPMU_GPIO2	38
74	P3V8AON_HS_ISENSE	G7	AMUX_A<2>	GPIO3	H13	NC_FPMU_GPIO3	38
74	WLBT_3V8_ISENSE	F12	AMUX_A<3>	GPIO4	J13	NC_FPMU_GPIO4	38
74	SPKRAMP_DEF_ISENSE	G6	AMUX_A<4>	GPIO5	J14	NC_FPMU_GPIO5	38
74	FPMU_3V8_ISENSE	F11	AMUX_A<5>	GPIO6	K15	NC_FPMU_GPIO6	38
74	FAN1_PBUS_ISENSE	F8	AMUX_A<6>	GPIO7	K14	NC_FPMU_GPIO7	38
74	P1V8VDDH_ISENSE	F10	AMUX_A<7>	GPIO8	K13	NC_FPMU_GPIO8	38
38	NC_FPMU_AMUX_AY	J9	AMUX_AY	GPIO9	L13	NC_FPMU_GPIO9	38
74	USB01_3V8_ISENSE	G9	AMUX_B<0>	GPIO10	L14	NC_FPMU_GPIO10	38
74	NC_FPMU_AMUX_B1_TBD	F9	AMUX_B<1>	GPIO11	M15	NC_FPMU_GPIO11	38
74	P5VUSB01_HS_ISENSE	G10	AMUX_B<2>	GPIO12	M14	NC_HDMI_CECFET_EN	OUT 155
74	TCON_3V8_ISENSE	G11	AMUX_B<3>	GPIO13	M13	NC_FPMU_GPIO13	38
74	BKLT_HS_ISENSE	G13	AMUX_B<4>	GPIO14	M12	NC_FPMU_GPIO14	OUT 38
74	SD_HS_ISENSE	G14	AMUX_B<5>	GPIO15	M7	NC_FPMU_GPIO15	38
74	ALSCAM_5V_ISENSE	H10	AMUX_B<6>	GPIO16	M6	NC_FPMU_GPIO16	38
74	BKLTCONN_3V8_ISENSE	H9	AMUX_B<7>	GPIO17	M5	NC_FPMU_GPIO17	38
38	NC_FPMU_AMUX_BY	J7	AMUX_BY	GPIO18	N4	NC_FPMU_GPIO18	38
				GPIO19	P4	NC_FPMU_GPIO19	38
74	P1V8VDDH_THMSNS_3	H5	TDEV1	GPIO20	P6	NC_FPMU_GPIO20	38
74	AIRFLOW_C_THMSNS	H6	TDEV2	GPIO21	N6	NC_FPMU_GPIO21	38
74	FINSTACK_R_THMSNS	H7	TDEV3	GPIO22	N7	NC_FPMU_GPIO22	38
74	FINSTACK_L_THMSNS	J5	TDEV4	GPIO23	N8	NC_FPMU_GPIO23	38
74	P1V8VDDH_THMSNS_1	K5	TDEV5	GPIO24	N9	NC_FPMU_GPIO24	38
74	P1V8VDDH_THMSNS_2	H8	TDEV6	(3V3AON/OD) GPIO25	N12	IPD_TOUCH_RESET_L	OUT 139 145
74	FPMU_THMSNS	J6	TDEV7	(3V3AON/OD) GPIO26	N13	IPD_MCU_RESET_L	OUT 139 143
74	WLBT_THMSNS	J8	TDEV8	GPIO27	L15	NC_FPMU_GPIO27	38
42	FPMU_TCAL	K6	TCAL	SLEEP_32K	R6	NC_FPMU_SLEEP_32K	
				OUT_32K_0	P8	NC_FPMU_OUT_32K_0	
				OUT_32K_1	P9	NC_FPMU_OUT_32K_1	
	NC_FPMU_BUTTON1	P12	BUTTON1	DBLCLICK_DET	U12	NC_FPMU_DBLCLICK_DET	
	NC_FPMU_BUTTON2	P11	BUTTON2				
	NC_FPMU_RESET_IN0	T9	RESET_IN0	FAULT_OUT_L	T13	NC_FPMU_FAULT_OUT_L	
	NC_FPMU_RESET_IN1	T8	RESET_IN1	(1V2AON) CRASH0_L	T12	FPMU_CRASH0_L	BI 38 145
	NC_FPMU_RESET_IN2	T7	RESET_IN2	(1V8AON) CRASH1_L	R11	FPMU_CRASH1_L	IN 38 145
	NC_FPMU_RESET_IN3	T6	RESET_IN3	CRASH2_L	R10	NC_FPMU_CRASH2_L	
	NC_FPMU_SHDN	U10	SHDN	OFF_REQ	N5	NC_FPMU_OFF_REQ	
	NC_FPMU_PSU_12V_PGOOD	T11	PSU_P12V_PGOOD	WAKE2LF	R12	NC_FPMU_WAKE2LF	
50 46	SGPIO_READY_REQ	R14	SGPIO_READY_REQ (1V2AON)	ACTIVE_READY	U13	NC_FPMU_ACTIVE_READY	
38	SGPIO_FPMU_DATA	L11	SGPIO_SDATA (1V2AON)	SYS_ALIVE	R13	NC_FPMU_SYS_ALIVE	
38	SGPIO_FPMU_CLK	M11	SGPIO_SCLK_0 (1V2AON)	RESET_L	T10	NC_FPMU_RESET_L	
	NC_FPMU_SGPIO_SCLK_1	M10	SGPIO_SCLK_1	FORCE_DFU	P7	NC_FPMU_FORCE_DFU	
12	SPMI_FPMU_CLK	K11	SPMI_SCLK (1V2S2)	(1V2S2/OD) THROTTLE0_L	R9	NC_FABRIC_ILIMIT_L	OUT 153
12	SPMI_FPMU_DATA	L12	SPMI_SDATA (1V2S2)	THROTTLE1_L	R8	NC_FPMU_THROTTLE1_L	
12	SWD_FPMU_SWDIO	M8	SWD_TMS (1V2S2)	THROTTLE2_L	R7	NC_FPMU_THROTTLE2_L	
12	SWD_FPMU_SWCLK	L10	DFT_CTRL1 (1V2S2)	UVWARN_L	U11	NC_FPMU_UVWARN_L	
				VPP	E11	GND	42
		T15	CFG_EXT_CLK	CFG_OTP	L6	GND	42
		T20	XOUT	DFT_CTRL0	K10		
		U20	XIN	DFT_CTRL2	J10	GND	42

HDMI CEC FET is planned to be deprecated
Its parts are NOSTUFF and bypassed, and this IO is not configured

153 151 48 43 40 38 PP3V8_AON_FPMU

R7972 10K 0201 TK NOSTUFF
PACK_IGNORE=TRUE 5% 1/20W
PACK_OPTION=PMU_CFGOTP:R
R7971 10K 0201 TK
PACK_IGNORE=TRUE 5% 1/20W
PACK_OPTION=PMU_CFGOTP:R
42 GND
PACK_OPTION=PMU_CFGOTP:GND MAKE_BASE=TRUE

R7970 10K 0201 TK
PACK_IGNORE=TRUE 5% 1/20W
PACK_OPTION=VPP:R
42 GND
PACK_OPTION=VPP:GND MAKE_BASE=TRUE

R7973 10K 0201 TK
PACK_IGNORE=TRUE 5% 1/20W
PACK_OPTION=VPP:R
42 GND
PACK_OPTION=VPP:GND MAKE_BASE=TRUE

103S00584 R7911 3.92K 0.1% 1/20W TK 0201
131S0805 C7911 100PF 5% 25V C0G 0201
FPMU_TCAL 42

OMIT_TABLE
U7700
CHAPEL-PMU
WLCSP
SYM 3 OF 6

BUCK8_LX L19 L20 FPMU_BUCK8_LX0 SWITCH_NODE=TRUE DIDT=TRUE
PP7980 SM P4MM
L7980 0.47UH-20%-6.9A-0.022OHM MEMK2520-SM CRITICAL 152S01325
PP1V2_AWAKE 39 43 153

BUCK8_FB L17 FPMU_BUCK8_FB
BUCK8_VSS_FB L18
R7980 0 0201 0% 1/20W
FPMU_BUCK8_FB_R
PLACE_NEAR=C8080:3MM NO_XNET_CONNECTION=1 XW7980 SHORT-20L-0.1MM-SM
PP1V2_AWAKE 153

BUCK9_LX H1 H2 FPMU_BUCK9_LX0 SWITCH_NODE=TRUE DIDT=TRUE
PP7990 SM P4MM
L7990 0.47UH-20%-6.9A-0.022OHM MEMK2520-SM CRITICAL 152S01325
PPVDD_AMPH0_S2SW 39 43 153

BUCK9_FB H4 FPMU_BUCK9_FB
BUCK9_VSS_FB H3
R7990 0 0201 0% 1/20W
FPMU_BUCK9_FB_R
PLACE_NEAR=U0600:10MM NO_XNET_CONNECTION=1 XW7990 SHORT-20L-0.1MM-SM
PPVDD_AMPH0_S2SW 153

BOM_COST_GROUP=SOC POWER

PAGE TITLE
FPMU GPIO & BUCKS 8-9

Apple Inc.

DRAWING NUMBER 051-08286 SIZE D
REVISION 5.0.3
BRANCH
PAGE 79 OF 700
SHEET 42 OF 168

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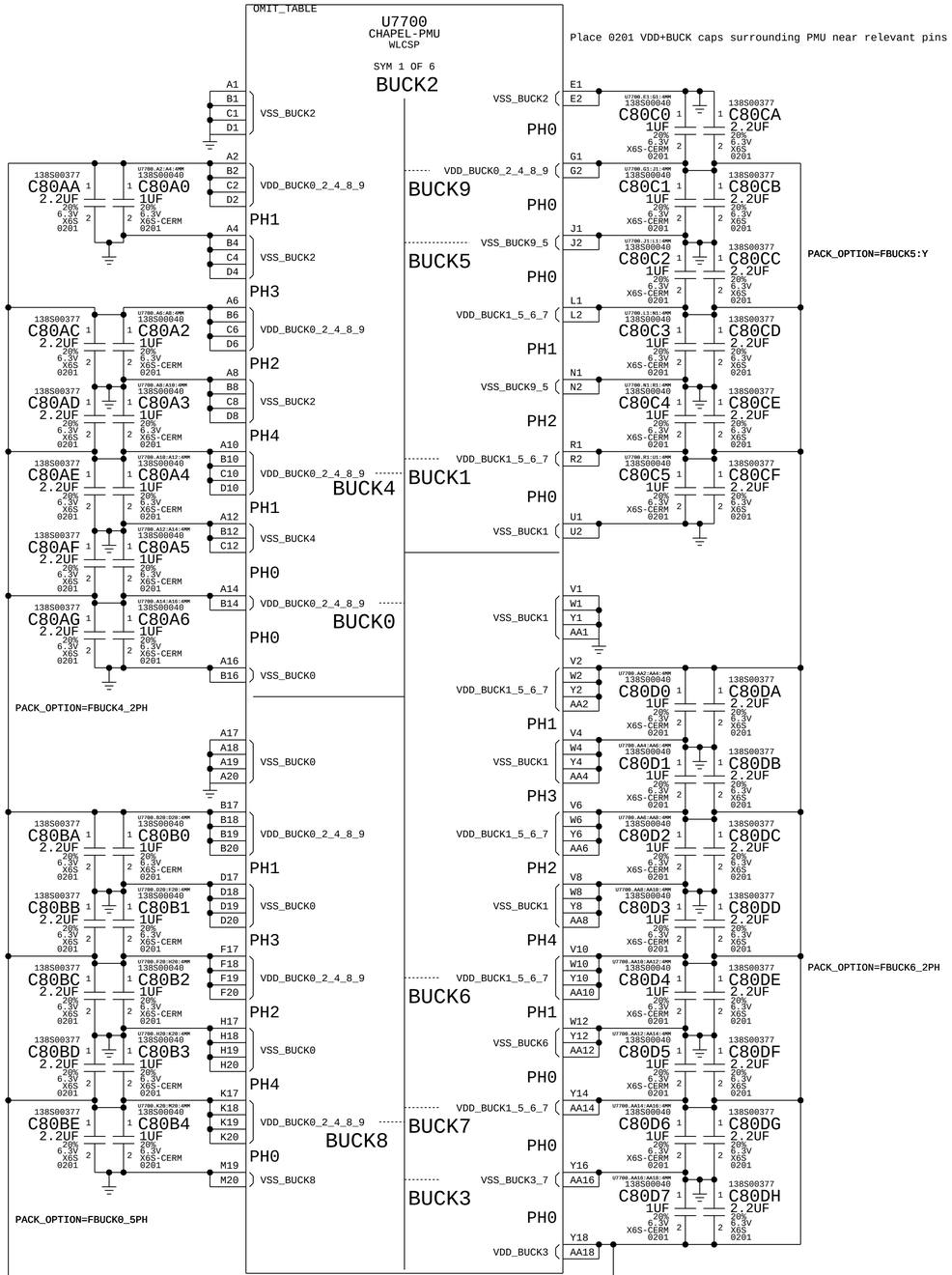

Buck Output Caps (near PMU)

1x 2.2uF 0402 per inductor, rounded up to even number to mirror
2x 0201 per CL pair
More 0402 caps on Bucks that serve system loads, for local bulk/FB

0 PPVDD_DCS_S1
1 PPVDD_DISP_EXT_AWAKESW
2 PPVDD2H0_S2SW
3 PP1V8_S2 (NOSTUFF)
4 PPVDDQ0_S1
5 PPVDD_DISP_INT_AWAKESW (PACK_OPTION=FBUCK5:Y)
6 PPVDD_CIO_S2SW
7 PPVDD_FIXED_S1
8 PP1V2_AWAKE
9 PPVDD_AMPH0_S2SW

1x 10uF input per inductor

Place under LX pins of each single-inductor phase
Place under shared VSS_BUCK pins of each CL-inductor pair

BOM_COST_GROUP=SOC POWER

PAGE TITLE: FPMU BUCK IN/OUT CAPS
Apple Inc.
DRAWING NUMBER: 051-08286
SIZE: D
REVISION: 5.0.3
BRANCH:
PAGE: 80 OF 700
SHEET: 43 OF 168

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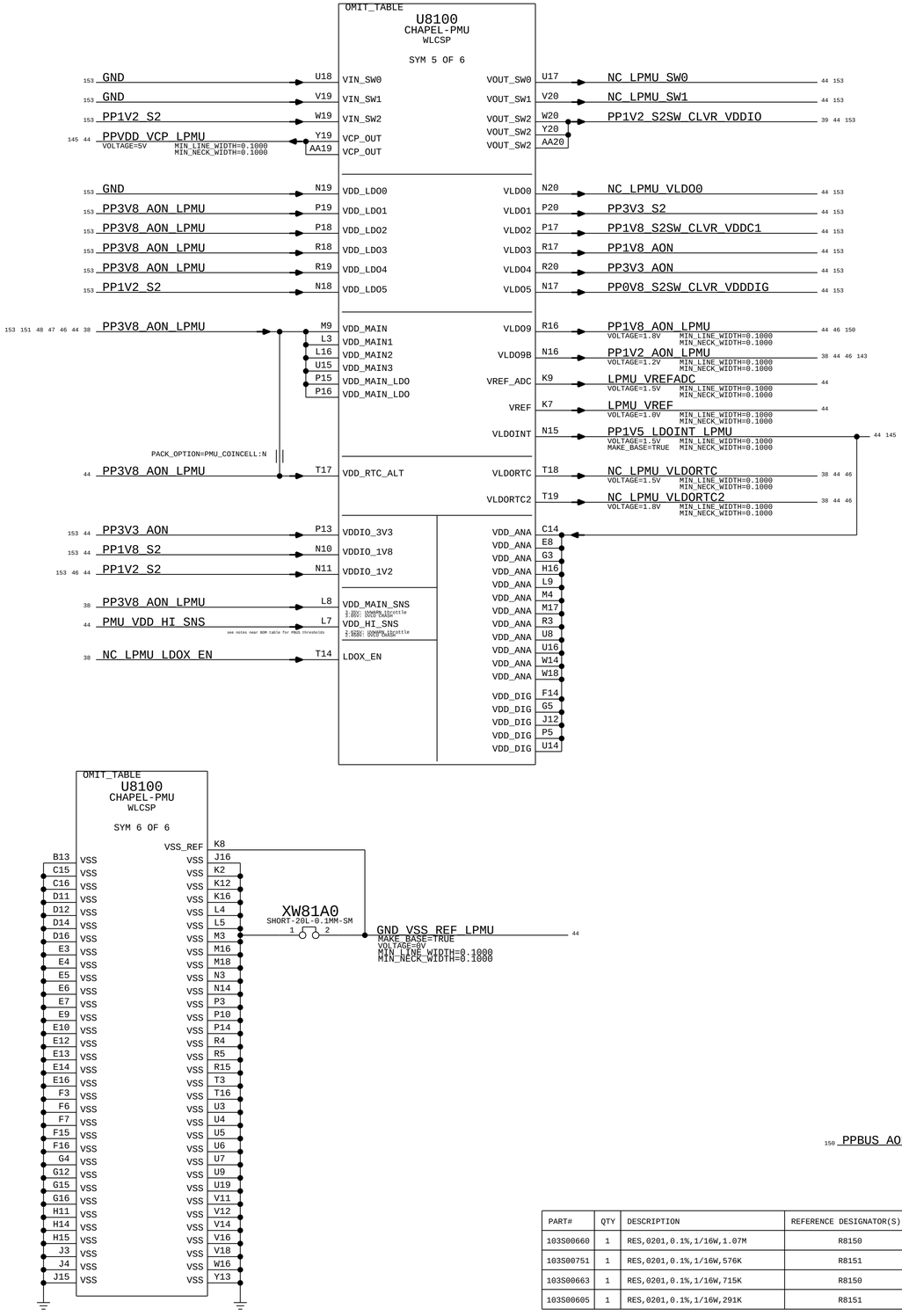

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
103S00660	1	RES,0201,0.1%,1/16W,1.07M	R8150	PBUS:3S
103S00751	1	RES,0201,0.1%,1/16W,576K	R8151	PBUS:3S
103S00663	1	RES,0201,0.1%,1/16W,715K	R8150	PBUS:12VDCIN
103S00605	1	RES,0201,0.1%,1/16W,291K	R8151	PBUS:12VDCIN

PAGE TITLE: LPMU VIN/LDO/SW/GND

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REVISION: 5.0.3
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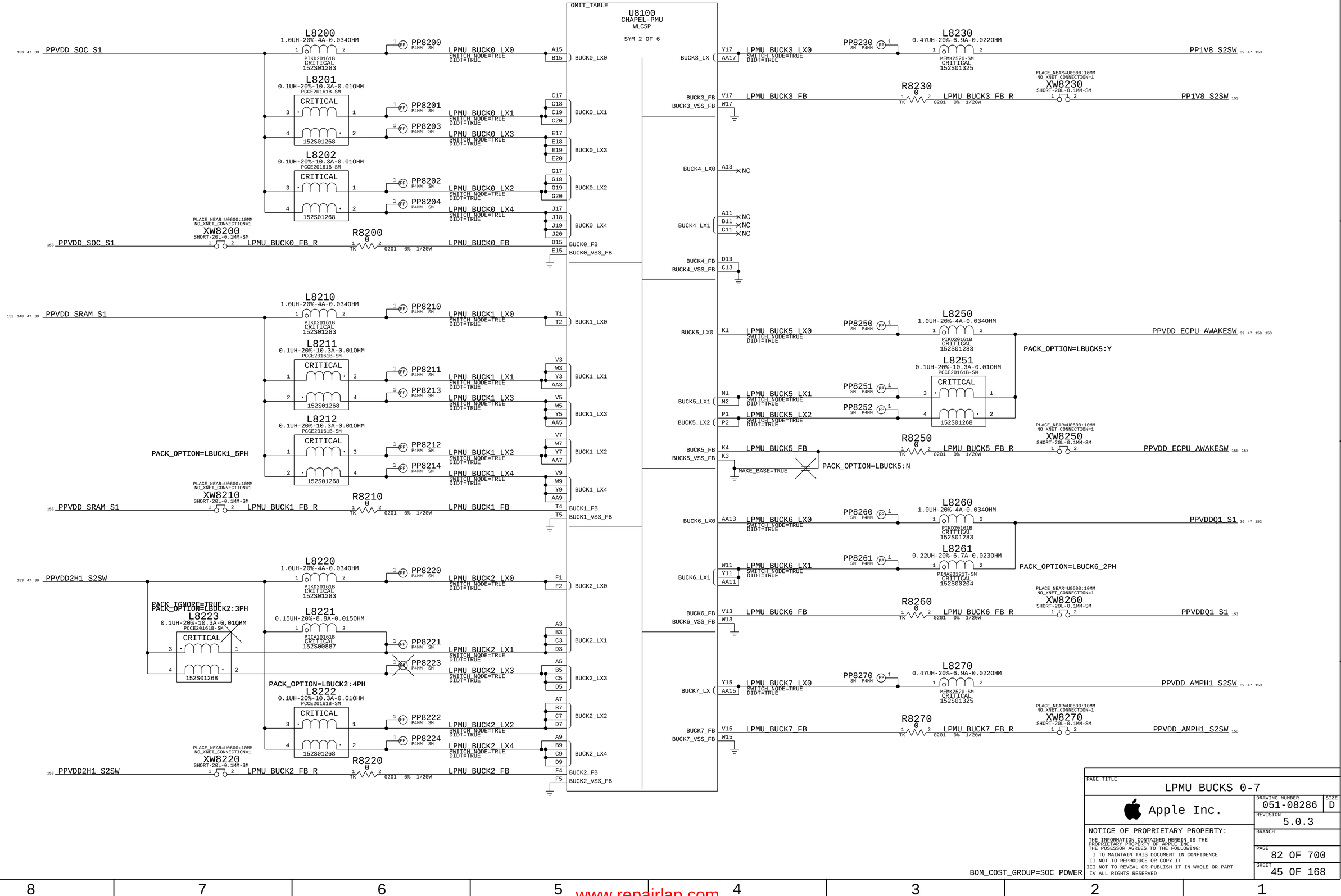

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OMIT_TABLE

U8100
CHAPEL-PMU
WLCSP

SYM 4 OF 6

See CSA79 for pin note context

74	DCIN_ISENSE	G8	AMUX_A<0>	(1V8AON)	GPIO1	H12	IPD_LID_OPEN_1V8
74	DCIN_VSENSE	F13	AMUX_A<1>	[1V2S2/*]	GPIO2	J11	SDCONN_STATE_CHANGE
74	BMON_ISENSE	G7	AMUX_A<2>	[1V2S2/PU]	GPIO3	H13	CODEC_WAKE_L
74	PBUS_VSENSE	F12	AMUX_A<3>	*	GPIO4	J13	CHGR_AUX_OK
74	P5VUSB23_HS_ISENSE	G6	AMUX_A<4>	*	GPIO5	J14	IPD_WAKE_L
74	P5VS2_HS_ISENSE	F11	AMUX_A<5>	[1V2S2/PD]	GPIO6	K15	WLBT_WAKE
74	SPKRAMP_ABC_ISENSE	F8	AMUX_A<6>	[1V2S2]	GPIO7	K14	NC_DP2HDMI_CEC_IRQ
74	TOUCHID_3V8_HS_ISENSE	F10	AMUX_A<7>		GPIO8	K13	NC_LPMU_GPIO8_RSVD
38	NC_LPMU_AMUX_AY	J9	AMUX_AY	[1V8S2]	GPIO9	L13	FAN_PWR_EN
74	IPD_3V8_ISENSE	G9	AMUX_B<0>	(1V2S2)	GPIO10	L14	CLVR_RESET_L
74	LPMU_3V8_ISENSE	F9	AMUX_B<1>	(1V8S2)	GPIO11	M15	PVDD1_PWR_EN
74	VCCNAND0_HS_ISENSE	G10	AMUX_B<2>		GPIO12	M14	NC_LPMU_GPIO12_RSVD
74	VCCNAND1_HS_ISENSE	G11	AMUX_B<3>	(1V8AON)	GPIO13	M13	P5VS2HOLD_PWR_EN
74	P3V8AON_ISENSE	G13	AMUX_B<4>	[1V2S2]	GPIO14	M12	SE_PWR_EN
74	USB23_3V8_ISENSE	G14	AMUX_B<5>	[1V8S2]	GPIO15	M7	HDMI_PWR_EN
74	SSD0_3V8_ISENSE	H10	AMUX_B<6>	[1V2S2/OD]	GPIO16	M6	DP2HDMI_RESET_L
74	SSD1_3V8_ISENSE	H9	AMUX_B<7>	[1V2S2/OD]	GPIO17	M5	NC_SD_MAIN_PWR_EN
38	NC_LPMU_AMUX_BY	J7	AMUX_BY	*	GPIO18	N4	IPD_PWR_EN
				[1V8S2]	GPIO19	P4	WLBT_PWR_EN
74	P3V8AON_THMSNS	H5	TDEV1	(1V8AON)	GPIO20	P3	P3V8AON_LPM
74	LPMU_THMSNS	H6	TDEV2	(1V2S2)	GPIO21	N6	LP5_IN_RESET_L
74	AIRFLOW_L_THMSNS	H7	TDEV3	[1V8S2]	GPIO22	N7	LCD_PWR_EN
74	AIRFLOW_R_THMSNS	J5	TDEV4	*	GPIO23	N8	BL_PWR_EN
74	WING_R_THMSNS	K5	TDEV5	[1V8S2]	GPIO24	N9	BL_PMIC_PWR_EN
74	CHGR_THMSNS	H8	TDEV6	[1V8S2]	GPIO25	N12	SD_PWR_EN
74	SOC_THMSNS_1	J6	TDEV7	[1V8S2]	GPIO26	N13	DP2HDMI_PWR_EN
74	WING_L_THMSNS	J8	TDEV8	*3V3AON*	GPIO27	L15	PMU_CLK32K_IPD_R
46	LPMU_TCAL	K6	TCAL	(1V2S2)	SLEEP_32K	R6	PMU_CLK32K_SOC_R
				(1V2S2)	OUT_32K_0	P8	PMU_CLK32K_CLVR_R
				(1V2S2)	OUT_32K_1	P9	PMU_CLK32K_WLBT_R
144 141 46 38 28 147	PMU_ONOFF_L	P12	BUTTON1 (1V8AON)	(1V2S2)	DBLCLICK_DET	U12	DBL_CLICK_DET
147 144 137 46 38	PMU_RSLOC_RST_L	P11	BUTTON2 (1V8AON)				
38	NC_ENET_LOM_RESET	T9	RESET_IN0 (1V2S2/PD)		FAULT_OUT_L	T13	NC_LPMU_FAULT_OUT_L
10	SOC_WDOG_L	T8	RESET_IN1 (1V2S2/PD*)	(1V2AON)	CRASH0_L	T12	LPMU_CRASH0_L
155 149 147 145	UPC_PMU_RESET_1V2	T7	RESET_IN2 (1V2S2/PD)	(1V2AON)	CRASH1_L	R11	LPMU_CRASH1_L
144 5	SOC_SOCHOT_L	T6	RESET_IN3 (1V2S2)	(1V2AON)	CRASH2_L	R10	LPMU_CRASH2_L
147 144 38	PMU_SHDN	U10	SHDN (1V8AON/PD)	(1V8AON)	OFF_REQ	N5	NC_PMU2_SHDN
38	NC_PMU_PSU_12V_PGOOD	T11	PSU_P12V_PGOOD (1V2AON)	(1V2AON/PU)	WAKE2LF	R12	NC_PMU_WAKE2LF
50 42	SGPIO_READY_REQ	R14	SGPIO_READY_REQ (1V2AON)	(1V2S2/OD)	ACTIVE_READY	U13	PMU_ACTIVE_READY
38	SGPIO_DATA_R	L11	SGPIO_SDATA (1V2AON)	(1V8S2)	SYS_ALIVE	R13	PMU_SYS_ALIVE
38	SGPIO_CLK0_R	M11	SGPIO_SCLK_0 (1V2AON)	(1V2S2/OD)	RESET_L	T10	PMU_RESET_L
38	SGPIO_CLK1_R	M10	SGPIO_SCLK_1 (1V2AON)	(1V2S2)	FORCE_DFU	P7	PMU_FORCE_DFU
12	SPMI_LPMU_CLK	K11	SPMI_SCLK (1V2S2)		THROTTLE0_L	R9	NC_LPMU_THROTTLE0_L
12	SPMI_LPMU_DATA	L12	SPMI_SDATA (1V2S2)	(1V2S2/OD)	THROTTLE1_L	R8	PMU_VDDHI_UVWARN_L
12	SWD_LPMU_SWDIO	M8	SWD_TMS (1V2S2)		THROTTLE2_L	R7	NC_LPMU_THROTTLE2_L
12	SWD_LPMU_SWCLK	L10	DFT_CTRL1 (1V2S2)	(1V2S2/OD)	UVWARN_L	U11	PMU_VDDMAIN_UVWARN_L
					VPP	E11	GND
					CFG_OTP	L6	GND
					DFT_CTRL0	K10	
					DFT_CTRL2	J10	GND
46	LPMU_XOUT	T15 T20 U20	CFG_EXT_CLK XOUT XIN				

OTP always selects externally injected CLK
CFG_EXT_CLK is ignored by OTP

OMIT_TABLE

U8100
CHAPEL-PMU
WLCSP

SYM 3 OF 6

BUCK8_LX	L19 L20	LPMU_BUCK8_LX0	SWITCH_NODE=TRUE DIDT=TRUE	PP8380 SM P40MM	L8380 0.47UH-20%-6.9A-0.022OHM MEMK2520-SM CRITICAL 152S01325
BUCK8_FB	L17	LPMU_BUCK8_FB	R8380 0 TK 0201 0% 1/20W	PLACE_NEAR=C8480:3MM NO_XNET_CONNECTION=1 XW8380 SHORT-20L-0.1MM-SM	
BUCK8_VSS_FB	L18				
BUCK9_LX	H1 H2	LPMU_BUCK9_LX0	SWITCH_NODE=TRUE DIDT=TRUE	PP8390 SM P40MM	L8390 0.47UH-20%-6.9A-0.022OHM MEMK2520-SM CRITICAL 152S01325
BUCK9_FB	H4	LPMU_BUCK9_FB	R8390 0 TK 0201 0% 1/20W	PLACE_NEAR=U0600:10MM NO_XNET_CONNECTION=1 XW8390 SHORT-20L-0.1MM-SM	
BUCK9_VSS_FB	H3				

PP1V2_S2 39 47 153

PPVDD_ECPU_SRAM_AWAKESW 39 47 153

PP1V8_AON_LPMU 150 46 44
PP1V2_S2 153 44
PP1V2_AWAKE 153
PP1V2_AON_LPMU 143 44 38

46 38	LPMU_CRASH0_L	R8320	10K 5% 1/20W 0201 TK
46 38	LPMU_CRASH1_L	R8321	10K 5% 1/20W 0201 TK
46 38	LPMU_CRASH2_L	R8322	1K 5% 1/20W 0201-1TK
155 146 144 143 46 10 5	PMU_ACTIVE_READY	R8324	10K 5% 1/20W 0201 TK
144 143 46 10	PMU_RESET_L	R8325	10K 5% 1/20W 0201 TK
147 144 141 46 38 28	PMU_ONOFF_L	R8326	1K 5% 1/20W 0201-1 TK
147 144 137 46 38	PMU_RSLOC_RST_L	R8327	10K 5% 1/20W 0201 TK

153 151 48 47 44 38 PP3V8_AON_LPMU

R8372 10K 5% 1/20W 0201 TK NOSTUFF
PACK_IGNORE=TRUE
PACK_OPTION=PMU_CFGOTP:R

46 GND

R8371 10K 5% 1/20W 0201 TK
PACK_IGNORE=TRUE
PACK_OPTION=PMU_CFGOTP:R
PACK_OPTION=PMU_CFGOTP:GND
MAKE_BASE=TRUE

46 GND

R8370 10K 5% 1/20W 0201 TK
PACK_IGNORE=TRUE
PACK_OPTION=VPP:R
PACK_OPTION=VPP:GND
MAKE_BASE=TRUE

46 GND

R8373 10K 5% 1/20W 0201 TK
PACK_IGNORE=TRUE
PACK_OPTION=VPP:R
PACK_OPTION=VPP:GND
MAKE_BASE=TRUE

LPMU_TCAL 46

103S00584 R8311 3.92K 0.1% 1/20W TK 0201

131S0805 C8311 100PF 5% 25V C0G 0201

46 LPMU_XOUT
Inverter Output<->
(RTC bypass)

197S00323 32.768KHZ-20PPM-1.8V 2.5X2.0-SM-COMBO

R8351 0 0201 TK 0% 1/20W

U8355 CRITICAL
VCC OUT EN/DIS GND

PMUOSC_PIN1

132S0395 C8355 0.1UF 10% 6.3V X6S 0201
PACK_OPTION=PMUOSC:QRTZ
BOMOPTION=PMUOSC:QRTZ

PP1V8_AON_LPMU 44 46 150

R8355 1K 5% 1/20W TK 0201-1
PACK_OPTION=PMUOSC:QRTZ
BOMOPTION=PMUOSC:QRTZ

NC_LPMU_VLDORTC 38 44

132S0395 C8365 0.1UF 10% 6.3V X6S 0201
PACK_IGNORE=TRUE
PACK_OPTION=PMUOSC:MEMS_1V5
BOMOPTION=PMUOSC:MEMS_1V5

197S00397 32.768KHZ-20PPM-250NA DFN

PMUOSC_OUT

U8365 CRITICAL
VDD CLK-0 NC NC NC NC NC NC GND

NC_LPMU_VLDORTC2 38 44

132S0395 C8366 0.1UF 10% 6.3V X6S 0201
PACK_IGNORE=TRUE
PACK_OPTION=PMUOSC:MEMS_1V8
BOMOPTION=PMUOSC:MEMS_1V8

197S00358 32.768KHZ-20PPM-2.7UA CSP

U8366 CRITICAL
VDD CLKOUT NC GND

PACK_IGNORE=TRUE
PACK_OPTION=PMUOSC:MEMS_1V8
BOMOPTION=PMUOSC:MEMS_1V8

BOM_COST_GROUP=SOC POWER

PAGE TITLE
LPMU GPIO & BUCKS 8-9

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REVISION 5.0.3
BRANCH
PAGE 83 OF 700
SHEET 46 OF 168

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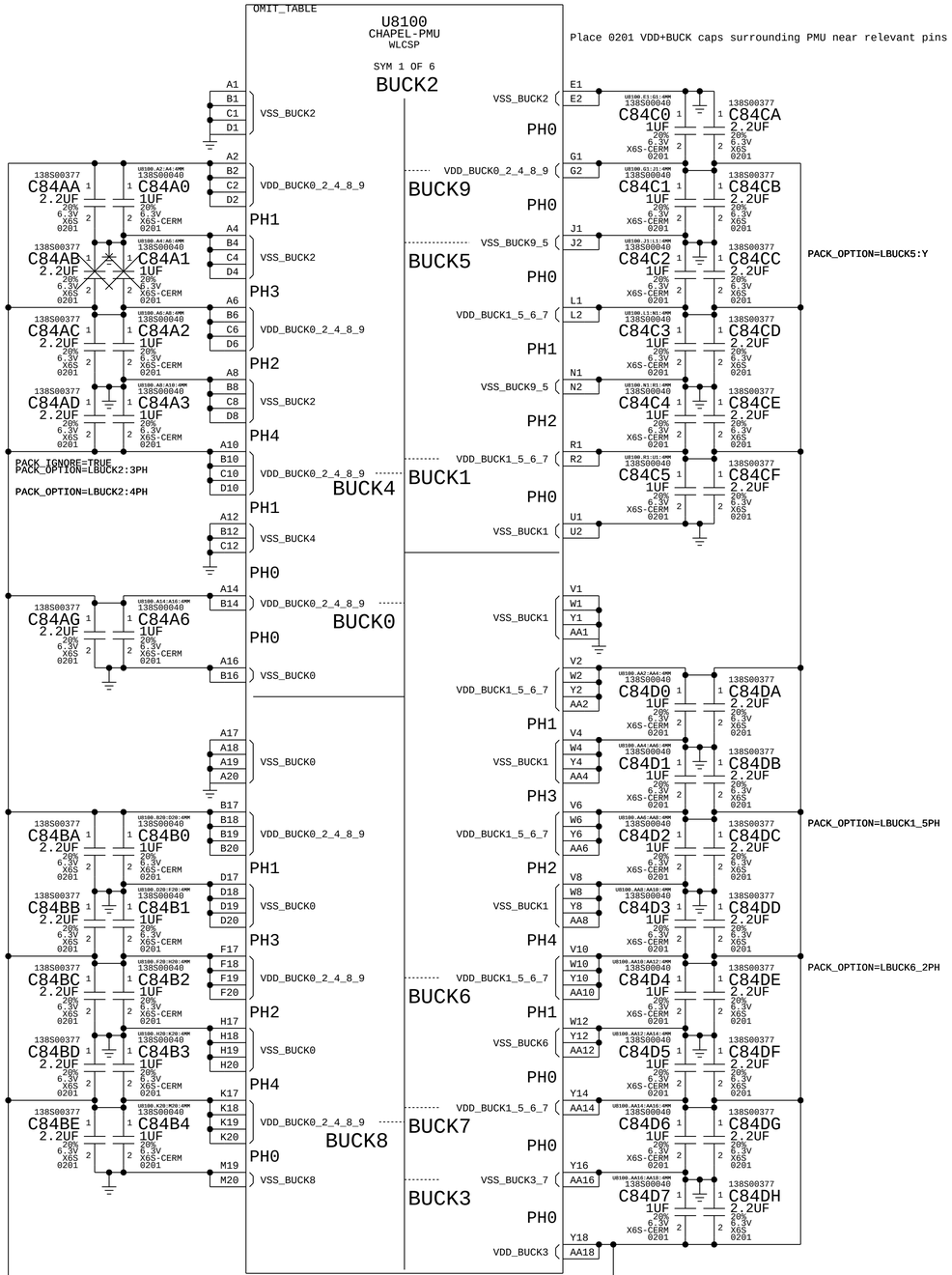

Buck Output Caps (near PMU)

1x 2.2uF 0402 per inductor, rounded up to even number to mirror
2x 0201 per CL pair
More 0402 caps on Bucks that serve system loads, for local bulk/FB

153 45 39 PPVDD_SOC_S1

0

C8400	C8401	C8402	C8403	C8404	C8405	C8406	C8407
138S00041	138S00041	138S00041	138S00041	132S0406	132S0406	132S0406	132S0406
2.2UF	2.2UF	2.2UF	2.2UF	0.22UF	0.22UF	0.22UF	0.22UF
20% 10V X6S-CERM 0402	MIRROR_WITH=C8400 20% 10V X6S-CERM 0402	MIRROR_WITH=C8400 20% 10V X6S-CERM 0402	MIRROR_WITH=C8400 20% 10V X6S-CERM 0402	20% 6.3V X6S-CERM 0201	20% 6.3V X6S-CERM 0201	20% 6.3V X6S-CERM 0201	20% 6.3V X6S-CERM 0201

153 148 45 39 PPVDD_SRAM_S1

1

C8410	C8411	C8412	C8413	C8414	C8415	C8416	C8417
138S00041	138S00041	138S00041	138S00041	132S0406	132S0406	132S0406	132S0406
2.2UF	2.2UF	2.2UF	2.2UF	0.22UF	0.22UF	0.22UF	0.22UF
20% 10V X6S-CERM 0402	MIRROR_WITH=C8410 20% 10V X6S-CERM 0402	MIRROR_WITH=C8410 20% 10V X6S-CERM 0402	MIRROR_WITH=C8410 20% 10V X6S-CERM 0402	20% 6.3V X6S-CERM 0201	20% 6.3V X6S-CERM 0201	20% 6.3V X6S-CERM 0201	20% 6.3V X6S-CERM 0201

PACK_OPTION=LBUCK1_5PH PACK_OPTION=LBUCK1_5PH

153 45 39 PPVDD2H1_S2SW

2

C8420	C8421	C8422	C8423	C8424	C8425
138S00041	138S00041	138S00041	138S00041	132S0406	132S0406
2.2UF	2.2UF	2.2UF	2.2UF	0.22UF	0.22UF
20% 10V X6S-CERM 0402	MIRROR_WITH=C8420 20% 10V X6S-CERM 0402	MIRROR_WITH=C8420 20% 10V X6S-CERM 0402	MIRROR_WITH=C8420 20% 10V X6S-CERM 0402	20% 6.3V X6S-CERM 0201	20% 6.3V X6S-CERM 0201

PACK_OPTION=LBUCK2:4PH

153 45 39 PP1V8_S2SW

3

C8430	C8431
138S00041	138S00041
2.2UF	2.2UF
20% 10V X6S-CERM 0402	MIRROR_WITH=C8430 20% 10V X6S-CERM 0402

4 <Unused>

153 150 45 39 PPVDD_ECPU_AWAKESW

5

C8450	C8451	C8454	C8455
138S00041	138S00041	132S0406	132S0406
2.2UF	2.2UF	0.22UF	0.22UF
20% 10V X6S-CERM 0402	MIRROR_WITH=C8450 20% 10V X6S-CERM 0402	20% 6.3V X6S-CERM 0201	20% 6.3V X6S-CERM 0201

PACK_OPTION=LBUCK5:Y

153 45 39 PPVDDQ1_S1

6

C8460	C8461
138S00041	138S00041
2.2UF	2.2UF
20% 10V X6S-CERM 0402	MIRROR_WITH=C8460 20% 10V X6S-CERM 0402

153 45 39 PPVDD_AMPH1_S2SW

7

C8470	C8471
138S00041	138S00041
2.2UF	2.2UF
20% 10V X6S-CERM 0402	MIRROR_WITH=C8470 20% 10V X6S-CERM 0402

153 46 39 PP1V2_S2

8

C8480	C8481	C8484	C8485	C8486	C8487	C8488	C8489
138S00041	138S00041	138S00423	138S00423	138S00423	138S00423	138S00423	138S00423
2.2UF	2.2UF	15UF	15UF	15UF	15UF	15UF	15UF
20% 10V X6S-CERM 0402	MIRROR_WITH=C8480 20% 10V X6S-CERM 0402	20% 2.5V X6S 0402-4	MIRROR_WITH=C8484 20% 2.5V X6S 0402-4	MIRROR_WITH=C8484 20% 2.5V X6S 0402-4	MIRROR_WITH=C8484 20% 2.5V X6S 0402-4	MIRROR_WITH=C8484 20% 2.5V X6S 0402-4	MIRROR_WITH=C8484 20% 2.5V X6S 0402-4

BOMSWAP=138S00392 BOMSWAP=138S00392 BOMSWAP=138S00392 BOMSWAP=138S00392 BOMSWAP=138S00392 BOMSWAP=138S00392

153 46 39 PPVDD_ECPU_SRAM_AWAKESW

9

C8490	C8491
138S00041	138S00041
2.2UF	2.2UF
20% 10V X6S-CERM 0402	MIRROR_WITH=C8490 20% 10V X6S-CERM 0402

C84F0	C84F1	C84F2	C84F3	C84F4	C84F5	C84F6	C84F7	C84F8	C84F9
138S0858	138S0858	138S0858	138S0858	138S0858	138S0858	138S0858	138S0858	138S0858	138S0858
10UF	10UF	10UF	10UF	10UF	10UF	10UF	10UF	10UF	10UF
20% 6.3V CERM-X6S 0402	20% 6.3V CERM-X6S 0402	20% 6.3V CERM-X6S 0402	20% 6.3V CERM-X6S 0402	20% 6.3V CERM-X6S 0402	20% 6.3V CERM-X6S 0402	20% 6.3V CERM-X6S 0402	20% 6.3V CERM-X6S 0402	20% 6.3V CERM-X6S 0402	20% 6.3V CERM-X6S 0402

C84FA	C84FB	C84FC	C84FD	C84FE	C84FF	C84FG
138S0858	138S0858	138S0858	138S0858	138S0858	138S0858	138S0858
10UF	10UF	10UF	10UF	10UF	10UF	10UF
20% 6.3V CERM-X6S 0402	20% 6.3V CERM-X6S 0402	20% 6.3V CERM-X6S 0402	20% 6.3V CERM-X6S 0402	20% 6.3V CERM-X6S 0402	20% 6.3V CERM-X6S 0402	20% 6.3V CERM-X6S 0402

1x 10uF input per inductor

Place under LX pins of each single-inductor phase
Place under shared VSS_BUCK pins of each CL-inductor pair

TBD whether we want to use PACK OPTIONS for unused phases

BOM_COST_GROUP=SOC POWER

PAGE TITLE
LPMU BUCK IN/OUT CAPS

Apple Inc.

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Input desense caps are shared across portables, until further notice

LPMU

153 151 47 46 44 38 PP3V8_AON_LPMU

131S0198 C8500 1.8PF +/-0.1PF 25V C0G 201	131S0445 C8501 12PF 5% 25V NP0-C0G 0201	131S0439 C8502 3.0PF +/-0.1PF 25V NP0-C0G 0201	131S0198 C8503 1.8PF +/-0.1PF 25V C0G 201	131S0445 C8504 12PF 5% 25V NP0-C0G 0201	131S0439 C8505 3.0PF +/-0.1PF 25V NP0-C0G 0201	131S0445 C8506 12PF 5% 25V NP0-C0G 0201	131S0445 C8507 12PF 5% 25V NP0-C0G 0201	131S0198 C8508 1.8PF +/-0.1PF 25V C0G 201
131S0445 C8509 12PF 5% 25V NP0-C0G 0201	131S0439 C850A 3.0PF +/-0.1PF 25V NP0-C0G 0201	131S0439 C850B 3.0PF +/-0.1PF 25V NP0-C0G 0201	131S0198 C850C 1.8PF +/-0.1PF 25V C0G 201	131S0198 C850D 1.8PF +/-0.1PF 25V C0G 201	131S0445 C850E 12PF 5% 25V NP0-C0G 0201	131S0439 C850F 3.0PF +/-0.1PF 25V NP0-C0G 0201	131S0198 C850G 1.8PF +/-0.1PF 25V C0G 201	131S0445 C850H 12PF 5% 25V NP0-C0G 0201
131S0439 C850I 3.0PF +/-0.1PF 25V NP0-C0G 0201	131S0445 C850J 12PF 5% 25V NP0-C0G 0201	131S0445 C850K 12PF 5% 25V NP0-C0G 0201	131S0198 C850L 1.8PF +/-0.1PF 25V C0G 201	131S0445 C850M 12PF 5% 25V NP0-C0G 0201	131S0439 C850N 3.0PF +/-0.1PF 25V NP0-C0G 0201	131S0445 C850O 12PF 5% 25V NP0-C0G 0201	131S0439 C850P 3.0PF +/-0.1PF 25V NP0-C0G 0201	131S0439 C850Q 3.0PF +/-0.1PF 25V NP0-C0G 0201

FPMU

153 151 43 42 40 38 PP3V8_AON_FPMU

131S0445 C8550 12PF 5% 25V NP0-C0G 0201	131S0439 C8551 3.0PF +/-0.1PF 25V NP0-C0G 0201	131S0439 C8552 3.0PF +/-0.1PF 25V NP0-C0G 0201	131S0445 C8553 12PF 5% 25V NP0-C0G 0201	131S0445 C8554 12PF 5% 25V NP0-C0G 0201	131S0198 C8555 1.8PF +/-0.1PF 25V C0G 201	131S0445 C8556 12PF 5% 25V NP0-C0G 0201	131S0439 C8557 3.0PF +/-0.1PF 25V NP0-C0G 0201	131S0439 C8558 3.0PF +/-0.1PF 25V NP0-C0G 0201
131S0198 C8559 1.8PF +/-0.1PF 25V C0G 201	131S0445 C855A 12PF 5% 25V NP0-C0G 0201	131S0445 C855B 12PF 5% 25V NP0-C0G 0201	131S0439 C855C 3.0PF +/-0.1PF 25V NP0-C0G 0201	131S0439 C855D 3.0PF +/-0.1PF 25V NP0-C0G 0201	131S0198 C855E 1.8PF +/-0.1PF 25V C0G 201	131S0445 C855F 12PF 5% 25V NP0-C0G 0201	131S0445 C855G 12PF 5% 25V NP0-C0G 0201	131S0439 C855H 3.0PF +/-0.1PF 25V NP0-C0G 0201
131S0198 C855I 1.8PF +/-0.1PF 25V C0G 201	131S0445 C855J 12PF 5% 25V NP0-C0G 0201	131S0439 C855K 3.0PF +/-0.1PF 25V NP0-C0G 0201	131S0198 C855L 1.8PF +/-0.1PF 25V C0G 201					

BOM_COST_GROUP=SOC POWER

PAGE TITLE
PMU PROJECT-SPECIFIC SUPPORT 2

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INPUT

DUE TO PHASES NOT PLACED TOGETHER, START WITH 9X 33UF INPUT PER PHASE

ADD CAPS HERE TO AUGMENT REFERENCE DESIGN CAPS

POTENTIALLY NOSTUFF/REMOVE CAPS AFTER PLACEMENT/SIMS

OUTPUT

moved to CSA95

ADD 2.5X 180UF OUTPUT CAPS PER 1X 470UF REMOVED FROM REFERENCE DESIGN

PLUS 1X NOSTUFF 180UF (AND 1X NOSTUFF 470UF ON CSA95)

INPUT

ADDITIONAL INPUT DESENSE CAPS

PPVIN_VDDH 50 52 53 54 159

C92A1	25V	NP0-C0G	12PF 5%	0201
C92A2	25V	NP0-C0G	3.0PF +/-0.1PF	0201
C92A3	25V	C0G	1.8PF +/-0.1PF	201
C92B1	25V	NP0-C0G	12PF 5%	0201
C92B2	25V	NP0-C0G	3.0PF +/-0.1PF	0201
C92B3	25V	C0G	1.8PF +/-0.1PF	201
C92C1	25V	NP0-C0G	12PF 5%	0201
C92C2	25V	NP0-C0G	3.0PF +/-0.1PF	0201
C92C3	25V	C0G	1.8PF +/-0.1PF	201
C92D1	25V	NP0-C0G	12PF 5%	0201
C92D2	25V	NP0-C0G	3.0PF +/-0.1PF	0201
C92D3	25V	C0G	1.8PF +/-0.1PF	201
C92E1	25V	NP0-C0G	12PF 5%	0201
C92E2	25V	NP0-C0G	3.0PF +/-0.1PF	0201
C92E3	25V	C0G	1.8PF +/-0.1PF	201
C92F1	25V	NP0-C0G	12PF 5%	0201
C92F2	25V	NP0-C0G	3.0PF +/-0.1PF	0201
C92F3	25V	C0G	1.8PF +/-0.1PF	201
C92G1	25V	NP0-C0G	12PF 5%	0201
C92G2	25V	NP0-C0G	3.0PF +/-0.1PF	0201
C92H1	25V	NP0-C0G	12PF 5%	0201
C92H2	25V	NP0-C0G	3.0PF +/-0.1PF	0201
C92I1	25V	NP0-C0G	12PF 5%	0201
C92I2	25V	NP0-C0G	3.0PF +/-0.1PF	0201
C92J1	25V	NP0-C0G	12PF 5%	0201
C92J2	25V	NP0-C0G	3.0PF +/-0.1PF	0201
C92K2	25V	NP0-C0G	3.0PF +/-0.1PF	0201

OUTPUT

ADDITIONAL OUTPUT DESENSE CAPS

PPVDDH_S1_CLVR 55 72 152

C92Z1	25V	NP0-C0G	12PF 5%	0201
C92Z2	25V	C0G	1.8PF +/-0.1PF	201
C92Z3	25V	C0G	1.8PF +/-0.1PF	201
C92Y1	25V	NP0-C0G	12PF 5%	0201
C92Y2	25V	NP0-C0G	3.0PF +/-0.1PF	0201
C92Y3	25V	C0G	1.8PF +/-0.1PF	201
C92X1	25V	NP0-C0G	12PF 5%	0201
C92X2	25V	C0G	1.8PF +/-0.1PF	201
C92X3	25V	C0G	1.8PF +/-0.1PF	201
C92W1	25V	NP0-C0G	12PF 5%	0201
C92W2	25V	C0G	1.8PF +/-0.1PF	201
C92W3	25V	C0G	1.8PF +/-0.1PF	201
C92V1	25V	NP0-C0G	12PF 5%	0201
C92V2	25V	NP0-C0G	3.0PF +/-0.1PF	0201
C92V3	25V	C0G	1.8PF +/-0.1PF	201
C92U1	25V	NP0-C0G	12PF 5%	0201
C92U2	25V	NP0-C0G	3.0PF +/-0.1PF	0201
C92U3	25V	C0G	1.8PF +/-0.1PF	201
C92T1	25V	NP0-C0G	12PF 5%	0201
C92T2	25V	NP0-C0G	3.0PF +/-0.1PF	0201
C92T3	25V	C0G	1.8PF +/-0.1PF	201
C92S1	25V	NP0-C0G	12PF 5%	0201
C92S2	25V	NP0-C0G	3.0PF +/-0.1PF	0201
C92S3	25V	C0G	1.8PF +/-0.1PF	201
C92R1	25V	NP0-C0G	12PF 5%	0201
C92R2	25V	NP0-C0G	3.0PF +/-0.1PF	0201
C92Q1	25V	NP0-C0G	12PF 5%	0201
C92Q2	25V	NP0-C0G	3.0PF +/-0.1PF	0201
C92P1	25V	NP0-C0G	12PF 5%	0201
C92P2	25V	NP0-C0G	3.0PF +/-0.1PF	0201
C92O1	25V	NP0-C0G	12PF 5%	0201
C92O2	25V	NP0-C0G	3.0PF +/-0.1PF	0201
C92N1	25V	NP0-C0G	12PF 5%	0201
C92N2	25V	NP0-C0G	3.0PF +/-0.1PF	0201
C92M1	25V	NP0-C0G	12PF 5%	0201
C92M2	25V	NP0-C0G	3.0PF +/-0.1PF	0201
C92L1	25V	NP0-C0G	12PF 5%	0201
C92L2	25V	NP0-C0G	3.0PF +/-0.1PF	0201
C92Z9	25V	NP0-C0G	12PF 5%	0201
C92Z8	25V	NP0-C0G	3.0PF +/-0.1PF	0201
C92Y9	25V	NP0-C0G	12PF 5%	0201
C92Y8	25V	NP0-C0G	3.0PF +/-0.1PF	0201
C92X9	25V	NP0-C0G	12PF 5%	0201

PP9268 P3MM SM (PP) VDDH_SPS_TSENSE 51 52 53 54

BOM_COST_GROUP=SOC POWER

PAGE TITLE: VDDH VR: Project Support

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R9300
PP3V8_AON → 1 R9300 2 → PP3V8_AON_VDDMAIN_VDDHVR
5% 1/20W TK 0201
VOLTAGE=3.8V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.2000
TBD final VDD_MAIN R value for RC filter
Place series R between 3V8AON VR source, and VDD_MAIN pins
...to avoid noise from VDD_BUCK

C9300 10UF 20% 6.3V CERM-X6S 0402 (138S0858)
C9301 2.2UF 10% 10V X6S-CERM 0402-0.1MM (138S00041)
C9305 0.1UF 10% 25V X6S-CERM 0201 (132S00029)
C9306 0.1UF 10% 25V X6S-CERM 0201 (132S00029)
C9307 0.1UF 10% 25V X6S-CERM 0201 (132S00029)
C9308 0.1UF 10% 25V X6S-CERM 0201 (132S00029)

VDD_MAIN_SNS:
3.4V: UVWARN throttle
3.3V: UVLO CRASH (disabled in OFF)

PP5V_S2_HOLD (159 51)
C9310 2.2UF 10% 10V X6S-CERM 0402-0.1MM (138S00041)
XW9310 SHORT-20L-0.1MM-SM PLACE_NEAR=C9310:3MM
XW9380 SHORT-20L-0.1MM-SM
PPVIN_VDDH (159 54 53 52 49)
XW9380 should be placed at a polymer input PBUS cap
Which cap is layout-dependant. Consult DCDC

PP1V2_S2 (159) → C9320 1UF 20% 10V X6S-CERM 0201 (138S00044)
GND (50)

PP1V5_AON_VDDHVR
C9330 20UF 20% 2.5V X6S-CERM 0402 (138S00035)
C9340 2.2UF 10% 10V X6S-CERM 0402-0.1MM (138S00041)
C9341 0.1UF 10% 25V X6S-CERM 0201 (132S00029)
C9342 0.1UF 10% 25V X6S-CERM 0201 (132S00029)
C9343 0.1UF 10% 25V X6S-CERM 0201 (132S00029)
XW9340 SHORT-20L-0.1MM-SM PLACE_NEAR=C9330:3MM
XW9350 SHORT-20L-0.1MM-SM PLACE_NEAR=C9330:3MM

PP1V5_AON_ANA_VDDHVR
C9350 2.2UF 10% 10V X6S-CERM 0402-0.1MM (138S00041)
C9351 0.1UF 10% 25V X6S-CERM 0201 (132S00029)
C9352 0.1UF 10% 25V X6S-CERM 0201 (132S00029)
C9353 0.1UF 10% 25V X6S-CERM 0201 (132S00029)
C9354 0.1UF 10% 25V X6S-CERM 0201 (132S00029)
C9355 0.1UF 10% 25V X6S-CERM 0201 (132S00029)
C9356 0.1UF 10% 25V X6S-CERM 0201 (132S00029)

Caps for VDD ANA and DIG may get reduced based on layout

PP1V2_AON_VDDHVR
C9360 4.7UF 20% 6.3V CER 0402 (138S00097)
C9361 2.2UF 10% 10V X6S-CERM 0402-0.1MM (138S00041)
C9362 0.1UF 10% 25V X6S-CERM 0201 (132S00029)

VDDHVR_VMBX
VDDHVR_VREF_ADC
VDDHVR_VREF
C9370 0.01UF 10% 25V X7R 0201 (132S00070)
C9371 0.22UF 10% 10V X6S 0201 (132S00195)
C9372 2.2UF 10% 10V X6S-CERM 0402-0.1MM (138S00041)
GND_VSS_REF_VDDHVR
MAKE_BASE=TRUE
VOLTAGE=0V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
XW9370 SHORT-20L-0.1MM-SM

U9300
SPITFIRE-PMU-1
WLCSP
SYM 3 OF 3
OMIT_TABLE

A12	VDD_MAIN	VSS	A3
A13	VDD_MAIN	VSS	A5
K9	VDD_MAIN_BUCK0	VSS	B2
C3	VDD_MAIN_BUCK1	VSS	C10
B10	VDD_MAIN_SNS	VSS	C12
		VSS	D3
		VSS	D9
H11	VCC	VSS	D12
C8	VCC_SNS	VSS	D13
H3	BUCK0_VIN_SENSE	VSS	E3
		VSS	E5
C5	VDDIO_1V2	VSS	E9
E13	VPP	VSS	E12
		VSS	F3
		VSS	F9
		VSS	F12
		VSS	G3
B13	VLDOINT	VSS	G4
		VSS	G7
B5	VDD_DIG	VSS	G8
E6	VDD_DIG	VSS	G10
E10	VDD_DIG	VSS	G11
		VSS	G13
C9	VDD_ANA	VSS	H1
D4	VDD_ANA	VSS	H2
F10	VDD_ANA	VSS	H4
K3	VDD_ANA	VSS	H6
K7	VDD_ANA	VSS	H8
K11	VDD_ANA	VSS	H10
		VSS	H12
C13	VLD09B	VSS	J2
		VSS	J3
A4	VDDIO1V2_AON	VSS	J5
		VSS	J7
		VSS	J9
		VSS	J11
		VSS	J13
		VSS	K1
		VSS	K2
		VSS	K4
A10	VMBX	VSS	K5
		VSS	K6
B8	VREF_ADC	VSS	K8
		VSS	K10
B9	VREF	VSS	K12
		VSS	L13
A9	VSS_REF	VSS	M12
		VSS	N13

U9300
SPITFIRE-PMU-1
WLCSP
SYM 1 OF 3
OMIT_TABLE

NC	D5	GPIO1	DFT_CTRL1	F8 SWD_VDDHVR_SWCLK (IN 12)
NC	D7	GPIO2	SWD_TMS	E7 SWD_VDDHVR_SWDIO (BI 12)
NC	E8	GPIO3		
NC	E4	GPIO4	SPMI_SCLK	D6 SPMI_VDDHVR_CLK (IN 12 145)
			SPMI_SDATA	C6 SPMI_VDDHVR_DATA (BI 12 145)
NC	A11	ATB0	SGPIO_SCLK	A6 SGPIO_VDDHVR_CLK (IN 38)
NC	B12	ATB1	SGPIO_SDATA	B6 SGPIO_VDDHVR_DATA (BI 38)
NC	B11	ATB2	SGPIO_READY_REQ	F7 SGPIO_READY_REQ (IN 42 46)
NC	D11	ATB3		
NC	C7	ATB4	RESET_IN	D8 VDDHVR_RESET_IN (1 PP9300)
NC	B7	ATB5	SCRASH*	F6 VDDHVR_SCRASH_L (BI)
NC	A7	ATB6		
NC	A8	ATB7	THROTTLE0*	G6 VDDHVR_ILIMIT_L (OUT 5 145)
	G5	DFT_CTRL0	THROTTLE1*	F5 VDDHVR_THROTTLE1_L (1 PP9301)
GND (50)	C11	DFT_CTRL2	UVWARN*	C4 NC
			BUCK0_VDD_THROT*	F4 NC

PP9300 P3MM SM 38 145
PP9301 P3MM SM

R93A0 10K 5% 1/20W 0201 TK
PACK_IGNORE=TRUE
PACK_OPTION=VPP:R
PACK_OPTION=VPP:GND = MAKE_BASE=TRUE

R93A1 10K 5% 1/20W 0201 TK
PACK_IGNORE=TRUE
PACK_OPTION=VPP:R
PACK_OPTION=VPP:GND = MAKE_BASE=TRUE

DUMMY RESISTOR FOR DFM UF
R93B0 10K 5% 1/20W 0201 TK CKPLUS_WAIVE=TERMSHORTED
R93B1 10K 5% 1/20W 0201 TK CKPLUS_WAIVE=TERMSHORTED

BOM_COST_GROUP=SOC POWER

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
998-32290	1	IC,PMU,SPITFIRE,A0,OTP-CPJ,DEV,CSP169	U9300	CRITICAL	
353S03340	5	Ekara,RAA227028,A123:3.3V-PWM,220nH,42,OTP-rev3	U9500,U9550,U9600,U9650,U9700	CRITICAL	

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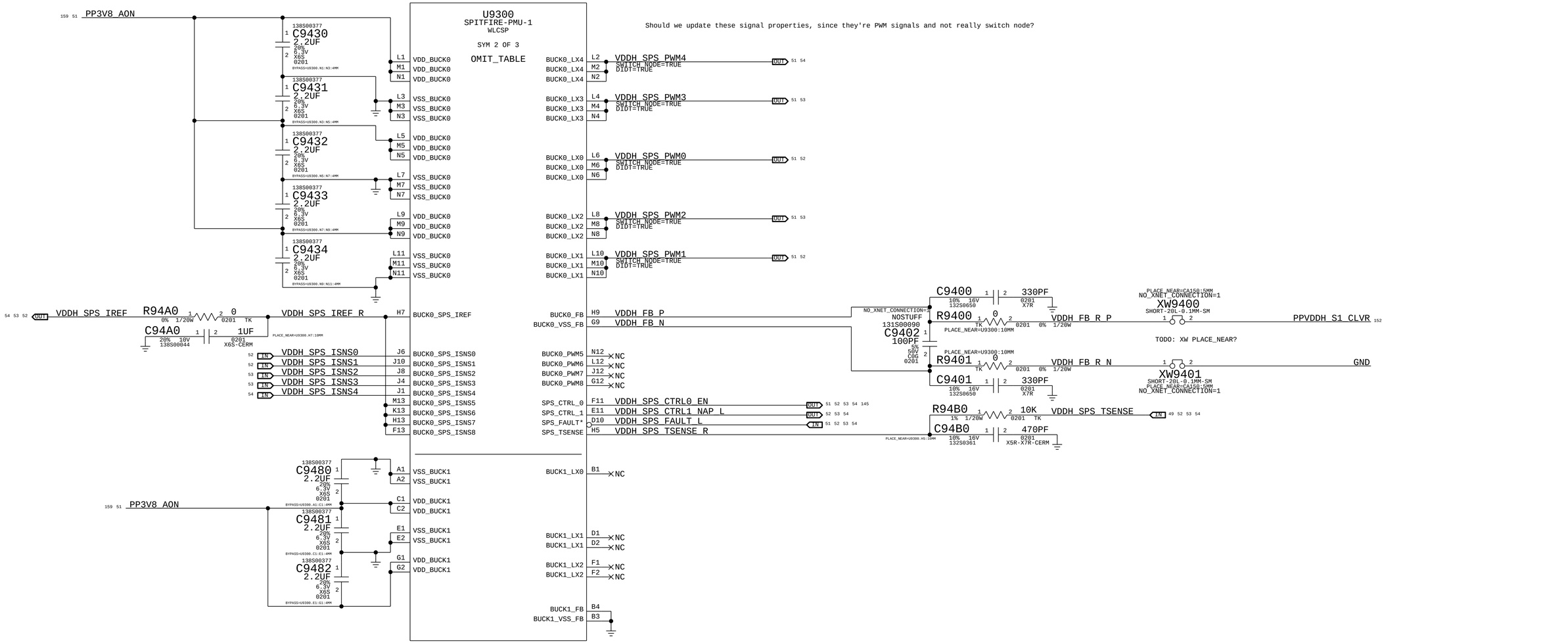

BOM_COST_GROUP=SOC POWER

PAGE TITLE	VDDH VR: Buck Controller
	Apple Inc.
DRAWING NUMBER	051-08286
SIZE	D
REVISION	5.0.3
BRANCH	
PAGE	94 OF 700
SHEET	51 OF 168

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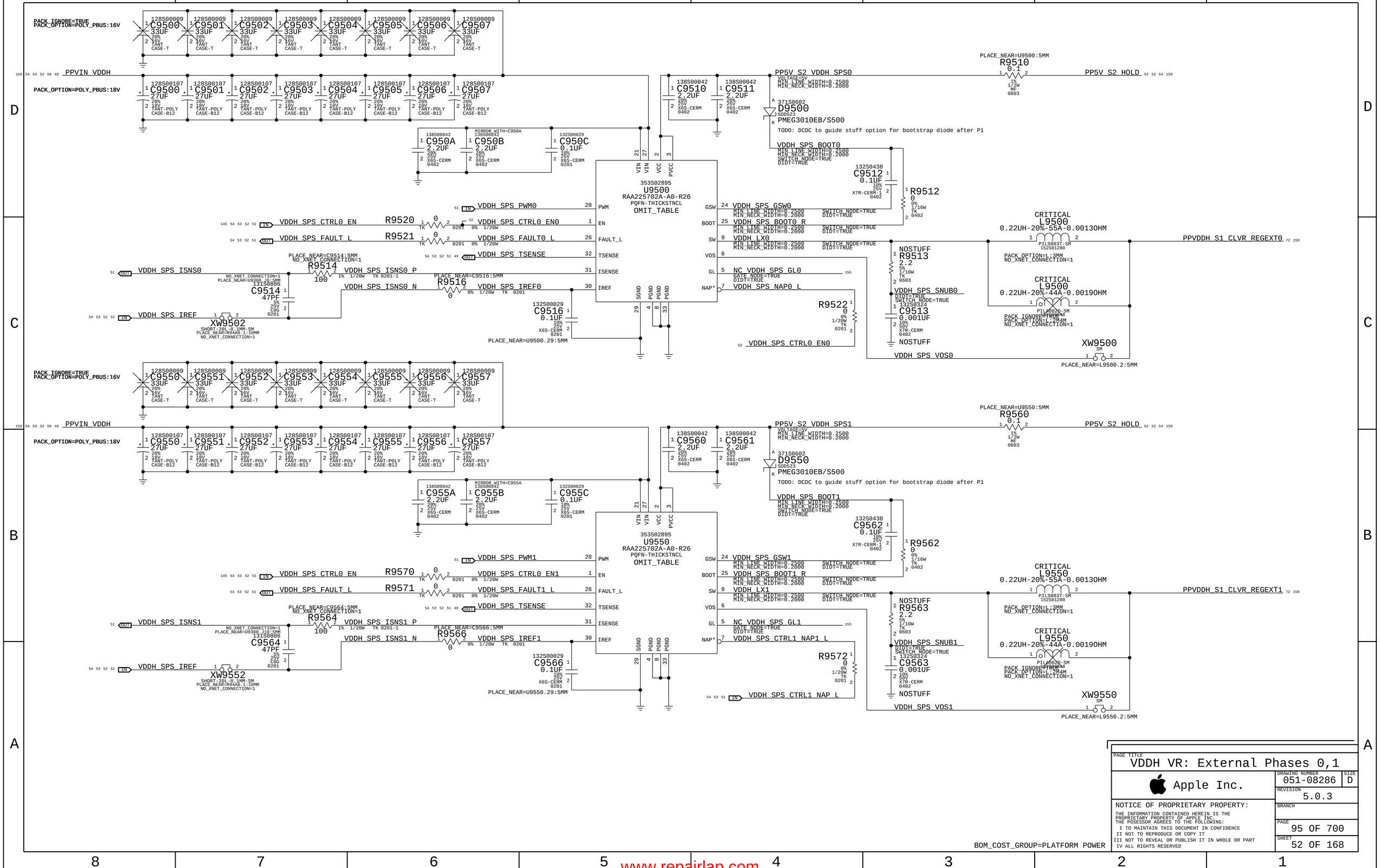

PAGE TITLE
VDDH VR: External Phases 0,1

Apple Inc.

DRAWING NUMBER 051-08286 | SIZE D
REVISION 5.0.3
BRANCH
PAGE 95 OF 700
SHEET 52 OF 168

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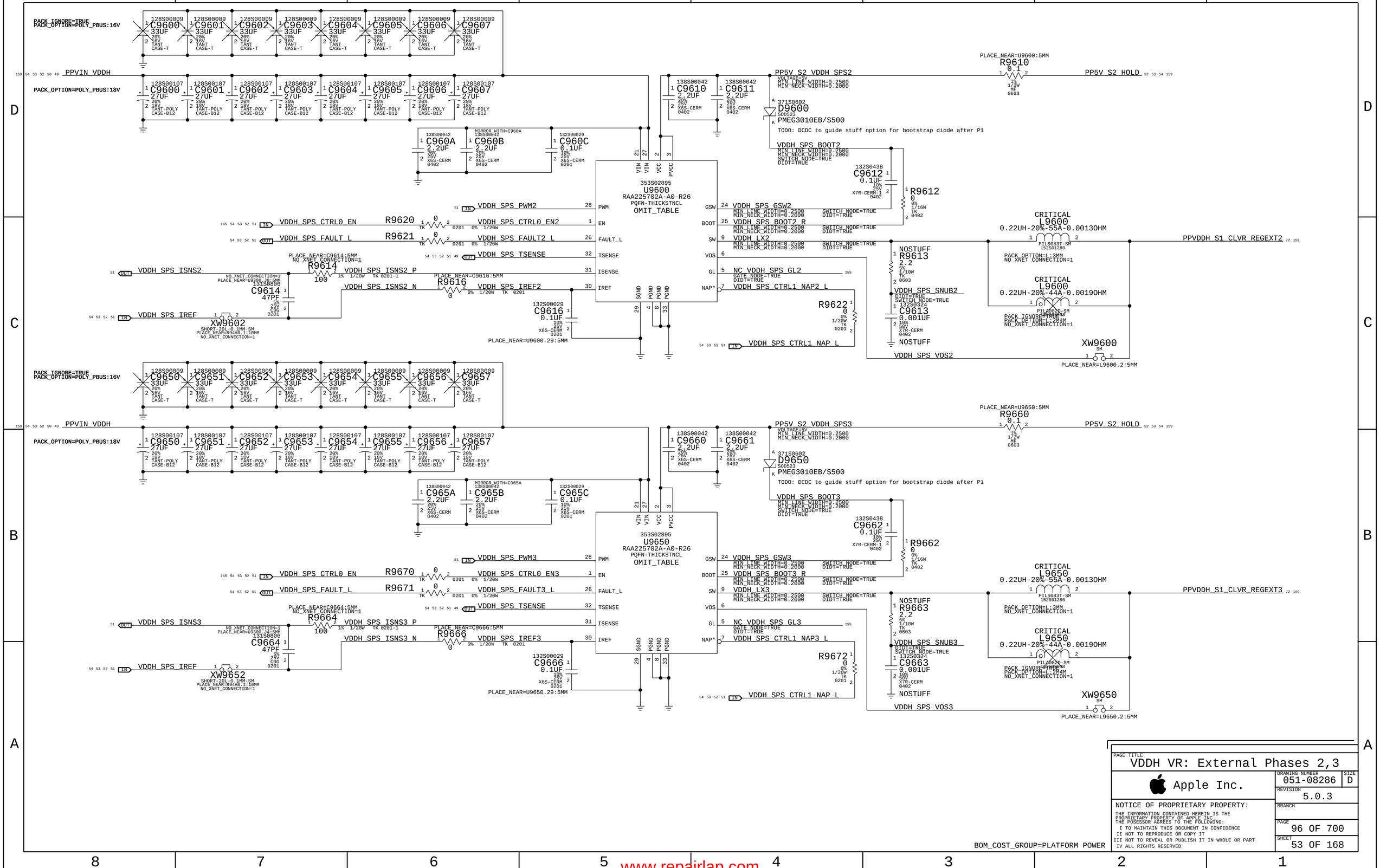

PAGE TITLE
VDDH VR: External Phases 2,3

Apple Inc.

DRAWING NUMBER 051-08286 | SIZE D
REVISION 5.0.3
BRANCH
PAGE 96 OF 700
SHEET 53 OF 168

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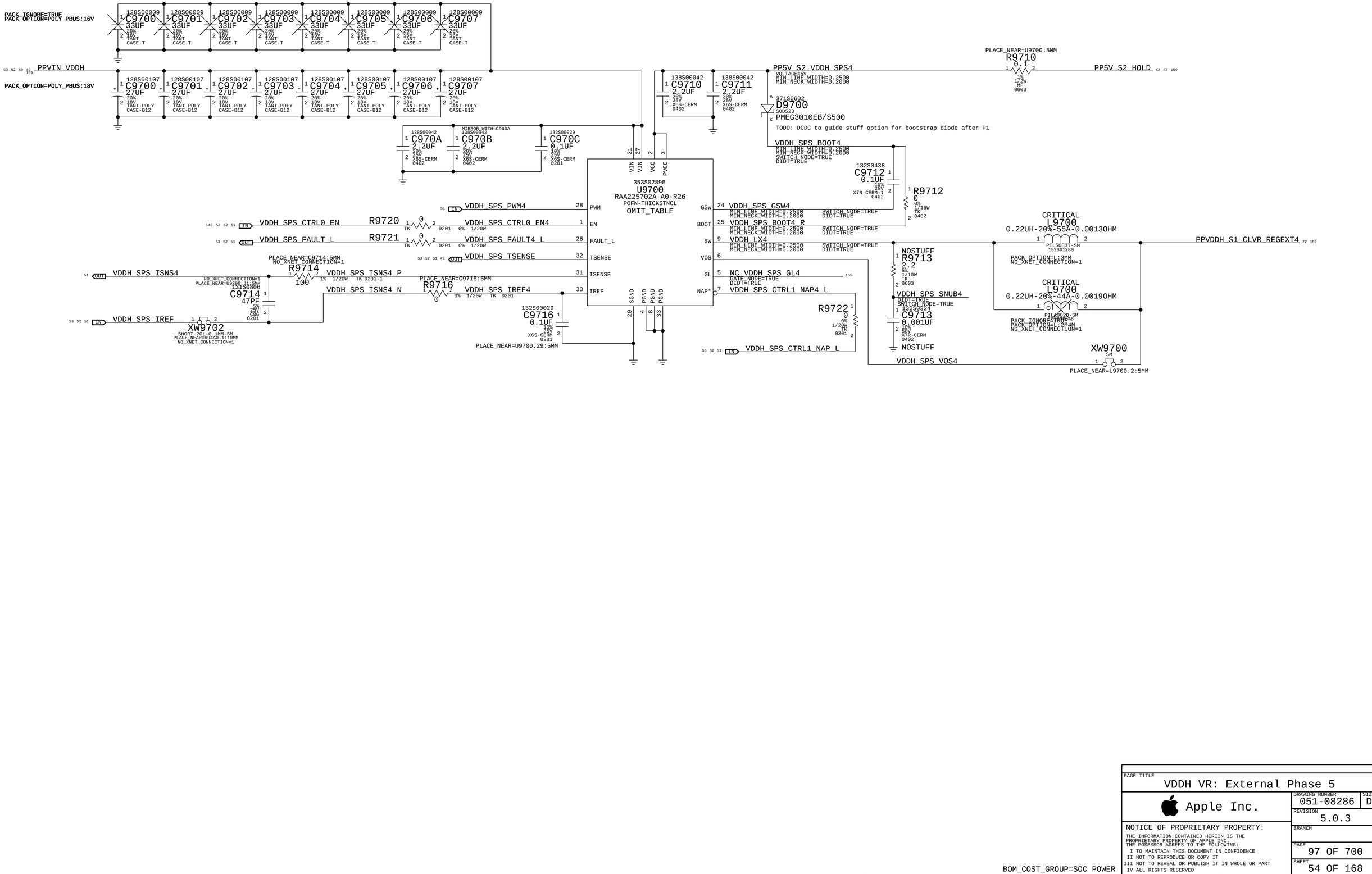

PAGE TITLE
VDDH VR: External Phase 5

Apple Inc.

DRAWING NUMBER 051-08286 | SIZE D
REVISION 5.0.3
BRANCH
PAGE 97 OF 700
SHEET 54 OF 168

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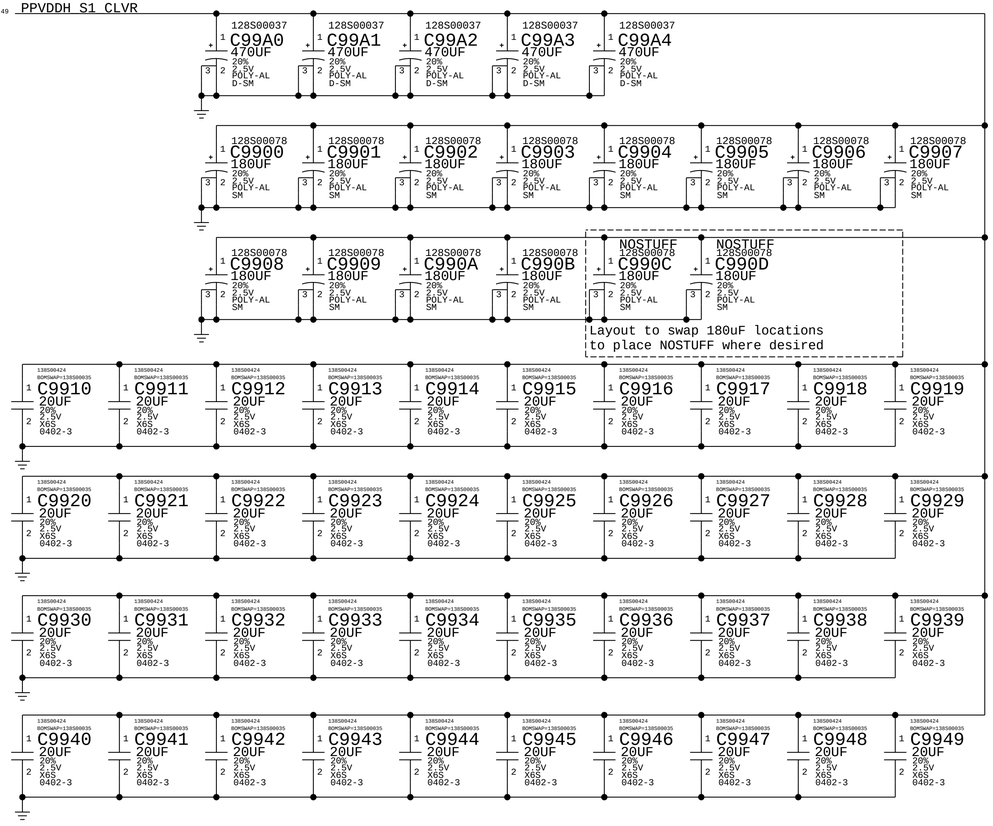
These Caps are placed near the VR, but AFTER any output Rsense

VR-side Output Caps

152 72 49 PPVDDH_S1_CLVR



BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE	VDDH VR: Output Caps
	Apple Inc.
DRAWING NUMBER	051-08286
SIZE	D
REVISION	5.0.3
BRANCH	
PAGE	99 OF 700
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OK2INTEGRATE

INSTANCE = C0
CFG = H (11+1+14+2)
OTP = MP_

PPVDDH_S1_CLVR 56 57 58 59 60 61 152

CA150 CA151 CA152 CA153 CA154 CA155 CA156 CA157 CA158 CA159
CA160 CA161 CA162 CA163 CA164 CA165 CA166 CA167 CA168 CA169
CA170 CA171 CA172 CA173 CA174 CA175 CA176 CA177 CA178 CA179
CA180 CA181 CA182 CA183 CA184 CA185 CA186 CA187 CA188 CA189
CA190 CA191
11UF 20% 2.5V X6T 0402

OMIT_TABLE

UA100
SEBRING-A0
FCCSP

SYM 1 OF 2

VDDH: B4 B11 C3 C4 C7 C8 C11 C12 D1 D7 D8 D14 E3 E4 E11 E12 F1 F14 G3 G4 G7 G8 G11 G12 H1 H7 H8 H14 J3 J4 J11 J12 K4 K11

VDD_DIG: M6
VDDIO: M4
VDDC: M9
VDDC1: M11

153 60 59 58 57 PP0V8_S2SW_CLVR_VDDDIG
153 61 60 59 58 57 PP1V2_S2SW_CLVR_VDDIO

138S00073
CA130 10UF 20% 6.3V CER-X6S 0402
CA131 10UF 20% 6.3V CER-X6S 0402

153 58 57 PP1V8_S2SW
59 58 57 56 153 60 PP1V8_S2SW_CLVR_VDDC1

XWA100 SHORT-20L-0.1MM-SM
XWA101 SHORT-20L-0.1MM-SM

RAIL0_FB: L9 — 152 IN PVDDANE_FB
RAIL01_VSS_FB: K8 — C0_BUCK0_1_SVSS
RAIL2_FB: L6 — 152 IN PVDDPCPU0_FB
RAIL23_VSS_FB: K7 — C0_BUCK2_3_SVSS
RAIL1_FB: L8 — 152 IN PVDDANESRAM_FB
RAIL3_FB: L7 — 152 IN PVDDPCPUSRAM0_FB

SVDDH (CRASH@1.6V): M7 — 152 61 60 59 58 57 56 PPVDDH_S1_CLVR

VOUTA00 L13 — PPVDD_ANE_AWAKESW 61 152
VOUTB00 L11
VOUTA01 K13
VOUTB01 K10
VOUTA02 J13
VOUTB02 J10
VOUTA03 H13
VOUTB03 H10
VOUTA04 G13
VOUTB04 G10
VOUTA05 F13 — PPVDD_ANE_SRAM_AWAKESW 152
VOUTB05 F10
VOUTA06 E13
VOUTB06 E10
VOUTA07 D13
VOUTB07 D10
VOUTA08 C13
VOUTB08 C10
VOUTA09 B13
VOUTB09 B10
VOUTA10 J9
VOUTB10 J6
VOUTA11 H9
VOUTB11 H6
VOUTA12 G9 — PPVDD_PCPU0_AWAKESW 61 152
VOUTB12 G6
VOUTA13 F9
VOUTB13 F6
VOUTA14 E9
VOUTB14 E6
VOUTA15 D9
VOUTB15 D6
VOUTA16 C9
VOUTB16 C6
VOUTA17 B9
VOUTB17 B6
VOUTA18 L4
VOUTB18 L2
VOUTA19 K5
VOUTB19 K2
VOUTA20 J5
VOUTB20 J2
VOUTA21 H5
VOUTB21 H2
VOUTA22 G5 — PPVDD_PCPU_SRAM0_AWAKESW 152
VOUTB22 G2
VOUTA23 F5
VOUTB23 F2
VOUTA24 E5
VOUTB24 E2
VOUTA25 D5
VOUTB25 D2
VOUTA26 C5
VOUTB26 C2
VOUTA27 B5
VOUTB27 B2

BUCK0/HP0
Vboot=?V

BUCK1/LP0
Vboot=?V

BUCK2/HP1
Vboot=?V

BUCK3/LP1
Vboot=?V

OMIT_TABLE

UA100
SEBRING-A0
FCCSP

SYM 2 OF 2

VSS: A1 A2 A4 A6 A9 A11 A14 B3 B7 B8 B12 D3 D4 D11 D12 E1 E7 E8 E14 F3 F4 F7 F8 F11 F12 H3 H4 H11 H12 J1 J7 J8 J14 K3 K6 K9 K12 L5 L10 M1 M14

VSSC: M8 — XWA102 SHORT-20L-0.1MM-SM — 2 CLVR0_VSSC

GPIO[0] B1 CLVR_ANE_ILIMIT_L — OUT 5
GPIO[1] A12 NC_CLVR0_GPIO1
GPIO[2] C1 CLVR_PCPU0_ILIMIT_L — OUT 5
GPIO[3] G1 NC_CLVR0_GPIO3
GPIO[4] G14 NC_CLVR0_GPIO4
GPIO[5] B14 NC_CLVR0_GPIO5

JTAG_TCK M12 SWD_CLVR0_SWCLK — IN 12
JTAG_TMS L12 SWD_CLVR0_SWDIO — BI 12
JTAG_TDI A13
JTAG_TDO A10 NC_TDO0
JTAG_TRSTN C14

ATB[0] A7 NC_ATB00
ATB[1] A8 NC_ATB01
ATB[2] A5 NC_ATB02
ATB[3] A3 NC_ATB03

SGPIO_CLK L1 SGPIO_CLVR0_CLK — IN 38
SGPIO_D K1 SGPIO_CLVR0_DATA — BI 38
ADDR0 M5 GND — IN 61
ADDR1 M3 PP1V2_S2SW_CLVR_VDDIO — IN 61

SPMI_SCLK K14 SPMI_CLVR0_CLK — IN 12
SPMI_SDATA L14 SPMI_CLVR0_DATA — BI 12

CRASH* M13 CLVR_CRASH_L — BI 38 57 58 59 60 145
UT* M2 NC_CLVR0_UT_L — 156

CLK32K M10 PMU_CLK32K_CLVR — IN 38 57 58 59 60 145
RESET* L3 CLVR_RESET_L — IN 46 57 58 59 60 145

153 60 59 58 57 56 PP1V8_S2SW_CLVR_VDDC1

138S00377
CA122 2.2UF 20% 6.3V X6S 0201
CA123 2.2UF 20% 6.3V X6S 0201
CA124 2.2UF 20% 6.3V X6S 0201
CA125 2.2UF 20% 6.3V X6S 0201

1x 2.2uF should be placed near UA100
1x 2.2uF should be placed near UA300
For CA124, CA125 placement guidance, refer to rdar://104493789

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
998-32699	1	IC,PMU,SEBRING,B0,OTP-MPI,DEV,FCCSP168	UA100	CRITICAL	

BOM_COST_GROUP=SOC POWER

PAGE TITLE: CLVR0

Apple Inc.

DRAWING NUMBER: 051-08286
SIZE: D
REVISION: 5.0.3
BRANCH:
PAGE: 101 OF 700
SHEET: 56 OF 168

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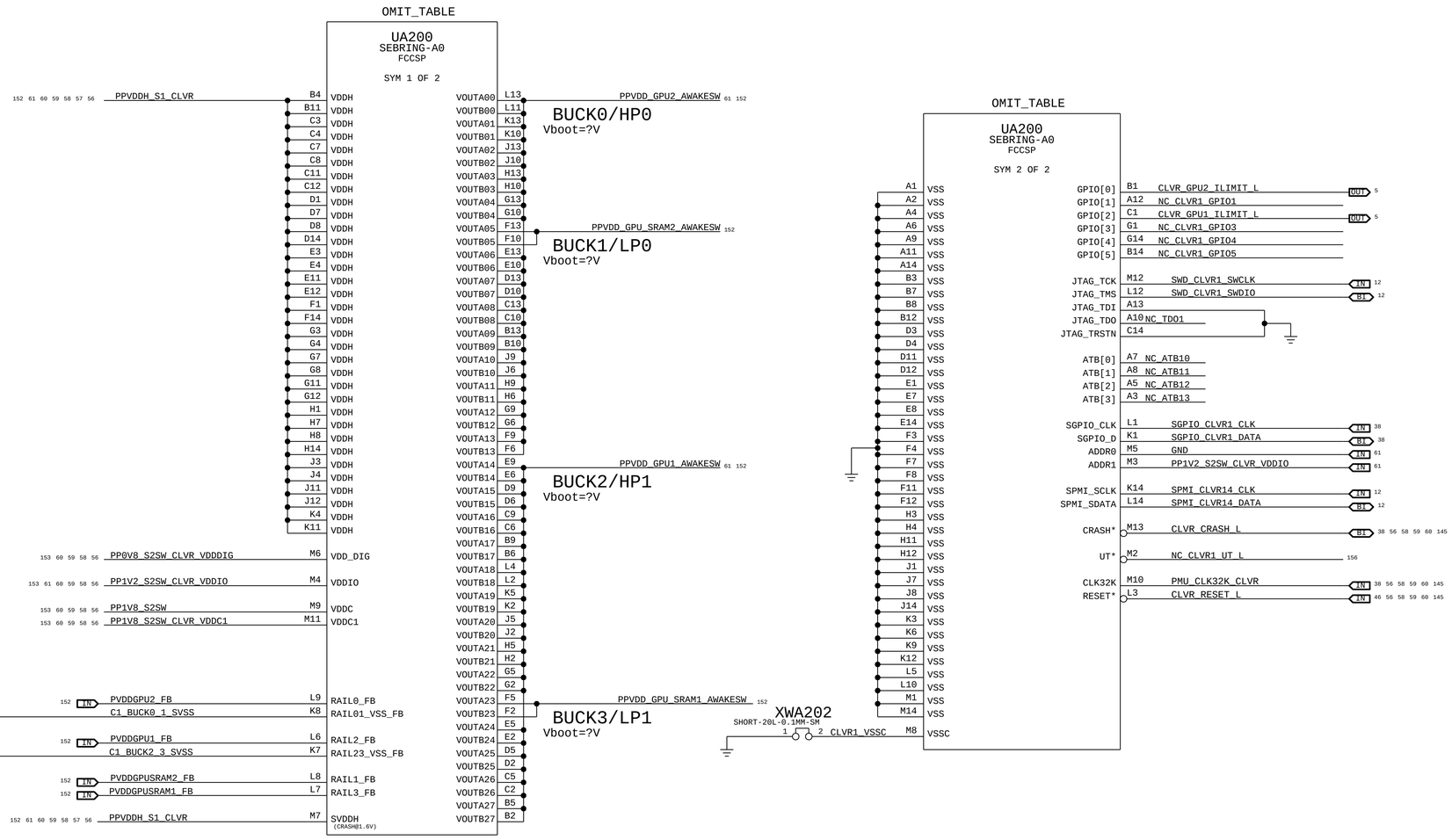
OK2INTEGRATE

INSTANCE = C1
CFG = A (13+1+13+1)
OTP = AP_



TODO: Update with APN

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
998-32696	1	IC,PMU,SEBRING,B0,OTP-API,DEV,FCCSP168	UA200	CRITICAL	

BOM_COST_GROUP=SOC POWER

PAGE TITLE
CLVR1

Apple Inc.

DRAWING NUMBER 051-08286
SIZE D
REVISION 5.0.3
BRANCH
PAGE 102 OF 700
SHEET 57 OF 168

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OK2INTEGRATE

VDDH 11uF caps to be distributed across all CLVRs in layout
11UF APN: 138S00328

INSTANCE = C2
CFG = A (13+1+13+1)
OTP = AP_

OMIT_TABLE

UA300
SEBRING-A0
FCCSP

SYM 1 OF 2

152 61 60 59 58 57 56 PPVDDH_S1_CLVR

B4	VDDH	VOUTA00	L13
B11	VDDH	VOUTB00	L11
C3	VDDH	VOUTA01	K13
C4	VDDH	VOUTB01	K10
C7	VDDH	VOUTA02	J13
C8	VDDH	VOUTB02	J10
C11	VDDH	VOUTA03	H13
C12	VDDH	VOUTB03	H10
D1	VDDH	VOUTA04	G13
D7	VDDH	VOUTB04	G10
D8	VDDH	VOUTA05	F13
D14	VDDH	VOUTB05	F10
E3	VDDH	VOUTA06	E13
E4	VDDH	VOUTB06	E10
E11	VDDH	VOUTA07	D13
E12	VDDH	VOUTB07	D10
F1	VDDH	VOUTA08	C13
F14	VDDH	VOUTB08	C10
G3	VDDH	VOUTA09	B13
G4	VDDH	VOUTB09	B10
G7	VDDH	VOUTA10	J9
G8	VDDH	VOUTB10	J6
G11	VDDH	VOUTA11	H9
G12	VDDH	VOUTB11	H6
H1	VDDH	VOUTA12	G9
H7	VDDH	VOUTB12	G6
H8	VDDH	VOUTA13	F9
H14	VDDH	VOUTB13	F6
J3	VDDH	VOUTA14	E9
J4	VDDH	VOUTB14	E6
J11	VDDH	VOUTA15	D9
J12	VDDH	VOUTB15	D6
K4	VDDH	VOUTA16	C9
K11	VDDH	VOUTB16	C6
		VOUTA17	B9
		VOUTB17	B6
		VOUTA18	L4
		VOUTB18	L2
		VOUTA19	K5
		VOUTB19	K2
		VOUTA20	J5
		VOUTB20	J2
		VOUTA21	H5
		VOUTB21	H2
		VOUTA22	G5
		VOUTB22	G2
		VOUTA23	F5
		VOUTB23	F2
		VOUTA24	E5
		VOUTB24	E2
		VOUTA25	D5
		VOUTB25	D2
		VOUTA26	C5
		VOUTB26	C2
		VOUTA27	B5
		VOUTB27	B2

PPVDD_GPU0_AWAKESW 61 152

BUCK0/HP0
Vboot=?V

PPVDD_GPU_SRAM0_AWAKESW 152

BUCK1/LP0
Vboot=?V

PPVDD_GPU3_AWAKESW 61 152

BUCK2/HP1
Vboot=?V

PPVDD_GPU_SRAM3_AWAKESW 152

BUCK3/LP1
Vboot=?V

153 60 59 57 56 PP0V8_S2SW_CLVR_VDDDIG → M6 VDD_DIG
153 61 60 59 57 56 PP1V2_S2SW_CLVR_VDDIO → M4 VDDIO
153 60 59 57 56 PP1V8_S2SW → M9 VDDC
153 60 59 57 56 PP1V8_S2SW_CLVR_VDDC1 → M11 VDDC1

XWA300
SHORT-20L-0.1MM-SM
1 2

152 IN PVDDGPU0_FB → L9 RAIL0_FB
C2_BUCK0_1_SVSS → K8 RAIL01_VSS_FB

XWA301
SHORT-20L-0.1MM-SM
1 2

152 IN PVDDGPU3_FB → L6 RAIL2_FB
C2_BUCK2_3_SVSS → K7 RAIL23_VSS_FB

152 IN PVDDGPUSRAM0_FB → L8 RAIL1_FB
152 IN PVDDGPUSRAM3_FB → L7 RAIL3_FB

152 61 60 59 58 57 56 PPVDDH_S1_CLVR → M7 SVDDH (CRASH@1.6V)

OMIT_TABLE

UA300
SEBRING-A0
FCCSP

SYM 2 OF 2

A1	VSS	GPIO[0]	B1	CLVR_GPU0_ILIMIT_L	OUT 5
A2	VSS	GPIO[1]	A12	NC_CLVR2_GPIO1	
A4	VSS	GPIO[2]	C1	CLVR_GPU3_ILIMIT_L	OUT 5
A6	VSS	GPIO[3]	G1	NC_CLVR2_GPIO3	
A9	VSS	GPIO[4]	G14	NC_CLVR2_GPIO4	
A11	VSS	GPIO[5]	B14	NC_CLVR2_GPIO5	
A14	VSS				
B3	VSS	JTAG_TCK	M12	SWD_CLVR2_SWCLK	IN 12
B7	VSS	JTAG_TMS	L12	SWD_CLVR2_SWDIO	BI 12
B8	VSS	JTAG_TDI	A13		
B12	VSS	JTAG_TDO	A10	NC_TDO2	
D3	VSS	JTAG_TRSTN	C14		
D4	VSS				
D11	VSS	ATB[0]	A7	NC_ATB20	
D12	VSS	ATB[1]	A8	NC_ATB21	
E1	VSS	ATB[2]	A5	NC_ATB22	
E7	VSS	ATB[3]	A3	NC_ATB23	
E8	VSS				
E14	VSS	SGPIO_CLK	L1	SGPIO_CLVR2_CLK	IN 38
F3	VSS	SGPIO_D	K1	SGPIO_CLVR2_DATA	BI 38
F4	VSS	ADDR0	M5	PP1V2_S2SW_CLVR_VDDIO	IN 61
F7	VSS	ADDR1	M3	PP1V2_S2SW_CLVR_VDDIO	IN 61
F8	VSS				
F11	VSS	SPMI_SCLK	K14	SPMI_CLVR23_CLK	IN 12
F12	VSS	SPMI_SDATA	L14	SPMI_CLVR23_DATA	BI 12
H3	VSS				
H4	VSS	CRASH*	M13	CLVR_CRASH_L	BI 38 56 57 59 60 145
H11	VSS				
H12	VSS	UT*	M2	NC_CLVR2_UT_L	156
J1	VSS				
J7	VSS	CLK32K	M10	PMU_CLK32K_CLVR	IN 38 56 57 59 60 145
J8	VSS	RESET*	L3	CLVR_RESET_L	IN 46 56 57 59 60 145
J14	VSS				
K3	VSS				
K6	VSS				
K9	VSS				
K12	VSS				
L5	VSS				
L10	VSS				
M1	VSS				
M14	VSS				
M8	VSSC				

XWA302
SHORT-20L-0.1MM-SM
1 2 CLVR2_VSSC

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
998-32696	1	IC,PMU,SEBRING,B0,OTP-API,DEV,FCCSP168	UA300	CRITICAL	

BOM_COST_GROUP=SOC POWER

PAGE TITLE
CLVR2

Apple Inc.

DRAWING NUMBER 051-08286
SIZE D
REVISION 5.0.3
BRANCH
PAGE 103 OF 700
SHEET 58 OF 168

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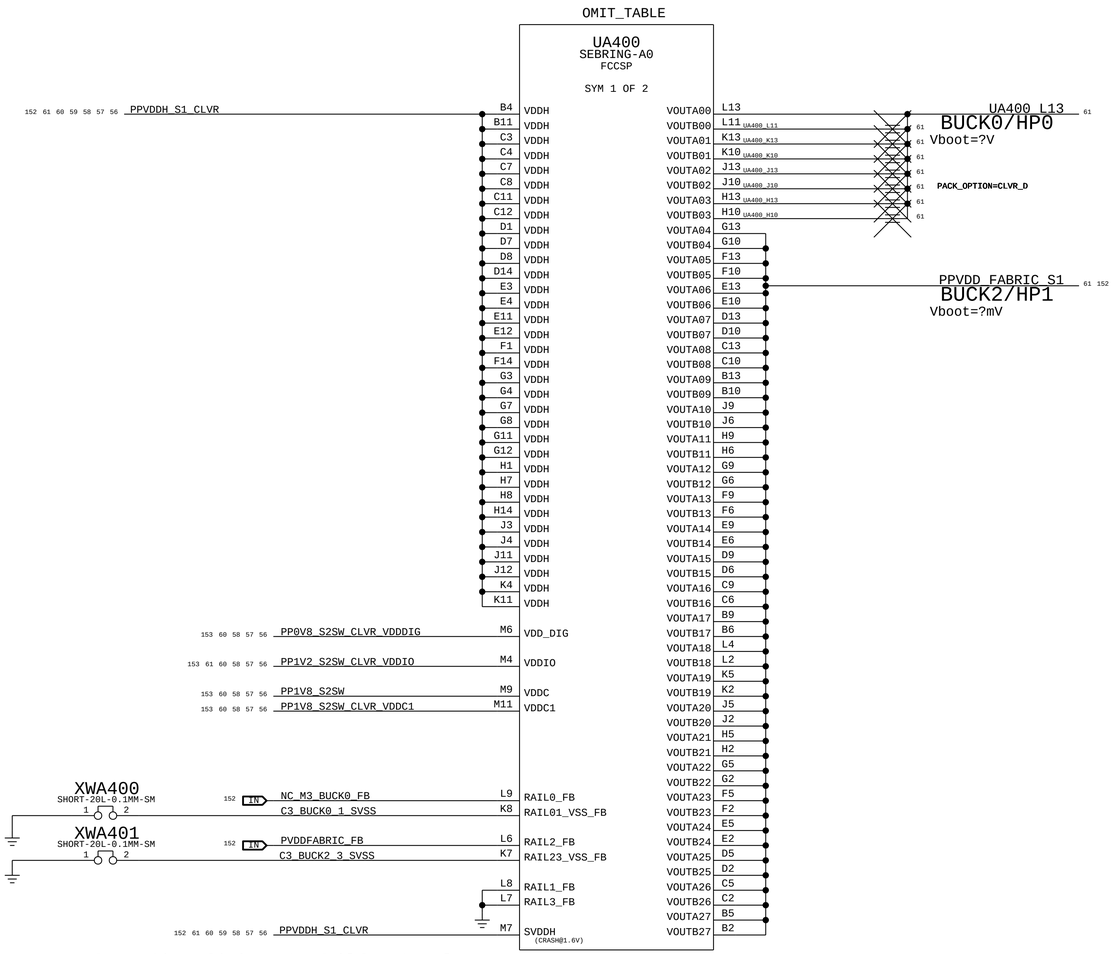
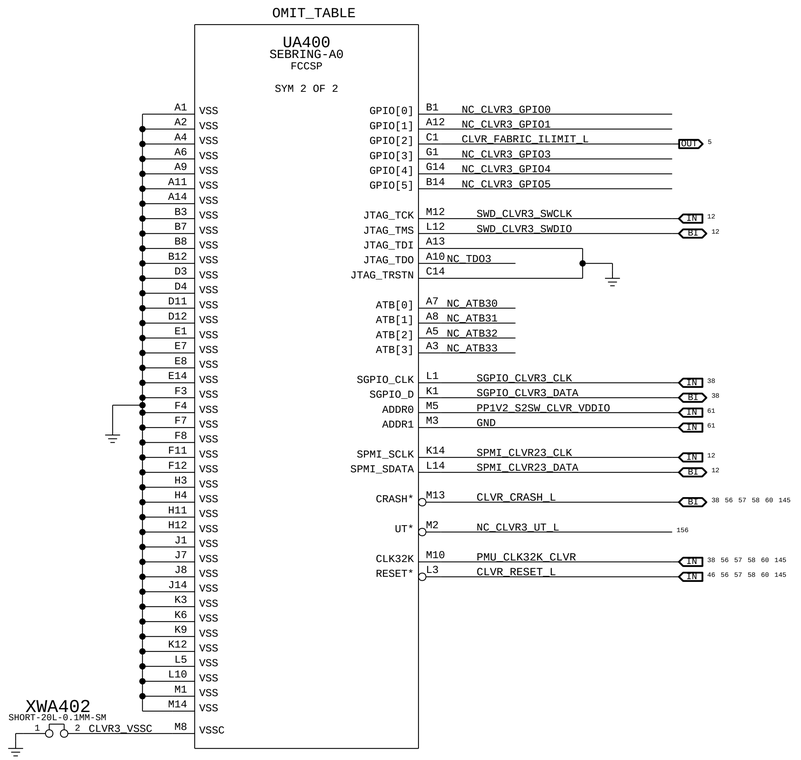
OK2INTEGRATE

INSTANCE = C3
CFG = E (4+0+24+0)
OTP = EP_



SVDD_LP0/1 could change to NC if layout prefers



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
998-32697	1	IC,PMU,SEBRING,B0,OTP-EPI,DEV,FCCSP168	UA400	CRITICAL	

BOM_COST_GROUP=SOC POWER

PAGE TITLE
CLVR3

Apple Inc.

DRAWING NUMBER 051-08286
SIZE D
REVISION 5.0.3
BRANCH
PAGE 104 OF 700
SHEET 59 OF 168

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OK2INTEGRATE

INSTANCE = C4
CFG = G (14+0+12+2)
OTP = IP_

OMIT_TABLE

UA500
SEBRING-A0
FCCSP

SYM 1 OF 2

152 61 60 59 58 57 56 PPVDDH_S1_CLVR	B4	VDDH	VOUTA00	L13	PPVDD_AFR_CS_S1 61 152
	B11	VDDH	VOUTB00	L11	
	C3	VDDH	VOUTA01	K13	BUCK0/HP0
	C4	VDDH	VOUTB01	K10	Vboot=?V
	C7	VDDH	VOUTA02	J13	
	C8	VDDH	VOUTB02	J10	
	C11	VDDH	VOUTA03	H13	
	C12	VDDH	VOUTB03	H10	
	D1	VDDH	VOUTA04	G13	
	D7	VDDH	VOUTB04	G10	
	D8	VDDH	VOUTA05	F13	
	D14	VDDH	VOUTB05	F10	
	E3	VDDH	VOUTA06	E13	
	E4	VDDH	VOUTB06	E10	
	E11	VDDH	VOUTA07	D13	
	E12	VDDH	VOUTB07	D10	
	F1	VDDH	VOUTA08	C13	
	F14	VDDH	VOUTB08	C10	
	G3	VDDH	VOUTA09	B13	
	G4	VDDH	VOUTB09	B10	
	G7	VDDH	VOUTA10	J9	
	G8	VDDH	VOUTB10	J6	
	G11	VDDH	VOUTA11	H9	
	G12	VDDH	VOUTB11	H6	
	H1	VDDH	VOUTA12	G9	
	H7	VDDH	VOUTB12	G6	
	H8	VDDH	VOUTA13	F9	
	H14	VDDH	VOUTB13	F6	
	J3	VDDH	VOUTA14	E9	PPVDD_PCPU1_AWAKESW 61 152
	J4	VDDH	VOUTB14	E6	
	J11	VDDH	VOUTA15	D9	BUCK2/HP1
	J12	VDDH	VOUTB15	D6	Vboot=?V
	K4	VDDH	VOUTA16	C9	
	K11	VDDH	VOUTB16	C6	
			VOUTA17	B9	
			VOUTB17	B6	
			VOUTA18	L4	
			VOUTB18	L2	
			VOUTA19	K5	
			VOUTB19	K2	
			VOUTA20	J5	
			VOUTB20	J2	
			VOUTA21	H5	
			VOUTB21	H2	
			VOUTA22	G5	PPVDD_PCPU_SRAM1_AWAKESW 152
			VOUTB22	G2	BUCK3/LP1
			VOUTA23	F5	Vboot=?V
			VOUTB23	F2	
			VOUTA24	E5	
			VOUTB24	E2	
			VOUTA25	D5	
			VOUTB25	D2	
			VOUTA26	C5	
			VOUTB26	C2	
			VOUTA27	B5	
			VOUTB27	B2	
153 59 58 57 56 PP0V8_S2SW_CLVR_VDDDIG	M6	VDD_DIG			
153 61 59 58 57 56 PP1V2_S2SW_CLVR_VDDIO	M4	VDDIO			
153 59 58 57 56 PP1V8_S2SW	M9	VDDC			
153 59 58 57 56 PP1V8_S2SW_CLVR_VDDC1	M11	VDDC1			
	M7	SVDDH (CRASH@1.6V) (UT@1.67V)			

XWA500
SHORT-20L-0.1MM-SM
1 2

152 IN PVDDAFRCS_FB
C4_BUCK0_1_SVSS

XWA501
SHORT-20L-0.1MM-SM
1 2

152 IN PVDDPCPU1_FB
C4_BUCK2_3_SVSS

152 IN PVDDPCPUSRAM1_FB

	L9	RAIL0_FB
	K8	RAIL01_VSS_FB
	L6	RAIL2_FB
	K7	RAIL23_VSS_FB
	L8	RAIL1_FB
	L7	RAIL3_FB

PLACE_NEAR=XW9400:8MM
RA530
22
1% 1/20W TK 0201
152 61 60 59 58 57 56 PPVDDH_S1_CLVR
P1V8S1CLVR_VDDH_SENSE

KEEP BELOW 25 OHM FOR ONE SVDDH

PLACE_NEAR=UA500.M7:5MM
CA530
470PF
5% 25V C0G 0201
FILTER CUTOFF: 15MHZ

OMIT_TABLE

UA500
SEBRING-A0
FCCSP

SYM 2 OF 2

	A1	VSS	GPIO[0]	B1	CLVR_AFR_ILIMIT_L OUT 5
	A2	VSS	GPIO[1]	A12	NC_CLVR4_GPIO1
	A4	VSS	GPIO[2]	C1	CLVR_PCPU1_ILIMIT_L OUT 5
	A6	VSS	GPIO[3]	G1	NC_CLVR4_GPIO3
	A9	VSS	GPIO[4]	G14	NC_CLVR4_GPIO4
	A11	VSS	GPIO[5]	B14	NC_CLVR4_GPIO5
	A14	VSS			
	B3	VSS	JTAG_TCK	M12	SWD_CLVR4_SWCLK IN 12
	B7	VSS	JTAG_TMS	L12	SWD_CLVR4_SWDIO BI 12
	B8	VSS	JTAG_TDI	A13	
	B12	VSS	JTAG_TDO	A10	NC_TDO4
	D3	VSS	JTAG_TRSTN	C14	
	D4	VSS			
	D11	VSS	ATB[0]	A7	NC_ATB40
	D12	VSS	ATB[1]	A8	NC_ATB41
	E1	VSS	ATB[2]	A5	NC_ATB42
	E7	VSS	ATB[3]	A3	NC_ATB43
	E8	VSS			
	E14	VSS	SGPIO_CLK	L1	SGPIO_CLVR4_CLK IN 38
	F3	VSS	SGPIO_D	K1	SGPIO_CLVR4_DATA BI 38
	F4	VSS	ADDR0	M5	PP1V2_S2SW_CLVR_VDDIO IN 61
	F7	VSS	ADDR1	M3	GND IN 61
	F8	VSS			
	F11	VSS	SPMI_SCLK	K14	SPMI_CLVR14_CLK IN 12
	F12	VSS	SPMI_SDATA	L14	SPMI_CLVR14_DATA BI 12
	H3	VSS			
	H4	VSS	CRASH*	M13	CLVR_CRASH_L BI 38 56 57 58 59 145
	H11	VSS			
	H12	VSS	UT*	M2	CLVR_VDDH_UVWARN_L OUT 5
	J1	VSS			
	J7	VSS	CLK32K	M10	PMU_CLK32K_CLVR IN 38 56 57 58 59 145
	J8	VSS	RESET*	L3	CLVR_RESET_L IN 46 56 57 58 59 145
	J14	VSS			
	K3	VSS			
	K6	VSS			
	K9	VSS			
	K12	VSS			
	L5	VSS			
	L10	VSS			
	M1	VSS			
	M14	VSS			
	M8	VSSC			

XWA502
SHORT-20L-0.1MM-SM
1 2 CLVR4_VSSC

BOM_COST_GROUP=SOC POWER

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
998-32698	1	IC,PMU,SEBRING,B0,OTP-IPI,DEV,FCCSP168	UA500	CRITICAL	

PAGE TITLE
CLVR4

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DRAWING NUMBER 051-08286
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CLVR SPMI Probe Access

CLVR SPMI Probe Access are removed for DVT onwards

CLVR Throttle Probe Access

CLVR SPMI Probe Access PPs are remvoed for DVT onwards

CLVR Address Straps

SWD TINSTANCE and SGPIO SID are the same value within a given CLVR
ADDR[1:0] define LSB
OTP defines MSB

CLVR	Hex	MSB (OTP)	LSB (ADDR strap)	
0	0x6	b01	b10 :	56 OUT GND — GND MAKE_BASE=TRUE 56 OUT PP1V2_S2SW_CLVR_VDDIO — PP1V2_S2SW_CLVR_VDDIO 56 57 58 59 60 61 153
1	0x2	b00	b10 :	57 OUT GND — GND MAKE_BASE=TRUE 57 OUT PP1V2_S2SW_CLVR_VDDIO — PP1V2_S2SW_CLVR_VDDIO 56 57 58 59 60 61 153
2	0x3	b00	b11 :	58 OUT PP1V2_S2SW_CLVR_VDDIO — PP1V2_S2SW_CLVR_VDDIO 56 57 58 59 60 61 153 58 OUT PP1V2_S2SW_CLVR_VDDIO — PP1V2_S2SW_CLVR_VDDIO 56 57 58 59 60 61 153
3	0x9	b10	b01 :	59 OUT PP1V2_S2SW_CLVR_VDDIO — PP1V2_S2SW_CLVR_VDDIO 56 57 58 59 60 61 153 59 OUT GND — GND MAKE_BASE=TRUE
4	0x1	b00	b01 :	60 OUT PP1V2_S2SW_CLVR_VDDIO — PP1V2_S2SW_CLVR_VDDIO 56 57 58 59 60 61 153 60 OUT GND — GND MAKE_BASE=TRUE

CLVR Output Desense Caps (MLB Only)

152 56 PPVDD_ANE_AWAKESW
CA140 12PF 5% 25V NP0-C0G 0201
CA141 3.0PF +/-0.1PF 25V NP0-C0G 0201
CA142 1.8PF +/-0.1PF 25V C0G 201

152 56 PPVDD_PCPU0_AWAKESW
CA145 12PF 5% 25V NP0-C0G 0201
CA146 3.0PF +/-0.1PF 25V NP0-C0G 0201
CA147 1.8PF +/-0.1PF 25V C0G 201

152 57 PPVDD_GPU2_AWAKESW
CA240 12PF 5% 25V NP0-C0G 0201
CA241 3.0PF +/-0.1PF 25V NP0-C0G 0201
CA242 1.8PF +/-0.1PF 25V C0G 201

152 57 PPVDD_GPU1_AWAKESW
CA245 12PF 5% 25V NP0-C0G 0201
CA246 3.0PF +/-0.1PF 25V NP0-C0G 0201
CA247 1.8PF +/-0.1PF 25V C0G 201

152 58 PPVDD_GPU0_AWAKESW
CA340 12PF 5% 25V NP0-C0G 0201
CA341 3.0PF +/-0.1PF 25V NP0-C0G 0201
CA342 1.8PF +/-0.1PF 25V C0G 201

152 58 PPVDD_GPU3_AWAKESW
CA345 12PF 5% 25V NP0-C0G 0201
CA346 3.0PF +/-0.1PF 25V NP0-C0G 0201
CA347 1.8PF +/-0.1PF 25V C0G 201

61 59 UA400_L13
CA440 12PF 5% 25V NP0-C0G 0201
CA441 3.0PF +/-0.1PF 25V NP0-C0G 0201
CA442 1.8PF +/-0.1PF 25V C0G 201
PACK_IGNORE=TRUE
PACK_OPTION=CLVR_D

152 59 PPVDD_FABRIC_S1
CA445 12PF 5% 25V NP0-C0G 0201
CA446 3.0PF +/-0.1PF 25V NP0-C0G 0201
CA447 1.8PF +/-0.1PF 25V C0G 201

152 60 PPVDD_AFR_CS_S1
CA540 12PF 5% 25V NP0-C0G 0201
CA541 3.0PF +/-0.1PF 25V NP0-C0G 0201
CA542 1.8PF +/-0.1PF 25V C0G 201

152 60 PPVDD_PCPU1_AWAKESW
CA545 12PF 5% 25V NP0-C0G 0201
CA546 3.0PF +/-0.1PF 25V NP0-C0G 0201
CA547 1.8PF +/-0.1PF 25V C0G 201

CLVR0 Desense Caps

PPVDDH_S1_CLVR 56 57 58 59 60 152

CA250 1.8PF +/-0.1PF 25V C0G 201
CA251 3.0PF +/-0.1PF 25V NP0-C0G 0201
CA252 12PF 5% 25V NP0-C0G 0201
CA253 1.8PF +/-0.1PF 25V C0G 201
CA254 3.0PF +/-0.1PF 25V NP0-C0G 0201
CA255 12PF 5% 25V NP0-C0G 0201
CA256 1.8PF +/-0.1PF 25V C0G 201
CA257 3.0PF +/-0.1PF 25V NP0-C0G 0201
CA258 12PF 5% 25V NP0-C0G 0201

CLVR1 Desense Caps

CA260 1.8PF +/-0.1PF 25V C0G 201
CA261 3.0PF +/-0.1PF 25V NP0-C0G 0201
CA262 12PF 5% 25V NP0-C0G 0201
CA263 1.8PF +/-0.1PF 25V C0G 201
CA264 3.0PF +/-0.1PF 25V NP0-C0G 0201
CA265 12PF 5% 25V NP0-C0G 0201

CLVR2 Desense Caps

CA270 1.8PF +/-0.1PF 25V C0G 201
CA271 3.0PF +/-0.1PF 25V NP0-C0G 0201
CA272 12PF 5% 25V NP0-C0G 0201
CA273 1.8PF +/-0.1PF 25V C0G 201
CA274 3.0PF +/-0.1PF 25V NP0-C0G 0201
CA275 12PF 5% 25V NP0-C0G 0201

CLVR3 Desense Caps

CA280 1.8PF +/-0.1PF 25V C0G 201
CA281 3.0PF +/-0.1PF 25V NP0-C0G 0201
CA282 12PF 5% 25V NP0-C0G 0201
CA283 1.8PF +/-0.1PF 25V C0G 201
CA284 3.0PF +/-0.1PF 25V NP0-C0G 0201
CA285 12PF 5% 25V NP0-C0G 0201
CA286 1.8PF +/-0.1PF 25V C0G 201
CA287 3.0PF +/-0.1PF 25V NP0-C0G 0201
CA288 12PF 5% 25V NP0-C0G 0201

CLVR4 Desense Caps

CA290 1.8PF +/-0.1PF 25V C0G 201
CA291 3.0PF +/-0.1PF 25V NP0-C0G 0201
CA292 12PF 5% 25V NP0-C0G 0201
CA293 1.8PF +/-0.1PF 25V C0G 201
CA294 3.0PF +/-0.1PF 25V NP0-C0G 0201
CA295 12PF 5% 25V NP0-C0G 0201

CLVR resolution between C/D deltas (C only)

CLVR3 BUCK0 is NC/unused in C, but the pins need net names to allow rel vias in pad

61 59 UA400_L13 — UA400_L13 MAKE_BASE=TRUE CKPLUS_WAIVE=SINGLE_NODENET

I65	UA400_L11	CKPLUS_WAIVE=SINGLE_NODENET 59
I66	UA400_K10	CKPLUS_WAIVE=SINGLE_NODENET 59
I67	UA400_K13	CKPLUS_WAIVE=SINGLE_NODENET 59
I68	UA400_J10	CKPLUS_WAIVE=SINGLE_NODENET 59
I69	UA400_J13	CKPLUS_WAIVE=SINGLE_NODENET 59
I70	UA400_H10	CKPLUS_WAIVE=SINGLE_NODENET 59
I71	UA400_H13	CKPLUS_WAIVE=SINGLE_NODENET 59

BOM_COST_GROUP=SOC POWER

PAGE TITLE: CLVR PROJECT SUPPORT

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* OK2INTEGRATE *

5V_S2 Voltage Regulator (low power option)

SET ONE OPTION FOR PBUS CAPS

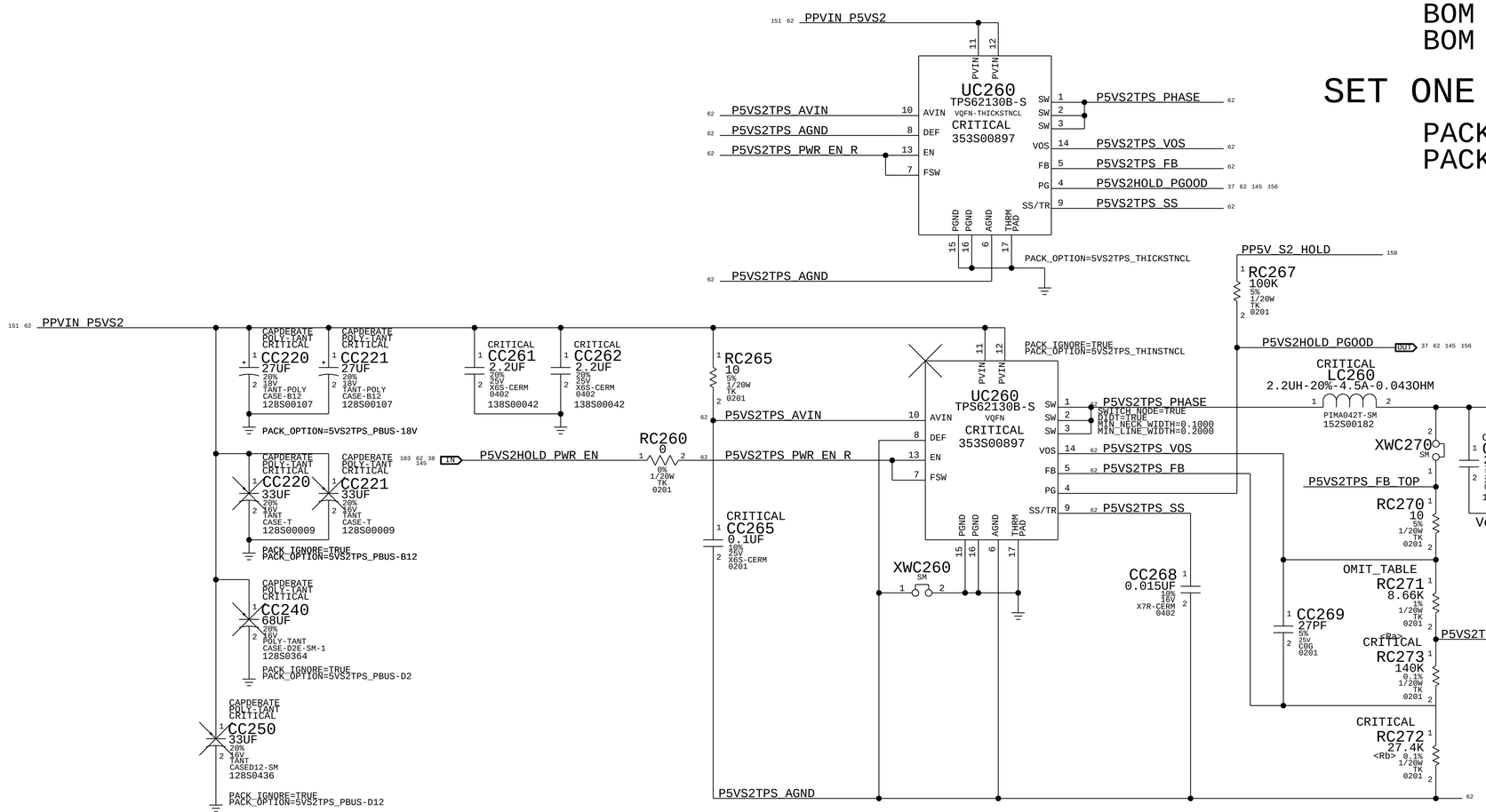
PACK_OPTION=5VS2TPS_PBUS-B12
PACK_OPTION=5VS2TPS_PBUS-D2
PACK_OPTION=5VS2TPS_PBUS-D12
PACK_OPTION=5VS2TPS_PBUS-18V

SET ONE OPTION FOR OUTPUT VOLTAGE

BOM OPTION=5VS2TPS_VOUT:5V140
BOM OPTION=5VS2TPS_VOUT:5V232

SET ONE OPTION FOR UC260

PACK_OPTION=5VS2TPS_THINSTNCL
PACK_OPTION=5VS2TPS_THICKSTNCL

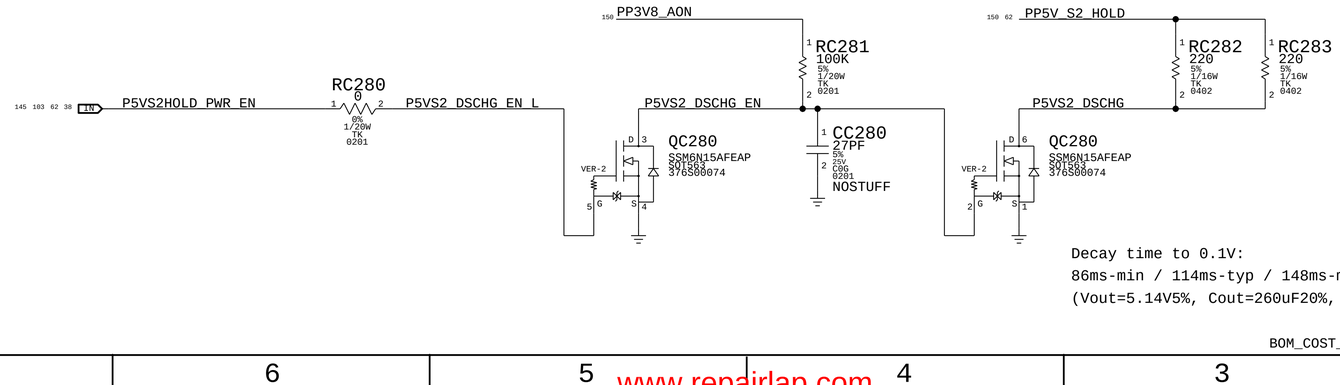


Start up time = 4.7/7.5/10.5 ms
(min/typ/max)

Vout-nom = 5.14V / 5.232V (BOM options)
Iout Max = 2.1A
f = 1.25 MHZ

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
118S00394	1	RES,0201,8.66K,1%,1/20W	RC271	5VS2TPS_VOUT:5V140
118S00536	1	RES,0201,11.8K,1%,1/20W	RC271	5VS2TPS_VOUT:5V232

Vout of 5.232V, rdar://80397668



Decay time to 0.1V:
86ms-min / 114ms-typ / 148ms-max
(Vout=5.14V5%, Cout=260uF20%, R=2x220R5%)

BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE: POWER: 5V S2 TPS62130

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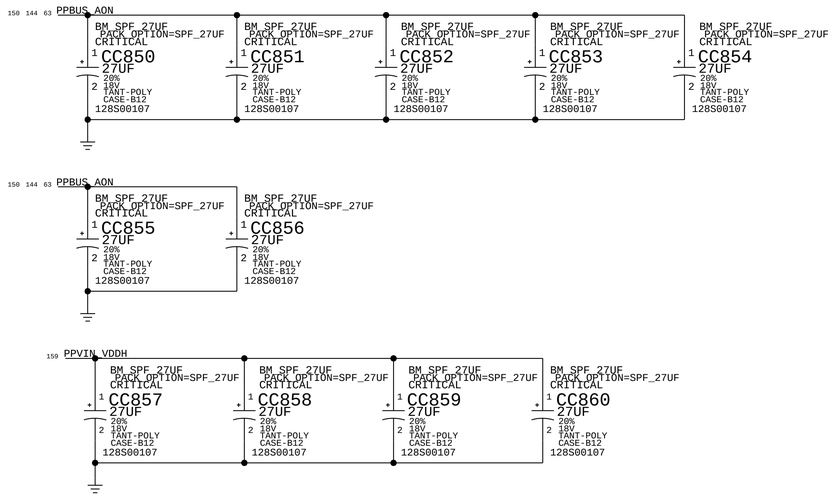

BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE
SPF 27UF Caps

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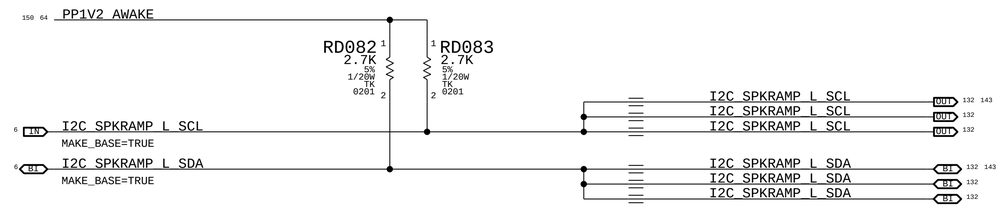
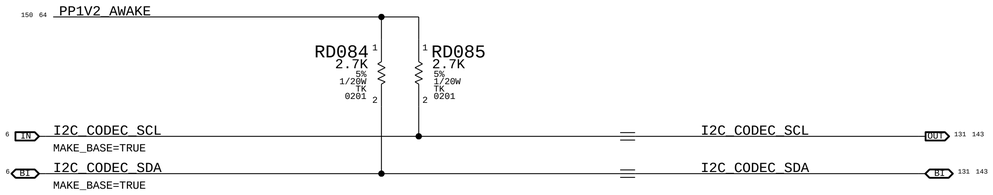
AP_I2C1

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
AP	1	400kHz	0x38	0x70	SPKRAMP_TAWANG_A
AP	1	400kHz	0x39	0x72	SPKRAMP_TAWANG_B
AP	1	400kHz	0x3A	0x74	SPKRAMP_TAWANG_C



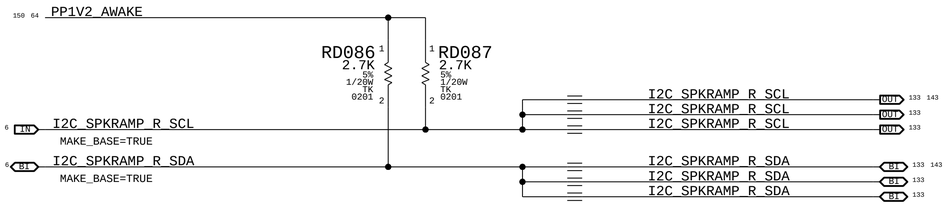
AP_I2C2

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
AP	2	400kHz	0x48	0x90	CODEC - CLIFDEN
AP	2	400kHz	0x4B	0x95	CODEC - CARLOW (POR)



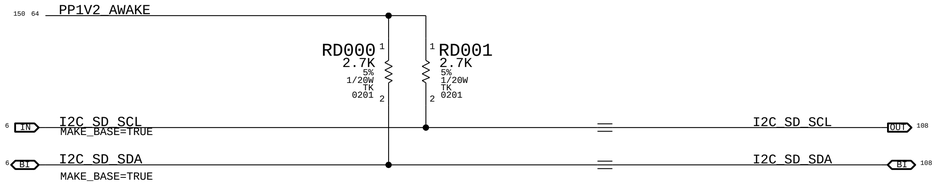
AP_I2C3

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
AP	3	400kHz	0x3B	0x76	SPKRAMP_TAWANG_D
AP	3	400kHz	0x3C	0x78	SPKRAMP_TAWANG_E
AP	3	400kHz	0x3D	0x7A	SPKRAMP_TAWANG_F



AP_I2C4

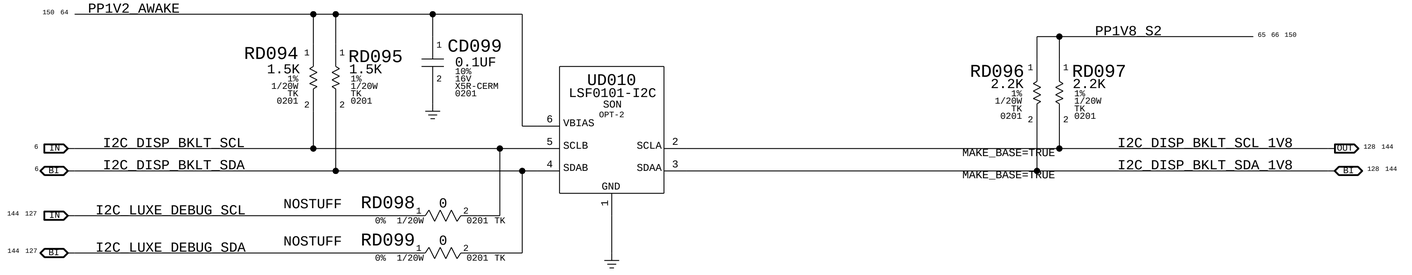
MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
AP	4	100kHz	0x6A	0xD4	SDCARD



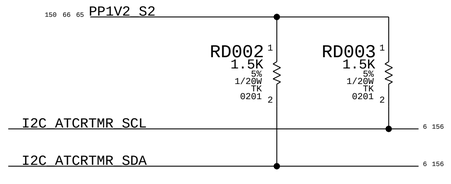
AP_I2C7

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
AP	7	400KHz	0X44	0X88	Aveillino PMIC

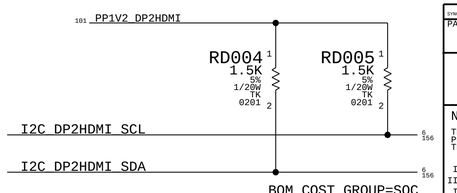
I2C is hooked up to testpoints on BCON brd



AP_I2C6



AP_I2C8



SYNC_MASTER=MLB_S_0.64.4 SYNC_DATE=09/11/2022

PAGE TITLE

I2C Connections - AP

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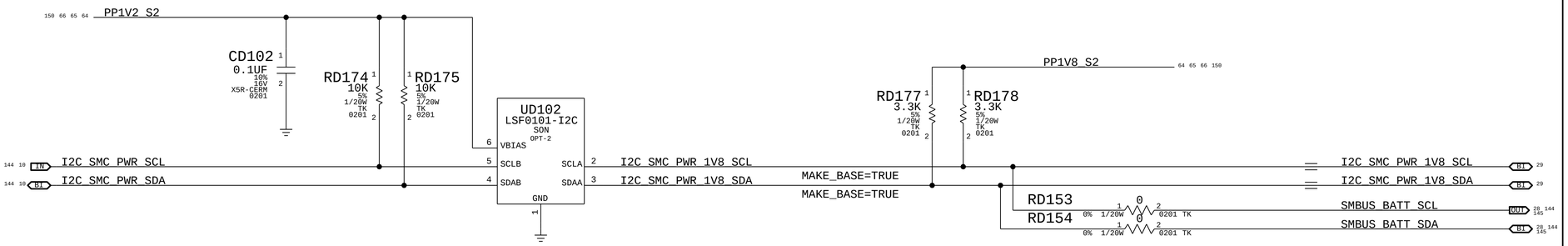
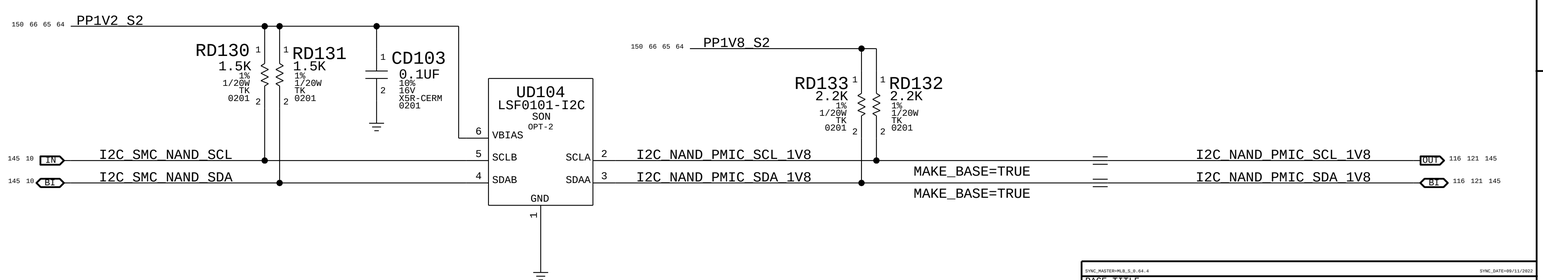


SMC_I2C1

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
SMC	1	100kHz	0X09	0X12	CHARGER - MANDOLA
SMC	1	100kHz	0X0B	0X16	BMU

SMC_I2C2

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
SMC	2	100kHz	0X79	0XF2	NAND PMIC 0
SMC	2	100kHz	0X78	0XF0	NAND PMIC 1



BOM_COST_GROUP=SOC

SYNC_MASTER=MLB_3_0_64_4 SYNC_DATE=09/11/2022

PAGE TITLE

I2C Connections - SMC

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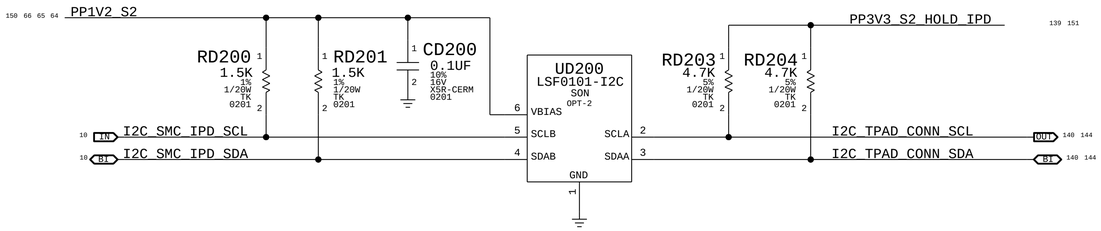
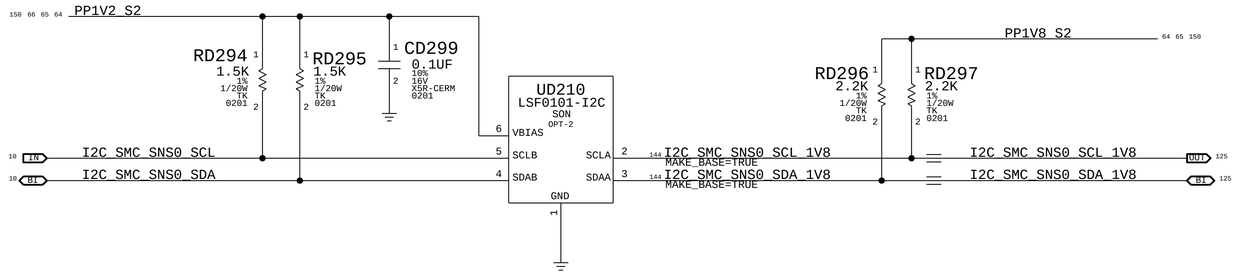
SMC_I2C3

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
SMC	3	100kHz	0X4C	0X98	Palm Rest Temp



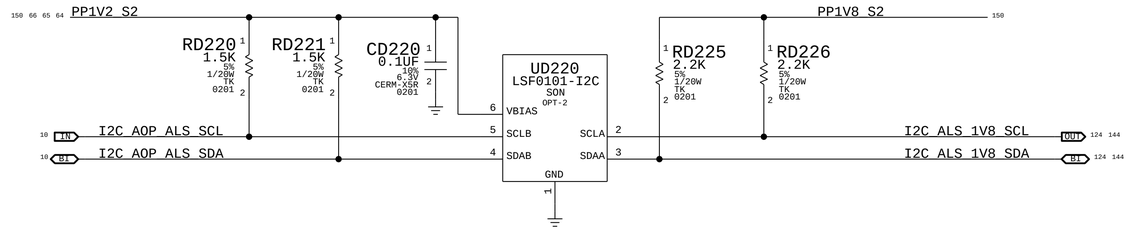
SMC_I2C4

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
SMC	4	100kHz	0X48	0X90	Temp Sensors



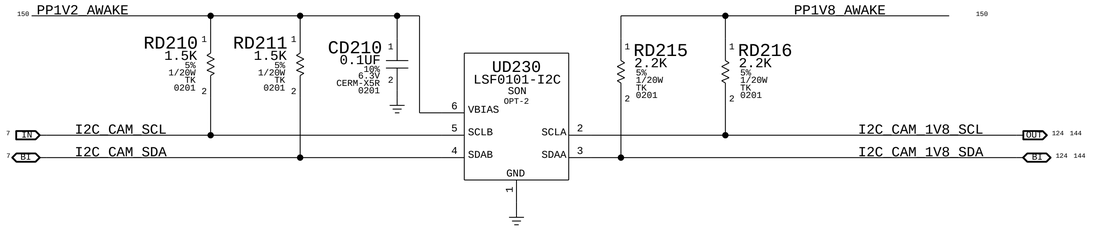
AOP_I2C0

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
AOP	0	400kHz	0X29	0X52	ALS
AOP	0	400kHz	0X24	0X48	ALS Temp



ISP_I2C0

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
ISP	0	400kHz	0X10	0X20	FHS1+
ISP	0	400kHz	0X6C	0XD8	Camera Sensor



UNUSED and already aliased

ISP_I2C1	SMC_I2C5	AP_I2C0	AP_SPI3	AOP_I2C1
ISP_I2C2	SMC_I2C6	AP_I2C5	AP_SPI5	AP_I2S3
ISP_I2C3				

SI2C0

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
S	0	400kHz	0XXX	0XX	SEP EEPROM

Pull-ups on CSA19

MISSING WLAN/BT, R1, CELL - VENDOR CARDS

BOM_COST_GROUP=SOC

SYNC_MASTER=K26D2_JIAPENG_WANG2_MLB_S_0.86.4 SYNC_DATE=09/11/2022

PAGE TITLE: I2C Connections - Other

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DRAWING NUMBER: 051-08286 SIZE: D
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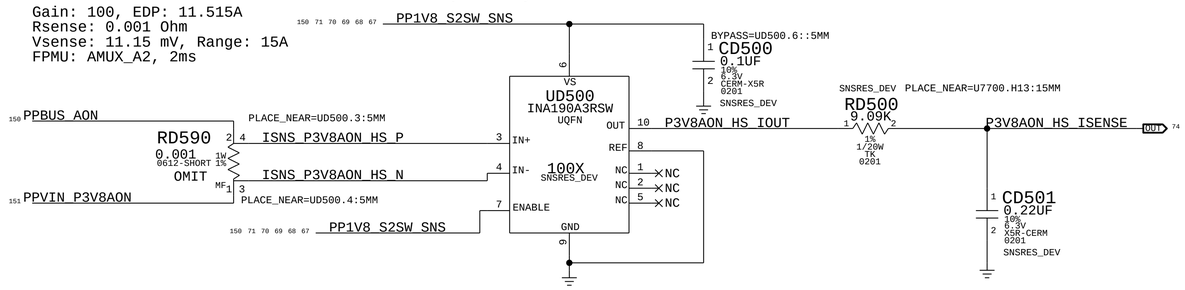
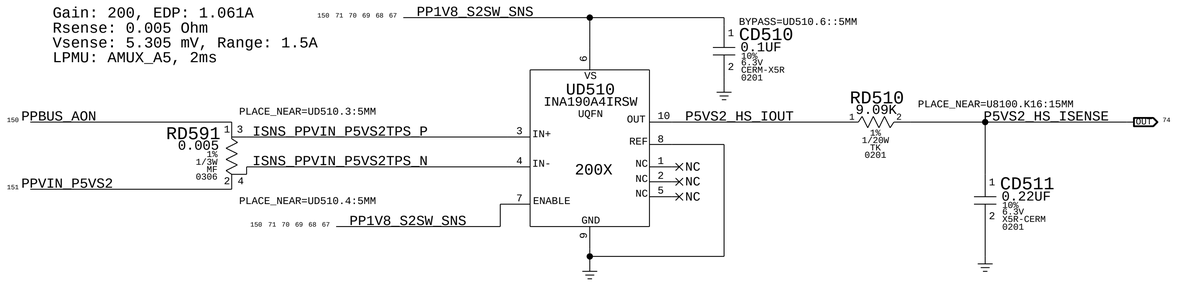
P3V8 AON HIGH SIDE ISENSE (IMVR)

Gain: 100, EDP: 11.515A
Rsense: 0.001 Ohm
Vsense: 11.15 mV, Range: 15A
FPMU: AMUX_A2, 2ms



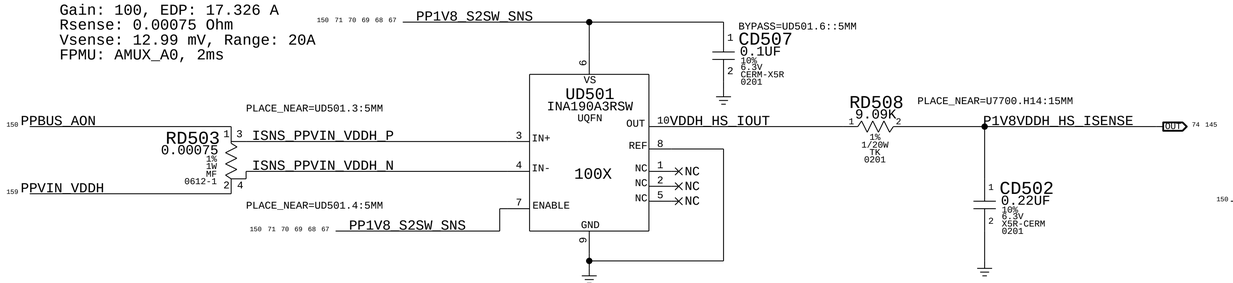
5V S2 VR HIGH SIDE ISENSE (I5SR)

Gain: 200, EDP: 1.061A
Rsense: 0.005 Ohm
Vsense: 5.305 mV, Range: 1.5A
LPMU: AMUX_A5, 2ms



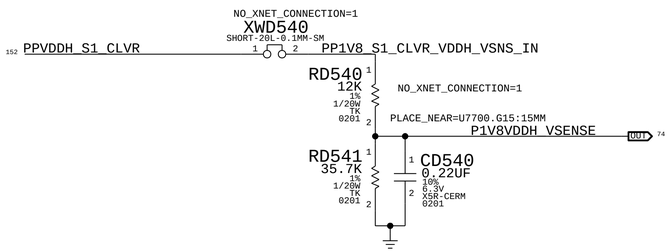
VDDH HIGH SIDE ISENSE (ISVR)

Gain: 100, EDP: 17.326 A
Rsense: 0.00075 Ohm
Vsense: 12.99 mV, Range: 20A
FPMU: AMUX_A0, 2ms



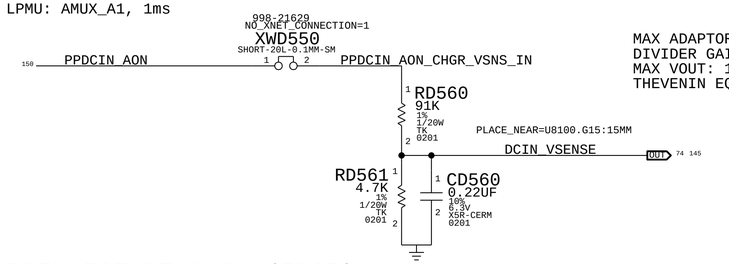
P1V8VDDH VSENSE (VSVR)

FPMU: AMUX_A1, 2ms
P1V8VDDH MAX VOLTAGE: 2V
DIVIDER GAIN:0.748
MAX VOUT:1.5V
THEVENIN EQUIVELENT: 8.98K



DCIN VOLTAGE SENSE (VD0R)

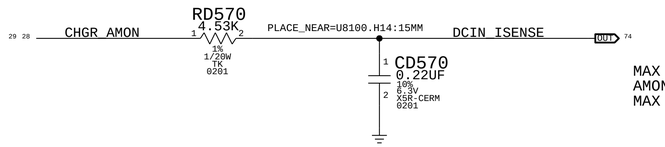
LPMU: AMUX_A1, 1ms



MAX ADAPTOR VOLTAGE = 28V + 5% -> 30V
DIVIDER GAIN: 0.0491
MAX VOUT: 1.4733
THEVENIN EQUIVELENT: 4.47K

DCIN ISENSE AMON (ID0R)

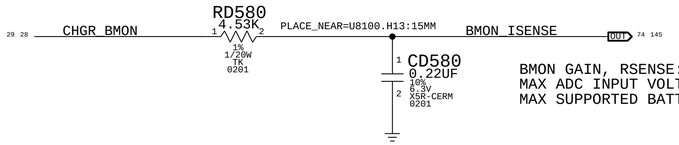
LPMU: AMUX_A0, 1ms



MAX ADAPTOR CURRENT: 5A
AMON GAIN, RSENSE: 20X, 10m
MAX AMON OUTPUT VOLTAGE: 1V

BATTERY ISENSE BMON (IPBR)

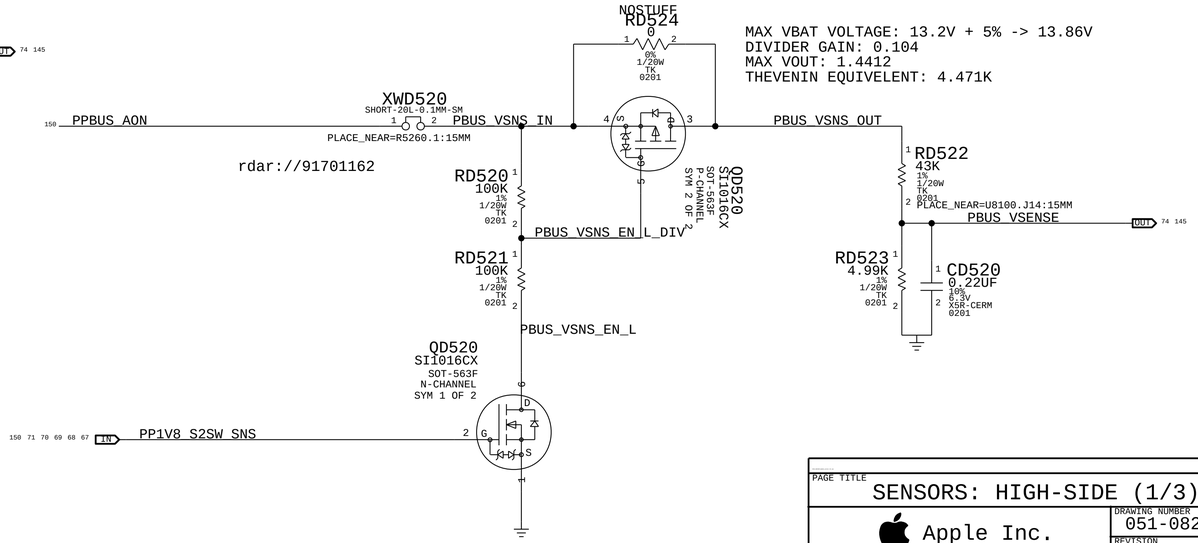
LPMU: AMUX_A2, 1ms



BMON GAIN, RSENSE: 7.9X, 5m
MAX ADC INPUT VOLTAGE: 1.5V (G=1)
MAX SUPPORTED BATTERY CURRENT SENSE: 37.97A

PBUS VOLTAGE SENSE (VP0R)

LPMU: AMUX_A3, 1ms



MAX VBAT VOLTAGE: 13.2V + 5% -> 13.86V
DIVIDER GAIN: 0.104
MAX VOUT: 1.4412
THEVENIN EQUIVELENT: 4.471K

rdar://91701162

BOM_COST_GROUP=SENSORS

PAGE TITLE
SENSORS: HIGH-SIDE (1/3)

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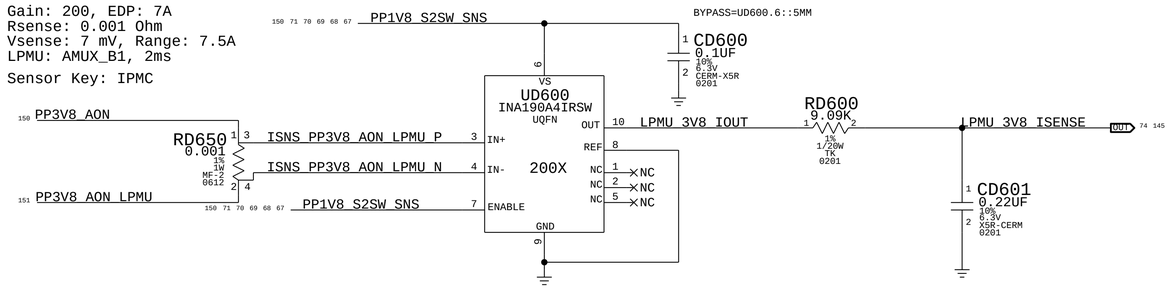
LPMU HIGH SIDE 3V8 ISENSE

Gain: 200, EDP: 7A
Rsense: 0.001 Ohm
Vsense: 7 mV, Range: 7.5A
LPMU: AMUX_B1, 2ms

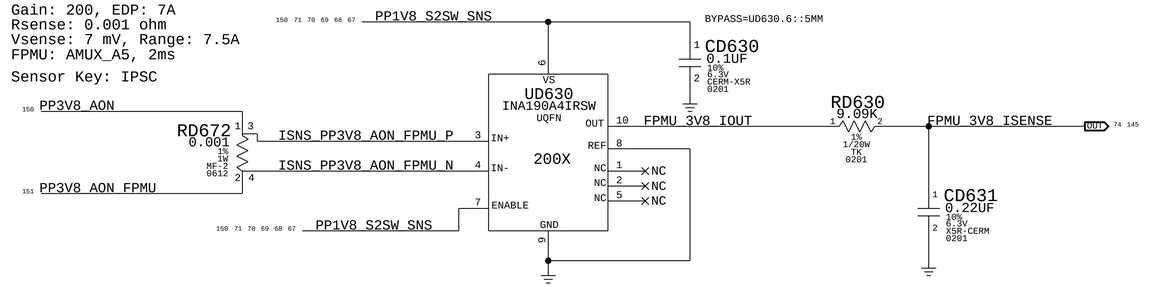
Sensor Key: IPMC



FPMU HIGH SIDE 3V8 ISENSE

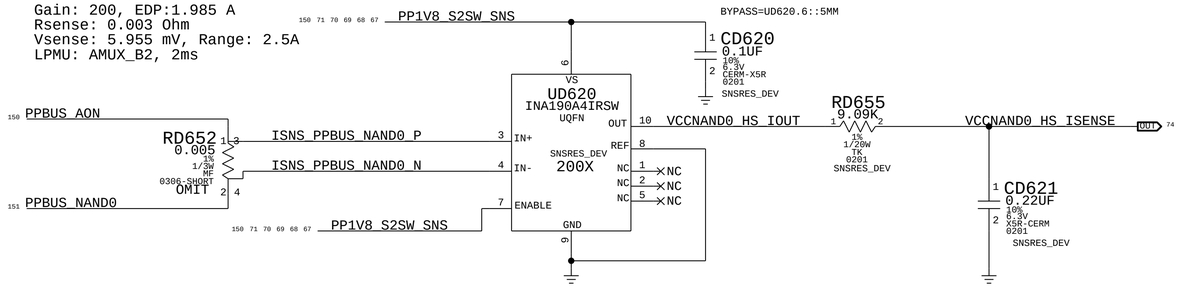
Gain: 200, EDP: 7A
Rsense: 0.001 ohm
Vsense: 7 mV, Range: 7.5A
FPMU: AMUX_A5, 2ms

Sensor Key: IPSC



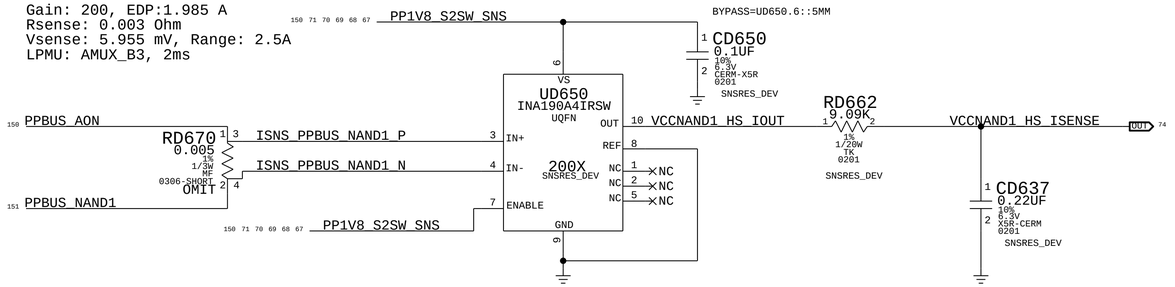
NAND 0 PBUS ISENSE (IH0R)

Gain: 200, EDP:1.985 A
Rsense: 0.003 Ohm
Vsense: 5.955 mV, Range: 2.5A
LPMU: AMUX_B2, 2ms



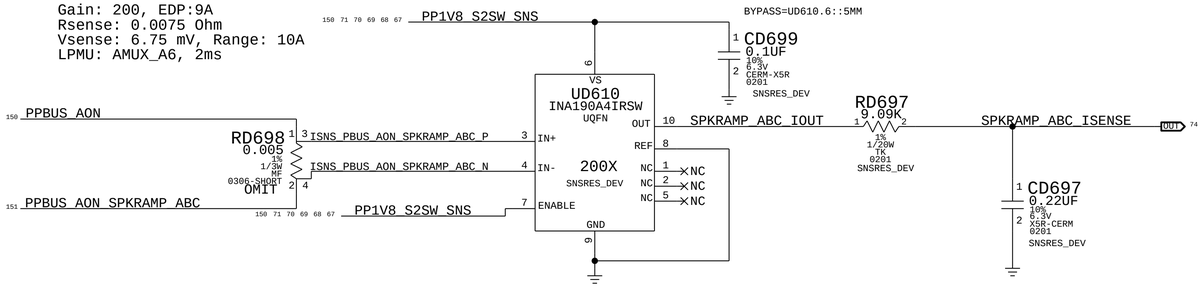
NAND 1 PBUS ISENSE (IH1R)

Gain: 200, EDP:1.985 A
Rsense: 0.003 Ohm
Vsense: 5.955 mV, Range: 2.5A
LPMU: AMUX_B3, 2ms



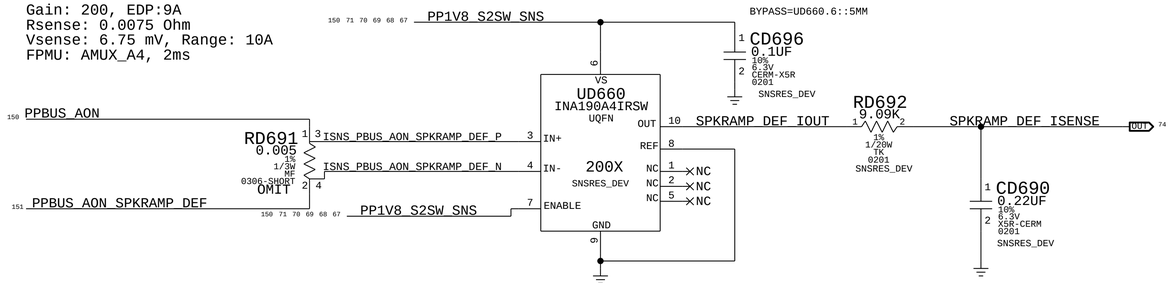
LEFT SPKRAMP PBUS ISENSE (IALR)

Gain: 200, EDP:9A
Rsense: 0.0075 Ohm
Vsense: 6.75 mV, Range: 10A
LPMU: AMUX_A6, 2ms



RIGHT SPKRAMP PBUS ISENSE (IARR)

Gain: 200, EDP:9A
Rsense: 0.0075 Ohm
Vsense: 6.75 mV, Range: 10A
FPMU: AMUX_A4, 2ms



BOM_COST_GROUP=SENSORS

PAGE TITLE
SENSORS: HIGH-SIDE (2/3)

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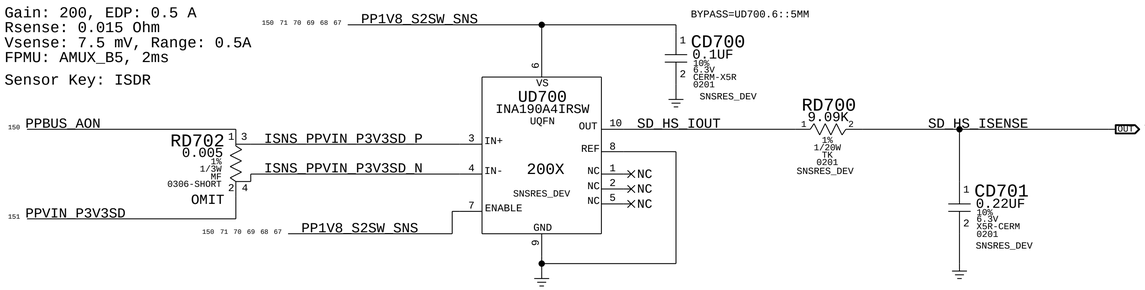
SD PBUS ISENSE

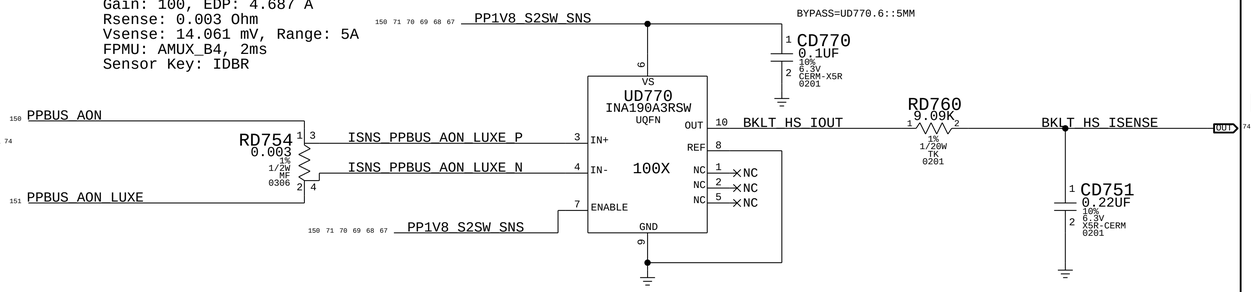
Gain: 200, EDP: 0.5 A
Rsense: 0.015 Ohm
Vsense: 7.5 mV, Range: 0.5A
FPMU: AMUX_B5, 2ms

Sensor Key: ISDR



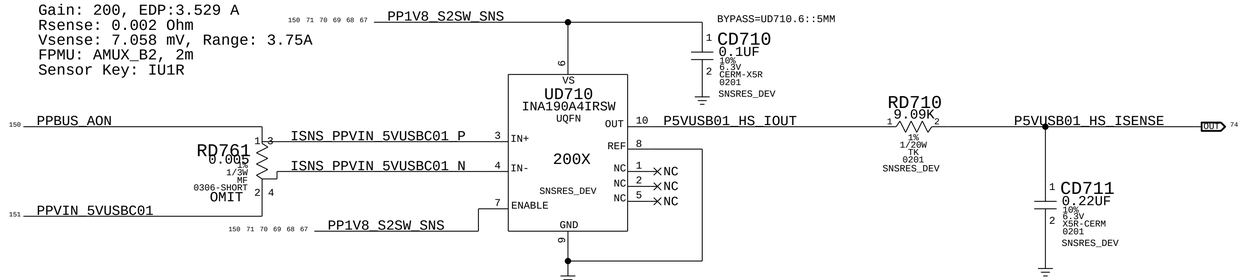
LCD BKLT (LUXE) ISENSE

Gain: 100, EDP: 4.687 A
Rsense: 0.003 Ohm
Vsense: 14.061 mV, Range: 5A
FPMU: AMUX_B4, 2ms
Sensor Key: IDBR



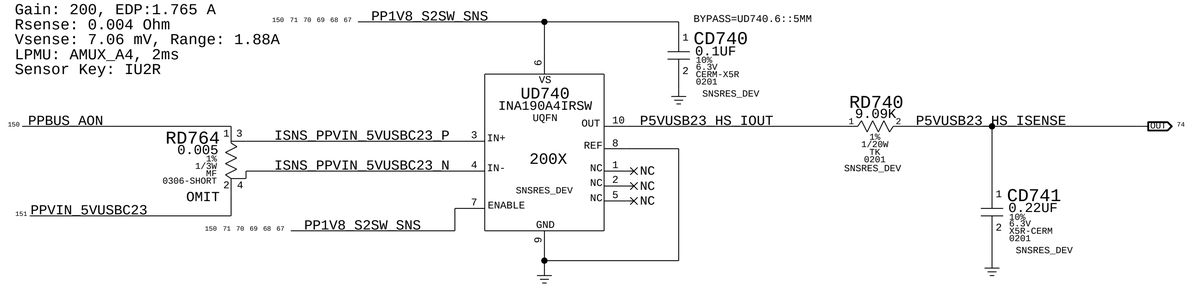
USB 5V OUT LEFT ISENSE

Gain: 200, EDP:3.529 A
Rsense: 0.002 Ohm
Vsense: 7.058 mV, Range: 3.75A
FPMU: AMUX_B2, 2m
Sensor Key: IU1R



USB 5V OUT RIGHT ISENSE

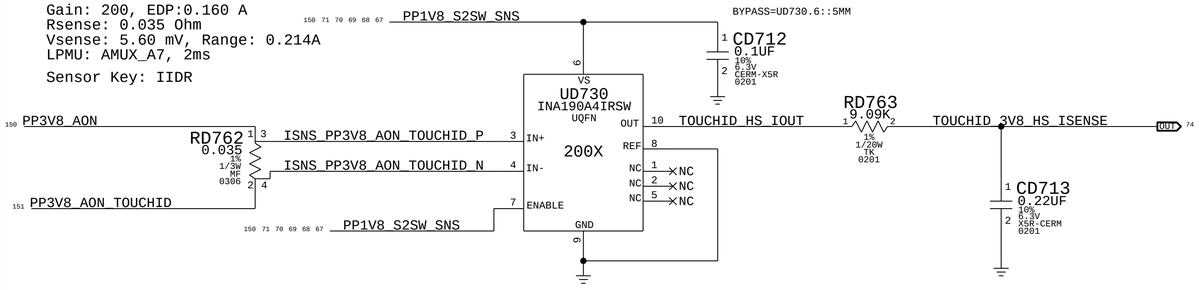
Gain: 200, EDP:1.765 A
Rsense: 0.004 Ohm
Vsense: 7.06 mV, Range: 1.88A
LPMU: AMUX_A4, 2ms
Sensor Key: IU2R



TOUCHID 3V8 ISENSE

Gain: 200, EDP:0.160 A
Rsense: 0.035 Ohm
Vsense: 5.60 mV, Range: 0.214A
LPMU: AMUX_A7, 2ms

Sensor Key: IIDR



PAGE TITLE
SENSORS: HIGH-SIDE(3/3)

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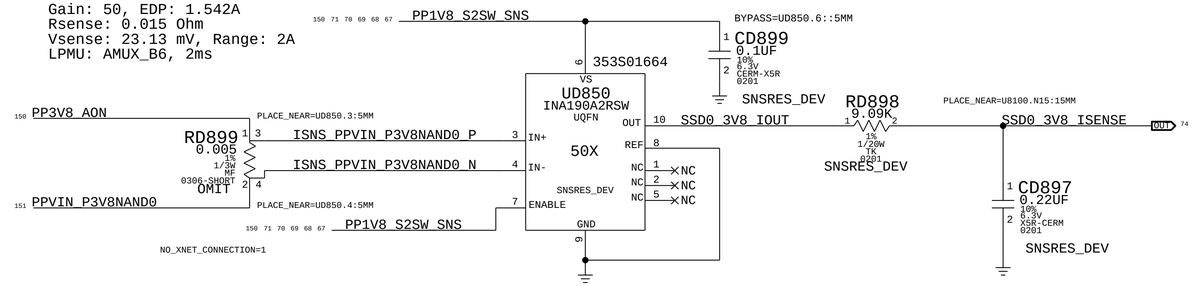
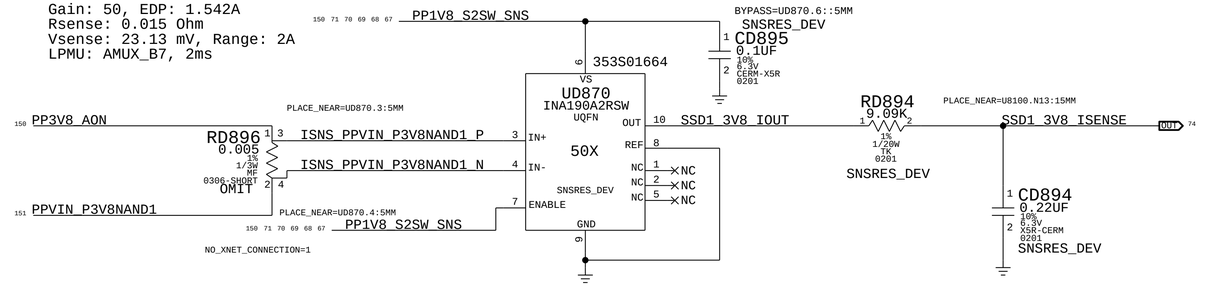
OCARINA 0 ISENSE (IHCR)

Gain: 50, EDP: 1.542A
Rsense: 0.015 Ohm
Vsense: 23.13 mV, Range: 2A
LPMU: AMUX_B6, 2ms



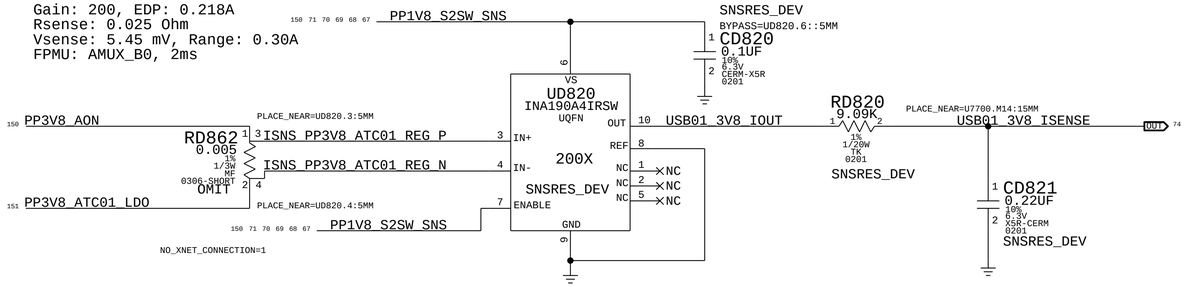
OCARINA 1 ISENSE (IHDR)

Gain: 50, EDP: 1.542A
Rsense: 0.015 Ohm
Vsense: 23.13 mV, Range: 2A
LPMU: AMUX_B7, 2ms



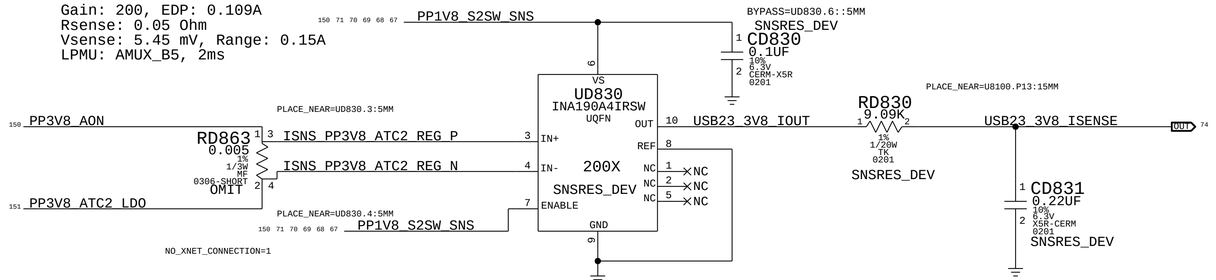
USB 3V8 LEFT ISENSE (IU1C)

Gain: 200, EDP: 0.218A
Rsense: 0.025 Ohm
Vsense: 5.45 mV, Range: 0.30A
FPMU: AMUX_B0, 2ms



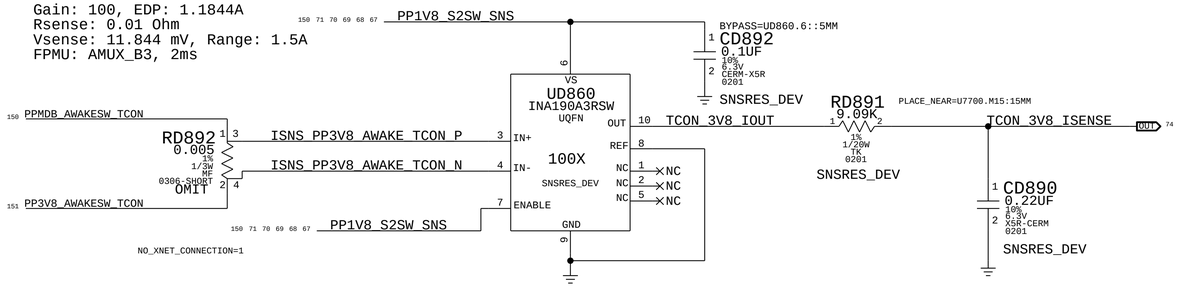
USB 3V8 RIGHT ISENSE (IU2C)

Gain: 200, EDP: 0.109A
Rsense: 0.05 Ohm
Vsense: 5.45 mV, Range: 0.15A
LPMU: AMUX_B5, 2ms



DISPLAY 3V8 ISENSE (ID3C)

Gain: 100, EDP: 1.1844A
Rsense: 0.01 Ohm
Vsense: 11.844 mV, Range: 1.5A
FPMU: AMUX_B3, 2ms



BOM_COST_GROUP=SENSORS

PAGE TITLE: SENSORS: LOW-SIDE (1/3)

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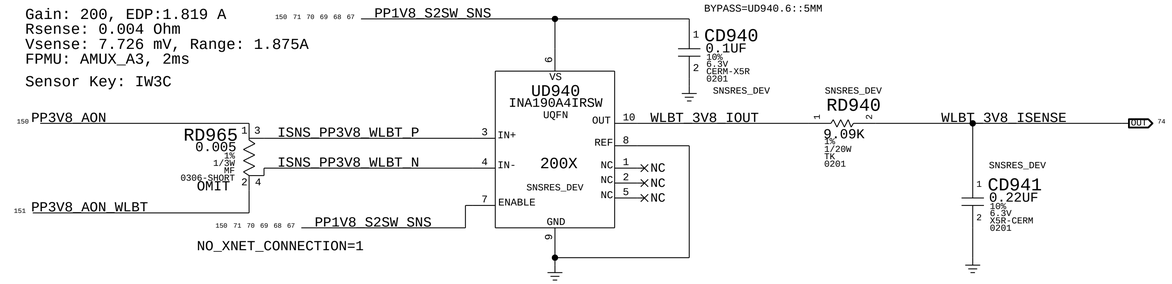
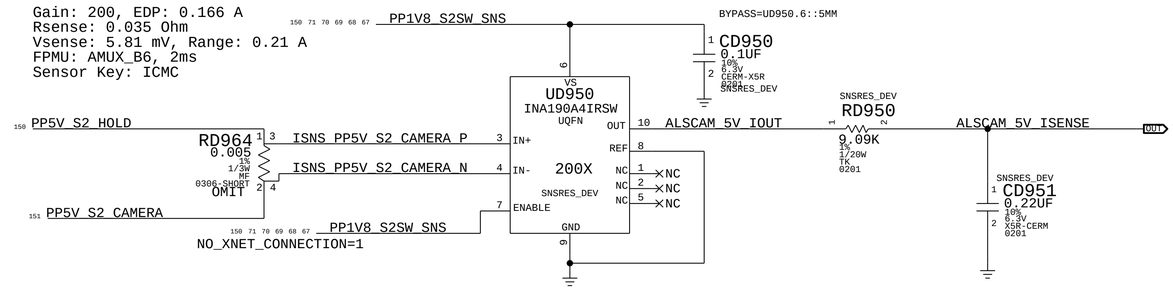
WLAN BT 3V8 ISENSE

Gain: 200, EDP:1.819 A
Rsense: 0.004 Ohm
Vsense: 7.726 mV, Range: 1.875A
FPMU: AMUX_A3, 2ms
Sensor Key: IW3C



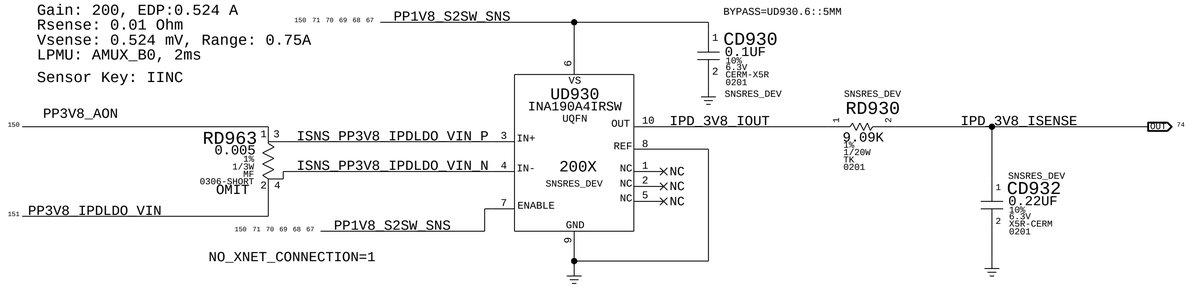
CAMERA/ALS 5V ISENSE

Gain: 200, EDP: 0.166 A
Rsense: 0.035 Ohm
Vsense: 5.81 mV, Range: 0.21 A
FPMU: AMUX_B6, 2ms
Sensor Key: ICMC



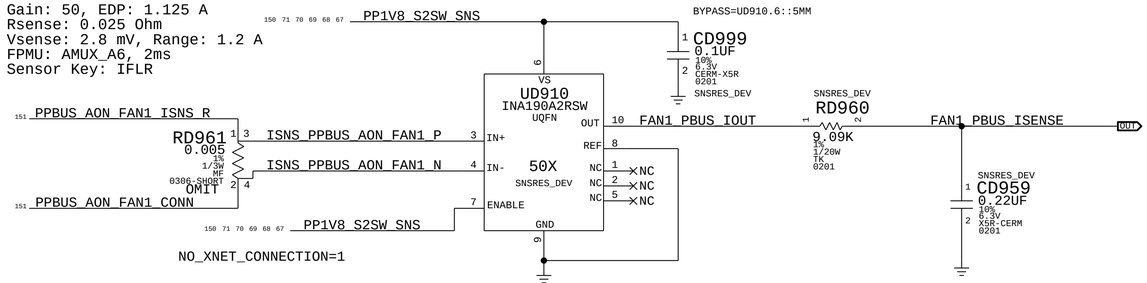
IPD 3V8 ISENSE

Gain: 200, EDP:0.524 A
Rsense: 0.01 Ohm
Vsense: 0.524 mV, Range: 0.75A
LPMU: AMUX_B0, 2ms
Sensor Key: IINC



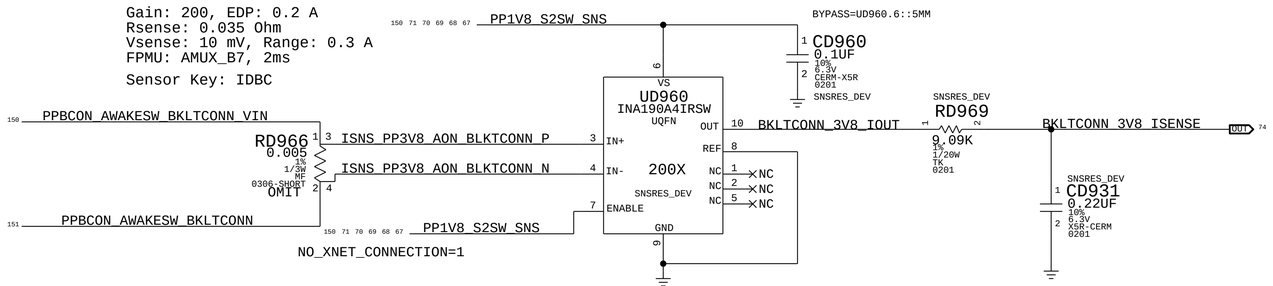
Right Fan (FAN1) PBUS ISENSE

Gain: 50, EDP: 1.125 A
Rsense: 0.025 Ohm
Vsense: 2.8 mV, Range: 1.2 A
FPMU: AMUX_A6, 2ms
Sensor Key: IFLR



DISPLAY BACKLIGHT 3V8 ISENSE

Gain: 200, EDP: 0.2 A
Rsense: 0.035 Ohm
Vsense: 10 mV, Range: 0.3 A
FPMU: AMUX_B7, 2ms
Sensor Key: IDBC



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PAGE TITLE
SENSORS: LOW-SIDE (2/3)

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Ekara phase sense resistors

159 52 PPVDDH_S1_CLVR_REGEXT0 — P1V8VDDH_RISNS1_P 72, P1V8VDDH_RISNS1_N 72
RE060 0.0005 0612-2 MF 1W 1%
NO_XNET_CONNECTION=1

159 52 PPVDDH_S1_CLVR_REGEXT1 — P1V8VDDH_RISNS2_P 72, P1V8VDDH_RISNS2_N 72
RE061 0.0005 0612-2 MF 1W 1%
NO_XNET_CONNECTION=1

159 53 PPVDDH_S1_CLVR_REGEXT2 — P1V8VDDH_RISNS3_P 72, P1V8VDDH_RISNS3_N 72
RE062 0.0005 0612-2 MF 1W 1%
NO_XNET_CONNECTION=1

159 53 PPVDDH_S1_CLVR_REGEXT3 — P1V8VDDH_RISNS4_P 72, P1V8VDDH_RISNS4_N 72
RE063 0.0005 0612-2 MF 1W 1%
NO_XNET_CONNECTION=1

159 54 PPVDDH_S1_CLVR_REGEXT4 — P1V8VDDH_RISNS5_P 72, P1V8VDDH_RISNS5_N 72
RE064 0.0005 0612-2 MF 1W 1%
NO_XNET_CONNECTION=1

PPVDDH_S1_CLVR 49 55 152

P1V8VDDH LOW SIDE ISENSE (SUMMING AMP FOR 5 PHASES)

EDP: 156.2A, 32.24A/PHASE

FPMU AMUX_A7, 2ms
Sensor Key: ISVC
Gain: 96

72 P1V8VDDH_RISNS1_P — NO_XNET_CONNECTION=1 — RE017 30.1K 0.1% 1/20W TK 0201-1 SNSRES_DEV — P1V8VDDH_RISNS_IN_P_R
72 P1V8VDDH_RISNS2_P — NO_XNET_CONNECTION=1 — RE018 30.1K 0.1% 1/20W TK 0201-1 SNSRES_DEV
72 P1V8VDDH_RISNS3_P — NO_XNET_CONNECTION=1 — RE019 30.1K 0.1% 1/20W TK 0201-1 SNSRES_DEV
72 P1V8VDDH_RISNS4_P — NO_XNET_CONNECTION=1 — RE022 30.1K 0.1% 1/20W TK 0201-1 SNSRES_DEV
72 P1V8VDDH_RISNS5_P — NO_XNET_CONNECTION=1 — RE023 30.1K 0.1% 1/20W TK 0201-1 SNSRES_DEV

150 37 PP3V8_AON — RE020 267 0.1% 1/20W TK 0201-1 SNSRES_DEV — P1V8VDDH_RISNS_IN_P

RE021 604K 0.1% 1/20W TK 0201-1 SNSRES_DEV — NO_XNET_CONNECTION=1

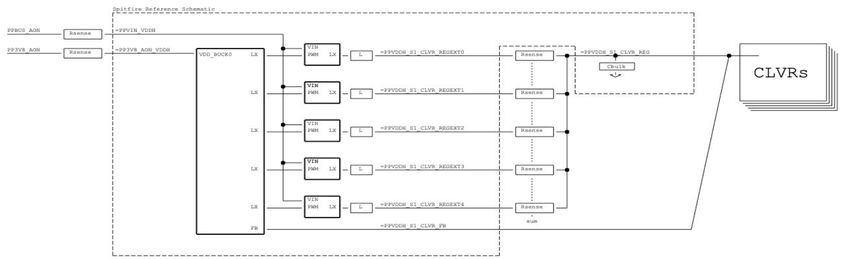
353S1429 UE022 OPA333DCKG4 SC70-5-COMBO SNSRES_DEV
BYPASS=UE022.5::5MM
CE023 0.1UF 10% 6.3V CERM-X5R 0201 SNSRES_DEV

<-- Rp_ACTUAL = 6.287K
<-- Rp_GOAL = 6.289K

RE026 604K 0.1% 1/20W TK 0201-1 NO_XNET_CONNECTION=1 SNSRES_DEV

P1V8VDDH_ISENSE_EXT — RE048 9.09K 0.1% 1/20W TK 0201-1 SNSRES_DEV — P1V8VDDH_ISENSE_EXT_R
PLACE_NEAR=U7700.L14:15MM
RE051 0 0% 1/20W TK 0201 SNSRES_DEV — P1V8VDDH_ISENSE 74
CE029 0.22UF 10% 6.3V X5R-CERM 0201 SNSRES_DEV

72 P1V8VDDH_RISNS1_N — NO_XNET_CONNECTION=1 — RE024 30.1K 0.1% 1/20W TK 0201-1 SNSRES_DEV — P1V8VDDH_RISNS_IN_N_R
RE025 267 0.1% 1/20W TK 0201-1 SNSRES_DEV — P1V8VDDH_RISNS_IN_N
72 P1V8VDDH_RISNS2_N — NO_XNET_CONNECTION=1 — RE030 30.1K 0.1% 1/20W TK 0201-1 SNSRES_DEV
72 P1V8VDDH_RISNS3_N — NO_XNET_CONNECTION=1 — RE031 30.1K 0.1% 1/20W TK 0201-1 SNSRES_DEV
72 P1V8VDDH_RISNS4_N — NO_XNET_CONNECTION=1 — RE042 30.1K 0.1% 1/20W TK 0201-1 SNSRES_DEV
72 P1V8VDDH_RISNS5_N — NO_XNET_CONNECTION=1 — RE043 30.1K 0.1% 1/20W TK 0201-1 SNSRES_DEV



LPMU AMUX_B4, 2ms

37 P3V8AON_ISENSE_EXT — RE053 9.09K 0.1% 1/20W TK 0201-1 — P3V8AON_ISENSE_EXT_R
PLACE_NEAR=U8100.N14:15MM
RE056 0 0% 1/20W TK 0201 — P3V8AON_ISENSE
CE030 0.22UF 10% 6.3V X5R-CERM 0201

[[P3V8 LOW SIDE ISENSE AND ILIMIT moved to CSA140]]

BOM_COST_GROUP=SENSORS

PAGE TITLE: SENSORS: LOW-SIDE (3/3)

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DRAWING NUMBER: 051-08286 | SIZE: D
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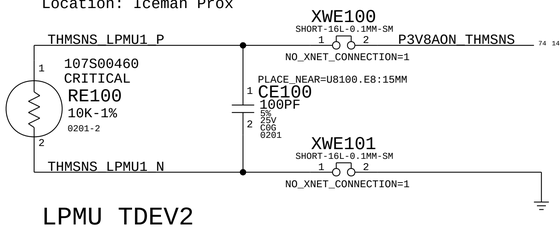
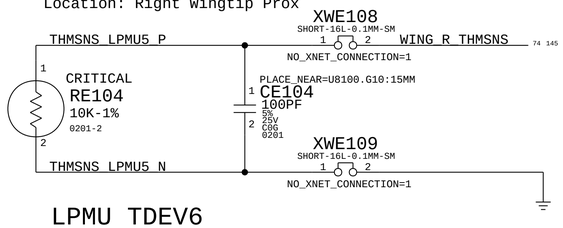
LPMU TDEV1

Sensor Key: TMVR
Location: Iceman Prox



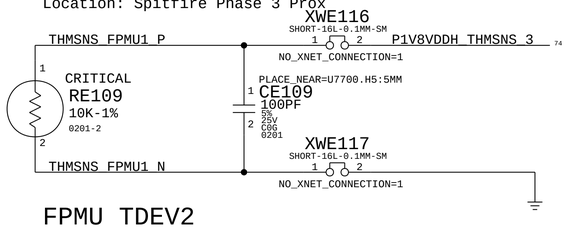
LPMU TDEV5

Sensor Key: TaRT
Location: Right Wingtip Prox



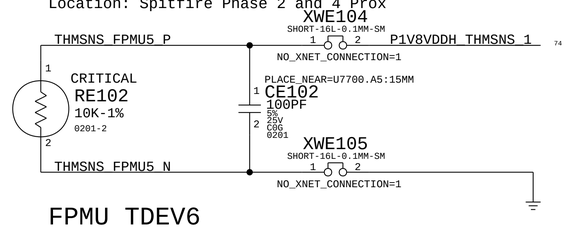
FPMU TDEV1

Sensor Key: TSXR
Location: Spitfire Phase 3 Prox



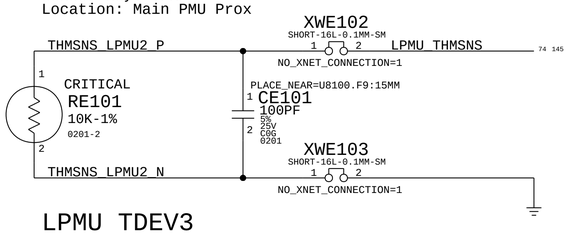
FPMU TDEV5

Sensor Key: TSVR
Location: Spitfire Phase 2 and 4 Prox



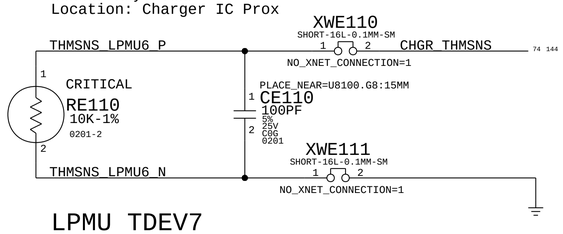
LPMU TDEV2

Sensor Key: TPMP
Location: Main PMU Prox



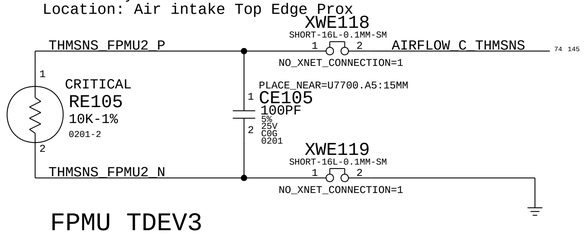
LPMU TDEV6

Sensor Key: TCHP
Location: Charger IC Prox



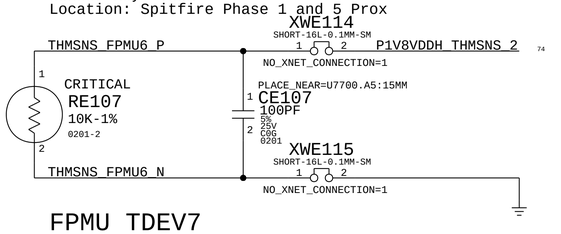
FPMU TDEV2

Sensor Key: TaTP
Location: Air intake Top Edge Prox



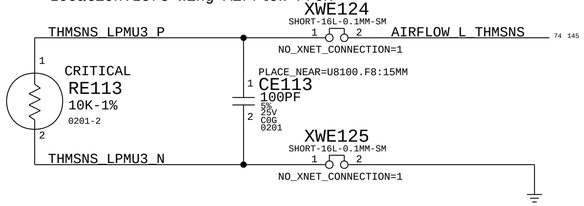
FPMU TDEV6

Sensor Key: TSWR
Location: Spitfire Phase 1 and 5 Prox



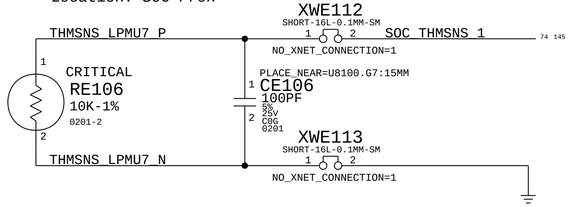
LPMU TDEV3

Sensor Key: TaLW
Location:Left Wing Airflow Prox



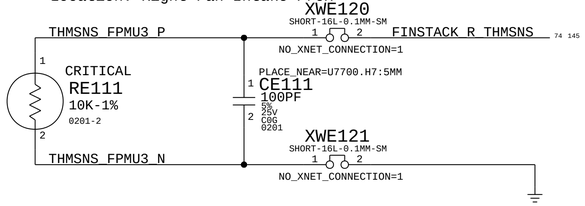
LPMU TDEV7

Sensor Key: TS0P
Location: SoC Prox



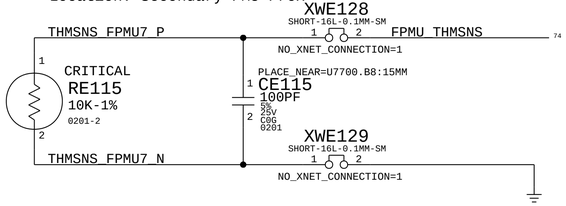
FPMU TDEV3

Sensor Key: TaRF
Location: Right Fan Intake Prox



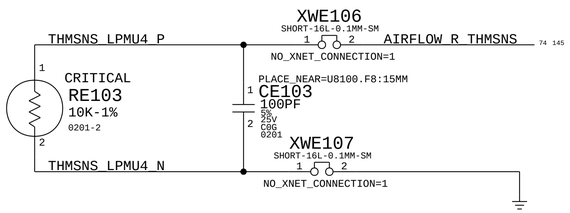
FPMU TDEV7

Sensor Key: TPSP
Location: Secondary PMU Prox



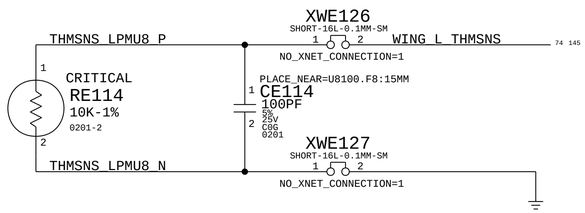
LPMU TDEV4

Sensor Key: TaRW
Location: Right Wing Airflow Prox



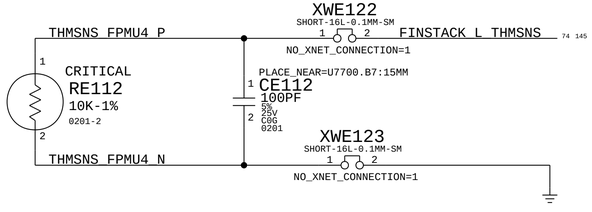
LPMU TDEV8

Sensor Key: TaLT
Location: Left Wingtip Prox



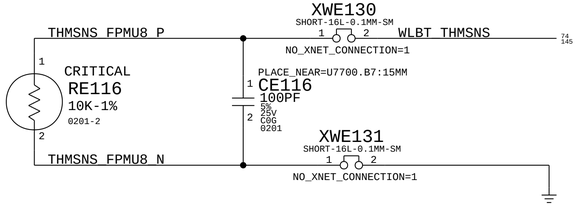
FPMU TDEV4

Sensor Key: TaLP
Location: Air Intake Top Left Edge Prox



FPMU TDEV8

Sensor Key: TW0P
Location: Wireless Prox



PAGE TITLE
SENSORS:THERMAL

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46	DCIN_ISENSE	MAKE_BASE=TRUE	DCIN_ISENSE	67	
46	DCIN_VSENSE	MAKE_BASE=TRUE	DCIN_VSENSE	67	145
46	BMON_ISENSE	MAKE_BASE=TRUE	BMON_ISENSE	67	145 I:MPMU_AMUX_A2
46	PBUS_VSENSE	MAKE_BASE=TRUE	PBUS_VSENSE	67	145 V:MPMU_AMUX_A3
46	P5VUSB23_HS_ISENSE	MAKE_BASE=TRUE	P5VUSB23_HS_ISENSE	69	
46	P5VS2_HS_ISENSE	MAKE_BASE=TRUE	P5VS2_HS_ISENSE	67	
46	SPKRAMP_ABC_ISENSE	MAKE_BASE=TRUE	SPKRAMP_ABC_ISENSE	68	
46	TOUCHID_3V8_HS_ISENSE	MAKE_BASE=TRUE	TOUCHID_3V8_HS_ISENSE	69	
46	IPD_3V8_ISENSE	MAKE_BASE=TRUE	IPD_3V8_ISENSE	71	
46	LPMU_3V8_ISENSE	MAKE_BASE=TRUE	LPMU_3V8_ISENSE	68	145
46	VCCNAND0_HS_ISENSE	MAKE_BASE=TRUE	VCCNAND0_HS_ISENSE	68	
46	VCCNAND1_HS_ISENSE	MAKE_BASE=TRUE	VCCNAND1_HS_ISENSE	68	
46	P3V8AON_ISENSE	MAKE_BASE=TRUE	P3V8AON_ISENSE	72	
46	USB23_3V8_ISENSE	MAKE_BASE=TRUE	USB23_3V8_ISENSE	70	
46	SSD0_3V8_ISENSE	MAKE_BASE=TRUE	SSD0_3V8_ISENSE	70	
46	SSD1_3V8_ISENSE	MAKE_BASE=TRUE	SSD1_3V8_ISENSE	70	
42	P1V8VDDH_HS_ISENSE	MAKE_BASE=TRUE	P1V8VDDH_HS_ISENSE	67	145
42	P1V8VDDH_VSENSE	MAKE_BASE=TRUE	P1V8VDDH_VSENSE	67	
42	P3V8AON_HS_ISENSE	MAKE_BASE=TRUE	P3V8AON_HS_ISENSE	67	
42	WLBT_3V8_ISENSE	MAKE_BASE=TRUE	WLBT_3V8_ISENSE	71	
42	SPKRAMP_DEF_ISENSE	MAKE_BASE=TRUE	SPKRAMP_DEF_ISENSE	68	
42	FPMU_3V8_ISENSE	MAKE_BASE=TRUE	FPMU_3V8_ISENSE	68	145
42	FAN1_PBUS_ISENSE	MAKE_BASE=TRUE	FAN1_PBUS_ISENSE	71	
42	P1V8VDDH_ISENSE	MAKE_BASE=TRUE	P1V8VDDH_ISENSE	72	
42	USB01_3V8_ISENSE	MAKE_BASE=TRUE	USB01_3V8_ISENSE	70	
42	NC_FPMU_AMUX_B1_TBD	MAKE_BASE=TRUE	NC_FPMU_AMUX_B1_TBD		
42	P5VUSB01_HS_ISENSE	MAKE_BASE=TRUE	P5VUSB01_HS_ISENSE	69	
42	TCON_3V8_ISENSE	MAKE_BASE=TRUE	TCON_3V8_ISENSE	70	
42	BKLT_HS_ISENSE	MAKE_BASE=TRUE	BKLT_HS_ISENSE	69	
42	SD_HS_ISENSE	MAKE_BASE=TRUE	SD_HS_ISENSE	69	
42	ALSCAM_5V_ISENSE	MAKE_BASE=TRUE	ALSCAM_5V_ISENSE	71	
42	BKLTCONN_3V8_ISENSE	MAKE_BASE=TRUE	BKLTCONN_3V8_ISENSE	71	
46	P3V8AON_THMSNS	MAKE_BASE=TRUE	P3V8AON_THMSNS	73	145
46	LPMU_THMSNS	MAKE_BASE=TRUE	LPMU_THMSNS	73	145
46	AIRFLOW_L_THMSNS	MAKE_BASE=TRUE	AIRFLOW_L_THMSNS	73	145
46	AIRFLOW_R_THMSNS	MAKE_BASE=TRUE	AIRFLOW_R_THMSNS	73	145
46	WING_R_THMSNS	MAKE_BASE=TRUE	WING_R_THMSNS	73	145
46	CHGR_THMSNS	MAKE_BASE=TRUE	CHGR_THMSNS	73	144
46	SOC_THMSNS_1	MAKE_BASE=TRUE	SOC_THMSNS_1	73	145
46	WING_L_THMSNS	MAKE_BASE=TRUE	WING_L_THMSNS	73	145
42	P1V8VDDH_THMSNS_3	MAKE_BASE=TRUE	P1V8VDDH_THMSNS_3	73	
42	AIRFLOW_C_THMSNS	MAKE_BASE=TRUE	AIRFLOW_C_THMSNS	73	145
42	FINSTACK_R_THMSNS	MAKE_BASE=TRUE	FINSTACK_R_THMSNS	73	145
42	FINSTACK_L_THMSNS	MAKE_BASE=TRUE	FINSTACK_L_THMSNS	73	145
42	P1V8VDDH_THMSNS_1	MAKE_BASE=TRUE	P1V8VDDH_THMSNS_1	73	
42	P1V8VDDH_THMSNS_2	MAKE_BASE=TRUE	P1V8VDDH_THMSNS_2	73	
42	FPMU_THMSNS	MAKE_BASE=TRUE	FPMU_THMSNS	73	145
42	WLBT_THMSNS	MAKE_BASE=TRUE	WLBT_THMSNS	73	145

BOM_COST_GROUP=SENSORS

PAGE TITLE

SENSORS: ALIASES

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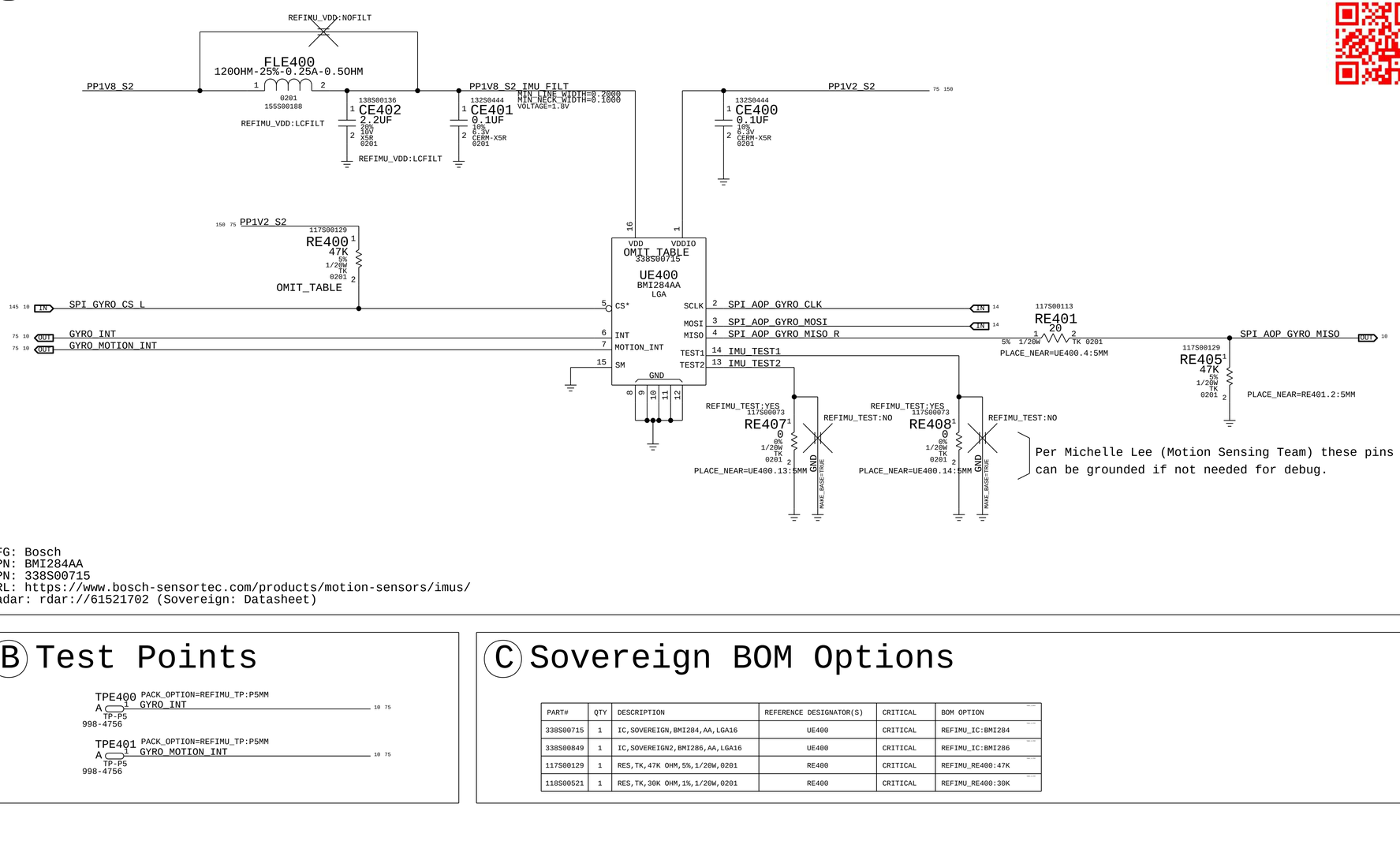
*** OK2INTEGRATE ***

A Sovereign Accelerometer and Gyroscope

Datasheet Radar:



MFG: Bosch
MPN: BMI284AA
APN: 338S00715
URL: https://www.bosch-sensortec.com/products/motion-sensors/imus/
Radar: rdar://61521702 (Sovereign: Datasheet)

B Test Points

C Sovereign BOM Options

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S00715	1	IC,SOVEREIGN,BMI284,AA,LGA16	UE400	CRITICAL	REFIMU_IC:BMI284
338S00849	1	IC,SOVEREIGN2,BMI286,AA,LGA16	UE400	CRITICAL	REFIMU_IC:BMI286
117S00129	1	RES,TK,47K OHM,5%,1/20W,0201	RE400	CRITICAL	REFIMU_RE400:47K
118S00521	1	RES,TK,30K OHM,1%,1/20W,0201	RE400	CRITICAL	REFIMU_RE400:30K

BOM_COST_GROUP=SENSORS

PAGE TITLE
SENSORS: MOTION

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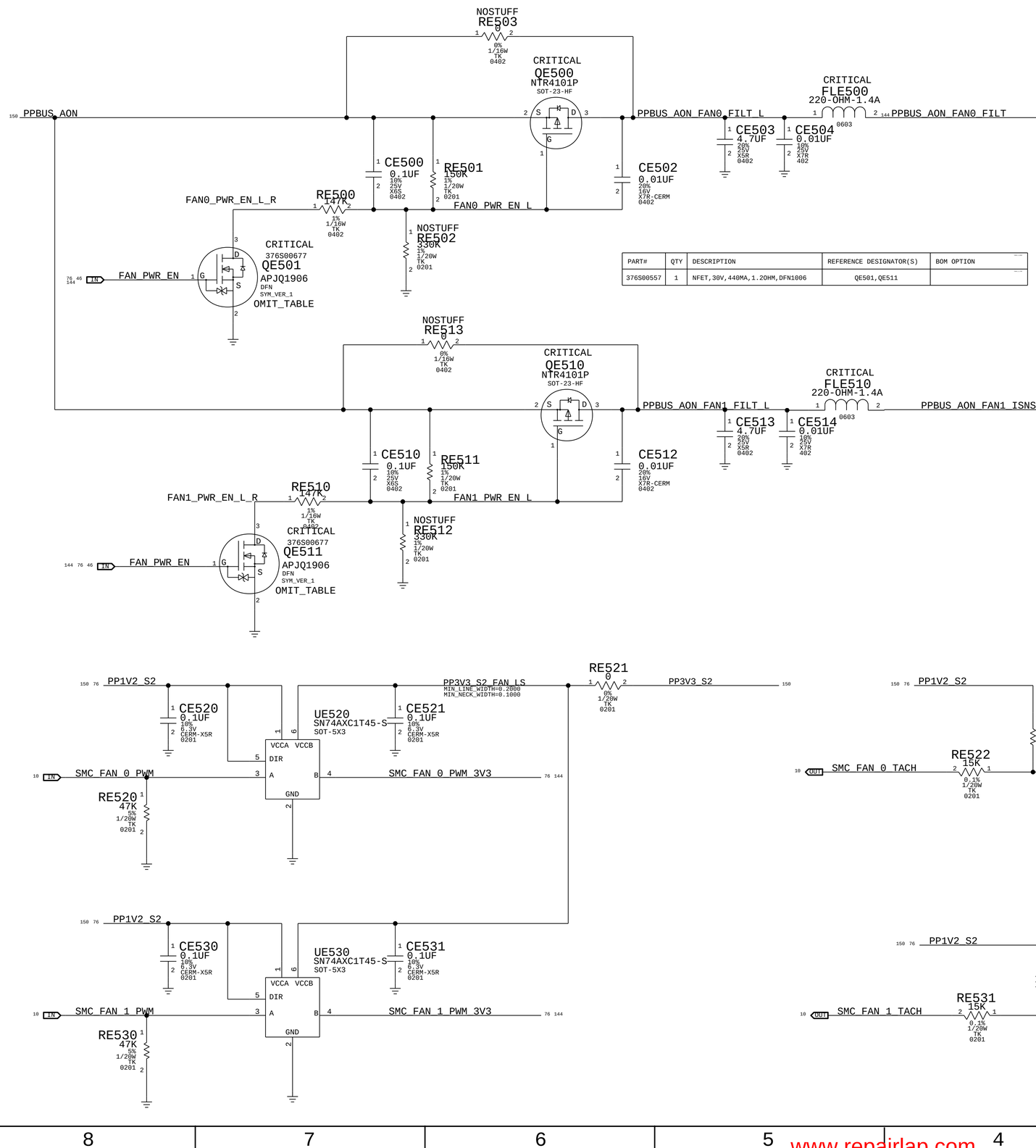

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Left Side Port

PLACE VBUS CAP NEAR EACH VBUS PIN

PPVBUS_USBC0
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
VOLTAGE=20V

PLACE_NEAR=JE700.30:5MM
ALLOW_APPLE_PREFIX=D

DE722
TVS3300
WSON-1

516S00686
PACK_IGNORE=TRUE
JE700
20875-028E-01
F-ST-SMM
PACK_OPTION=NOT_FLIPPED

USBC0_D2R_CR_N<1>
USBC0_D2R_CR_P<1>
USBC0_R2D_N<1>
USBC0_R2D_P<1>
USBC0_USB_TOP_P
USBC0_USB_TOP_N
USBC0_D2R_CR_N<2>
USBC0_D2R_CR_P<2>
USBC0_SBU2
USBC0_CC1
USBC0_USB_BOT_N
USBC0_USB_BOT_P
USBC0_SBU1
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USBC0_R2D_P<2>
USBC0_LDCM_LB

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USBC0_D2R_N<1>
USBC0_D2R_P<1>
USBC0_SBU2
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USBC0_USB_BOT_P

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USBC0_D2R_CR_P<1>

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USBC0_SBU1
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USBC0_USB_BOT_P

USBC0_R2D_C_N<2>
USBC0_R2D_C_P<2>
USBC0_D2R_R_N<2>
USBC0_D2R_R_P<2>

USBC0_R2D_CR_N<2>
USBC0_R2D_CR_P<2>
USBC0_USB_TOP_P
USBC0_USB_TOP_N
USBC0_SBU1

516S00686
PACK_IGNORE=TRUE
JE701
20875-028E-01
F-ST-SMM
PACK_OPTION=NOT_FLIPPED

USBC1_D2R_CR_N<1>
USBC1_D2R_CR_P<1>
USBC1_R2D_N<1>
USBC1_R2D_P<1>
USBC1_USB_TOP_P
USBC1_USB_TOP_N
USBC1_D2R_CR_N<2>
USBC1_D2R_CR_P<2>
USBC1_SBU2
USBC1_CC1
USBC1_USB_BOT_N
USBC1_USB_BOT_P
USBC1_SBU1
USBC1_CC2
USBC1_LDCM
USBC1_R2D_N<2>
USBC1_R2D_P<2>
USBC1_LDCM_LB

USBC1_SBU2
USBC1_CC1
USBC1_USB_BOT_N
USBC1_USB_BOT_P

USBC1_R2D_C_P<1>
USBC1_R2D_C_N<1>
USBC1_D2R_R_P<1>
USBC1_D2R_R_N<1>

USBC1_R2D_P<1>
USBC1_R2D_N<1>
USBC1_D2R_CR_P<1>
USBC1_D2R_CR_N<1>

USBC1_CC2
USBC1_R2D_CR_P<2>
USBC1_R2D_CR_N<2>
USBC1_D2R_P<2>
USBC1_D2R_N<2>
USBC1_SBU1
USBC1_USB_BOT_N
USBC1_USB_BOT_P

USBC1_R2D_C_N<2>
USBC1_R2D_C_P<2>
USBC1_D2R_R_N<2>
USBC1_D2R_R_P<2>

USBC1_R2D_CR_N<2>
USBC1_R2D_CR_P<2>
USBC1_USB_TOP_P
USBC1_USB_TOP_N
USBC1_SBU1

PPVBUS_USBC1
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
VOLTAGE=20V

PLACE_NEAR=JE701.30:5MM
ALLOW_APPLE_PREFIX=D

DE702
TVS3300
WSON-1

BOM_COST_GROUP=USB-C

PAGE TITLE	USB-C: Left Connectors
	Apple Inc.
DRAWING NUMBER	051-08286
SIZE	D
REVISION	5.0.3
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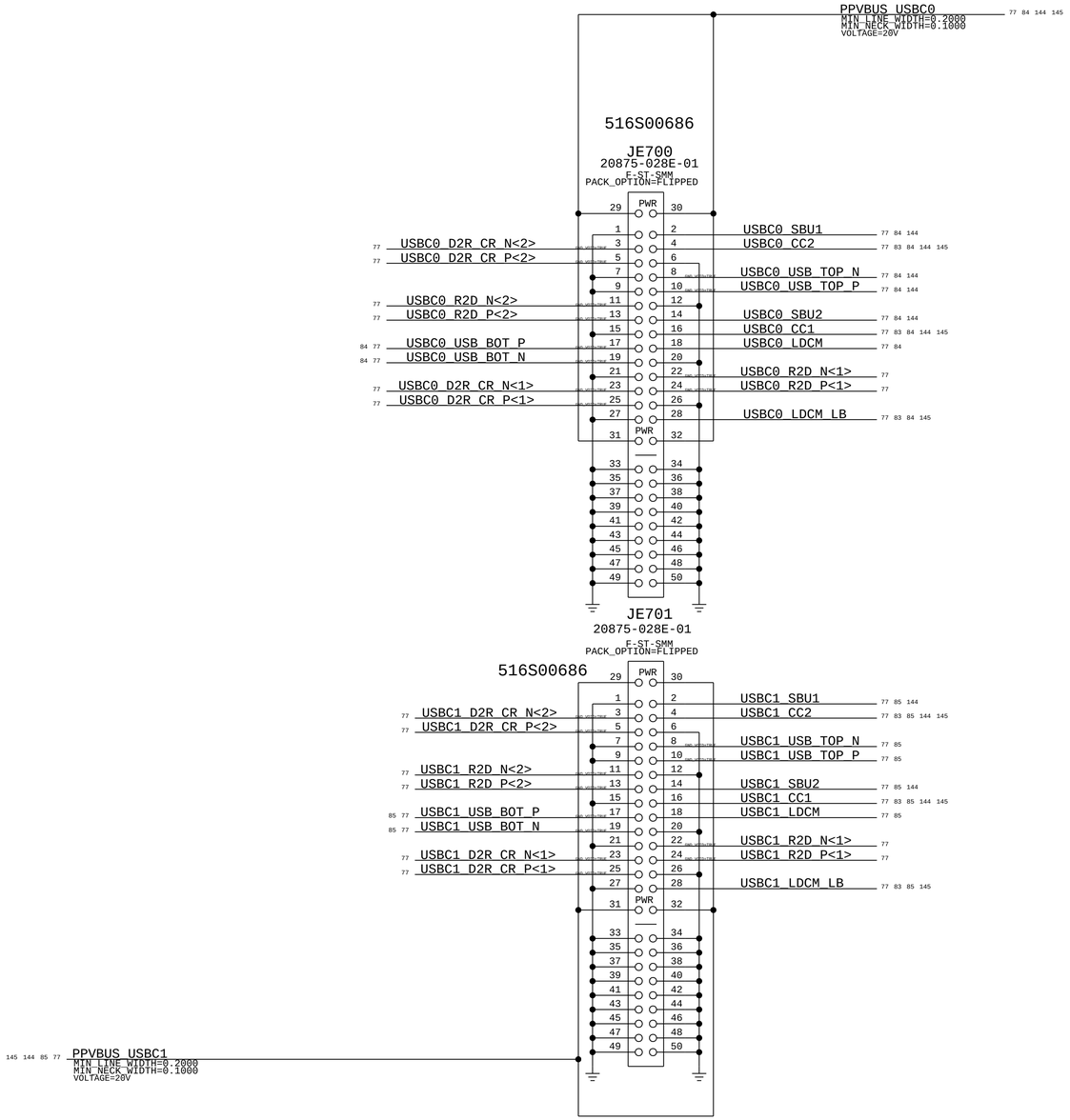
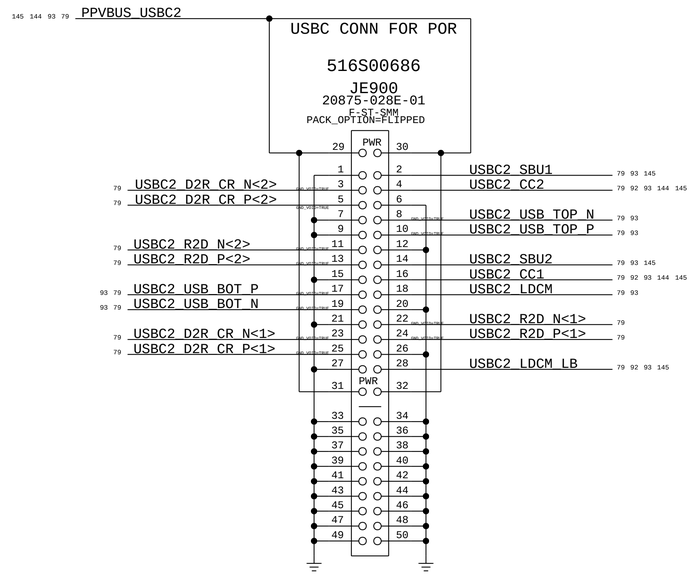
Flipped Top/Bottom Connections

To use reversed top/bottom connections,
Specify PACK_OPTION=FLIPPED and include CSA148





BOM_COST_GROUP=USB-C

PAGE TITLE
USB-C: Alt Flipped Connector(s)

Apple Inc.

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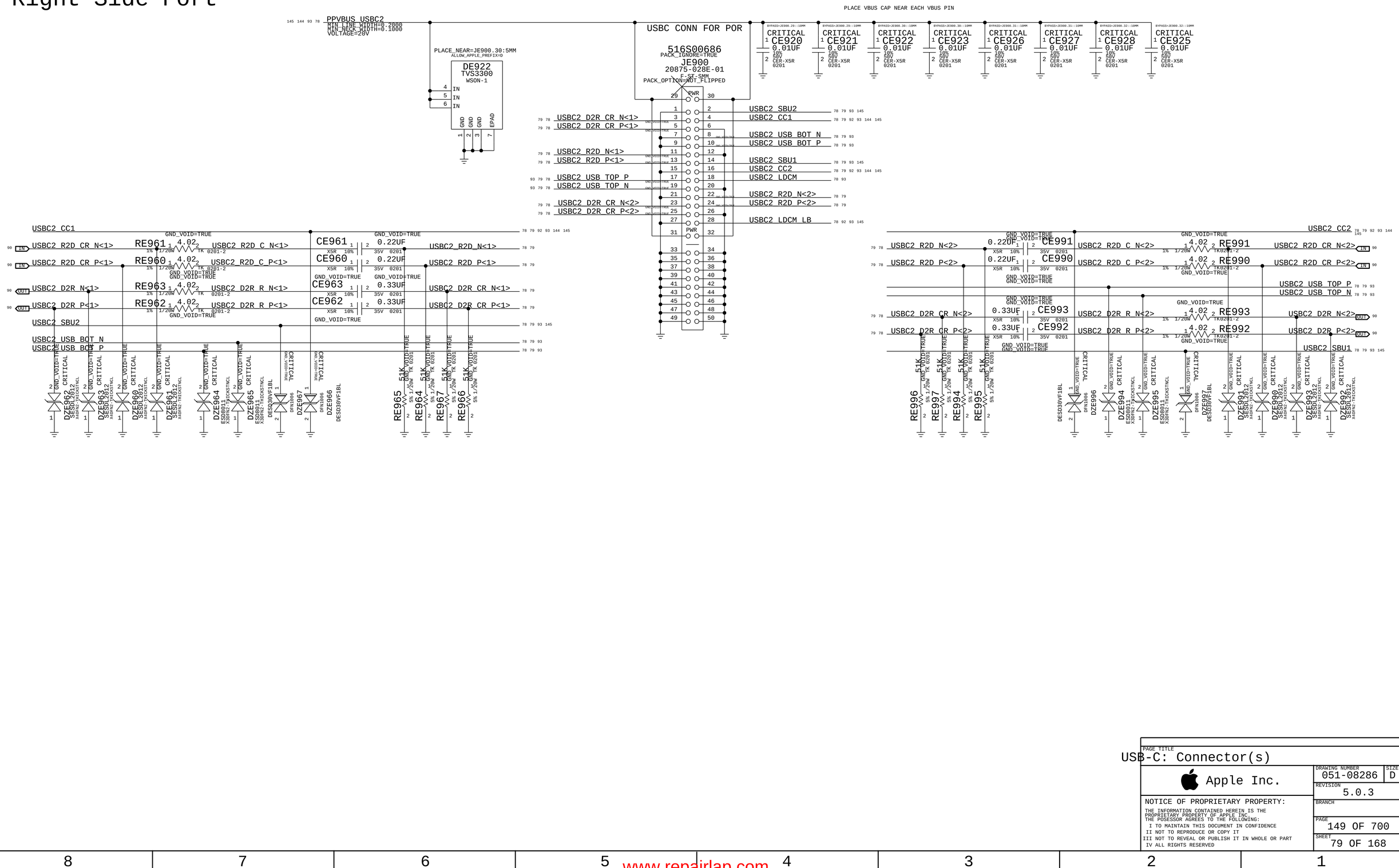
Right Side Port



PAGE TITLE

USB-C: Connector(s)

Apple Inc.

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*** OK2INTEGRATE ***

No lane swapping is allowed
Re-timer to SOC connections are set

Re-timer to connector connections are set

PP1V2_S2

RF062 1.5K 0201 TK 5% 1/20W — I2C_UPC0_ATCRTMR0_SCL
RF063 1.5K 0201 TK 5% 1/20W — I2C_UPC0_ATCRTMR0_SDA

RF043 47K 1/20W 5% TK 0201 — CIO_ATC0_LSTX
RF044 47K 1/20W 5% TK 0201 — CIO_ATC0_LSRX

CF011 10PF 5% 25V C0G 0201 — RF011 200 1% 1/20W TK 0201 — ATCRTMR0_CFP_RCAL_NEG / ATCRTMR0_CFP_RCAL_POS
CF010 10PF 5% 25V C0G 0201 — RF010 200 1% 1/20W TK 0201-1 — ATCRTMR0_SFP_RCAL_NEG / ATCRTMR0_SFP_RCAL_POS

USBC HIGH-SPEED AC COUPLING

USBC_ATC0_R2D_C_P<1>	CF020 0.22UF 20% 6.3V X5R 0201	USBC_ATC0_R2D_P<1>
USBC_ATC0_R2D_C_N<1>	CF021 0.22UF 20% 6.3V X5R 0201	USBC_ATC0_R2D_N<1>
USBC_ATC0_R2D_C_P<2>	CF024 0.22UF 20% 6.3V X5R 0201	USBC_ATC0_R2D_P<2>
USBC_ATC0_R2D_C_N<2>	CF025 0.22UF 20% 6.3V X5R 0201	USBC_ATC0_R2D_N<2>
USBC_ATC0_D2R_P<1>	CF022 0.22UF 20% 6.3V X5R 0201	USBC_ATC0_D2R_C_P<1>
USBC_ATC0_D2R_N<1>	CF023 0.22UF 20% 6.3V X5R 0201	USBC_ATC0_D2R_C_N<1>
USBC_ATC0_D2R_P<2>	CF026 0.22UF 20% 6.3V X5R 0201	USBC_ATC0_D2R_C_P<2>
USBC_ATC0_D2R_N<2>	CF027 0.22UF 20% 6.3V X5R 0201	USBC_ATC0_D2R_C_N<2>

GND_VOID=TRUE

ATCRTMR0_XTAL24M_OUT — RF060 499 1% 1/20W TK 0201 — ATCRTMR0_XTAL24M_IN
197S0591 CRITICAL YF000 1.60X1.20MM 24.000MHZ-20PPM-9.5PF-60OHM
ATC0_24M_O_R
CRITICAL CF060 15PF 5% 50V C0G 0201
CRITICAL 131S0831 CF061 15PF 5% 50V C0G 0201

PP0V855_ATCRTMR01_VDD_CIO
CF030 14UF 20% 4V X5R 0402-D2X-1 (138S00149)
CF031 14UF 20% 4V X5R 0402-D2X-1
CF032 0.1UF 10% 6.3V X6S 0201
CF033 0.1UF 10% 6.3V X6S 0201

UF000 TMNB25B1-K1S1 FCCSP 338S00888 SYM 2 OF 2

J4, J6, J8	VDD_CIO_0	OMIT_TABLE CRITICAL
F4, F6, F8	VDD_CIO_1	
G4, G5, H5, H6	VDD_FIXED	
G7	VDD_FIXED_PLL	
G9	VDD_FIXED_XTAL	
K5, K7, L6	VDDIO12_CIO_0	
D6, E5, E7	VDDIO12_CIO_1	
K8	VDDIO12_PLL_SOC0	
H8	VDDIO12_PLL_SOC1	
H9	VDDIO12_XTAL	
E9, H3, K9	VDDIO12	
F3	VDDIO12_EFUSE1	
F7	VDDIO12_AMUX	
A1, A2, A4, A6, A8, A10, A11, B2, B4, B6, B8, B10, C3, C5, C6, C7, C9, D1, D5, D7, D11, E3, E4, E6, E8, F2, F5, F10, G3, G6, G8	VSS	
H4, H7, J2, J3, J5, J7, J10, K4, K6, L1, L5, L7, L11, M3, M5, M6, M7, M9, N2, N4, N6, N8, N10, P1, P2, P4, P6, P8, P10, P11	VSS	

PP1V2_ATCRTMR01_VDDIO
132S0395 CF034 0.1UF 10% 6.3V X6S 0201
138S00039 CF035 2.2UF 20% 4V X6S-CERM 0201
CF036 14UF 20% 4V X5R 0402-D2X-1
CF037 14UF 20% 4V X5R 0402-D2X-1

PP0V805_ATCRTMR01_VDD_FIXED
CF040 0.1UF 10% 6.3V X6S 0201
CF041 0.1UF 10% 6.3V X6S 0201
CF042 2.2UF 20% 4V X6S-CERM 0201
CF043 2.2UF 20% 4V X6S-CERM 0201
CF044 2.2UF 20% 4V X6S-CERM 0201
CF045 14UF 20% 4V X5R 0402-D2X-1
CF046 14UF 20% 4V X5R 0402-D2X-1

PP1V2_ATCRTMR01_VDDIO_XTAL_F (VOLTAGE=1.2V)
CF062 0.1UF 10% 6.3V X6S 0201 (132S0395)
155S0644 FLF000 240-OHM-0.2A-0.9-OHM 0201
CF063 2.2UF 20% 4V X6S-CERM 0201 (138S00039)

PP1V2_ATCRTMR01_VDDIO
138S00039 CF052 2.2UF 20% 4V X6S-CERM 0201 (PLACE_NEAR=UF000.K8:5MM)

Connect to GND directly or via a resistor
GND

PP0V805_ATCRTMR01_VDD_FIXED
CF050 0.1UF 10% 6.3V X6S 0201 (PLACE_NEAR=UF000.G7:5MM)

PPVDD_FIXED_ATCRTMR0_XTAL_R
PP0V805_ATCRTMR01_VDD_FIXED
RF051 10 5% 1/20W TK 0201 (VOLTAGE=0.805V)
CF051 4UF 20% 2.5V X6S 0201 (117S00094, 138S00329)

PP1V2_ATCRTMR01_VDDIO
132S0395 CF064 0.1UF 10% 6.3V X6S 0201

PACK_OPTION=ATC_BOUNDARYSCAN:YES
RF045 47K 5% 1/20W TK 0201 — ATCRTMR0_JTAG_TDO
PACK_OPTION=ATC_BOUNDARYSCAN:NO
RF047 47K 5% 1/20W TK 0201 — ATCRTMR0_JTAG_SEL
PACK_OPTION=ATC_BOUNDARYSCAN:YES
RF040 10K 5% 1/20W 0201 — ATCRTMR0_TESTMODE
PACK_OPTION=ATC_BOUNDARYSCAN:NO

UF000 TMNB25B1-K1S1 FCCSP 338S00888 SYM 1 OF 2
OMIT_TABLE CRITICAL

USBC_ATC0_D2R_C_P<1>	P9	SFP_PHY_RXTX_0_P	SFP PHY
USBC_ATC0_D2R_C_N<1>	N9	SFP_PHY_RXTX_0_N	
USBC_ATC0_D2R_C_P<2>	P5	SFP_PHY_RXTX_2_P	
USBC_ATC0_D2R_C_N<2>	N5	SFP_PHY_RXTX_2_N	
USBC_ATC0_R2D_P<1>	P7	SFP_PHY_RXTX_1_P	
USBC_ATC0_R2D_N<1>	N7	SFP_PHY_RXTX_1_N	
USBC_ATC0_R2D_P<2>	P3	SFP_PHY_RXTX_3_P	
USBC_ATC0_R2D_N<2>	N3	SFP_PHY_RXTX_3_N	
USBC_ATC0_AUX_C_P	L4	SFP_LPDP_AUX_P	
USBC_ATC0_AUX_C_N	M4	SFP_LPDP_AUX_N	
CIO_ATC0_LSTX	G1	USB4_SFP_SB_RX	
CIO_ATC0_LSRX	G2	USB4_SFP_SB_TX	
ATCRTMR0_SFP_RCAL_POS	M8	SFP_PHY_RCAL_P	
ATCRTMR0_SFP_RCAL_NEG	L8	SFP_PHY_RCAL_N	
GND	M1	CHIP_ID_0	GPIO
GND	N1	CHIP_ID_1	
ATCRTMR0_BOOT_CONFIG0	H2	BOOT_CONFIG0	
ATCRTMR0_BOOT_CONFIG1	J1	BOOT_CONFIG1	
ATCRTMR0_BOOT_CONFIG2	K1	BOOT_CONFIG2	
ATCRTMR0_FORCE_DFU	C1	FORCE_DFU	
TP_ATCRTMR0_GPIO0	K2	GPIO0	
NC_ATCRTMR0_GPIO1 (NO_TEST=1)	L3	GPIO1	
TP_ATCRTMR0_GPIO2	K3	GPIO2	
TP_ATCRTMR0_GPIO3	L10	GPIO3	
ATCRTMR0_RESET_L	L2	COLD_RESET*	CLOCKS AND RESET
	M2	CFSB	
ATCRTMR0_XTAL24M_IN	F11	XI0	
ATCRTMR0_XTAL24M_OUT	E11	XO0	

CFP_PHY_RXTX_0_P	A9	USBC0_R2D_CR_P<1>	CFP PHY
CFP_PHY_RXTX_0_N	B9	USBC0_R2D_CR_N<1>	
CFP_PHY_RXTX_2_P	A5	USBC0_R2D_CR_P<2>	
CFP_PHY_RXTX_2_N	B5	USBC0_R2D_CR_N<2>	
CFP_PHY_RXTX_1_P	A7	USBC0_D2R_P<1>	
CFP_PHY_RXTX_1_N	B7	USBC0_D2R_N<1>	
CFP_PHY_RXTX_3_P	A3	USBC0_D2R_P<2>	
CFP_PHY_RXTX_3_N	B3	USBC0_D2R_N<2>	
CFP_LPDP_AUX_P	D4	USBC0_AUX_P	
CFP_LPDP_AUX_N	C4	USBC0_AUX_N	
USB4_CFP_SB_RX	F1	USBC0_CIO_LSRX	
USB4_CFP_SB_TX	E1	USBC0_CIO_LSTX	
USB4_CFP_SB_TX_DIR	H1	ATCRTMR0_LSTX_DIR	
CFP_PHY_RCAL_P	C8	ATCRTMR0_CFP_RCAL_POS	
CFP_PHY_RCAL_N	D8	ATCRTMR0_CFP_RCAL_NEG	
QSPI_CS*	N11	SPI_ATCRTMR0_CS_L	PERIPHERAL
QSPI_SCLK	M11	SPI_ATCRTMR0_CLK	
QSPI_DQ0	K10	SPI_ATCRTMR0_DIO<0>	
QSPI_DQ1	K11	SPI_ATCRTMR0_DIO<1>	
QSPI_DQ2	J9	SPI_ATCRTMR0_DIO<2>	
QSPI_DQ3	J11	SPI_ATCRTMR0_DIO<3>	
I2C0_SCL	C2	I2C_ATCRTMR_SCL	
I2C0_SDA	D3	I2C_ATCRTMR_SDA	
I2C1_SCL	E2	I2C_UPC0_ATCRTMR0_SCL	
I2C1_SDA	D2	I2C_UPC0_ATCRTMR0_SDA	
I2C1_INT	B1	UPC0_ATCRTMR0_I2C_INT_L	
TESTMODE	L9	ATCRTMR0_TESTMODE	TEST AND DEBUG
JTAG_SEL	C11	ATCRTMR0_JTAG_SEL	
JTAG_TCK	B11	SWD_NUB_ATCRTMR01_SWCLK	
JTAG_TMS	D10	SWD_NUB_ATCRTMR01_SWDIO	
JTAG_TDI	D9	TP_ATCRTMR0_JTAG_TDI	
JTAG_TDO	C10	ATCRTMR0_JTAG_TDO	
JTAG_TRST*	E10	TP_ATCRTMR0_JTAG_TRESET	
ANALOGMUX_OUT	F9	TP_ATCRTMR0_ANALOGMUX_OUT	
TST_CLKOUT	M10	TP_ATCRTMR0_TST_CLKOUT	
TST_CLK_LVDS_0_P	H10	NC_ATCRTMR0_CLK_LVDSP<0> (NO_TEST=1)	
TST_CLK_LVDS_0_N	H11	NC_ATCRTMR0_CLK_LVDSN<0> (NO_TEST=1)	
TST_CLK_LVDS_1_P	G11	NC_ATCRTMR0_CLK_LVDSP<1> (NO_TEST=1)	
TST_CLK_LVDS_1_N	G10	NC_ATCRTMR0_CLK_LVDSN<1> (NO_TEST=1)	

RF097 33 1/20W 5% TK 0201 — SPI_ATCRTMR0_DIO<0> / SPI_ATCRTMR0_R_DIO<0>
RF098 33 1/20W 5% TK 0201 — SPI_ATCRTMR0_DIO<1> / SPI_ATCRTMR0_R_DIO<1>

PP1V2_ATCRTMR01_VDDIO
RF090 3.3K 5% 1/20W TK 0201
NOSTUFF RF091 3.3K 5% 1/20W TK 0201
NOSTUFF RF092 3.3K 5% 1/20W TK 0201
NOSTUFF RF093 3.3K 5% 1/20W TK 0201
CF090 1.0UF 20% 6.3V X5R 0201-1

OMIT_TABLE CRITICAL 335S00574
UF090 64MBIT-1.2V W25Q64NE XSON-1

SPI_ATCRTMR0_CLK	RF094 33 0201	SPI_ATCRTMR0_CLK_R
SPI_ATCRTMR0_CS_L		SPI_ATCRTMR0_CS_L
SPI_ATCRTMR0_DIO<2>	RF095 33 0201	SPI_ATCRTMR0_R_DIO<2>
SPI_ATCRTMR0_DIO<3>	RF096 33 0201	SPI_ATCRTMR0_R_DIO<3>

CLK, CS*, WP*(IO2), HOLD*(IO3), DI(IO0), DO(IO1), GND, EPAD
SPI_ATCRTMR0_R_DIO<0>, SPI_ATCRTMR0_R_DIO<1>
PACK_OPTION=ATC_RTMR_ROM:XSON

PP1V2_ATCRTMR01_VDDIO
UF090 64MBIT-1.2V GD25UF64E WLCSP-COMBO
OMIT_TABLE 335S00638

SPI_ATCRTMR0_CLK_R	D2 SCLK	
SPI_ATCRTMR0_CS_L	B3 CS*	
SPI_ATCRTMR0_R_DIO<2>	D3 IO2	SI(IO0) E2 SPI_ATCRTMR0_R_DIO<0>
SPI_ATCRTMR0_R_DIO<3>	C2 IO3	SO(IO1) C3 SPI_ATCRTMR0_R_DIO<1>
		A2, A3, F2, F3 NC
		VSS E3

PACK_IGNORE=TRUE
PACK_OPTION=ATC_RTMR_ROM:WLCSP

BOM_COST_GROUP=TBT

PAGE TITLE: USB-C: High Speed ATC0

Apple Inc.

DRAWING NUMBER: 051-08286
SIZE: D
REVISION: 5.0.3
BRANCH:
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*** OK2INTEGRATE ***

No lane swapping is allowed
Re-timer to SOC connections are set

Re-timer to connector connections are set

PP1V2_S2

RF162 1.5K 1/20W 0201 TK 5% — I2C_UPC1_ATCRTMR1_SCL
RF163 1.5K 1/20W 0201 TK 5% — I2C_UPC1_ATCRTMR1_SDA

RF143 47K 1/20W 5% TK 0201 — CIO_ATC1_LSTX
RF144 47K 1/20W 5% TK 0201 — CIO_ATC1_LSRX

CF111 10PF 5% 25V C0G 0201 — RF111 200 1% 1/20W TK 0201 — ATCRTMR1_CFP_RCAL_NEG / ATCRTMR1_CFP_RCAL_POS
CF110 10PF 5% 25V C0G 0201 — RF110 200 1% 1/20W TK 0201-1 — ATCRTMR1_SFP_RCAL_NEG / ATCRTMR1_SFP_RCAL_POS

USBC HIGH-SPEED AC COUPLING

USBC_ATC1_R2D_C_P<1>	CF120 0.22UF 20% 6.3V X5R 0201	USBC_ATC1_R2D_P<1>	GND_VOID=TRUE
USBC_ATC1_R2D_C_N<1>	CF121 0.22UF 20% 6.3V X5R 0201	USBC_ATC1_R2D_N<1>	GND_VOID=TRUE
USBC_ATC1_R2D_C_P<2>	CF124 0.22UF 20% 6.3V X5R 0201	USBC_ATC1_R2D_P<2>	GND_VOID=TRUE
USBC_ATC1_R2D_C_N<2>	CF125 0.22UF 20% 6.3V X5R 0201	USBC_ATC1_R2D_N<2>	GND_VOID=TRUE
USBC_ATC1_D2R_P<1>	CF122 0.22UF 20% 6.3V X5R 0201	USBC_ATC1_D2R_C_P<1>	GND_VOID=TRUE
USBC_ATC1_D2R_N<1>	CF123 0.22UF 20% 6.3V X5R 0201	USBC_ATC1_D2R_C_N<1>	GND_VOID=TRUE
USBC_ATC1_D2R_P<2>	CF126 0.22UF 20% 6.3V X5R 0201	USBC_ATC1_D2R_C_P<2>	GND_VOID=TRUE
USBC_ATC1_D2R_N<2>	CF127 0.22UF 20% 6.3V X5R 0201	USBC_ATC1_D2R_C_N<2>	

UF100
TMNB25B1-K1S1
FCCSP
338S00888
SYM 1 OF 2
OMIT_TABLE
CRITICAL

USBC_ATC1_D2R_C_P<1>	P9	SFP_PHY_RXTX_0_P	CFP_PHY_RXTX_0_P<1>
USBC_ATC1_D2R_C_N<1>	N9	SFP_PHY_RXTX_0_N	CFP_PHY_RXTX_0_N<1>
USBC_ATC1_D2R_C_P<2>	P5	SFP_PHY_RXTX_2_P	CFP_PHY_RXTX_2_P<2>
USBC_ATC1_D2R_C_N<2>	N5	SFP_PHY_RXTX_2_N	CFP_PHY_RXTX_2_N<2>
USBC_ATC1_R2D_P<1>	P7	SFP_PHY_RXTX_1_P	CFP_PHY_RXTX_1_P<1>
USBC_ATC1_R2D_N<1>	N7	SFP_PHY_RXTX_1_N	CFP_PHY_RXTX_1_N<1>
USBC_ATC1_R2D_P<2>	P3	SFP_PHY_RXTX_3_P	CFP_PHY_RXTX_3_P<2>
USBC_ATC1_R2D_N<2>	N3	SFP_PHY_RXTX_3_N	CFP_PHY_RXTX_3_N<2>
USBC_ATC1_AUX_C_P	L4	SFP_LPDP_AUX_P	CFP_LPDP_AUX_P
USBC_ATC1_AUX_C_N	M4	SFP_LPDP_AUX_N	CFP_LPDP_AUX_N
CIO_ATC1_LSTX	G1	USB4_SFP_SB_RX	USB4_CFP_SB_RX
CIO_ATC1_LSRX	G2	USB4_SFP_SB_TX	USB4_CFP_SB_TX
			USB4_CFP_SB_TX_DIR
ATCRTMR1_SFP_RCAL_POS	M8	SFP_PHY_RCAL_P	CFP_PHY_RCAL_P
ATCRTMR1_SFP_RCAL_NEG	L8	SFP_PHY_RCAL_N	CFP_PHY_RCAL_N

SFP PHY / CFP PHY

ATCRTMR1_CHIPID_0	M1	CHIP_ID_0	
GND	N1	CHIP_ID_1	
ATCRTMR1_BOOT_CONFIG0	H2	BOOT_CONFIG0	
ATCRTMR1_BOOT_CONFIG1	J1	BOOT_CONFIG1	
ATCRTMR1_BOOT_CONFIG2	K1	BOOT_CONFIG2	
ATCRTMR1_FORCE_DFU	C1	FORCE_DFU	
TP_ATCRTMR1_GPIO0	K2	GPIO0	
NC_ATCRTMR1_GPIO1 NO_TEST=1	L3	GPIO1	
TP_ATCRTMR1_GPIO2	K3	GPIO2	
TP_ATCRTMR1_GPIO3	L10	GPIO3	

GPIO

		QSPI_CS*	SPI_ATCRTMR1_CS_L
		QSPI_SCLK	SPI_ATCRTMR1_CLK
		QSPI_DQ0	SPI_ATCRTMR1_DIO<0>
		QSPI_DQ1	SPI_ATCRTMR1_DIO<1>
		QSPI_DQ2	SPI_ATCRTMR1_DIO<2>
		QSPI_DQ3	SPI_ATCRTMR1_DIO<3>
		I2C0_SCL	I2C_ATCRTMR_SCL
		I2C0_SDA	I2C_ATCRTMR_SDA
		I2C1_SCL	I2C_UPC1_ATCRTMR1_SCL
		I2C1_SDA	I2C_UPC1_ATCRTMR1_SDA
		I2C1_INT	UPC1_ATCRTMR1_I2C_INT_L

PERIPHERAL

ATCRTMR1_RESET_L	L2	COLD_RESET*	TESTMODE
	M2	CFSB	JTAG_SEL
ATCRTMR1_XTAL24M_IN	F11	XI0	JTAG_TCK
ATCRTMR1_XTAL24M_OUT	E11	XO0	JTAG_TMS
			JTAG_TDI
			JTAG_TDO
			JTAG_TRST*
			ANALOGMUX_OUT
			TST_CLKOUT
			TST_CLK_LVDS_0_P
			TST_CLK_LVDS_0_N
			TST_CLK_LVDS_1_P
			TST_CLK_LVDS_1_N

CLOCKS AND RESET / TEST AND DEBUG

ATCRTMR1_TESTMODE	L9
ATCRTMR1_JTAG_SEL	C11
SWD_NUB_ATCRTMR01_SWCLK	B11
SWD_NUB_ATCRTMR01_SWDIO	D10
TP_ATCRTMR1_JTAG_TDI	D9
ATCRTMR1_JTAG_TDO	C10
TP_ATCRTMR1_JTAG_TRESET	E10
TP_ATCRTMR1_ANALOGMUX_OUT	F9
TP_ATCRTMR1_TST_CLKOUT	M10
NC_ATCRTMR1_CLK_LVDSP<0> NO_TEST=1	H10
NC_ATCRTMR1_CLK_LVDSN<0> NO_TEST=1	H11
NC_ATCRTMR1_CLK_LVDSP<1> NO_TEST=1	G11
NC_ATCRTMR1_CLK_LVDSN<1> NO_TEST=1	G10

ATCRTMR1_XTAL24M_OUT

RF160 499 1% 1/20W TK 0201
197S0591 CRITICAL YF100 1.60X1.20MM 24.000MHZ-20PPM-9.5PF-60OHM
ATC1_24M_O_R — ATCRTMR1_XTAL24M_IN
CF160 CRITICAL 15PF 5% 50V C0G 0201
CF161 CRITICAL 131S0831 15PF 5% 50V C0G 0201

PP0V855_ATCRTMR01_VDD_CIO

CF130 14UF 20% 4V X5R 0402-D2X-1 — 138S00149
CF131 14UF 20% 4V X5R 0402-D2X-1
CF132 0.1UF 10% 6.3V X6S 0201
CF133 0.1UF 10% 6.3V X6S 0201

UF100
TMNB25B1-K1S1
FCCSP
338S00888
SYM 2 OF 2
OMIT_TABLE
CRITICAL

VDD_CIO_0	J4	VDDIO12_CIO_0	K5
VDD_CIO_0	J6	VDDIO12_CIO_0	K7
VDD_CIO_0	J8	VDDIO12_CIO_0	L6
VDD_CIO_1	F4	VDDIO12_CIO_1	D6
VDD_CIO_1	F6	VDDIO12_CIO_1	E5
VDD_CIO_1	F8	VDDIO12_CIO_1	E7
		VDDIO12_PLL_SOC0	K8
		VDDIO12_PLL_SOC1	H8
		VDDIO12_XTAL	H9
		VDDIO12	E9
		VDDIO12	H3
		VDDIO12	K9
VDD_FIXED	G4	VDDIO12_EFUSE1	F3
VDD_FIXED	G5	VDDIO12_AMUX	F7
VDD_FIXED	H5		
VDD_FIXED	H6		
VDD_FIXED_PLL	G7		
VDD_FIXED_XTAL	G9		

VSS: A1, A2, A4, A6, A8, A10, A11, B2, B4, B6, B8, B10, C3, C5, C6, C7, C9, D1, D5, D7, D11, E3, E4, E6, E8, F2, F5, F10, G3, G6, G8 (J4, J6, J8, F4, F6, F8, G4, G5, H5, H6, G7, G9, K5, K7, L6, D6, E5, E7, K8, H8, H9, E9, H3, K9, F3, F7 also VSS)
VSS: H4, H7, J2, J3, J5, J7, J10, K4, K6, L1, L5, L7, L11, M3, M5, M6, M7, M9, N2, N4, N6, N8, N10, P1, P2, P4, P6, P8, P10, P11

PP1V2_ATCRTMR01_VDDIO

132S0395 CF134 0.1UF 10% 6.3V X6S 0201
138S00039 CF135 2.2UF 20% 4V X6S-CERM 0201
CF136 14UF 20% 4V X5R 0402-D2X-1
CF137 14UF 20% 4V X5R 0402-D2X-1

PP0V805_ATCRTMR01_VDD_FIXED

CF140 0.1UF 10% 6.3V X6S 0201
CF141 0.1UF 10% 6.3V X6S 0201
CF142 2.2UF 20% 4V X6S-CERM 0201
CF143 2.2UF 20% 4V X6S-CERM 0201
CF144 2.2UF 20% 4V X6S-CERM 0201
CF145 14UF 20% 4V X5R 0402-D2X-1
CF146 14UF 20% 4V X5R 0402-D2X-1

PP1V2_ATCRTMR01_VDDIO

138S00039 CF152 2.2UF 20% 4V X6S-CERM 0201 — PLACE_NEAR=UF100.K8:5MM
155S0644 FLF100 240-OHM-0.2A-0.9-OHM 0201
PP1V2_ATCRTMR01_VDDIO_XTAL_F VOLTAGE=1.2V
CF162 0.1UF 10% 6.3V X6S 0201 — 132S0395
CF163 2.2UF 20% 4V X6S-CERM 0201 — 138S00039

Connect to GND directly or via a resistor
GND

PP0V805_ATCRTMR01_VDD_FIXED

CF150 0.1UF 10% 6.3V X6S 0201 — PLACE_NEAR=UF100.G7:5MM
132S0395 CF164 0.1UF 10% 6.3V X6S 0201

PPVDD_FIXED_ATCRTMR1_XTAL_R

PP0V805_ATCRTMR01_VDD_FIXED — RF151 10 1/20W TK 0201 — VOLTAGE=0.805V
CF151 4UF 20% 2.5V X6S 0201 — 117S00094 — 138S00329

PACK_OPTION=ATC_BOUNDARYSCAN:YES
RF145 47K 1/20W 5% TK 0201 — ATCRTMR1_JTAG_TDO
PACK_OPTION=ATC_BOUNDARYSCAN:NO
RF147 47K 1/20W 5% TK 0201 — ATCRTMR1_JTAG_SEL
PACK_OPTION=ATC_BOUNDARYSCAN:YES
RF140 10K 1/20W 5% TK 0201 — ATCRTMR1_TESTMODE
PACK_OPTION=ATC_BOUNDARYSCAN:NO

RF197 33 1/20W 5% TK 0201 — SPI_ATCRTMR1_DIO<0> / SPI_ATCRTMR1_R_DIO<0>
RF198 33 1/20W 5% TK 0201 — SPI_ATCRTMR1_DIO<1> / SPI_ATCRTMR1_R_DIO<1>

PP1V2_ATCRTMR01_VDDIO

RF190 3.3K 5% 1/20W TK 0201
NOSTUFF RF191 3.3K 5% 1/20W TK 0201
NOSTUFF RF192 3.3K 5% 1/20W TK 0201
NOSTUFF RF193 3.3K 5% 1/20W TK 0201
CF190 1.0UF 20% 6.3V X5R 0201-1

OMIT_TABLE
CRITICAL
335S00574
UF190
64MBIT-1.2V
W25Q64NE
XSON-1

SPI_ATCRTMR1_CLK	RF194 33	6	SPI_ATCRTMR1_CLK_R
SPI_ATCRTMR1_CS_L		1	SPI_ATCRTMR1_CS_L
SPI_ATCRTMR1_DIO<2>	RF195 33	3	SPI_ATCRTMR1_R_DIO<2>
SPI_ATCRTMR1_DIO<3>	RF196 33	7	SPI_ATCRTMR1_R_DIO<3>
		5	SPI_ATCRTMR1_R_DIO<0>
		2	SPI_ATCRTMR1_R_DIO<1>

CLK, CS*, WP*(IO2), HOLD*(IO3), DI(IO0), DO(IO1), GND, EPAD

PACK_OPTION=ATC_RTMR_ROM:XSON

PP1V2_ATCRTMR01_VDDIO

UF190
64MBIT-1.2V
GD25UF64E
WLCSP-COMBO

SPI_ATCRTMR1_CLK_R	D2	SCLK	
SPI_ATCRTMR1_CS_L	B3	CS*	
SPI_ATCRTMR1_R_DIO<2>	D3	IO2	
SPI_ATCRTMR1_R_DIO<3>	C2	IO3	
		SI(IO0)	E2 SPI_ATCRTMR1_R_DIO<0>
		SO(IO1)	C3 SPI_ATCRTMR1_R_DIO<1>

OMIT_TABLE 335S00638
NC: A2, A3, F2, F3
VSS: E3

PACK_IGNORE=TRUE
PACK_OPTION=ATC_RTMR_ROM:WLCSP

BOM_COST_GROUP=TBT

PAGE TITLE: USB-C: High Speed ATC1

Apple Inc.

DRAWING NUMBER: 051-08286
SIZE: D
REVISION: 5.0.3
BRANCH:
PAGE: 151 OF 700
SHEET: 81 OF 168

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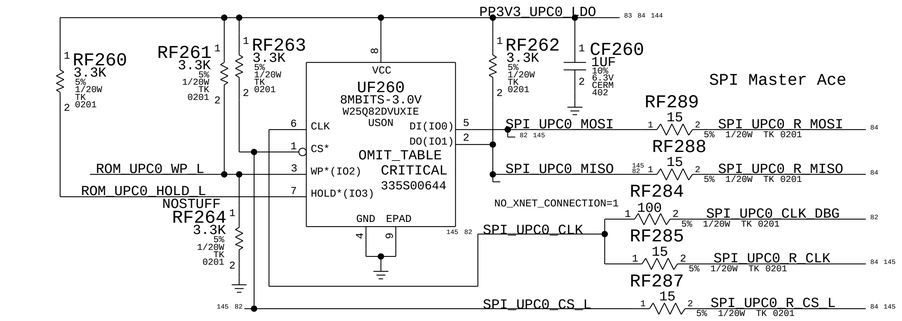
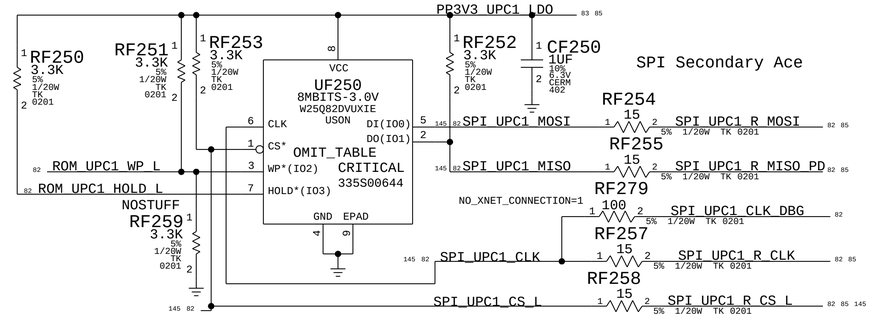


PACK_OPTION=UPC1_ROM:YES



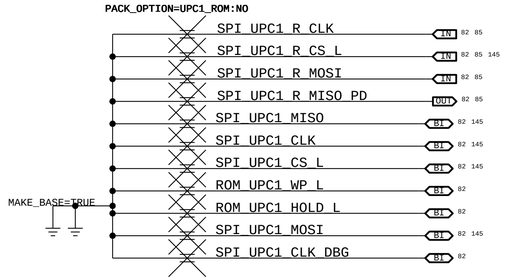
UPC1 Dedicated ROM and UART Debug chain possible pack_options:

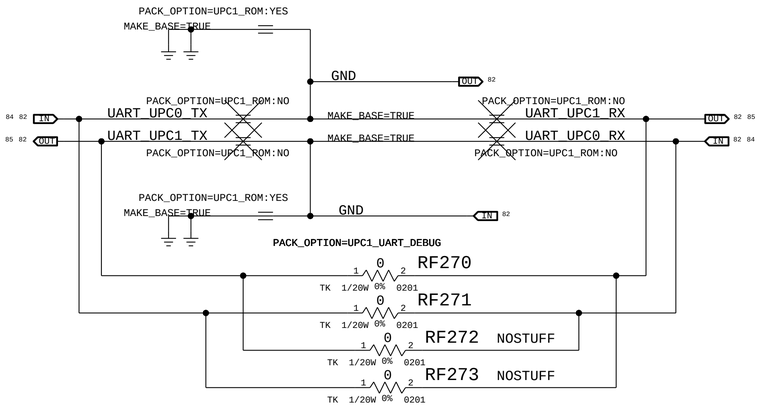
1. UPC1 may need its own ROM and need a fall-back method to no ROM for UPC1
 pick: "UPC1_ROM:YES" , "UPC1_UART_DEBUG" and "UPC1_UART_PD:NO"

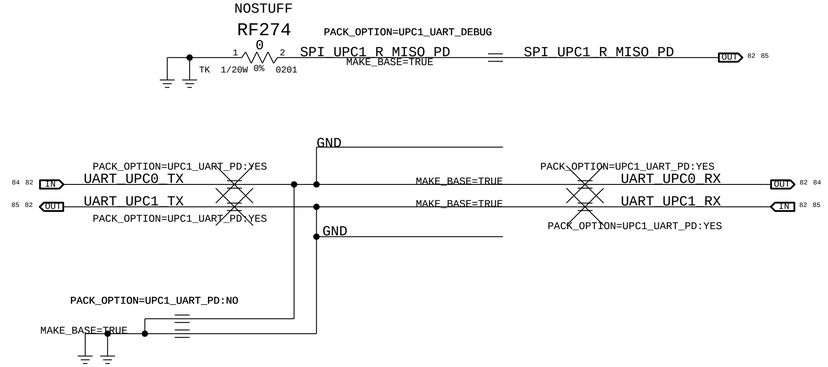
2. UPC1 needs its own ROM and do not need a fall-back method to no ROM for UPC1
 pick: "UPC1_ROM:YES" and "UPC1_UART_PD:YES"

3. UPC1 does not need its own ROM
 pick: "UPC1_ROM:NO" and "UPC1_UART_PD:NO"

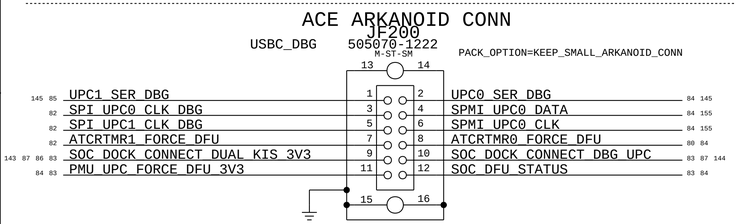
Ace 1 is UART Ace?

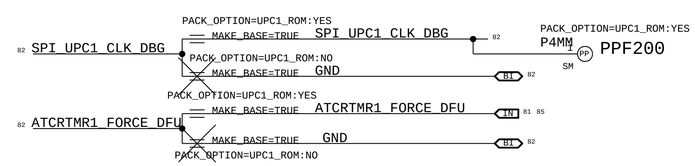




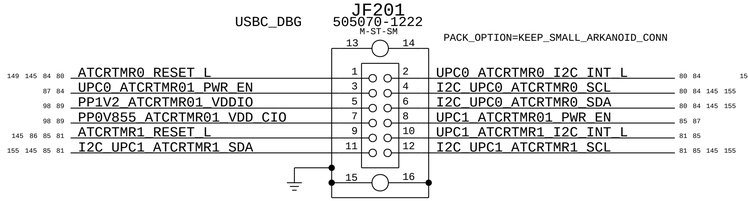


ACE ARKANOID CONN

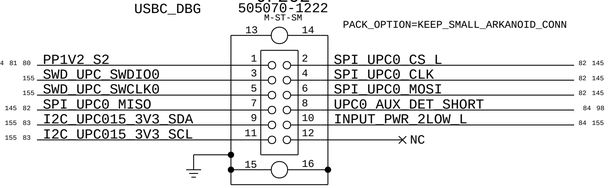


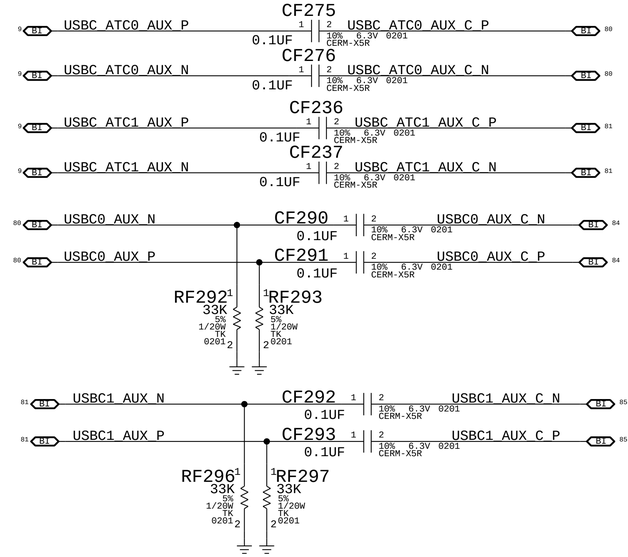


BRIDGE ARKANOID CONN



AARDVARKANOID CONN UPC0





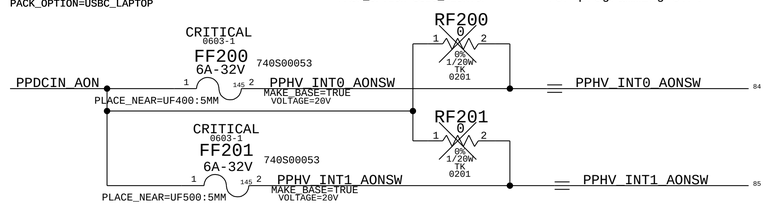
HV POWER ALIASES

Fuses for laptop charging.

PACK_OPTION=USBC_LAPTOP

PACK_IGNORE=TRUE
PACK_OPTION=USBC_DESKTOP

Desktops only need connection for programming OTP.



BOM_COST_GROUP=USB-C

PAGE TITLE
USB-C: Support 1 ATC01

Apple Inc.

DRAWING NUMBER 051-08286
SIZE D
REVISION 5.0.3
BRANCH
PAGE 152 OF 700
SHEET 82 OF 168

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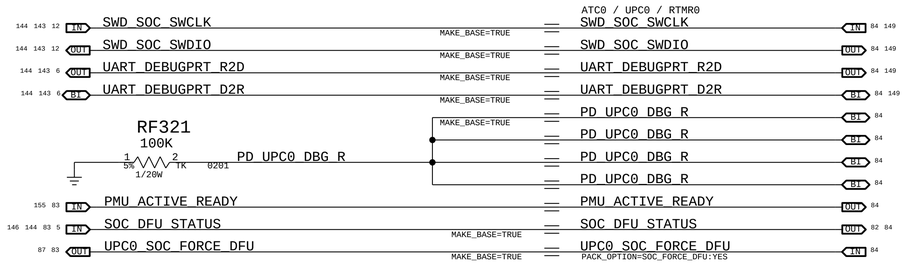
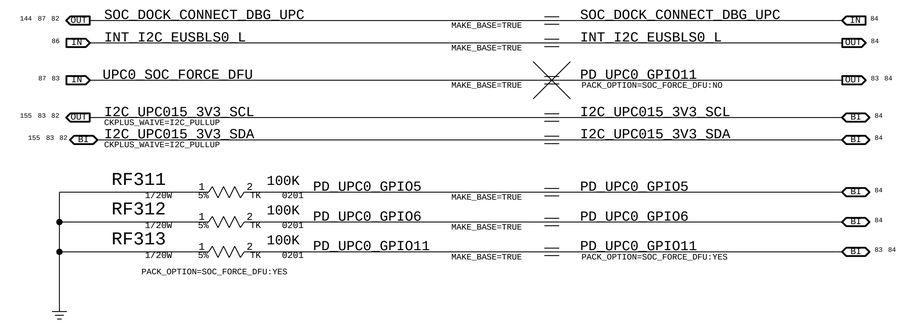
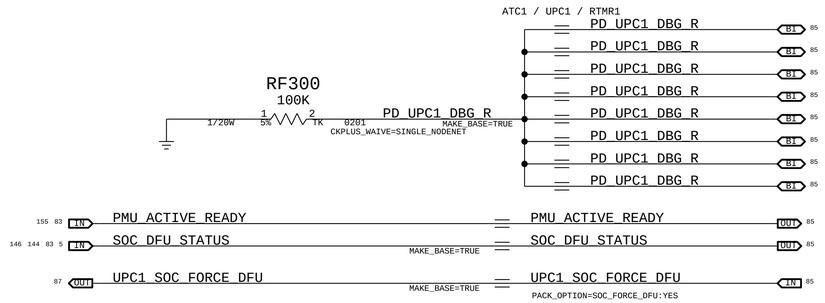
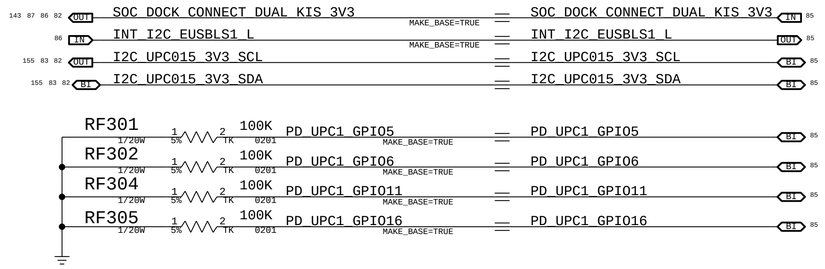
UPC 0 is the Debug Port





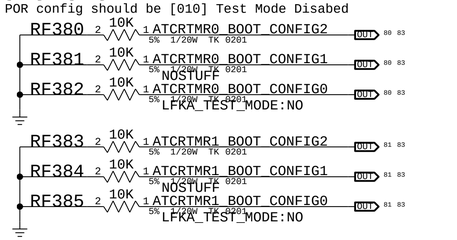
UPC 1 GPIOs

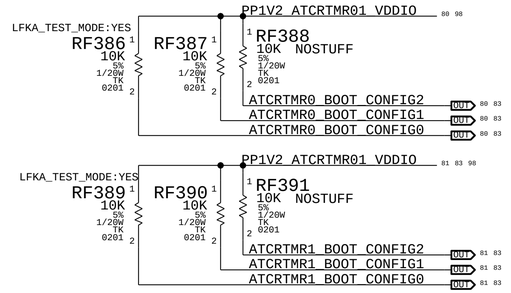




ATCRTMR Boot Config

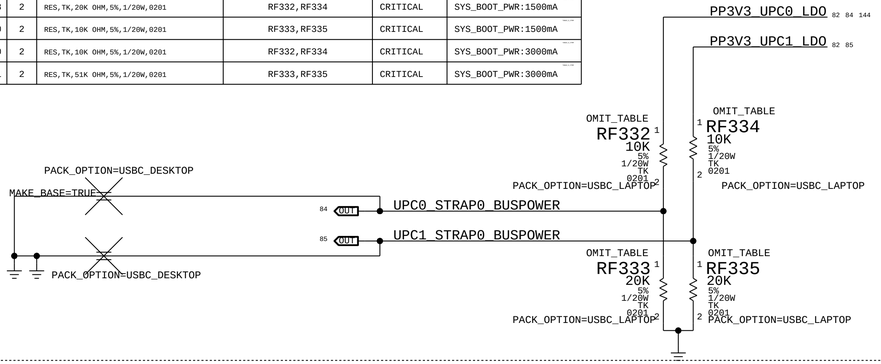
[2:0] = [011] 30Mhz QSPI and Test Mode Enabled
POR config should be [010] Test Mode Disabed



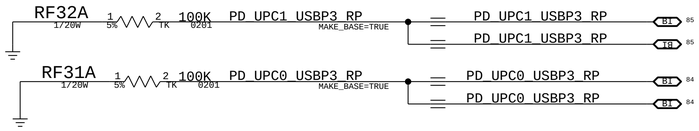


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
117S00073	2	RES,TK,0 OHM, 1A MAX,1/20W,0201	RF332,RF334	CRITICAL	SYS_BOOT_PWR:DEFAULT_500mA
117S00073	2	RES,TK,0 OHM, 1A MAX,1/20W,0201	RF333,RF335	CRITICAL	SYS_BOOT_PWR:DISABLED
117S00131	2	RES,TK,51K OHM,5%,1/20W,0201	RF332,RF334	CRITICAL	SYS_BOOT_PWR:1000mA
117S00090	2	RES,TK,10K OHM,5%,1/20W,0201	RF333,RF335	CRITICAL	SYS_BOOT_PWR:1000mA
117S00098	2	RES,TK,20K OHM,5%,1/20W,0201	RF332,RF334	CRITICAL	SYS_BOOT_PWR:1500mA
117S00090	2	RES,TK,10K OHM,5%,1/20W,0201	RF333,RF335	CRITICAL	SYS_BOOT_PWR:1500mA
117S00090	2	RES,TK,10K OHM,5%,1/20W,0201	RF332,RF334	CRITICAL	SYS_BOOT_PWR:3000mA
117S00131	2	RES,TK,51K OHM,5%,1/20W,0201	RF333,RF335	CRITICAL	SYS_BOOT_PWR:3000mA

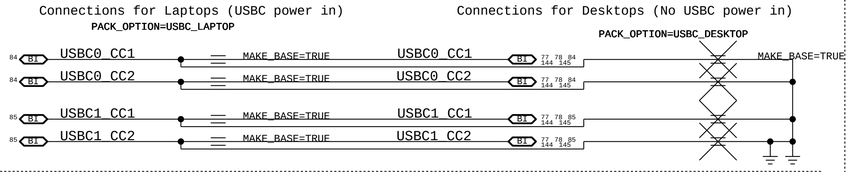
STRAP0/BUSPOWER



Unused ports

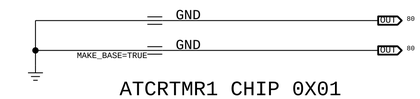


Connections for Laptops (USBC power in)

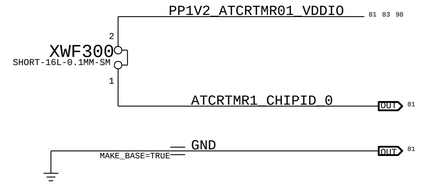


Connections for Desktops (No USBC power in)

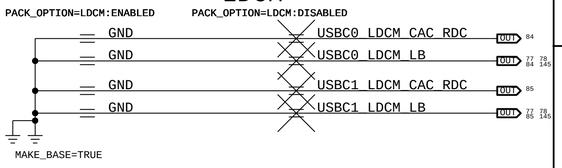
ATCRTMR0 CHIP 0X00



ATCRTMR1 CHIP 0X01

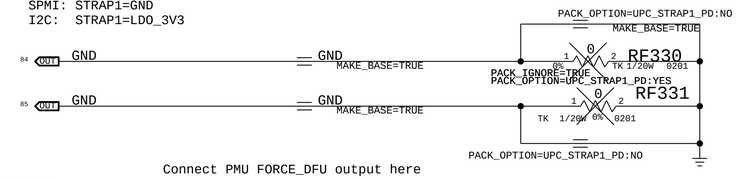


LDCM



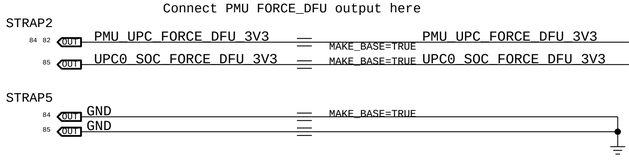
STRAPS Configurations

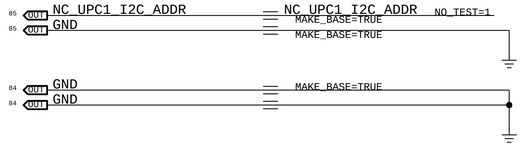
For production tie SPMI STRAP to GND directly
Enables SPMI Interface to SoC
SPMI: STRAP1=GND
I2C: STRAP1=LDO_3V3



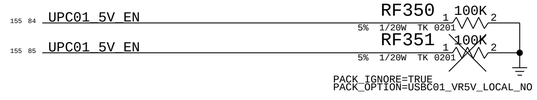
UPC0: STRAP3=GND STRAP4=GND
UPC1: STRAP3=NC STRAP4=GND
UPC2: STRAP3=GND STRAP4=NC
UPC5: STRAP3=NC STRAP4=140K

Connect PMU FORCE_DFU output here





Is UPCx_5V_EN being used?



PP TO AVOID UPC01_REQUEST_DFU NOT CONNECTED WARNING

BOM_COST_GROUP=USB-C

PAGE TITLE
USB-C: Support 2 ATC01

Apple Inc.

DRAWING NUMBER 051-08286
SIZE D
REVISION 5.0.3
BRANCH
PAGE 153 OF 700
SHEET 83 OF 168

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*** IN PROGRESS ***

82 PPHV_INT0_AONSW

MAX 100uF TOTAL ON RAIL

151 85 PP5V_S2SW_USBC01

151 85 PP5V_S2SW_USBC01

138S00123
CF406 10UF 20% 10V X5R 0402

PP_5V0 PP_CABLE PP_HV VBUS

OMIT_TABLE

UF400
SN2012024
BGA

POWER

DIGITAL CORE I/O & CONTROL

TYPE-C

PORT MUX

		M22	HRESET	
145 84	PD_UPC0_MRESET	H18	GPIO14_MRESET	
149 145 82 80 OUT	ATCRTMR0_RESET_L	B4	GPIO15_RESETZ	
145 82 OUT	UPC0_SER_DBG	F26	GPIO0	
83 IN	PMU_ACTIVE_READY	D18	GPIO1	
83 82 IN	SOC_DFU_STATUS	K24	GPIO2	
83 OUT	UPC0_SOC_FORCE_DFU	L21	GPIO3	PU
83 OUT	SOC_DOCK_CONNECT_DBG_UPC	J25	GPIO4	
83 OUT	PD_UPC0_GPIO5	J9	GPIO5	
83 IN	PD_UPC0_GPIO6	C1	GPIO6	
155 83 OUT	UPC01_5V_EN	C5	GPIO7	
82 80 OUT	ATCRTMR0_FORCE_DFU	F10	GPIO8	
82 80 IN	UPC0_ATCRTMR0_I2C_INT_L	H10	GPIO9	PU
83 IN	INT_I2C_EUSBLS0_L	A3	GPIO10	PU
83 BI	PD_UPC0_GPIO11	L25	GPIO11	
155 82 OUT	INPUT_PWR_2LOW_L	E11	GPIO12	PU
157 OUT	UPC_DFU_BOOTED_L	M26	GPIO16_DFU_BOOTED_L	
155 OUT	UPC_PMU_RESET_1V2	G19	GPIO17_FORCE_RST_REQ	
80 BI	USBC0_CIO_LSTX	L13	GPIO18_LSTXRX	
80 OUT	USBC0_CIO_LSRX	C3	GPIO19_LSRX	
98 82 OUT	UPC0_AUX_DET_SHORT	N23	GPIO20_SS_HOLD	
80 IN	ATCRTMR0_LSTX_DIR	G25	GPIO21_LSX_DIR	
83 IN	UPC0_STRAP0_BUSPOWER	J17	STRAP0_BUSPOWER	
83 IN	GND	L27	STRAP1_I2C_SPMI_SEL	
83 82 IN	PMU_UPC_FORCE_DFU_3V3	J13	STRAP2_DFU_EN	
83 IN	GND	M20	STRAP3_I2C_ADDR0	
83 IN	GND	N21	STRAP4_I2C_ADDR1	
83 IN	GND	J21	STRAP5_VDDIO_CFG	
	UPC0_R_OSC	B10	R_OSC	
155 87	NC_UPC0_AID0	F14	AID0	
	NC_UPC0_AID1 NO_TEST=1	G15	AID1	
	NC_UPC0_AID2 NO_TEST=1	H14	AID2	
	NC_UPC0_AID3 NO_TEST=1	E15	AID3	
155 145 82 80 BI	I2C_UPC0_ATCRTMR0_SDA	A25	I2C_SDA	
155 145 82 80 BI	I2C_UPC0_ATCRTMR0_SCL	B26	I2C_SCL	
83 BI	I2C_UPC015_3V3_SDA	K28	I2C1_SDA_GPIO23	
83 IN	I2C_UPC015_3V3_SCL	J27	I2C1_SCL_GPIO22	
	NC_INT_I2C_UPC0_L NO_TEST=1	H26	I2C_IRQ1Z	
155 82 BI	SPMI_UPC0_DATA	N25	SPMI_I2C2_DATA	1V25
155 82 IN	SPMI_UPC0_CLK	M24	SPMI_I2C2_CLK	1V25
	NC_INT_I2C_SMC_UPC0_L NO_TEST=1	K26	I2C_IRQ2Z	
145 82 OUT	SPI_UPC0_R_CLK	G27	SPI_CLK	
82 OUT	SPI_UPC0_R_MOSI	H28	SPI_COPI	
82 IN	SPI_UPC0_R_MISO	F28	SPI_CIPO	
145 82 OUT	SPI_UPC0_R_CS_L	E27	SPI_CSZ	
155 12 BI	SWD_UPC_SWDIO0	E25	SWD_DATA	IPU
155 12 BI	SWD_UPC_SWCLK0	E23	SWD_CLK	IPU
84 82 IN	UART_UPC0_RX	D28	UART_RX	
82 OUT	UART_UPC0_TX	C27	UART_TX	
98 BI	USB2_UPC0_P1_P	A15	USB_RP1_P	
98 BI	USB2_UPC0_P1_N	B16	USB_RP1_N	
158 BI	USB_DBG_LS_P	A17	USB_RP2_P	
158 BI	USB_DBG_LS_N	B18	USB_RP2_N	
83 BI	PD_UPC0_USBP3_RP	A19	USB_RP3_P	
83 BI	PD_UPC0_USBP3_RP	B20	USB_RP3_N	
82 BI	USBC0_AUX_C_P	D14	AUX_P	
82 BI	USBC0_AUX_C_N	C15	AUX_N	
84	PD_UPC0_HPD	G11	GPIO13_HPDTXRX	
149 83 IN	SWD_SOC_SWCLK	E19	DEBUG0_GPIO24	
149 83 OUT	SWD_SOC_SWDIO	F18	DEBUG1_GPIO25	
149 83 OUT	UART_DEBUGPRT_R2D	H22	DEBUG2_GPIO26	
149 83 BI	UART_DEBUGPRT_D2R	D22	DEBUG3_GPIO27	
83 BI	PD_UPC0_DBG_R	G23	DEBUG4_GPIO28	
83 BI	PD_UPC0_DBG_R	F22	DEBUG5_GPIO29	
83 BI	PD_UPC0_DBG_R	C23	DEBUG6_GPIO30	
83 BI	PD_UPC0_DBG_R	D26	DEBUG7_GPIO31	

1M 5% 1/20W TK 0201 RF405 UART_UPC0_RX 82 84

100K 5% 1/20W TK 0201 RF406 PD_UPC0_MRESET 84 145

100K 5% 1/20W TK 0201 RF407 PD_UPC0_HPD 84

Either a Testpoint or Arkanoid connector must be present for GPIO0 (EVEN IN PRODUCTION)

CRITICAL RF403 15K 0.1% 1/20W TK 0201 103S00582

Configurable as SPMI or I2C Port 2
SMC SPMI: 0XD
AP SPMI: 0XC
I2C: 0X38

REAR PORT: CONNECT UPC SPI TO ROM
FRONT PORT: GROUND UPC SPI

GROUND

GND A1 B2 K16 K20 M28 N19 N27

VIN_3V3	C19		
VDDIO	C25		
LDO_3V3	B22		
LDO_1V8	A23		
VIN_LV	A27		
	B28		
VOUT_LV	B24		
SS	A5	UPC0_SS	
LDO_CORE	A21	PP1V5_UPC0_LDO_CORE	
C_CC1	M16	USBC0_CC1	
	N15		
C_CC2	M18	USBC0_CC2	
	N17		
RPD_G1	L17	USBC0_CC1	BI 83
RPD_G2	L19	USBC0_CC2	BI 83
C_USB_TP	A11	USBC0_USB_TOP_P	BI 77 78 144
C_USB_TN	A13	USBC0_USB_TOP_N	BI 77 78 144
C_USB_BP	B12	USBC0_USB_BOT_P	BI 77 78
C_USB_BN	B14	USBC0_USB_BOT_N	BI 77 78
C_SBU1	C11	USBC0_SBU1	BI 77 78 144
C_SBU2	D10	USBC0_SBU2	BI 77 78 144
3V3 LDCM	B8	USBC0_LDCM_CAC_RDC	
3V3 LDCM_LB	C7	USBC0_LDCM_LB	IN 77 78 83 145
3V3 LDCM_SENSE	A7	USBC0_LDCM_SW	
3V3 LDCM_COMP	B6	USBC0_LDCM_COMP	
3V3 LDCM_SW	A9	USBC0_LDCM_SW	

PPVBUS_USBC0 77 78 144 145

CF401 1UF 10% 35V X5R 0402

DF400 DSN2 NSR20F40NX_G CRITICAL 371S00085

PP3V3_S2 85 87 88 150

CF400 10UF 20% 6.3V CERM 0402

PP1V2_S2 80 81 82 85 87 88 150

MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.0750
VOLTAGE=3.3V

CF402 1.0UF 20% 6.3V X5R 0201-1

PP3V3_UPC0_LDO 82 83 144

MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.0750
VOLTAGE=1.8V

CF408 10UF 20% 6.3V CERM 0402

PP1V8_UPC0_LDO

CF417 10UF 20% 6.3V CERM 0402

PP1V8_S2 85 88 150

CF403 0.1UF 10% 6.3V CERM-X5R 0201

UPC0_ATCRTMR01_PWR_EN 82 87
(cap needed when used as power source)

VOLTAGE=1.5V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.0750

CF405 10UF 20% 6.3V CERM 0402

PACK_OPTION=ACE2_SS_CAP

CF409 0.68UF 5% 6.3V X6S 0402

PACK_OPTION=ACE2_SS_GND
GND
MAKE_BASE=TRUE

MIN_LINE_WIDTH=0.4000
MIN_NECK_WIDTH=0.1500

BI 77 78 83 144 145

MIN_LINE_WIDTH=0.4000
MIN_NECK_WIDTH=0.1500

BI 77 78 83 144 145

CF414 220PF 5% 50V C0G 0201-1

CF413 220PF 5% 50V C0G 0201-1

LDCM circuit subject to change

PACK_OPTION=LDCM:ENABLED
CRITICAL
CF420 2.2UF 10% 35V X5R 0402 138S00488

CAC

RDC

PACK_OPTION=LDCM:ENABLED
CRITICAL
RF411 402K 1% 1/20W TK 0201 118S00666

PACK_IGNORE=TRUE
PACK_OPTION=LDCM:DISABLED
RF414 100K 5% 1/20W TK 0201

PACK_OPTION=LDCM:DISABLED
10K RF415 1/20W 5% 0201 TK

PACK_OPTION=LDCM:ENABLED
R2 4.99K CRITICAL RF410 1/20W 0.1% 0201 TK 103S00656

PACK_OPTION=LDCM:ENABLED

PACK_OPTION=LDCM:ENABLED
CRITICAL
RF413 10K 1/20W 0.1% 0201 TK 103S00593

78 77 IN USBC0_LDCM R1 USBC0_LDCM_R

BOM_COST_GROUP=USB-C

PAGE TITLE	USB-C: Port Controller ATC0
	Apple Inc.
DRAWING NUMBER	051-08286
SIZE	D
REVISION	5.0.3
BRANCH	
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82 PPHV_INT1_AONSW

MAX 100uF TOTAL ON RAIL

151 84 PP5V_S2SW_USBC01

151 84 PP5V_S2SW_USBC01

138S00123
CF506
10UF
20%
16V
X5R
0402

K10 K12 L9 L11 M10 M12 N9 N11 — PP_5V0

M14 N13 — PP_CABLE

D2 D4 E1 E3 F2 F4 G1 G3 H2 H4 J1 J3 K2 K4 L1 L3 M2 M4 N1 N3 — PP_HV

D6 D8 E5 E7 F6 F8 G5 G7 H6 H8 J5 J7 K6 K8 L5 L7 M6 M8 N5 N7 — VBUS

OMIT_TABLE
UF500
SN2012024
BGA

M22 HRESET

85		PD_UPC1_MRESET	H18	GPIO14_MRESET	
145 86 82 81	OUT	ATCRTMR1_RESET_L	B4	GPIO15_RESETZ	
145 82	OUT	UPC1_SER_DBG	F26	GPIO0	
83	IN	PMU_ACTIVE_READY	D18	GPIO1	
83	IN	SOC_DFU_STATUS	K24	GPIO2	
83	OUT	UPC1_SOC_FORCE_DFU	L21	GPIO3	PU
83	OUT	SOC_DOCK_CONNECT_DUAL_KIS_3V3	J25	GPIO4	
83	OUT	PD_UPC1_GPIO5	J9	GPIO5	
83	IN	PD_UPC1_GPIO6	C1	GPIO6	
155 83	OUT	UPC01_5V_EN	C5	GPIO7	
82 81	OUT	ATCRTMR1_FORCE_DFU	F10	GPIO8	
82 81	IN	UPC1_ATCRTMR1_I2C_INT_L	H10	GPIO9	PU
83	IN	INT_I2C_EUSBLS1_L	A3	GPIO10	PU
83	BI	PD_UPC1_GPIO11	L25	GPIO11	
155	OUT	INPUT_PWR_2LOW_L	E11	GPIO12	PU
83	OUT	PD_UPC1_GPIO16	M26	GPIO16_DFU_BOOTED_L	
155	OUT	UPC_PMU_RESET_1V2	G19	GPIO17_FORCE_RST_REQ	
81	BI	USBC1_CIO_LSTX	L13	GPIO18_LSTXRX	
81	OUT	USBC1_CIO_LSRX	C3	GPIO19_LSRX	
98	OUT	UPC1_AUX_DET_SHORT	N23	GPIO20_SS_HOLD	
81	IN	ATCRTMR1_LSTX_DIR	G25	GPIO21_LSX_DIR	
83	IN	UPC1_STRAP0_BUSPOWER	J17	STRAP0_BUSPOWER	
83	IN	GND	L27	STRAP1_I2C_SPMI_SEL	
83	IN	UPC0_SOC_FORCE_DFU_3V3	J13	STRAP2_DFU_EN	
83	IN	NC_UPC1_I2C_ADDR	M20	STRAP3_I2C_ADDR0	
83	IN	GND	N21	STRAP4_I2C_ADDR1	
83	IN	GND	J21	STRAP5_VDDIO_CFG	
		UPC1_R_OSC	B10	R_OSC	
		NC_UPC1_AID0 NO_TEST=1	F14	AID0	
		NC_UPC1_AID1 NO_TEST=1	G15	AID1	
		NC_UPC1_AID2 NO_TEST=1	H14	AID2	
		NC_UPC1_AID3 NO_TEST=1	E15	AID3	
155 145 82 81	BI	I2C_UPC1_ATCRTMR1_SDA	A25	I2CC_SDA	
155 145 82 81	BI	I2C_UPC1_ATCRTMR1_SCL	B26	I2CC_SCL	
83	BI	I2C_UPC015_3V3_SDA	K28	I2C1_SDA_GPIO23	
83	IN	I2C_UPC015_3V3_SCL	J27	I2C1_SCL_GPIO22	
		NC_INT_I2C_UPC1_L NO_TEST=1	H26	I2C_IRQ1Z	
155	BI	SPMI_UPC1_DATA	N25	SPMI_I2C2_DATA	
155	IN	SPMI_UPC1_CLK	M24	SPMI_I2C2_CLK	
		NC_INT_I2C_SMC_UPC1_L NO_TEST=1	K26	I2C_IRQ2Z	
82	OUT	SPI_UPC1_R_CLK	G27	SPI_CLK	
82	OUT	SPI_UPC1_R_MOSI	H28	SPI_COPI	
82	IN	SPI_UPC1_R_MISO_PD	F28	SPI_CIPO	
145 82	OUT	SPI_UPC1_R_CS_L	E27	SPI_CSZ	

Configurable as SPMI
or I2C Port 2
SMC_SPMI: 0XB
AP SPMI: 0XA
I2C: 0X3F

POWER

DIGITAL CORE I/O & CONTROL

12	BI	SWD_UPC_SWDIO1	E25	SWD_DATA	IPU
12	BI	SWD_UPC_SWCLK1	E23	SWD_CLK	IPU
85 82	IN	UART_UPC1_RX	D28	UART_RX	
82	OUT	UART_UPC1_TX	C27	UART_TX	
98	BI	USB2_UPC1_P1_P	A15	USB_RP1_P	
98	BI	USB2_UPC1_P1_N	B16	USB_RP1_N	
158 87	BI	USB2_ATC1_DBG_LS_P	A17	USB_RP2_P	
158 87	BI	USB2_ATC1_DBG_LS_N	B18	USB_RP2_N	
83	BI	PD_UPC1_USBP3_RP	A19	USB_RP3_P	
83	BI	PD_UPC1_USBP3_RP	B20	USB_RP3_N	
82	BI	USBC1_AUX_C_P	D14	AUX_P	
82	BI	USBC1_AUX_C_N	C15	AUX_N	
85		PD_UPC1_HPD	G11	GPIO13_HPDTXRX	
83	BI	PD_UPC1_DBG_R	E19	DEBUG0_GPIO24	
83	BI	PD_UPC1_DBG_R	F18	DEBUG1_GPIO25	
83	BI	PD_UPC1_DBG_R	H22	DEBUG2_GPIO26	
83	BI	PD_UPC1_DBG_R	D22	DEBUG3_GPIO27	
83	BI	PD_UPC1_DBG_R	G23	DEBUG4_GPIO28	
83	BI	PD_UPC1_DBG_R	F22	DEBUG5_GPIO29	
83	BI	PD_UPC1_DBG_R	C23	DEBUG6_GPIO30	
83	BI	PD_UPC1_DBG_R	D26	DEBUG7_GPIO31	

PORT MUX

1M 5% 1/20W TK 0201 — RF505 — UART_UPC1_RX — 82 85

100K 5% 1/20W TK 0201 — RF506 — PD_UPC1_MRESET — 85

100K 5% 1/20W TK 0201 — RF507 — PD_UPC1_HPD — 85

Either a Testpoint or Arkanoid connector
must be present for GPIO0
(EVEN IN PRODUCTION)

CRITICAL
RF503
15K 0.1% 1/20W TK 0201
103S00582

Configurable as SPMI
or I2C Port 2
SMC_SPMI: 0XB
AP SPMI: 0XA
I2C: 0X3F

TYPE-C

		VIN_3V3	C19		
		VDDIO	C25		
		LDO_3V3	B22		
		LDO_1V8	A23		
		VIN_LV	A27		
			B28		
		VOUT_LV	B24	UPC1_ATCRTMR01_PWR_EN 82 87 (cap needed when used as power source)	
		SS	A5	UPC1_SS	
		LDO_CORE	A21	PP1V5_UPC1_LDO_CORE	
		C_CC1	M16	USBC1_CC1	
			N15		
		C_CC2	M18	USBC1_CC2	
			N17		
		RPD_G1	L17	USBC1_CC1 BI 83	
		RPD_G2	L19	USBC1_CC2 BI 83	
		C_USB_TP	A11	USBC1_USB_TOP_P BI 77 78	
		C_USB_TN	A13	USBC1_USB_TOP_N BI 77 78	
		C_USB_BP	B12	USBC1_USB_BOT_P BI 77 78	
		C_USB_BN	B14	USBC1_USB_BOT_N BI 77 78	
		C_SBU1	C11	USBC1_SBU1 BI 77 78 144	
		C_SBU2	D10	USBC1_SBU2 BI 77 78 144	
3V3		LDCM	B8	USBC1_LDCM_CAC_RDC	
3V3		LDCM_LB	C7	USBC1_LDCM_LB IN 77 78 83 145	
3V3		LDCM_SENSE	A7	USBC1_LDCM_SW	
3V3		LDCM_COMP	B6	USBC1_LDCM_COMP	
3V3		LDCM_SW	A9	USBC1_LDCM_SW MAKE_BASE=TRUE	

PPVBUS_USBC1 77 78 144 145

CF501 1UF 10% 35V X5R 0402

DF500 DSN2 NSR20F40NX_G CRITICAL 371S00085

PP3V3_S2 84 87 88 150

CF500 10UF 20% 6.3V CERM 0402

PP1V2_S2 80 81 82 84 87 88 150

CF502 1.0UF 20% 6.3V X5R 0201-1

MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.0750
VOLTAGE=3.3V

PP3V3_UPC1_LDO 82 83

CF508 10UF 20% 6.3V CERM 0402

MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.0750
VOLTAGE=1.8V

PP1V8_UPC1_LDO

CF517 10UF 20% 6.3V CERM 0402

PP1V8_S2 84 88 150

CF503 0.1UF 10% 6.3V CERM-X5R 0201

VOLTAGE=1.5V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.0750

CF505 10UF 20% 6.3V CERM 0402

PACK_OPTION=ACE2_SS_CAP

CF509 0.68UF 5% 6.3V X6S 0402

PACK_OPTION=ACE2_SS_GND
GND
MAKE_BASE=TRUE

MIN_LINE_WIDTH=0.4000
MIN_NECK_WIDTH=0.1500

BI 77 78 83 144
BI 77 78 83 144 145

CF514 220PF 5% 50V C0G 0201-1

CF513 220PF 5% 50V C0G 0201-1

LDCM circuit subject to change

PACK_OPTION=LDCM:ENABLED
CRITICAL
CF520 2.2UF 10% 35V X5R 0402
138S00488

CAC

RDC

PACK_OPTION=LDCM:ENABLED
CRITICAL
RF511 402K 1% 1/20W TK 0201
118S00666

PACK_IGNORE=TRUE
PACK_OPTION=LDCM:DISABLED
RF515 10K 5% 1/20W 0201 TK

PACK_OPTION=LDCM:DISABLED
RF514 100K 5% 1/20W TK 0201

PACK_OPTION=LDCM:ENABLED
CRITICAL
R2 4.99K 1/20W 0.1% 0201 TK
RF510
103S00656

PACK_OPTION=LDCM:ENABLED

PACK_OPTION=LDCM:ENABLED
CRITICAL
RF513 10K 1/20W 0.1% 0201 TK
R1
USBC1_LDCM — USBC1_LDCM_R
78 77 IN
103S00593

BOM_COST_GROUP=USB-C

GROUND

GND — A1 B2 K16 K20 M28 M19 M27

PAGE TITLE	USB-C: Port Controller ATC1
	Apple Inc.
DRAWING NUMBER	051-08286
SIZE	D
REVISION	5.0.3
BRANCH	
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*** OK2INTEGRATE ***

MACAW 0

PP1V2_S2
CF612 1.0UF 20% 6.3V X5R 0201-1
CF613 1.0UF 20% 6.3V X5R 0201-1
PLACE_NEAR=UF600.A4:5MM
PLACE_NEAR=UF600.A4:5MM

PP1V8_S2
CF604 0.1UF 10% 10V X5R-CERM 0201
CF602 0.1UF 10% 10V X5R-CERM 0201
CF603 4.7UF 20% 4V CER-X5R 0201
CF600 1.0UF 20% 6.3V X5R 0201-1
CF615 1.0UF 20% 6.3V X6S 0201-1
PLACE_NEAR=UF600.B5:5MM
PLACE_NEAR=UF600.B5:5MM
PLACE_NEAR=UF600.B5:5MM
PLACE_NEAR=UF600.B5:5MM
PLACE_NEAR=UF600.B5:5MM

PP1V1_MACAW0_VCCD
VOLTAGE=1.1V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.0750
CF606 4.7UF 20% 6.3V X6S 0402

PP3V3_S2
CF607 0.1UF 10% 10V X5R-CERM 0201
CF608 1.0UF 20% 6.3V X5R 0201-1
PLACE_NEAR=UF600.C6:5MM
PLACE_NEAR=UF600.C6:5MM

UF600
CYUSB2405A2
CSP
338S00851

BOMOPTION=USBC_DUAL_KIS:NO
PLACE_NEAR=UF690.1:2MM
EUSB_DBG_P — RF690 0 1/20W 0% TK 0201 — NO_XNET_CONNECTION=1 — EUSB_ATC0_DBG_P
EUSB_DBG_N — RF691 0 1/20W 0% TK 0201 — NO_XNET_CONNECTION=1 — EUSB_ATC0_DBG_N
PLACE_NEAR=UF690.2:2MM
BOMOPTION=USBC_DUAL_KIS:NO

ATCRTMR0_RESET_1V2_1V8_MCW_L — RF603 4.7K 5% 1/20W TK 0201 — C4 RESET*
TPF600 A TP-P50 ATCRTMR0_RESET_L_R

OMIT_TABLE
CRITICAL

INT_I2C_EUSBLS0_L — B4 INT
I2C_UPC0_ATCRTMR0_SDA — A1 SDA
I2C_UPC0_ATCRTMR0_SCL — B1 SCL
EUSB_ATC0_P — A6 EDP0
EUSB_ATC0_N — A5 EDN0
EUSB_ATC0_DBG_P — A2 EDP1
EUSB_ATC0_DBG_N — A3 EDN1
B3 CROSS
TP_MACAW0_DEBUG_SWDCLK — C3 GPIO_0/SWDCLK
TP_MACAW0_DEBUG_SWDDAT — B2 GPIO_1/SWDDAT

DP0 D6 USB2_ATC0_LS_MUX_P
DN0 D5 USB2_ATC0_LS_MUX_N
DP1 D2 USB_DBG_LS_MUX_P
DN1 D3 USB_DBG_LS_MUX_N

BOMOPTION=USBC_DUAL_KIS:YES
PP3V3_S2
CF690 1.0UF 20% 6.3V X5R 0201-1
EUSB_DBG_P — D+ CRITICAL UF690 TMUXHS221 UQFN 353S03251 DA+ — EUSB_ATC0_DBG_P
EUSB_DBG_N — D- DA- — EUSB_ATC0_DBG_N
DB+ — EUSB_ATC1_DBG_P
DB- — EUSB_ATC1_DBG_N
VCC GND SEL OE*
BOMOPTION=USBC_DUAL_KIS:YES
NO_XNET_CONNECTION=1
SOC_DOCK_CONNECT_DUAL_KIS_3V3 — SEL
RF692 47K 5% 1/20W TK 0201
LOW --> UPC0 Default KIS
HIGH --> UPC1 KIS
BOMOPTION=USBC_DUAL_KIS:YES

XIP C1 MACAW0_CLK24M_IN
XOP D1 MACAW0_CLK24M_OUT_R
RF600 0 1/20W 0% TK 0201
MACAW0_CLK24M_OUT
YF600 1.60X1.20MM 197S0591
CRITICAL CF611 9.5PF ±0.1PF 50V C0G 0201 CER-C0G 131S00077
CRITICAL 131S00077 CF610 9.5PF ±0.1PF 50V CER-C0G 0201
RESREF B6 MACAW0_RESREF
RF601 6.04K 1% 1/20W TK 0201

VCCD VDDD VDDIO VDD3V3 VSS VSSQ
C5 C2

MACAW 1

PP1V2_S2
CF662 1.0UF 20% 6.3V X5R 0201-1
CF663 1.0UF 20% 6.3V X5R 0201-1
PLACE_NEAR=UF650.A4:5MM
PLACE_NEAR=UF650.A4:5MM

PP1V8_S2
CF654 0.1UF 10% 10V X5R-CERM 0201
CF651 0.1UF 10% 10V X5R-CERM 0201
CF652 4.7UF 20% 4V CER-X5R 0201
CF653 1.0UF 20% 6.3V X5R 0201-1
CF665 1.0UF 20% 6.3V X5R 0201-1
138S00138
PLACE_NEAR=UF650.B5:5MM
PLACE_NEAR=UF650.B5:5MM
PLACE_NEAR=UF650.B5:5MM
PLACE_NEAR=UF650.B5:5MM
PLACE_NEAR=UF650.B5:5MM

PP1V1_MACAW1_VCCD
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.0750
VOLTAGE=1.1V
CF656 4.7UF 20% 6.3V X6S 0402

PP3V3_S2
CF657 0.1UF 10% 10V X5R-CERM 0201
CF658 1.0UF 20% 6.3V X5R 0201-1
PLACE_NEAR=UF650.C6:5MM
PLACE_NEAR=UF650.C6:5MM

UF650
CYUSB2405A2
CSP
338S00851

ATCRTMR1_RESET_L — C4 RESET*

OMIT_TABLE
CRITICAL

INT_I2C_EUSBLS1_L — B4 INT
I2C_UPC1_ATCRTMR1_SDA — A1 SDA
I2C_UPC1_ATCRTMR1_SCL — B1 SCL
EUSB_ATC1_P — A6 EDP0
EUSB_ATC1_N — A5 EDN0
EUSB_ATC1_DBG_P — A2 EDP1
EUSB_ATC1_DBG_N — A3 EDN1
B3 CROSS
TP_MACAW1_DEBUG_SWDCLK — C3 GPIO_0/SWDCLK
TP_MACAW1_DEBUG_SWDDAT — B2 GPIO_1/SWDDAT

DP0 D6 USB2_ATC1_LS_P
DN0 D5 USB2_ATC1_LS_N
DP1 D2 USB2_ATC1_DBG_LS_P
DN1 D3 USB2_ATC1_DBG_LS_N

XIP C1 MACAW1_CLK24M_IN
XOP D1 MACAW1_CLK24M_OUT_R
RF650 0 1/20W 0% TK 0201
MACAW1_CLK24M_OUT
YF660 1.60X1.20MM 197S0591
CRITICAL CF661 9.5PF ±0.1PF 50V C0G 0201 CER-C0G 131S00077
CRITICAL 131S00077 CF660 9.5PF ±0.1PF 50V CER-C0G 0201
RESREF B6 MACAW1_RESREF
RF651 6.04K 1% 1/20W TK 0201

VCCD VDDD VDDIO VDD3V3 VSS VSSQ
C5 C2

BOM_COST_GROUP=USB-C

PAGE TITLE: USB-C: USB2 RPT

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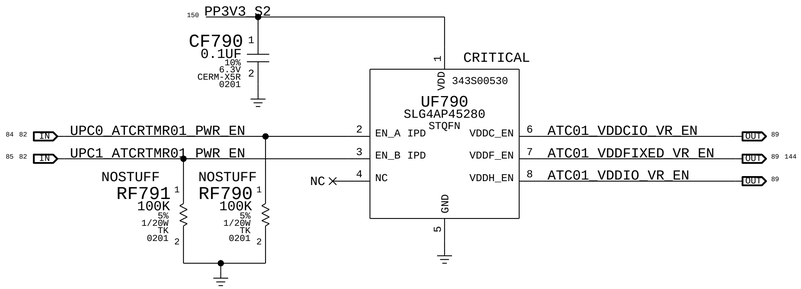
*** REFERENCE ONLY ***

Sequencing Requirements: 3.3V to UF790 --> system 1.2V (UF400 VDDIO) same time or before System 1.8V (UF400 VIN_LV pin)

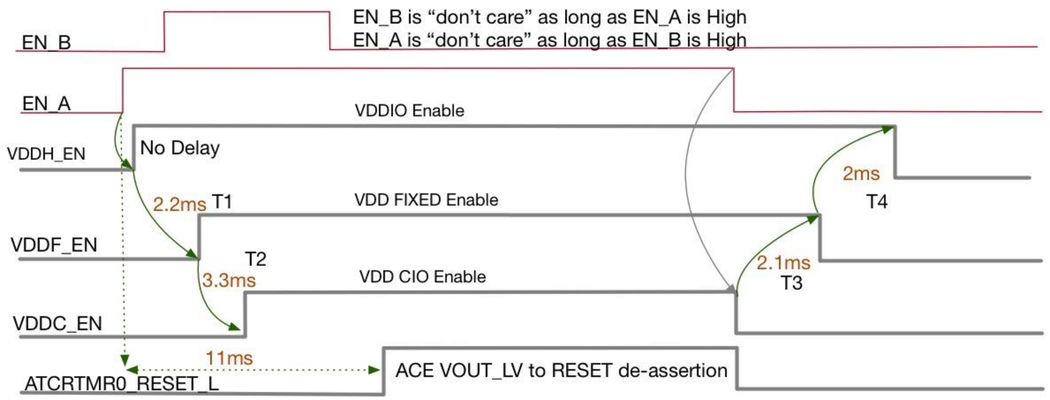
Power-up Sequence Requirements: 3.3_S2 to UF790 --> system 1.2V (UF400 VDDIO) same time or before system 1.8V (UF400) VIN_LV pin)

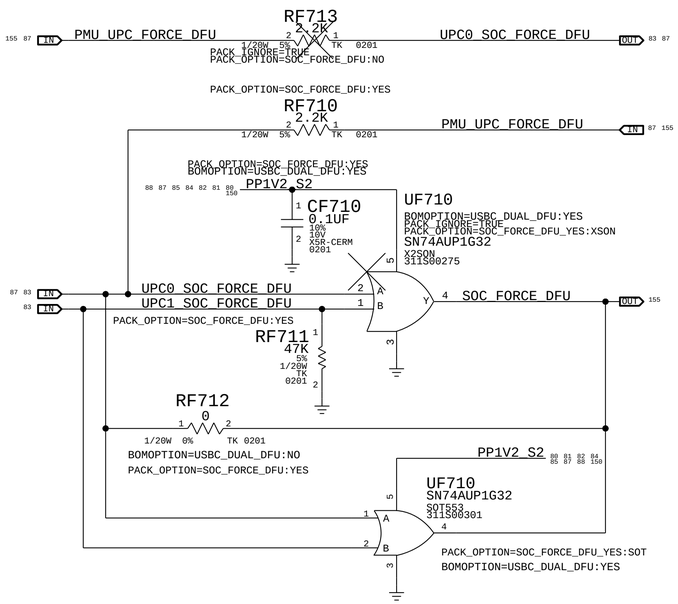
Power-down Sequence Requirements: The 1.8V first or at the same time as 1V2 --> 3V3_S2 needs to get disabled at minimum of 6ms from when 1V8 is discharged to below 300mV

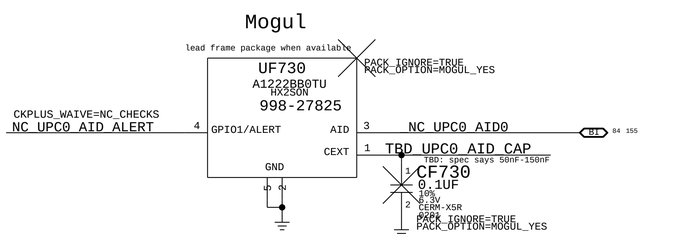
The 3.3V needs to be HIGH before VIN_LV of Aces



Note1: As long as EN_A or EN_B are High, the outputs stay High
Note2: Outputs are an ORed and delayed version of EN_A or EN_B

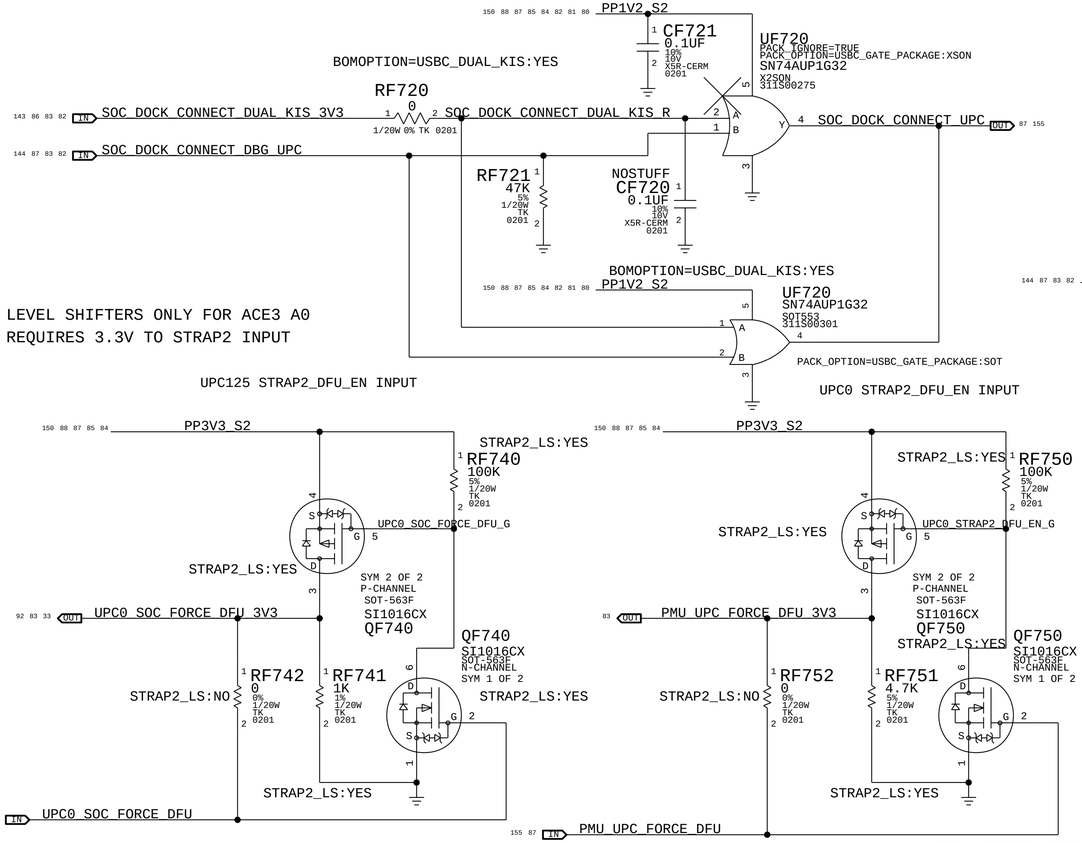




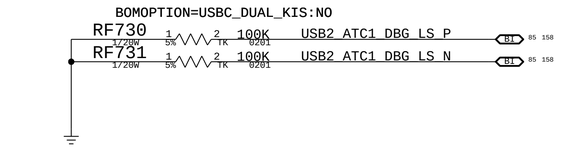


DUAL KIS Connection

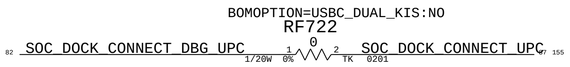
BOMOPTION=USBC_DUAL_KIS:YES



BOMOPTION=USBC_DUAL_KIS:NO



BOMOPTION=USBC_DUAL_KIS:NO



BOM_COST_GROUP=USB-C

PAGE TITLE
USB-C: Support 3 ATC01

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*** OK2INTEGRATE ***

SET ONE OPTION FOR THE PBUS CAPS

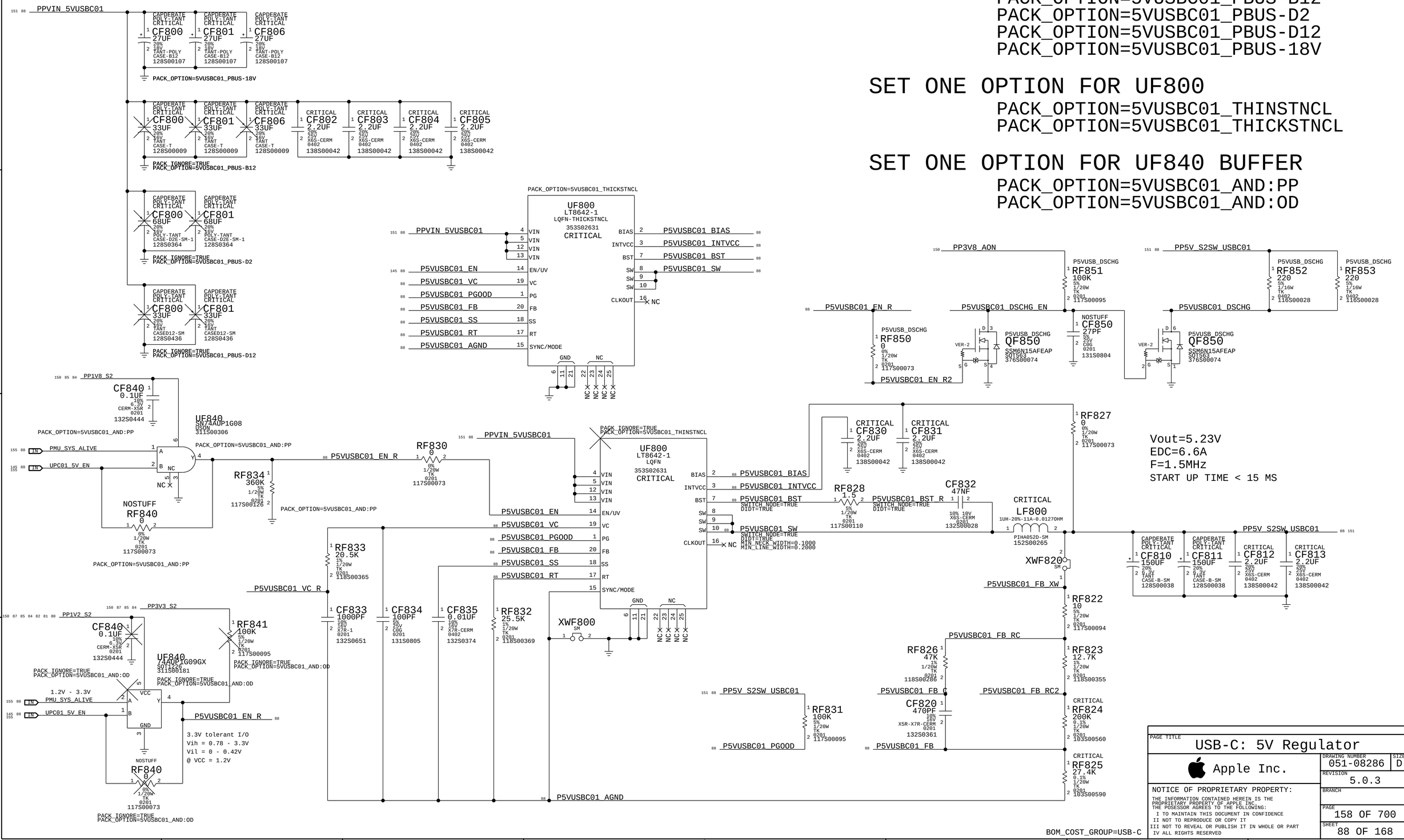
PACK_OPTION=5VUSBC01_PBUS-B12
PACK_OPTION=5VUSBC01_PBUS-D2
PACK_OPTION=5VUSBC01_PBUS-D12
PACK_OPTION=5VUSBC01_PBUS-18V

SET ONE OPTION FOR UF800

PACK_OPTION=5VUSBC01_THINSTNCL
PACK_OPTION=5VUSBC01_THICKSTNCL

SET ONE OPTION FOR UF840 BUFFER

PACK_OPTION=5VUSBC01_AND:PP
PACK_OPTION=5VUSBC01_AND:OD



PAGE TITLE: USB-C: 5V Regulator

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*** OK2INTEGRATE ***

PP1V2_ATCRTMR01_VDDIO 82 89 98
NOSTUFF
RF904 4.7K 5% 1/20W TK 0201
P1V2_ATC01_PGOOD 89
PACK_OPTION=ATC_VR_PG-RES

PP3V8_ATC01_LDO 151
XWF901 SM NO_XNET_CONNECTION=1
XWF902 SM PLACE_NEAR=UF900.8:2MM NO_XNET_CONNECTION=1
PACK_IGNORE=TRUE PACK_OPTION=ATC01_VR_MLCC-COMBO
VOLTAGE=3.8V MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000
PP3V8_ATC01_VDDIO_REG
PACK_OPTION=ATC01_VR_MLCC-REGULAR
CRITICAL CF902 CF903 CF904 CF905 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL CF902 CF903 CF904 CF905 10UF 20% 6.3V CER-X6S 0402
P1V2_ATC01_SVR_PGND VOLTAGE=0V MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000

PACK_IGNORE=TRUE PACK_OPTION=ATC01_VR_MLCC-COMBO
PP1V2_ATCRTMR01_VDDIO
CRITICAL CF908 CF909 CF910 CF911 CF912 CF913 CF914 CF915 CF916 CF917 CF918 CF919 CF920 CF921 10UF 20% 6.3V CER-X6S 0402-COMBO 82 89 98
CRITICAL CF908 CF909 CF910 CF911 CF912 CF913 CF914 CF915 CF916 CF917 CF918 CF919 CF920 CF921 10UF 20% 6.3V CER-X6S 0402
PACK_OPTION=ATC01_VR_MLCC-REGULAR

ATC01_VDDIO_VR_EN 89 87 IN
RF909 0 0% 1/20W TK 0201
RF901 100K 5% 1/20W TK 0201
RF900 100K 1% 1/20W TK 0201
P1V2_ATC01_AGND 89
P1V2_ATC01_PGOOD 89
P1V2_ATC01_COMP_FSET
UF900 TPS628502 SOT583 353S02660
VIN EN MODE_SYNC PG COMP_FSET GND SW FB
CRITICAL LF900 0.47UH-3.7A-0.034OHM PIJD16140H-SM 152S00984
DIDT=TRUE SWITCH_NODE=TRUE MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000
P1V2_ATC01_SW P1V2_ATC01_REG_XW
VOLTAGE=1.23V MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000
XWF904 SM NO_XNET_CONNECTION=1
XWF903 SM NO_XNET_CONNECTION=1
P1V2_ATC01_FB_RC
RF910 3.16K 1% 1/20W TK 0201
131S00090 CF906 100PF 5% 50V C0G 0201
P1V2_ATC01_AGND 89
P1V2_ATC01_FB_TOP_R
P1V2_ATC01_FB_R
RF907 15K 0.1% 1/20W TK 0201
RF906 316 1% 1/20W TK 0201
CF901 3300PF 10% 10V X7R-CERM 0201
P1V2_ATC01_FB_TOP
RF905 10 5% 1/20W TK 0201
XWF900 SM VOLTAGE=0V NO_XNET_CONNECTION=1 PLACE_NEAR=UF900.8:2MM
P1V2_ATC01_FB

PACK_OPTION=ATC_VR_DSCHG-EN-R:NO
RF915 0 0% 1/20W TK 0201
ATC01_VDDIO_VR_EN 89 87 IN MAKE_BASE=TRUE
PACK_IGNORE=TRUE PACK_OPTION=ATC_VR_DSCHG-EN-R:YES
ATC01_VDDIO_VR_EN
CRITICAL QF910 SSM6N37FEAP SOT563 376S00078
RF914 100K 5% 1/20W TK 0201 117S00095
NOSTUFF CF929 47PF 20% 6V 0201 CGB
ATC01_P1V2_DSCHG_EN_RC
PACK_IGNORE=TRUE PACK_OPTION=ATC_VR_MLCC-DSCHG
PP3V8_AON 150 89
PP1V2_ATCRTMR01_VDDIO 98 89 82
RF911 10 5% 1/5W TK 0402
RF912 10 5% 1/5W TK 0402
RF913 10 5% 1/5W TK 0402
P1V2_ATC01_DSCHG
CRITICAL QF910 SSM6N37FEAP SOT563 376S00078

Vout = 1.213V
Iout Max = 0.96A
F = 1.8 MHZ

PP1V2_ATCRTMR01_VDDIO 82 89 98
NOSTUFF
RF934 4.7K 5% 1/20W TK 0201
P0V855_ATC01_PGOOD 89
PACK_OPTION=ATC_VR_PG-RES

PP3V8_ATC01_LDO 151
XWF931 SM NO_XNET_CONNECTION=1
XWF932 SM PLACE_NEAR=UF930.8:2MM NO_XNET_CONNECTION=1
PACK_IGNORE=TRUE PACK_OPTION=ATC01_VR_MLCC-COMBO
VOLTAGE=3.8V MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000
PP3V8_ATC01_VDDCIO_REG
PACK_OPTION=ATC01_VR_MLCC-REGULAR
CRITICAL CF932 CF933 CF934 CF935 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL CF932 CF933 CF934 CF935 10UF 20% 6.3V CER-X6S 0402
P0V855_ATC01_SVR_PGND VOLTAGE=0V MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000

PACK_IGNORE=TRUE PACK_OPTION=ATC01_VR_MLCC-COMBO
PP0V855_ATCRTMR01_VDD_CIO
CRITICAL CF938 CF939 CF940 CF941 CF942 CF943 CF944 CF945 CF946 CF947 CF948 CF949 CF950 CF951 10UF 20% 6.3V CER-X6S 0402-COMBO 82 89 98
CRITICAL CF938 CF939 CF940 CF941 CF942 CF943 CF944 CF945 CF946 CF947 CF948 CF949 CF950 CF951 10UF 20% 6.3V CER-X6S 0402
PACK_OPTION=ATC01_VR_MLCC-REGULAR

ATC01_VDDCIO_VR_EN 89 87 IN
RF939 0 0% 1/20W TK 0201
RF931 100K 5% 1/20W TK 0201
RF930 100K 1% 1/20W TK 0201
P0V855_ATC01_AGND 89
P0V855_ATC01_PGOOD 89
P0V855_ATC01_COMP_FSET
UF930 TPS628502 SOT583 353S02660
VIN EN MODE_SYNC PG COMP_FSET GND SW FB
CRITICAL LF930 0.47UH-3.7A-0.034OHM PIJD16140H-SM 152S00984
DIDT=TRUE SWITCH_NODE=TRUE MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000
P0V855_ATC01_SW P0V855_ATC01_REG_XW
VOLTAGE=0.88V MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000
XWF934 SM NO_XNET_CONNECTION=1
XWF933 SM NO_XNET_CONNECTION=1
P0V855_ATC01_FB_RC
RF940 3.16K 1% 1/20W TK 0201
131S00090 CF936 100PF 5% 50V C0G 0201
P0V855_ATC01_AGND 89
P0V855_ATC01_FB_TOP_R
P0V855_ATC01_FB_R
RF937 10K 0.1% 1/20W TK 0201
RF936 1.96K 1% 1/20W TK 0201
CF931 3300PF 10% 10V X7R-CERM 0201
P0V855_ATC01_FB_TOP
RF935 10 5% 1/20W TK 0201
XWF930 SM VOLTAGE=0V NO_XNET_CONNECTION=1 PLACE_NEAR=UF930.8:2MM
P0V855_ATC01_FB

PACK_OPTION=ATC_VR_DSCHG-EN-R:NO
RF945 0 0% 1/20W TK 0201
ATC01_VDDCIO_VR_EN 89 87 IN MAKE_BASE=TRUE
PACK_IGNORE=TRUE PACK_OPTION=ATC_VR_DSCHG-EN-R:YES
ATC01_VDDCIO_VR_EN
CRITICAL QF940 SSM6N37FEAP SOT563 376S00078
RF944 100K 5% 1/20W TK 0201 117S00095
CF959 4700PF 10% 25V 0201-1 CER-X5R
ATC01_P0V855_DSCHG_EN_RC
PP3V8_AON 150 89
PP0V855_ATCRTMR01_VDD_CIO 98 89 82
RF941 10 5% 1/5W TK 0402
RF942 10 5% 1/5W TK 0402
RF943 10 5% 1/5W TK 0402
P0V855_ATC01_DSCHG
CRITICAL QF940 SSM6N37FEAP SOT563 376S00078

VOUT = 0.8621V
IOUT MAX = 0.5A
F = 1.8 MHZ

PP1V2_ATCRTMR01_VDDIO 82 89 98
NOSTUFF
RF964 4.7K 5% 1/20W TK 0201
P0V805_ATC01_PGOOD 89
PACK_OPTION=ATC_VR_PG-RES

PP3V8_ATC01_LDO 151
XWF961 SM NO_XNET_CONNECTION=1
XWF962 SM PLACE_NEAR=UF960.8:2MM NO_XNET_CONNECTION=1
PACK_IGNORE=TRUE PACK_OPTION=ATC01_VR_MLCC-COMBO
VOLTAGE=3.8V MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000
PP3V8_ATC01_VDDFIXED_REG
PACK_OPTION=ATC01_VR_MLCC-REGULAR
CRITICAL CF962 CF963 CF964 CF965 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL CF962 CF963 CF964 CF965 10UF 20% 6.3V CER-X6S 0402
P0V805_ATC01_SVR_PGND VOLTAGE=0V MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000

PACK_IGNORE=TRUE PACK_OPTION=ATC01_VR_MLCC-COMBO
PP0V805_ATCRTMR01_VDD_FIXED
CRITICAL CF968 CF969 CF970 CF971 CF972 CF973 CF974 CF975 CF976 CF977 CF978 CF979 CF980 CF981 10UF 20% 6.3V CER-X6S 0402-COMBO 89 98
CRITICAL CF968 CF969 CF970 CF971 CF972 CF973 CF974 CF975 CF976 CF977 CF978 CF979 CF980 CF981 10UF 20% 6.3V CER-X6S 0402
PACK_OPTION=ATC01_VR_MLCC-REGULAR

ATC01_VDDFIXED_VR_EN 144 89 87 IN
RF969 0 0% 1/20W TK 0201
RF961 100K 5% 1/20W TK 0201
RF960 100K 1% 1/20W TK 0201
P0V805_ATC01_AGND 89
P0V805_ATC01_PGOOD 89
P0V805_ATC01_COMP_FSET
UF960 TPS628502 SOT583 353S02660
VIN EN MODE_SYNC PG COMP_FSET GND SW FB
CRITICAL LF960 0.47UH-3.7A-0.034OHM PIJD16140H-SM 152S00984
DIDT=TRUE SWITCH_NODE=TRUE MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000
P0V805_ATC01_SW P0V805_ATC01_REG_XW
VOLTAGE=0.805V MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000
XWF964 SM NO_XNET_CONNECTION=1
XWF963 SM NO_XNET_CONNECTION=1
P0V805_ATC01_FB_RC
RF970 3.16K 1% 1/20W TK 0201
131S00090 CF966 100PF 5% 50V C0G 0201
P0V805_ATC01_AGND 89
P0V805_ATC01_FB_TOP_R
P0V805_ATC01_FB_R
RF967 10K 0.1% 1/20W TK 0201
RF966 665 1% 1/20W TK 0201
CF961 3300PF 10% 10V X7R-CERM 0201
P0V805_ATC01_FB_TOP
RF965 10 5% 1/20W TK 0201
XWF960 SM VOLTAGE=0V NO_XNET_CONNECTION=1 PLACE_NEAR=UF960.8:2MM
P0V805_ATC01_FB

PACK_OPTION=ATC_VR_DSCHG-EN-R:NO
RF975 0 0% 1/20W TK 0201
ATC01_VDDFIXED_VR_EN 144 89 87 IN MAKE_BASE=TRUE
PACK_IGNORE=TRUE PACK_OPTION=ATC_VR_DSCHG-EN-R:YES
ATC01_VDDFIXED_VR_EN
CRITICAL QF960 SSM6N37FEAP SOT563 376S00078
RF974 100K 5% 1/20W TK 0201 117S00095
NOSTUFF CF989 47PF 20% 6V 0201 CGB
ATC01_P0V805_DSCHG_EN_RC
PACK_IGNORE=TRUE PACK_OPTION=ATC_VR_MLCC-DSCHG
PP3V8_AON 150 89
PP0V805_ATCRTMR01_VDD_FIXED 98 89
RF971 10 5% 1/5W TK 0402
RF972 10 5% 1/5W TK 0402
RF973 10 5% 1/5W TK 0402
P0V805_ATC01_DSCHG
CRITICAL QF960 SSM6N37FEAP SOT563 376S00078

VOUT = 8073V
IOUT MAX = 0.7A
F = 1.8 MHZ

BOM_COST_GROUP=TBT

PAGE TITLE
USB-C: ATC01 REGULATORS

Apple Inc.

DRAWING NUMBER 051-08286 SIZE D
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*** OK2INTEGRATE ***

No lane swapping is allowed
Re-timer to SOC connections are set

USBC HIGH-SPEED AC COUPLING

PP1V2_S2

RG062 1.5K 1% 1/20W 0201 — I2C_UPC2_ATCRTMR2_SCL
RG063 1.5K 1% 1/20W 0201 — I2C_UPC2_ATCRTMR2_SDA
RG043 47K 5% 1/20W 0201 — CIO_ATC2_LSTX
RG044 47K 5% 1/20W 0201 — CIO_ATC2_LSRX

ATCRTMR2_CFP_RCAL_NEG
CG011 10PF 5% 25V C0G 0201
RG011 200 1% 1/20W 0201
ATCRTMR2_CFP_RCAL_POS

ATCRTMR2_SFP_RCAL_NEG
CG010 10PF 5% 25V C0G 0201
RG010 200 1% 1/20W TK 0201-1
ATCRTMR2_SFP_RCAL_POS

ATCRTMR2_XTAL24M_OUT
RG060 499 1% 1/20W TK 0201
197S0591 CRITICAL YG000 1.60X1.20MM 24.000MHZ-20PPM-9.5PF-60OHM
ATC2_24M_O_R
CRITICAL CG060 15PF 5% 50V C0G 0201
CRITICAL 131S0831 CG061 15PF 5% 50V C0G 0201
ATCRTMR2_XTAL24M_IN

PP0V855_ATCRTMR2_VDD_CIO
CG030 14UF 20% 4V X5R 0402-D2X-1
CG031 14UF 20% 4V X5R 0402-D2X-1
138S00149
CG032 0.1UF 10% 6.3V X6S 0201
CG033 0.1UF 10% 6.3V X6S 0201

PP0V805_ATCRTMR2_VDD_FIXED
CG040 0.1UF 10% 6.3V X6S 0201
CG041 0.1UF 10% 6.3V X6S 0201
CG042 2.2UF 20% 4V X6S-CERM 0201
CG043 2.2UF 20% 4V X6S-CERM 0201
CG044 2.2UF 20% 4V X6S-CERM 0201
CG045 14UF 20% 4V X5R 0402-D2X-1
CG046 14UF 20% 4V X5R 0402-D2X-1

PP0V805_ATCRTMR2_VDD_FIXED
CG050 0.1UF 10% 6.3V X6S 0201
PLACE_NEAR=UG000.G7:5MM

PPVDD_FIXED_ATCRTMR2_XTAL_R
RG051 10 5% 1/20W TK 0201 VOLTAGE=0.805V
PP0V805_ATCRTMR2_VDD_FIXED
CG051 4UF 20% 2.5V X6S 0201
117S00094
138S00329

UG000 TMNB25B1-K1S1 FCCSP 338S00888 SYM 2 OF 2 OMIT_TABLE CRITICAL

J4	VDD_CIO_0	VDDIO12_CIO_0	K5
J6	VDD_CIO_0	VDDIO12_CIO_0	K7
J8	VDD_CIO_0	VDDIO12_CIO_0	L6
F4	VDD_CIO_1	VDDIO12_CIO_1	D6
F6	VDD_CIO_1	VDDIO12_CIO_1	E5
F8	VDD_CIO_1	VDDIO12_CIO_1	E7
G4	VDD_FIXED	VDDIO12_PLL_SOC0	K8
G5	VDD_FIXED	VDDIO12_PLL_SOC1	H8
H5	VDD_FIXED	VDDIO12_XTAL	H9
H6	VDD_FIXED	VDDIO12	E9
G7	VDD_FIXED_PLL	VDDIO12	H3
G9	VDD_FIXED_XTAL	VDDIO12	K9
		VDDIO12_EFUSE1	F3
		VDDIO12_AMUX	F7

VSS: A1 A2 A4 A6 A8 A10 A11 B2 B4 B6 B8 B10 C3 C5 C6 C7 C9 D1 D5 D7 D11 E3 E4 E6 E8 F2 F5 F10 G3 G6 G8 | H4 H7 J2 J3 J5 J7 J10 K4 K6 L1 L5 L7 L11 M3 M5 M6 M7 M9 N2 N4 N6 N8 N10 P1 P2 P4 P6 P8 P10 P11

PP1V2_ATCRTMR2_VDDIO
132S0395 CG034 0.1UF 10% 6.3V X6S 0201
138S00039 CG035 2.2UF 20% 4V X6S-CERM 0201
CG036 14UF 20% 4V X5R 0402-D2X-1
CG037 14UF 20% 4V X5R 0402-D2X-1

PP1V2_ATCRTMR2_VDDIO
138S00039 CG052 2.2UF 20% 4V X6S-CERM 0201
PLACE_NEAR=UG000.K8:5MM

PP1V2_ATCRTMR2_VDDIO_XTAL_F
155S0644 FLG000 240-OHM-0.2A-0.9-OHM 0201
VOLTAGE=1.2V
CG063 2.2UF 20% 4V X6S-CERM 0201
CG062 0.1UF 10% 6.3V X6S 0201
138S00039
132S0395
PP1V2_ATCRTMR2_VDDIO

Connect to GND directly or via a resistor
GND

PP1V2_ATCRTMR2_VDDIO
132S0395 CG064 0.1UF 10% 6.3V X6S 0201

PACK_OPTION=ATC_BOUNDARYSCAN:YES
RG045 47K 5% 1/20W TK 0201
ATCRTMR2_JTAG_TDO
PACK_OPTION=ATC_BOUNDARYSCAN:NO
RG047 47K 5% 1/20W TK 0201
ATCRTMR2_JTAG_SEL
PACK_OPTION=ATC_BOUNDARYSCAN:YES
RG040 10K 5% 1/20W TK 0201
ATCRTMR2_TESTMODE
PACK_OPTION=ATC_BOUNDARYSCAN:NO

UG000 TMNB25B1-K1S1 FCCSP OMIT_TABLE CRITICAL 338S00888 SYM 1 OF 2

USBC_ATC2_D2R_C_P<1>	P9	SFP_PHY_RXTX_0_P	SFP PHY	CFP PHY	A9	USBC2_R2D_CR_P<1>
USBC_ATC2_D2R_C_N<1>	N9	SFP_PHY_RXTX_0_N			B9	USBC2_R2D_CR_N<1>
USBC_ATC2_D2R_C_P<2>	P5	SFP_PHY_RXTX_2_P			A5	USBC2_R2D_CR_P<2>
USBC_ATC2_D2R_C_N<2>	N5	SFP_PHY_RXTX_2_N			B5	USBC2_R2D_CR_N<2>
USBC_ATC2_R2D_P<1>	P7	SFP_PHY_RXTX_1_P			A7	USBC2_D2R_P<1>
USBC_ATC2_R2D_N<1>	N7	SFP_PHY_RXTX_1_N			B7	USBC2_D2R_N<1>
USBC_ATC2_R2D_P<2>	P3	SFP_PHY_RXTX_3_P			A3	USBC2_D2R_P<2>
USBC_ATC2_R2D_N<2>	N3	SFP_PHY_RXTX_3_N			B3	USBC2_D2R_N<2>
USBC_ATC2_AUX_C_P	L4	SFP_LPDP_AUX_P			D4	USBC2_AUX_P
USBC_ATC2_AUX_C_N	M4	SFP_LPDP_AUX_N			C4	USBC2_AUX_N
CIO_ATC2_LSTX	G1	USB4_SFP_SB_RX			F1	USBC2_CIO_LSRX
CIO_ATC2_LSRX	G2	USB4_SFP_SB_TX			E1	USBC2_CIO_LSTX
					H1	ATCRTMR2_LSTX_DIR
ATCRTMR2_SFP_RCAL_POS	M8	SFP_PHY_RCAL_P			C8	ATCRTMR2_CFP_RCAL_POS
ATCRTMR2_SFP_RCAL_NEG	L8	SFP_PHY_RCAL_N			D8	ATCRTMR2_CFP_RCAL_NEG
GND	M1	CHIP_ID_0	GPIO	PERIPHERAL	N11	SPI_ATCRTMR2_CS_L
ATCRTMR2_CHIPID_1	N1	CHIP_ID_1			M11	SPI_ATCRTMR2_CLK
ATCRTMR2_BOOT_CONFIG0	H2	BOOT_CONFIG0			K10	SPI_ATCRTMR2_DIO<0>
ATCRTMR2_BOOT_CONFIG1	J1	BOOT_CONFIG1			K11	SPI_ATCRTMR2_DIO<1>
ATCRTMR2_BOOT_CONFIG2	K1	BOOT_CONFIG2			J9	SPI_ATCRTMR2_DIO<2>
ATCRTMR2_FORCE_DFU	C1	FORCE_DFU			J11	SPI_ATCRTMR2_DIO<3>
TP_ATCRTMR2_GPIO0	K2	GPIO0			C2	I2C_ATCRTMR_SCL
NC_ATCRTMR2_GPIO1 NO_TEST=1	L3	GPIO1			D3	I2C_ATCRTMR_SDA
TP_ATCRTMR2_GPIO2	K3	GPIO2			E2	I2C_UPC2_ATCRTMR2_SCL
TP_ATCRTMR2_GPIO3	L10	GPIO3			D2	I2C_UPC2_ATCRTMR2_SDA
					B1	UPC2_ATCRTMR2_I2C_INT_L
ATCRTMR2_RESET_L	L2	COLD_RESET*	CLOCKS AND RESET	TEST AND DEBUG	L9	ATCRTMR2_TESTMODE
	M2	CFSB			C11	ATCRTMR2_JTAG_SEL
ATCRTMR2_XTAL24M_IN	F11	XI0			B11	SWD_NUB_ATCRTMR2_SWCLK
ATCRTMR2_XTAL24M_OUT	E11	XO0			D10	SWD_NUB_ATCRTMR2_SWDIO
					D9	TP_ATCRTMR2_JTAG_TDI
					C10	ATCRTMR2_JTAG_TDO
					E10	TP_ATCRTMR2_JTAG_TRESET
					F9	TP_ATCRTMR2_ANALOGMUX_OUT
					M10	TP_ATCRTMR2_TST_CLKOUT
		TST_CLK_LVDS_0_P			H10	NC_ATCRTMR2_CLK_LVDSP<0> NO_TEST=1
		TST_CLK_LVDS_0_N			H11	NC_ATCRTMR2_CLK_LVDSN<0> NO_TEST=1
		TST_CLK_LVDS_1_P			G11	NC_ATCRTMR2_CLK_LVDSP<1> NO_TEST=1
		TST_CLK_LVDS_1_N			G10	NC_ATCRTMR2_CLK_LVDSN<1> NO_TEST=1

RG097 33 1/20W 5% TK 0201 — SPI_ATCRTMR2_DIO<0> — SPI_ATCRTMR2_R_DIO<0>
RG098 33 1/20W 5% TK 0201 — SPI_ATCRTMR2_DIO<1> — SPI_ATCRTMR2_R_DIO<1>

PP1V2_ATCRTMR2_VDDIO
RG090 3.3K 5% 1/20W TK 0201
NOSTUFF RG091 3.3K 5% 1/20W TK 0201
RG092 3.3K 5% 1/20W TK 0201
NOSTUFF RG093 3.3K 5% 1/20W TK 0201
CG090 1.0UF 20% 6.3V X5R 0201-1

UG090 64MBIT-1.2V W25Q64NE XSON-1 OMIT_TABLE CRITICAL 335S00574

SPI_ATCRTMR2_CLK	RG094 33	SPI_ATCRTMR2_CLK_R	6 CLK
SPI_ATCRTMR2_CS_L		SPI_ATCRTMR2_CS_L	1 CS*
SPI_ATCRTMR2_DIO<2>	RG095 33	SPI_ATCRTMR2_R_DIO<2>	3 WP*(IO2)
SPI_ATCRTMR2_DIO<3>	RG096 33	SPI_ATCRTMR2_R_DIO<3>	7 HOLD*(IO3)
		SPI_ATCRTMR2_R_DIO<0>	5 DI(IO0)
		SPI_ATCRTMR2_R_DIO<1>	2 DO(IO1)
		GND	4
		EPAD	9

PACK_OPTION=ATC_RTMR_ROM:XSON

PP1V2_ATCRTMR2_VDDIO

UG090 64MBIT-1.2V GD25UF64E WLCSP-COMBO VCC CRITICAL

SPI_ATCRTMR2_CLK_R	D2	SCLK	SI(IO0) E2 SPI_ATCRTMR2_R_DIO<0>
SPI_ATCRTMR2_CS_L	B3	CS*	SO(IO1) C3 SPI_ATCRTMR2_R_DIO<1>
SPI_ATCRTMR2_R_DIO<2>	D3	IO2	NC A2 NC
SPI_ATCRTMR2_R_DIO<3>	C2	IO3	NC A3 NC
		OMIT_TABLE 335S00638	NC F2 NC
			NC F3 NC
		VSS E3	

PACK_IGNORE=TRUE
PACK_OPTION=ATC_RTMR_ROM:WLCSP

BOM_COST_GROUP=TBT

PAGE TITLE: USB-C: High Speed ATC2

Apple Inc.

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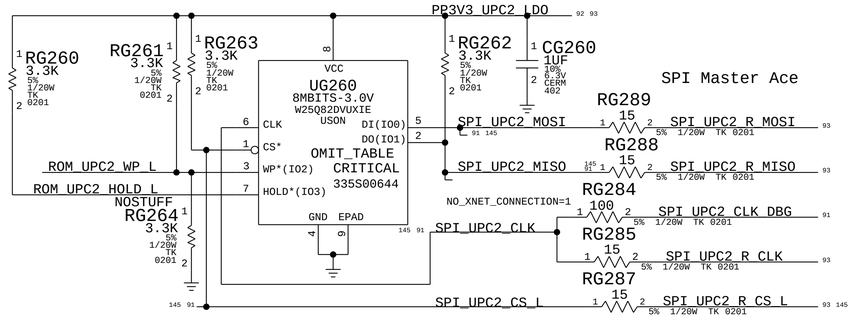
*** OK2INTEGRATE ***

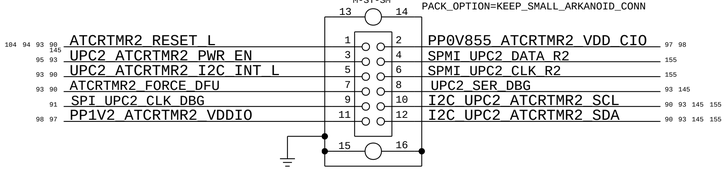


ACE ARKANOID CONN

JG200

USBC_DBG 505070-1222 M-ST-SM

PACK_OPTION=KEEP_SMALL_ARKANOID_CONN

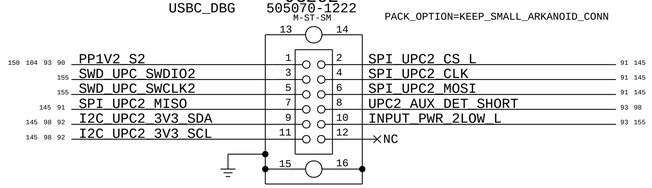


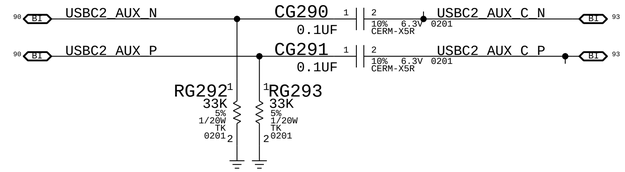
AARDVARKANOID CONN

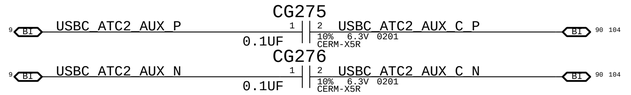
JG202

USBC_DBG 505070-1222 M-ST-SM

PACK_OPTION=KEEP_SMALL_ARKANOID_CONN







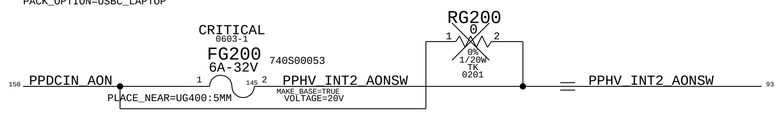
HV POWER ALIASES

Fuses for laptop charging.

PACK_OPTION=USBC_LAPTOP

PACK_IGNORE=TRUE
PACK_OPTION=USBC_DESKTOP

Desktops only need connection for programming OTP.



BOM_COST_GROUP=USB-C

PAGE TITLE: USB-C: Support 1 ATC2

Apple Inc.

DRAWING NUMBER: 051-08286 SIZE: D

REVISION: 5.0.3

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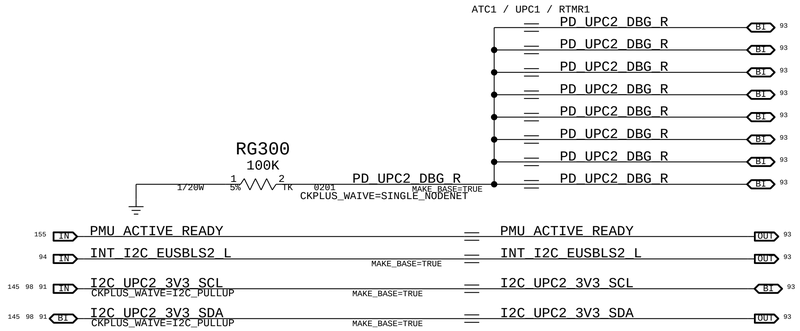
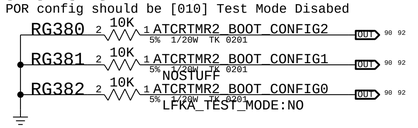
*** OK2INTEGRATE ***

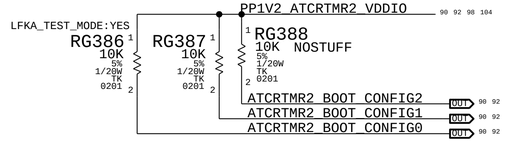
UPC 2 GPIOs



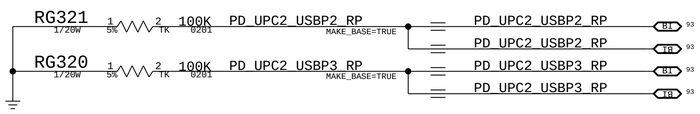
ATCRTMR Boot Config

[2:0] = [011] 30Mhz QSPI and Test Mode Enabled
POR config should be [010] Test Mode Disabed

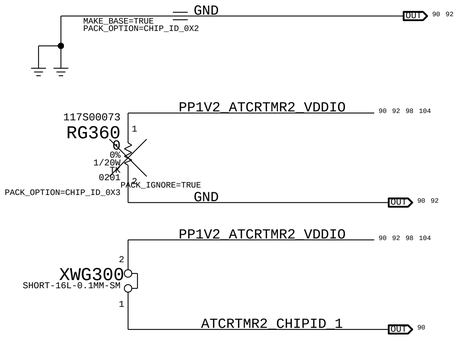




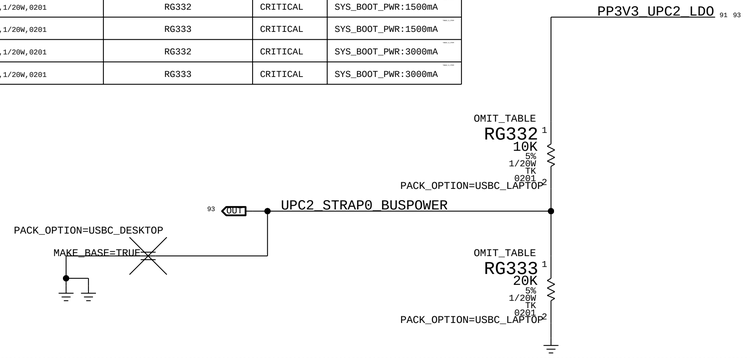
Unused ports



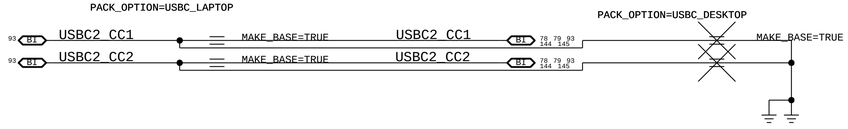
ATCRTMR2 CHIP 0X02/0X03



STAP0/BUSPOWER

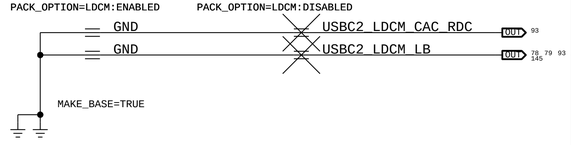


Connections for Laptops (USBC power in)



Connections for Desktops (No USBC power in)

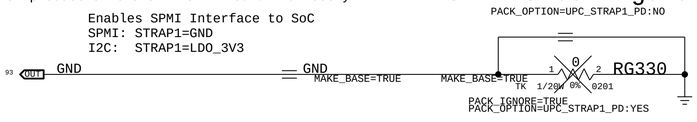
LDCM



STRAPS Configurations

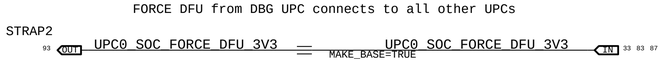
For production tie SPMI STRAP to GND directly

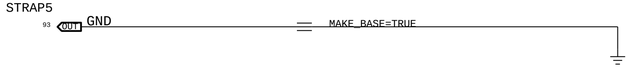
Enables SPMI Interface to SoC
SPMI: STRAP1=GND
I2C: STRAP1=LDO_3V3

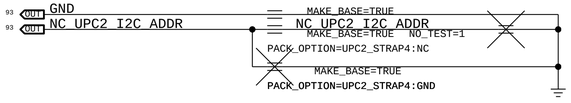


UPC0: STRAP3=GND STRAP4=GND
UPC1: STRAP3=NC STRAP4=GND
UPC2: STRAP3=GND STRAP4=NC (LEGACY) GND (CURRENT)
UPC5: STRAP3=NC STRAP4=140K

FORCE DFU from DBG UPC connects to all other UPCs







Is UPCx_5V_EN being used?

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
117S00073	1	RES,TK,0 OHM, 1A MAX,1/20W,0201	RG332	CRITICAL	SYS_BOOT_PWR:DEFAULT_500mA
117S00073	1	RES,TK,0 OHM, 1A MAX,1/20W,0201	RG333	CRITICAL	SYS_BOOT_PWR:DISABLED
117S00131	1	RES,TK,51K OHM,5%,1/20W,0201	RG332	CRITICAL	SYS_BOOT_PWR:1000mA
117S00090	1	RES,TK,10K OHM,5%,1/20W,0201	RG333	CRITICAL	SYS_BOOT_PWR:1000mA
117S00098	1	RES,TK,20K OHM,5%,1/20W,0201	RG332	CRITICAL	SYS_BOOT_PWR:1500mA
117S00090	1	RES,TK,10K OHM,5%,1/20W,0201	RG333	CRITICAL	SYS_BOOT_PWR:1500mA
117S00090	1	RES,TK,10K OHM,5%,1/20W,0201	RG332	CRITICAL	SYS_BOOT_PWR:3000mA
117S00131	1	RES,TK,51K OHM,5%,1/20W,0201	RG333	CRITICAL	SYS_BOOT_PWR:3000mA

BOM_COST_GROUP=USB-C

PAGE TITLE: USB-C: Support 2 ATC2

Apple Inc.

DRAWING NUMBER: 051-08286 SIZE: D
REVISION: 5.0.3
BRANCH:
PAGE: 163 OF 700
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*** OK2INTEGRATE ***

MAX 100uF TOTAL ON RAIL

91 PPHV_INT2_AONSW

151 PP5V_S2SW_USBC23
151 PP5V_S2SW_USBC23

138S00123 CG406 10UF 20% 10V X5R 0402

PP_5V0 PP_CABLE PP_HV VBUS

OMIT_TABLE
UG400
SN20120024
BGA

POWER

DIGITAL CORE I/O & CONTROL

TYPE-C

PORT MUX

	M22	HRESET		
93 PD_UPC2_MRESET	H18	GPIO14_MRESET		
145 104 94 91 90 OUT ATCRTMR2_RESET_L	B4	GPIO15_RESETZ		
145 91 OUT UPC2_SER_DBG	F26	GPIO0		
92 IN PMU_ACTIVE_READY	D18	GPIO1		
92 IN PD_UPC2_GPIO2	K24	GPIO2		
92 OUT PD_UPC2_GPIO3	L21	GPIO3	PU	
92 OUT PD_UPC2_GPIO4	J25	GPIO4		
92 OUT PD_UPC2_GPIO5	J9	GPIO5		
92 IN PD_UPC2_GPIO6	C1	GPIO6		
145 96 92 OUT UPC23_5V_EN	C5	GPIO7		
91 90 OUT ATCRTMR2_FORCE_DFU	F10	GPIO8		
91 90 OUT UPC2_ATCRTMR2_I2C_INT_L	H10	GPIO9	PU	
92 IN INT_I2C_EUSBLS2_L	A3	GPIO10	PU	
92 BI PD_UPC2_GPIO11	L25	GPIO11		
155 91 OUT INPUT_PWR_2L0W_L	E11	GPIO12	PU	
92 OUT PD_UPC2_GPIO16	M26	GPIO16_DFU_BOOTED_L		
155 OUT UPC_PMU_RESET_1V2	G19	GPIO17_FORCE_RST_REQ		
90 BI USBC2_CIO_LSTX	L13	GPIO18_LSTXRX		
90 OUT USBC2_CIO_LSRX	C3	GPIO19_LSRX		
98 91 OUT UPC2_AUX_DET_SHORT	N23	GPIO20_SS_HOLD		
90 IN ATCRTMR2_LSTX_DIR	G25	GPIO21_LSX_DIR		
92 UPC2_STRAP0_BUSPOWER	J17	STRAP0_BUSPOWER		
92 GND	L27	STRAP1_I2C_SPMI_SEL		
92 IN UPC0_SOC_FORCE_DFU_3V3	J13	STRAP2_DFU_EN		
92 GND	M20	STRAP3_I2C_ADDR0		
92 NC_UPC2_I2C_ADDR	N21	STRAP4_I2C_ADDR1		
92 GND	J21	STRAP5_VDDIO_CFG		
UPC2_R_OSC	B10	R_OSC		
NC_UPC2_AID0 NO_TEST=1	F14	AID0		
NC_UPC2_AID1 NO_TEST=1	G15	AID1		
NC_UPC2_AID2 NO_TEST=1	H14	AID2		
NC_UPC2_AID3 NO_TEST=1	E15	AID3		
155 145 91 90 BI I2C_UPC2_ATCRTMR2_SDA	A25	I2C0_SDA		
155 145 91 90 BI I2C_UPC2_ATCRTMR2_SCL	B26	I2C0_SCL		
92 BI I2C_UPC2_3V3_SDA	K28	I2C1_SDA_GPIO23		
92 IN I2C_UPC2_3V3_SCL	J27	I2C1_SCL_GPIO22		
NC_INT_I2C_UPC2_L NO_TEST=1	H26	I2C_IRQ1Z		
Configurable as SPMI or I2C Port 2 SMC_SPMI: 0X9 AP_SPMI: 0X8 I2C: 0X3B				
155 BI SPMI_UPC2_DATA	N25	SPMI_I2C2_DATA		
155 IN SPMI_UPC2_CLK	M24	SPMI_I2C2_CLK		
NC_INT_I2C_SMC_UPC2_L NO_TEST=1	K26	I2C_IRQ2Z		
91 OUT SPI_UPC2_R_CLK	G27	SPI_CLK		
91 OUT SPI_UPC2_R_MOSI	H28	SPI_COPI		
91 IN SPI_UPC2_R_MISO	F28	SPI_CIPO		
145 91 OUT SPI_UPC2_R_CS_L	E27	SPI_CSZ		
155 12 BI SWD_UPC_SWDIO2	E25	SWD_DATA	IPU	
155 12 BI SWD_UPC_SWCLK2	E23	SWD_CLK	IPU	
93 92 IN UART_UPC2_RX_TX_PD	D28	UART_RX		
92 OUT UART_UPC2_RX_TX_PD	C27	UART_TX		
98 BI USB2_UPC2_P1_P	A15	USB_RP1_P		
98 BI USB2_UPC2_P1_N	B16	USB_RP1_N		
92 BI PD_UPC2_USBP2_RP	A17	USB_RP2_P		
92 BI PD_UPC2_USBP2_RP	B18	USB_RP2_N		
92 BI PD_UPC2_USBP3_RP	A19	USB_RP3_P		
92 BI PD_UPC2_USBP3_RP	B20	USB_RP3_N		
91 BI USBC2_AUX_C_P	D14	AUX_P		
91 BI USBC2_AUX_C_N	C15	AUX_N		
93 PD_UPC2_HPD	G11	GPIO13_HPDTXRX		
92 BI PD_UPC2_DBG_R	E19	DEBUG0_GPIO24		
92 BI PD_UPC2_DBG_R	F18	DEBUG1_GPIO25		
92 BI PD_UPC2_DBG_R	H22	DEBUG2_GPIO26		
92 BI PD_UPC2_DBG_R	D22	DEBUG3_GPIO27		
92 BI PD_UPC2_DBG_R	G23	DEBUG4_GPIO28		
92 BI PD_UPC2_DBG_R	F22	DEBUG5_GPIO29		
92 BI PD_UPC2_DBG_R	C23	DEBUG6_GPIO30		
92 BI PD_UPC2_DBG_R	D26	DEBUG7_GPIO31		

VIN_3V3	C19		
VDDIO	C25		
LDO_3V3	B22		
LDO_1V8	A23		
VIN_LV	A27		
	B28		
VOUT_LV	B24	UPC2_ATCRTMR2_PWR_EN	91 95
SS	A5	UPC2_SS	
LDO_CORE	A21	PP1V5_UPC2_LDO_CORE	
C_CC1	M16	USBC2_CC1	
	N15		
C_CC2	M18	USBC2_CC2	
	N17		
RPD_G1	L17	USBC2_CC1	BI 92
RPD_G2	L19	USBC2_CC2	BI 92
C_USB_TP	A11	USBC2_USB_TOP_P	BI 78 79
C_USB_TN	A13	USBC2_USB_TOP_N	BI 78 79
C_USB_BP	B12	USBC2_USB_BOT_P	BI 78 79
C_USB_BN	B14	USBC2_USB_BOT_N	BI 78 79
C_SBU1	C11	USBC2_SBU1	BI 78 79 145
C_SBU2	D10	USBC2_SBU2	BI 78 79 145
3V3 LDCM	B8	USBC2_LDCM_CAC_RDC	92
3V3 LDCM_LB	C7	USBC2_LDCM_LB	IN 78 79 92 145
3V3 LDCM_SENSE	A7	USBC2_LDCM_SW	
3V3 LDCM_COMP	B6	USBC2_LDCM_COMP	
3V3 LDCM_SW	A9	USBC2_LDCM_SW	MAKE_BASE=TRUE

PPVBUS_USBC2 78 79 144 145

CG401 1UF 10% 25V X5R 0402

DG400 DSN2 NSR20F40NX_G CRITICAL 371S00085

PP3V3_S2 150

CG400 10UF 20% 6.3V CERM 0402

PP1V2_S2 90 91 104 150

CG402 1.0UF 20% 6.3V X5R 0201-1

MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.0750
VOLTAGE=3.3V

PP3V3_UPC2_LDO 91 92

CG408 10UF 20% 6.3V CERM 0402

MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.0750
VOLTAGE=1.8V

PP1V8_UPC2_LDO

CG417 10UF 20% 6.3V CERM 0402

PP1V8_S2 150

CG403 0.1UF 10% 6.3V CERM-X5R 0201

UPC2_ATCRTMR2_PWR_EN 91 95
(cap needed when used as power source)

VOLTAGE=1.5V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.0750

CG405 10UF 20% 6.3V CERM 0402

PACK_OPTION=ACE2_SS_CAP

CG409 0.68UF 5% 6.3V X6S 0402

PACK_OPTION=ACE2_SS_GND
GND MAKE_BASE=TRUE

MIN_LINE_WIDTH=0.4000
MIN_NECK_WIDTH=0.1500

BI 78 79 92 144 145

MIN_LINE_WIDTH=0.4000
MIN_NECK_WIDTH=0.1500

BI 78 79 92 144 145

CG414 220PF 5% 50V C0G 0201-1

CG413 220PF 5% 50V C0G 0201-1

LDCM circuit subject to change

PACK_OPTION=LDCM:ENABLED

CRITICAL CG420 2.2UF 10% 35V X5R 0402 138S00488

CAC

RDC

PACK_OPTION=LDCM:ENABLED

CRITICAL RG411 402K 1% 1/20W TK 0201 118S00666

PACK_IGNORE=TRUE
PACK_OPTION=LDCM:DISABLED

RG415 10K 1% 1/20W 0201 TK

PACK_OPTION=LDCM:DISABLED

RG414 100K 5% 1/20W TK 0201

PACK_OPTION=LDCM:ENABLED

CRITICAL RG410 R2 4.99K 1/20W 0.1% 0201 TK 103S00656

PACK_OPTION=LDCM:ENABLED

PACK_OPTION=LDCM:ENABLED

CRITICAL RG413 R1 10K 1/20W 0.1% 0201 TK 103S00593

79 78 IN USBC2_LDCM

USBC2_LDCM_R

1M RG405 5% 1/20W TK 0201 UART_UPC2_RX_TX_PD 92 93

100K RG406 5% 1/20W TK 0201 PD_UPC2_MRESET 93

100K RG407 5% 1/20W TK 0201 PD_UPC2_HPD 93

Either a Testpoint or Arkanoid connector must be present for GPIO0 (EVEN IN PRODUCTION)

CRITICAL RG403 15K 0.1% 1/20W TK 0201 103S00582

GROUND

GND

A1 B2 K16 K20 M28 N19 N27

BOM_COST_GROUP=USB-C

PAGE TITLE
USB-C: Port Controller ATC2

Apple Inc.

DRAWING NUMBER 051-08286
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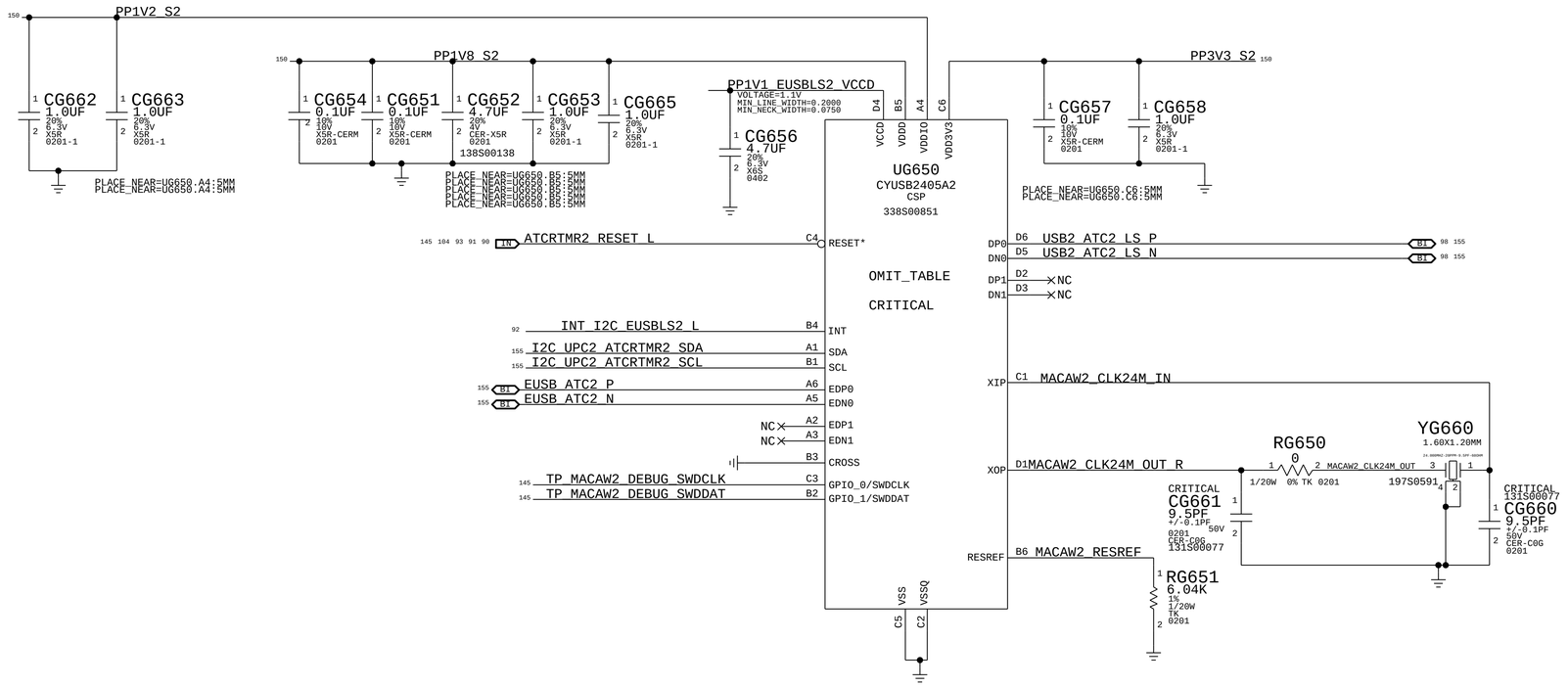
*** OK2INTEGRATE ***

MACAW 2



BOM_COST_GROUP=USB-C

PAGE TITLE: USB-C: USB2 RPT2

Apple Inc.

DRAWING NUMBER: 051-08286 SIZE: D

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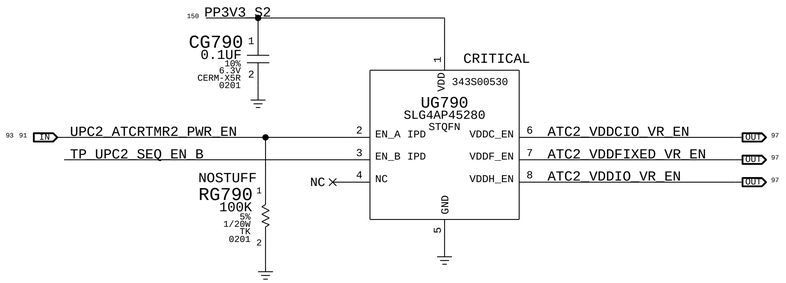
*** OK2INTEGRATE ***

Sequencing Requirements: 3.3V to UG790 --> system 1.2V (UG400 VDDIO) same time or before System 1.8V (UG400 VIN_LV pin)

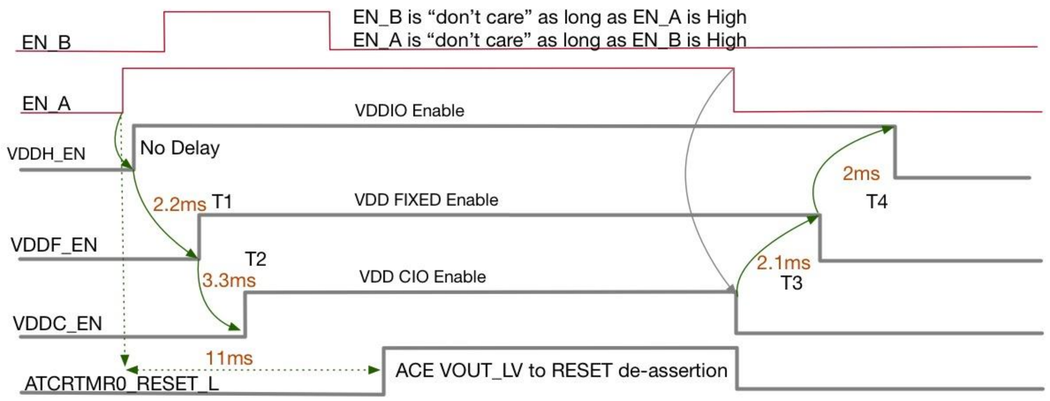
Power-up Sequence Requirements: 3.3_S2 to UG790 --> system 1.2V (UG400 VDDIO) same time or before system 1.8V (UG400) VIN_LV pin)

Power-down Sequence Requirements: The 1.8V first or at the same time as 1V2 --> 3V3_S2 needs to get disabled at minimum of 6ms from when 1V8 is discharged to below 300mV

The 3.3V needs to be HIGH before VIN_LV of Aces



Note1: As long as EN_A or EN_B are High, the outputs stay High
Note2: Outputs are an ORed and delayed version of EN_A or EN_B



BOM_COST_GROUP=USB-C

PAGE TITLE
USB-C: HS Level Shifters ATC2

Apple Inc.

DRAWING NUMBER 051-08286
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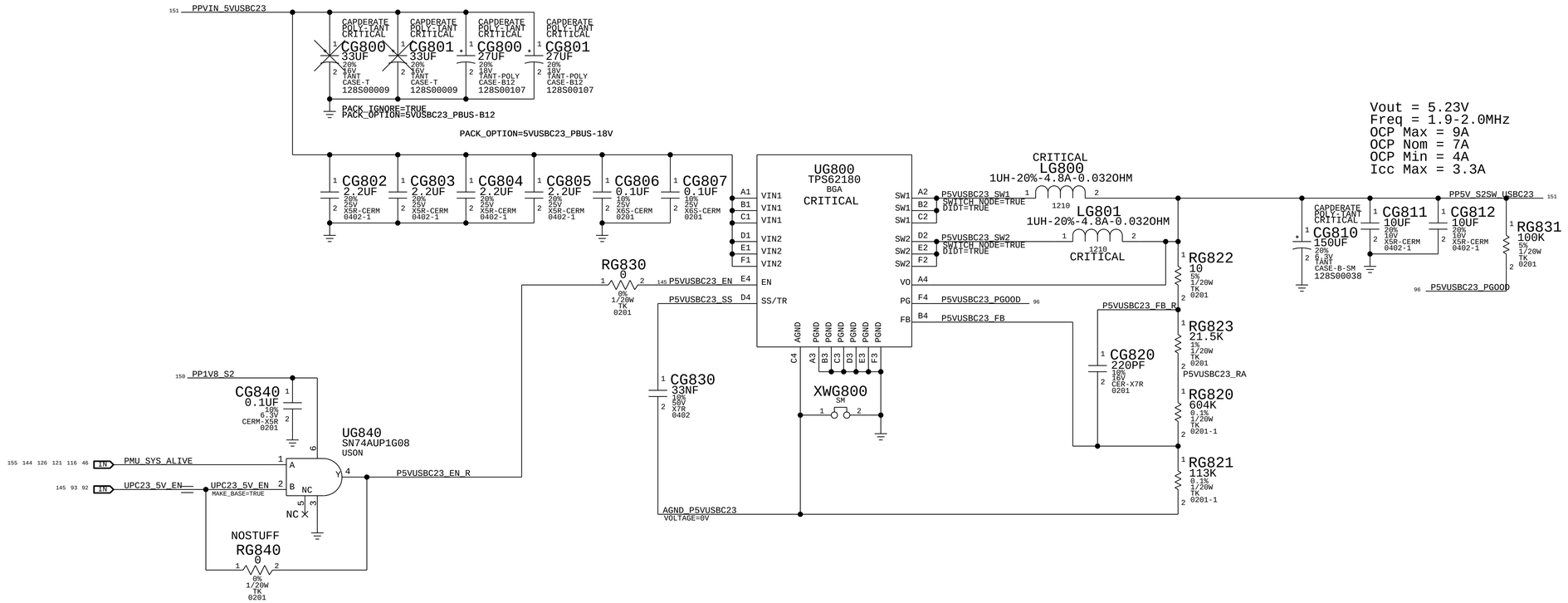
*** OK2INTEGRATE ***

Set one option for the PBUS caps

PACK_OPTION=5VUSBC23_PBUS-B12

PACK_OPTION=5VUSBC23_PBUS-18V



PAGE TITLE	USB-C: 5V Regulator
	Apple Inc.
DRAWING NUMBER	051-08286
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BOM_COST_GROUP=USB-C

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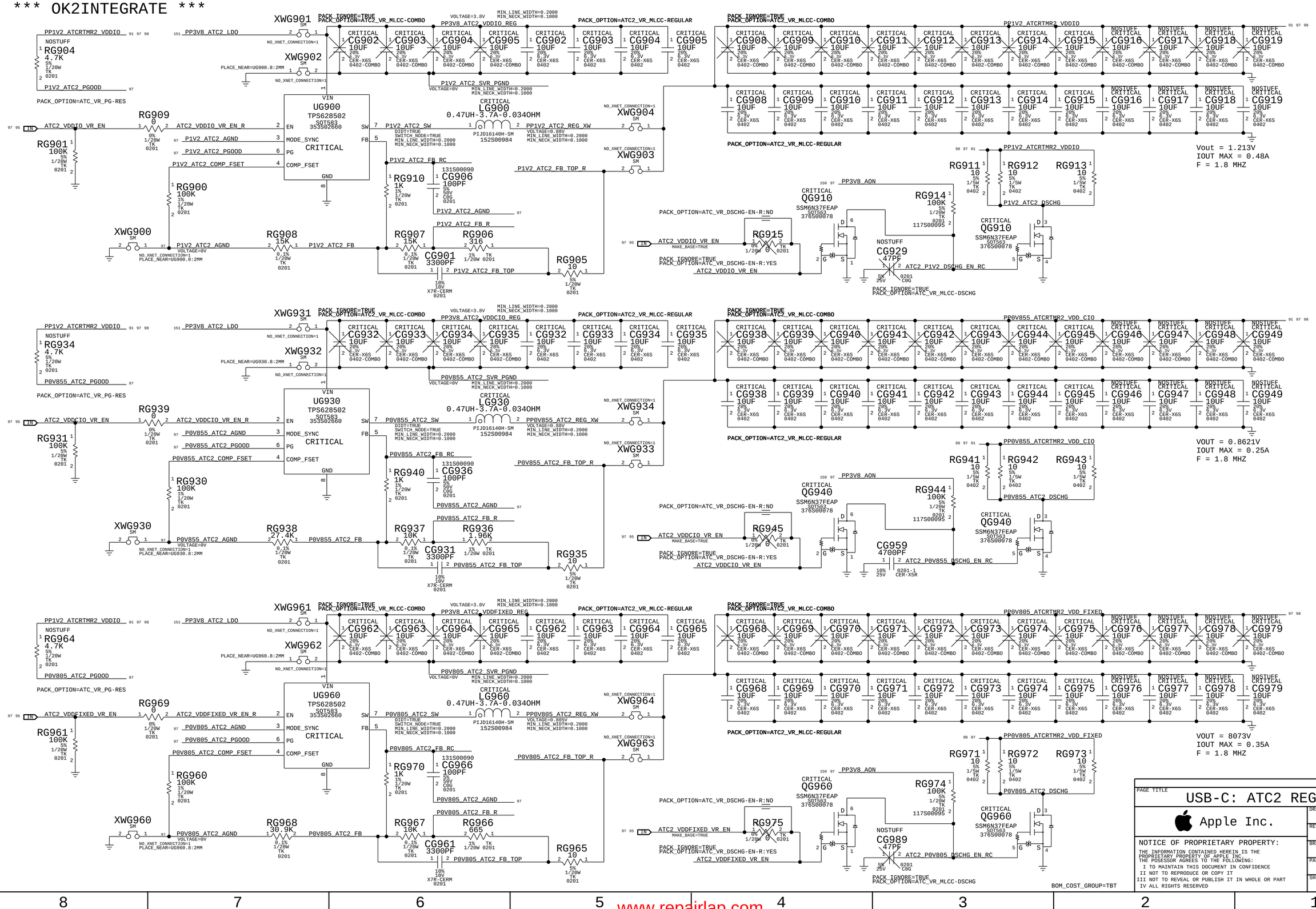

PAGE TITLE

USB-C: ATC2 REGULATORS

Apple Inc.

DRAWING NUMBER	051-08286
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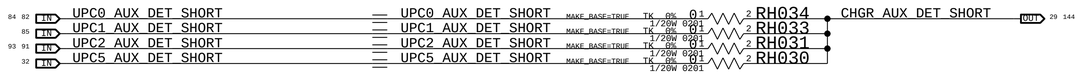
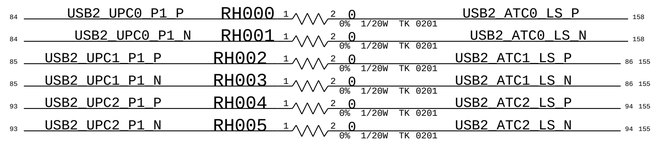
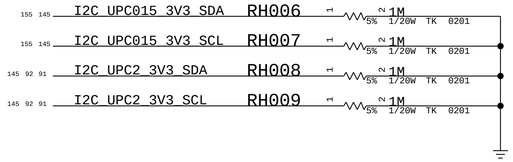
USB Power Signalling

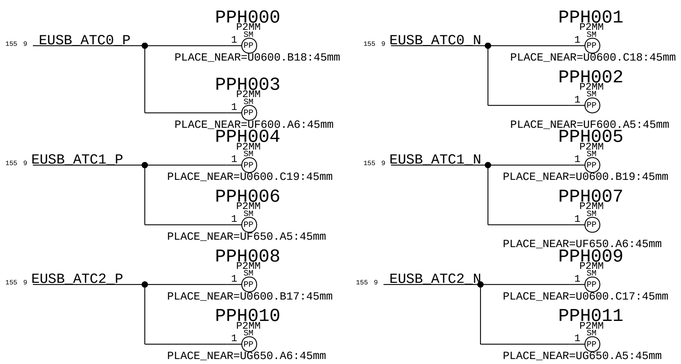


Ace3 USB2 Connections

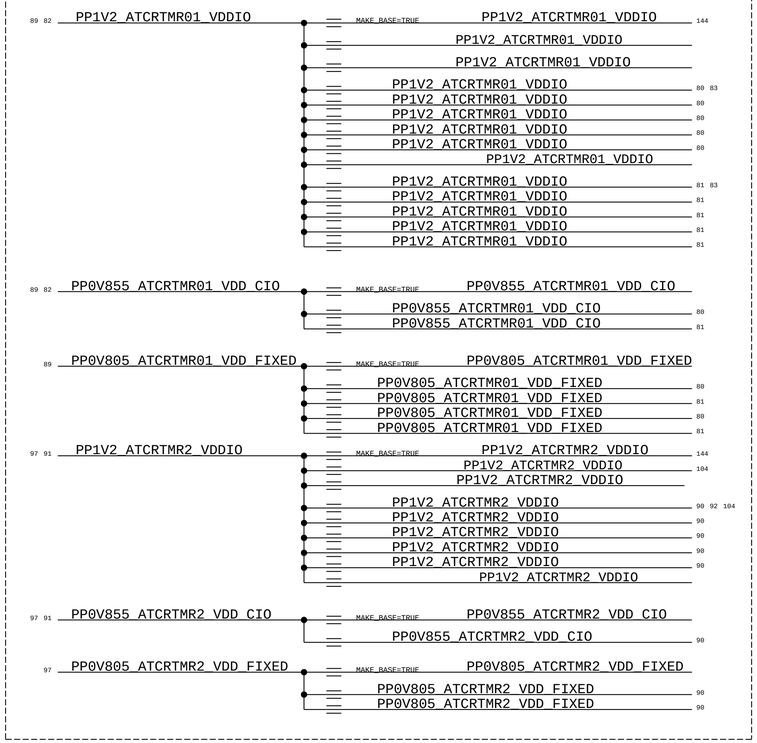




USB2 Probe Points



Lifuka Power



BOM_COST_GROUP=USB-C

PAGE TITLE	USB-C: SUPPORT
	Apple Inc.
DRAWING NUMBER	051-08286
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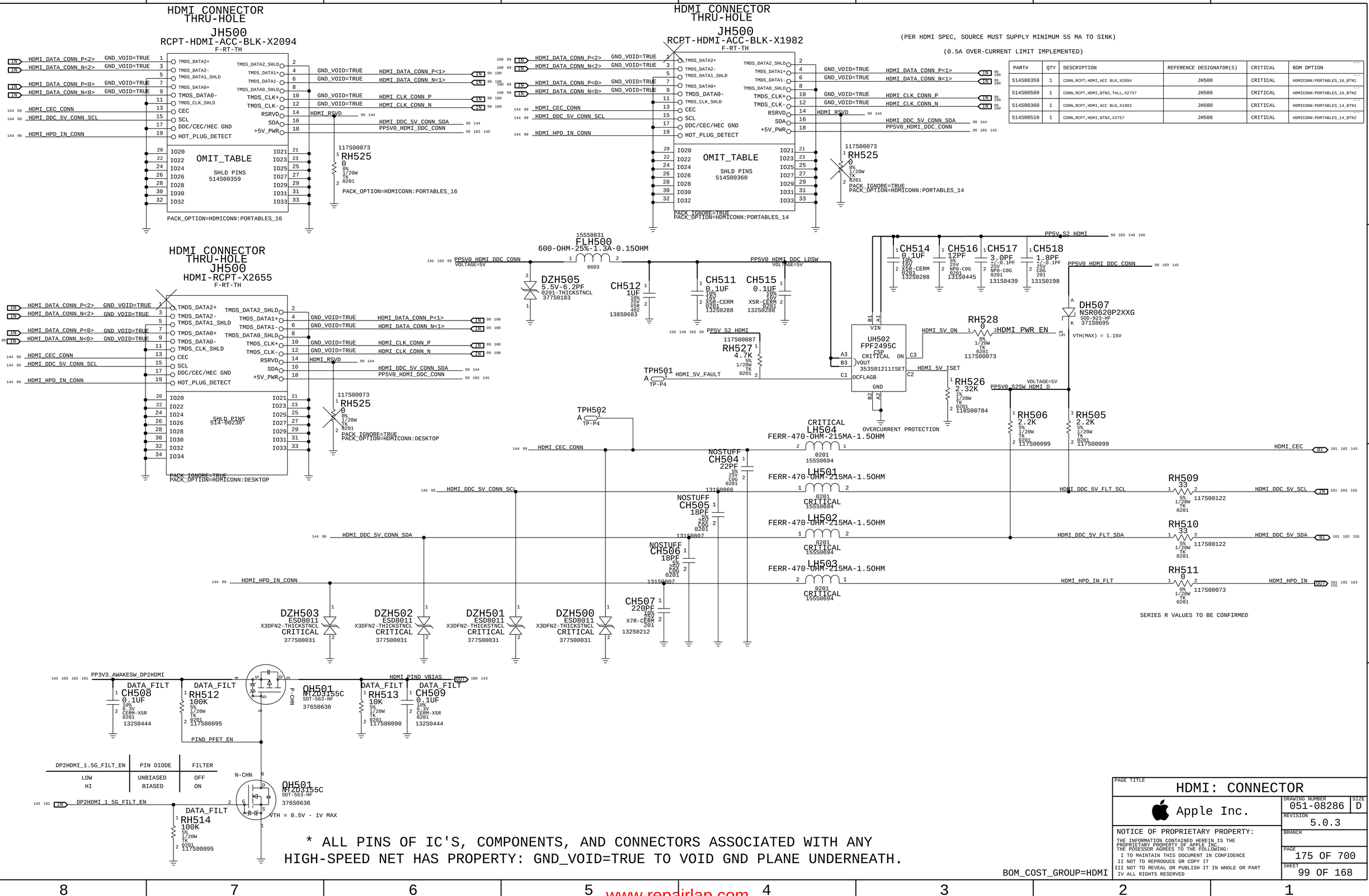

(PER HDMI SPEC, SOURCE MUST SUPPLY MINIMUM 55 MA TO SINK)

(0.5A OVER-CURRENT LIMIT IMPLEMENTED)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514S00359	1	CONN,RCPT,HDMI,ACC BLK,X2094	JH500	CRITICAL	HDMICONN:PORTABLES_16_BTN1
514S00509	1	CONN,RCPT,HDMI,BTN2,TALL,X2757	JH500	CRITICAL	HDMICONN:PORTABLES_16_BTN2
514S00360	1	CONN,RCPT,HDMI,ACC BLK,X1982	JH500	CRITICAL	HDMICONN:PORTABLES_14_BTN1
514S00510	1	CONN,RCPT,HDMI,BTN2,X2757	JH500	CRITICAL	HDMICONN:PORTABLES_14_BTN2

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*** OK2INTEGRATE***

* ALL PINS OF IC'S, COMPONENTS, AND CONNECTORS ASSOCIATED WITH ANY HIGH-SPEED NET HAS PROPERTY: GND_VOID=TRUE TO VOID GND PLANE UNDERNEATH.

8	7	6	5	4	3	2	1

CL FILT

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
152S00850	8	IND,0.5NH,+/-0.1NH,0.85A,0.08OHM,0201	LH600,LH601,LH603,LH604,LH606,LH607,LH609,LH610	HDMI_CL_FILT:YES
117S00073	8	RES,TK,0.0OHM,1,1/20W,0201,HIGHFREQ	LH600,LH601,LH603,LH604,LH606,LH607,LH609,LH610	HDMI_CL_FILT:NO

PAGE TITLE	HDMI: DESENSE FILTERS
	Apple Inc.
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BOM_COST_GROUP=HDMI

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*** IN PROGRESS ***

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S00772	1	IC,COBRA,PS190,DP2 TO HDMI,A0,BGA120	UH700	CRITICAL	COBRA-A0
338S00957	1	IC,COBRA,PS190,DP2 TO HDMI,A1,BGA120	UH700	CRITICAL	COBRA-A1_CGF2
998-29948	1	IC,COBRA,A1,DP TO HDMI CNVTR,DEV,BGA120	UH700	CRITICAL	COBRA-A1_CGF1

BOM_COST_GROUP=HDMI

PAGE TITLE
HDMI: COBRA

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*** IN PROGRESS ***

LPDP AC Caps

From SOC

To HDMI

DP_DP2HDMI_DATA_N<0>	CH820 0.1UF	DPRX_DATA_N<0>	132S0444
DP_DP2HDMI_DATA_P<0>	CH821 0.1UF	DPRX_DATA_P<0>	132S0444
DP_DP2HDMI_DATA_N<1>	CH822 0.1UF	DPRX_DATA_N<1>	132S0444
DP_DP2HDMI_DATA_P<1>	CH823 0.1UF	DPRX_DATA_P<1>	132S0444
DP_DP2HDMI_DATA_N<2>	CH824 0.1UF	DPRX_DATA_N<2>	132S0444
DP_DP2HDMI_DATA_P<2>	CH825 0.1UF	DPRX_DATA_P<2>	132S0444
DP_DP2HDMI_DATA_N<3>	CH826 0.1UF	DPRX_DATA_N<3>	132S0444
DP_DP2HDMI_DATA_P<3>	CH827 0.1UF	DPRX_DATA_P<3>	132S0444
DP_DP2HDMI_AUX_N	CH828 0.1UF	DPRX_AUX_N	132S0444
DP_DP2HDMI_AUX_P	CH829 0.1UF	DPRX_AUX_P	132S0444

GND_VOID=TRUE; 10% 6.3V CERM-X5R 0201

DP2HDMI_RESET_L → RH801 0 (0% 1/20W TK 0201, 117S00073) → DP2HDMI_RESET_R_L

THIS SHORTS PMU TO SAK CONTROL

HDMI ROM BOM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S0915	1	IC,SRL SPI FLASH ROM,4MBIT,50MHZ,USON8	UH701	CRITICAL	HDMI_ROM:512
341S02274	1	ROM,HDMI (V03.00.00) DVT,X2267	UH701	CRITICAL	HDMI_ROM:3_00

USE APN:341 ROM OPTIONS
APN:335 ARE BASE BLANK PARTS

THIS IS USED FOR CONTROLLING HDMI PORT POWER VIA THE PMU SYS ALIVE NET
THIS SAK IS USED FOR COBRA POWER SEQUENCING

***PLEASE REFER TO NOTE1 ON CSA2 FOR PROPER SIGNAL NAMING OF "PP1V8_HDMI_PWR_SEQ"

PP1V8_AON → CH806 0.1UF (10% 6.3V CERM-X5R 0201, 132S0444)

UH806 SLG4AP45256 STQFN 343S00528

PMU_SYS_ALIVE	SYS_ACTIVE	DISCHARGE_EN	P0V95_DSCHG_EN_RC
DP2HDMI_PWR_EN	HDMI_ENABLE	PP0V95V_EN	P0V95_HDMI_EN
NC_UH805_5	NC	PP1V2_EN	P1V2_HDMI_PWR_EN
NC_UH805_11	NC	PP3V3_EN	P3V3_HDMI_PWR_EN
		RESETB	DP2HDMI_RESET_R_L
		RESETB_2	NC_HDMI_SAK_RESETB_2

VDD, GND

TPH704 A 1 TP-P40

LEVEL SHIFTERS

PP1V2_S2 → CH842 0.1UF (10% 6.3V CERM-X5R 0201, 132S0444)

NO_XNET_CONNECTION=1 → RH822 30K (1% 1/20W TK 0201, 118S00521)

PP3V3_AWAKESW_DP2HDMI → CH841 0.1UF (10% 6.3V CERM-X5R 0201, 132S0444)

UH840 311S00337 SN74AXC1T45-S SOT-5X3 (VCCA VCCB DIR A B GND)

SPI_DP2HDMI_HOLD_L → SPI_DP2HDMI_HOLD_L_3V3

PP3V3_S2 → CH802 0.1UF (10% 16V X5R-CERM 0201, 132S0288)

UH802 SN74LVC1G07 SON 311S0536 (VCC A Y GND, NC NC NC)

HDMI_HPD_IN → HDMI_AOP_HPD_R → HDMI_HPD_AOP

PP1V2_S2 → RH803 30K (1% 1/20W TK 0201, 118S00521) NOSTUFF

RH804 100 (1% 1/20W TK 0201-1, 118S00250)

PP1V2_S2 → CH801 0.1UF (10% 16V X5R-CERM 0201, 132S0288)

NO_XNET_CONNECTION=1 → RH815 30K (1% 1/20W TK 0201, 118S00521)

UH801 SN74AUP2G07 SON 311S00285 (VCC 1A 1Y 2A 2Y GND)

HDMI_CEC_AOP_TX → RH806 0 (0% 1/20W TK 0201, 117S00073) → AOP_HDMI_CEC_R

CEC_R → RH810 187 (1% 1/20W TK 0201, 118S00361) → HDMI_CEC

NO_XNET_CONNECTION=1 → RH816 27K (5% 1/20W TK 0201, 117S00121)

HDMI_AOP_CEC_R → RH805 100 (1% 1/20W TK 0201-1, 118S00250) → HDMI_CEC_AOP_RX

CONNECT THIS NET TO 5V_S2_MAIN

PLACE THIS NEAR 5V_S2_MAIN_VR_OUTPUT
PLACE_NEAR=CH917:10mm

XWH801 SM: PP5V_S2_HOLD → PP5V_S2_HDMI_LDO (VOLTAGE=5)

BOM_COST_GROUP=HDMI

PAGE TITLE: HDMI: Project Support 1

Apple Inc.

DRAWING NUMBER: 051-08286 SIZE: D
REVISION: 5.0.3
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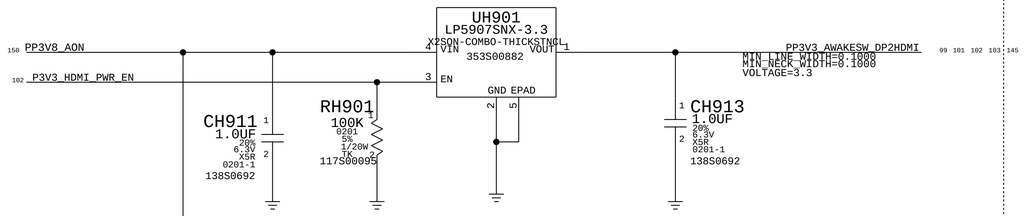
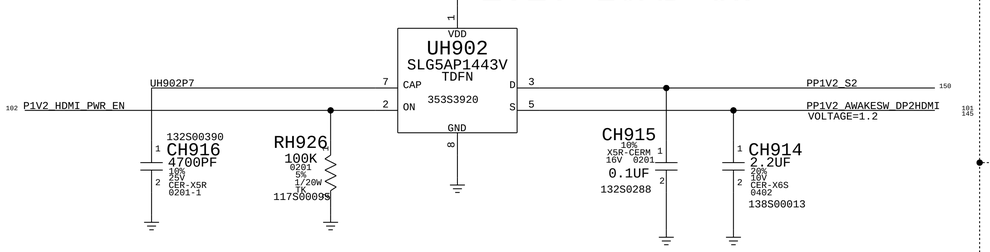
3.3V LDO

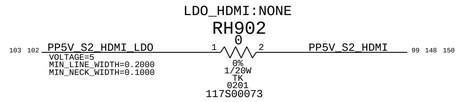


1.2V LOAD SW

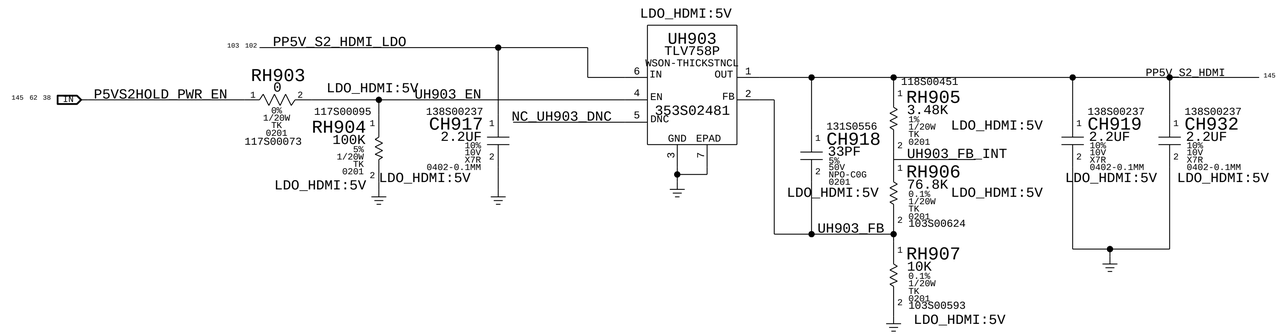


THIS IS USED FOR LONGER 5V POWER PATHS TO ENSURE GOOD 5V REGULATION

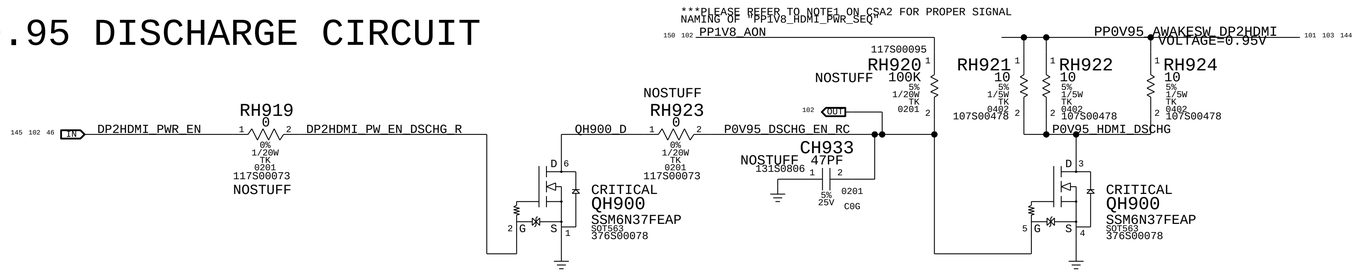
Enable BOMOPTION LDO_HDMI:NONE to disable the LDO use



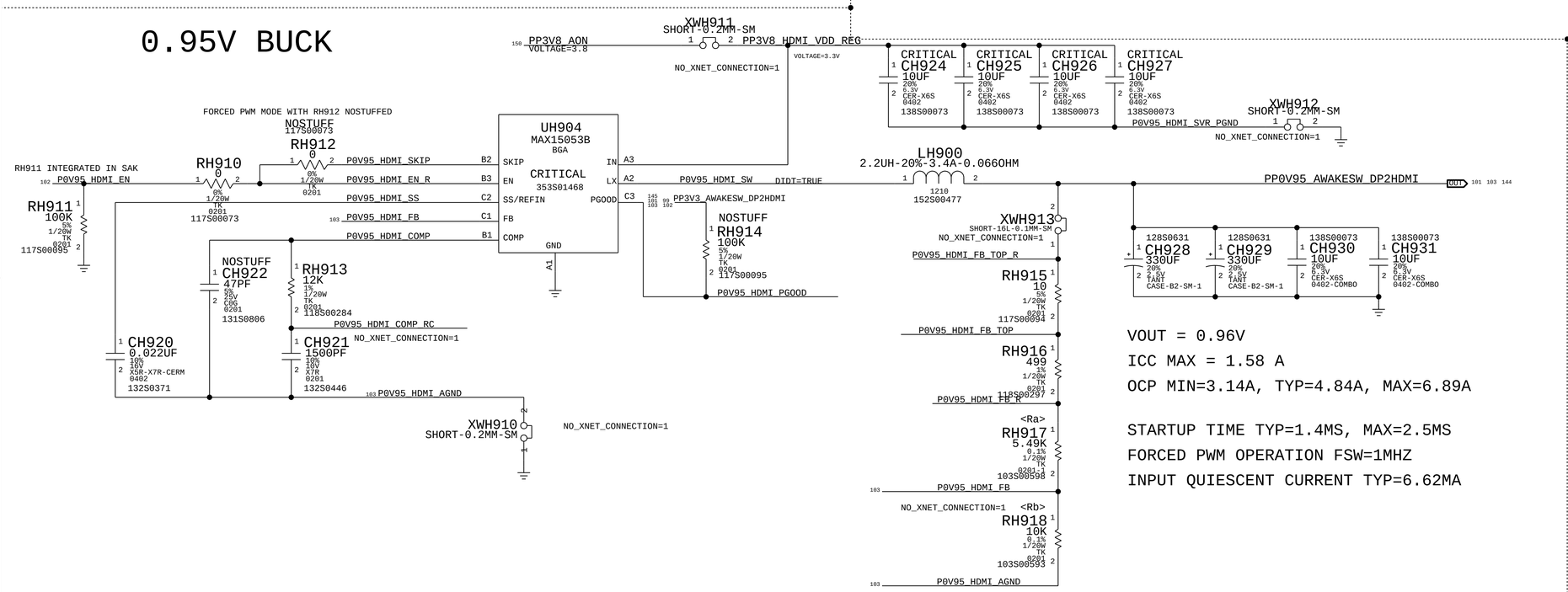
Enable BOMOPTION LDO_HDMI:5V to test HDMI 5V limit to 5.3V



0.95 DISCHARGE CIRCUIT



0.95V BUCK



VOUT = 0.96V

ICC MAX = 1.58 A

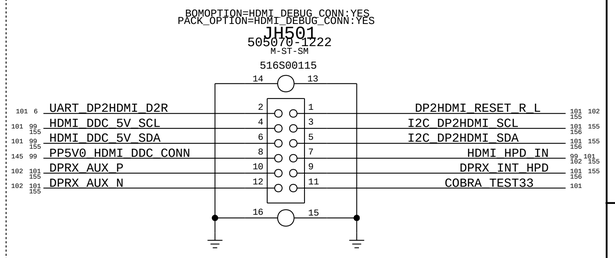
OCP MIN=3.14A, TYP=4.84A, MAX=6.89A

STARTUP TIME TYP=1.4MS, MAX=2.5MS

FORCED PWM OPERATION FSW=1MHZ

INPUT QUIESCENT CURRENT TYP=6.62MA

HDMI DEBUG CONNECTOR



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	Apple Inc.
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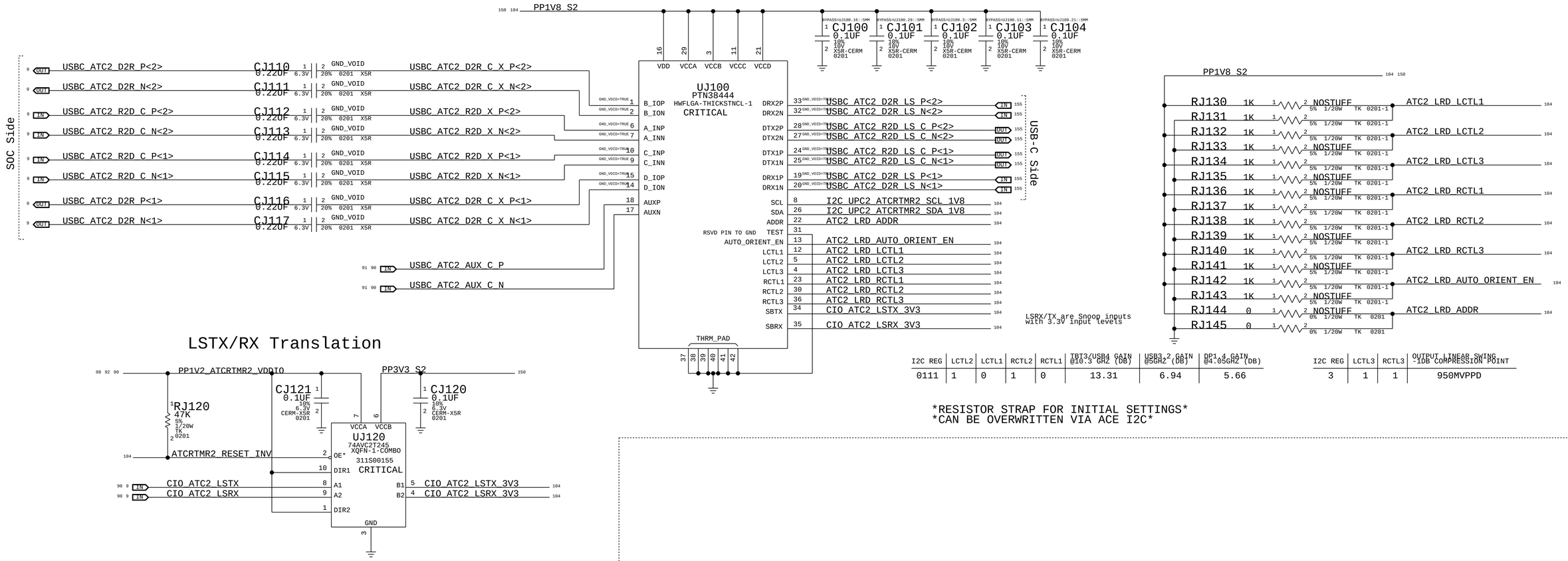


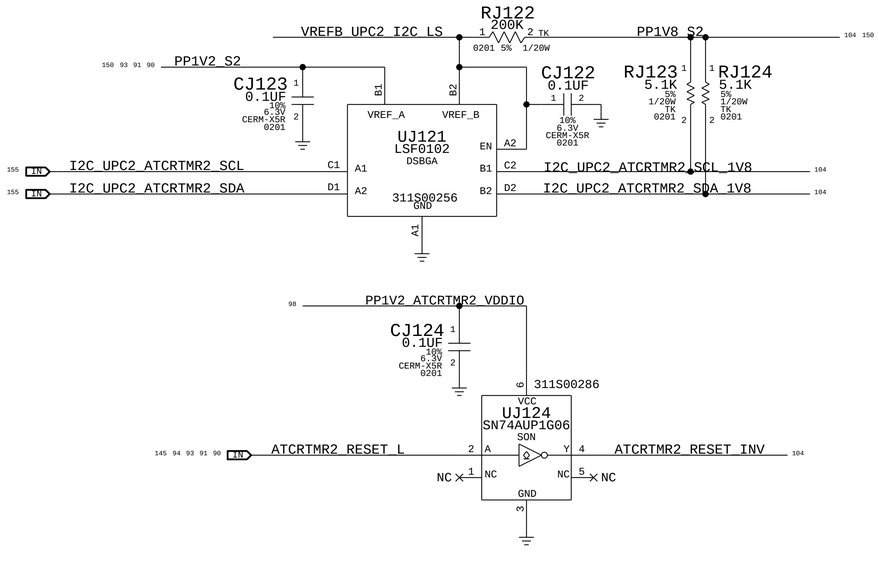
I2C REG	LCTL2	LCTL1	RCTL2	RCTL1	TBT3/USB4 GAIN @10.3 GHZ (DB)	USB3.2 GAIN @5GHZ (DB)	DP1.4 GAIN @4.05GHZ (DB)
0111	1	0	1	0	13.31	6.94	5.66

I2C REG	LCTL3	RCTL3	OUTPUT LINEAR SWING -1DB COMPRESSION POINT
3	1	1	950MVPPD

RESISTOR STRAP FOR INITIAL SETTINGS
CAN BE OVERWRITTEN VIA ACE I2C

LSTX/RX Translation

I2C Translation



Possible ATC3 Redriver
Circuit will be identical to that of ATC2

BOM_COST_GROUP=USB-C

PAGE TITLE
USB-C: CIO Redrivers 2/3

Apple Inc.

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BOM_COST_GROUP=SECURE ELEMENT

PAGE TITLE
USB-C: CIO Redrivers 4/5

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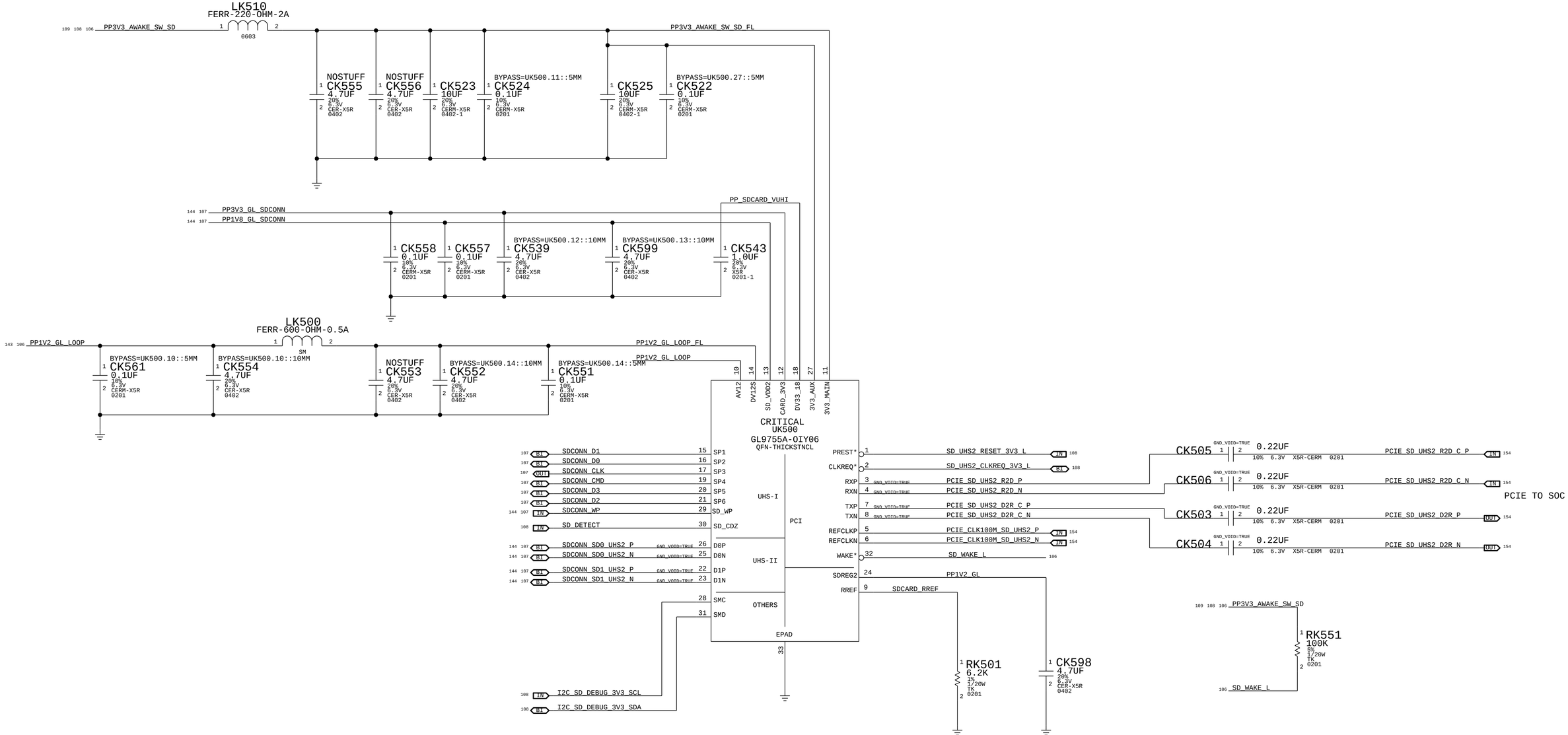

PAGE TITLE
SDCARD CONTROLLER

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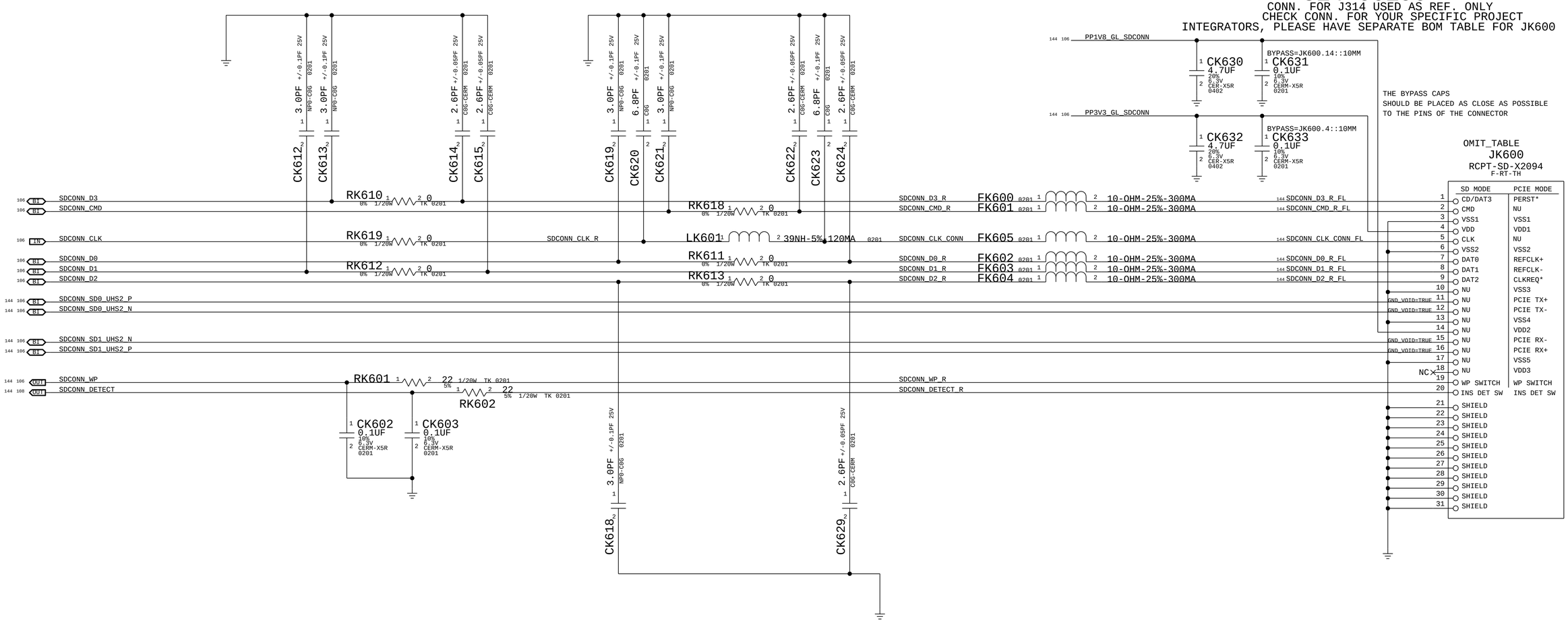
SD CARD CONNECTOR
514-00196

CONN. FOR J314 USED AS REF. ONLY
CHECK CONN. FOR YOUR SPECIFIC PROJECT
INTEGRATORS, PLEASE HAVE SEPARATE BOM TABLE FOR JK600



BOM_COST_GROUP=SDCARD

PAGE TITLE: SDCARD CONNECTOR

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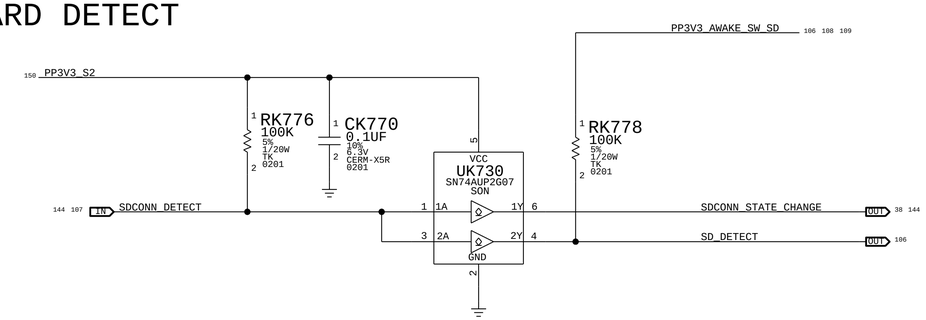
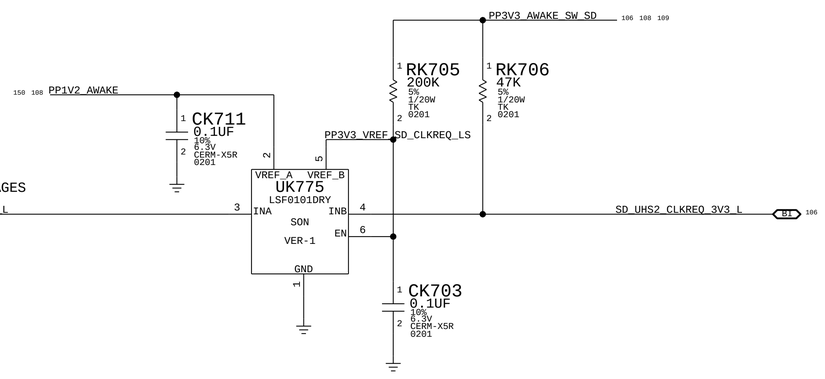
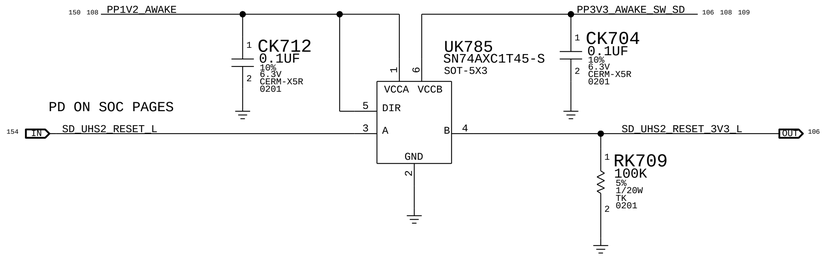
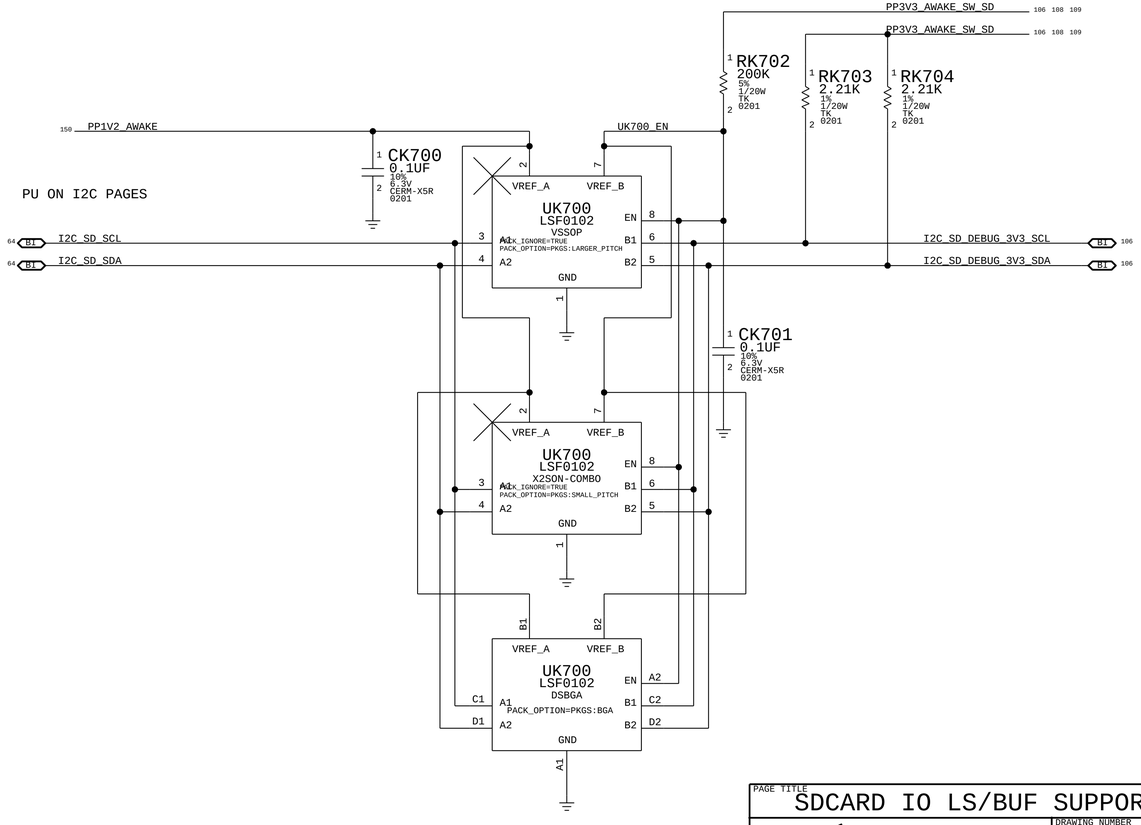
CARD DETECT



CONTROLLER IO







BOM_COST_GROUP=SDCARD

PAGE TITLE
SDCARD IO LS/BUF SUPPORT

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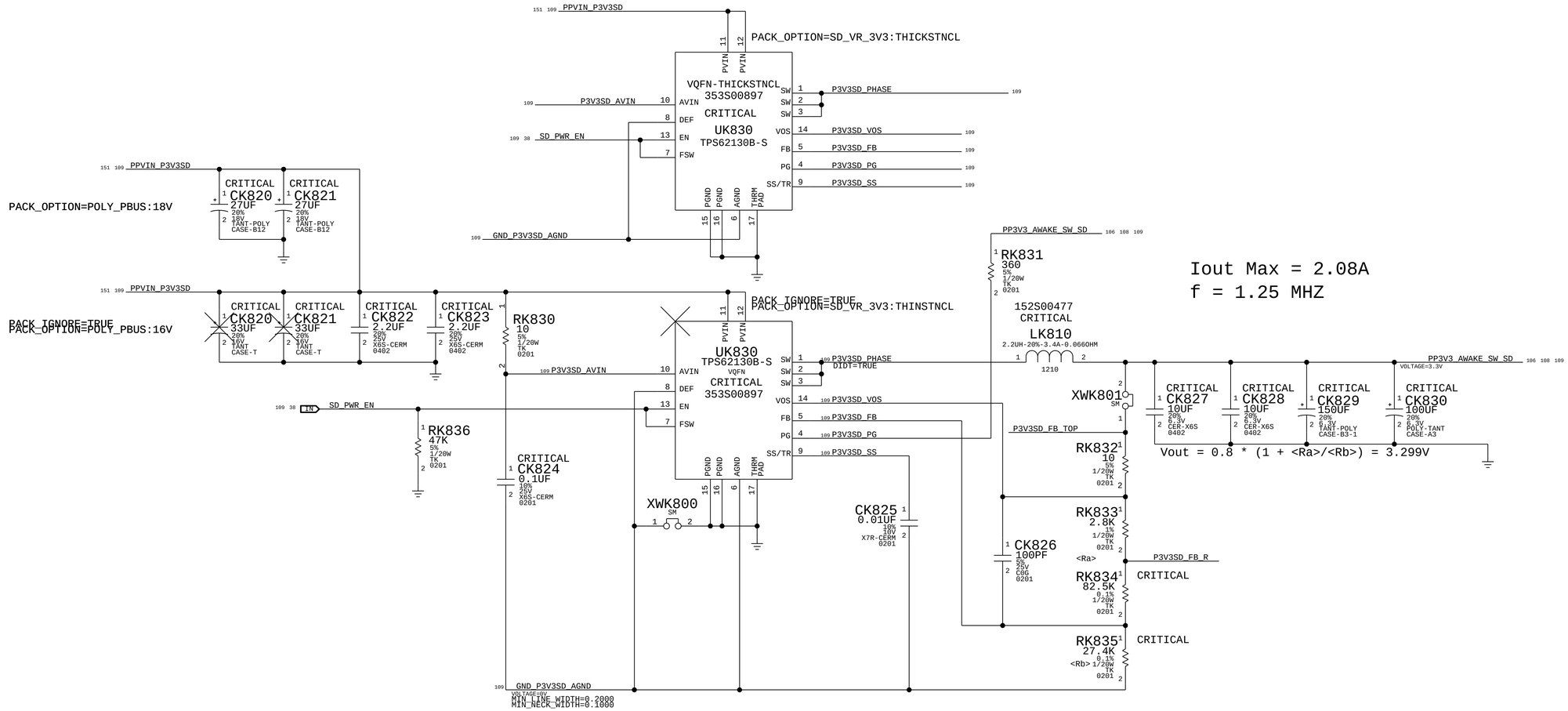

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*** OK2INTEGRATE ***

FOR SYSTEM INTEGRATION INFORMATION OF WILLAMETTE REFER TO
RDAR://PROBLEM/72432057

WILLAMETTE WIFI/BT MODULE

PLACE_NEAR=UL000.48:5MM
PLACE_NEAR=UL000.48:5MM
PLACE_NEAR=UL000.48:5MM
PP3V8_AON_WLBT 110 148 151
CL005 10UF 20% 10V X5R-CERM 0402-8
CL030 3PF +/-0.1PF 25V C0G 0201
CRITICAL
CL020 12PF 5% 25V NP0-C0G 0201
VBAT

PLACE_NEAR=UL000.37:5MM
PLACE_NEAR=UL000.37:5MM
PLACE_NEAR=UL000.37:5MM
PP3V8_AON_WLBT 110 148 151
CL006 10UF 20% 10V X5R-CERM 0402-8
CL031 3PF +/-0.1PF 25V C0G 0201
CRITICAL
CL021 12PF 5% 25V NP0-C0G 0201
2GFEM_C0

PLACE_NEAR=UL000.79:5MM
PLACE_NEAR=UL000.79:5MM
PLACE_NEAR=UL000.79:5MM
PP3V8_AON_WLBT 110 148 151
CL007 10UF 20% 10V X5R-CERM 0402-8
CL032 3PF +/-0.1PF 25V C0G 0201
CRITICAL
CL022 12PF 5% 25V NP0-C0G 0201
2GFEM_C1

PLACE_NEAR=UL000.12:5MM
PLACE_NEAR=UL000.12:5MM
PLACE_NEAR=UL000.12:5MM
PP3V8_AON_WLBT 110 148 151
CL008 10UF 20% 10V X5R-CERM 0402-8
CL033 3PF +/-0.1PF 25V C0G 0201
CRITICAL
CL023 12PF 5% 25V NP0-C0G 0201
5GFEM

PLACE_NEAR=UL000.31:5MM
PLACE_NEAR=UL000.31:5MM
PLACE_NEAR=UL000.31:5MM
PP1V8_S2 110 148 150
CL010 0.1UF 10% 6.3V CERM-X5R 0201
CRITICAL
CL024 12PF 5% 25V NP0-C0G 0201
2GFEM_C0

PLACE_NEAR=UL000.86:5MM
PLACE_NEAR=UL000.86:5MM
PLACE_NEAR=UL000.86:5MM
PP1V8_S2 110 148 150
CL011 10UF 20% 10V X5R-CERM 0402-8
CRITICAL
CL025 12PF 5% 25V NP0-C0G 0201
2GFEM_C1

PLACE_NEAR=UL000.22:5MM
PLACE_NEAR=UL000.22:5MM
PLACE_NEAR=UL000.22:5MM
PP1V8_S2 110 148 150
CL012 0.1UF 10% 6.3V CERM-X5R 0201
CL034 3PF +/-0.1PF 25V C0G 0201
5GFEM_C0

PLACE_NEAR=UL000.4:5MM
PLACE_NEAR=UL000.4:5MM
PLACE_NEAR=UL000.4:5MM
PP1V8_S2 110 148 150
CL013 0.1UF 10% 6.3V CERM-X5R 0201
CL035 3PF +/-0.1PF 25V C0G 0201
5GFEM_C1

PP1V8_S2 150 148 110
PP3V8_AON_WLBT 151 148 110
PP1V2_S2
PLACE_NEAR=UL000.52:4MM
CL014 0.1UF 10% 6.3V CERM-X5R 0201

UL000
2103-602102-10
LGA
SYM 1 OF 4

11	VDD_5G_C0C1	VDD1V8_2G_C0	31	
12	VDD_5G_C0C1	VDD1V8_2G_C1	86	
13	VDD_5G_C0C1	VDD1V8_5G_C0	22	
14	VDD_5G_C0C1	VDD1V8_5G_C1	4	
37	VDD_2G_C0	VDDIO_RF	66	
38	VDD_2G_C0	VDDIOIP8	67	
79	VDD_2G_C1	VDDIOIP2	52	
80	VDD_2G_C1			
69	VDD_BT			
48	VBAT			
49	VBAT			
50	VBAT			
133	VBAT			
134	VBAT			
135	VBAT			

111	BT	RF_ANT_0 NO_TEST=1	28	ANT_0
111	BT	RF_ANT_1 NO_TEST=1	89	ANT_1
111	BT	RF_BT_DED NO_TEST=1	73	BT_DEDICATED
		NC_BT_GPIO_2 NO_TEST=1	413	BT_GPIO_2
145 111 110 6	OUT	BT_TIME_SYNC	435	BT_GPIO_3
110	BT	BT_I2C_DATA	129	BT_GPIO_4
110	BT	BT_I2C_CLK	41	BT_GPIO_5
110 12	IN	SPMI_WLBT_CLK	126	SPMI_HEB_CLK
110 12	BT	SPMI_WLBT_DATA	391	SPMI_HEB_DAT
110		BT_LHL_GPIO2	523	LHL_GPIO2
		NC_SPMI_IDC_CLK	40	SPMI_IDC_CLK
		NC_SPMI_IDC_DATA	127	SPMI_IDC_DAT
145 111 110 46 38	IN	WLBT_PWR_EN	130	WLBT_REG_ON
145 111 110 38	IN	PMU_CLK32K_WLBT	479	WLBT_CLK_32K
110		WLAN_JTAG_SEL	540	JTAG_SEL
			131	PACKAGEOPTION_2

RL002 10K 5% 1/20W TK 0201

OMIT_TABLE

WL_GPIO_0	542	WLBT_WAKE	OUT 46 110 111
WL_GPIO_1	528	WLAN_TIME_SYNC	OUT 6 110 111
WL_GPIO_2	526	TP_WLAN_JTAG_TCK	110 111
WL_GPIO_3	525	TP_WLAN_JTAG_TMS	110 111
WL_GPIO_4	75	TP_WLAN_JTAG_TDI	110
WL_GPIO_5	76	TP_WLAN_JTAG_TDO	110
WL_GPIO_6	158	TP_WLAN_JTAG_TRSTN	110
WL_GPIO_7	538	WL_GPIO_7	110
WL_GPIO_8	153	NC_WL_GPIO_8 NO_TEST=1	
WL_GPIO_9	527	NC_WL_GPIO_9 NO_TEST=1	
WL_GPIO_10	159	NC_WL_GPIO_10 NO_TEST=1	
WL_GPIO_11	140	NC_WL_GPIO_11 NO_TEST=1	
WL_GPIO_12	138	NC_WL_GPIO_12 NO_TEST=1	
WL_GPIO_13	42	NC_WL_GPIO_13 NO_TEST=1	
WL_GPIO_14	539	NC_WL_GPIO_14 NO_TEST=1	
WL_GPIO_15	139	NC_WL_GPIO_15 NO_TEST=1	
WL_GPIO_16	541	NC_WL_GPIO_16 NO_TEST=1	
WL_GPIO_18	44	NC_WL_GPIO_18 NO_TEST=1	
WL_GPIO_19	43	NC_WL_GPIO_19 NO_TEST=1	
WLBT_PCIE_PERST_L	534	WLBT_RESET_L	IN 8 110 111
WLBT_PCIE_CLKREQ_L	531	WLBT_CLKREQ_R_L	110
WLBT_PCIE_RXD_P	143	PCIE_WLBT_R2D_P	110
WLBT_PCIE_RXD_N	142	PCIE_WLBT_R2D_N	110
WLBT_PCIE_TXD_P	146	PCIE_WLBT_D2R_C_P	110
WLBT_PCIE_TXD_N	145	PCIE_WLBT_D2R_C_N	110
WLBT_PCIE_REFCLK_P	148	PCIE_CLK100M_WLBT_P	IN 8 110
WLBT_PCIE_REFCLK_N	149	PCIE_CLK100M_WLBT_N	IN 8 110

GND_VOID=TRUE
PLACE_NEAR=UL000.143:4MM
8 IN PCIE_WLBT_R2D_C_P — CL001 0.1UF 6.3V 10% 1 2 CERM-X5R 0201 — PCIE_WLBT_R2D_P 110
8 IN PCIE_WLBT_R2D_C_N — CL002 0.1UF 6.3V 10% 1 2 CERM-X5R 0201 — PCIE_WLBT_R2D_N 110
PLACE_NEAR=UL000.142:4MM
GND_VOID=TRUE

GND_VOID=TRUE
PLACE_NEAR=UL000.146:4MM
110 PCIE_WLBT_D2R_C_P — CL003 0.1UF 6.3V 10% 1 2 CERM-X5R 0201 — PCIE_WLBT_D2R_P OUT 8 110
110 PCIE_WLBT_D2R_C_N — CL004 0.1UF 6.3V 10% 1 2 CERM-X5R 0201 — PCIE_WLBT_D2R_N OUT 8 110
PLACE_NEAR=UL000.145:4MM
GND_VOID=TRUE

110 12 SPMI_WLBT_CLK — RL003 200K 1/20W 5% 1 2 0201 TK
110 12 SPMI_WLBT_DATA — RL004 200K 1/20W 5% 1 2 0201 TK

110 WLBT_CLKREQ_R_L — RL001 1K 1/20W 5% 1 2 0201-1 TK — WLBT_CLKREQ_L BI 8 110 111

BOM_COST_GROUP=WIRELESS

TPL001 A 1 — TPL001 A 1 — PMU_CLK32K_WLBT 38 110 111 145
TPL002 — WLBT_PWR_EN 38 46 110 111 145
TPL003 — WLBT_WAKE 46 110 111
TPL004 — TP_WLAN_JTAG_TCK 110 111
TPL005 — TP_WLAN_JTAG_TMS 110 111
TPL006 — TP_WLAN_JTAG_TDI 110
TPL007 — TP_WLAN_JTAG_TDO 110
TPL008 — TP_WLAN_JTAG_TRSTN 110
TPL009 — WLAN_JTAG_SEL 110
TPL010 — BT_TIME_SYNC 6 110 111 145
TPL011 — WLAN_TIME_SYNC 6 110 111
TPL012 — BT_I2C_DATA 110
TPL013 — BT_I2C_CLK 110
PACK_OPTION=IGNORE=TRUE
PACK_OPTION=WLBT_TP_0P5
PACK_OPTION=WLBT_TP_0P4
TP-P40

TPL018 — SPMI_WLBT_CLK 12 110
TPL019 — SPMI_WLBT_DATA 12 110
TPL020 — BT_LHL_GPIO2 110

PPL021 P2MM 3M PP 1 — PCIE_CLK100M_WLBT_P 8 110
PPL022 P2MM 3M PP 1 — PCIE_CLK100M_WLBT_N 8 110

TPL023 — WLBT_RESET_L 8 110 111
TPL024 — WLBT_CLKREQ_L 8 110 111
TPL025 — WL_GPIO_7 110

PPL026 P2MM 3M PP 1 — PACK_OPTION=WLBT_PP_D2R — PCIE_WLBT_D2R_P 8 110
PPL027 P2MM 3M PP 1 — PACK_OPTION=WLBT_PP_D2R — PCIE_WLBT_D2R_N 8 110

WILLAMETTE BOM TABLE:

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
339S01093	1	MODULE,WLAN/BT,WILLAMETTE, ES4.7	UL000	CRITICAL	

WLMT ALT BOM TABLE:

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
339S01206	339S01093	ANY	UL000	AMKOR

PAGE TITLE: WIFI/BT: MODULE

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WILLAMETTE WIFI/BT MODULE GND

UL000
2103-602102-10
LGA
SYM 2 OF 4

1	GND	GND	110
2	GND	GND	111
3	GND	GND	112
5	GND	GND	113
6	GND	GND	114
7	GND	GND	115
8	GND	GND	116
9	GND	GND	117
10	GND	GND	118
15	GND	GND	119
16	GND	GND	120
17	GND	GND	121
18	GND	GND	122
19	GND	GND	123
20	GND	GND	124
21	GND	GND	125
23	GND	GND	128
24	GND	GND	132
25	GND	GND	136
26	GND	GND	137
27	GND	GND	141
29	GND	GND	144
30	GND	GND	147
32	GND	GND	150
33	GND	GND	151
34	GND	GND	152
35	GND	GND	154
36	GND	GND	155
39	GND	GND	156
45	GND	GND	157
46	GND	GND	160
47	GND	GND	161
51	GND	GND	162
53	GND	GND	163
54	GND	GND	164
55	GND	GND	165
56	GND	GND	166
57	GND	GND	167
58	GND	GND	168
59	GND	GND	169
60	GND	GND	170
61	GND	GND	171
62	GND	GND	172
63	GND	GND	173
64	GND	GND	174
65	GND	GND	175
68	GND	GND	176
70	GND	GND	177
71	GND	GND	178
72	GND	GND	179
74	GND	GND	180
77	GND	GND	181
78	GND	GND	182
81	GND	GND	183
82	GND	GND	184
83	GND	GND	185
84	GND	GND	186
85	GND	GND	187
87	GND	GND	188
88	GND	GND	189
90	GND	GND	190
91	GND	GND	191
92	GND	GND	192
93	GND	GND	193
94	GND	GND	194
95	GND	GND	195
96	GND	GND	196
97	GND	GND	197
98	GND	GND	198
99	GND	GND	199
100	GND	GND	200
101	GND	GND	201
102	GND	GND	202
103	GND	GND	203
104	GND	GND	204
105	GND	GND	205
106	GND	GND	206
107	GND	GND	207
108	GND	GND	208
109	GND	GND	209

UL000
2103-602102-10
LGA
SYM 3 OF 4

210	GND	GND	290
211	GND	GND	291
212	GND	GND	292
213	GND	GND	293
214	GND	GND	294
215	GND	GND	295
216	GND	GND	296
217	GND	GND	297
218	GND	GND	298
219	GND	GND	299
220	GND	GND	300
221	GND	GND	301
222	GND	GND	302
223	GND	GND	303
224	GND	GND	304
225	GND	GND	305
226	GND	GND	306
227	GND	GND	307
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231	GND	GND	311
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243	GND	GND	323
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246	GND	GND	326
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284	GND	GND	364
285	GND	GND	365
286	GND	GND	366
287	GND	GND	367
288	GND	GND	368
289	GND	GND	369

UL000
2103-602102-10
LGA
SYM 4 OF 4

370	GND	GND	453
371	GND	GND	454
372	GND	GND	455
373	GND	GND	456
374	GND	GND	457
375	GND	GND	458
376	GND	GND	459
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389	GND	GND	472
390	GND	GND	473
392	GND	GND	474
393	GND	GND	475
394	GND	GND	476
395	GND	GND	477
396	GND	GND	478
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402	GND	GND	485
403	GND	GND	486
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405	GND	GND	488
406	GND	GND	489
407	GND	GND	490
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412	GND	GND	495
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442	GND	GND	524
443	GND	GND	529
444	GND	GND	530
445	GND	GND	532
446	GND	GND	533
447	GND	GND	535
448	GND	GND	536
449	GND	GND	537
450	GND	GND	543
451	GND	GND	544
452	GND	GND	545

ANTENNA CONNECTORS

2G_C0
5G_C0
BT_C0

JL120
IR050D15010C
F-ST-SM
1 RF_ANT_0 — NO_TEST=1 — BI 110 111
SUNWAY_1P5MM
PACK_OPTION=SUNWAY
BOMOPTION=RF_CONN

JL140
20449-001E-03
F-ST-SM
1 RF_ANT_0 110 111
SUNWAY_1P5MM
PACK_IGNORE=TRUE
PACK_OPTION=IPEX_1P5
BOMOPTION=RF_CONN

JL130
20431-001E-01
F-ST-SM
2 GND, SIGNAL 1 RF_ANT_0 110 111
IPEX 2MM
PACK_OPTION=3X_ANTENNA_IPEX
BOMOPTION=RF_CONN
PACK_IGNORE=TRUE

RF CONNECTOR ALTERNATE BOM:

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
518S0867	518S00033	RFCONN_ALT	ALL	IPEX

2G_C1
5G_C1
BT_C1

JL121
IR050D15010C
F-ST-SM
1 RF_ANT_1 — NO_TEST=1 — BI 110 111
SUNWAY_1P5MM
PACK_OPTION=SUNWAY
BOMOPTION=RF_CONN

JL141
20449-001E-03
F-ST-SM
1 RF_ANT_1 110 111
SUNWAY_1P5MM
PACK_IGNORE=TRUE
PACK_OPTION=IPEX_1P5
BOMOPTION=RF_CONN

JL131
20431-001E-01
F-ST-SM
2 GND, SIGNAL 1 RF_ANT_1 110 111
IPEX 2MM
PACK_OPTION=3X_ANTENNA_IPEX
BOMOPTION=RF_CONN
PACK_IGNORE=TRUE

BT_C1_DED

JL122
IR050D15010C
F-ST-SM
1 111 RF_BT_DED_ANT — NO_TEST=1
SUNWAY_1P5MM
PACK_OPTION=3X_ANTENNA
BOMOPTION=RF_CONN

JL142
20449-001E-03
F-ST-SM
1
SUNWAY_1P5MM
PACK_IGNORE=TRUE
PACK_OPTION=IPEX_1P5_3X
BOMOPTION=RF_CONN

UL101
2GHZ
LFL182G44UA1F627
IN 1, OUT 3, GND 2
RF_BT_DED — NO_TEST=1 — BI 110 111
PACK_OPTION=BT_FILTER_1P5MM
BOMOPTION=RF_CONN
ALLOW_APPLE_PREFIX=U

JL132
20431-001E-01
F-ST-SM
2 GND, SIGNAL 1 111 RF_BT_DED_ANT
IPEX 2MM
PACK_OPTION=3X_ANTENNA_IPEX
BOMOPTION=RF_CONN
PACK_IGNORE=TRUE

UL111
2GHZ
LFL182G44UA1F627
IN 1, OUT 3, GND 2
RF_BT_DED 110 111
PACK_IGNORE=TRUE
PACK_OPTION=3X_ANTENNA_IPEX
BOMOPTION=RF_CONN
ALLOW_APPLE_PREFIX=U

WLBT DEBUG CONNECTOR

JL103
505070-1222
M-ST-SM

110 6	WLAN_TIME_SYNC	TP_WLAN_JTAG_TCK	4388 SWD:
NC		TP_WLAN_JTAG_TMS	SWD_CLK 110
NC		NC	SWD_DIO 110
110 46	WLBT_WAKE	WLBT_CLKREQ_L	8 110
145 110 46 38	WLBT_PWR_EN	BT_TIME_SYNC	6 110 145
110 8	WLBT_RESET_L	PMU_CLK32K_WLBT	38 110 145

BOMOPTION=WLBT_DBG
PACK_IGNORE=TRUE
PACK_OPTION=WLBT_DBG_CONN

BOM_COST_GROUP=WIRELESS

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WIFI/BT: ANTENNA and GND

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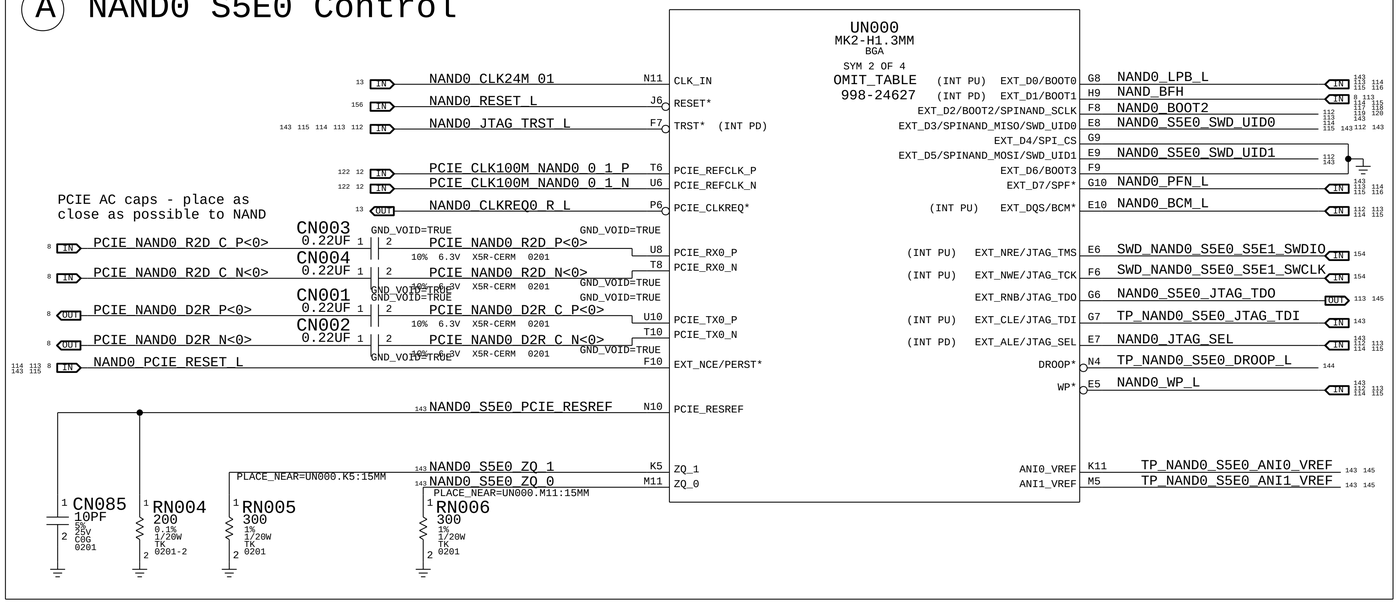
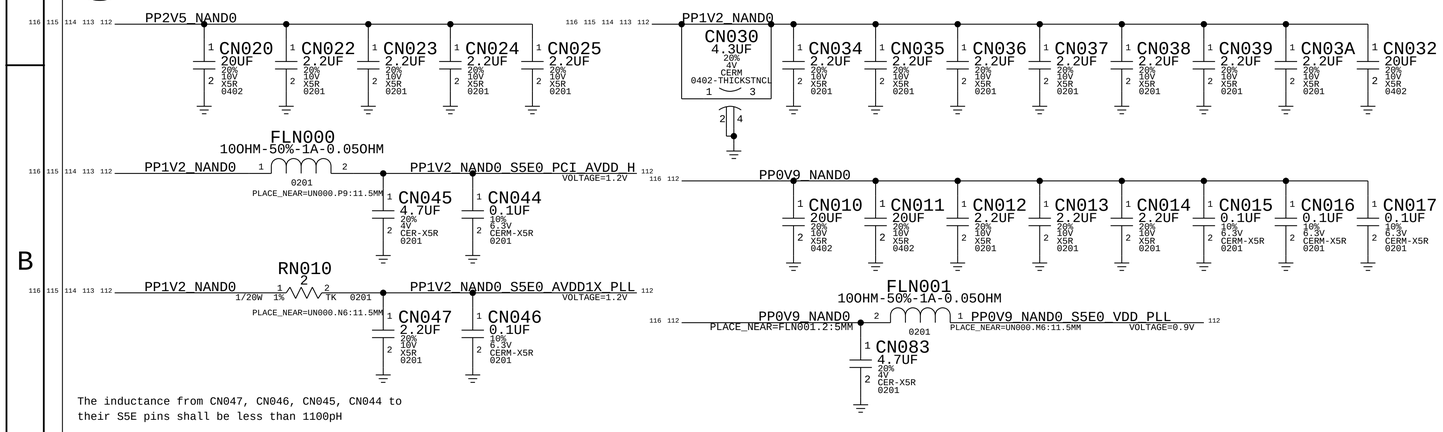
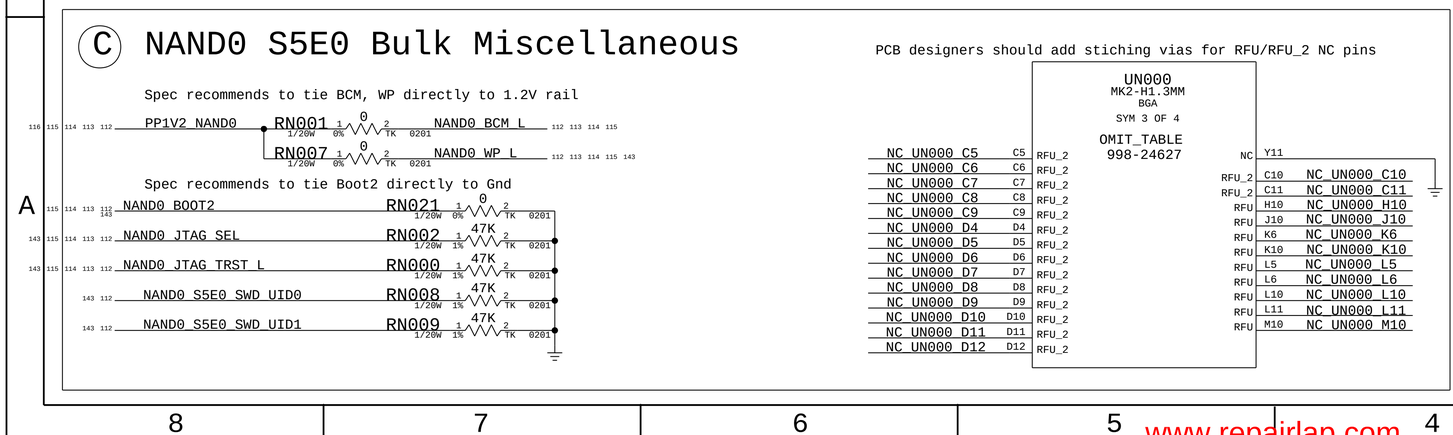
A NAND0 S5E0 Control



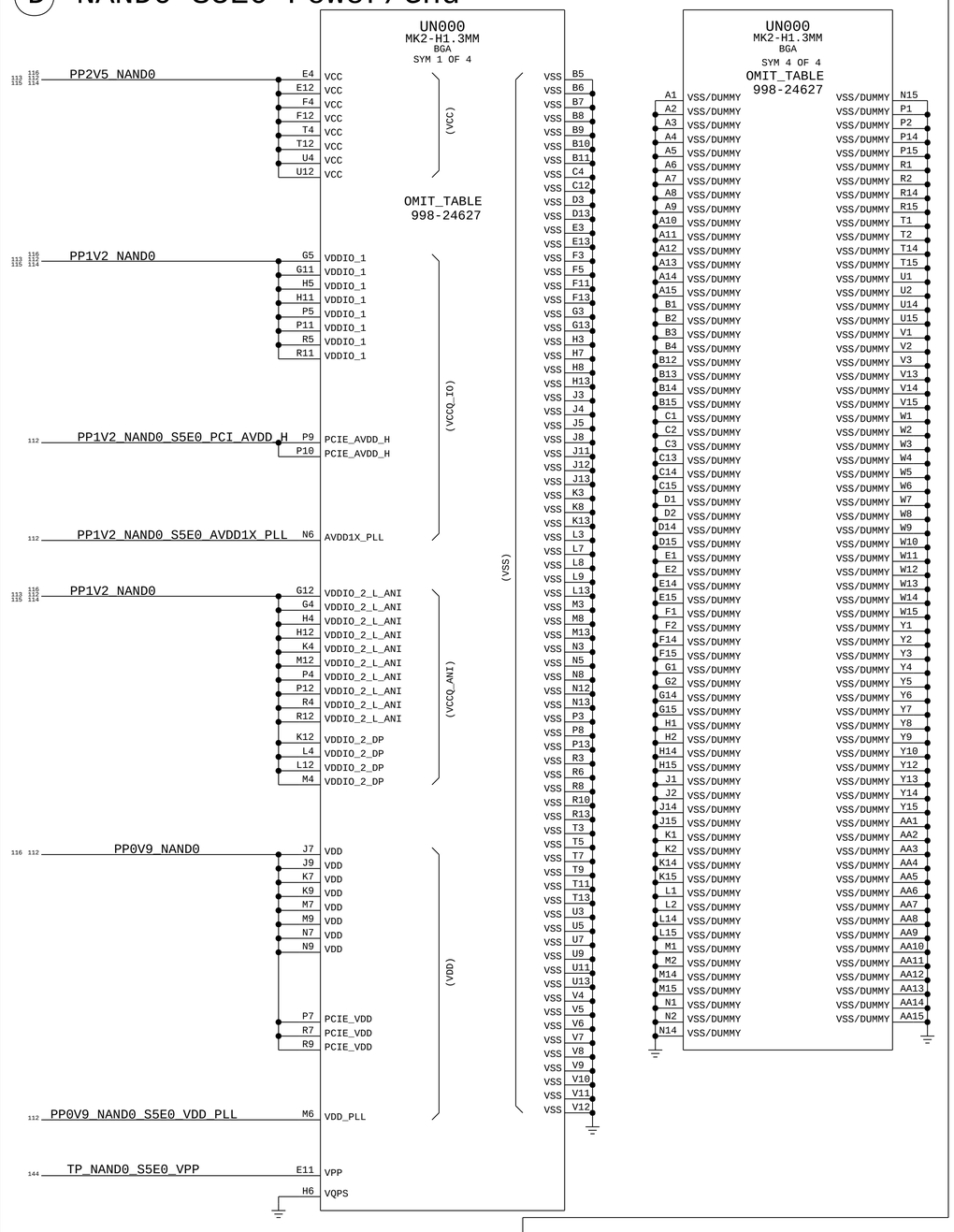
B NAND0 S5E0 Bulk Capacitance



C NAND0 S5E0 Bulk Miscellaneous



D NAND0 S5E0 Power/Gnd



PAGE TITLE
STORAGE: SSD0 S5E MK2 <0>
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A NAND0 S5E1 Control

UN100 MK2-H1.3MM BGA SYM 2 OF 4 OMIT_TABLE 998-24627

NAND0_CLK24M_01 → CLK_IN (N11)
NAND0_RESET_L → RESET* (J6)
NAND0_JTAG_TRST_L → TRST* (INT PD) (F7)
PCIE_CLK100M_NAND0_0_1_P → PCIE_REFCLK_P (T6)
PCIE_CLK100M_NAND0_0_1_N → PCIE_REFCLK_N (U6)
NAND0_CLKREQ1_R_L → PCIE_CLKREQ* (P6)

PCIE AC caps - place as close as possible to NAND

PCIE_NAND0_R2D_C_P<1> → SSD_2L CN103 0.22UF → PCIE_NAND0_R2D_P<1> → PCIE_RX0_P (U8)
PCIE_NAND0_R2D_C_N<1> → SSD_2L CN104 0.22UF → PCIE_NAND0_R2D_N<1> → PCIE_RX0_N (T8)
PCIE_NAND0_D2R_P<1> → SSD_2L CN101 0.22UF → PCIE_NAND0_D2R_C_P<1> → PCIE_TX0_P (U10)
PCIE_NAND0_D2R_N<1> → SSD_2L CN102 0.22UF → PCIE_NAND0_D2R_C_N<1> → PCIE_TX0_N (T10)
NAND0_PCIE_RESET_L → EXT_NCE/PERST* (F10)

NAND0_S5E1_PCIE_RESREF → PCIE_RESREF (N10)

SSD_2L CN185 10PF 5% 25V C0G 0201
SSD_2L RN104 200 0.1% 1/20W TK 0201-2
SSD_2L RN105 300 1% 1/20W TK 0201 (PLACE_NEAR=UN100.K5:15MM)
SSD_2L RN106 300 1% 1/20W TK 0201 (PLACE_NEAR=UN100.M11:15MM)

NAND0_S5E1_ZQ_1 → ZQ_1 (K5)
NAND0_S5E1_ZQ_0 → ZQ_0 (M11)

(INT PU)	EXT_D0/BOOT0 (G8)	NAND0_LPB_L
(INT PD)	EXT_D1/BOOT1 (H9)	NAND_BFH
	EXT_D2/BOOT2/SPINAND_SCLK (F8)	NAND0_BOOT2
	EXT_D3/SPINAND_MISO/SWD_UID0 (E8)	NAND0_S5E1_SWD_UID0
	EXT_D4/SPI_CS (G9)	
	EXT_D5/SPINAND_MOSI/SWD_UID1 (E9)	NAND0_S5E1_SWD_UID1
	EXT_D6/BOOT3 (F9)	
	EXT_D7/SPF* (G10)	NAND0_PFN_L
(INT PU)	EXT_DQS/BCM* (E10)	NAND0_BCM_L
(INT PU)	EXT_NRE/JTAG_TMS (E6)	SWD_NAND0_S5E0_S5E1_SWDIO
(INT PU)	EXT_NWE/JTAG_TCK (F6)	SWD_NAND0_S5E0_S5E1_SWCLK
	EXT_RNB/JTAG_TDO (G6)	NAND0_S5E1_JTAG_TDO
(INT PU)	EXT_CLE/JTAG_TDI (G7)	NAND0_S5E0_JTAG_TDO
(INT PD)	EXT_ALE/JTAG_SEL (E7)	NAND0_JTAG_SEL
DROOP*	N4	TP_NAND0_S5E1_DROOP_L
WP*	E5	NAND0_WP_L
ANI0_VREF	K11	TP_NAND0_S5E1_ANI0_VREF
ANI1_VREF	M5	TP_NAND0_S5E1_ANI1_VREF

B NAND0 S5E1 Bulk Capacitance

PP2V5_NAND0
SSD_2L CN120 20UF 20% 10V X5R 0402
SSD_2L CN122 2.2UF 20% 10V X5R 0201
SSD_2L CN123 2.2UF 20% 10V X5R 0201
SSD_2L CN124 2.2UF 20% 10V X5R 0201
SSD_2L CN125 2.2UF 20% 10V X5R 0201

PP1V2_NAND0
SSD_2L CN130 4.3UF 20% 4V CERM 0402-THICKSTNCL
SSD_2L CN134 2.2UF 20% 10V X5R 0201
SSD_2L CN135 2.2UF 20% 10V X5R 0201
SSD_2L CN136 2.2UF 20% 10V X5R 0201
SSD_2L CN137 2.2UF 20% 10V X5R 0201
SSD_2L CN138 2.2UF 20% 10V X5R 0201
SSD_2L CN139 2.2UF 20% 10V X5R 0201
SSD_2L CN13A 2.2UF 20% 10V X5R 0201
SSD_2L CN132 20UF 20% 10V X5R 0402

SSD_2L FLN100 10OHM-50%-1A-0.05OHM
PP1V2_NAND0 → PP1V2_NAND0_S5E1_PCI_AVDD_H (VOLTAGE=1.2V)
PLACE_NEAR=UN100.P9:11.5MM
SSD_2L CN145 4.7UF 20% 6.3V CER-X5R 0201
SSD_2L CN144 0.1UF 10% 6.3V CERM-X5R 0201

SSD_2L RN110 2 1/20W 1% TK 0201
PP1V2_NAND0 → PP1V2_NAND0_S5E1_AVDD1X_PLL (VOLTAGE=1.2V)
PLACE_NEAR=UN100.N6:11.5MM
SSD_2L CN147 2.2UF 20% 10V X5R 0201
SSD_2L CN146 0.1UF 10% 6.3V CERM-X5R 0201

PP0V9_NAND0
SSD_2L CN110 20UF 20% 10V X5R 0402
SSD_2L CN111 20UF 20% 10V X5R 0402
SSD_2L CN112 2.2UF 20% 10V X5R 0201
SSD_2L CN113 2.2UF 20% 10V X5R 0201
SSD_2L CN114 2.2UF 20% 10V X5R 0201
SSD_2L CN115 0.1UF 10% 6.3V CERM-X5R 0201
SSD_2L CN116 0.1UF 10% 6.3V CERM-X5R 0201
SSD_2L CN117 0.1UF 10% 6.3V CERM-X5R 0201

SSD_2L FLN101 10OHM-50%-1A-0.05OHM
PP0V9_NAND0 → PP0V9_NAND0_S5E1_VDD_PLL (VOLTAGE=0.9V)
PLACE_NEAR=FLN101.2:5MM
PLACE_NEAR=UN100.M6:11.5MM
SSD_2L CN183 4.7UF 20% 6.3V CER-X5R 0201

The inductance from CN147, CN146, CN145, CN144 to their S5E pins shall be less than 1100pH

C NAND0 S5E1 Bulk Miscellaneous

PP1V2_NAND0 → SSD_2L RN108 47K 1/20W 1% TK 0201 → NAND0_S5E1_SWD_UID0
NAND0_S5E1_SWD_UID1 → SSD_2L RN109 47K 1/20W 1% TK 0201

PCB designers should add stiching vias for RFU/RFU_2 NC pins

UN100 MK2-H1.3MM BGA SYM 3 OF 4 OMIT_TABLE 998-24627

NC_UN100_C5	C5	RFU_2	
NC_UN100_C6	C6	RFU_2	
NC_UN100_C7	C7	RFU_2	
NC_UN100_C8	C8	RFU_2	
NC_UN100_C9	C9	RFU_2	
NC_UN100_D4	D4	RFU_2	
NC_UN100_D5	D5	RFU_2	
NC_UN100_D6	D6	RFU_2	
NC_UN100_D7	D7	RFU_2	
NC_UN100_D8	D8	RFU_2	
NC_UN100_D9	D9	RFU_2	
NC_UN100_D10	D10	RFU_2	
NC_UN100_D11	D11	RFU_2	
NC_UN100_D12	D12	RFU_2	
NC	Y11		
RFU_2	C10	NC_UN100_C10	
RFU_2	C11	NC_UN100_C11	
RFU	H10	NC_UN100_H10	
RFU	J10	NC_UN100_J10	
RFU	K6	NC_UN100_K6	
RFU	K10	NC_UN100_K10	
RFU	L5	NC_UN100_L5	
RFU	L6	NC_UN100_L6	
RFU	L10	NC_UN100_L10	
RFU	L11	NC_UN100_L11	
RFU	M10	NC_UN100_M10	

D NAND0 S5E1 Power/Gnd

UN100 MK2-H1.3MM BGA SYM 1 OF 4 OMIT_TABLE 998-24627

PP2V5_NAND0	E4, E12, F4, F12, T4, T12, U4, U12	VCC (VCC)
PP1V2_NAND0	G5, G11, H5, H11, P5, P11, R5, R11	VDDIO_1 (VCCQ_IO)
PP1V2_NAND0_S5E1_PCI_AVDD_H	P9, P10	PCIE_AVDD_H
PP1V2_NAND0_S5E1_AVDD1X_PLL	N6	AVDD1X_PLL
PP1V2_NAND0	G12, G4, H4, H12, K4, M12, P4, P12, R4, R12	VDDIO_2_L_ANI (VCCQ_ANI)
	K12, L4, L12, M4	VDDIO_2_DP
PP0V9_NAND0	J7, J9, K7, K9, M7, M9, N7, N9	VDD (VDD)
	P7, R7, R9	PCIE_VDD
PP0V9_NAND0_S5E1_VDD_PLL	M6	VDD_PLL
TP_NAND0_S5E1_VPP	E11	VPP
	H6	VQPS

VSS: B5, B6, B7, B8, B9, B10, B11, C4, C12, D3, D13, E3, E13, F3, F5, F11, F13, G3, G13, H3, H7, H8, H13, J3, J4, J5, J8, J11, J12, J13, K3, K8, K13, L3, L7, L8, L9, L13, M3, M8, M13, N3, N5, N8, N12, N13, P3, P8, P13, R3, R6, R8, R10, R13, T3, T5, T7, T9, T11, T13, U3, U5, U7, U9, U11, U13, V4, V5, V6, V7, V8, V9, V10, V11, V12

UN100 MK2-H1.3MM BGA SYM 4 OF 4 OMIT_TABLE 998-24627

A1	VSS/DUMMY	VSS/DUMMY	N15
A2	VSS/DUMMY	VSS/DUMMY	P1
A3	VSS/DUMMY	VSS/DUMMY	P2
A4	VSS/DUMMY	VSS/DUMMY	P14
A5	VSS/DUMMY	VSS/DUMMY	P15
A6	VSS/DUMMY	VSS/DUMMY	R1
A7	VSS/DUMMY	VSS/DUMMY	R2
A8	VSS/DUMMY	VSS/DUMMY	R14
A9	VSS/DUMMY	VSS/DUMMY	R15
A10	VSS/DUMMY	VSS/DUMMY	T1
A11	VSS/DUMMY	VSS/DUMMY	T2
A12	VSS/DUMMY	VSS/DUMMY	T14
A13	VSS/DUMMY	VSS/DUMMY	T15
A14	VSS/DUMMY	VSS/DUMMY	U1
A15	VSS/DUMMY	VSS/DUMMY	U2
B1	VSS/DUMMY	VSS/DUMMY	U14
B2	VSS/DUMMY	VSS/DUMMY	U15
B3	VSS/DUMMY	VSS/DUMMY	V1
B4	VSS/DUMMY	VSS/DUMMY	V2
B12	VSS/DUMMY	VSS/DUMMY	V3
B13	VSS/DUMMY	VSS/DUMMY	V13
B14	VSS/DUMMY	VSS/DUMMY	V14
B15	VSS/DUMMY	VSS/DUMMY	V15
C1	VSS/DUMMY	VSS/DUMMY	W1
C2	VSS/DUMMY	VSS/DUMMY	W2
C3	VSS/DUMMY	VSS/DUMMY	W3
C13	VSS/DUMMY	VSS/DUMMY	W4
C14	VSS/DUMMY	VSS/DUMMY	W5
C15	VSS/DUMMY	VSS/DUMMY	W6
D1	VSS/DUMMY	VSS/DUMMY	W7
D2	VSS/DUMMY	VSS/DUMMY	W8
D14	VSS/DUMMY	VSS/DUMMY	W9
D15	VSS/DUMMY	VSS/DUMMY	W10
E1	VSS/DUMMY	VSS/DUMMY	W11
E2	VSS/DUMMY	VSS/DUMMY	W12
E14	VSS/DUMMY	VSS/DUMMY	W13
E15	VSS/DUMMY	VSS/DUMMY	W14
F1	VSS/DUMMY	VSS/DUMMY	W15
F2	VSS/DUMMY	VSS/DUMMY	Y1
F14	VSS/DUMMY	VSS/DUMMY	Y2
F15	VSS/DUMMY	VSS/DUMMY	Y3
G1	VSS/DUMMY	VSS/DUMMY	Y4
G2	VSS/DUMMY	VSS/DUMMY	Y5
G14	VSS/DUMMY	VSS/DUMMY	Y6
G15	VSS/DUMMY	VSS/DUMMY	Y7
H1	VSS/DUMMY	VSS/DUMMY	Y8
H2	VSS/DUMMY	VSS/DUMMY	Y9
H14	VSS/DUMMY	VSS/DUMMY	Y10
H15	VSS/DUMMY	VSS/DUMMY	Y12
J1	VSS/DUMMY	VSS/DUMMY	Y13
J2	VSS/DUMMY	VSS/DUMMY	Y14
J14	VSS/DUMMY	VSS/DUMMY	Y15
J15	VSS/DUMMY	VSS/DUMMY	AA1
K1	VSS/DUMMY	VSS/DUMMY	AA2
K2	VSS/DUMMY	VSS/DUMMY	AA3
K14	VSS/DUMMY	VSS/DUMMY	AA4
K15	VSS/DUMMY	VSS/DUMMY	AA5
L1	VSS/DUMMY	VSS/DUMMY	AA6
L2	VSS/DUMMY	VSS/DUMMY	AA7
L14	VSS/DUMMY	VSS/DUMMY	AA8
L15	VSS/DUMMY	VSS/DUMMY	AA9
M1	VSS/DUMMY	VSS/DUMMY	AA10
M2	VSS/DUMMY	VSS/DUMMY	AA11
M14	VSS/DUMMY	VSS/DUMMY	AA12
M15	VSS/DUMMY	VSS/DUMMY	AA13
N1	VSS/DUMMY	VSS/DUMMY	AA14
N2	VSS/DUMMY	VSS/DUMMY	AA15
N14	VSS/DUMMY		

BOM_COST_GROUP=SSD

PAGE TITLE: STORAGE: SSD0 S5E MK2 <1>
Apple Inc.
DRAWING NUMBER: 051-08286
SIZE: D
REVISION: 5.0.3
BRANCH:
PAGE: 221 OF 700
SHEET: 113 OF 168

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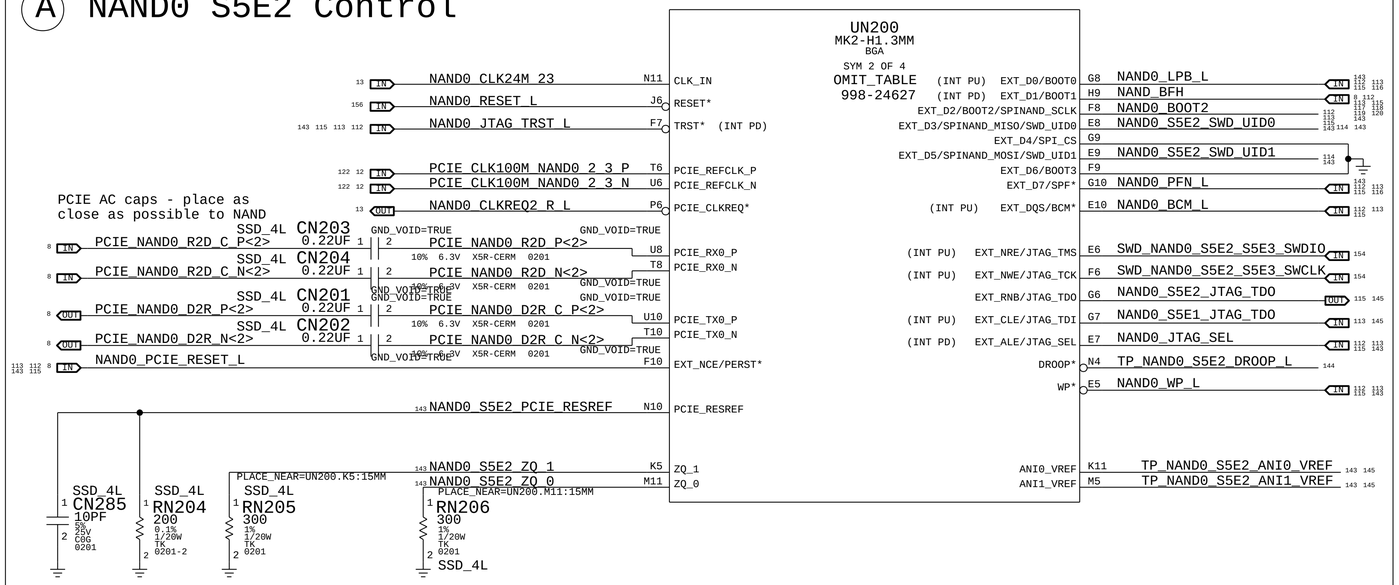
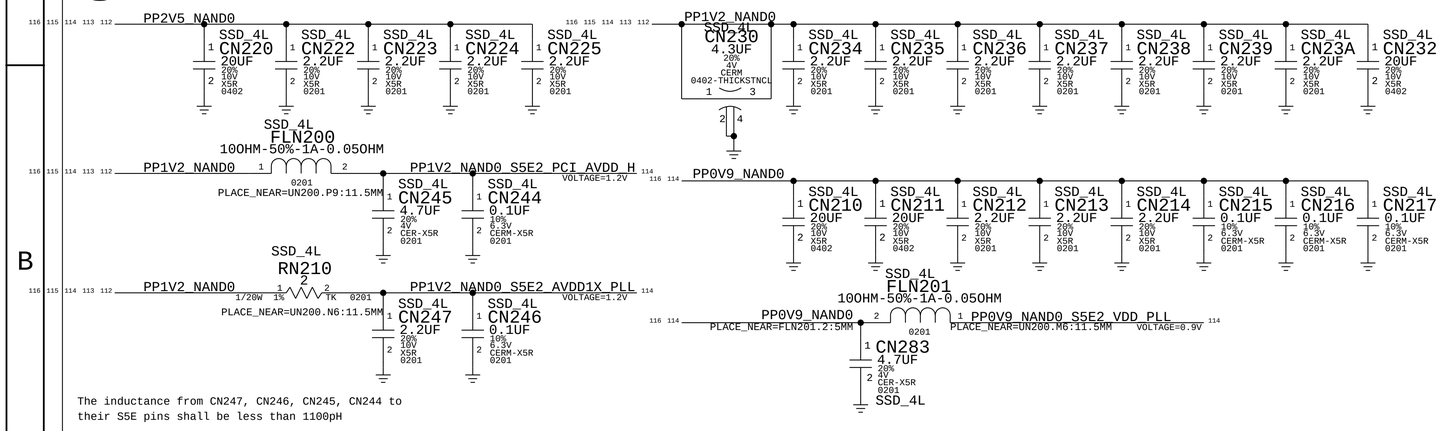
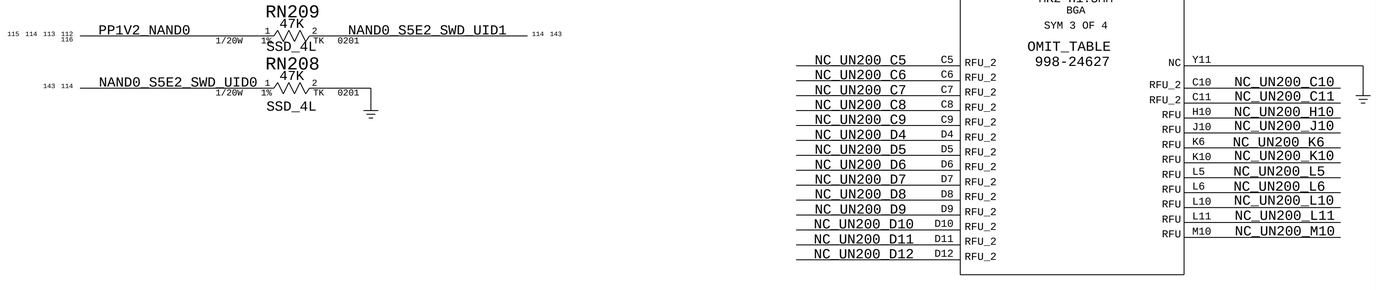
A NAND0 S5E2 Control



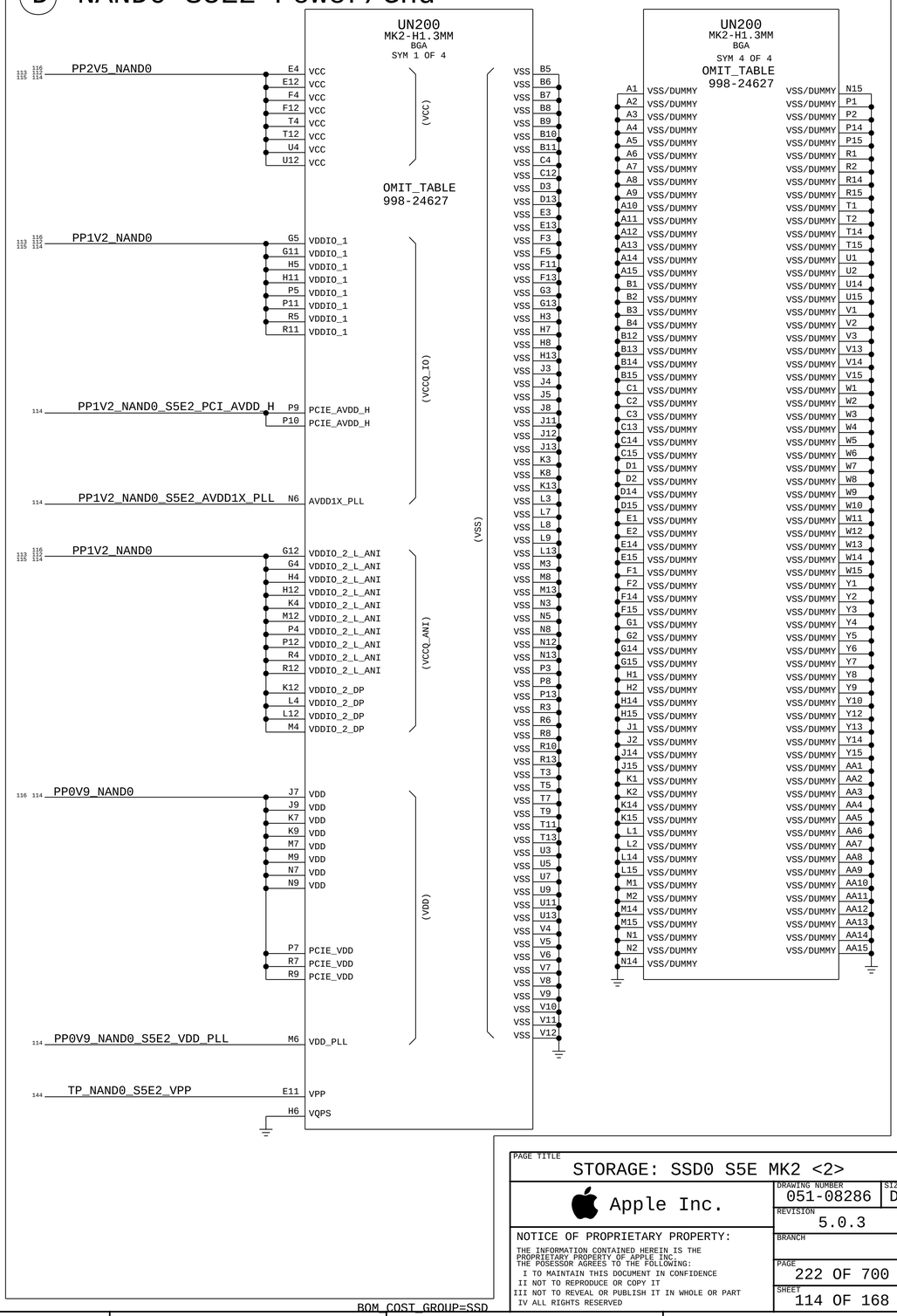
B NAND0 S5E2 Bulk Capacitance



C NAND0 S5E2 Bulk Miscellaneous



D NAND0 S5E2 Power/Gnd



BOM_COST_GROUP=SSD

PAGE TITLE	STORAGE: SSD0 S5E MK2 <2>
Apple Inc.	DRAWING NUMBER 051-08286 · SIZE D
	REVISION 5.0.3
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A NAND0 S5E3 Control

UN300
MK2-H1.3MM
BGA
SYM 2 OF 4
OMIT_TABLE
998-24627

13 IN NAND0_CLK24M_23 N11 CLK_IN
156 IN NAND0_RESET_L J6 RESET*
143 114 113 112 IN NAND0_JTAG_TRST_L F7 TRST* (INT PD)

12 IN PCIE_CLK100M_NAND0_2_3_P T6 PCIE_REFCLK_P
12 IN PCIE_CLK100M_NAND0_2_3_N U6 PCIE_REFCLK_N
13 OUT NAND0_CLKREQ3_R_L P6 PCIE_CLKREQ*

PCIE AC caps - place as close as possible to NAND

8 IN PCIE_NAND0_R2D_C_P<3> — SSD_4L CN303 0.22UF 10% 6.3V X5R-CERM 0201 — PCIE_NAND0_R2D_P<3> U8 PCIE_RX0_P
8 IN PCIE_NAND0_R2D_C_N<3> — SSD_4L CN304 0.22UF 10% 6.3V X5R-CERM 0201 — PCIE_NAND0_R2D_N<3> T8 PCIE_RX0_N
8 OUT PCIE_NAND0_D2R_P<3> — SSD_4L CN301 0.22UF 10% 6.3V X5R-CERM 0201 — PCIE_NAND0_D2R_C_P<3> U10 PCIE_TX0_P
8 OUT PCIE_NAND0_D2R_N<3> — SSD_4L CN302 0.22UF 10% 6.3V X5R-CERM 0201 — PCIE_NAND0_D2R_C_N<3> T10 PCIE_TX0_N
GND_VOID=TRUE
113 112 143 114 8 IN NAND0_PCIE_RESET_L F10 EXT_NCE/PERST*

143 NAND0_S5E3_PCIE_RESREF N10 PCIE_RESREF

SSD_4L CN385 10PF 5% 25V C0G 0201
SSD_4L RN304 200 0.1% 1/20W TK 0201-2
SSD_4L RN305 300 1% 1/20W TK 0201
PLACE_NEAR=UN300.K5:15MM
143 NAND0_S5E3_ZQ_1 K5 ZQ_1
143 NAND0_S5E3_ZQ_0 M11 ZQ_0
PLACE_NEAR=UN300.M11:15MM
SSD_4L RN306 300 1% 1/20W TK 0201

(INT PU) EXT_D0/BOOT0 G8 NAND0_LPB_L IN
(INT PD) EXT_D1/BOOT1 H9 NAND_BFH IN
EXT_D2/BOOT2/SPINAND_SCLK F8 NAND0_BOOT2 112 113 114 143
EXT_D3/SPINAND_MISO/SWD_UID0 E8 NAND0_S5E3_SWD_UID0 115 143
EXT_D4/SPI_CS G9
EXT_D5/SPINAND_MOSI/SWD_UID1 E9 NAND0_S5E3_SWD_UID1 115 143
EXT_D6/BOOT3 F9
EXT_D7/SPF* G10 NAND0_PFN_L IN
(INT PU) EXT_DQS/BCM* E10 NAND0_BCM_L IN

(INT PU) EXT_NRE/JTAG_TMS E6 SWD_NAND0_S5E2_S5E3_SWDIO IN 154
(INT PU) EXT_NWE/JTAG_TCK F6 SWD_NAND0_S5E2_S5E3_SWCLK IN 154
EXT_RNB/JTAG_TDO G6 TP_NAND0_S5E3_JTAG_TDO OUT 143
(INT PU) EXT_CLE/JTAG_TDI G7 NAND0_S5E2_JTAG_TDO IN 114 145
(INT PD) EXT_ALE/JTAG_SEL E7 NAND0_JTAG_SEL IN 112 113 114 143
DROOP* N4 TP_NAND0_S5E3_DROOP_L 144
WP* E5 NAND0_WP_L IN 112 113 114 143

ANI0_VREF K11 TP_NAND0_S5E3_ANI0_VREF 143 145
ANI1_VREF M5 TP_NAND0_S5E3_ANI1_VREF 143 145

B NAND0 S5E3 Bulk Capacitance

PP2V5_NAND0
SSD_4L CN320 20UF 20% 4V CERM 0402
SSD_4L CN322 2.2UF 20% 10V X5R 0201
SSD_4L CN323 2.2UF 20% 10V X5R 0201
SSD_4L CN324 2.2UF 20% 10V X5R 0201
SSD_4L CN325 2.2UF 20% 10V X5R 0201

PP1V2_NAND0
SSD_4L CN330 4.3UF 20% 4V CERM 0402-THICKSTNCL
SSD_4L CN334 2.2UF 20% 10V X5R 0201
SSD_4L CN335 2.2UF 20% 10V X5R 0201
SSD_4L CN336 2.2UF 20% 10V X5R 0201
SSD_4L CN337 2.2UF 20% 10V X5R 0201
SSD_4L CN338 2.2UF 20% 10V X5R 0201
SSD_4L CN339 2.2UF 20% 10V X5R 0201
SSD_4L CN33A 2.2UF 20% 10V X5R 0201
SSD_4L CN332 20UF 20% 10V X5R 0402

SSD_4L FLN300 10OHM-50%-1A-0.05OHM
PP1V2_NAND0 — 0201 — PP1V2_NAND0_S5E3_PCI_AVDD_H VOLTAGE=1.2V
PLACE_NEAR=UN300.P9:11.5MM
SSD_4L CN345 4.7UF 20% 4V CER-X5R 0201
SSD_4L CN344 0.1UF 10% 6.3V CERM-X5R 0201

SSD_4L RN310 2 1/20W 1% TK 0201
PP1V2_NAND0 — PP1V2_NAND0_S5E3_AVDD1X_PLL VOLTAGE=1.2V
PLACE_NEAR=UN300.N6:11.5MM
SSD_4L CN347 2.2UF 20% 10V X5R 0201
SSD_4L CN346 0.1UF 10% 6.3V CERM-X5R 0201

PP0V9_NAND0
SSD_4L CN310 20UF 20% 10V X5R 0402
SSD_4L CN311 20UF 20% 10V X5R 0402
SSD_4L CN312 2.2UF 20% 10V X5R 0201
SSD_4L CN313 2.2UF 20% 10V X5R 0201
SSD_4L CN314 2.2UF 20% 10V X5R 0201
SSD_4L CN315 0.1UF 10% 6.3V CERM-X5R 0201
SSD_4L CN316 0.1UF 10% 6.3V CERM-X5R 0201
SSD_4L CN317 0.1UF 10% 6.3V CERM-X5R 0201

SSD_4L FLN301 10OHM-50%-1A-0.05OHM
PP0V9_NAND0 — 0201 — PP0V9_NAND0_S5E3_VDD_PLL VOLTAGE=0.9V
PLACE_NEAR=FLN301.2:5MM PLACE_NEAR=UN300.M6:11.5MM
SSD_4L CN383 4.7UF 20% 2V CER-X5R 0201

The inductance from CN347, CN346, CN345, CN344 to their S5E pins shall be less than 1100pH

C NAND0 S5E3 Bulk Miscellaneous

PP1V2_NAND0 — SSD_4L RN308 47K 1/20W 1% TK 0201 — NAND0_S5E3_SWD_UID0 115 143
PP1V2_NAND0 — SSD_4L RN309 47K 1/20W 1% TK 0201 — NAND0_S5E3_SWD_UID1 115 143

PCB designers should add stiching vias for RFU/RFU_2 NC pins

UN300
MK2-H1.3MM
BGA
SYM 3 OF 4
OMIT_TABLE
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NC_UN300_C5 C5 RFU_2
NC_UN300_C6 C6 RFU_2
NC_UN300_C7 C7 RFU_2
NC_UN300_C8 C8 RFU_2
NC_UN300_C9 C9 RFU_2
NC_UN300_D4 D4 RFU_2
NC_UN300_D5 D5 RFU_2
NC_UN300_D6 D6 RFU_2
NC_UN300_D7 D7 RFU_2
NC_UN300_D8 D8 RFU_2
NC_UN300_D9 D9 RFU_2
NC_UN300_D10 D10 RFU_2
NC_UN300_D11 D11 RFU_2
NC_UN300_D12 D12 RFU_2

NC Y11
RFU_2 C10 NC_UN300_C10
RFU_2 C11 NC_UN300_C11
RFU H10 NC_UN300_H10
RFU J10 NC_UN300_J10
RFU K6 NC_UN300_K6
RFU K10 NC_UN300_K10
RFU L5 NC_UN300_L5
RFU L6 NC_UN300_L6
RFU L10 NC_UN300_L10
RFU L11 NC_UN300_L11
RFU M10 NC_UN300_M10

D NAND0 S5E3 Power/Gnd

PP2V5_NAND0 — E4 E12 F4 F12 T4 T12 U4 U12 VCC (VCC)
PP1V2_NAND0 — G5 G11 H5 H11 P5 P11 R5 R11 VDDIO_1 (VCCQ_IO)
PP1V2_NAND0_S5E3_PCI_AVDD_H — P9 P10 PCIE_AVDD_H
PP1V2_NAND0_S5E3_AVDD1X_PLL — N6 AVDD1X_PLL
PP1V2_NAND0 — G12 G4 H4 H12 K4 M12 P4 P12 R4 R12 VDDIO_2_L_ANI (VCCQ_ANI)
K12 L4 L12 M4 VDDIO_2_DP
PP0V9_NAND0 — J7 J9 K7 K9 M7 M9 N7 N9 VDD (VDD)
P7 R7 R9 PCIE_VDD
PP0V9_NAND0_S5E3_VDD_PLL — M6 VDD_PLL
TP_NAND0_S5E3_VPP — E11 VPP
H6 VQPS

OMIT_TABLE
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VSS B5 B6 B7 B8 B9 B10 B11 C4 C12 D3 D13 E3 E13 F3 F5 F11 F13 G3 G13 H3 H7 H8 H13 J3 J4 J5 J8 J11 J12 J13 K3 K8 K13 L3 L7 L8 L9 L13 M3 M8 M13 N3 N5 N8 N12 N13 P3 P8 P13 R3 R6 R8 R10 R13 T3 T5 T7 T9 T11 T13 U3 U5 U7 U9 U11 U13 V4 V5 V6 V7 V8 V9 V10 V11 V12 (VSS)

UN300
MK2-H1.3MM
BGA
SYM 4 OF 4
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A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 B1 B2 B3 B4 B12 B13 B14 B15 C1 C2 C3 C13 C14 C15 D1 D2 D14 D15 E1 E2 E14 E15 F1 F2 F14 F15 G1 G2 G14 G15 H1 H2 H14 H15 J1 J2 J14 J15 K1 K2 K14 K15 L1 L2 L14 L15 M1 M2 M14 M15 N1 N2 N14 VSS/DUMMY
N15 P1 P2 P14 P15 R1 R2 R14 R15 T1 T2 T14 T15 U1 U2 U14 U15 V1 V2 V3 V13 V14 V15 W1 W2 W3 W4 W5 W6 W7 W8 W9 W10 W11 W12 W13 W14 W15 Y1 Y2 Y3 Y4 Y5 Y6 Y7 Y8 Y9 Y10 Y12 Y13 Y14 Y15 AA1 AA2 AA3 AA4 AA5 AA6 AA7 AA8 AA9 AA10 AA11 AA12 AA13 AA14 AA15 VSS/DUMMY

BOM_COST_GROUP=SSD

PAGE TITLE
STORAGE: SSD0 S5E MK2 <3>

Apple Inc.

DRAWING NUMBER 051-08286
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REVISION 5.0.3
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A NAND0 NAND VCC (2.5V)

PPBUS_NAND0

CN479 27UF 20% 16V TANT-POLY CASE-B12 — 128S00107
CN480 27UF 20% 16V TANT-POLY CASE-B12 — 128S00107
CN481 27UF 20% 16V TANT-POLY CASE-B12 — 128S00107
CN482 27UF 20% 16V TANT-POLY CASE-B12 — 128S00107

PACK_OPTION=2V5_NAND_PBUS-B12-18V

CN483 2.2UF 20% 25V X6S-CERM 0402
CN484 2.2UF 20% 25V X6S-CERM 0402
CN485 2.2UF 20% 25V X6S-CERM 0402
CN486 2.2UF 20% 25V X6S-CERM 0402

CN479 33UF 20% 16V TANT CASE-T — 128S00009
CN480 33UF 20% 16V TANT CASE-T — 128S00009
CN481 33UF 20% 16V TANT CASE-T — 128S00009
CN482 33UF 20% 16V TANT CASE-T — 128S00009

PACK_OPTION=2V5_NAND_PBUS-B12-16V
PACK_IGNORE=TRUE

CN480 33UF 20% 16V TANT CASED12-SM
CN481 33UF 20% 16V TANT CASED12-SM
CN480 68UF 20% 16V POLY-TANT CASE-D2E-SM
CN481 68UF 20% 16V POLY-TANT CASE-D2E-SM

PACK_OPTION=2V5_NAND_PBUS-D12
PACK_IGNORE=TRUE

PACK_OPTION=2V5_NAND_PBUS-D2E
PACK_IGNORE=TRUE

P2V5_NAND0_EN — RN488 0 1/20W 0% TK 0201 — P2V5_NAND0_EN_R

UN480
LT8642-1
LQFN-THICKSTNCL
CRITICAL

4	VIN	
5	VIN	
12	VIN	
13	VIN	
14	EN/UV	P2V5_NAND0_EN_R
19	VC	P2V5_NAND0_VC
1	PG	P2V5_NAND0_PGOOD
20	FB	P2V5_NAND0_FB
18	SS	P2V5_NAND0_SS
17	RT	P2V5_NAND0_RT
15	SYNC/MODE	
2	BIAS	P2V5_NAND0_BIAS
3	INTVCC	P2V5_NAND0_INTVCC, VOLTAGE=2.5V
7	BST	P2V5_NAND0_BST, SWITCH_NODE=TRUE, DIDT=TRUE
8	SW	
9	SW	
10	SW	P2V5_NAND0_SW, SWITCH_NODE=TRUE, DIDT=TRUE, MIN_NECK_WIDTH=0.1000, MIN_LINE_WIDTH=0.2000
16	CLKOUT	NC
6, 11, 21	GND	
22, 23, 24, 25	NC	

P2V5_NAND0_VC_R

RN481 18K 1% 1/20W TK 0201-1
CN488 1000PF 10% 16V X7R-1 0201 — NO_XNET_CONNECTION=1
CN489 56PF 5% 25V NP0-C0G 0201 — NO_XNET_CONNECTION=1
CN487 1.2NF ±10% 10V CERM 0201-1 — NO_XNET_CONNECTION=1
SOFT START TIME SET TO: 0.42/0.63/1.1 ms (min / typ / max)
RN480 25.5K 1% 1/20W TK 0201 — NO_XNET_CONNECTION=1
FREQUENCY SET TO: 1.5MHz
XWN480 SM — NO_XNET_CONNECTION=1
AGND_P2V5_NAND0

RN485 27.4K 0.1% 1/20W TK 0201
RN484 82.5K 0.1% 1/20W TK 0201 — P2V5_NAND0_FB_RC2
RN483 6.98K 1% 1/20W TK 0201

P2V5_NAND0_FB
CN493 1000PF 10% 16V X7R-1 0201 — P2V5_NAND0_FB_C
RN486 10K 1% 1/20W TK 0201 — P2V5_NAND0_FB_RC

CN490 2.2UF 20% 25V X6S-CERM 0402
RN492 1.5 5% 1/20W TK 0201 — P2V5_NAND0_BST_R — SWITCH_NODE=TRUE, DIDT=TRUE
CN492 47NF 10% 10V X6S-CERM 0201

RN487 0 1/20W 0% TK 0201 — PPVIN_P3V8NAND0
CN491 2.2UF 20% 25V X6S-CERM 0402
P2V5_NAND0_PGOOD
RN412 100K 1% 1/20W TK 0201

LN480 0.56UH-20%-16A-0.0072OHM PILA052D-SM — PP2V5_NAND0
XWN481 SM — NO_XNET_CONNECTION=1
P2V5_NAND0_FB_XW
RN482 10 5% 1/20W TK 0201

CN494 150UF 20% 6.3V TANT CASE-B-SM
CN495 150UF 20% 6.3V TANT CASE-B-SM
CN496 150UF 20% 6.3V TANT CASE-B-SM
CN498 10UF 20% 6.3V CER-X6S 0402
CN499 10UF 20% 6.3V CER-X6S 0402

B NAND0 Ocarina

PPVIN_P3V8NAND0

CN400 10UF 20% 6.3V CERM-X6S 0402
CN401 10UF 20% 6.3V CERM-X6S 0402
CN402 0.1UF 20% 16V X6S-CERM 0201
CN403 4.7UF 20% 6.3V X6S 0402
CN404 4.7UF 20% 6.3V X6S 0402
CN405 0.1UF 20% 16V X6S-CERM 0201
CN406 150UF 20% 6.3V TANT-POLY CASE-B3-1 — CRITICAL

PLACE CN400-CN402 NEAR OCARINA PINS E7/E8
PLACE CN403-CN405 NEAR OCARINA PINS A7/A8
PLACE CN406 NEAR OCARINA PIN B4

OCARINA I2C BASE ADDRESS
STG0: F2
STG1: F0

PPVDD_LDO_NAND0_OCARINA, VOLTAGE=2.5V
CN407 0.22UF 20% 6.3V X6S-CERM 0201
TP_NAND0_OCARINA_VCC_DET
PP1V8_S2
CN409 0.1UF 10% 6.3V CERM-X5R 0201

UN400
D2499A0P0VLAVBC2
WLCSP

338S00600
CRITICAL
OMIT_TABLE

F3	ATM	
D2	ADDR	NAND0_STG01_ADDR — RN406 10K 5% 1/20W TK 0201 — PPVIN_P3V8NAND0
E1	FORCE_EN	NAND0_FORCE_EN — RN411 100K 1% 1/20W TK 0201 — PPVIN_P3V8NAND0
G2	I2C_SCL	I2C_NAND_PMIC_SCL_1V8
G3	I2C_SDA	I2C_NAND_PMIC_SDA_1V8
F4	LPBN	NAND0_LPB_L — RN419 47K 1% 1/20W TK 0201 — PP1V2_NAND0
G5	PFN*	NAND0_PFN_L — RN417 47K 1% 1/20W TK 0201 — PP1V2_NAND0
G6	PGOOD	NAND0_OCARINA_PGOOD — RN410 100K 1% 1/20W TK 0201 — PPVIN_P3V8NAND0
D1	PMIC_RESET*	PPVIN_P3V8NAND0
D3	POK1	P2V5_NAND0_PGOOD
F1	POK2	
E5	RESET*	NAND0_RESET_L — RN418 47K 1% 1/20W TK 0201 — PP1V2_NAND0
F2	SYS_ALIVE	PMU_SYS_ALIVE
F5	VEN1	P2V5_NAND0_EN
E4	VEN2/PMIC_CTRL	TP_NAND0_OCARINA_VEN2
G4	WP*	NC_NAND0_OCARINA_WP_L

VDD_BUCK0 (E8, E7), VDD_BUCK1 (A8, A7), VDD_MAIN (B4), VDD_LDO (B5), VCC_DET (G1), V_BUF_1.8V (C1)

TCAL A4 — NAND0_OCARINA_TCAL
VREF B3 — NAND0_OCARINA_VREF
IREF B2 — NAND0_OCARINA_IREF
TDEV1 B1 — NAND0_OCARINA_TDEV1
TDEV2 C2 — NAND0_OCARINA_TDEV2
VR1_DISCHG A3 — PP2V5_NAND0
VR2_DISCHG A1

RN405 200K 1% 1/20W TK 0201
CN408 0.1UF 10% 6.3V CERM-X5R 0201
RN400 8.06K 0.1% 1/20W TK 0201-1

BUCK0_FB_DIS D5 — PP0V9_NAND0_FB_DIS, VOLTAGE=0.9V
BUCK1_FB_DIS C5 — PP1V2_NAND0_FB_DIS

RN420 0 1/20W TK 0201 — PP0V9_NAND0
RN430 0 1/20W TK 0201 — PP1V2_NAND0

BUCK0_LX0 F8, BUCK0_LX0 F7 — VOLTAGE=1.2V
P0V9_LX0_NAND0, DIDT=TRUE, SWITCH_NODE=TRUE
LN421 1UH-20%-4.8A-0.032OHM 1210

BUCK0_LX1 D8, BUCK0_LX1 D7
P0V9_LX1_NAND0, DIDT=TRUE, SWITCH_NODE=TRUE
CRITICAL LN420 0.47UH-20%-6.7A-0.023OHM 1210

BUCK1_LX0 B8, BUCK1_LX0 B7
P1V2_LX0_NAND0, DIDT=TRUE, SWITCH_NODE=TRUE
CRITICAL LN430 0.47UH-20%-6.7A-0.023OHM 1210

CN420 20UF 20% 10V X5R 0402 — MIRROR_WITH=CN42A — PP0V9_NAND0
CN421 20UF 20% 10V X5R 0402 — MIRROR_WITH=CN42A
CN422 20UF 20% 10V X5R 0402 — MIRROR_WITH=CN42A
CN423 20UF 20% 10V X5R 0402 — MIRROR_WITH=CN42A
CN424 20UF 20% 10V X5R 0402 — MIRROR_WITH=CN42A
CN425 20UF 20% 10V X5R 0402 — MIRROR_WITH=CN42A
CN426 20UF 20% 10V X5R 0402 — MIRROR_WITH=CN42A
CN427 20UF 20% 10V X5R 0402 — MIRROR_WITH=CN42A
CN428 20UF 20% 10V X5R 0402 — MIRROR_WITH=CN42A
CN429 20UF 20% 10V X5R 0402 — MIRROR_WITH=CN42A
CN42A 20UF 20% 10V X5R 0402 — MIRROR_WITH=CN42A
CN42B 20UF 20% 10V X5R 0402 — MIRROR_WITH=CN42A

CN430 20UF 20% 10V X5R 0402 — MIRROR_WITH=CN43B — PP1V2_NAND0
CN431 20UF 20% 10V X5R 0402 — MIRROR_WITH=CN43B
CN432 20UF 20% 10V X5R 0402 — MIRROR_WITH=CN43B
CN433 20UF 20% 10V X5R 0402 — MIRROR_WITH=CN43B
CN434 20UF 20% 10V X5R 0402 — MIRROR_WITH=CN43B
CN435 20UF 20% 10V X5R 0402 — MIRROR_WITH=CN43B
CN436 20UF 20% 10V X5R 0402 — MIRROR_WITH=CN43B
CN437 20UF 20% 10V X5R 0402 — MIRROR_WITH=CN43B
CN438 20UF 20% 10V X5R 0402 — MIRROR_WITH=CN43B
CN439 20UF 20% 10V X5R 0402 — MIRROR_WITH=CN43B

Temperature Sensors

NAND0_OCARINA_TDEV1 — RN402 100K-1%-0.001A 0201 — RN401 18.2K 0.1% 1/20W TK 0201-1
NAND0_OCARINA_TDEV2 — RN404 100K-1%-0.001A 0201 — RN403 18.2K 0.1% 1/20W TK 0201-1

C NAND0 Power Aliases

PP2V5_NAND0 = PP2V5_NAND0, VOLTAGE=2.5V, MAKE_BASE=TRUE = PP2V5_NAND0
PP1V2_NAND0 = PP1V2_NAND0, VOLTAGE=1.2V, MAKE_BASE=TRUE = PP1V2_NAND0
PP0V9_NAND0 = PP0V9_NAND0, VOLTAGE=0.9V, MAKE_BASE=TRUE = PP0V9_NAND0 = PP0V9_NAND0 = PP0V9_NAND0 = PP0V9_NAND0

BOM_COST_GROUP=SSD

PAGE TITLE: STORAGE: SSD0 OCARINA & NAND VCC

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A NAND1 S5E0 Control

UN500
MK2-H1.3MM
BGA
SYM 2 OF 4
OMIT_TABLE
998-24627

13 IN	NAND1_CLK24M_01	N11	CLK_IN		
156 IN	NAND1_RESET_L	J6	RESET*		
143 120 119 118 117 IN	NAND1_JTAG_TRST_L	F7	TRST* (INT PD)		
122 12 IN	PCIE_CLK100M_NAND1_0_1_P	T6	PCIE_REFCLK_P		
122 12 IN	PCIE_CLK100M_NAND1_0_1_N	U6	PCIE_REFCLK_N		
13 OUT	NAND1_CLKREQ0_R_L	P6	PCIE_CLKREQ*		
				(INT PU) EXT_D0/BOOT0	G8 NAND1_LPB_L IN 143 110 120 115 118 112 121
				(INT PD) EXT_D1/BOOT1	H9 NAND_BFH IN 143 117 113 114
				EXT_D2/BOOT2/SPINAND_SCLK	F8 NAND1_BOOT2 117 118 119 120 143
				EXT_D3/SPINAND_MISO/SWD_UID0	E8 NAND1_S5E0_SWD_UID0 117 143
				EXT_D4/SPI_CS	G9
				EXT_D5/SPINAND_MOSI/SWD_UID1	E9 NAND1_S5E0_SWD_UID1 117 143
				EXT_D6/BOOT3	F9
				EXT_D7/SPF*	G10 NAND1_PFN_L IN 143 118 119 121
				(INT PU) EXT_DQS/BCM*	E10 NAND1_BCM_L IN 117 118 119 120
				(INT PU) EXT_NRE/JTAG_TMS	E6 SWD_NAND1_S5E0_S5E1_SWDIO IN 154
				(INT PU) EXT_NWE/JTAG_TCK	F6 SWD_NAND1_S5E0_S5E1_SWCLK IN 154
				EXT_RNB/JTAG_TDO	G6 NAND1_S5E0_JTAG_TDO OUT 118 145
				(INT PU) EXT_CLE/JTAG_TDI	G7 TP_NAND1_S5E0_JTAG_TDI IN 143
				(INT PD) EXT_ALE/JTAG_SEL	E7 NAND1_JTAG_SEL IN 143 117 118 119 120
				DROOP*	N4 TP_NAND1_S5E0_DROOP_L 144
				WP*	E5 NAND1_WP_L IN 143 118 119 120
8 IN	PCIE_NAND1_R2D_C_P<0>		SSD_8L CN503 0.22UF 10% 6.3V X5R-CERM 0201 GND_VOID=TRUE	PCIE_NAND1_R2D_P<0>	U8 PCIE_RX0_P
8 IN	PCIE_NAND1_R2D_C_N<0>		SSD_8L CN504 0.22UF 10% 6.3V X5R-CERM 0201 GND_VOID=TRUE	PCIE_NAND1_R2D_N<0>	T8 PCIE_RX0_N
8 OUT	PCIE_NAND1_D2R_P<0>		SSD_8L CN501 0.22UF 10% 6.3V X5R-CERM 0201 GND_VOID=TRUE	PCIE_NAND1_D2R_C_P<0>	U10 PCIE_TX0_P
8 OUT	PCIE_NAND1_D2R_N<0>		SSD_8L CN502 0.22UF 10% 6.3V X5R-CERM 0201 GND_VOID=TRUE	PCIE_NAND1_D2R_C_N<0>	T10 PCIE_TX0_N
110 118 143 120 8 IN	NAND1_PCIE_RESET_L				F10 EXT_NCE/PERST*
				NAND1_S5E0_PCIE_RESREF 143	N10 PCIE_RESREF
				NAND1_S5E0_ZQ_1 143 PLACE_NEAR=UN500.K5:15MM	K5 ZQ_1
				NAND1_S5E0_ZQ_0 143 PLACE_NEAR=UN500.M11:15MM	M11 ZQ_0
				ANI0_VREF	K11 TP_NAND1_S5E0_ANI0_VREF 143 145
				ANI1_VREF	M5 TP_NAND1_S5E0_ANI1_VREF 143 145

PCIE AC caps - place as close as possible to NAND

SSD_8L CN585 10PF 5% 25V C0G 0201
SSD_8L RN504 200 0.1% 1/20W TK 0201-2
SSD_8L RN505 300 1% 1/20W TK 0201
SSD_8L RN506 300 1% 1/20W TK 0201

B NAND1 S5E0 Bulk Capacitance

PP2V5_NAND1 (121 120 119 118 117)
SSD_8L CN520 20UF 20% 10V X5R 0402
SSD_8L CN522 2.2UF 20% 10V X5R 0201
SSD_8L CN523 2.2UF 20% 10V X5R 0201
SSD_8L CN524 2.2UF 20% 10V X5R 0201
SSD_8L CN525 2.2UF 20% 10V X5R 0201

SSD_8L FLN500 10OHM-50%-1A-0.05OHM
PP1V2_NAND1 (121 120 119 118 117) — 0201 — PP1V2_NAND1_S5E0_PCI_AVDD_H (117) VOLTAGE=1.2V
PLACE_NEAR=UN500.P9:11.5MM

SSD_8L CN545 4.7UF 20% 4V CER-X5R 0201
SSD_8L CN544 0.1UF 10% 6.3V CERM-X5R 0201

SSD_8L RN510 2
PP1V2_NAND1 (121 120 119 118 117) — 1/20W 1% TK 0201 — PP1V2_NAND1_S5E0_AVDD1X_PLL (117) VOLTAGE=1.2V
PLACE_NEAR=UN500.N6:11.5MM

SSD_8L CN547 2.2UF 20% 10V X5R 0201
SSD_8L CN546 0.1UF 10% 6.3V CERM-X5R 0201

PP1V2_NAND1 (121 120 119 118 117)
SSD_8L CN530 4.3UF 20% 4V CERM 0402-THICKSTNCL
SSD_8L CN534 2.2UF 20% 10V X5R 0201
SSD_8L CN535 2.2UF 20% 10V X5R 0201
SSD_8L CN536 2.2UF 20% 10V X5R 0201
SSD_8L CN537 2.2UF 20% 10V X5R 0201
SSD_8L CN538 2.2UF 20% 10V X5R 0201
SSD_8L CN539 2.2UF 20% 10V X5R 0201
SSD_8L CN53A 2.2UF 20% 10V X5R 0201
SSD_8L CN532 20UF 20% 10V X5R 0402

PP0V9_NAND1 (117)
SSD_8L CN510 20UF 20% 10V X5R 0402
SSD_8L CN511 20UF 20% 10V X5R 0402
SSD_8L CN512 2.2UF 20% 10V X5R 0201
SSD_8L CN513 2.2UF 20% 10V X5R 0201
SSD_8L CN514 2.2UF 20% 10V X5R 0201
SSD_8L CN515 0.1UF 10% 6.3V CERM-X5R 0201
SSD_8L CN516 0.1UF 10% 6.3V CERM-X5R 0201
SSD_8L CN517 0.1UF 10% 6.3V CERM-X5R 0201

SSD_8L FLN501 10OHM-50%-1A-0.05OHM
PP0V9_NAND1 (117) — 0201 — PP0V9_NAND1_S5E0_VDD_PLL (117) VOLTAGE=0.9V
PLACE_NEAR=FLN501.2:5MM PLACE_NEAR=UN500.M6:11.5MM

SSD_8L CN583 4.7UF 20% 4V CER-X5R 0201

The inductance from CN547, CN546, CN545, CN544 to their S5E pins shall be less than 1100pH

C NAND1 S5E0 Bulk Miscellaneous

Spec recommends to tie BCM, WP directly to 1.2V rail

PP1V2_NAND1 (121 120 119 118 117)
SSD_8L RN501 0 1/20W 0% TK 0201 — NAND1_BCM_L (117 118 119 120)
SSD_8L RN507 0 1/20W 0% TK 0201 — NAND1_WP_L (117 118 119 120 143)

Spec recommends to tie Boot2 directly to Gnd

143 120 119 118 117	NAND1_BOOT2	SSD_8L RN521 0 1/20W 0% TK 0201	
143 120 119 118 117	NAND1_JTAG_SEL	SSD_8L RN502 47K 1/20W 1% TK 0201	
143 120 119 118 117	NAND1_JTAG_TRST_L	SSD_8L RN500 47K 1/20W 1% TK 0201	
143 117	NAND1_S5E0_SWD_UID0	SSD_8L RN508 47K 1/20W 1% TK 0201	
143 117	NAND1_S5E0_SWD_UID1	SSD_8L RN509 47K 1/20W 1% TK 0201	

PCB designers should add stiching vias for RFU/RFU_2 NC pins

UN500
MK2-H1.3MM
BGA
SYM 3 OF 4
OMIT_TABLE
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NC_UN500_C5	C5	RFU_2	
NC_UN500_C6	C6	RFU_2	
NC_UN500_C7	C7	RFU_2	
NC_UN500_C8	C8	RFU_2	
NC_UN500_C9	C9	RFU_2	
NC_UN500_D4	D4	RFU_2	
NC_UN500_D5	D5	RFU_2	
NC_UN500_D6	D6	RFU_2	
NC_UN500_D7	D7	RFU_2	
NC_UN500_D8	D8	RFU_2	
NC_UN500_D9	D9	RFU_2	
NC_UN500_D10	D10	RFU_2	
NC_UN500_D11	D11	RFU_2	
NC_UN500_D12	D12	RFU_2	
NC	Y11		
RFU_2	C10	NC_UN500_C10	
RFU_2	C11	NC_UN500_C11	
RFU	H10	NC_UN500_H10	
RFU	J10	NC_UN500_J10	
RFU	K6	NC_UN500_K6	
RFU	K10	NC_UN500_K10	
RFU	L5	NC_UN500_L5	
RFU	L6	NC_UN500_L6	
RFU	L10	NC_UN500_L10	
RFU	L11	NC_UN500_L11	
RFU	M10	NC_UN500_M10	

D NAND1 S5E0 Power/Gnd

UN500
MK2-H1.3MM
BGA
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PP2V5_NAND1 (121 117 118 119 120)	E4 VCC		
	E12 VCC		
	F4 VCC		
	F12 VCC		
	T4 VCC		
	T12 VCC		
	U4 VCC		
	U12 VCC		
PP1V2_NAND1 (121 117 118 119 120)	G5 VDDIO_1		
	G11 VDDIO_1		
	H5 VDDIO_1		
	H11 VDDIO_1		
	P5 VDDIO_1		
	P11 VDDIO_1		
	R5 VDDIO_1		
	R11 VDDIO_1		
117 PP1V2_NAND1_S5E0_PCI_AVDD_H	P9 PCIE_AVDD_H		
	P10 PCIE_AVDD_H		
117 PP1V2_NAND1_S5E0_AVDD1X_PLL	N6 AVDD1X_PLL		
PP1V2_NAND1 (121 117 118 119 120)	G12 VDDIO_2_L_ANI		
	G4 VDDIO_2_L_ANI		
	H4 VDDIO_2_L_ANI		
	H12 VDDIO_2_L_ANI		
	K4 VDDIO_2_L_ANI		
	M12 VDDIO_2_L_ANI		
	P4 VDDIO_2_L_ANI		
	P12 VDDIO_2_L_ANI		
	R4 VDDIO_2_L_ANI		
	R12 VDDIO_2_L_ANI		
	K12 VDDIO_2_DP		
	L4 VDDIO_2_DP		
	L12 VDDIO_2_DP		
	M4 VDDIO_2_DP		
121 117 PP0V9_NAND1	J7 VDD		
	J9 VDD		
	K7 VDD		
	K9 VDD		
	M7 VDD		
	M9 VDD		
	N7 VDD		
	N9 VDD		
	P7 PCIE_VDD		
	R7 PCIE_VDD		
	R9 PCIE_VDD		
117 PP0V9_NAND1_S5E0_VDD_PLL	M6 VDD_PLL		
144 TP_NAND1_S5E0_VPP	E11 VPP		
	H6 VQPS		

(VCC) (VCCQ_IO) (VCCQ_ANI) (VDD) (VSS)

UN500
MK2-H1.3MM
BGA
SYM 4 OF 4
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A1	VSS/DUMMY	VSS/DUMMY	N15
A2	VSS/DUMMY	VSS/DUMMY	P1
A3	VSS/DUMMY	VSS/DUMMY	P2
A4	VSS/DUMMY	VSS/DUMMY	P14
A5	VSS/DUMMY	VSS/DUMMY	P15
A6	VSS/DUMMY	VSS/DUMMY	R1
A7	VSS/DUMMY	VSS/DUMMY	R2
A8	VSS/DUMMY	VSS/DUMMY	R14
A9	VSS/DUMMY	VSS/DUMMY	R15
A10	VSS/DUMMY	VSS/DUMMY	T1
A11	VSS/DUMMY	VSS/DUMMY	T2
A12	VSS/DUMMY	VSS/DUMMY	T14
A13	VSS/DUMMY	VSS/DUMMY	T15
A14	VSS/DUMMY	VSS/DUMMY	U1
A15	VSS/DUMMY	VSS/DUMMY	U2
B1	VSS/DUMMY	VSS/DUMMY	U14
B2	VSS/DUMMY	VSS/DUMMY	U15
B3	VSS/DUMMY	VSS/DUMMY	V1
B4	VSS/DUMMY	VSS/DUMMY	V2
B12	VSS/DUMMY	VSS/DUMMY	V3
B13	VSS/DUMMY	VSS/DUMMY	V13
B14	VSS/DUMMY	VSS/DUMMY	V14
B15	VSS/DUMMY	VSS/DUMMY	V15
C1	VSS/DUMMY	VSS/DUMMY	W1
C2	VSS/DUMMY	VSS/DUMMY	W2
C3	VSS/DUMMY	VSS/DUMMY	W3
C13	VSS/DUMMY	VSS/DUMMY	W4
C14	VSS/DUMMY	VSS/DUMMY	W5
C15	VSS/DUMMY	VSS/DUMMY	W6
D1	VSS/DUMMY	VSS/DUMMY	W7
D2	VSS/DUMMY	VSS/DUMMY	W8
D14	VSS/DUMMY	VSS/DUMMY	W9
D15	VSS/DUMMY	VSS/DUMMY	W10
E1	VSS/DUMMY	VSS/DUMMY	W11
E2	VSS/DUMMY	VSS/DUMMY	W12
E14	VSS/DUMMY	VSS/DUMMY	W13
E15	VSS/DUMMY	VSS/DUMMY	W14
F1	VSS/DUMMY	VSS/DUMMY	W15
F2	VSS/DUMMY	VSS/DUMMY	Y1
F14	VSS/DUMMY	VSS/DUMMY	Y2
F15	VSS/DUMMY	VSS/DUMMY	Y3
G1	VSS/DUMMY	VSS/DUMMY	Y4
G2	VSS/DUMMY	VSS/DUMMY	Y5
G14	VSS/DUMMY	VSS/DUMMY	Y6
G15	VSS/DUMMY	VSS/DUMMY	Y7
H1	VSS/DUMMY	VSS/DUMMY	Y8
H2	VSS/DUMMY	VSS/DUMMY	Y9
H14	VSS/DUMMY	VSS/DUMMY	Y10
H15	VSS/DUMMY	VSS/DUMMY	Y12
J1	VSS/DUMMY	VSS/DUMMY	Y13
J2	VSS/DUMMY	VSS/DUMMY	Y14
J14	VSS/DUMMY	VSS/DUMMY	Y15
J15	VSS/DUMMY	VSS/DUMMY	AA1
K1	VSS/DUMMY	VSS/DUMMY	AA2
K2	VSS/DUMMY	VSS/DUMMY	AA3
K14	VSS/DUMMY	VSS/DUMMY	AA4
K15	VSS/DUMMY	VSS/DUMMY	AA5
L1	VSS/DUMMY	VSS/DUMMY	AA6
L2	VSS/DUMMY	VSS/DUMMY	AA7
L14	VSS/DUMMY	VSS/DUMMY	AA8
L15	VSS/DUMMY	VSS/DUMMY	AA9
M1	VSS/DUMMY	VSS/DUMMY	AA10
M2	VSS/DUMMY	VSS/DUMMY	AA11
M14	VSS/DUMMY	VSS/DUMMY	AA12
M15	VSS/DUMMY	VSS/DUMMY	AA13
N1	VSS/DUMMY	VSS/DUMMY	AA14
N2	VSS/DUMMY	VSS/DUMMY	AA15
N14	VSS/DUMMY		

BOM_COST_GROUP=SSD

PAGE TITLE
STORAGE: SSD1 S5E MK2 <0>

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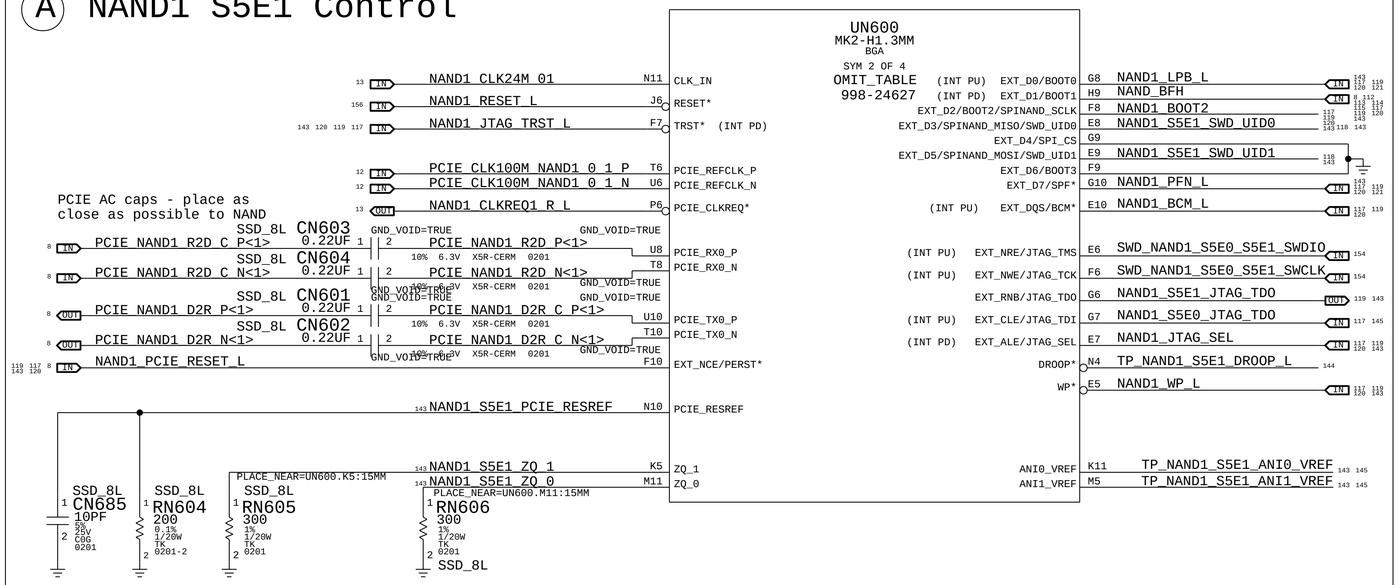
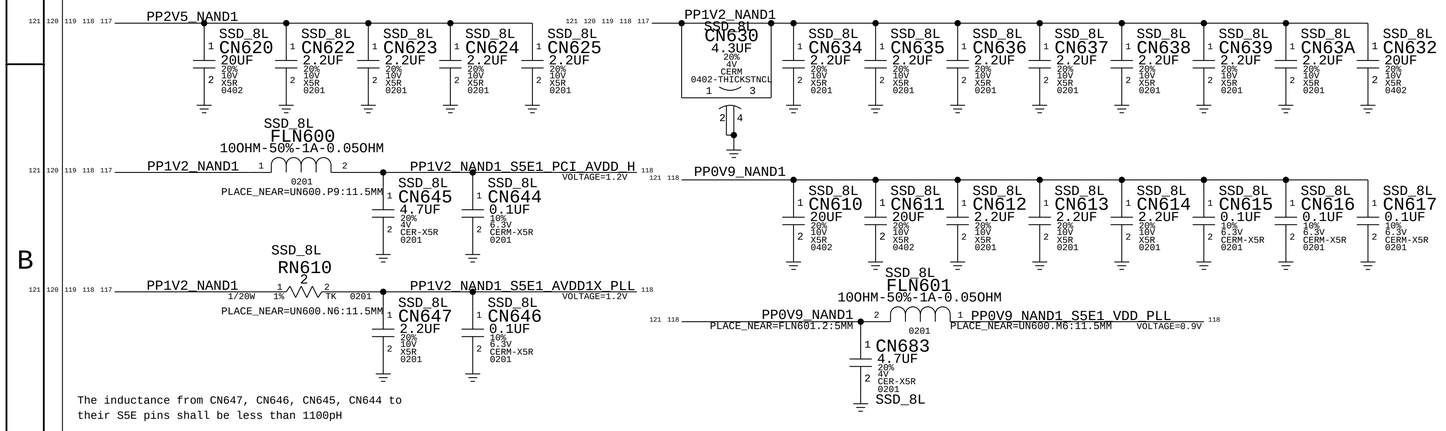
A NAND1 S5E1 Control

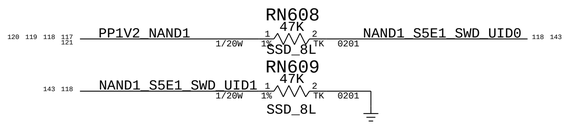


B NAND1 S5E1 Bulk Capacitance

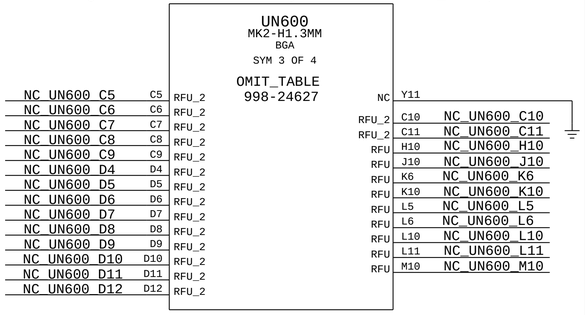


The inductance from CN647, CN646, CN645, CN644 to their S5E pins shall be less than 1100pH

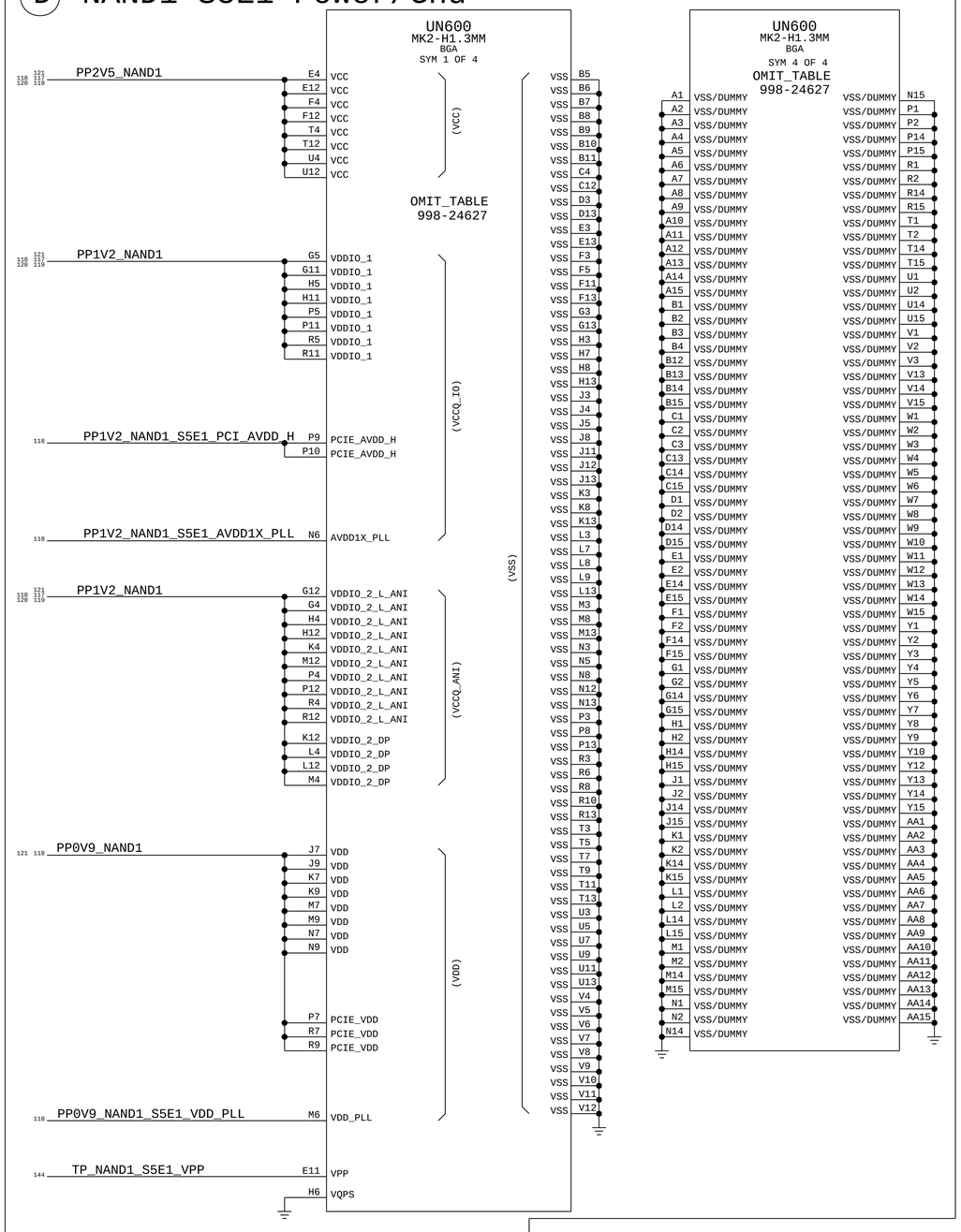
C NAND1 S5E1 Bulk Miscellaneous



PCB designers should add stiching vias for RFU/RFU_2 NC pins



D NAND1 S5E1 Power/Gnd



BOM_COST_GROUP=SSD

PAGE TITLE	STORAGE: SSD1 S5E MK2 <1>
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A NAND1 S5E2 Control

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NAND1_CLK24M_23 → CLK_IN (N11)
NAND1_RESET_L → RESET* (J6)
NAND1_JTAG_TRST_L → TRST* (INT PD) (F7)
PCIE_CLK100M_NAND1_2_3_P → PCIE_REFCLK_P (T6)
PCIE_CLK100M_NAND1_2_3_N → PCIE_REFCLK_N (U6)
NAND1_CLKREQ2_R_L → PCIE_CLKREQ* (P6)

PCIE AC caps - place as close as possible to NAND

PCIE_NAND1_R2D_C_P<2>	SSD_8L CN703	0.22UF	PCIE_NAND1_R2D_P<2>	U8 PCIE_RX0_P
PCIE_NAND1_R2D_C_N<2>	SSD_8L CN704	0.22UF	PCIE_NAND1_R2D_N<2>	T8 PCIE_RX0_N
PCIE_NAND1_D2R_P<2>	SSD_8L CN701	0.22UF	PCIE_NAND1_D2R_C_P<2>	U10 PCIE_TX0_P
PCIE_NAND1_D2R_N<2>	SSD_8L CN702	0.22UF	PCIE_NAND1_D2R_C_N<2>	T10 PCIE_TX0_N

All: GND_VOID=TRUE; 10% 6.3V X5R-CERM 0201

NAND1_PCIE_RESET_L → EXT_NCE/PERST* (F10)
NAND1_S5E2_PCIE_RESREF → PCIE_RESREF (N10)

SSD_8L CN785 10PF 5% 25V C0G 0201
SSD_8L RN704 200 0.1% 1/20W TK 0201-2
SSD_8L RN705 300 1% 1/20W TK 0201
SSD_8L RN706 300 1% 1/20W TK 0201

NAND1_S5E2_ZQ_1 → ZQ_1 (K5) — PLACE_NEAR=UN700.K5:15MM
NAND1_S5E2_ZQ_0 → ZQ_0 (M11) — PLACE_NEAR=UN700.M11:15MM

EXT_D0/BOOT0 (G8)	NAND1_LPB_L	
EXT_D1/BOOT1 (H9)	NAND_BFH	
EXT_D2/BOOT2/SPINAND_SCLK (F8)	NAND1_BOOT2	
EXT_D3/SPINAND_MISO/SWD_UID0 (E8)	NAND1_S5E2_SWD_UID0	
EXT_D4/SPI_CS (G9)		
EXT_D5/SPINAND_MOSI/SWD_UID1 (E9)	NAND1_S5E2_SWD_UID1	
EXT_D6/BOOT3 (F9)		
EXT_D7/SPF* (G10)	NAND1_PFN_L	
EXT_DQS/BCM* (E10)	NAND1_BCM_L	
EXT_NRE/JTAG_TMS (E6)	SWD_NAND1_S5E2_S5E3_SWDIO	
EXT_NWE/JTAG_TCK (F6)	SWD_NAND1_S5E2_S5E3_SWCLK	
EXT_RNB/JTAG_TDO (G6)	NAND1_S5E2_JTAG_TDO	
EXT_CLE/JTAG_TDI (G7)	NAND1_S5E1_JTAG_TDO	
EXT_ALE/JTAG_SEL (E7)	NAND1_JTAG_SEL	
DROOP* (N4)	TP_NAND1_S5E2_DROOP_L	
WP* (E5)	NAND1_WP_L	
ANI0_VREF (K11)	TP_NAND1_S5E2_ANI0_VREF	
ANI1_VREF (M5)	TP_NAND1_S5E2_ANI1_VREF	

B NAND1 S5E2 Bulk Capacitance

PP2V5_NAND1 → SSD_8L CN720 20UF 20% 10V X5R 0402; SSD_8L CN722 2.2UF 20% 10V X5R 0201; SSD_8L CN723 2.2UF 20% 10V X5R 0201; SSD_8L CN724 2.2UF 20% 10V X5R 0201; SSD_8L CN725 2.2UF 20% 10V X5R 0201

SSD_8L FLN700 10OHM-50%-1A-0.05OHM

PP1V2_NAND1 → PP1V2_NAND1_S5E2_PCI_AVDD_H (VOLTAGE=1.2V)
PLACE_NEAR=UN700.P9:11.5MM
SSD_8L CN745 4.7UF 20% 4V CER-X5R 0201; SSD_8L CN744 0.1UF 10% 6.3V CERM-X5R 0201

SSD_8L RN710 2 1/20W 1% TK 0201
PP1V2_NAND1 → PP1V2_NAND1_S5E2_AVDD1X_PLL (VOLTAGE=1.2V)
PLACE_NEAR=UN700.N6:11.5MM
SSD_8L CN747 2.2UF 20% 10V X5R 0201; SSD_8L CN746 0.1UF 10% 6.3V CERM-X5R 0201

PP1V2_NAND1 → SSD_8L CN730 4.3UF 20% 4V CERM 0402-THICKSTNCL; SSD_8L CN734 2.2UF 20% 10V X5R 0201; SSD_8L CN735 2.2UF 20% 10V X5R 0201; SSD_8L CN736 2.2UF 20% 10V X5R 0201; SSD_8L CN737 2.2UF 20% 10V X5R 0201; SSD_8L CN738 2.2UF 20% 10V X5R 0201; SSD_8L CN739 2.2UF 20% 10V X5R 0201; SSD_8L CN73A 2.2UF 20% 10V X5R 0201; SSD_8L CN732 20UF 20% 10V X5R 0402

PP0V9_NAND1 → SSD_8L CN710 20UF 20% 10V X5R 0402; SSD_8L CN711 20UF 20% 10V X5R 0402; SSD_8L CN712 2.2UF 20% 10V X5R 0201; SSD_8L CN713 2.2UF 20% 10V X5R 0201; SSD_8L CN714 2.2UF 20% 10V X5R 0201; SSD_8L CN715 0.1UF 10% 6.3V CERM-X5R 0201; SSD_8L CN716 0.1UF 10% 6.3V CERM-X5R 0201; SSD_8L CN717 0.1UF 10% 6.3V CERM-X5R 0201

SSD_8L FLN701 10OHM-50%-1A-0.05OHM
PP0V9_NAND1 → PP0V9_NAND1_S5E2_VDD_PLL (VOLTAGE=0.9V)
PLACE_NEAR=FLN701.2:5MM — PLACE_NEAR=UN700.M6:11.5MM
SSD_8L CN783 4.7UF 20% 4V CER-X5R 0201

The inductance from CN747, CN746, CN745, CN744 to their S5E pins shall be less than 1100pH

C NAND1 S5E2 Bulk Miscellaneous

PP1V2_NAND1 → SSD_8L RN709 47K 1/20W 1% TK 0201 → NAND1_S5E2_SWD_UID1

NAND1_S5E2_SWD_UID0 → SSD_8L RN708 47K 1/20W 1% TK 0201

PCB designers should add stiching vias for RFU/RFU_2 NC pins

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NC_UN700_C5	C5	RFU_2	NC	Y11
NC_UN700_C6	C6	RFU_2	RFU_2 C10	NC_UN700_C10
NC_UN700_C7	C7	RFU_2	RFU_2 C11	NC_UN700_C11
NC_UN700_C8	C8	RFU_2	RFU H10	NC_UN700_H10
NC_UN700_C9	C9	RFU_2	RFU J10	NC_UN700_J10
NC_UN700_D4	D4	RFU_2	RFU K6	NC_UN700_K6
NC_UN700_D5	D5	RFU_2	RFU K10	NC_UN700_K10
NC_UN700_D6	D6	RFU_2	RFU L5	NC_UN700_L5
NC_UN700_D7	D7	RFU_2	RFU L6	NC_UN700_L6
NC_UN700_D8	D8	RFU_2	RFU L10	NC_UN700_L10
NC_UN700_D9	D9	RFU_2	RFU L11	NC_UN700_L11
NC_UN700_D10	D10	RFU_2	RFU M10	NC_UN700_M10
NC_UN700_D11	D11	RFU_2		
NC_UN700_D12	D12	RFU_2		

D NAND1 S5E2 Power/Gnd

UN700
MK2-H1.3MM
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PP2V5_NAND1 → (VCC)
E4 E12 F4 F12 T4 T12 U4 U12 VCC

PP1V2_NAND1 → (VDDIO_1)
G5 G11 H5 H11 P5 P11 R5 R11 VDDIO_1

PP1V2_NAND1_S5E2_PCI_AVDD_H → (PCIE_AVDD_H)
P9 P10 PCIE_AVDD_H

PP1V2_NAND1_S5E2_AVDD1X_PLL → N6 AVDD1X_PLL

PP1V2_NAND1 → (VDDIO_2_L_ANI)
G12 G4 H4 H12 K4 M12 P4 P12 R4 R12 VDDIO_2_L_ANI

(VDDIO_2_DP)
K12 L4 L12 M4 VDDIO_2_DP

PP0V9_NAND1 → (VDD)
J7 J9 K7 K9 M7 M9 N7 N9 VDD

(PCIE_VDD)
P7 R7 R9 PCIE_VDD

PP0V9_NAND1_S5E2_VDD_PLL → M6 VDD_PLL

TP_NAND1_S5E2_VPP → E11 VPP

H6 VQPS

(VSS)
B5 B6 B7 B8 B9 B10 B11 C4 C12 D3 D13 E3 E13 F3 F5 F11 F13 G3 G13 H3 H7 H8 H13 J3 J4 J5 J8 J11 J12 J13 K3 K8 K13 L3 L7 L8 L9 L13 M3 M8 M13 N3 N5 N8 N12 N13 P3 P8 P13 R3 R6 R8 R10 R13 T3 T5 T7 T9 T11 T13 U3 U5 U7 U9 U11 U13 V4 V5 V6 V7 V8 V9 V10 V11 V12

UN700
MK2-H1.3MM
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A1	VSS/DUMMY	VSS/DUMMY	N15
A2	VSS/DUMMY	VSS/DUMMY	P1
A3	VSS/DUMMY	VSS/DUMMY	P2
A4	VSS/DUMMY	VSS/DUMMY	P14
A5	VSS/DUMMY	VSS/DUMMY	P15
A6	VSS/DUMMY	VSS/DUMMY	R1
A7	VSS/DUMMY	VSS/DUMMY	R2
A8	VSS/DUMMY	VSS/DUMMY	R14
A9	VSS/DUMMY	VSS/DUMMY	R15
A10	VSS/DUMMY	VSS/DUMMY	T1
A11	VSS/DUMMY	VSS/DUMMY	T2
A12	VSS/DUMMY	VSS/DUMMY	T14
A13	VSS/DUMMY	VSS/DUMMY	T15
A14	VSS/DUMMY	VSS/DUMMY	U1
A15	VSS/DUMMY	VSS/DUMMY	U2
B1	VSS/DUMMY	VSS/DUMMY	U14
B2	VSS/DUMMY	VSS/DUMMY	U15
B3	VSS/DUMMY	VSS/DUMMY	V1
B4	VSS/DUMMY	VSS/DUMMY	V2
B12	VSS/DUMMY	VSS/DUMMY	V3
B13	VSS/DUMMY	VSS/DUMMY	V13
B14	VSS/DUMMY	VSS/DUMMY	V14
B15	VSS/DUMMY	VSS/DUMMY	V15
C1	VSS/DUMMY	VSS/DUMMY	W1
C2	VSS/DUMMY	VSS/DUMMY	W2
C3	VSS/DUMMY	VSS/DUMMY	W3
C13	VSS/DUMMY	VSS/DUMMY	W4
C14	VSS/DUMMY	VSS/DUMMY	W5
C15	VSS/DUMMY	VSS/DUMMY	W6
D1	VSS/DUMMY	VSS/DUMMY	W7
D2	VSS/DUMMY	VSS/DUMMY	W8
D14	VSS/DUMMY	VSS/DUMMY	W9
D15	VSS/DUMMY	VSS/DUMMY	W10
E1	VSS/DUMMY	VSS/DUMMY	W11
E2	VSS/DUMMY	VSS/DUMMY	W12
E14	VSS/DUMMY	VSS/DUMMY	W13
E15	VSS/DUMMY	VSS/DUMMY	W14
F1	VSS/DUMMY	VSS/DUMMY	W15
F2	VSS/DUMMY	VSS/DUMMY	Y1
F14	VSS/DUMMY	VSS/DUMMY	Y2
F15	VSS/DUMMY	VSS/DUMMY	Y3
G1	VSS/DUMMY	VSS/DUMMY	Y4
G2	VSS/DUMMY	VSS/DUMMY	Y5
G14	VSS/DUMMY	VSS/DUMMY	Y6
G15	VSS/DUMMY	VSS/DUMMY	Y7
H1	VSS/DUMMY	VSS/DUMMY	Y8
H2	VSS/DUMMY	VSS/DUMMY	Y9
H14	VSS/DUMMY	VSS/DUMMY	Y10
H15	VSS/DUMMY	VSS/DUMMY	Y12
J1	VSS/DUMMY	VSS/DUMMY	Y13
J2	VSS/DUMMY	VSS/DUMMY	Y14
J14	VSS/DUMMY	VSS/DUMMY	Y15
J15	VSS/DUMMY	VSS/DUMMY	AA1
K1	VSS/DUMMY	VSS/DUMMY	AA2
K2	VSS/DUMMY	VSS/DUMMY	AA3
K14	VSS/DUMMY	VSS/DUMMY	AA4
K15	VSS/DUMMY	VSS/DUMMY	AA5
L1	VSS/DUMMY	VSS/DUMMY	AA6
L2	VSS/DUMMY	VSS/DUMMY	AA7
L14	VSS/DUMMY	VSS/DUMMY	AA8
L15	VSS/DUMMY	VSS/DUMMY	AA9
M1	VSS/DUMMY	VSS/DUMMY	AA10
M2	VSS/DUMMY	VSS/DUMMY	AA11
M14	VSS/DUMMY	VSS/DUMMY	AA12
M15	VSS/DUMMY	VSS/DUMMY	AA13
N1	VSS/DUMMY	VSS/DUMMY	AA14
N2	VSS/DUMMY	VSS/DUMMY	AA15
N14	VSS/DUMMY		

BOM_COST_GROUP=SSD

PAGE TITLE: STORAGE: SSD1 S5E MK2 <2>

Apple Inc.

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NAND1_CLK24M_23 → N11 CLK_IN
NAND1_RESET_L → J6 RESET*
NAND1_JTAG_TRST_L → F7 TRST* (INT PD)
PCIE_CLK100M_NAND1_2_3_P → T6 PCIE_REFCLK_P
PCIE_CLK100M_NAND1_2_3_N → U6 PCIE_REFCLK_N
NAND1_CLKREQ3_R_L → P6 PCIE_CLKREQ*

PCIE AC caps - place as close as possible to NAND

PCIE_NAND1_R2D_C_P<3> → SSD_8L CN803 0.22UF 10% 6.3V X5R-CERM 0201 → PCIE_NAND1_R2D_P<3> → U8 PCIE_RX0_P
PCIE_NAND1_R2D_C_N<3> → SSD_8L CN804 0.22UF 10% 6.3V X5R-CERM 0201 → PCIE_NAND1_R2D_N<3> → T8 PCIE_RX0_N
PCIE_NAND1_D2R_P<3> → SSD_8L CN801 0.22UF 10% 6.3V X5R-CERM 0201 → PCIE_NAND1_D2R_C_P<3> → U10 PCIE_TX0_P
PCIE_NAND1_D2R_N<3> → SSD_8L CN802 0.22UF 10% 6.3V X5R-CERM 0201 → PCIE_NAND1_D2R_C_N<3> → T10 PCIE_TX0_N
GND_VOID=TRUE

NAND1_PCIE_RESET_L → F10 EXT_NCE/PERST*

NAND1_S5E3_PCIE_RESREF → N10 PCIE_RESREF

SSD_8L CN885 10PF 5% 25V C0G 0201
SSD_8L RN804 200 0.1% 1/20W TK 0201-2
SSD_8L RN805 300 1% 1/20W TK 0201
PLACE_NEAR=UN800.K5:15MM
NAND1_S5E3_ZQ_1 → K5 ZQ_1
NAND1_S5E3_ZQ_0 → M11 ZQ_0
PLACE_NEAR=UN800.M11:15MM
SSD_8L RN806 300 1% 1/20W TK 0201

EXT_D0/BOOT0 G8 NAND1_LPB_L
EXT_D1/BOOT1 (INT PU) H9 NAND_BFH
EXT_D2/BOOT2/SPINAND_SCLK F8 NAND1_BOOT2
EXT_D3/SPINAND_MISO/SWD_UID0 E8 NAND1_S5E3_SWD_UID0
EXT_D4/SPI_CS G9
EXT_D5/SPINAND_MOSI/SWD_UID1 E9 NAND1_S5E3_SWD_UID1
EXT_D6/BOOT3 F9
EXT_D7/SPF* G10 NAND1_PFN_L
EXT_DQS/BCM* (INT PU) E10 NAND1_BCM_L
EXT_NRE/JTAG_TMS (INT PU) E6 SWD_NAND1_S5E2_S5E3_SWDIO
EXT_NWE/JTAG_TCK (INT PU) F6 SWD_NAND1_S5E2_S5E3_SWCLK
EXT_RNB/JTAG_TDO G6 TP_NAND1_S5E3_JTAG_TDO
EXT_CLE/JTAG_TDI (INT PU) G7 NAND1_S5E2_JTAG_TDO
EXT_ALE/JTAG_SEL (INT PD) E7 NAND1_JTAG_SEL
DROOP* N4 TP_NAND1_S5E3_DROOP_L
WP* E5 NAND1_WP_L
ANI0_VREF K11 TP_NAND1_S5E3_ANI0_VREF
ANI1_VREF M5 TP_NAND1_S5E3_ANI1_VREF

B NAND1 S5E3 Bulk Capacitance

PP2V5_NAND1
SSD_8L CN820 20UF 20% 10V X5R 0402
SSD_8L CN822 2.2UF 20% 10V X5R 0201
SSD_8L CN823 2.2UF 20% 10V X5R 0201
SSD_8L CN824 2.2UF 20% 10V X5R 0201
SSD_8L CN825 2.2UF 20% 10V X5R 0201
SSD_8L FLN800 10OHM-50%-1A-0.05OHM 0201
PP1V2_NAND1 → PP1V2_NAND1_S5E3_PCI_AVDD_H VOLTAGE=1.2V
PLACE_NEAR=UN800.P9:11.5MM
SSD_8L CN845 4.7UF 20% 4V CER-X5R 0201
SSD_8L CN844 0.1UF 10% 6.3V CERM-X5R 0201

SSD_8L RN810 2 1/20W 1% TK 0201
PP1V2_NAND1 → PP1V2_NAND1_S5E3_AVDD1X_PLL VOLTAGE=1.2V
PLACE_NEAR=UN800.N6:11.5MM
SSD_8L CN847 2.2UF 20% 10V X5R 0201
SSD_8L CN846 0.1UF 10% 6.3V CERM-X5R 0201

The inductance from CN847, CN846, CN845, CN844 to their S5E pins shall be less than 1100pH

PP1V2_NAND1
SSD_8L CN830 4.3UF 20% 4V CERM 0402-THICKSTNCL
SSD_8L CN834 2.2UF 20% 10V X5R 0201
SSD_8L CN835 2.2UF 20% 10V X5R 0201
SSD_8L CN836 2.2UF 20% 10V X5R 0201
SSD_8L CN837 2.2UF 20% 10V X5R 0201
SSD_8L CN838 2.2UF 20% 10V X5R 0201
SSD_8L CN839 2.2UF 20% 10V X5R 0201
SSD_8L CN83A 2.2UF 20% 10V X5R 0201
SSD_8L CN832 20UF 20% 10V X5R 0402

PP0V9_NAND1
SSD_8L CN810 20UF 20% 10V X5R 0402
SSD_8L CN811 20UF 20% 10V X5R 0402
SSD_8L CN812 2.2UF 20% 10V X5R 0201
SSD_8L CN813 2.2UF 20% 10V X5R 0201
SSD_8L CN814 2.2UF 20% 10V X5R 0201
SSD_8L CN815 0.1UF 10% 6.3V CERM-X5R 0201
SSD_8L CN816 0.1UF 10% 6.3V CERM-X5R 0201
SSD_8L CN817 0.1UF 10% 6.3V CERM-X5R 0201

SSD_8L FLN801 10OHM-50%-1A-0.05OHM 0201
PP0V9_NAND1 → PP0V9_NAND1_S5E3_VDD_PLL VOLTAGE=0.9V
PLACE_NEAR=FLN801.2:5MM
PLACE_NEAR=UN800.M6:11.5MM
SSD_8L CN883 4.7UF 20% 4V CER-X5R 0201

C NAND1 S5E3 Bulk Miscellaneous

PP1V2_NAND1
SSD_8L RN808 47K 1/20W 1% TK 0201 → NAND1_S5E3_SWD_UID0
SSD_8L RN809 47K 1/20W 1% TK 0201 → NAND1_S5E3_SWD_UID1

PCB designers should add stiching vias for RFU/RFU_2 NC pins

UN800
MK2-H1.3MM
BGA
SYM 3 OF 4
OMIT_TABLE
998-24627

NC_UN800_C5 C5 RFU_2
NC_UN800_C6 C6 RFU_2
NC_UN800_C7 C7 RFU_2
NC_UN800_C8 C8 RFU_2
NC_UN800_C9 C9 RFU_2
NC_UN800_D4 D4 RFU_2
NC_UN800_D5 D5 RFU_2
NC_UN800_D6 D6 RFU_2
NC_UN800_D7 D7 RFU_2
NC_UN800_D8 D8 RFU_2
NC_UN800_D9 D9 RFU_2
NC_UN800_D10 D10 RFU_2
NC_UN800_D11 D11 RFU_2
NC_UN800_D12 D12 RFU_2

NC Y11
RFU_2 C10 NC_UN800_C10
RFU_2 C11 NC_UN800_C11
RFU H10 NC_UN800_H10
RFU J10 NC_UN800_J10
RFU K6 NC_UN800_K6
RFU K10 NC_UN800_K10
RFU L5 NC_UN800_L5
RFU L6 NC_UN800_L6
RFU L10 NC_UN800_L10
RFU L11 NC_UN800_L11
RFU M10 NC_UN800_M10

D NAND1 S5E3 Power/Gnd

UN800
MK2-H1.3MM
BGA
SYM 1 OF 4

PP2V5_NAND1 → E4 E12 F4 F12 T4 T12 U4 U12 VCC (VCC)
OMIT_TABLE
998-24627
PP1V2_NAND1 → G5 G11 H5 H11 P5 P11 R5 R11 VDDIO_1 (VCCQ_IO)
PP1V2_NAND1_S5E3_PCI_AVDD_H → P9 P10 PCIE_AVDD_H
PP1V2_NAND1_S5E3_AVDD1X_PLL → N6 AVDD1X_PLL
PP1V2_NAND1 → G12 G4 H4 H12 K4 M12 P4 P12 R4 R12 VDDIO_2_L_ANI (VCCQ_ANI)
K12 L4 L12 M4 VDDIO_2_DP
PP0V9_NAND1 → J7 J9 K7 K9 M7 M9 N7 N9 VDD (VDD)
P7 R7 R9 PCIE_VDD
PP0V9_NAND1_S5E3_VDD_PLL → M6 VDD_PLL
TP_NAND1_S5E3_VPP → E11 VPP
H6 VQPS

VSS: B5 B6 B7 B8 B9 B10 B11 C4 C12 D3 D13 E3 E13 F3 F5 F11 F13 G3 G13 H3 H7 H8 H13 J3 J4 J5 J8 J11 J12 J13 K3 K8 K13 L3 L7 L8 L9 L13 M3 M8 M13 N3 N5 N8 N12 N13 P3 P8 P13 R3 R6 R8 R10 R13 T3 T5 T7 T9 T11 T13 U3 U5 U7 U9 U11 U13 V4 V5 V6 V7 V8 V9 V10 V11 V12

UN800
MK2-H1.3MM
BGA
SYM 4 OF 4
OMIT_TABLE
998-24627

A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 B1 B2 B3 B4 B12 B13 B14 B15 C1 C2 C3 C13 C14 C15 D1 D2 D14 D15 E1 E2 E14 E15 F1 F2 F14 F15 G1 G2 G14 G15 H1 H2 H14 H15 J1 J2 J14 J15 K1 K2 K14 K15 L1 L2 L14 L15 M1 M2 M14 M15 N1 N2 N14 VSS/DUMMY
N15 P1 P2 P14 P15 R1 R2 R14 R15 T1 T2 T14 T15 U1 U2 U14 U15 V1 V2 V3 V13 V14 V15 W1 W2 W3 W4 W5 W6 W7 W8 W9 W10 W11 W12 W13 W14 W15 Y1 Y2 Y3 Y4 Y5 Y6 Y7 Y8 Y9 Y10 Y12 Y13 Y14 Y15 AA1 AA2 AA3 AA4 AA5 AA6 AA7 AA8 AA9 AA10 AA11 AA12 AA13 AA14 AA15 VSS/DUMMY

BOM_COST_GROUP=SSD

PAGE TITLE: STORAGE: SSD1 S5E MK2 <3>
Apple Inc.
DRAWING NUMBER: 051-08286
SIZE: D
REVISION: 5.0.3
BRANCH:
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A NAND1 NAND VCC (2.5V)

SSD_OC1VR1 PPBUS_NAND1 — CN979 27UF 20% 16V TANT-POLY CASE-B12 — CN980 27UF 20% 16V TANT-POLY CASE-B12 — CN981 27UF 20% 16V TANT-POLY CASE-B12 — CN982 27UF 20% 16V TANT-POLY CASE-B12 (128S00107)

PACK_OPTION=2V5_NAND_PBUS-B12-18V

CN983 2.2UF 20% 25V X6S-CERM 0402 — CN984 2.2UF 20% 25V X6S-CERM 0402 — CN985 2.2UF 20% 25V X6S-CERM 0402 — CN986 2.2UF 20% 25V X6S-CERM 0402

CN979 33UF 20% 16V TANT CASE-T — CN980 33UF 20% 16V TANT CASE-T — CN981 33UF 20% 16V TANT CASE-T — CN982 33UF 20% 16V TANT CASE-T (128S00009)

PACK_OPTION=2V5_NAND_PBUS-B12-16V
PACK_IGNORE=TRUE

CN980 33UF 20% 16V TANT CASED12-SM — CN981 33UF 20% 16V TANT CASED12-SM — CN980 68UF 20% 16V POLY-TANT CASE-D2E-SM — CN981 68UF 20% 16V POLY-TANT CASE-D2E-SM

PACK_OPTION=2V5_NAND_PBUS-D12
PACK_IGNORE=TRUE

PACK_OPTION=2V5_NAND_PBUS-D2E
PACK_IGNORE=TRUE

RN988 0 1/20W 0% TK 0201 — P2V5_NAND1_EN → P2V5_NAND1_EN_R

RN981 16K 1% 1/20W TK 0201-1

CN988 1000PF 10% 16V X7R-1 0201 — CN989 56PF 5% 25V NP0-C0G 0201 — CN987 1.2NF ±10% 10V CERM 0201-1 — RN980 25.5K 1% 1/20W TK 0201

SOFT START TIME SET TO: 0.42/0.63/1.1 ms (min / typ / max)

FREQUENCY SET TO: 1.5MHz

XWN980 SM

UN980 LT8642-1 LQFN-THICKSTNCL CRITICAL SSD_OC1VR1

4	VIN	BIAS	2
5	VIN	INTVCC	3
12	VIN	BST	7
13	VIN	SW	8
14	EN/UV	SW	9
19	VC	SW	10
1	PG	CLKOUT	16
20	FB		
18	SS		
17	RT		
15	SYNC/MODE		
6	GND		
11	GND		
21	GND		
22	NC		
23	NC		
24	NC		
25	NC		

P2V5_NAND1_BIAS
PP2V5_NAND1_INTVCC VOLTAGE=2.5V

RN992 1.5 1% 1/20W TK 0201 — P2V5_NAND1_BST → P2V5_NAND1_BST_R (SWITCH_NODE=TRUE DIDT=TRUE)

CN990 2.2UF 20% 25V X6S-CERM 0402 — CN992 47NF 10% 10V X6S-CERM 0201

P2V5_NAND1_SW SWITCH_NODE=TRUE DIDT=TRUE MIN_NECK_WIDTH=0.1000 MIN_LINE_WIDTH=0.2000

LN980 0.56UH-20%-16A-0.0072OHM PILA052D-SM — XWN981 SM

RN987 0 1/20W 0% TK 0201 — PPVIN_P3V8NAND1

CN991 2.2UF 20% 25V X6S-CERM 0402

P2V5_NAND1_PGOOD → RN912 100K 1% 1/20W TK 0201 → PP2V5_NAND1

CN994 150UF 20% 6.3V TANT CASE-B-SM — CN995 150UF 20% 6.3V TANT CASE-B-SM — CN996 150UF 20% 6.3V TANT CASE-B-SM

P2V5_NAND1_FB_XW → RN982 10 5% 1/20W TK 0201

CN998 10UF 20% 6.3V CER-X6S 0402 — CN999 10UF 20% 6.3V CER-X6S 0402

P2V5_NAND1_FB → CN993 1000PF 10% 16V X7R-1 0201 → P2V5_NAND1_FB_C → RN986 10K 1% TK 0201 → P2V5_NAND1_FB_RC

RN985 27.4K 0.1% TK 0201 — RN984 82.5K 0.1% TK 0201 — RN983 6.98K 1% TK 0201 — P2V5_NAND1_FB_RC2

AGND_P2V5_NAND1

B NAND1 Ocarina

PPVIN_P3V8NAND1 — CN900 10UF 20% 6.3V CERM-X6S 0402 — CN901 10UF 20% 6.3V CERM-X6S 0402 — CN902 0.1UF 10% 16V X6S-CERM 0201 — CN903 4.7UF 20% 6.3V X6S 0402 — CN904 4.7UF 20% 6.3V X6S 0402 — CN905 0.1UF 10% 16V X6S-CERM 0201 — CN906 150UF 20% 6.3V TANT-POLY CASE-B3-1 CRITICAL

PLACE CN900-CN902 NEAR OCARINA PINS E7/E8
PLACE CN903-CN905 NEAR OCARINA PINS A7/A8
PLACE CN906 NEAR OCARINA PIN B4

OCARINA I2C BASE ADDRESS
STG0: F2
STG1: F0

PPVDD_LDO_NAND1_OCARINA VOLTAGE=2.5V → CN907 0.22UF 20% 6.3V X6S-CERM 0201

TP_NAND1_OCARINA_VCC_DET → PP1V8_S2 → CN909 0.1UF 10% 6.3V CERM-X5R 0201

UN900 D2499A0P0VLAVBC2 WLCSP

338S00600 CRITICAL OMIT_TABLE

E8	VDD_BUCK0	ATM	F3
E7	VDD_BUCK0	ADDR	D2
A8	VDD_BUCK1	FORCE_EN	E1
A7	VDD_BUCK1	I2C_SCL	G2
B4	VDD_MAIN	I2C_SDA	G3
B5	VDD_LDO	LPBN	F4
G1	VCC_DET	PFN*	G5
C1	V_BUF_1.8V	PGOOD	G6
		PMIC_RESET*	D1
		POK1	D3
		POK2	F1
		RESET*	E5
		SYS_ALIVE	F2
		VEN1	F5
		VEN2/PMIC_CTRL	E4
		WP*	G4
A6	VSS		
A5	VSS		
B6	VSS		
A2	VSS		
C3	VSS		
C4	VSS		
D6	VSS		
D4	VSS		
E6	VSS		
E2	VSS		
F6	VSS		
E3	VSS		
G8	VSS(VSS_BUCK0)		
G7	VSS(VSS_BUCK0)		
C8	VSS(VSS_BUCK01)		
C7	VSS(VSS_BUCK01)		
C6	VSS(VSS_BUCK01)		

RN906 0 1/20W 0% TK 0201 — NAND1_STG01_ADDR
RN911 100K 1/20W 1% TK 0201 — NAND1_FORCE_EN
I2C_NAND_PMIC_SCL_1V8
I2C_NAND_PMIC_SDA_1V8
RN919 47K 1/20W 1% TK 0201 — NAND1_LPB_L
RN917 47K 1/20W 1% TK 0201 — NAND1_PFN_L
RN910 100K 1/20W 1% TK 0201 — NAND1_OCARINA_PGOOD
PPVIN_P3V8NAND1 → PPVIN_P3V8NAND1
P2V5_NAND1_PGOOD
RN918 47K 1/20W 1% TK 0201 — NAND1_RESET_L
PMU_SYS_ALIVE
P2V5_NAND1_EN → TP_NAND1_OCARINA_VEN2
NC_NAND1_OCARINA_WP_L

TCAL	A4	NAND1_OCARINA_TCAL	
VREF	B3	NAND1_OCARINA_VREF	
IREF	B2	NAND1_OCARINA_IREF	
TDEV1	B1	NAND1_OCARINA_TDEV1	
TDEV2	C2	NAND1_OCARINA_TDEV2	
VR1_DISCHG	A3	PP2V5_NAND1	
VR2_DISCHG	A1		
BUCK0_FB_DIS	D5	PP0V9_NAND1_FB_DIS	VOLTAGE=0.9V
BUCK1_FB_DIS	C5	PP1V2_NAND1_FB_DIS	
BUCK0_LX0	F8		VOLTAGE=1.2V
BUCK0_LX0	F7	P0V9_LX0_NAND1 DIDT=TRUE SWITCH_NODE=TRUE	
BUCK0_LX1	D8		
BUCK0_LX1	D7	P0V9_LX1_NAND1 DIDT=TRUE SWITCH_NODE=TRUE	
BUCK1_LX0	B8		
BUCK1_LX0	B7	P1V2_LX0_NAND1 DIDT=TRUE SWITCH_NODE=TRUE	

RN905 200K 1% 1/20W TK 0201 — CN908 0.1UF 10% 6.3V CERM-X5R 0201 — RN900 8.06K 0.1% 1/20W TK 0201-1

RN920 0 0% 1/20W TK 0201 — PP0V9_NAND1

RN930 0 0% 1/20W TK 0201 — PP1V2_NAND1

LN921 1UH-20%-4.8A-0.032OHM 1210 — CN920 20UF 20% 10V X5R 0402 — CN921 20UF 20% 10V X5R 0402 — CN922 20UF 20% 10V X5R 0402 — CN923 20UF 20% 10V X5R 0402 — CN924 20UF 20% 10V X5R 0402 — CN925 20UF 20% 10V X5R 0402 — CN926 20UF 20% 10V X5R 0402 — CN927 20UF 20% 10V X5R 0402 — CN928 20UF 20% 10V X5R 0402 — CN929 20UF 20% 10V X5R 0402 — CN92A 20UF 20% 10V X5R 0402 — CN92B 20UF 20% 10V X5R 0402 → PP0V9_NAND1

LN920 CRITICAL 0.47UH-20%-6.7A-0.023OHM 1210

LN930 CRITICAL 0.47UH-20%-6.7A-0.023OHM 1210

CN930 20UF 20% 10V X5R 0402 — CN931 20UF 20% 10V X5R 0402 — CN932 20UF 20% 10V X5R 0402 — CN933 20UF 20% 10V X5R 0402 — CN934 20UF 20% 10V X5R 0402 — CN935 20UF 20% 10V X5R 0402 — CN936 20UF 20% 10V X5R 0402 — CN937 20UF 20% 10V X5R 0402 — CN938 20UF 20% 10V X5R 0402 — CN939 20UF 20% 10V X5R 0402 → PP1V2_NAND1

Temperature Sensors

NAND1_OCARINA_TDEV1 — RN902 100K-1%-0.001A 0201 — RN901 18.2K 0.1% 1/20W TK 0201-1

NAND1_OCARINA_TDEV2 — RN904 100K-1%-0.001A 0201 — RN903 18.2K 0.1% 1/20W TK 0201-1

C NAND1 Power Aliases

PP2V5_NAND1 = PP2V5_NAND1 (VOLTAGE=2.5V MAKE_BASE=TRUE) = PP2V5_NAND1

PP1V2_NAND1 = PP1V2_NAND1 (VOLTAGE=1.2V MAKE_BASE=TRUE) = PP1V2_NAND1

PP0V9_NAND1 = PP0V9_NAND1 (VOLTAGE=0.9V MAKE_BASE=TRUE) = PP0V9_NAND1 = PP0V9_NAND1 = PP0V9_NAND1

BOM_COST_GROUP=SSD

PAGE TITLE: STORAGE: SSD1 OCARINA & NAND VCC

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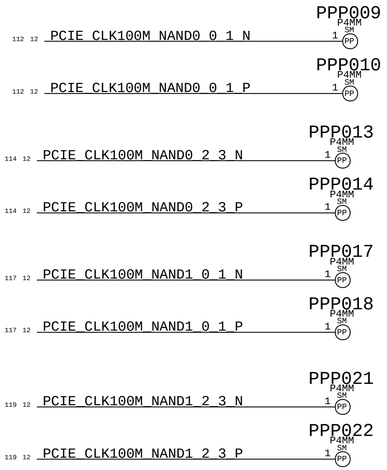
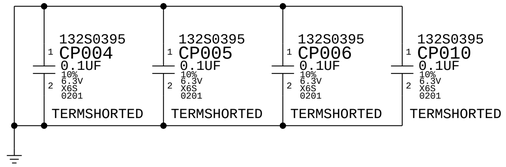
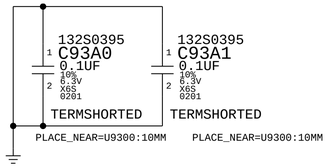
NAND CLK TEST POINTS



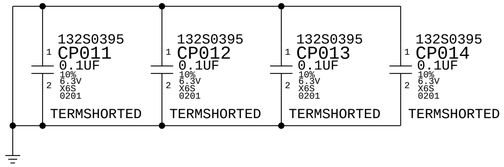
DUMMY 0201 CAPS FOR UNDERFILL RETIANING FOR NANDS



DUMMY 0201 CAPS FOR UNDERFILL RETIANING FOR SPITFIRE



DUMMY 0201 CAPS FOR UNDERFILL RETIANING FOR NAND



BOM_COST_GROUP=SSD

PAGE TITLE
STORAGE: SSD SUPPORT

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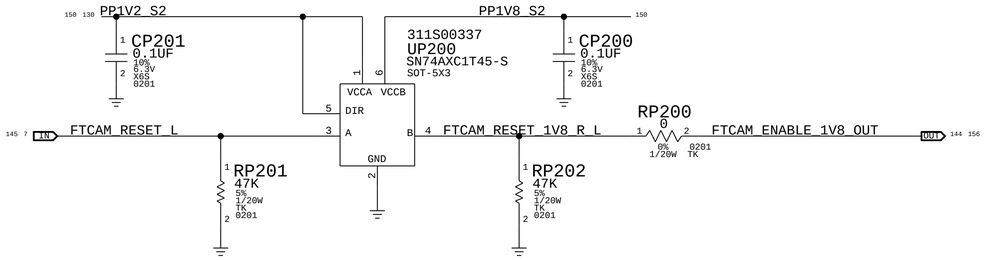
Level Shifter - FTCAM



PP CLOSE TO SOC FOR PROBING

PLACE_NEAR=U0600.C70:18MM
PPP200
P2MM
SM
144 124 7 LPDP_FTCAM_DATA_P<0>
FP

PLACE_NEAR=U0600.B70:18MM
PPP201
P2MM
SM
144 124 7 LPDP_FTCAM_DATA_N<0>
FP

BOM_COST_GROUP=CAMERA

PAGE TITLE
CAMERA-SUPPORT

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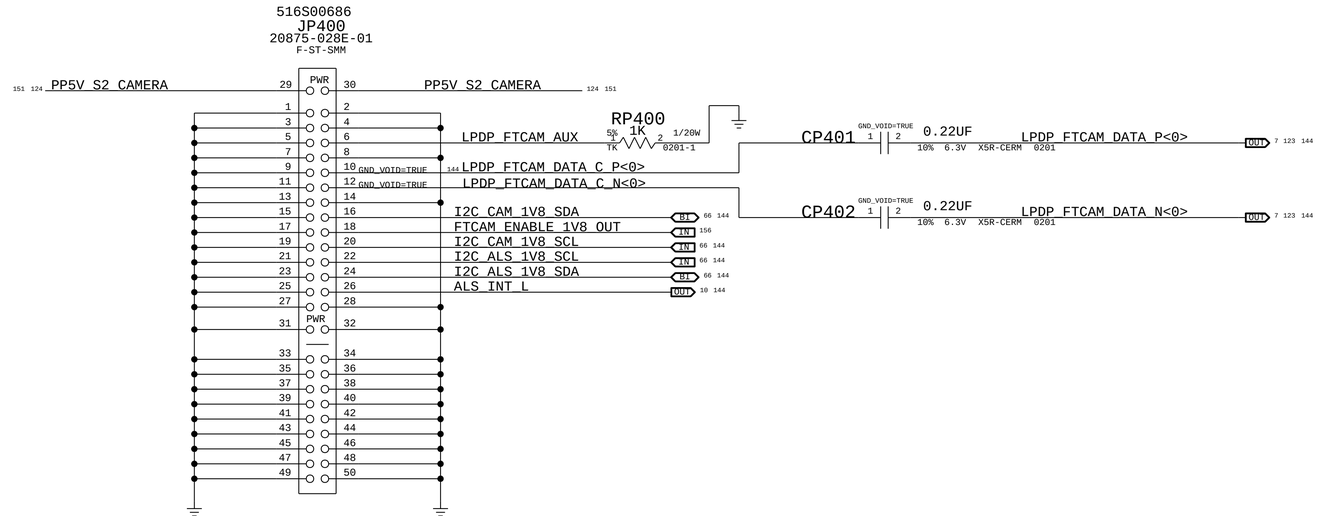

BOM_COST_GROUP=CAMERA

PAGE TITLE
CAMERA: FLEX CONNECTOR

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CP620 0.1UF 10% 16V X5R-CERM 0201
LPDP_INT_DATA_C_N<3> GND_VOID=TRUE → LPDP_INT_DATA_N<3>
CP621 0.1UF 10% 16V X5R-CERM 0201
LPDP_INT_DATA_C_P<3> GND_VOID=TRUE → LPDP_INT_DATA_P<3>

CP612 0.1UF 10% 16V X5R-CERM 0201
LPDP_INT_DATA_C_N<2> GND_VOID=TRUE → LPDP_INT_DATA_N<2>
CP613 0.1UF 10% 16V X5R-CERM 0201
LPDP_INT_DATA_C_P<2> GND_VOID=TRUE → LPDP_INT_DATA_P<2>

CP614 0.1UF 10% 16V X5R-CERM 0201
LPDP_INT_DATA_C_N<1> GND_VOID=TRUE → LPDP_INT_DATA_N<1>
CP615 0.1UF 10% 16V X5R-CERM 0201
LPDP_INT_DATA_C_P<1> GND_VOID=TRUE → LPDP_INT_DATA_P<1>

CP616 0.1UF 10% 16V X5R-CERM 0201
LPDP_INT_DATA_C_N<0> GND_VOID=TRUE → LPDP_INT_DATA_N<0>
CP617 0.1UF 10% 16V X5R-CERM 0201
LPDP_INT_DATA_C_P<0> GND_VOID=TRUE → LPDP_INT_DATA_P<0>

CP618 0.1UF 10% 16V X5R-CERM 0201
LPDP_INT_AUX_C_N GND_VOID=TRUE → LPDP_INT_AUX_N
CP619 0.1UF 10% 16V X5R-CERM 0201
LPDP_INT_AUX_C_P GND_VOID=TRUE → LPDP_INT_AUX_P

NOSTUFF RP601 1M 5% 1/20W TK 0201 (GND_VOID=TRUE)
NOSTUFF RP602 1M 5% 1/20W TK 0201 (GND_VOID=TRUE)

APN: 516S00682

JP600
20875-034E-01
F-ST-SMM

35 PWR	36		
SIGNAL			
1	2		
3 LPDP_INT_DATA_N<3> GND_VOID=TRUE	4	PP1V8_S2	150
5 LPDP_INT_DATA_P<3> GND_VOID=TRUE	6	I2C_SMC_SNS0_SCL_1V8	IN 66
7	8	I2C_SMC_SNS0_SDA_1V8	BI 66
9 LPDP_INT_DATA_N<2> GND_VOID=TRUE	10		
11 LPDP_INT_DATA_P<2> GND_VOID=TRUE	12		
13	14	UART_TCON_D2R_1V8	125 144
15 LPDP_INT_DATA_N<1> GND_VOID=TRUE	16		
17 LPDP_INT_DATA_P<1> GND_VOID=TRUE	18		
19	20		
21 LPDP_INT_DATA_N<0> GND_VOID=TRUE	22	SPI_TCON_CS_L	IN 13 144
23 LPDP_INT_DATA_P<0> GND_VOID=TRUE	24	SPI_TCON_MOSI_CONN	125
25	26	SPI_TCON_MISO_CONN	125
27 LPDP_INT_AUX_N GND_VOID=TRUE	28	SPI_TCON_CLK_CONN	125 143
29 LPDP_INT_AUX_P GND_VOID=TRUE	30		
31	32	EDP_PANEL_1V8_EN	IN 126 144
33	34	LPDP_INT_HPD	OUT 7 144 154 156
PWR			
37 PP3V8_AWAKESW_TCON 125 125 151	38	PP3V8_AWAKESW_TCON	125 151
GND			
39	40		
41	42		
43	44		
45	46		
47	48		
49	50		
51	52		
53	54		
55	56		

1.8V I/O CONNECT TO SMC I2C4

SWD Not Needed on MLB

RESISTORS AT SOC SIDE
MOSI, CLK SHOULD HAVE 33 OHM

RESISTORS AT SOC SIDE

PP1V2_AWAKE
CP622 0.1UF 10% 10V X5R-CERM 0201
311S00246
UP600
SN74AUP1G17 SON
144 125 UART_TCON_D2R_1V8 → UART_TCON_D2R OUT 6
RP603 1M 5% 1/20W TK 0201
NC
NC

RC FILTER

SPI_TCON_MISO_CONN → RP633 0 0% 1/20W TK 0201 → SPI_TCON_MISO OUT 6 144
SPI_TCON_MOSI_CONN → RP632 0 0% 1/20W TK 0201 → SPI_TCON_MOSI IN 13 144
SPI_TCON_CLK_CONN → RP631 0 0% 1/20W TK 0201 → SPI_TCON_CLK IN 13 144

NOSTUFF CP631 12PF 5% 50V C0G-CERM 0201
NOSTUFF CP632 12PF 5% 50V C0G-CERM 0201
NOSTUFF CP633 12PF 5% 50V C0G-CERM 0201

BOM_COST_GROUP=DISPLAY

PAGE TITLE: DISPLAY CONNECTOR

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*** OK2INTEGRATE ***

150 PP3V8_AON

CP730 1.0UF 20% 6.3V X5R 0201-1

CRITICAL

UP730 TLV758P WSON-THICKSTNCL

IN, EN, DNC (NC), OUT, FB, GND, EPAD

3V29 FEED TO BACKLIGHT

PPBCON_AWAKESW_BKLTCONN_VIN

CP731 0.1UF 10% 16V X5R-CERM 0201

CP732 10UF 20% 16V X5R-CERM 0402-7

RP732 49.9K 1% 1/20W TF 0201

FB_BLKT_2D

RP731 10K 1% 1/20W TF 0201

VOUT = VFB * (1 + R1/R2)
VOUT = 0.55 * (1 + 49.9/10)
VOUT = 3.2945

NOSTUFF
RP730 0 0% 1/16W TF 0402

CP710 1.0UF 20% 6.3V X5R 0201-1

CRITICAL

UP701 SLG5AP1564V STDFN

VDD, ON, D, S, PG (NC), GND

3V8 FEED TO MDB

PPMDB_AWAKESW_TCON 150

CP718 0.1UF 10% 16V X5R-CERM 0201 CKPLUS_WAIVE=CAPDERATE

CP719 10UF 20% 16V X5R-CERM 0402-7 CKPLUS_WAIVE=CAPDERATE

150 PP1V8_AON_FPMU

BYPASS=UP710::4MM
CP770 0.1UF 10% 10V X5R-CERM 0201

UP710 SLG4AP44015 STQFN

38 IN LCD_PWR_EN → LCD_EN_IN
144 121 116 96 155 46 IN PMU_SYS_ALIVE → SYS_ALIVE
NC: 5, 6, 7, 8, 12, 14
VDD, GND

LCD_EN_OUT → EDP_PANEL_1V8_EN OUT 125 144
PANEL_3V8_EN → EDP_PANEL_PWR_EN
BLC_1V29_EN → EDP_BKLT_1V29_EN OUT 38 145
CONTROLS 1.29V LDO IN PMIC
PANEL_DISCHARGE → EDP_PANEL_DISCHARGE

RP700 300 5% 1/16W TF 0402
PPPANEL_PANEL_DISCHARGE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
VOLTAGE=4V

DMN2250UFB DFN1006-3 QP700

RP701 100K 5% 1/20W TF 0201

BOM_COST_GROUP=DISPLAY

PAGE TITLE: DISPLAY POWER SEQUENCER

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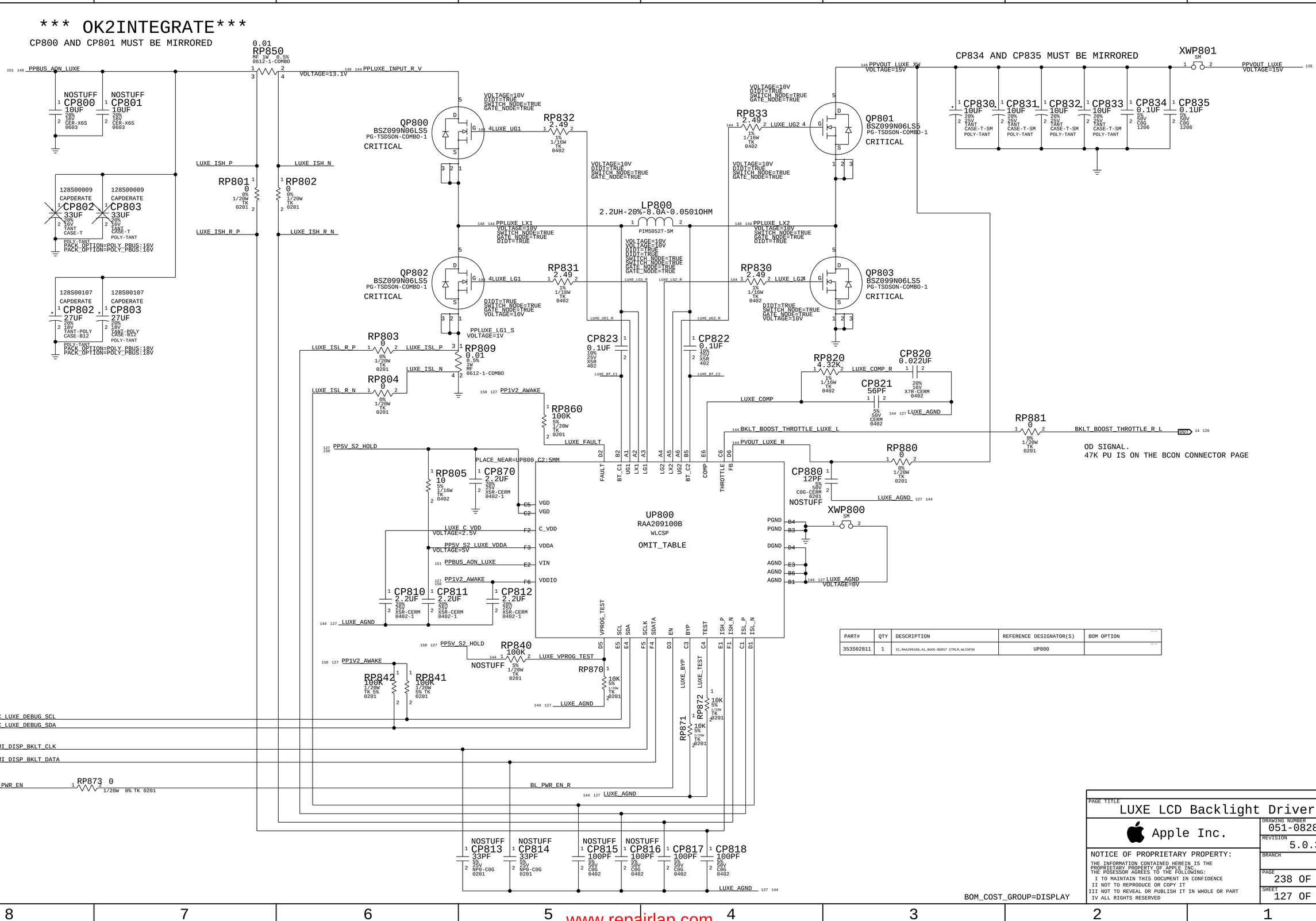

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
353S02811	1	IC,RAA209100,A1,BUCK-BOOST CTRLR,WLCSP36	UP800	

PAGE TITLE: LUXE LCD Backlight Driver

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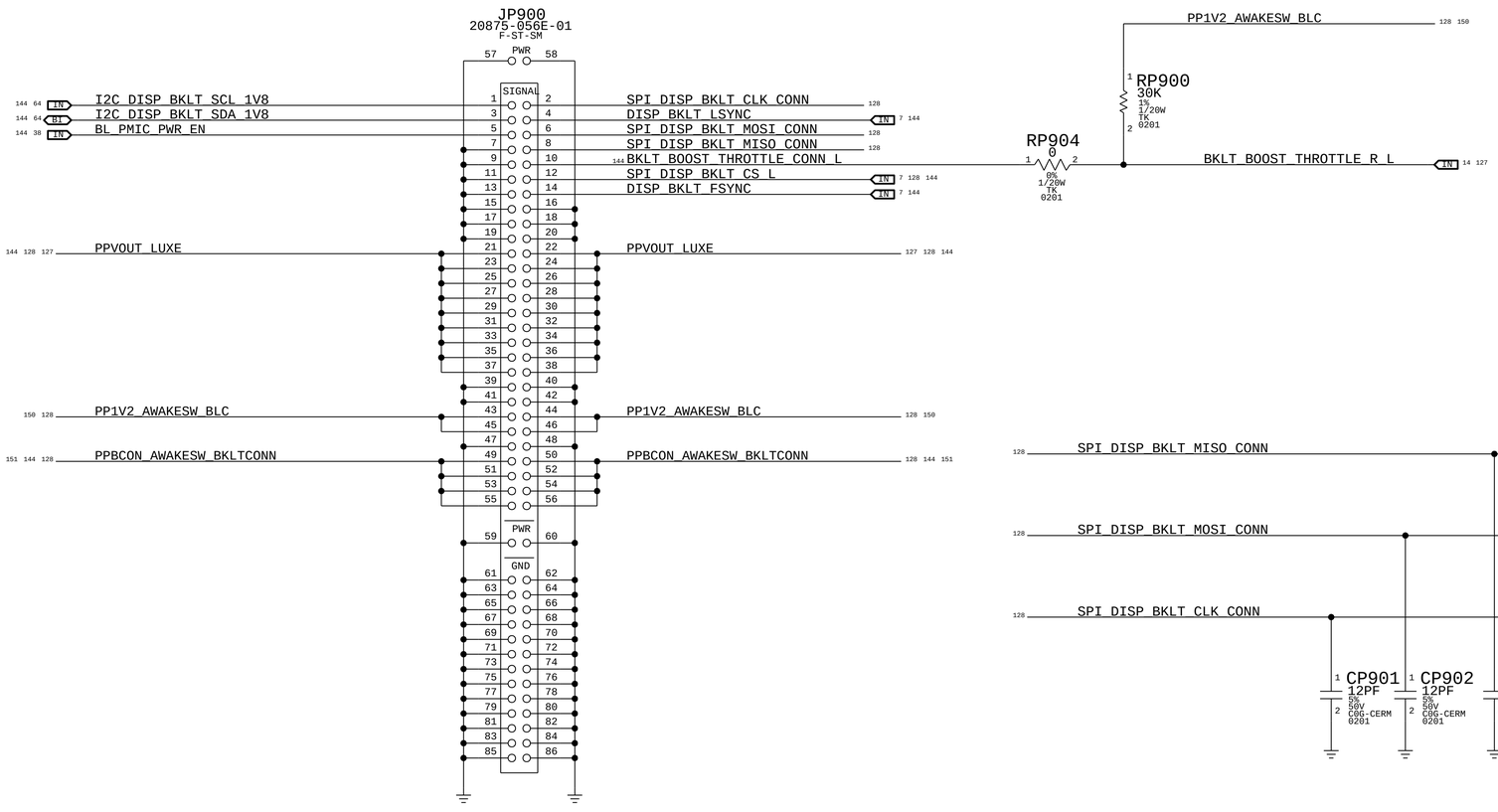

BOM_COST_GROUP=DISPLAY

PAGE TITLE: BCON CONNECTOR

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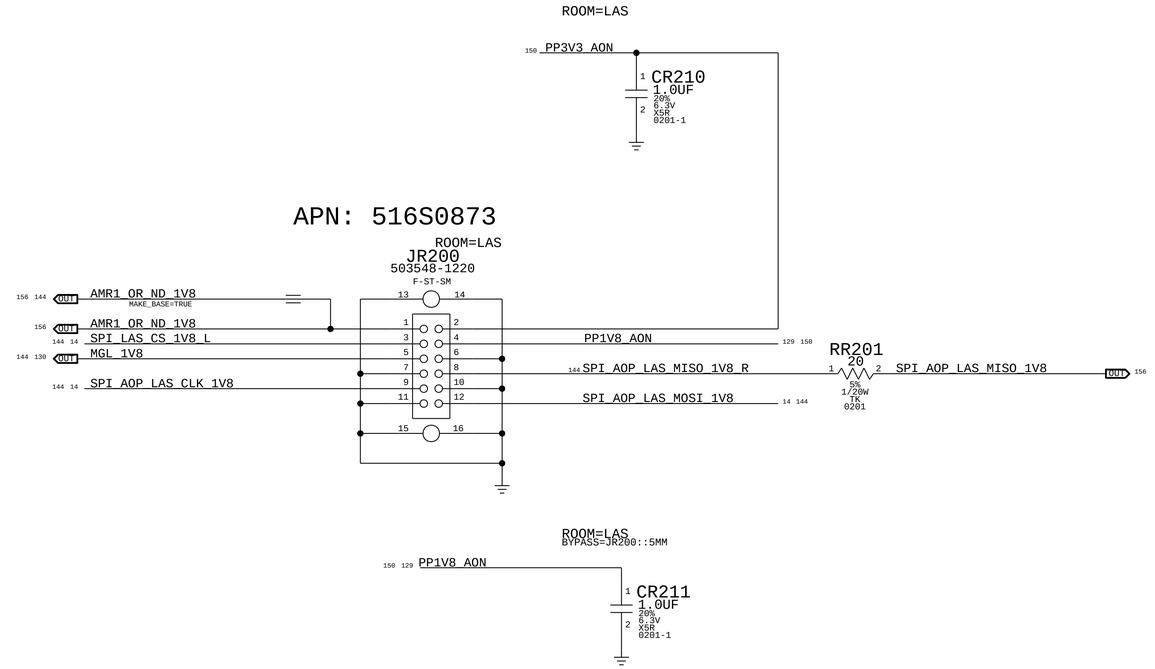

CURRENT PER RAIL

RAIL	TYPICAL	PEAK
1.2 S2	22UA	1.2MA
1.8 AON	30UA	8 MA
3.3 AON	1UA	10 MA

BOM_COST_GROUP=SOC

PAGE TITLE
SECDIS: LID ANGLE SENSOR

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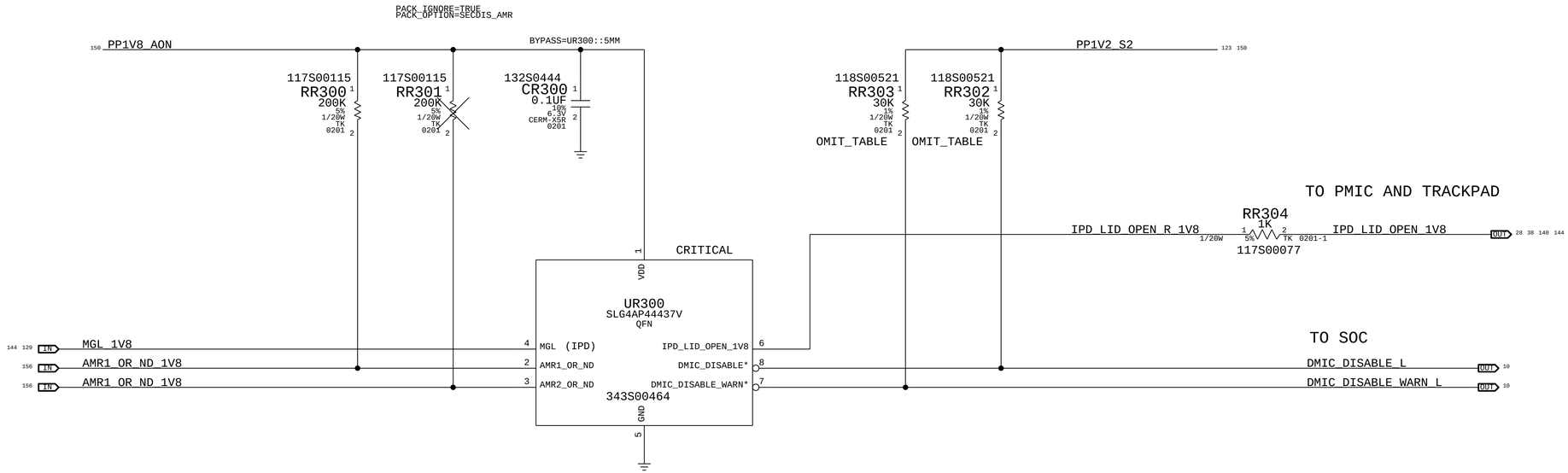
LID SECDIS LOGIC



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
117S00129	1	RES,TK,47K OHM,5%,1/20W,0201	RR302,RR303	CRITICAL	REFSECDIS_SOC_PU:47K
118S00521	1	RES,TK,30K OHM,1%,1/20W,0201	RR302,RR303	CRITICAL	REFSECDIS_SOC_PU:30K

BOM_COST_GROUP=SOC

PAGE TITLE
SECDIS: SAK

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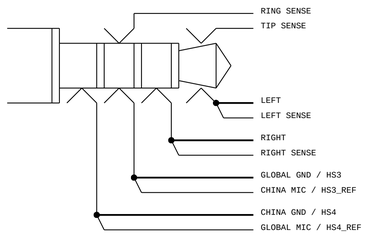
*** OK2INTEGRATE ***

CARLOW CODEC I2C ADDRESS	
ADDR PIN	ADDRESS
0R TO GND	0X48
100K TO GND	0X49
100K TO VDDIO	0X4A
0R TO VDDIO	0X4B <--

AUDIO JACK PINOUT



LR500 FERR-22-OHM-1A-0.055OHM 0201
PP1V2_AWAKE 150 — EDC CURRENT = 20MA — TDC CURRENT = 10MA
PP1V2_CODEC_VL_VD 131 — MIN_LINE_WIDTH=0.1500 — MIN_NECK_WIDTH=0.1000 — VOLTAGE=1.225V
BYPASS=UR500.A6:A7:5MM
CR500 1.0UF 20% 6.3V X5R 0201-1
BYPASS=UR500.A1:A2:5MM
CR501 0.1UF 10% 6.3V CERM-X5R 0201

LR503 FERR-22-OHM-1A-0.055OHM 0201
PP3V8_AON 150 — EDC CURRENT = 850MA — TDC CURRENT = 110MA
PP3V8_CODEC_VP 143 — MIN_LINE_WIDTH=0.3000 — MIN_NECK_WIDTH=0.2000 — VOLTAGE=3.8V
BYPASS=UR500.C7:A7:5MM
CR504 10UF 20% 10V X5R-CERM 0402-7

PP1V8_CODEC_VA — MIN_LINE_WIDTH=0.2000 — MIN_NECK_WIDTH=0.1000 — VOLTAGE=1.8V
NO_XNET_CONNECTION=1 — BYPASS=UR500.B1:C2:4MM
CR502 2.2UF 20% 35V X5R-CERM 0402-0.1MM
CODEC_AGND 131

LR501 FERR-22-OHM-1A-0.055OHM 0201 NO_XNET_CONNECTION=1
PP1V8_AWAKE 150 — * SEE NOTE — EDC CURRENT = 400MA — TDC CURRENT = 150MA

LR502 FERR-22-OHM-1A-0.055OHM 0201
PP1V8_CODEC_VCP 143 — MIN_LINE_WIDTH=0.2000 — MIN_NECK_WIDTH=0.1500 — VOLTAGE=1.8V

CODEC_CP_LDO_FILT
NO_XNET_CONNECTION=1 — BYPASS=UR500.D5:F6:5MM
CR505 2.2UF 20% 35V X5R-CERM 0402-0.1MM
NO_XNET_CONNECTION=1 — BYPASS=UR500.D6:F6:6MM
CR503 2.2UF 20% 35V X5R-CERM 0402-0.1MM
PLACE_NEAR=CR506.2:5MM
XWR500 SM
CODEC_VCP_FILT_GND — MIN_LINE_WIDTH=0.2000 — MIN_NECK_WIDTH=0.1000

CODEC_VCP_FILTP — MIN_LINE_WIDTH=0.2000 — MIN_NECK_WIDTH=0.1000
NO_XNET_CONNECTION=1 — BYPASS=UR500.E6:F6:4MM
CR506 4.7UF 20% 25V X5R 0402
NO_XNET_CONNECTION=1 — BYPASS=UR500.F6:G6:4MM
CR507 4.7UF 20% 25V X5R 0402
CODEC_VCP_FILTM — MIN_LINE_WIDTH=0.2000 — MIN_NECK_WIDTH=0.1000

PP1V2_AWAKE 132 150
PP1V2_S2 150
NOSTUFF RR502 47K 5% 1/20W TK 0201
NOSTUFF RR503 47K 5% 1/20W TK 0201

AUDIO_JACK_LEFT_OUT 135 OUT
AUDIO_JACK_RIGHT_OUT 135 OUT * SEE NOTE
NO_XNET_CONNECTION=1 — NOSTUFF RR500 1K 5% 1/20W TK 0201-1
NO_XNET_CONNECTION=1 — NOSTUFF RR501 1K 5% 1/20W TK 0201-1
CODEC_AGND 131
AUDIO_JACK_LEFT_SNS 135 IN
AUDIO_JACK_RIGHT_SNS 135 IN
AUDIO_JACK_CH_GND 135 IN
AUDIO_JACK_GB_GND 135 IN * SEE NOTE
AUDIO_JACK_GB_MIC 135 IN
CR512 0.1UF 0603 10% 50V X7R — CODEC_GB_MIC
AUDIO_JACK_CH_MIC 135 IN * SEE NOTE
CR513 0.1UF 0603 10% 50V X7R — CODEC_CH_MIC
AUDIO_JACK_RING_SNS 135 IN
AUDIO_JACK_TIP_SNS 135 IN

TO / FROM
AUDIO JACK
CONNECTOR

UR500 CRITICAL CS42L84A WLCSP

	C7	A1	A6	B1	D6		
	VDD_P	VDD_IO	VDD_D	VDD_A	VDD_CP		
F5	HP_SENSEA					D5	CP_LDO_FILT
G5	OUTA_HP					E6	CP_FILTP
F4	HP_SENSEB					G6	CP_FILTN
G4	OUTB_HP					F6	GND_CP
F1	HS4					C6	LDO_EN
E2	HS4_CLAMP					B7	IRQ*
G2	HS3					C5	WAKE*
F2	HS3_CLAMP					D4	RESET*
D1	IN_HSP					A4	MCLK
E1	IN_HSN					B2	ASP_FSYNC
G3	HS4_REF					B3	ASP_DIN
E4	HS3_REF					B4	ASP_DOUT
F3	RING_SENSE					A3	ASP_BCLK
E5	TIP_SENSE					B5	I2C_ADDR
E3	HSBIAS_FILT					B6	I2C_SDA
D3	HSBIAS_FILT_REF					A5	I2C_SCL
C1	FILTP					D7	CP_FLY1P
						E7	CP_FLY1N
						F7	CP_FLY2P
						G7	CP_FLY2N
	TSTI	GND_IO	GND_D	GND_HS	GND_A		
	C3	C4	A2	A7	G1	C2	D2

CODEC_HSBIAS_FILT — MIN_LINE_WIDTH=0.2000 — MIN_NECK_WIDTH=0.1000
BYPASS=UR500.E3:D3:4MM
CR510 4.7UF 20% 10V X5R-CERM 0402
CODEC_HSBIAS_FILT_REF — MIN_LINE_WIDTH=0.2000 — MIN_NECK_WIDTH=0.1000
CODEC_FILT — MIN_LINE_WIDTH=0.2000 — MIN_NECK_WIDTH=0.1000
NO_XNET_CONNECTION=1 — BYPASS=UR500.C1:C2:3 4MM
CR511 10UF 20% 10V X5R 0603-1
CODEC_AGND 131

XWR501 SM — PLACE_NEAR=UR500.G1:2MM — CODEC_AGND 131

RR504 47K 5% 1/20W TK 0201

TDM_CODEC_FSYNC 13 143 IN
TDM_CODEC_R2D 13 143 IN
TDM_CODEC_D2R 6 143 OUT
TDM_CODEC_BCLK 13 143 IN
TDM_CODEC_D2R_R — RR505 33 1/20W TK 0201 — PLACE_NEAR=UR500.B4:5MM
PP1V2_CODEC_VL_VD 131
I2C_CODEC_SDA 64 143 BI
I2C_CODEC_SCL 64 143 IN

CODEC_FLY1P — MIN_LINE_WIDTH=0.2000 — MIN_NECK_WIDTH=0.1000
CODEC_FLY1M — NO_XNET_CONNECTION=1 — BYPASS=UR500.D7:E7:4MM
CODEC_FLY2P — CR508 4.7UF 20% 25V X5R 0402 — MIN_LINE_WIDTH=0.2000 — MIN_NECK_WIDTH=0.1000
CODEC_FLY2M — MIN_LINE_WIDTH=0.2000 — MIN_NECK_WIDTH=0.1000 — NO_XNET_CONNECTION=1 — BYPASS=UR500.F7:G7:4MM — CR509 4.7UF 20% 25V X5R 0402 — MIN_LINE_WIDTH=0.2000 — MIN_NECK_WIDTH=0.1000

CODEC_INT_L 6 143 OUT -> TO SOC
CODEC_WAKE_L 46 143 OUT -> TO PMU
CODEC_RESET_L 10 143 IN <- FROM SOC

NOTES:

- SEE TEST POINT SIGNALS & LOCATIONS ON REF DESIGN PAGE 1

- THE FOLLOWING SIGNALS SHOULD HAVE A LOW DCR PATH:
  - VP SUPPLY
  - VCP SUPPLY
  - AUDIO_JACK_LEFT/RIGHT_OUT
  - AUDIO_JACK_GB/CH_GND

- GB_MIC SIGNAL CONNECTS TO CH_GND AT A/J CONNECTOR.
  CH_MIC SIGNAL CONNECTS TO GB_GND AT A/J CONNECTOR.

- VP SUPPLY RAIL ACCEPTS 3.0V TO 5.25V AND NEEDS TO
  COME UP FIRST AND TURN OFF LAST (NEED TO STAY UP
  WHEN THE OTHER RAILS GO DOWN)
  VP CURRENT CONSUMPTION WITH PART IN LOWEST POWER STATE:
  3.1UA (1V8 OFF, RST# LOW)
  TBD (1V8 ON, RST# LOW)
  37UA (1V8 OFF, RST# HIGH)

CARLOW B0 SILICON

BOM_COST_GROUP=AUDIO

PAGE TITLE: AUDIO JACK CODEC

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*** OK2INTEGRATE ***

PP1V8_AWAKE
PP1V2_AWAKE

SPKRAMP_A_DREG
CR600 1.0UF 20% 6.3V X5R 0201-1
CR601 1.0UF 20% 6.3V X5R 0201-1
CR602 1.0UF 20% 6.3V X5R 0201-1

UR600
SN012776B0B
DSBGA
SPKRAMP_A
353S03375
TAWANG
B0B

I2C_SPKRAMP_L_SCL
I2C_SPKRAMP_L_SDA
SPKRAMP_A_ADDR
TDM_SPKRAMP_L_BCLK
TDM_SPKRAMP_L_FSYNC
TDM_SPKRAMP_L_R2D
TDM_SPKRAMP_L_D2R
SPKRAMP_ABC_ICC
TP_SPKRAMP_A_LV_EN
SPKRAMP_INT_L
SPKRAMP_RESET_L

RR600 33 5% 1/20W TK 0201 — TDM_SPKRAMP_A_D2R_R
RR601 33 5% 1/20W TK 0201 — SPKRAMP_A_ICC_R

SPKRAMP_A_BOOTP — CR608 0.1UF 10% 25V X5R — SPKRAMP_A_BOOTP_R
SPKRAMP_A_BOOTN — CR609 0.1UF 10% 25V X5R — SPKRAMP_A_BOOTN_R
SPKRAMP_A_OUTP_R — RR602 0 — SPKRAMP_A_OUTP
SPKRAMP_A_OUTN_R — RR603 0 — SPKRAMP_A_OUTN

CR603 0.1UF 10% 25V X5R 0201
CR604 10UF 20% 25V X5R-CERM 0603
CR605 10UF 20% 25V X5R-CERM 0603
CR606 0.1UF 10% 25V X5R 0201
CR607 10UF 20% 10V X5R-CERM 0402-7

PP3V8_AON — MAX CURRENT EDC = 1A (PER AMP)
PPBUS_AON_SPKRAMP_ABC — MAX CURRENT EDC = 4A (PER AMP)
XWR600 SHORT-18L-0.1MM-SM
SPKRAMP_A_PVDD_SNS
SPKRAMP_A_VSENSEP
SPKRAMP_A_VSENSEN

CR610 12PF 5% 25V CERM 0201 — OMIT_TABLE
CR611 12PF 5% 25V CERM 0201 — OMIT_TABLE

AMP A

RR605 0 — SPKRAMP_A_ADDR 0x70
RR635 470 — SPKRAMP_B_ADDR 0x72
RR664 470 — SPKRAMP_C_ADDR 0x74

PP1V2_AWAKE
NOSTUFF RR691 47K
SPKRAMP_INT_L
SPKRAMP_RESET_L
RR692 47K

THIS RESISTOR TIES ICC SIGNAL
BETWEEN AMPS A,B,C AND AMPS D,E,F:
0R --> GLOBAL ICC (ABCDEF)
DNE --> LOCAL ICC (ABC, DEF)

SPKRAMP_ICC_GB
RR693 0
SPKRAMP_ABC_ICC — SPKRAMP_DEF_ICC

NOTES:
- SEE TEST POINTS SIGNALS AND LOCATIONS ON REF DESIGN PAGE 1.
- VSENSEP/N SIGNALS CONNECT TO OUTP/N SIGNALS AT THE SPEAKER CONNECTOR PINS.
- PVDD_SNS XW SHOULD BE LOCATED BY MAIN PBUS SHAPE.
- THE FOLLOWING SIGNALS SHOULD HAVE A VERY LOW DCR PATH:
  - SPKRAMP_XX_OUTP/N_R
  - SPKRAMP_XX_OUTP/N
  - PVDD SUPPLY
- FOR THERMALS PGND PINS MUST CONNECT TO GND LAYERS USING COPIOUS AMOUNT OF VIAS.
- BULK CAPACITORS SHOULD BE ADDED TO SPEAKER CONNECTOR PAGE.

BOM_COST_GROUP=AUDIO

PAGE TITLE: AUDIO AMPLIFIERS (1/2)
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*** OK2INTEGRATE ***

AMP D

PP1V8_AWAKE
PP1V2_AWAKE
PP3V8_AON
MAX CURRENT EDC = 1A (PER AMP)
PPBUS_AON_SPKRAMP_DEF
MAX CURRENT EDC = 4A (PER AMP)

SPKRAMP_D_DREG
CR700 1.0UF 20% 6.3V X5R 0201-1 — SPKRAMP_D PLACE_NEAR=UR700.E5:5MM
CR701 1.0UF 20% 6.3V X5R 0201-1 — SPKRAMP_D PLACE_NEAR=UR700.F3:5MM
CR702 1.0UF 20% 6.3V X5R 0201-1 — SPKRAMP_D PLACE_NEAR=UR700.C2:5MM

CR703 0.1UF 10% 25V X5R 0201 — SPKRAMP_D PLACE_NEAR=UR700.C5:5MM
CR704 10UF 20% 25V X5R-CERM 0603 — SPKRAMP_D PLACE_NEAR=UR700.C5:10MM
CR705 10UF 20% 25V X5R-CERM 0603 — SPKRAMP_D PLACE_NEAR=UR700.C5:10MM
CR706 0.1UF 10% 25V X5R 0201 — SPKRAMP_D PLACE_NEAR=UR700.D5:5MM
CR707 10UF 20% 10V X5R-CERM 0402-7 — SPKRAMP_D PLACE_NEAR=UR700.D5:10MM

XWR700 SHORT-10L-0.1MM-SM * SEE NOTE — SPKRAMP_D

UR700 SN012776B0B DSBGA — SPKRAMP_D 353S03375 — TAWANG B0B

C2	DREG	
C3	PVDD_SNS	SPKRAMP_D_PVDD_SNS
B1	VSNS_P	SPKRAMP_D_VSENSEP (* SEE NOTE) → SPKRAMP_D IN 134
A1	VSNS_N	SPKRAMP_D_VSENSEN → SPKRAMP_D IN 134
F2	SCL	I2C_SPKRAMP_R_SCL (SPKRAMP_D 143 64 IN)
F1	SDA	I2C_SPKRAMP_R_SDA (SPKRAMP_D 143 64 BI)
D4	ADDR	SPKRAMP_D_ADDR (133)
E1	SBCLK	TDM_SPKRAMP_R_BCLK (SPKRAMP_D 143 13 IN)
D2	FSYNC	TDM_SPKRAMP_R_FSYNC (SPKRAMP_D 143 13 IN)
E2	SDIN	TDM_SPKRAMP_R_R2D (SPKRAMP_D 143 13 IN)
D1	SDOUT	TDM_SPKRAMP_R_D2R (SPKRAMP_D 143 13 OUT) via RR700 33 5% 1/20W TK 0201 (SPKRAMP_D PLACE_NEAR=UR700.D1:10MM) → TDM_SPKRAMP_D_D2R_R
F5	ICC	SPKRAMP_DEF_ICC_R (133) via RR701 33 5% 1/20W TK 0201 (SPKRAMP_D PLACE_NEAR=UR700.F5:10MM) → SPKRAMP_D_ICC_R
D3	BYP_EN	TP_SPKRAMP_D_LV_EN (143)
E3	IRQ*	SPKRAMP_INT_L (SPKRAMP_D 133 132 143 6 OUT)
F4	SD*	SPKRAMP_RESET_L (SPKRAMP_D 133 132 143 6 IN)
E5	AVDD	
C4	PVDD	
C5	PVDD	
D5	VBAT1S	
F3	IOVDD	
E4	GND	
C1	GND	
B4	PGND	
A4	PGND	

SPKRAMP_D_BOOTP — CR708 0.1UF 10% 25V X5R 0201 — MIN_LINE_WIDTH=0.1000
SPKRAMP_D_OUTP_R — MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.1000 SWITCH_NODE=TRUE
SPKRAMP_D_OUTN_R — MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.1000 SWITCH_NODE=TRUE
SPKRAMP_D_BOOTN — CR709 0.1UF 10% 25V X5R 0201 — MIN_LINE_WIDTH=0.1000
SPKRAMP_D BYPASS=UR700.B2:B3:10MM NO_XNET_CONNECTION=1

RR702 0 1% 1/1W 0603 1/5W — MIN_NECK_WIDTH=0.1000 MIN_LINE_WIDTH=0.4000 SWITCH_NODE=TRUE
RR703 0 1% 1/1W 0603 1/5W — MIN_NECK_WIDTH=0.1000 MIN_LINE_WIDTH=0.4000 SWITCH_NODE=TRUE

SPKRAMP_D_OUTP (* SEE NOTE) → SPKRAMP_D OUT 134 144
SPKRAMP_D_OUTN (* SEE NOTE) → SPKRAMP_D OUT 134 144

CR710 12PF 5% 25V CERM 0201 — OMIT_TABLE
CR711 12PF 5% 25V CERM 0201 — OMIT_TABLE

RR705 2.2K 5% 1/20W TK 0201 — SPKRAMP_D_ADDR 0X76
RR734 2.2K 5% 1/20W TK 0201 — SPKRAMP_E_ADDR 0X78
RR765 10K 5% 1/20W TK 0201 — SPKRAMP_F_ADDR 0X7A

RR706 0 0% 1/20W TK 0201 — SPKRAMP_DEF_ICC (SPKRAMP_D 143 132 BI) → SPKRAMP_DEF_ICC_R (133)
RR707 0 0% 1/20W TK 0201 — NOSTUFF

RR706 TO REDUCE STUB LENGTH FOR LOCAL ICC OPERATION. RR707 PROVIDES THE OPTION TO GND FLOATING SPKRAMP_DEF_ICC TRACE

AMP E

PP1V8_AWAKE
PP1V2_AWAKE
PP3V8_AON
PPBUS_AON_SPKRAMP_DEF

SPKRAMP_E_DREG
CR730 1.0UF 20% 6.3V X5R 0201-1 — SPKRAMP_E PLACE_NEAR=UR730.E5:5MM
CR731 1.0UF 20% 6.3V X5R 0201-1 — SPKRAMP_E PLACE_NEAR=UR730.F3:5MM
CR732 1.0UF 20% 6.3V X5R 0201-1 — SPKRAMP_E PLACE_NEAR=UR730.C2:5MM

CR733 0.1UF 10% 25V X5R 0201 — SPKRAMP_E PLACE_NEAR=UR730.C5:5MM
CR734 10UF 20% 25V X5R-CERM 0603 — SPKRAMP_E PLACE_NEAR=UR730.C5:10MM
CR735 10UF 20% 25V X5R-CERM 0603 — SPKRAMP_E PLACE_NEAR=UR730.C5:10MM
CR736 0.1UF 10% 25V X5R 0201 — SPKRAMP_E PLACE_NEAR=UR730.D5:5MM
CR737 10UF 20% 10V X5R-CERM 0402-7 — SPKRAMP_E PLACE_NEAR=UR730.D5:10MM

XWR701 SHORT-10L-0.1MM-SM * SEE NOTE — SPKRAMP_E

UR730 SN012776B0B DSBGA — SPKRAMP_E 353S03375 — TAWANG B0B

C2	DREG	
C3	PVDD_SNS	SPKRAMP_E_PVDD_SNS
B1	VSNS_P	SPKRAMP_E_VSENSEP (* SEE NOTE) → SPKRAMP_E IN 134
A1	VSNS_N	SPKRAMP_E_VSENSEN → SPKRAMP_E IN 134
F2	SCL	I2C_SPKRAMP_R_SCL (SPKRAMP_E 64 IN)
F1	SDA	I2C_SPKRAMP_R_SDA (SPKRAMP_E 64 BI)
D4	ADDR	SPKRAMP_E_ADDR (133)
E1	SBCLK	TDM_SPKRAMP_R_BCLK (SPKRAMP_E 13 IN)
D2	FSYNC	TDM_SPKRAMP_R_FSYNC (SPKRAMP_E 13 IN)
E2	SDIN	TDM_SPKRAMP_R_R2D (SPKRAMP_E 13 IN)
D1	SDOUT	TDM_SPKRAMP_R_D2R (SPKRAMP_E 13 OUT) via RR730 33 5% 1/20W TK 0201 (SPKRAMP_E PLACE_NEAR=UR730.D1:10MM) → TDM_SPKRAMP_E_D2R_R
F5	ICC	SPKRAMP_DEF_ICC_R (133) via RR731 33 5% 1/20W TK 0201 (SPKRAMP_E PLACE_NEAR=UR730.F5:10MM) → SPKRAMP_E_ICC_R
D3	BYP_EN	TP_SPKRAMP_E_LV_EN (143)
E3	IRQ*	SPKRAMP_INT_L (SPKRAMP_E 133 132 143 6 OUT)
F4	SD*	SPKRAMP_RESET_L (SPKRAMP_E 133 132 143 6 IN)
E5	AVDD	
C4	PVDD	
C5	PVDD	
D5	VBAT1S	
F3	IOVDD	
E4	GND	
C1	GND	
B4	PGND	
A4	PGND	

SPKRAMP_E_BOOTP — CR738 0.1UF 10% 25V X5R 0201 — MIN_LINE_WIDTH=0.1000
SPKRAMP_E_OUTP_R — MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.1000 SWITCH_NODE=TRUE
SPKRAMP_E_OUTN_R — MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.1000 SWITCH_NODE=TRUE
SPKRAMP_E_BOOTN — CR739 0.1UF 10% 25V X5R 0201 — MIN_LINE_WIDTH=0.1000
SPKRAMP_E BYPASS=UR730.B2:B3:10MM NO_XNET_CONNECTION=1

RR732 0 1% 1/1W 0603 1/5W — MIN_NECK_WIDTH=0.1000 MIN_LINE_WIDTH=0.4000 SWITCH_NODE=TRUE
RR733 0 1% 1/1W 0603 1/5W — MIN_NECK_WIDTH=0.1000 MIN_LINE_WIDTH=0.4000 SWITCH_NODE=TRUE

SPKRAMP_E_OUTP (* SEE NOTE) → SPKRAMP_E OUT 134 144
SPKRAMP_E_OUTN (* SEE NOTE) → SPKRAMP_E OUT 134 144

CR740 12PF 5% 25V CERM 0201 — OMIT_TABLE
CR741 12PF 5% 25V CERM 0201 — OMIT_TABLE

AMP F

PP1V8_AWAKE
PP1V2_AWAKE
PP3V8_AON
PPBUS_AON_SPKRAMP_DEF

SPKRAMP_F_DREG
CR760 1.0UF 20% 6.3V X5R 0201-1 — SPKRAMP_F PLACE_NEAR=UR760.E5:5MM
CR761 1.0UF 20% 6.3V X5R 0201-1 — SPKRAMP_F PLACE_NEAR=UR760.F3:5MM
CR762 1.0UF 20% 6.3V X5R 0201-1 — SPKRAMP_F PLACE_NEAR=UR760.C2:5MM

CR763 0.1UF 10% 25V X5R 0201 — SPKRAMP_F PLACE_NEAR=UR760.C5:5MM
CR764 10UF 20% 25V X5R-CERM 0603 — SPKRAMP_F PLACE_NEAR=UR760.C5:10MM
CR765 10UF 20% 25V X5R-CERM 0603 — SPKRAMP_F PLACE_NEAR=UR760.C5:10MM
CR766 0.1UF 10% 25V X5R 0201 — SPKRAMP_F PLACE_NEAR=UR760.D5:5MM
CR767 10UF 20% 10V X5R-CERM 0402-7 — SPKRAMP_F PLACE_NEAR=UR760.D5:10MM

XWR702 SHORT-10L-0.1MM-SM * SEE NOTE — SPKRAMP_F

UR760 SN012776B0B DSBGA — SPKRAMP_F 353S03375 — TAWANG B0B

C2	DREG	
C3	PVDD_SNS	SPKRAMP_F_PVDD_SNS
B1	VSNS_P	SPKRAMP_F_VSENSEP (* SEE NOTE) → SPKRAMP_F IN 134
A1	VSNS_N	SPKRAMP_F_VSENSEN → SPKRAMP_F IN 134
F2	SCL	I2C_SPKRAMP_R_SCL (SPKRAMP_F 64 IN)
F1	SDA	I2C_SPKRAMP_R_SDA (SPKRAMP_F 64 BI)
D4	ADDR	SPKRAMP_F_ADDR (133)
E1	SBCLK	TDM_SPKRAMP_R_BCLK (SPKRAMP_F 13 IN)
D2	FSYNC	TDM_SPKRAMP_R_FSYNC (SPKRAMP_F 13 IN)
E2	SDIN	TDM_SPKRAMP_R_R2D (SPKRAMP_F 13 IN)
D1	SDOUT	TDM_SPKRAMP_R_D2R (SPKRAMP_F 13 OUT) via RR760 33 5% 1/20W TK 0201 (SPKRAMP_F PLACE_NEAR=UR760.D1:10MM) → TDM_SPKRAMP_F_D2R_R
F5	ICC	SPKRAMP_DEF_ICC_R (133) via RR761 33 5% 1/20W TK 0201 (SPKRAMP_F PLACE_NEAR=UR760.F5:10MM) → SPKRAMP_F_ICC_R
D3	BYP_EN	TP_SPKRAMP_F_LV_EN (143)
E3	IRQ*	SPKRAMP_INT_L (SPKRAMP_F 133 132 143 6 OUT)
F4	SD*	SPKRAMP_RESET_L (SPKRAMP_F 133 132 143 6 IN)
E5	AVDD	
C4	PVDD	
C5	PVDD	
D5	VBAT1S	
F3	IOVDD	
E4	GND	
C1	GND	
B4	PGND	
A4	PGND	

SPKRAMP_F_BOOTP — CR768 0.1UF 10% 25V X5R 0201 — MIN_LINE_WIDTH=0.1000
SPKRAMP_F_OUTP_R — MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.1000 SWITCH_NODE=TRUE
SPKRAMP_F_OUTN_R — MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.1000 SWITCH_NODE=TRUE
SPKRAMP_F_BOOTN — CR769 0.1UF 10% 25V X5R 0201 — MIN_LINE_WIDTH=0.1000
SPKRAMP_F BYPASS=UR760.B2:B3:10MM NO_XNET_CONNECTION=1

RR762 0 1% 1/1W 0603 1/5W — MIN_NECK_WIDTH=0.1000 MIN_LINE_WIDTH=0.4000 SWITCH_NODE=TRUE
RR763 0 1% 1/1W 0603 1/5W — MIN_NECK_WIDTH=0.1000 MIN_LINE_WIDTH=0.4000 SWITCH_NODE=TRUE

SPKRAMP_F_OUTP (* SEE NOTE) → SPKRAMP_F OUT 134 144
SPKRAMP_F_OUTN (* SEE NOTE) → SPKRAMP_F OUT 134 144

CR770 12PF 5% 25V CERM 0201 — OMIT_TABLE
CR771 12PF 5% 25V CERM 0201 — OMIT_TABLE

NOTES:
- SEE TEST POINTS SIGNALS AND LOCATIONS ON REF DESIGN PAGE 1.
- VSENSEP/N SIGNALS CONNECT TO OUTP/N SIGNALS AT THE SPEAKER CONNECTOR PINS.
- PVDD_SNS XW SHOULD BE LOCATED BY MAIN PBUS SHAPE.
- THE FOLLOWING SIGNALS SHOULD HAVE A VERY LOW DCR PATH:
  - SPKRAMP_XX_OUTP/N_R
  - SPKRAMP_XX_OUTP/N
  - PVDD SUPPLY
- FOR THERMALS PGND PINS MUST CONNECT TO GND LAYERS USING COPIOUS AMOUNT OF VIAS.
- BULK CAPACITORS SHOULD BE ADDED TO SPEAKER CONNECTOR PAGE.

BOM_COST_GROUP=AUDIO

PAGE TITLE: AUDIO AMPLIFIERS (2/2)

Apple Inc.

DRAWING NUMBER: 051-08286 | SIZE: D
REVISION: 5.0.3
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PAGE: 247 OF 700
SHEET: 133 OF 168

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LEFT AUDIO SPEAKER CONNECTOR

NO_XNET_CONNECTION=1
NO_XNET_CONNECTION=1
NO_XNET_CONNECTION=1
NO_XNET_CONNECTION=1
NO_XNET_CONNECTION=1
NO_XNET_CONNECTION=1

132 OUT SPKRAMP_A_VSENSEP — XWR800 SHORT-16L-0.1MM-SM — PLACE_NEAR=JR800.5:10MM
132 OUT SPKRAMP_A_VSENSEN — XWR801 SHORT-16L-0.1MM-SM — PLACE_NEAR=JR800.6:10MM
132 OUT SPKRAMP_B_VSENSEP — XWR802 SHORT-16L-0.1MM-SM — PLACE_NEAR=JR800.7:10MM
132 OUT SPKRAMP_B_VSENSEN — XWR803 SHORT-16L-0.1MM-SM — PLACE_NEAR=JR800.8:10MM
132 OUT SPKRAMP_C_VSENSEP — XWR804 SHORT-16L-0.1MM-SM — PLACE_NEAR=JR800.1:10MM
132 OUT SPKRAMP_C_VSENSEN — XWR805 SHORT-16L-0.1MM-SM — PLACE_NEAR=JR800.2:10MM

516S00787
JR800
247129004101829
F-ST-SM

144 134 132 SPKRAMP_A_OUTP — 5 PWR 6 — SPKRAMP_A_OUTN 132 134 144
144 134 132 SPKRAMP_C_OUTP — 1 PWR 2 — SPKRAMP_C_OUTN 132 134 144
144 134 6 SPKR_ID0 — 3 PWR 4
144 134 132 SPKRAMP_B_OUTP — 7 PWR 8 — SPKRAMP_B_OUTN 132 134 144

13, 9, 10, 11, 12, 14

L Woofer 1
L Woofer 2
L Tweeter

144 134 132 IN SPKRAMP_A_OUTP
144 134 132 IN SPKRAMP_A_OUTN
144 134 132 IN SPKRAMP_B_OUTP
144 134 132 IN SPKRAMP_B_OUTN
144 134 132 IN SPKRAMP_C_OUTP
144 134 132 IN SPKRAMP_C_OUTN
144 134 6 OUT SPKR_ID0

RIGHT AUDIO SPEAKER CONNECTOR

NO_XNET_CONNECTION=1
NO_XNET_CONNECTION=1
NO_XNET_CONNECTION=1
NO_XNET_CONNECTION=1
NO_XNET_CONNECTION=1
NO_XNET_CONNECTION=1

133 OUT SPKRAMP_D_VSENSEP — XWR850 SHORT-16L-0.1MM-SM — PLACE_NEAR=JR850.5:10MM
133 OUT SPKRAMP_D_VSENSEN — XWR851 SHORT-16L-0.1MM-SM — PLACE_NEAR=JR850.6:10MM
133 OUT SPKRAMP_E_VSENSEP — XWR852 SHORT-16L-0.1MM-SM — PLACE_NEAR=JR850.7:10MM
133 OUT SPKRAMP_E_VSENSEN — XWR853 SHORT-16L-0.1MM-SM — PLACE_NEAR=JR850.8:10MM
133 OUT SPKRAMP_F_VSENSEP — XWR854 SHORT-16L-0.1MM-SM — PLACE_NEAR=JR850.3:10MM
133 OUT SPKRAMP_F_VSENSEN — XWR855 SHORT-16L-0.1MM-SM — PLACE_NEAR=JR850.4:10MM

516S00787
JR850
247129004101829
F-ST-SM

144 134 133 SPKRAMP_D_OUTP — 5 PWR 6 — SPKRAMP_D_OUTN 133 134 144
144 134 6 SPKR_ID1 — 1 PWR 2
144 134 133 SPKRAMP_F_OUTP — 3 PWR 4 — SPKRAMP_F_OUTN 133 134 144
144 134 133 SPKRAMP_E_OUTP — 7 PWR 8 — SPKRAMP_E_OUTN 133 134 144

13, 9, 10, 11, 12, 14

R Woofer 1
R Woofer 2
R Tweeter

144 134 133 IN SPKRAMP_D_OUTP
144 134 133 IN SPKRAMP_D_OUTN
144 134 133 IN SPKRAMP_E_OUTP
144 134 133 IN SPKRAMP_E_OUTN
144 134 133 IN SPKRAMP_F_OUTP
144 134 133 IN SPKRAMP_F_OUTN
144 134 6 OUT SPKR_ID1

DUMMY 0201 CAPS

PLACE_NEAR=UR600:5mm — CR860 10UF 20% 10V X5R-CERM 0402-7 — CKPLUS_WAIVE=TERMSHORTED
PLACE_NEAR=UR600:5mm — CR861 10UF 20% 10V X5R-CERM 0402-7 — CKPLUS_WAIVE=TERMSHORTED
PLACE_NEAR=UR600:5mm — CR862 10UF 20% 10V X5R-CERM 0402-7 — CKPLUS_WAIVE=TERMSHORTED

RIGHT AMPLIFIERS BULK CAPACITANCE

PPBUS_AON_SPKRAMP_DEF 133 134 151

128S00009 CR850 33UF 20% 16V TANT CASE-T
128S00009 CR851 33UF 20% 16V TANT CASE-T
128S00009 CR852 33UF 20% 16V TANT CASE-T
128S00009 CR853 33UF 20% 16V TANT CASE-T

PACK_IGNORE=TRUE
PACK_OPTION=POLY_PBUS:16V

PPBUS_AON_SPKRAMP_DEF 133 134 151

128S00107 CR850 27UF 20% 18V TANT-POLY CASE-B12
128S00107 CR851 27UF 20% 18V TANT-POLY CASE-B12
128S00107 CR852 27UF 20% 18V TANT-POLY CASE-B12
128S00107 CR853 27UF 20% 18V TANT-POLY CASE-B12

PACK_OPTION=POLY_PBUS:18V

PPBUS_AON_SPKRAMP_DEF 133 134 151

128S00009 CR854 33UF 20% 16V TANT CASE-T
128S00009 CR855 33UF 20% 16V TANT CASE-T
128S00009 CR856 33UF 20% 16V TANT CASE-T
128S00009 CR857 33UF 20% 16V TANT CASE-T

PACK_IGNORE=TRUE
PACK_OPTION=POLY_PBUS:16V

PPBUS_AON_SPKRAMP_DEF 133 134 151

128S00107 CR854 27UF 20% 18V TANT-POLY CASE-B12
128S00107 CR855 27UF 20% 18V TANT-POLY CASE-B12
128S00107 CR856 27UF 20% 18V TANT-POLY CASE-B12
128S00107 CR857 27UF 20% 18V TANT-POLY CASE-B12

PACK_OPTION=POLY_PBUS:18V

LEFT AMPLIFIERS BULK CAPACITANCE

PPBUS_AON_SPKRAMP_ABC 132 134 151

128S00107 CR800 27UF 20% 18V TANT-POLY CASE-B12
128S00107 CR801 27UF 20% 18V TANT-POLY CASE-B12
128S00107 CR802 27UF 20% 18V TANT-POLY CASE-B12
128S00107 CR803 27UF 20% 18V TANT-POLY CASE-B12

PACK_OPTION=POLY_PBUS:18V

PPBUS_AON_SPKRAMP_ABC 132 134 151

128S00107 CR804 27UF 20% 18V TANT-POLY CASE-B12
128S00107 CR805 27UF 20% 18V TANT-POLY CASE-B12
128S00107 CR806 27UF 20% 18V TANT-POLY CASE-B12
128S00107 CR807 27UF 20% 18V TANT-POLY CASE-B12

PACK_OPTION=POLY_PBUS:18V

PPBUS_AON_SPKRAMP_ABC 132 134 151

128S00009 CR800 33UF 20% 16V TANT CASE-T
128S00009 CR801 33UF 20% 16V TANT CASE-T
128S00009 CR802 33UF 20% 16V TANT CASE-T
128S00009 CR803 33UF 20% 16V TANT CASE-T

PACK_IGNORE=TRUE
PACK_OPTION=POLY_PBUS:16V

PPBUS_AON_SPKRAMP_ABC 132 134 151

128S00009 CR804 33UF 20% 16V TANT CASE-T
128S00009 CR805 33UF 20% 16V TANT CASE-T
128S00009 CR806 33UF 20% 16V TANT CASE-T
128S00009 CR807 33UF 20% 16V TANT CASE-T

PACK_IGNORE=TRUE
PACK_OPTION=POLY_PBUS:16V

BOM_COST_GROUP=AUDIO

PAGE TITLE
AUDIO CONNECTORS: AMPS

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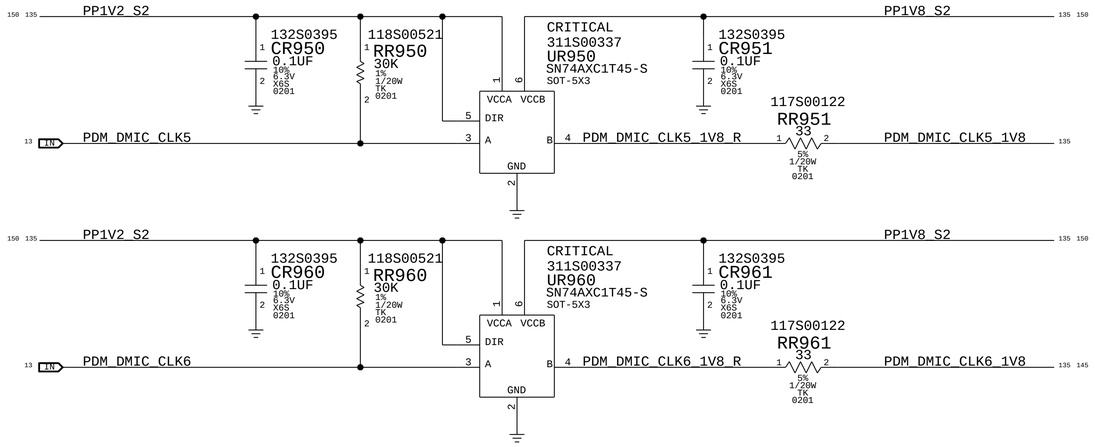
LEVEL SHIFTERS: DMIC CLOCK

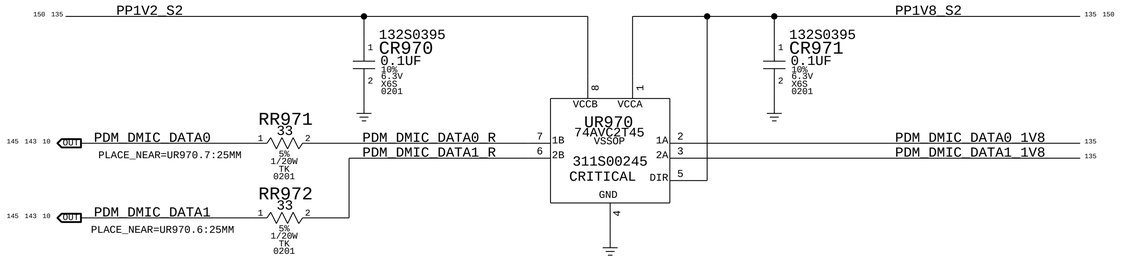
TWO SEPARATE SINGLE BIT LS FOR XTALK CONCERNS <RDAR://70058941> -- MAY CHANGE TO DUAL SHIFTER



LEVEL SHIFTER: DMIC DATA

HIGH ON DIR IS A -> B

BOTH A AND B SIDE CAN BE ANY VOLTAGE FROM 0.8 TO 3.6



Digital Mic Flex Connector

APN: 518S0818

JR940
FF14A-6C-R11DL-B-3H
F-RT-SM

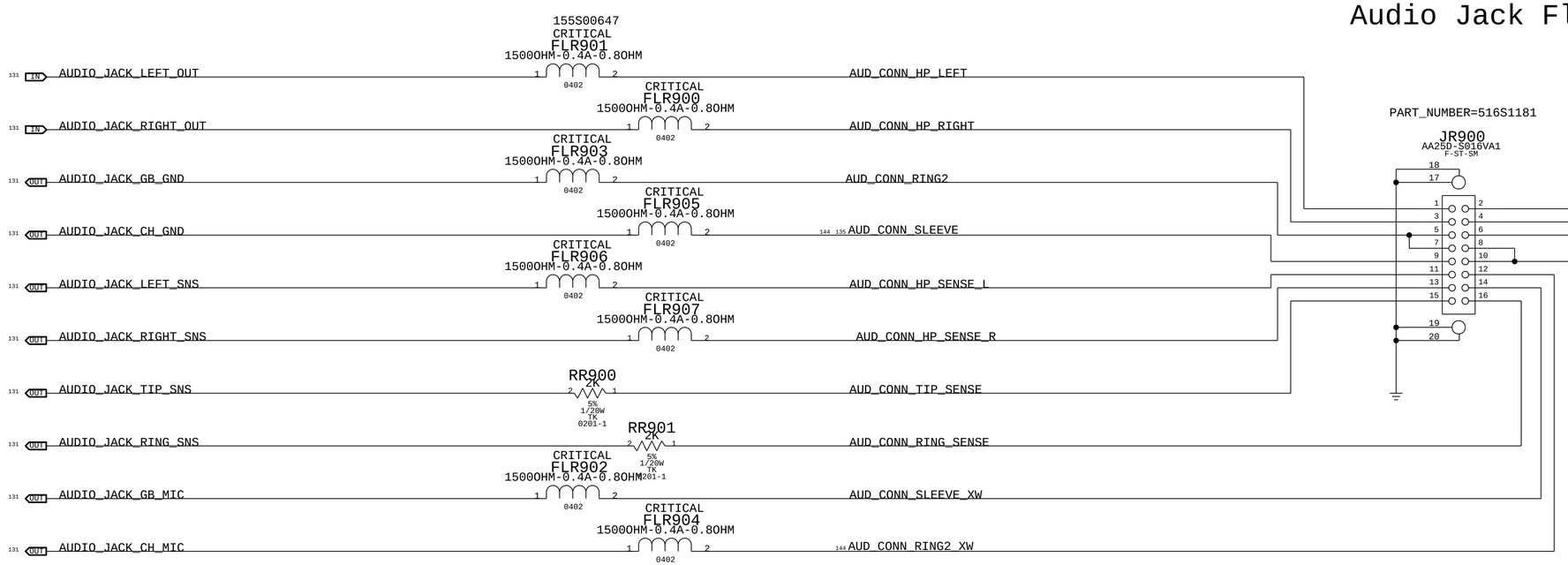
PDM_DMIC_CLK5_1V8
PDM_DMIC_DATA0_1V8
PP1V8_DMIC
PDM_DMIC_CLK6_1V8
PDM_DMIC_DATA1_1V8

LR940
FERR-470-OHM-215MA-1.5OHM
0201
PP1V8_S2

CR940
1UF
20%
16V
CER-X5R
0201

PDM_DMIC_CLK5_1V8 — MAKE_BASE=TRUE — PDM_DMIC_CLK5_1V8
PDM_DMIC_DATA0_1V8 — MAKE_BASE=TRUE — PDM_DMIC_DATA0_1V8
PDM_DMIC_CLK6_1V8 — MAKE_BASE=TRUE — PDM_DMIC_CLK6_1V8
PDM_DMIC_DATA1_1V8 — MAKE_BASE=TRUE — PDM_DMIC_DATA1_1V8

Audio Jack Flex Connector



PART_NUMBER=516S1181

JR900
AA25D-S016VA1
F-ST-SM

APN: 516S1181 ,MATINGM PLUG APN:516S1180
SAME AS J314

AUD_CONN_HP_LEFT
AUD_CONN_HP_RIGHT
AUD_CONN_RING2
AUD_CONN_SLEEVE

BOM_COST_GROUP=AUDIO

LAST CHANGE: Wed Feb 18 17:12:24 2015

PAGE TITLE
AUDIO FLEX CONNECTORS

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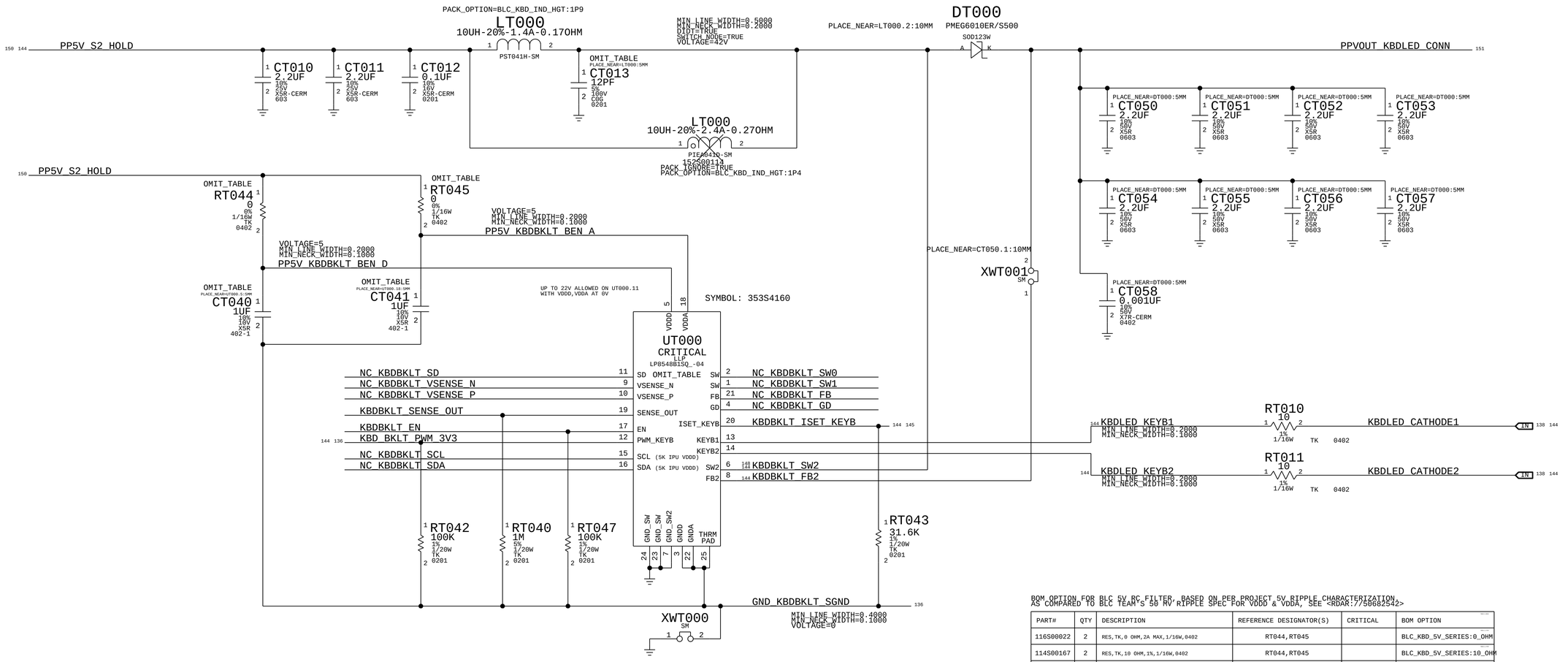
*** OK2INTEGRATE ***

BEN IC: KEYBOARD LED DRIVER

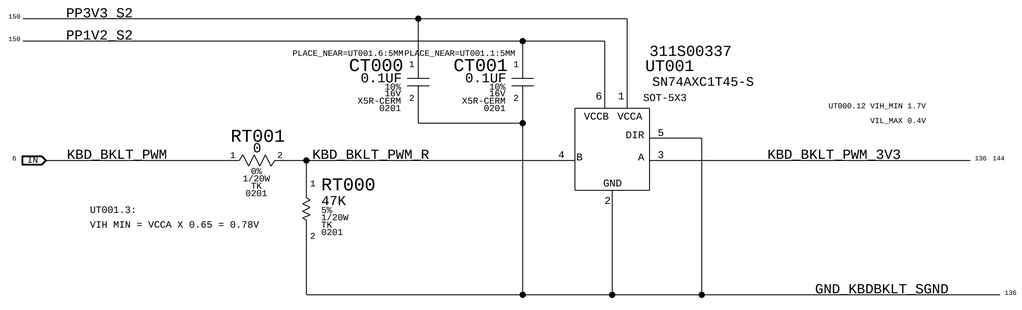


BOM OPTION FOR BLC 5V RC FILTER, BASED ON PER PROJECT 5V RIPPLE CHARACTERIZATION, AS COMPARED TO BLC TEAM'S 50 MV RIPPLE SPEC FOR VDDD & VDDA, SEE <RDAR:?50682542>

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S00022	2	RES,TK,0 OHM,2A MAX,1/16W,0402	RT044,RT045		BLC_KBD_5V_SERIES:0_OHM
114S00167	2	RES,TK,10 OHM,1%,1/16W,0402	RT044,RT045		BLC_KBD_5V_SERIES:10_OHM
138S0614	2	CAP,CER,X5R,1UF,10%,10V,0402	CT040,CT041		BLC_KBD_5V_CAP:1_UF
138S00070	2	CAP,CER,X5R,4.7UF,20%,25V,0402	CT040,CT041		BLC_KBD_5V_CAP:4P7_UF

KEYBOARD BKLT PWM LEVEL-SHIFTER

UT001.4: VOH_MIN = 2.3V
VOL_MAX = 0.1V @ PWM_KEYB I_MAX OF 1UA



BEN IC VERSION 4 VS 6 DEPENDS ON WHICH VERSION OF JERRY IC IS ON THE PANEL

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S01615	1	IC,LP8548B1-04,DC/DC CVTR,BST,AIZU,QFN-24	UT000		BLC_KBD_BEN_IC:V4
353S01685	1	IC,LP8548B1-06,DC/DC CVTR,BST,QFN24	UT000		BLC_KBD_BEN_IC:V6

ALTERNATE PART FOR BEN IC VERSION 4

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S4160	353S01615	BLC_KBD_BEN_IC:V4	ALL	RECOMMENDED BY LOUISA

KEYBOARD SWITCH NODE DESENSE OPTION

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
131S00141	1	CAP,C0G,12PF,5%,100V,0201	CT013		BLC_KBD_SW_NODE_DESENSE

BOM_COST_GROUP=DISPLAY

PAGE TITLE: BEN: KEYBD BKLT

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DRAWING NUMBER 051-08286 SIZE D
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*** OK2PLACE ***

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
311S0665	311S00405		ALL	RDAR://91779789

TO/FROM TRACKPAD

KEYBAORD IOX1

TIE TO SAME VOLTAGE AS TPAD CONTROLLER, EITHER 1V8 OR 3V3

PP3V3_S2_HOLD_IPD — CT110 1.0UF 20% 6.3V X5R 0201-1 138S0692 — CT112 0.1UF 10% 6.3V CERM-X5R 0201 132S0444

ALL PLATFORMS CONNECT TO 1V8

PP1V85_S2_HOLD_KBD — CT113 0.1UF 10% 6.3V CERM-X5R 0201 132S0444 — CT114 10UF 20% 10V X5R-CERM 0402-7

IOX1 DOESN'T SEND THE INTERRUPT INSTEAD, IOX2 SENDS INT WHEN A KEY IS PRESSED

IOXP1_INT_L → INT*

ADDR, SCL, SDA

IOXP1_RESET_L → RESET* — CT111 0.1UF 10% 6.3V CERM-X5R 0201 132S0444

UT101 TCAL6416 WQFN-COMBO (VCCI, VCCP, GND, EPAD)

311S0665
ALT:311S00405
WRITE: 0X40
READ: 0X41

P00	1	KBD_DRIVE_Y0
P01	2	KBD_DRIVE_Y1
P02	3	KBD_DRIVE_Y2
P03	4	KBD_DRIVE_Y3
P04	5	KBD_DRIVE_Y4
P05	6	KBD_DRIVE_Y5
P06	7	KBD_DRIVE_Y6
P07	8	KBD_DRIVE_Y7
P10	10	KBD_DRIVE_Y8
P11	11	KBD_DRIVE_Y9
P12	12	KBD_DRIVE_Y10
P13	13	KBD_DRIVE_Y11
P14	14	NC
P15	15	KBD_ID_DETECT2
P16	16	KBD_LAYOUT_DETECT
P17	17	CAPSLOCK_LED_EN

ADD 4X NEW IO,Y8,Y9,Y10,Y11 FOR ALL 34-PIN KBD
CONNECT THE NEW IO FROM KBD ZIF CONN TO NEARBY ESD DIODES

I2C_KBD_SCL — RT110 33 1% 1/20W TK 0201 — CKPLUS_WAIVE=I2C_PULLUP — IOXP_I2C_SCL
PLACE_NEAR=JT400.8:10MM — DZT110 5.5V-0.28PF 0201-THICKSTNCL

I2C_KBD_SDA — RT111 33 1% 1/20W TK 0201 — CKPLUS_WAIVE=I2C_PULLUP — IOXP_I2C_SDA
PLACE_NEAR=JT400.9:10MM — DZT111 5.5V-0.28PF 0201-THICKSTNCL

KBD_INT_L — RT112 33 1% 1/20W TK 0201 — IOXP2_INT_L
PLACE_NEAR=JT400.9:10MM — DZT112 5.5V-0.28PF 0201-THICKSTNCL

KEYBAORD IOX2

TIE TO SAME VOLTAGE AS TPAD CONTROLLER, EITHER 1V8 OR 3V3

PP3V3_S2_HOLD_IPD — RT121 100K 5% 1/20W TK 0201 — CT120 1.0UF 20% 6.3V X5R 0201-1 138S0692 — CT121 0.1UF 10% 6.3V CERM-X5R 0201 132S0444

ALL PLATFORMS CONNECT TO 1V8

PP1V85_S2_HOLD_KBD — CT122 0.1UF 10% 10V X5R-CERM 0201

IOXP2_ADDR → ADDR

IOXP2_RESET_L → RESET* — CT123 0.1UF 10% 6.3V CERM-X5R 0201 132S0444

UT102 TCAL6416 WQFN-COMBO (VCCI, VCCP, GND, EPAD)

WRITE: 0X42
READ: 0X43

P00	1	KBD_SENSE_X0
P01	2	KBD_SENSE_X1
P02	3	KBD_SENSE_X2
P03	4	KBD_SENSE_X3
P04	5	KBD_SENSE_X4
P05	6	KBD_SENSE_X5
P06	7	KBD_SENSE_X6
P07	8	KBD_SENSE_X7
P10	10	KBD_SENSE_X8
P11	11	KBD_SENSE_X9
P12	12	KBD_SENSE_X10
P13	13	KBD_SENSE_X11
P14	14	KBD_SENSE_X12
P15	15	KBD_CONTROL_L
P16	16	KBD_LEFT_OPTION_L
P17	17	KBD_RIGHT_SHIFT_L

PP1V85_S2_HOLD_KBD

RT130	10K	5% 1/20W TK 0201	KBD_SENSE_X0
RT131	10K	5% 1/20W TK 0201	KBD_SENSE_X1
RT132	10K	5% 1/20W TK 0201	KBD_SENSE_X2
RT133	10K	5% 1/20W TK 0201	KBD_SENSE_X3
RT134	10K	5% 1/20W TK 0201	KBD_SENSE_X4
RT135	10K	5% 1/20W TK 0201	KBD_SENSE_X5
RT136	10K	5% 1/20W TK 0201	KBD_SENSE_X6
RT137	10K	5% 1/20W TK 0201	KBD_SENSE_X7
RT138	10K	5% 1/20W TK 0201	KBD_SENSE_X8
RT139	10K	5% 1/20W TK 0201	KBD_SENSE_X9
RT140	10K	5% 1/20W TK 0201	KBD_SENSE_X10
RT141	10K	5% 1/20W TK 0201	KBD_SENSE_X11
RT142	10K	5% 1/20W TK 0201	KBD_SENSE_X12
RT143	1K	1% 1/20W TK 0201	IOXP2_ADDR

PP3V3_S2_HOLD_IPD

RT120	10K	5% 1/20W TK 0201	IOXP2_RESET_L
RT122	10K	5% 1/20W TK 0201	IOXP1_RESET_L
RT123	1.3K	1% 1/20W TK 0201	I2C_KBD_SCL
RT124	1.3K	1% 1/20W TK 0201	I2C_KBD_SDA
RT125	100K	1% 1/20W TK 0201	IOXP1_INT_L

3V3 KBD CONN SERIES R

KBD DRI REQUEST, TO MEASURE CAPSLOCK LED CURRENT

PP3V3_AON — RT103 0 5% 1/20W TK 0201 — PP3V3_AON_KBD_CONN
TO KBD CONN AND ESD
MIN_NECK_WIDTH=0.1200
MIN_LINE_WIDTH=0.2000
VOLTAGE=3.3V

ID_DETECT SERIES R

KBD_LAYOUT_DETECT — RT117 1K 5% 1/20W TK 0201-1 — KBD_ID1
KBD_ID 1 PIN ON KBD CONNECTOR
ANSI: NO CONNECT
ISO: TIED HIGH TO PP1V8
JIS: TIED LOW TO GND

KBD_ID_DETECT2 — RT119 1K 5% 1/20W TK 0201-1 — KBD_ID2
KBD_ID 2 PIN ON KBD CONNECTOR
TIED LOW TO GND FOR 34-PIN KBD

3.3V RSLOC ISOLATION KEYS/ASIC RESET

PP3V3_AON — CT150 1.0UF 20% 6.3V X5R 0201-1 138S0692 (PLACE_NEAR=UT103.10:5MM) — CT151 0.1UF 10% 6.3V CERM-X5R 0201 132S0444 (PLACE_NEAR=UT103.10:2MM)

PP1V85_S2_HOLD_KBD — 117S00073 RT190 0 5% 1/20W TK 0201 — OUT123_EN

UT103 SLG4AP45306 QFN-THICKSTNCL 343S00532 (2.97 < VDD < 3.63)
IN_X: VIH_MIN 2.0V, VIL_MAX 0.8V, 100K IPD
OUT_X: VOH_MIN 2.4V, VOL_MAX 0.4V, 12.5K IPU OE

KBD_RIGHT_SHIFT_KEY	1	IN_1	OUT_1 → KBD_RIGHT_SHIFT_L
KBD_LEFT_OPTION_KEY	2	IN_2	OUT_2 → KBD_LEFT_OPTION_L
KBD_CONTROL_KEY	3	IN_3	OUT_3 → KBD_CONTROL_L
			OUT_ALL* → RSLOC_RST_L

RSLOC_RST_L — RT152 33 1% 1/20W TK 0201 — PMU_RSLOC_RST_L

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S00879	353S00754		UT108	RDAR://32477358

USE SAME POWER RAIL AS TPAD 3V3 LDO INPUT

PP3V8_IPDLDO_VIN — CT180 1.0UF 20% 6.3V X5R 0201-1 138S0692

LP5907SNX-1.825 X2SON-COMBO-THICKSTNCL UT108 (VIN, EN, VOUT, GND EPAD)

IPD_PWR_EN

VOUT → PP1V85_S2_HOLD_KBD — CT181 1.0UF 20% 6.3V X5R 0201-1 138S0692

THE LDO OUTPUT SUPPLY POWER OF KBD IO EXPANDER IO PIN.
EVENTUALLY SHOUULD BE CONNECTED TO PP1V8_S2_KBD

CAPSLOCK LED DRIVER

CONSTANT CURRENT LED DRIVER

NOTE: THIS CAN BE THE SAME RAIL AS THE CAPSLOCK LED (3V3_AON), OR A RAIL THAT COMES UP AFTER (3V3_S2)

PP3V3_S2_HOLD_IPD — CT105 1.0UF 20% 6.3V X5R 0201-1 138S0692

CAPSLOCK_LED_EN — RT161 1K 5% 1/20W TK 0201-1 — LED_CTRL

LED_ISET — RT162 200K 5% 1/20W TK 0201 — RT160 19.1K 1% 1/20W TK 0201 <R_SET>

UT105 FAN5622 SSOT23 (VIN, CTRL, ISET, LED1, LED2, GND)
VIH_MIN 1.2V, VIL_MAX 0.4V

R_SET 19.1K = 15 MA SINK

LED1 → KBD_LED1 — RT118 1 1% 1/20W TK 0201 — KBD_CAP_CATHODE

BOM_COST_GROUP=KEYBOARD

PAGE TITLE	KEYBOARD IOX, SUPPORT
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REVISION	5.0.3
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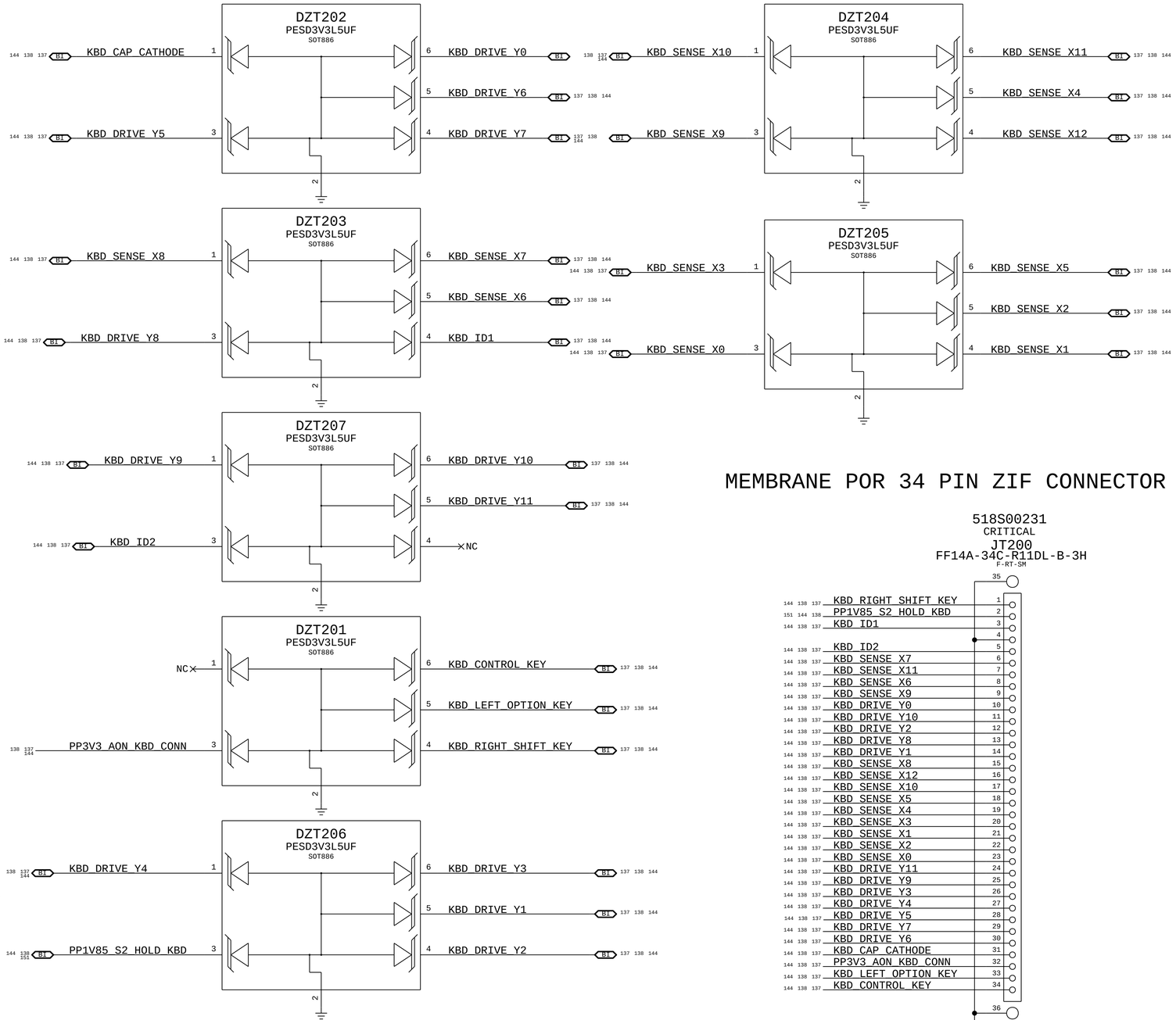
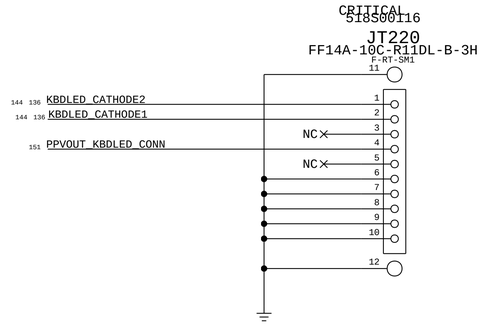
KEYBOARD ESD



MEMBRANE POR 34 PIN ZIF CONNECTOR

KBDLED Connector



BOM_COST_GROUP=KEYBOARD

PAGE TITLE: KEYBOARD SIGNAL CONNECTOR, ESD

Apple Inc.

DRAWING NUMBER: 051-08286
SIZE: D
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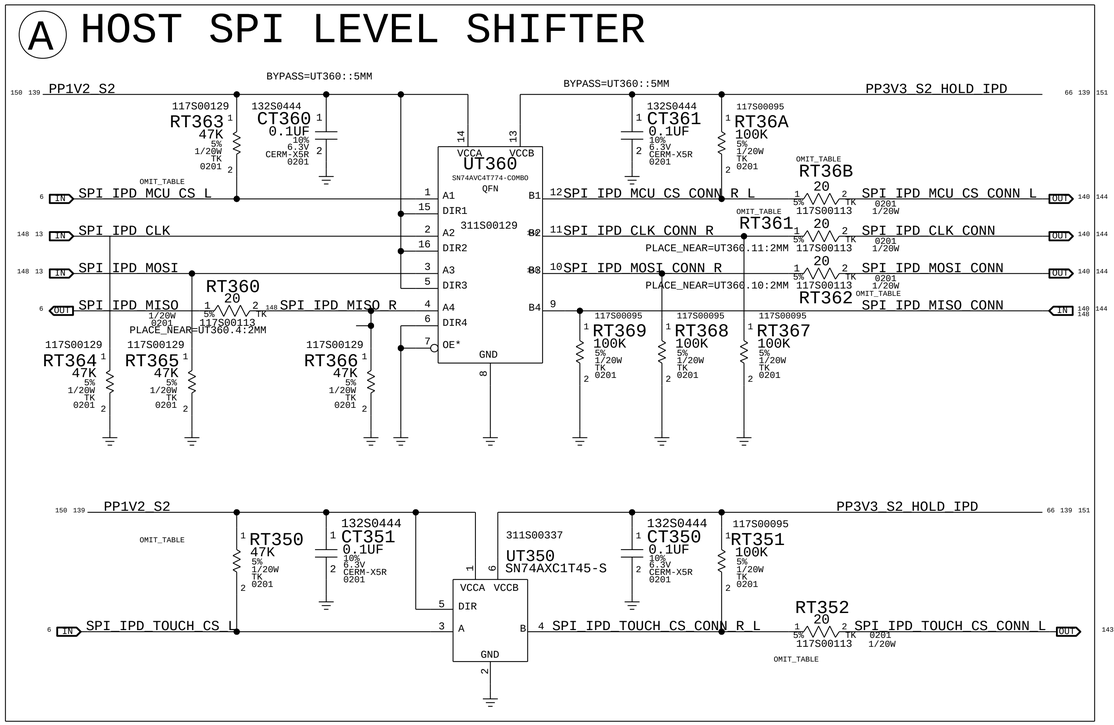

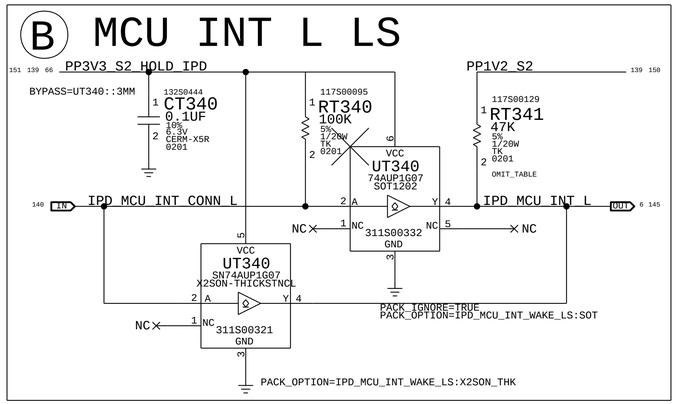

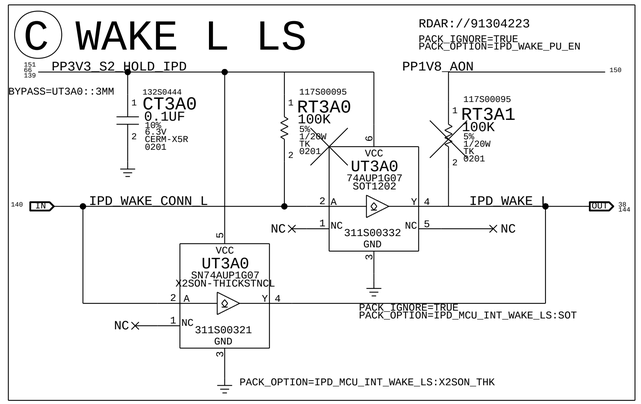

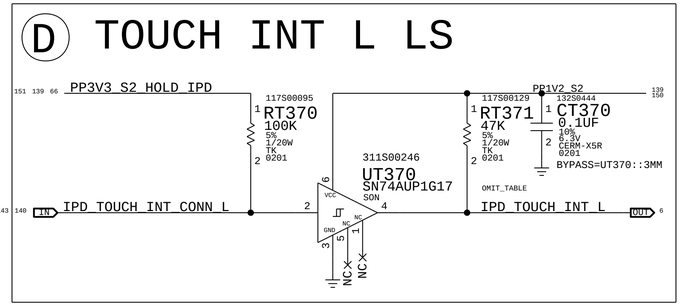

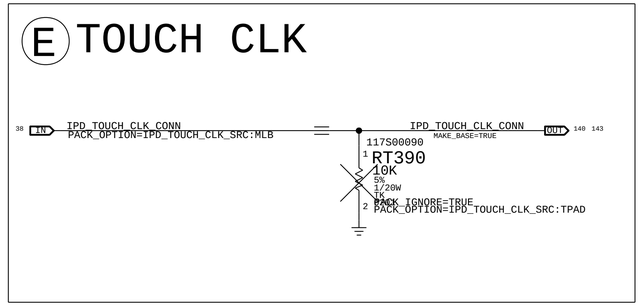

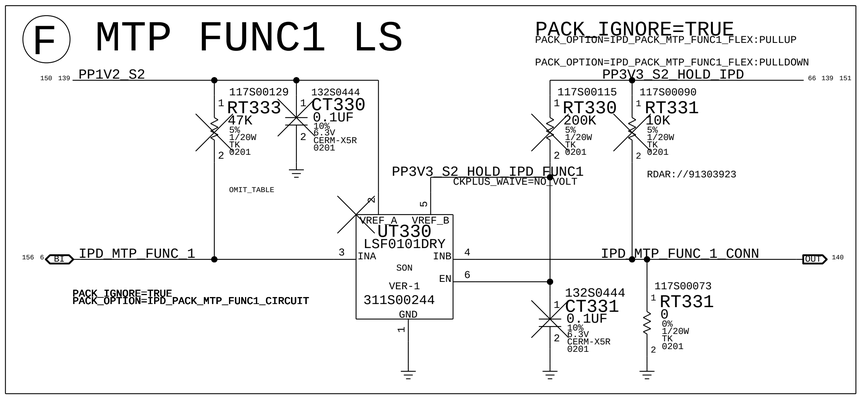

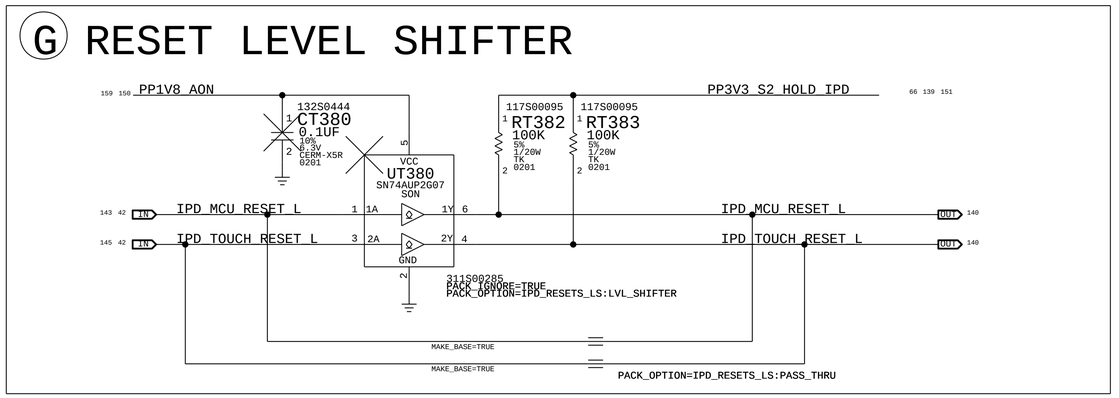

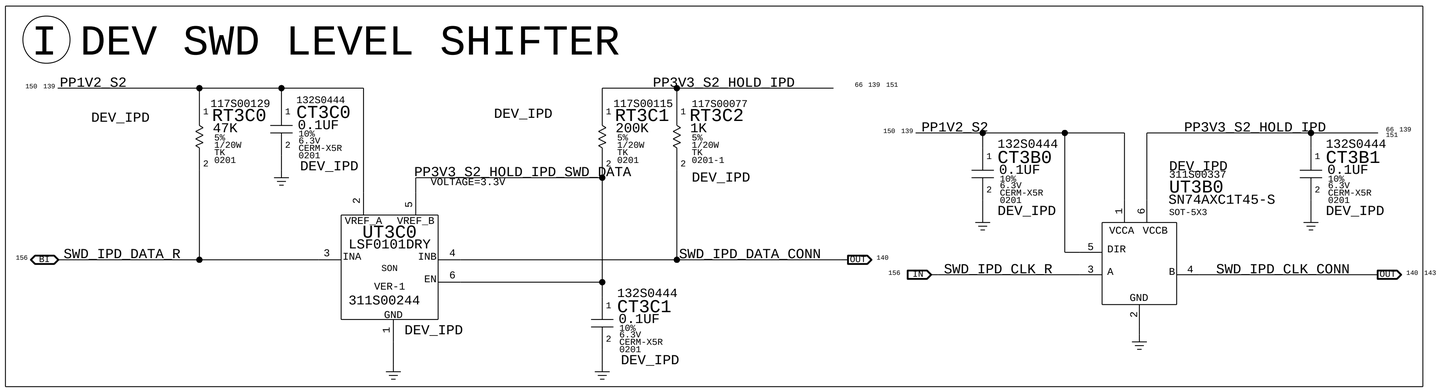

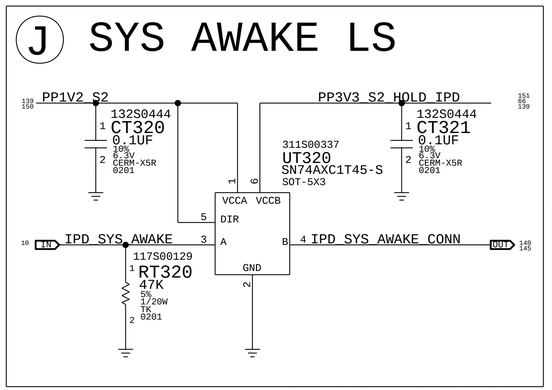

BOM_COST_GROUP=TRACKPAD

PAGE TITLE: TRACKPAD SUPPORT

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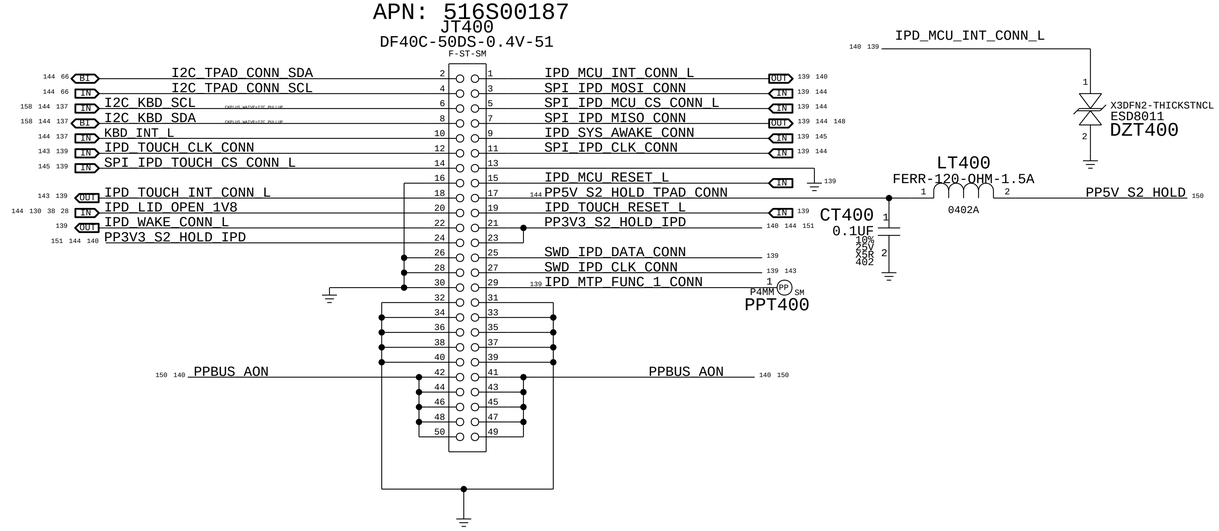
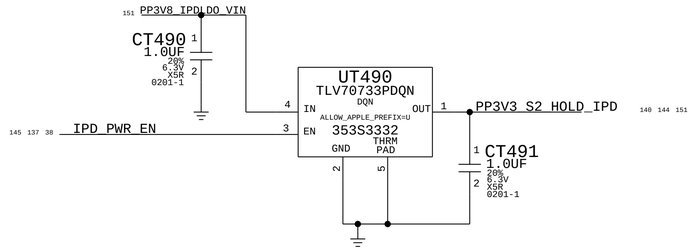
MATES WITH 518S00080
APN: 516S00187



3.3V LDO (LOCAL TO IPD)

Current Limit = 200mA



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PAGE TITLE: TRACKPAD SUPPORT 2

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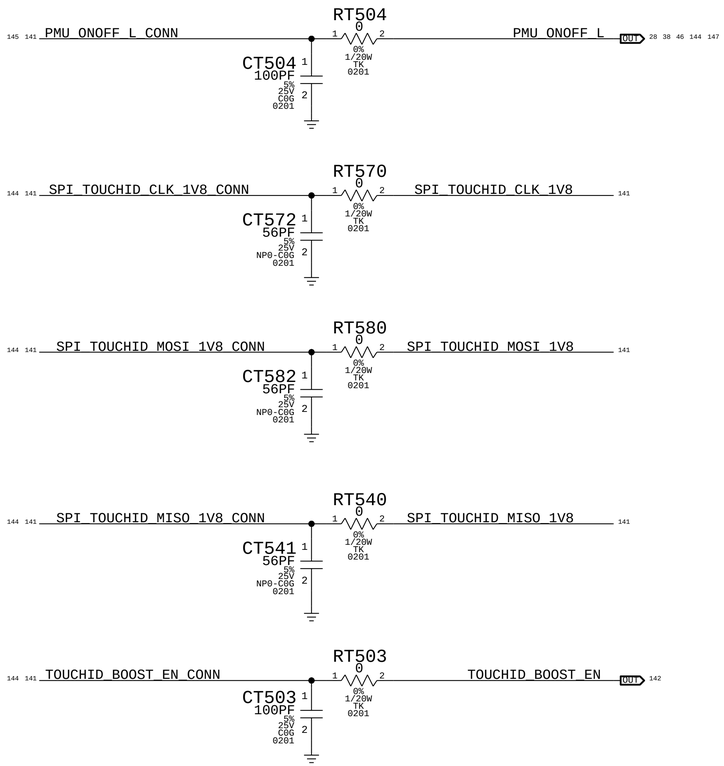

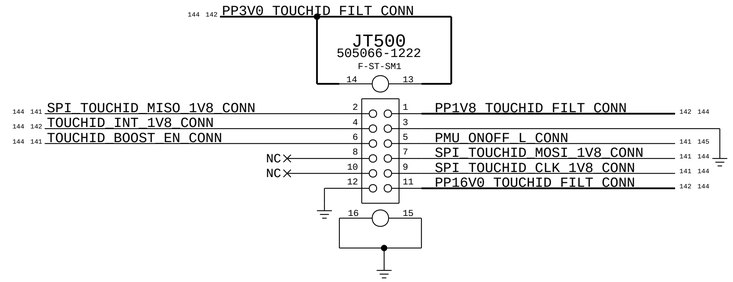

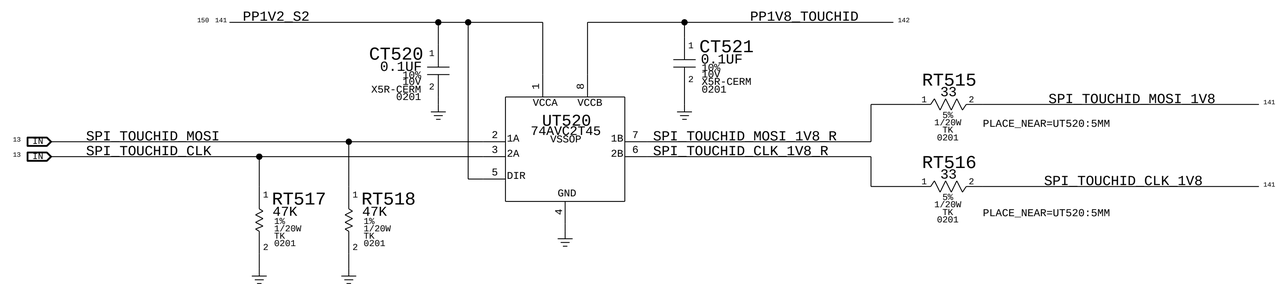

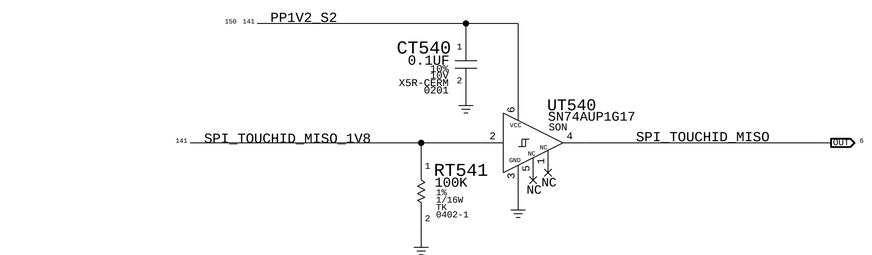

BOM_COST_GROUP=TOUCHID

PAGE TITLE: TOUCHID CONN

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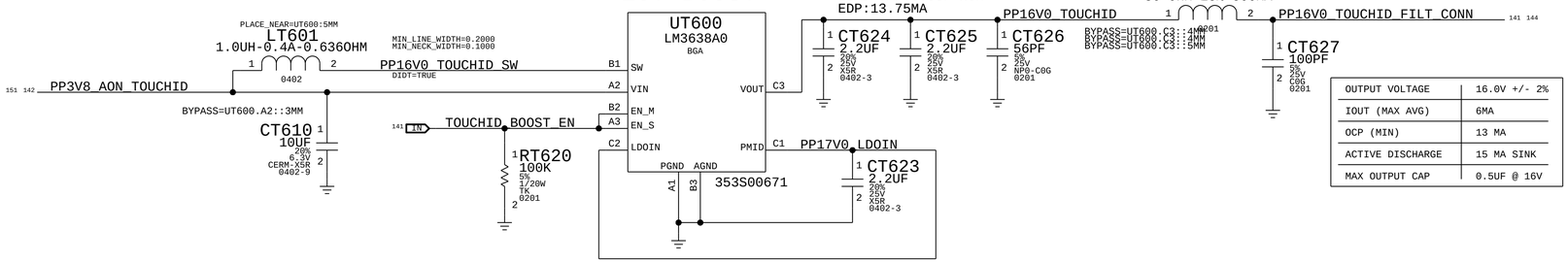
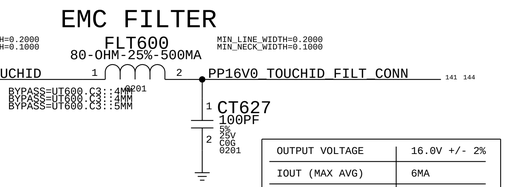
TOUCHID POWER SEQUENCING REQUIREMENTS

POWER ON: 1V8 -> 3V3 -> 16V0

16V BOOST

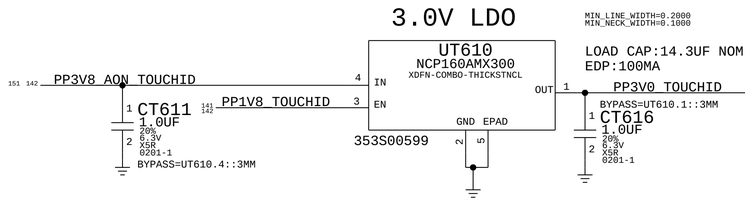


EMC FILTER

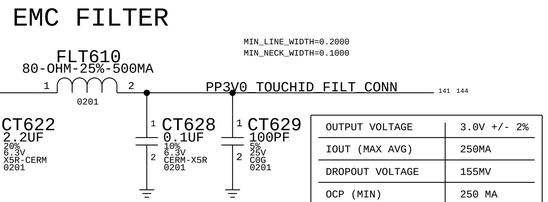


OUTPUT VOLTAGE	16.0V +/- 2%
IOUT (MAX AVG)	6MA
OCP (MIN)	13 MA
ACTIVE DISCHARGE	15 MA SINK
MAX OUTPUT CAP	0.5UF @ 16V

3.0V LDO

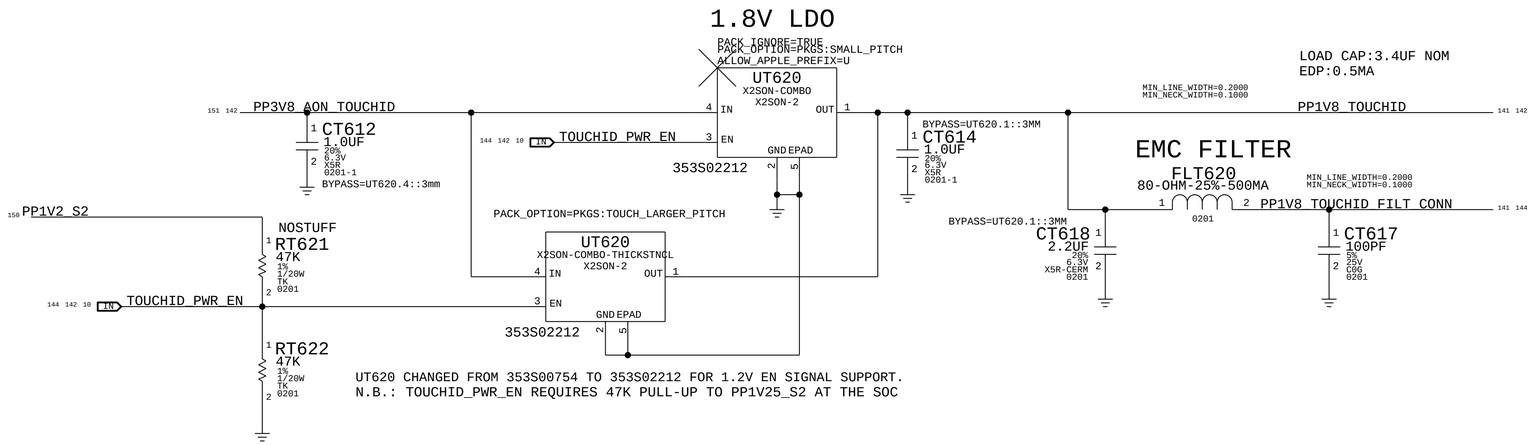


EMC FILTER



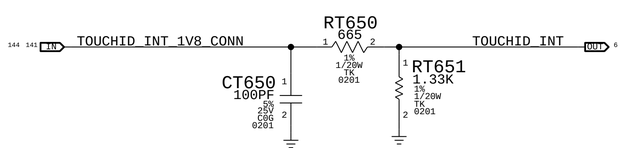
OUTPUT VOLTAGE	3.0V +/- 2%
IOUT (MAX AVG)	250MA
DROPOUT VOLTAGE	155MV
OCP (MIN)	250 MA
ACTIVE DISCHARGE	280 OHM TYP

1.8V LDO



OUTPUT VOLTAGE	1.825 V +/- 2%
IOUT (MAX AVG)	250 MA
DROPOUT VOLTAGE	75MV TYP @ 100MA
OCP (MIN)	250 MA
ACTIVE DISCHARGE	280 OHM TYP
MIN OUTPUT CAP	1.0 UF

UT620 CHANGED FROM 353S00754 TO 353S02212 FOR 1.2V EN SIGNAL SUPPORT.
N.B.: TOUCHID_PWR_EN REQUIRES 47K PULL-UP TO PP1V25_S2 AT THE SOC



BOM_COST_GROUP=TOUCHID

PAGE TITLE: TOUCHID SUPPORT

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Test Point Types Guide

PP are for EE debug (0.3mm)
TPs for general fixtures (0.4mm)
FCT test points use FUNC_TEST=TRUE, all go on TOP (0.4mm)
ICT test points placed by PCB designer not published in netlist, or use FCT (0.4mm)

NAND0 TPs

116 115 114 113 112	IN	NAND0_LPB_L	TOP	TPU603 TP-P4
116 115 114 113 112 8	IN	NAND_BFH	TOP	TPU604 TP-P4
116 115 114 113 112	IN	NAND0_BOOT2	TOP	TPU605 TP-P4
112	IN	NAND0_S5E0_SWD_UID0	TOP	TPU606 TP-P4
113	IN	NAND0_S5E1_SWD_UID0	TOP	TPU607 TP-P4
114	IN	NAND0_S5E2_SWD_UID0	TOP	TPU608 TP-P4
115	IN	NAND0_S5E3_SWD_UID0	TOP	TPU609 TP-P4
112	IN	NAND0_S5E0_SWD_UID1	TOP	TPU610 TP-P4
113	IN	NAND0_S5E1_SWD_UID1	TOP	TPU611 TP-P4
114	IN	NAND0_S5E2_SWD_UID1	TOP	TPU612 TP-P4
115	IN	NAND0_S5E3_SWD_UID1	TOP	TPU613 TP-P4
116 115 114 113 112	IN	NAND0_PFN_L	TOP	TPU614 TP-P4
115 114 113 112 8	IN	NAND0_PCIE_RESET_L	TOP	TPU615 TP-P4
12	IN	SWD_NAND0_SWDIO	TOP	TPU616 TP-P4
12	IN	SWD_NAND0_SWCLK	TOP	TPU617 TP-P4
115 114 113 112	IN	NAND0_WP_L	TOP	TPU618 TP-P4
13 8	IN	NAND0_CLKREQ0_L	TOP	TPU619 TP-P4
13 8	IN	NAND0_CLKREQ1_L	TOP	TPU620 TP-P4
13 8	IN	NAND0_CLKREQ2_L	TOP	TPU621 TP-P4
13 8	IN	NAND0_CLKREQ3_L	TOP	TPU622 TP-P4
112	IN	NAND0_S5E0_PCIE_RESREF	TOP	TPU623 TP-P4
113	IN	NAND0_S5E1_PCIE_RESREF	TOP	TPU624 TP-P4
114	IN	NAND0_S5E2_PCIE_RESREF	TOP	TPU625 TP-P4
115	IN	NAND0_S5E3_PCIE_RESREF	TOP	TPU626 TP-P4
156 116	IN	NAND0_RESET_L	TOP	TPU627 TP-P4
112	IN	NAND0_S5E0_ZQ_0	TOP	TPU628 TP-P4
112	IN	NAND0_S5E0_ZQ_1	TOP	TPU629 TP-P4
113	IN	NAND0_S5E1_ZQ_1	TOP	TPU630 TP-P4
113	IN	NAND0_S5E1_ZQ_0	TOP	TPU631 TP-P4
114	IN	NAND0_S5E2_ZQ_0	TOP	TPU632 TP-P4
114	IN	NAND0_S5E2_ZQ_1	TOP	TPU633 TP-P4
115	IN	NAND0_S5E3_ZQ_1	TOP	TPU634 TP-P4
115	IN	NAND0_S5E3_ZQ_0	TOP	TPU635 TP-P4
112	IN	TP_NAND0_S5E0_JTAG_TDI	TOP	TPU668 TP-P4
115	IN	TP_NAND0_S5E3_JTAG_TDO	TOP	TPU669 TP-P4
115 114 113 112	IN	NAND0_JTAG_SEL	TOP	TPU670 TP-P4
115 114 113 112	IN	NAND0_JTAG_TRST_L	TOP	TPU671 TP-P4
145 112	IN	TP_NAND0_S5E0_ANI1_VREF	TOP	TPU672 TP-P4
145 112	IN	TP_NAND0_S5E0_ANI0_VREF	TOP	TPU673 TP-P4
145 113	IN	TP_NAND0_S5E1_ANI1_VREF	TOP	TPU674 TP-P4
145 113	IN	TP_NAND0_S5E1_ANI0_VREF	TOP	TPU675 TP-P4
145 114	IN	TP_NAND0_S5E2_ANI1_VREF	TOP	TPU676 TP-P4
145 114	IN	TP_NAND0_S5E2_ANI0_VREF	TOP	TPU677 TP-P4
145 115	IN	TP_NAND0_S5E3_ANI1_VREF	TOP	TPU678 TP-P4
145 115	IN	TP_NAND0_S5E3_ANI0_VREF	TOP	TPU679 TP-P4
116	IN	TP_NAND0_OCARINA_VEN2	TOP	TPU600 TP-P4

NAND1 TPs

121 120 119 118 117	IN	NAND1_LPB_L	TOP	TPU636 TP-P4
120 119 118 117	IN	NAND1_BOOT2	TOP	TPU637 TP-P4
117	IN	NAND1_S5E0_SWD_UID0	TOP	TPU638 TP-P4
118	IN	NAND1_S5E1_SWD_UID0	TOP	TPU639 TP-P4
119	IN	NAND1_S5E2_SWD_UID0	TOP	TPU640 TP-P4
120	IN	NAND1_S5E3_SWD_UID0	TOP	TPU641 TP-P4
117	IN	NAND1_S5E0_SWD_UID1	TOP	TPU642 TP-P4
118	IN	NAND1_S5E1_SWD_UID1	TOP	TPU643 TP-P4
119	IN	NAND1_S5E2_SWD_UID1	TOP	TPU644 TP-P4
120	IN	NAND1_S5E3_SWD_UID1	TOP	TPU645 TP-P4
121 120 119 118 117	IN	NAND1_PFN_L	TOP	TPU646 TP-P4
120 119 118 117 8	IN	NAND1_PCIE_RESET_L	TOP	TPU647 TP-P4
120 119 118 117	IN	NAND1_WP_L	TOP	TPU650 TP-P4
13 8	IN	NAND1_CLKREQ0_L	TOP	TPU651 TP-P4
13 8	IN	NAND1_CLKREQ1_L	TOP	TPU652 TP-P4
13 8	IN	NAND1_CLKREQ2_L	TOP	TPU653 TP-P4
13 8	IN	NAND1_CLKREQ3_L	TOP	TPU654 TP-P4
117	IN	NAND1_S5E0_PCIE_RESREF	TOP	TPU655 TP-P4
118	IN	NAND1_S5E1_PCIE_RESREF	TOP	TPU656 TP-P4
119	IN	NAND1_S5E2_PCIE_RESREF	TOP	TPU657 TP-P4
120	IN	NAND1_S5E3_PCIE_RESREF	TOP	TPU658 TP-P4
156 121	IN	NAND1_RESET_L	TOP	TPU659 TP-P4
117	IN	NAND1_S5E0_ZQ_0	TOP	TPU660 TP-P4
117	IN	NAND1_S5E0_ZQ_1	TOP	TPU661 TP-P4
118	IN	NAND1_S5E1_ZQ_1	TOP	TPU662 TP-P4
118	IN	NAND1_S5E1_ZQ_0	TOP	TPU663 TP-P4
119	IN	NAND1_S5E2_ZQ_0	TOP	TPU664 TP-P4
119	IN	NAND1_S5E2_ZQ_1	TOP	TPU665 TP-P4
120	IN	NAND1_S5E3_ZQ_1	TOP	TPU666 TP-P4
120	IN	NAND1_S5E3_ZQ_0	TOP	TPU667 TP-P4
119 118	IN	NAND1_S5E1_JTAG_TDO	TOP	TPU680 TP-P4
120 119	IN	NAND1_S5E2_JTAG_TDO	TOP	TPU681 TP-P4
117	IN	TP_NAND1_S5E0_JTAG_TDI	TOP	TPU682 TP-P4
120	IN	TP_NAND1_S5E3_JTAG_TDO	TOP	TPU683 TP-P4
120 119 118 117	IN	NAND1_JTAG_SEL	TOP	TPU684 TP-P4
120 119 118 117	IN	NAND1_JTAG_TRST_L	TOP	TPU685 TP-P4
145 117	IN	TP_NAND1_S5E0_ANI1_VREF	TOP	TPU686 TP-P4
145 117	IN	TP_NAND1_S5E0_ANI0_VREF	TOP	TPU687 TP-P4
145 118	IN	TP_NAND1_S5E1_ANI1_VREF	TOP	TPU688 TP-P4
145 118	IN	TP_NAND1_S5E1_ANI0_VREF	TOP	TPU689 TP-P4
145 119	IN	TP_NAND1_S5E2_ANI1_VREF	TOP	TPU690 TP-P4
145 119	IN	TP_NAND1_S5E2_ANI0_VREF	TOP	TPU691 TP-P4
145 120	IN	TP_NAND1_S5E3_ANI1_VREF	TOP	TPU692 TP-P4
145 120	IN	TP_NAND1_S5E3_ANI0_VREF	TOP	TPU693 TP-P4
121	IN	TP_NAND1_OCARINA_VEN2	TOP	TPU601 TP-P4

SoC Misc Debug TPs

5	IN	TP_ANALOGMUX_OUT0	TOP	TPU6612 TP-P4
5	IN	TP_ANALOGMUX_OUT1	TOP	TPU6613 TP-P4
144 143 83 6	IN	UART_DEBUGPRT_D2R	BOTTOM	TPU6614 TP-P4
144 83 6	IN	UART_DEBUGPRT_R2D	BOTTOM	TPU6615 TP-P4
144 46 10	IN	PMU_RESET_L	BOTTOM	TPU6616 TP-P4
155 5	IN	SOC_FORCE_DFU	BOTTOM	TPU6617 TP-P4

FUNC_TEST=TRUE

155 146 144 46 10 5	IN	PMU_ACTIVE_READY	BOTTOM	TPU6621 TP-P4
144 5	IN	SOC_HOLD_RESET	BOTTOM	TPU6622 TP-P4
5	IN	SOC_KIS_DFU_SELECT	TOP	TPU6623 TP-P4
5	IN	SOC_DBG_PROBE_VALID	BOTTOM	TPU6624 TP-P4
38 10	IN	PMU_CLK32K_SOC	TOP	TPU6600 TP-P4
144 10	IN	SMC_FIXTURE_MODE_L	TOP	TPU6603 TP-P4
TPT_SOC_DOCK_ATTENTION (MAKE_BASE=TRUE)		TPT_SOC_DOCK_ATTENTION	TOP	TPU6601 TP-P4
TPT_TST_CLKOUT (MAKE_BASE=TRUE)		TPT_TST_CLKOUT	TRUE 5 BOTTOM	PPU1 P3MM SM

SoC JTAG TPs

10	IN	SOC_JTAG_SEL		TPU6604 TP-P4
144 83 12	IN	SWD_SOC_SWCLK (PLACE_NEAR=UF400:20mm)		TPU6605 TP-P4
144 83 12	IN	SWD_SOC_SWDIO (PLACE_NEAR=UF400:20mm)		TPU6608 TP-P4
158 10	IN	SOC_JTAG_TDI		TPU6606 TP-P4
158 10	IN	SOC_JTAG_TDO		TPU6607 TP-P4
TPT_JTAG_SOC_TRST_L (MAKE_BASE=TRUE)	10	TPT_JTAG_SOC_TRST_L		TPU6609 TP-P4

100 99	IN	HDMI_PIND_VBIAS		TPU66D0 TP-P4
101 99	IN	DP2HDMI_1_5G_FILT_EN		TPU66D1 TP-P4

MISC (cont.) — FUNC_TEST

U430	KISMUX_SEL	TRUE 149
U430	SOC_DOCK_CONNECT_DUAL_KIS_3V3	TRUE 82 83 86 87
153 145	PPVDD_ECPU_SRAM_AWAKESW (MAKE_BASE=TRUE)	PPVDD_ECPU_SRAM_AWAKESW TRUE
106	PP1V2_GL_LOOP (MAKE_BASE=TRUE)	PP1V2_GL_LOOP TRUE
U430	UART_DEBUGPRT_D2R	TRUE 6 83 143 144
U430	SPI_TCON_CLK_CONN	TRUE 125
U440	IPD_TOUCH_CLK_CONN	TRUE 139 140
U440	IPD_TOUCH_INT_CONN_L	TRUE 139 140
U440	IPD_MCU_RESET_L	TRUE 42 139
U440	SWD_IPD_CLK_CONN	TRUE 139 140

Board ID — FUNC_TEST

U440	BOARD_ID0	TRUE 4 6
U440	BOARD_ID1	TRUE 4 6
U440	BOARD_ID2	TRUE 4 6
U440	BOARD_ID3	TRUE 4 6
U440	BOARD_ID4	TRUE 4 6

Board REV — FUNC_TEST

U441	BOARD_REV0	TRUE 4 6
U441	BOARD_REV1	TRUE 4 6
U441	BOARD_REV2	TRUE 4 6
U441	BOARD_REV3	TRUE 4 6

Fan TPs

76	IN	TP_I2C_FAN0_SCL	BOTTOM	TPU6200 TP-P4
76	IN	TP_I2C_FAN0_SDA	BOTTOM	TPU6201 TP-P4
76	IN	TP_I2C_FAN1_SCL	BOTTOM	TPU6202 TP-P4
76	IN	TP_I2C_FAN1_SDA	BOTTOM	TPU203 TP-P4

FUNC_TEST

12	IN	SWD_NAND1_SWCLK	TRUE
12	IN	SWD_NAND1_SWDIO	TRUE

BATTERY (cont.) — FUNC_TEST

U430	DBS_BYPASS_L	TRUE 28 143
U430	DBS_BYPASS_L	TRUE 28 143
U437	LEDCTRL_VBAT	TRUE 28
U437	DISP_VBAT_L	TRUE 28
U437	INPUT_PWR_2LOW_L_R	TRUE 28
U437	CHGR_AUTO_CHARGE	TRUE 28 30
U437	CHGR_AUTO_CHARGE_R	TRUE 28 29 30
U145		

CHARGER (cont.) — FUNC_TEST

U437	CHGR_EN_MVR	TRUE 29 30 38
U437	P3V8AON_PWR_EN	TRUE 28 29 30 34 145

POWER (cont.) — FUNC_TEST

U437	VSNS_PVDDANE_SENSE	TRUE 11 19
U437	VSNS_PVDDPCPU0_SENSE_P	TRUE 11 15
U437	VSNS_PVDDPCPU0_SENSE_N	TRUE 11 26
U437	VSNS_PVDDPCPU0_SRAM_SENSE	TRUE 11 15
U438	TP_PPVDD_PCPU_SRAM1_AWAKESW	TRUE 11
U438	VSNS_PVDDGPU0_SENSE_P	TRUE 11 15
U438	VSNS_PVDDGPU0_SENSE_N	TRUE 11 26
U438	TP_PPVDD_GPU_SRAM0_AWAKESW	TRUE 11
U438	TP_PPVDD_GPU1_AWAKESW	TRUE 11
U438	TP_PPVDD_GPU_SRAM1_AWAKESW	TRUE 11
U438	TP_PPVDD_GPU2_AWAKESW	TRUE 11
U438	TP_PPVDD_GPU_SRAM2_AWAKESW	TRUE 11
U438	TP_PPVDD_GPU3_AWAKESW	TRUE 11
U438	TP_PPVDD_GPU_SRAM3_AWAKESW	TRUE 11
U439	VSNS_PVDDFABRIC_SENSE	TRUE 11 20
U439	VSNS_PVDDAFRCS_SENSE	TRUE 11 19
U140	TP_PPVDD_ANE_SRAM_AWAKESW	TRUE 11
U141	PP1V8_AWAKE_SEPROM_LDO	TRUE 153
U141	PP1V2_AON_LPMU	TRUE 38 44 46
U141	PMU_UPC_FORCE_DFU	TRUE 38 147 155

34	IN	I2C_P3V8AON_SCL		TPV001 TP-P4
34	IN	I2C_P3V8AON_SDA		TPV002 TP-P4
38 29 28	IN	CHGR_AUX_OK	TOP	TPU6664 TP-P4
137	IN	KBD_RIGHT_SHIFT_L (PLACE_NEAR=UT103.9:20MM)	TOP	TPU6666 TP-P4
137	IN	KBD_LEFT_OPTION_L (PLACE_NEAR=UT103.8:20MM)	TOP	TPU6667 TP-P4
137	IN	KBD_CONTROL_L (PLACE_NEAR=UT103.7:20MM)	TOP	TPU6668 TP-P4

DUMMY TEST POINTS TO MATCH C/S TPs

NC_DUMMY_TP_PCPU_ISENSE	TOP	TPU66B6 TP-P4	CKPLUS_WAIVE=NC_CHECKS
NC_DUMMY_TP_PCPU_VSENSE	TOP	TPU66B7 TP-P4	CKPLUS_WAIVE=NC_CHECKS
NC_DUMMY_TP_GPU_VSENSE	TOP	TPU66B8 TP-P4	CKPLUS_WAIVE=NC_CHECKS
NC_DUMMY_TP_PCPU_SRAM_VSENSE	TOP	TPU66B9 TP-P4	CKPLUS_WAIVE=NC_CHECKS
NC_DUMMY_TP_GPU_ISENSE	TOP	TPU66C0 TP-P4	CKPLUS_WAIVE=NC_CHECKS
NC_DUMMY_TP_PCPU_SRAM_ISENSE	TOP	TPU66C1 TP-P4	CKPLUS_WAIVE=NC_CHECKS
NC_DUMMY_TP_PMU_UPC_FORCE_DFU	TOP	TPU66C2 TP-P4	CKPLUS_WAIVE=NC_CHECKS
NC_DUMMY_TP_BOARD_REV2	TOP	TPU66C4 TP-P4	CKPLUS_WAIVE=NC_CHECKS
NC_DUMMY_TP_BOARD_REV3	TOP	TPU66D3 TP-P4	CKPLUS_WAIVE=NC_CHECKS
NC_DUMMY_TP_USBC2_LDCM_LB	TOP	TPU66D4 TP-P4	CKPLUS_WAIVE=NC_CHECKS
NC_DUMMY_TP_PP1V85_S2_KBD	TOP	TPU66D5 TP-P4	CKPLUS_WAIVE=NC_CHECKS
NC_DUMMY_TP_USBC1_LDCM_LB	TOP	TPU66D6 TP-P4	CKPLUS_WAIVE=NC_CHECKS
NC_TP_DUMMY_PP1V8_AWAKE_SEPROM	TOP	TPU66D7 TP-P4	CKPLUS_WAIVE=NC_CHECKS

Audio Team TPs

131	IN	PP3V8_CODEC_VP		TPU6626 TP-P4
131	IN	PP1V8_CODEC_VCP		TPU6627 TP-P4
131 10	IN	CODEC_RESET_L		TPU6628 TP-P4
131 6	IN	CODEC_INT_L		TPU6629 TP-P4
U120		CODEC_WAKE_L	TRUE 46 131	
131 13	IN	TDM_CODEC_FSYNC (PLACE_NEAR=UR500.B2:20MM)		TPU6630 TP-P4
131 13	IN	TDM_CODEC_R2D (PLACE_NEAR=UR500.B3:20MM)		TPU6631 TP-P4
131 6	IN	TDM_CODEC_D2R (PLACE_NEAR=U0600.BG75:20MM		TPU6632 TP-P4
131 13	IN	TDM_CODEC_BCLK (PLACE_NEAR=UR500.A3:20MM		TPU6633 TP-P4
131 64	IN	I2C_CODEC_SDA		TPU6634 TP-P4
131 64	IN	I2C_CODEC_SCL		TPU6635 TP-P4
133 132 6	IN	SPKRAMP_RESET_L		TPU6636 TP-P4
133 132 6	IN	SPKRAMP_INT_L		TPU6637 TP-P4
132 13	IN	TDM_SPKRAMP_L_BCLK (PLACE_NEAR=UR600.E1:20MM		TPU6638 TP-P4
132 13	IN	TDM_SPKRAMP_L_FSYNC (PLACE_NEAR=UR600.D2:20MM		TPU6639 TP-P4
132 13	IN	TDM_SPKRAMP_L_R2D (PLACE_NEAR=UR600.E2:20MM		TPU6640 TP-P4
132 13	IN	TDM_SPKRAMP_L_D2R (PLACE_NEAR=U0600.BP72:20MM		TPU6641 TP-P4
132	IN	SPKRAMP_ABC_ICC		TPU6642 TP-P4
133 132	IN	SPKRAMP_DEF_ICC		TPU6672 TP-P4
132 64	IN	I2C_SPKRAMP_L_SCL		TPU6643 TP-P4
132 64	IN	I2C_SPKRAMP_L_SDA		TPU6644 TP-P4
132	IN	TP_SPKRAMP_A_LV_EN		TPU6645 TP-P4
132	IN	TP_SPKRAMP_B_LV_EN		TPU6646 TP-P4
132	IN	TP_SPKRAMP_C_LV_EN		TPU6647 TP-P4
133 13	IN	TDM_SPKRAMP_R_BCLK (PLACE_NEAR=UR700.E1:20MM		TPU6648 TP-P4
133 13	IN	TDM_SPKRAMP_R_FSYNC (PLACE_NEAR=UR700.D2:20MM		TPU6649 TP-P4
133 13	IN	TDM_SPKRAMP_R_R2D (PLACE_NEAR=UR700.E2:20MM		TPU6650 TP-P4
133 13	IN	TDM_SPKRAMP_R_D2R (PLACE_NEAR=U0600.BC77:20MM		TPU6651 TP-P4
133 64	IN	I2C_SPKRAMP_R_SCL		TPU6652 TP-P4
133 64	IN	I2C_SPKRAMP_R_SDA		TPU6653 TP-P4
133	IN	TP_SPKRAMP_D_LV_EN		TPU6654 TP-P4
133	IN	TP_SPKRAMP_E_LV_EN		TPU6655 TP-P4
133	IN	TP_SPKRAMP_F_LV_EN		TPU6656 TP-P4
145 135 10	IN	PDM_DMIC_DATA1 (PLACE_NEAR=U0600.BB14:20MM	TOP	TPU6657 TP-P4
145 135 10	IN	PDM_DMIC_DATA0 (PLACE_NEAR=U0600.BB15:20MM	TOP	TPU6658 TP-P4

T818 — FUNC_TEST

145 32 31	IN	USBC5_CC1	TOP	TPU6663 TP-P4

DUMMY TEST POINTS TO MATCH C/S TPs

NC_DUMMY_TP_SOC_KIS_DFU_SELECT	TOP	TPU66A0 TP-P4	CKPLUS_WAIVE=NC_CHECKS
NC_DUMMY_TP_BOARD_ID0	TOP	TPU66A1 TP-P4	CKPLUS_WAIVE=NC_CHECKS
NC_DUMMY_TP_BOARD_ID1	TOP	TPU66A2 TP-P4	CKPLUS_WAIVE=NC_CHECKS
NC_DUMMY_TP_BOARD_ID2	TOP	TPU66A3 TP-P4	CKPLUS_WAIVE=NC_CHECKS
NC_DUMMY_TP_BOARD_ID3	TOP	TPU66A4 TP-P4	CKPLUS_WAIVE=NC_CHECKS
NC_DUMMY_TP_BOARD_ID4	TOP	TPU66A5 TP-P4	CKPLUS_WAIVE=NC_CHECKS
NC_DUMMY_TP_BOARD_REV0	TOP	TPU66A6 TP-P4	CKPLUS_WAIVE=NC_CHECKS
NC_DUMMY_TP_BOARD_REV1	TOP	TPU66A7 TP-P4	CKPLUS_WAIVE=NC_CHECKS
NC_DUMMY_TP_SMC_FIXTURE_MODE_L	TOP	TPU66A8 TP-P4	CKPLUS_WAIVE=NC_CHECKS
NC_DUMMY_TP_FPMU_3V8_ISENSE	TOP	TPU66B0 TP-P4	CKPLUS_WAIVE=NC_CHECKS
	TOP	TPU66B3 TP-P4	
NC_DUMMY_TP_PMU_SYS_ALIVE	TOP	TPU66C5 TP-P4	CKPLUS_WAIVE=NC_CHECKS

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DFU, Debug

		FUNC_TEST	
I3	USB2_ATC0_LS_P	TPU7A2 TP-P4	PLACE_NEAR=RH001.2:5MM
I4	USB2_ATC0_LS_N	TPU7A3 TP-P4	PLACE_NEAR=RH001.2:5MM
I1	USBC0_USB_TOP_P	TRUE	77 78 84
I2	USBC0_USB_TOP_N	TRUE	77 78 84
I5	USB_DBG_LS_N	TRUE	158
I6	USB_DBG_LS_P	TRUE	158
IN	SOC_DOCK_CONNECT	TPU6671 TP-P4	
I8	SOC_DFU_STATUS	TRUE	5 83 146
I9	SOC_FORCE_DFU_DBG	TRUE	147
I10	UART_DEBUGPRT_R2D	TRUE	6 83 143 144
I11	UART_DEBUGPRT_D2R	TRUE	6 83 143 144
I12	SWD_SOC_SWCLK	TRUE	12 83 143
I13	SWD_SOC_SWDIO	TRUE	12 83 143
I14	UART_DEBUGPRT_R2D	TRUE	6 83 143 144
I15	UART_DEBUGPRT_D2R	TRUE	6 83 143 144
I16	SMC_FIXTURE_MODE_L	TRUE	10 143
I19	PMU_SYS_ALIVE	TRUE	46 96 116 121 126 155
I638	P5VS2HOLD_PWR_EN	TRUE	38 46 145
I20	PMU_ACTIVE_READY	TRUE	5 10 46 143 146 155
I21	PMU_ONOFF_L	TRUE	28 38 46 141 147
I22	PMU_RSLOC_RST_L	TRUE	38 46 137 147
I23	SOC_SOCHOT_L	TRUE	5 46
I24	PMU_RESET_L	TRUE	10 46 143
I25	PMU_SHDN	TRUE	38 46 147
I643	RTMRMUX_OE_L	TRUE	149
I644	USB0_3V3_LDO_EN_VITC	TRUE	158
I676	USBC0_3V3LDO_EN	TRUE	149

Battery

		FUNC_TEST	
I26	PPVBAT_AON	TPU700 TP-P4	
		TPU701 TP-P4	
		TPU702 TP-P4	
		TPU703 TP-P4	
		TPU704 TP-P4	
		TPU705 TP-P4	
		TPU706 TP-P4	
		TPU707 TP-P4	
		TPU708 TP-P4	
		TPU709 TP-P4	
		TPU710 TP-P4	
		TPU711 TP-P4	
		TPU712 TP-P4	
		TPU713 TP-P4	
		TPU714 TP-P4	
		TPU715 TP-P4	
		TPU716 TP-P4	
I27	SMBUS_BATT_SDA	TRUE	28 65 145
I28	SMBUS_BATT_SCL	TRUE	28 65 145
I29	SYS_DETECT_L	TRUE	28
I30	SYS_DETECT	TRUE	28 147
I605	I2C_SMC_PWR_SCL	TRUE	10 65
I606	I2C_SMC_PWR_SDA	TRUE	10 65
	GND	TPU717 TP-P4	

Charger

		FUNC_TEST	
I32	PPDCIN_AON	TPU718 TP-P4	
		TPU719 TP-P4	
		TPU720 TP-P4	
		TPU721 TP-P4	
		TPU722 TP-P4	
		TPU723 TP-P4	
		TPU724 TP-P4	
		TPU725 TP-P4	
		TPU726 TP-P4	
		TPU727 TP-P4	
		TPU728 TP-P4	
I33	PPDCIN_AON	TRUE	144 150
I34	PPHV_INT5_AONSW	TRUE	33 145
I35	PPVBUS_USBC5	TPU729 TP-P4	
		TPU730 TP-P4	
		TPU731 TP-P4	
		TPU732 TP-P4	
		TPU733 TP-P4	
		TPU734 TP-P4	
		TPU735 TP-P4	
		TPU736 TP-P4	
		TPU737 TP-P4	
		TPU738 TP-P4	
		TPU739 TP-P4	
I616	CHGR_INT_L	TRUE	10 30 156
I617	CHGR_RST_IN	TRUE	28 29 38
I618	CHGR_THMSNS	TRUE	73 74
	GND	TPU740 TP-P4	
		TPU741 TP-P4	
		TPU742 TP-P4	
		TPU743 TP-P4	
		TPU744 TP-P4	
		TPU745 TP-P4	
		TPU746 TP-P4	
		TPU747 TP-P4	
		TPU748 TP-P4	
		TPU749 TP-P4	
		TPU750 TP-P4	

Power rails

		FUNC_TEST	
I62	PPBUS_AON	TPU751 TP-P4	
		TPU752 TP-P4	
		TPU753 TP-P4	
		TPU754 TP-P4	
		TPU755 TP-P4	
		TPU756 TP-P4	
		TPU757 TP-P4	
		TPU758 TP-P4	
		TPU759 TP-P4	
		TPU760 TP-P4	
		TPU761 TP-P4	
I53	PP3V8_AON	TRUE	150 159
I64	PPVDD_DISP_INT_AWAKESW	TRUE	153
I55	PPVDD_SRAM_S1	TRUE	153
I57	PP1V8_S2SW_VDD1	TRUE	17 148
I58	PPVDDQ0_S1	TRUE	153
I59	PPVDDQ1_S1	TRUE	153
I60	PPVDD_CIO_S2SW	TRUE	153
I62	PPVDD_AMPH1_S2SW	TRUE	153
I63	PPVDD_AMPH0_S2SW	TRUE	153
I64	PPVDD_ECPU_AWAKESW	TRUE	153
I65	PP1V8_AWAKE	TRUE	150 153
I67	PPVDD_FIXED_S1	TRUE	153
I68	PPVDD_SOC_S1	TRUE	145 146 153
I69	PPVDD_DCS_S1	TRUE	153
I71	PP1V8_S2	TRUE	150 153
I72	PP1V2_S2	TRUE	150 153 159
I74	PP1V8_AON	TRUE	150 153 159
I75	PP1V2_AWAKE	TRUE	150 153
I83	PP0V9_NAND0	TRUE	116
I84	PP1V2_NAND0	TRUE	116
I85	PP2V5_NAND0	TRUE	116
I86	PP0V9_NAND1	TRUE	121
I87	PP1V2_NAND1	TRUE	121
I88	PP2V5_NAND1	TRUE	121
I659	PP1V2_ATCRTMR01_VDDIO	TRUE	98
I658	PP1V2_ATCRTMR2_VDDIO	TRUE	98
I92	PP5V_S2SW_USBC01	TRUE	145 151
I93	PP5V_S2SW_USBC23	TRUE	145 151
I94	PPMDB_AWAKESW_TCON	TRUE	150
I95	PP3V3_AON	TRUE	146 150 153
I96	PP3V3_S2	TRUE	146 150 153
I97	PP5V_S2_HOLD	TPU762 TP-P4	
		TPU763 TP-P4	
I98	PP3V3_UPC0_LDO	TRUE	82 83 84
I100	PPVBAT_AON_CHGR_R	TRUE	29
I101	PPBUS_AON	TPU764 TP-P4	
		TPU765 TP-P4	
		TPU766 TP-P4	
I660	PP0V95_AWAKESW_DP2HDMI	TRUE	101 103
I670	PP1V85_S2_HOLD_KBD	TRUE	138 151

Fan

		FUNC_TEST	
I102	PPBUS_AON_FAN0_FILT	TPU767 TP-P4	76
		TPU768 TP-P4	
		TPU769 TP-P4	
I103	SMC_FAN_0_PWM_3V3	TRUE	76
I104	FAN_0_TACH	TRUE	76
I105	PPBUS_AON_FAN1_CONN	TPU770 TP-P4	76 151
		TPU771 TP-P4	
		TPU772 TP-P4	
I106	SMC_FAN_1_PWM_3V3	TRUE	76
I107	FAN_1_TACH	TRUE	76
I580	FAN_PWR_EN	TRUE	46 76
	GND	TPU773 TP-P4	
	GND	TPU774 TP-P4	
	GND	TPU775 TP-P4	
	GND	TPU776 TP-P4	

USB-C

		FUNC_TEST	
I312	PPVBUS_USBC0	TPU778 TP-P4	77 78 84 145
		TPU779 TP-P4	
		TPU780 TP-P4	
		TPU781 TP-P4	
		TPU782 TP-P4	
		TPU783 TP-P4	
I313	USBC0_SBU1	TRUE	77 78 84
I314	USBC0_SBU2	TRUE	77 78 84
I315	USBC0_CC1	TRUE	77 78 83 84 145
I316	USBC0_CC2	TRUE	77 78 83 84 145
	GND	TPU784 TP-P4	
I319	PPVBUS_USBC1	TPU785 TP-P4	77 78 85 145
		TPU786 TP-P4	
		TPU787 TP-P4	
		TPU788 TP-P4	
		TPU789 TP-P4	
		TPU790 TP-P4	
I120	USBC1_CC1	TRUE	77 78 83 85 145
I121	USBC1_CC2	TRUE	77 78 83 85 145
I122	USBC1_SBU1	TRUE	77 78 85
I123	USBC1_SBU2	TRUE	77 78 85
	GND	TPU791 TP-P4	
I126	PPVBUS_USBC2	TPU792 TP-P4	78 79 93 145
		TPU793 TP-P4	
		TPU794 TP-P4	
		TPU795 TP-P4	
		TPU796 TP-P4	
		TPU797 TP-P4	
I127	USBC2_CC1	TRUE	78 79 92 93 145
I128	USBC2_CC2	TRUE	78 79 92 93 145
I677	ATC01_VDDFIXED_VR_EN	TRUE	87 89
I673	ATCRTMR0_RESET_1V2_1V8_MCW_L	TRUE	158
I674	LPDP_FTCAM_DATA_C_P<0>	TRUE	124
I675	LPDP_FTCAM_DATA_C_N<0>	TRUE	124
	GND	TPU798 TP-P4	
	GND	TPU799 TP-P4	

Camera

		FUNC_TEST	
I141	PP5V_S2_CAMERA	TRUE	151
I142	I2C_CAM_1V8_SDA	TRUE	66 124
I143	I2C_ALS_1V8_SDA	TRUE	66 124
I144	I2C_CAM_1V8_SCL	TRUE	66 124
I145	I2C_ALS_1V8_SCL	TRUE	66 124
I146	ALS_INT_L	TRUE	10 124
I147	FTCAM_ENABLE_1V8_OUT	TRUE	123 156
I660	LPDP_FTCAM_DATA_P<0>	TRUE	7 123 124
I661	LPDP_FTCAM_DATA_N<0>	TRUE	7 123 124

Display

		FUNC_TEST	
I149	PP3V8_AWAKESW_TCON	TRUE	151
I150	I2C_SMC_SNS0_SCL_1V8	TRUE	66
I151	I2C_SMC_SNS0_SDA_1V8	TRUE	66
I152	UART_TCON_D2R_1V8	TRUE	125
I153	EDP_PANEL_1V8_EN	TRUE	125 126
I154	LPDP_INT_HPD	TRUE	7 125 154 156
I155	SPI_TCON_CS_L	TRUE	13 125
I156	SPI_TCON_MISO	TRUE	6 125
I157	SPI_TCON_MOSI	TRUE	13 125
I158	SPI_TCON_CLK	TRUE	13 125
	GND	TPU800 TP-P4	

Backlight

		FUNC_TEST	
I160	I2C_DISP_BKLT_SCL_1V8	TRUE	64 128
I161	I2C_DISP_BKLT_SDA_1V8	TRUE	64 128
I162	BL_PMIC_PWR_EN	TRUE	38 128
I163	PPVOUT_LUXE	TRUE	127 128 144
		TPU801 TP-P4	
		TPU802 TP-P4	
		TPU803 TP-P4	
		TPU804 TP-P4	
		TPU805 TP-P4	
		TPU806 TP-P4	
I164	PP1V2_AWAKESW_BLC	TRUE	128 150
I165	PPBCON_AWAKESW_BKLTCONN	TRUE	128 151
I166	DISP_BKLT_LSYNC	TRUE	7 128
I167	BKLT_BOOST_THROTTLE_CONN_L	TRUE	128
I168	DISP_BKLT_FSYNC	TRUE	7 128

SPI

		FUNC_TEST	
I169	SPI_DISP_BKLT_CS_L	TRUE	7 128
I170	SPI_DISP_BKLT_MISO	TRUE	7 128 145
I171	SPI_DISP_BKLT_MOSI	TRUE	13 128
I172	SPI_DISP_BKLT_CLK	TRUE	13 128
	GND	TP807 TP-P4	

AMR

		FUNC_TEST	
I174	MGL_1V8	TRUE	129 130
I175	AMR1_OR_ND_1V8	TRUE	129 156
I176	SPI_LAS_CS_1V8_L	TRUE	14 129
I177	SPI_AOP_LAS_CLK_1V8	TRUE	14 129
I178	SPI_AOP_LAS_MISO_1V8_R	TRUE	129
I179	SPI_AOP_LAS_MOSI_1V8	TRUE	14 129
	GND	TPU808 TP-P4	

Audio Jack

		FUNC_TEST	
I181	AUD_CONN_HP_LEFT	TRUE	135
I182	AUD_CONN_SLEEVE	TRUE	135
I183	AUD_CONN_HP_RIGHT	TRUE	135
I184	AUD_CONN_RING2	TRUE	135
I185	AUD_CONN_TIP_SENSE	TRUE	135
I186	AUD_CONN_HP_SENSE_L	TRUE	135
I187	AUD_CONN_RING2_XW	TRUE	135
I188	AUD_CONN_RING_SENSE	TRUE	135
I189	AUD_CONN_HP_SENSE_R	TRUE	135
I190	AUD_CONN_SLEEVE_XW	TRUE	135
	GND	TPU809 TP-P4	

Touch ID

		FUNC_TEST	
I191	PP1V8_TOUCHID_FILT_CONN	TRUE	141 142
I192	SPI_TOUCHID_MISO_1V8_CONN	TRUE	141
I193	SPI_TOUCHID_MOSI_1V8_CONN	TRUE	141
I194	TOUCHID_INT_1V8_CONN	TRUE	141 142
I195	SPI_TOUCHID_CLK_1V8_CONN	TRUE	141
I196	TOUCHID_BOOST_EN_CONN	TRUE	141
I197	PP16V0_TOUCHID_FILT_CONN	TRUE	141 142
I697	TOUCHID_PWR_EN	TRUE	10 142
I198	PP3V0_TOUCHID_FILT_CONN	TRUE	141 142
		TPU810 TP-P4	
		TPU811 TP-P4	
		TPU812 TP-P4	
		TPU813 TP-P4	
	GND		

Audio speaker amp

		FUNC_TEST	
I200	SPKRAMP_A_OUTP	TPU815 TP-P4	132 134
		TPU816 TP-P4	
		TPU817 TP-P4	
I207	SPKRAMP_A_OUTN	TPU818 TP-P4	132 134
		TPU819 TP-P4	
		TPU820 TP-P4	
I208	SPKRAMP_B_OUTP	TPU821 TP-P4	132 134
		TPU822 TP-P4	
		TPU823 TP-P4	
I209	SPKRAMP_B_OUTN	TPU824 TP-P4	132 134
		TPU825 TP-P4	
		TPU826 TP-P4	
I210	SPKRAMP_C_OUTP	TPU827 TP-P4	132 134
		TPU828 TP-P4	
		TPU864 TP-P4	
I211	SPKRAMP_C_OUTN	TPU829 TP-P4	132 134
		TPU830 TP-P4	
		TPU831 TP-P4	
I212	SPKR_ID0	TRUE	6 134
	GND	TPU832 TP-P4	
	GND	TPU833 TP-P4	
	GND	TPU834 TP-P4	
	GND	TPU835 TP-P4	
I217	SPKRAMP_D_OUTP	TPU836 TP-P4	133 134
		TPU837 TP-P4	
		TPU838 TP-P4	
I218	SPKRAMP_D_OUTN	TPU839 TP-P4	133 134
		TPU840 TP-P4	
		TPU841 TP-P4	
I219	SPKRAMP_E_OUTP	TPU842 TP-P4	133 134
		TPU843 TP-P4	
		TPU844 TP-P4	
I220	SPKRAMP_E_OUTN	TPU845 TP-P4	133 134
		TPU846 TP-P4	
		TPU847 TP-P4	

Keyboard

		FUNC_TEST	
I221	SPKRAMP_F_OUTP	TPU848 TP-P4	133 134
		TPU849 TP-P4	
		TPU850 TP-P4	
I222	SPKRAMP_F_OUTN	TPU851 TP-P4	133 134
		TPU852 TP-P4	
		TPU853 TP-P4	
I223	SPKR_ID1	TRUE	6 134
	GND	TPU854 TP-P4	
	GND	TPU855 TP-P4	
	GND	TPU856 TP-P4	
I220	KBD_ID1	TRUE	137 138
I665	KBD_ID2	TRUE	137 138
I230	KBD_DRIVE_Y8	TRUE	137 138
I666	KBD_DRIVE_Y9	TRUE	137 138
I667	KBD_DRIVE_Y10	TRUE	137 138
I668	KBD_DRIVE_Y11	TRUE	137 138
I231	KBD_DRIVE_Y2	TRUE	137 138
I232	KBD_DRIVE_Y1	TRUE	137 138
I233	KBD_DRIVE_Y3	TRUE	137 138
I234	KBD_DRIVE_Y4	TRUE	137 138
I235	KBD_SENSE_X0	TRUE	137 138
I236	KBD_SENSE_X1	TRUE	137 138
I237	KBD_SENSE_X2	TRUE	137 138
I238	KBD_SENSE_X5	TRUE	137 138
I239	KBD_SENSE_X3	TRUE	137 138
I240	KBD_SENSE_X9	TRUE	137 138
I241	KBD_SENSE_X12	TRUE	137 138
I242	KBD_SENSE_X4	TRUE	137 138
I243	KBD_SENSE_X11	TRUE	137 138
I244	KBD_SENSE_X10	TRUE	137 138
I245	KBD_SENSE_X6	TRUE	137 138
I246	KBD_SENSE_X7	TRUE	137 138
I247	KBD_SENSE_X8	TRUE	137 138
I248	KBD_DRIVE_Y5	TRUE	137 138
I249	KBD_DRIVE_Y7	TRUE	137 138
I250	KBD_DRIVE_Y6	TRUE	137 138
I251	KBD_DRIVE_Y0	TRUE	137 138
I252	KBD_CAP_CATHODE	TRUE	137 138
I253	PP3V3_AON_KBD_CONN	TRUE	137 138
I254	KBD_RIGHT_SHIFT_KEY	TRUE	137 138
I255	KBD_LEFT_OPTION_KEY	TRUE	137 138
I256	KBD_CONTROL_KEY	TRUE	137 138
	GND	TPU857 TP-P4	
I258	PPVOUT_KBDLED_CONN	TRUE	148 151
I259	KBDLED_CATHODE1	TRUE	136 138
I260	KBDLED_CATHODE2	TRUE	136 138
	GND	TPU858 TP-P4	
	GND	TPU859 TP-P4	

Trackpad

		FUNC_TEST	
I262	IPD_LID_OPEN_1V8	TRUE	28 38 130 140
I263	I2C_TPAD_CONN_SCL	TRUE	66 140
I264	I2C_TPAD_CONN_SDA	TRUE	66 140
I265	IPD_WAKE_L	TRUE	38 139
I266	KBD_INT_L	TRUE	137 140
I268	I2C_KBD_SDA	TRUE	137 140 158
I269	I2C_KBD_SCL	TRUE	137 140 158
I270	SPI_IPD_MOSI_CONN	TRUE	139 140
I271	SPI_IPD_MCU_CS_CONN_L	TRUE	139 140
I272	SPI_IPD_MISO_CONN	TRUE	139 140 148
I274	SPI_IPD_CLK_CONN	TRUE	139 140
I275	PP5V_S2_HOLD_TPAD_CONN	TRUE	140
I276	PP3V3_S2_HOLD_IPD	TRUE	140 151
	GND	TPU860 TP-P4	

Card Reader

		FUNC_TEST	
I278	SDCONN_CMD_R_FL	TRUE	107
I280	PP3V3_GL_SDCONN	TRUE	106 107
I281	SDCONN_CLK_CONN_FL	TRUE	107
I282	SDCONN_D0_R_FL	TRUE	107
I283	SDCONN_D1_R_FL	TRUE	107
I284	SDCONN_D2_R_FL	TRUE	107
I285	SDCONN_D3_R_FL	TRUE	107
I286	SDCONN_SD0_UHS2_P	TRUE	106 107
I287	SDCONN_SD0_UHS2_N	TRUE	106 107
I288	SDCONN_SD1_UHS2_P	TRUE	106 107
I289	SDCONN_SD1_UHS2_N	TRUE	106 107
I290	PP1V8_GL_SDCONN	TRUE	106 107
I664	SDCONN_WP	TRUE	106 107
I663	SDCONN_DETECT	TRUE	107 108
I678	SDCONN_STATE_CHANGE	TPU899 TP-P4 BOTTOM	
	GND	TPU861 TP-P4	

Misc

		FUNC_TEST	
I648	SOC_TESTMODE	TRUE	5
I647	SOC_HOLD_RESET	TPU7A1 TP-P4	5 143
I632	SE_PWR_EN	TRUE	27 38 46

LUXE

		FUNC_TEST	
I294	I2C_LUXE_DEBUG_SCL	TRUE	64 127
I295	I2C_LUXE_DEBUG_SDA	TRUE	64 127
I296	LUXE_VPROG_TEST	TRUE	127
I297	PPBUS_AON_LUXE	TRUE	151
I298	PPLUXE_INPUT_R_V	TRUE	127 144 148
I299	PPVOUT_LUXE	TRUE	127 128 144
I300	PPLUXE_LX1	TRUE	127 148
I301	PPLUXE_LX2	TRUE	127 148
I302	LUXE_UG1	TRUE	127
I303	LUXE_LG1	TRUE	127
I304	LUXE_UG2	TRUE	127
I305	LUXE_LG2	TRUE	127
I306	BL_PWR_EN	TRUE	38 127
I307	SPMI_DISP_BKLT_CLK_R	TRUE	7 13
I308	SPMI_DISP_BKLT_DATA_R	TRUE	7 13
I309	BKLT_BOOST_THROTTLE_LUXE_L	TRUE	127
I310	PVOUT_LUXE_R	TRUE	127
I311	PPLUXE_INPUT_R_V	TRUE	127 144 148
I312	LUXE_AGND	TRUE	127
	GND	TPU862 TP-P4	

KBD Backlight

		FUNC_TEST	
I313	PP5V_S2_HOLD	TRUE	136 150
I314	KBDBKLT_SW2	TRUE	136 148
I315	KBDBKLT_FB2	TRUE	136
I316	KBDLED_KEYB1	TRUE	136
I317	KBDLED_KEYB2	TRUE	136
I318	KBD_BKLT_PWM_3V3	TRUE	136
I319	KBDBKLT_ISET_KEYB	TRUE	136 145
	GND	TPU863 TP-P4	

CLVR

		FUNC_TEST	

NAND

		FUNC_TEST	
I557	TP_NAND0_OCARINA_VCC_DET	TRUE	116
I554	TP_NAND0_S5E0_DROOP_L	TRUE	112
I555	TP_NAND0_S5E0_VPP	TRUE	112
I556	TP_NAND0_S5E1_DROOP_L	TRUE	113
I553	TP_NAND0_S5E1_VPP	TRUE	113
I552	TP_NAND0_S5E2_DROOP_L	TRUE	114
I551	TP_NAND0_S5E2_VPP	TRUE	114
I550	TP_NAND0_S5E3_DROOP_L	TRUE	115
I549	TP_NAND0_S5E3_VPP	TRUE	115
I548	TP_NAND1_OCARINA_VCC_DET	TRUE	121
I547	TP_NAND1_S5E0_DROOP_L	TRUE	117
I546	TP_NAND1_S5E0_VPP	TRUE	117
I545	TP_NAND1_S5E1_DROOP_L	TRUE	118
I544	TP_NAND1_S5E1_VPP	TRUE	118
I543	TP_NAND1_S5E2_DROOP_L	TRUE	119
I542	TP_NAND1_S5E2_VPP	TRUE	119
I541	TP_NAND1_S5E3_DROOP_L	TRUE	120
I540	TP_NAND1_S5E3_VPP	TRUE	120

HDMI

		FUNC_TEST	
I539	HDMI_CEC_CONN	TRUE	99
I538	HDMI_DDC_5V_CONN_SCL	TRUE	99
I537	HDMI_DDC_5V_CONN_SDA	TRUE	99
I536	HDMI_HPD_IN_CONN	TRUE	99
I535	HDMI_RSVD	TRUE	99
	GND	TPU866 TP-P4	
I680	SPMI_UPC5_DATA	TRUE	12 155
I681	SPMI_UPC5_CLK	TRUE	12 155
I682	SOC_DOCK_CONNECT_DBG_UPC	TRUE	82 83 87
I683	CHGR_AUX_DET_SHORT	TRUE	29 98
I684	PP1V8_AON_DEADBATTERY_R	TRUE	28

PAGE TITLE

FCT 2

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BRANCH

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USBC Debug 3mm PP PLACE_SIDE=BOTTOM

144 84 78 77	1652	PPVBUS_USBC0	BOTTOM 1	PP	PPU8E0 P3MM
82	1650	PPHV_INT0_AONSW	BOTTOM 1	PP	PPU8E1 P3MM
151 144	1649	PP5V_S2SW_USBC01	BOTTOM 1	PP	PPU8E2 P3MM
144 85 78 77	1648	PPVBUS_USBC1	BOTTOM 1	PP	PPU8E3 P3MM
82	1647	PPHV_INT1_AONSW	BOTTOM 1	PP	PPU8E4 P3MM
144 93 79 78	1646	PPVBUS_USBC2	BOTTOM 1	PP	PPU8E5 P3MM
91	1645	PPHV_INT2_AONSW	BOTTOM 1	PP	PPU8C6 P3MM
151 144	1644	PP5V_S2SW_USBC23	BOTTOM 1	PP	PPU8C7 P3MM
144 32 31	1643	PPVBUS_USBC5	BOTTOM 1	PP	PPU8C8 P3MM
144 33	1641	PPHV_INT5_AONSW	BOTTOM 1	PP	PPU8C9 P3MM

DCDC Debug 3mm PP

144 65 28	1629	SMBUS_BATT_SCL	BOTTOM 1	PP	PPU8D2 P3MM
144 65 28	1631	SMBUS_BATT_SDA	BOTTOM 1	PP	PPU8D3 P3MM
29	1638	CHGR_COMP	TOP 1	PP	PPU8D4 P3MM
29	1632	CHGR_BGATE	TOP 1	PP	PPU8D5 P3MM
	1637	SPI_DISP_BKLT_MISO	BOTTOM 1	PP	PPU8D9 P3MM

PLACE_NEAR=U0600.BP78:17MM

1645	I2C_UPC0_ATCRTMR0_SCL	TRUE	80 82 84 145 155
1646	I2C_UPC0_ATCRTMR0_SDA	TRUE	80 82 84 145 155

MISC Power Rails FUNC_TEST

1678	P5VS2HOLD_PGOOD	TRUE	37 62 145 156
1660	HDMI_HPD_AOP	TRUE	10 102
1673	PMU_VDDHI_UVWARN_L	TRUE	5 46
1672	PMU_VDDMAIN_UVWARN_L	TRUE	5 46
1679	DBL_CLICK_DET	TRUE	6 46 145
1692	TP_AON_SLEEP1_RESET_L	TRUE	10 145
1638	USBC0_CC1	TRUE	77 78 83 84 144
1698	USBC0_CC2	TRUE	77 78 83 84 144
1697	USBC1_CC1	TRUE	77 78 83 85 144
1688	USBC1_CC2	TRUE	77 78 83 85 144
1689	USBC2_CC1	TRUE	78 79 92 93 144
1698	USBC2_CC2	TRUE	78 79 92 93 144

USB-C (cont.) FUNC_TEST

1618	P5VUSBC01_EN	TRUE	88
1615	P5VUSBC23_EN	TRUE	96
1671	UPC5_SER_DBG	TRUE	32 33
1675	PD_UPC0_MRESET	TRUE	84
1676	PD_UPC5_MRESET	TRUE	32
1674	I2C_UPC015_3V3_SDA	TRUE	98 155
1675	I2C_UPC015_3V3_SCL	TRUE	98 155
1676	I2C_UPC2_3V3_SDA	TRUE	91 92 98
1677	I2C_UPC2_3V3_SCL	TRUE	91 92 98
1678	I2C_UPC015_3V3_SDA	TRUE	32 33 155
1679	I2C_UPC015_3V3_SCL	TRUE	32 33 155
1683	USBC0_LDCM_LB	TRUE	77 78 83 84
1682	USBC1_LDCM_LB	TRUE	77 78 83 85
1681	USBC2_LDCM_LB	TRUE	78 79 92 93
1684	ATCRTMR0_JTAG_SEL	TRUE	80
1685	ATCRTMR0_TESTMODE	TRUE	80
1693	ATCRTMR0_JTAG_TDO	TRUE	80
1686	ATCRTMR1_JTAG_SEL	TRUE	81
1687	ATCRTMR1_TESTMODE	TRUE	81
1692	ATCRTMR1_JTAG_TDO	TRUE	81
1693	ATCRTMR2_JTAG_SEL	TRUE	90
1690	ATCRTMR2_TESTMODE	TRUE	90
1688	ATCRTMR2_JTAG_TDO	TRUE	90
1693	SPI_UPC0_MOSI	TRUE	82
1694	SPI_UPC0_MISO	TRUE	82
1695	SPI_UPC0_CLK	TRUE	82
1696	SPI_UPC0_CS_L	TRUE	82
1697	SPI_UPC1_MOSI	TRUE	82
1698	SPI_UPC1_MISO	TRUE	82
1699	SPI_UPC1_CLK	TRUE	82
1688	SPI_UPC1_CS_L	TRUE	82
1691	SPI_UPC2_MOSI	TRUE	91
1692	SPI_UPC2_MISO	TRUE	91
1688	SPI_UPC2_CLK	TRUE	91
1684	SPI_UPC2_CS_L	TRUE	91
1688	SPI_UPC5_MOSI	TRUE	33
1688	SPI_UPC5_MISO	TRUE	33
1688	SPI_UPC5_CLK	TRUE	33
1697	SPI_UPC5_CS_L	TRUE	33
1236	CLVR_RESET_L	TRUE	46 56 57 58 59 60 145
1235	P3V8AON_PWR_EN	TRUE	28 29 30 34 143

NAND (cont.) FUNC_TEST

1177	I2C_SMC_NAND_SCL	TRUE	10 65
1175	I2C_SMC_NAND_SDA	TRUE	10 65
1174	NAND0_OCARINA_VREF	TRUE	116
1174	NAND1_OCARINA_VREF	TRUE	121
1172	NAND1_S5E0_JTAG_TDO	TRUE	117 118
1173	P2V5_NAND0_PGOOD	TRUE	116
1170	P2V5_NAND1_PGOOD	TRUE	121
1171	PPVDD_LDO_NAND0_OCARINA	TRUE	116
1169	PPVDD_LDO_NAND1_OCARINA	TRUE	121

SoC FUNC_TEST

1167	I2C_SEEPROM_SCL	TRUE	6 11
1166	I2C_SEEPROM_SDA	TRUE	6 11

NAND (cont.) FUNC_TEST

1165	NAND0_OCARINA_TDEV1	TRUE	116
1164	NAND1_OCARINA_TDEV2	TRUE	121 145
1162	NAND0_S5E0_JTAG_TDO	TRUE	112 113
1160	NAND0_S5E1_JTAG_TDO	TRUE	113 114
1161	NAND0_S5E2_JTAG_TDO	TRUE	114 115
1159	NAND1_OCARINA_TDEV1	TRUE	121
1158	NAND1_OCARINA_TDEV2	TRUE	121 145
1157	P2V5_NAND0_EN_R	TRUE	116
1156	P2V5_NAND1_EN_R	TRUE	121

PMICs FUNC_TEST

1125	PMU_CLK32K_CLVR	TRUE	38 56 57 58 59 60
1585	PVDD1_PWR_EN	TRUE	17 46
1589	VDDH_SPS_CTRL0_EN	TRUE	51 52 53 54
1588	PMU_ONOFF_L_CONN	TRUE	141

WLBT FUNC_TEST

1110	PMU_CLK32K_WLBT	TRUE	38 110 111
1111	BT_TIME_SYNC	TRUE	6 110 111
1109	WLBT_PWR_EN	TRUE	38 46 110 111

IPD FUNC_TEST

1108	CAPSLOCK_LED_EN	TRUE	137
1107	IOXP1_RESET_L	TRUE	137
1105	IOXP2_RESET_L	TRUE	137
1106	KBDBKLT_ISET_KEYB	TRUE	136 144

Sensor FUNC_TEST

1201	AIRFLOW_C_THMSNS	TRUE	73 74
1200	AIRFLOW_L_THMSNS	TRUE	73 74
1195	AIRFLOW_R_THMSNS	TRUE	73 74
1194	DCIN_VSENSE	TRUE	67 74
1193	FINSTACK_L_THMSNS	TRUE	73 74
1192	FINSTACK_R_THMSNS	TRUE	73 74
1191	LPMU_THMSNS	TRUE	73 74
1190	P3V8AON_THMSNS	TRUE	73 74
1186	PBUS_VSENSE	TRUE	67 74
1185	SOC_THMSNS_1	TRUE	73 74
1184	FPMU_THMSNS	TRUE	73 74
1186	WING_L_THMSNS	TRUE	73 74
1182	WING_R_THMSNS	TRUE	73 74
1183	WLBT_THMSNS	TRUE	73 74
1181	WLBT_THMSNS	TRUE	73 74

1416	PP5V0_HDMI_DDC_CONN	TRUE	99 103 145
1625	PP5V0_HDMI_DDC_CONN	TP TOP	TPU897
1414	PPVDD_LOW_S2	TRUE	153
1417	PP1V8_S2SW_SNS	TRUE	145 150
1425	PP5V_S2_HDMI	TRUE	103 150
1426	PP1V2_AWAKESW_DP2HDMI	TRUE	101 103
1428	PP3V3_AWAKESW_DP2HDMI	TRUE	99 101 102 103

Additional TP per HWTE

USB2 DEBUG PPs

P3MM SM	PPU800	BOTTOM 1 PP	TP_MACAW0_DEBUG_SWDCLK 86
P3MM SM	PPU801	BOTTOM 1 PP	TP_MACAW0_DEBUG_SWDDAT 86
P3MM SM	PPU802	BOTTOM 1 PP	TP_MACAW1_DEBUG_SWDCLK 86
P3MM SM	PPU803	BOTTOM 1 PP	TP_MACAW1_DEBUG_SWDDAT 86
P3MM SM	PPU804	BOTTOM 1 PP	TP_MACAW2_DEBUG_SWDCLK 94
P3MM SM	PPU805	BOTTOM 1 PP	TP_MACAW2_DEBUG_SWDDAT 94

MISC FUNC_TEST

1560	SPI_ATCRTMR0_CS_L	TRUE	80
1561	SPI_ATCRTMR1_CS_L	TRUE	81
1562	SPI_ATCRTMR2_CS_L	TRUE	90
1563	SPI_SOCROM_CS_L	TRUE	6 11
1563	SPI_UPC0_R_CS_L	TRUE	82 84
1564	SPI_UPC1_R_CS_L	TRUE	82 85
1565	SPI_UPC2_R_CS_L	TRUE	91 93
1566	SPI_UPC5_R_CS_L	TRUE	32 33
1570	I2C_NAND_PMIC_SCL_1V8	TRUE	65 116 121
1568	I2C_NAND_PMIC_SDA_1V8	TRUE	65 116 121
1569	SWD_NUB_ATCRTMR01_SWCLK	TRUE	12 156
1438	I2C_UPC0_ATCRTMR0_SCL	TRUE	80 82 84 145 155
1437	I2C_UPC0_ATCRTMR0_SDA	TRUE	80 82 84 145 155
1439	ATCRTMR0_RESET_L	TRUE	80 82 84 149
1440	I2C_UPC1_ATCRTMR1_SCL	TRUE	81 82 85 155
1441	I2C_UPC1_ATCRTMR1_SDA	TRUE	81 82 85 155
1443	ATCRTMR1_RESET_L	TRUE	81 82 85 86
1442	UPC01_5V_EN	TRUE	88 155
1444	I2C_UPC2_ATCRTMR2_SCL	TRUE	90 91 93 155
1446	I2C_UPC2_ATCRTMR2_SDA	TRUE	90 91 93 155
1445	ATCRTMR2_RESET_L	TRUE	90 91 93 94 104
1447	UPC23_5V_EN	TRUE	92 93 96
1449	USBC2_SBU1	TRUE	78 79 93
1448	USBC2_SBU2	TRUE	78 79 93

DIGITAL MIC FUNC_TEST

1405	PDM_DMIC_DATA1	TRUE	10 135 143
1411	PDM_DMIC_DATA0	TRUE	10 135 143
135 1404	PDM_DMIC_CLK5_1V8	TOP 1 TP	TPU865 TP-P4

PLACE_NEAR=JR940.1:20MM

1408	PDM_DMIC_DATA0_1V8	TRUE	135
1407	PP1V8_DMIC	TRUE	135
1406	PDM_DMIC_CLK6_1V8	TRUE	135
1405	PDM_DMIC_DATA1_1V8	TRUE	135
	GND	TOP 1 TP	TPU814 TP-P4

SSD FUNC_TEST

1385	TP_NAND0_S5E0_ANI0_VREF	TRUE	112 143
1386	TP_NAND0_S5E0_ANI1_VREF	TRUE	112 143
1387	TP_NAND0_S5E1_ANI0_VREF	TRUE	113 143
1388	TP_NAND0_S5E1_ANI1_VREF	TRUE	113 143
1389	TP_NAND0_S5E2_ANI0_VREF	TRUE	114 143
1390	TP_NAND0_S5E2_ANI1_VREF	TRUE	114 143
1391	TP_NAND0_S5E3_ANI0_VREF	TRUE	115 143
1392	TP_NAND0_S5E3_ANI1_VREF	TRUE	115 143
1393	TP_NAND1_S5E0_ANI0_VREF	TRUE	117 143
1394	TP_NAND1_S5E0_ANI1_VREF	TRUE	117 143
1395	TP_NAND1_S5E1_ANI0_VREF	TRUE	118 143
1396	TP_NAND1_S5E1_ANI1_VREF	TRUE	118 143
1397	TP_NAND1_S5E2_ANI0_VREF	TRUE	119 143
1398	TP_NAND1_S5E2_ANI1_VREF	TRUE	119 143
1399	TP_NAND1_S5E3_ANI0_VREF	TRUE	120 143
1400	TP_NAND1_S5E3_ANI1_VREF	TRUE	120 143

1413	FTCAM_RESET_L	TRUE	7 123
TP-P4 1455	ATCRTMR0_RESET_1V2_1V8_MCW_L	TRUE	158
1457	UPC0_SER_DBG	TRUE	82 84
1461	UPC1_SER_DBG	TRUE	82 85
1462	UPC2_SER_DBG	TRUE	91 93
1458	SPI_UPC0_R_CLK	TRUE	82 84
1459	UPC_PMU_RESET_1V2	TRUE	46 145 147 149 155
155 149 147 145 46	UPC_PMU_RESET_1V2	BOTTOM 1 TP	TPU6800 TP-P4
1458	EDP_BKLT_1V29_EN	TRUE	38 126 145
1457	IPD_PWR_EN	TRUE	38 137 140 145
153 146 144 4N	PPVDD_SOC_S1	1 PP	PPU8B1 P3MM

TP for PPVDDH_S1_CLVR

Removed 0.9mm TPs per DC-DC
and to extend the soldermask
opening for C990C and C990D on PCB.

MISC FUNC_TEST

1616	P3V8AON_LPM	TRUE	34 38 145
1618	PP3V3_S2_FAN_LS	TRUE	76
1617	PDM_DMIC_CLK6_1V8	TRUE	135
1616	PP1V2_AON_FPMU	TRUE	40
1615	PP1V2_S2SW_CLVR_VDDIO	TRUE	153
1614	PP1V8_S2SW_CLVR_VDDC1	TRUE	153
1613	PP1V8_S2SW_SNS	TRUE	145 150
1612	PPVDD_ECPU_SRAM_AWAKESW	TRUE	143 153
1611	PPVDD_VCP_FPMU	TRUE	40
1610	PPVDD_VCP_LPMU	TRUE	44
1620	PP0V8_S2SW_CLVR_VDDDIG	TRUE	153
1621	IPD_SYS_AWAKE_CONN	TRUE	139 140
1436	SPI_GYRO_CS_L	TRUE	10 75

DCDC Debug 3mm PP

143 32 31 USBC5_CC1 BOTTOM 1 PP PPU5

1488	DP2HDMI_PWR_EN	TRUE	46 102 103
1492	HDMI_PWR_EN	TRUE	46 99
1490	DP2HDMI_RESET_L	TRUE	46 102
1489	SPI_DP2HDMI_CS_L	TRUE	101
1493	HDMI_CEC_AOP_RX	TRUE	10 102
1494	HDMI_CEC_AOP_TX	TRUE	10 102
1433	HDMI_CEC	TRUE	99 101 102
1434	IPD_TOUCH_RESET_L	TRUE	42 139
1435	SPI_IPD_TOUCH_CS_CONN_L	TRUE	139 140
1495	LPMU_3V8_ISENSE	TRUE	68 74 145
1497	FPMU_3V8_ISENSE	TRUE	68 74 145
1498	BMON_ISENSE	TRUE	67 74 145
1631	CHGR_PMU_SHDN	TRUE	28 38
1632	IPD_MCU_INT_L	TRUE	6 139

MLB_C Specific TP-PPs

PPU813	PP	1	VDDHVR_ILIMIT_L	5 50
PPU828	PP	1	SPMI_VDDHVR_DATA	12 50
PPU829	PP	1	SPMI_VDDHVR_CLK	12 50
PPU8A5 P3MM	PP	1	DBL_CLICK_DET	6 46 145
PPU8A6 P3MM	PP	1	P5VS2HOLD_PWR_EN	38 46 144
PPU8A8 P3MM	PP	1	P5VS2HOLD_PGOOD	37 62 145 156
PPU8B0 P3MM	PP	1	IPD_PWR_EN	38 137 140 145
PPU8B2 P3MM	PP	1	FPMU_CRASH0_L	38 42
PPU8B5 P3MM	PP	1	CLVR_RESET_L	46 56 57 58 59 60 145
TP-P4 TPU66D2	TP	1	P3V8AON_LPM	34 38 145

TOP

PPU8B9 P3MM	PP	1	FPMU_CRASH1_L	38 42
PPU8C1 P3MM	PP	1	CLVR_CRASH_L	38 56 57 58 59 60
PPU8C4 P3MM	PP	1	EDP_BKLT_1V29_EN	38 126 145
PPU8C5 P3MM	PP	1	UPC_PMU_RESET_1V2	46 145 147 149 155
PPU850 P3MM	PP	1	LP5_IN_RESET_L	5 46

FUNC_TEST

1600	VDDHVR_SCRASH_L	TRUE	38 50	
TPU8A7 TP-P4	TP	1	P5VS2HOLD_PWR_EN	TRUE 38 62 103

PLACE_SIDE=TOP

SoC TP Nets

6	TP_AP_GPIO37	BOTTOM 1	TP	TPU880 TP-P4
6	TP_AP_GPIO38	BOTTOM 1	TP	TPU881 TP-P4
6	TP_AP_I2C05_SCL	BOTTOM 1	TP	TPU883 TP-P4
6	TP_AP_I2C05_SDA	BOTTOM 1	TP	TPU884 TP-P4
6	TP_MTP_I2C0_SCL	BOTTOM 1	TP	TPU885 TP-P4
6	TP_MTP_I2C0_SDA	BOTTOM 1	TP	TPU886 TP-P4
156	IPD_MTP_FUNC_1	BOTTOM 1	TP	TPU887 TP-P4
145 10	TP_AON_SLEEP1_RESET_L	BOTTOM 1	TP	TPU894 TP-P4
10	TP_AOP_LEAP_MADI_IN	BOTTOM 1	TP	TPU895 TP-P4
10	TP_AOP_LEAP_MADI_OUT	BOTTOM 1	TP	TPU896 TP-P4

MISC FUNC_TEST

1622	PP2V5_VREF_P3V8AONILIMIT	TRUE	37
1624	PP1V5_LDOINT_FPMU	TRUE	40
1625	PP1V5_LDOINT_LPMU	TRUE	44
1626	PP1V8_AWAKE_SEPROM	TRUE	11
1627	PPCHGR_VDDA	TRUE	28 29 30
1628	PP5V_AON_P3V8AON	TRUE	34 150

SMC ISENSE

145 74 68 1634	LPMU_3V8_ISENSE	PLACE_NEAR=CD601.1:3MM TOP 1 TP		TPU7H0 TP-P4
	GND	PLACE_NEAR=CD601.2:3MM TOP 1 TP		TPU7H1 TP-P4
145 74 68 1632	FPMU_3V8_ISENSE	PLACE_NEAR=CD631.1:3MM TOP 1 TP		TPU7H2 TP-P4
	GND	PLACE_NEAR=CD631.2:3MM TOP 1 TP		TPU7H3 TP-P4
74 67 1628	P1V8VDDH_HS_ISENSE	PLACE_NEAR=CD582.1:3MM TOP 1 TP		TPU7H4 TP-P4
	GND	PLACE_NEAR=CD582.2:3MM TOP 1 TP		TPU7H5 TP-P4
145 74 67 1627	BMON_ISENSE	PLACE_NEAR=CD580.1:3MM TOP 1 TP		TPU7H6 TP-P4
	GND	PLACE_NEAR=CD580.2:3MM TOP 1 TP		TPU7H7 TP-P4

PAGE TITLE

FCT 3 and PMU TPs

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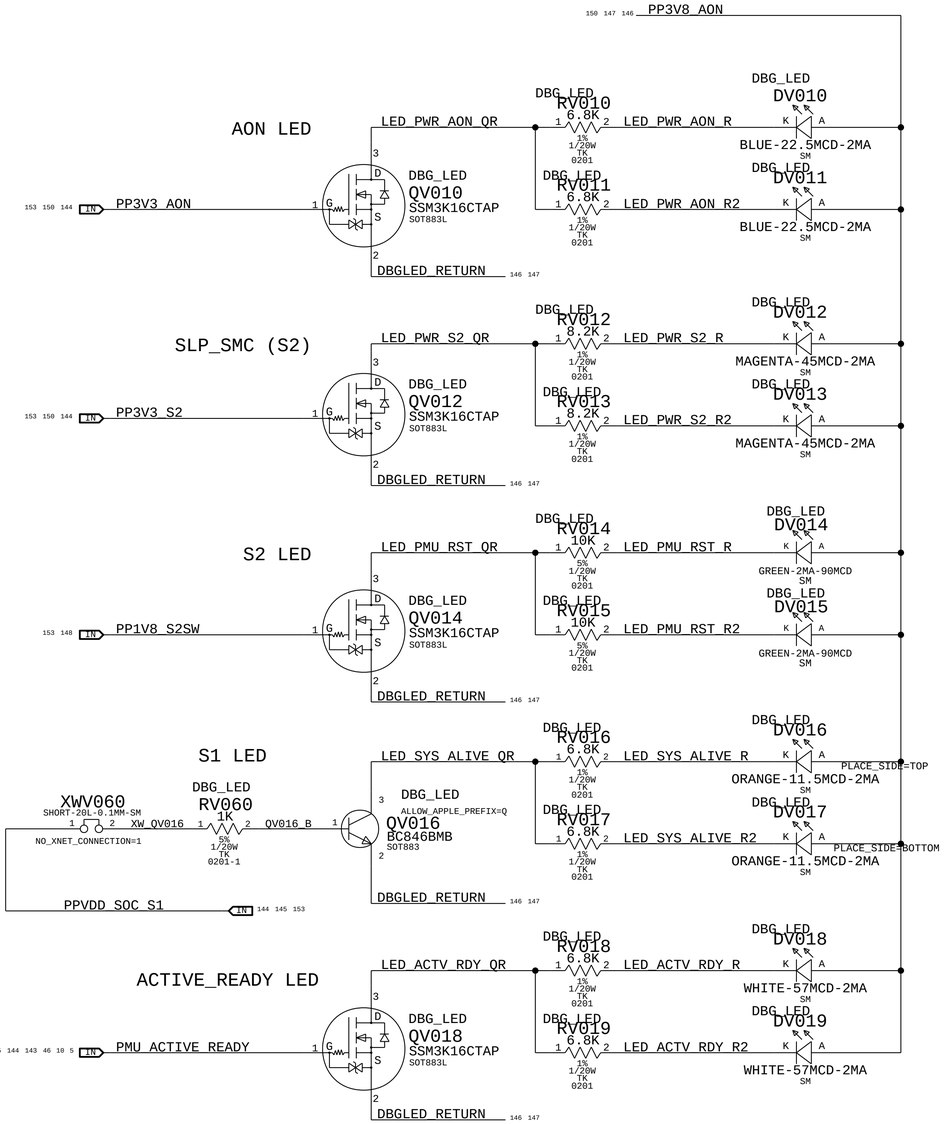
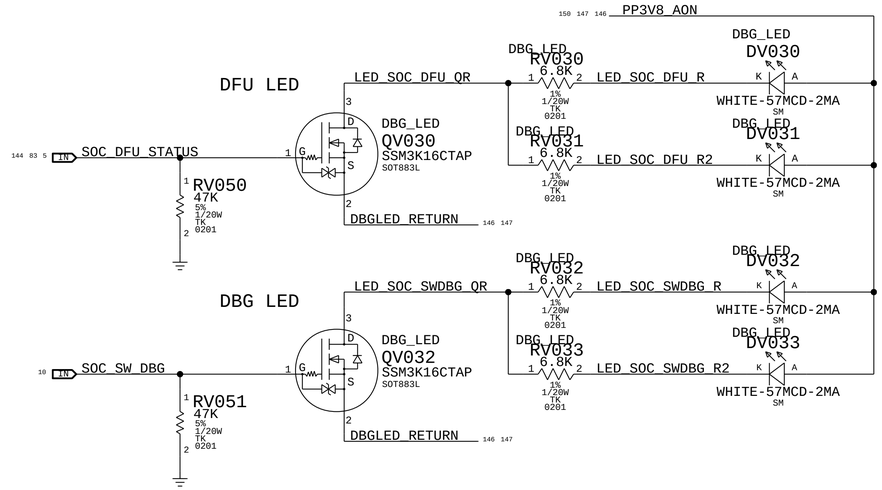
Debug LEDs





BOM_COST_GROUP=DEBUG

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	Apple Inc.
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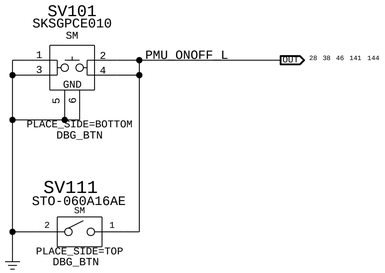
POWER BUTTON

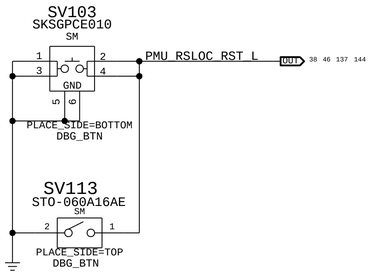
Imitate a user-facing Power Button press, many functions:
- Press to Wake from any state
- Combine with RSLOC (see RSLOC)
- Hold for 8sec to trigger "one-finger reset"
- - Similar to PMU RESET, except SW gets a warning to initiate panic-flow



RSLOC BUTTON

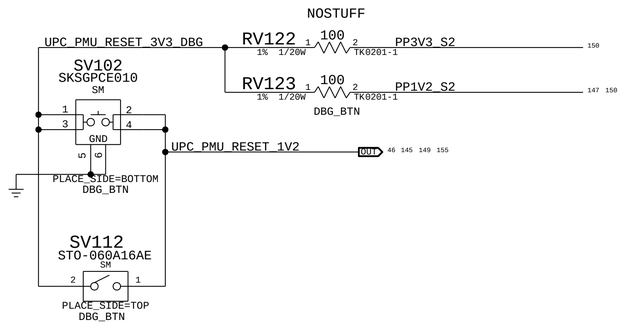
Imitate a user-facing key combo Right-Shift + Left-Option + Control:
- Hold RSLOC 4sec, then press Power Button to initiate PMU RESET
- Hold RSLOC 4sec, then hold Power Button 4sec to power-cycle P3V8AON VR
- Hold Power Button 1sec, then hold RSLOC 10sec which will trigger PMU RESET, then release RSLOC while continue to hold power button for 6 Sec. Board will boot into DFU during the final 6 Sec hold.

(continue holding first button when second button is added)



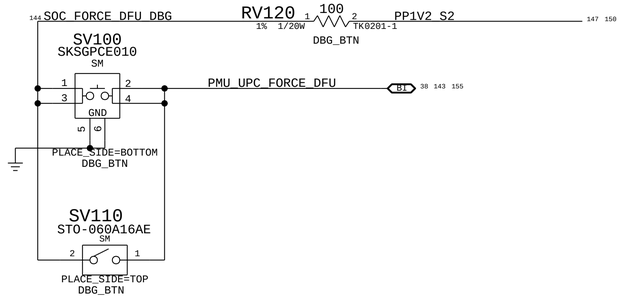
PMU RESET

PMU transitions to OFF and automatically proceeds up to AWAKE



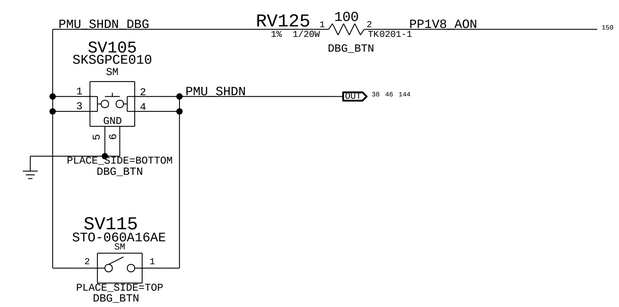
FORCE DFU

Hold during OFF->AWAKE transition to enter SOC's "Debug Firmware Update" mode



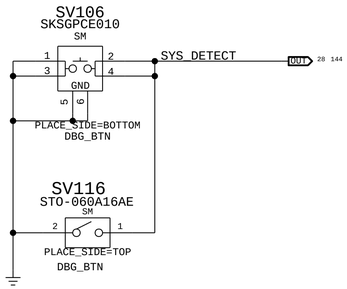
PMU SHUTDOWN

PMU transitions to OFF state and waits for a WAKE source*



SYS_DETECT (Battery Disconnect)

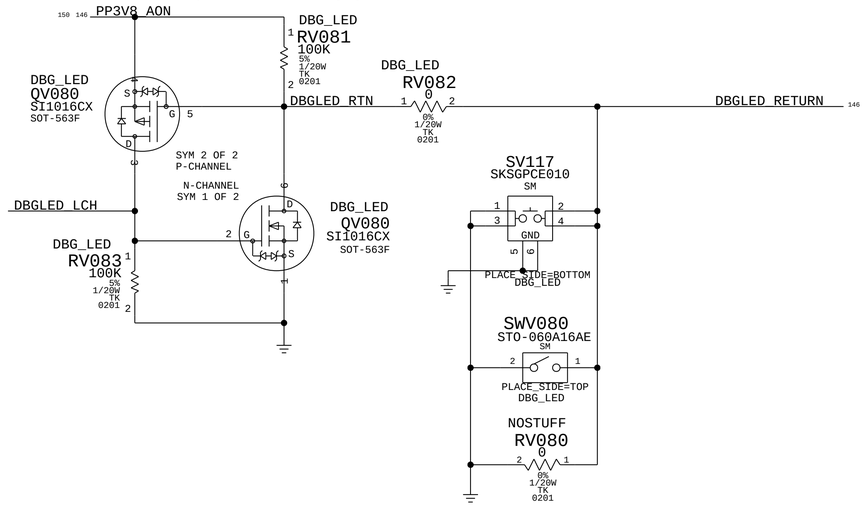
Imitate unplugging the battery signal flex, to disconnect MLB from Battery power
- Disconnect all DCIN sources, then hold SYS_DETECT for 2sec. MLB will completely power down



Debug LED Latch

Press button once to engage.
Remove power to disengage.

Debug LED Enable



*WAKE sources in OFF:
CHGR_AUX_OK (DCIN present)
IPD_LID_OPEN_1V8 (Lid is open)
PMU_ONOFF_L (User Power Button)

BOM_COST_GROUP=DEBUG

PAGE TITLE: Debug: Buttons

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Desense caps

151 127 PPBUS_AON_LUXE
- CW120 1 | 2 12PF 25V NP0-C0G 5% 0201
- CW122 1 | 2 12PF 25V NP0-C0G 5% 0201
- CW125 1 | 2 1.8PF 25V C0G +/-0.1PF 201
- CW127 1 | 2 3.0PF 25V NP0-C0G +/-0.1PF 0201

127 PPVOUT_LUXE_XW
- CW110 1 | 2 12PF 25V NP0-C0G 5% 0201
- CW111 1 | 2 12PF 25V NP0-C0G 5% 0201
- CW117 1 | 2 12PF 25V NP0-C0G 5% 0201
- CW113 1 | 2 1.8PF 25V C0G +/-0.1PF 201
- CW115 1 | 2 12PF 25V NP0-C0G 5% 0201
- CW118 1 | 2 3.0PF 25V NP0-C0G +/-0.1PF 0201
- CW225 1 | 2 1.8PF 25V C0G +/-0.1PF 201

144 127 PPLUXE_LX1
- CW112 1 | 2 12PF 25V NP0-C0G 5% 0201 NOSTUFF
- CW123 1 | 2 3.0PF 25V NP0-C0G +/-0.1PF 0201 NOSTUFF
- CW227 1 | 2 1.8PF 25V C0G +/-0.1PF 201 NOSTUFF

144 127 PPLUXE_LX2
- CW114 1 | 2 12PF 25V NP0-C0G 5% 0201 NOSTUFF
- CW228 1 | 2 3.0PF 25V NP0-C0G +/-0.1PF 0201 NOSTUFF
- CW229 1 | 2 1.8PF 25V C0G +/-0.1PF 201 NOSTUFF

144 127 PPLUXE_INPUT_R_V
- CW116 1 | 2 12PF 25V NP0-C0G 5% 0201
- CW119 1 | 2 1.8PF 25V C0G +/-0.1PF 201
- CW128 1 | 2 3.0PF 25V NP0-C0G +/-0.1PF 0201

151 110 PP3V8_AON_WLBT
- CW1A2 1 | 2 1.8PF 25V C0G +/-0.1PF 201
- CW1A3 1 | 2 1.8PF 25V C0G +/-0.1PF 201
- CW1A4 1 | 2 1.8PF 25V C0G +/-0.1PF 201
- CW1A5 1 | 2 1.8PF 25V C0G +/-0.1PF 201

150 110 PP1V8_S2
- CW1A6 1 | 2 1.8PF 25V C0G +/-0.1PF 201
- CW1A7 1 | 2 1.8PF 25V C0G +/-0.1PF 201

144 17 PP1V8_S2SW_VDD1
- CW166 1 | 2 1.8PF 25V C0G +/-0.1PF 201
- CW167 1 | 2 3.0PF 25V NP0-C0G +/-0.1PF 0201
- CW168 1 | 2 12PF 25V NP0-C0G 5% 0201

151 148 35 34 PPVIN_P3V8AON
- CW150 1 | 2 12PF 25V NP0-C0G 5% 0201
- CW151 1 | 2 12PF 25V NP0-C0G 5% 0201
- CW152 1 | 2 12PF 25V NP0-C0G 5% 0201
- CW153 1 | 2 12PF 25V NP0-C0G 5% 0201
- CW154 1 | 2 1.8PF 25V C0G +/-0.1PF 201
- CW155 1 | 2 3.0PF 25V NP0-C0G +/-0.1PF 0201
- CW156 1 | 2 12PF 25V NP0-C0G 5% 0201
- CW157 1 | 2 3.0PF 25V NP0-C0G +/-0.1PF 0201
- CW158 1 | 2 1.8PF 25V C0G +/-0.1PF 201
- CW159 1 | 2 3.0PF 25V NP0-C0G +/-0.1PF 0201
- CW140 1 | 2 1.8PF 25V C0G +/-0.1PF 201
- CW235 1 | 2 1.8PF 25V C0G +/-0.1PF 201
- CW236 1 | 2 1.8PF 25V C0G +/-0.1PF 201

150 148 35 PP3V8_AON
- CW144 1 | 2 1.8PF 25V C0G +/-0.1PF 201
- CW145 1 | 2 12PF 25V NP0-C0G 5% 0201
- CW146 1 | 2 12PF 25V NP0-C0G 5% 0201
- CW147 1 | 2 1.8PF 25V C0G +/-0.1PF 201
- CW148 1 | 2 1.8PF 25V C0G +/-0.1PF 201
- CW149 1 | 2 12PF 25V NP0-C0G 5% 0201
- CW143 1 | 2 3.0PF 25V NP0-C0G +/-0.1PF 0201

153 146 PP1V8_S2SW
- CW139 1 | 2 1.8PF 25V C0G +/-0.1PF 201
- CW141 1 | 2 12PF 25V NP0-C0G 5% 0201
- CW142 1 | 2 3.0PF 25V NP0-C0G +/-0.1PF 0201

148 35 P3V8AON_VSW1
- CW160 1 | 2 12PF 25V NP0-C0G 5% 0201

35 34 P3V8AON_SW2
- CW161 1 | 2 12PF 25V NP0-C0G 5% 0201

148 35 34 P3V8AON_SW3
- CW162 1 | 2 12PF 25V NP0-C0G 5% 0201

ICEMAN PHASE1 GATE DRIVER desense caps

35 34 P3V8AON_DRVH1
- CW173 1 | 2 3.0PF 25V NP0-C0G +/-0.1PF 0201 131S0198
- CW174 1 | 2 1.8PF 25V C0G +/-0.1PF 201

151 144 PPVOUT_KBDLED_CONN
- CW232 1 | 2 12PF 100V C0G 5% 0201 NOSTUFF
- CW233 1 | 2 3PF 100V C0G +/-0.1PF 0201 NOSTUFF
- CW234 1 | 2 1.8PF 100V C0G +/-0.1PF 0201 NOSTUFF
- CW238 1 | 2 12PF 100V C0G 5% 0201 NOSTUFF
- CW239 1 | 2 3PF 100V C0G +/-0.1PF 0201 NOSTUFF
- CW240 1 | 2 1.8PF 100V C0G +/-0.1PF 0201 NOSTUFF

151 PPVIN_P5VS2
- CW180 1 | 2 12PF 25V NP0-C0G 5% 0201
- CW181 1 | 2 3.0PF 25V NP0-C0G +/-0.1PF 0201
- CW184 1 | 2 1.8PF 25V C0G +/-0.1PF 201

159 150 144 PP5V_S2_HOLD
- CW182 1 | 2 12PF 25V NP0-C0G 5% 0201
- CW183 1 | 2 3.0PF 25V NP0-C0G +/-0.1PF 0201
- CW185 1 | 2 1.8PF 25V C0G +/-0.1PF 201

151 121 PPBUS_NAND1
- CW130 1 | 2 12PF 25V NP0-C0G 5% 0201
- CW178 1 | 2 3.0PF 25V NP0-C0G +/-0.1PF 0201
- CW179 1 | 2 1.8PF 25V C0G +/-0.1PF 201

151 116 PPBUS_NAND0
- CW131 1 | 2 12PF 25V NP0-C0G 5% 0201
- CW132 1 | 2 3.0PF 25V NP0-C0G +/-0.1PF 0201
- CW133 1 | 2 1.8PF 25V C0G +/-0.1PF 201

144 136 KBDBKLT_SW2
- CW134 1 | 2 1.8PF 100V C0G +/-0.1PF 0201 NOSTUFF

153 21 10 PP1V2_S2
- CW190 1 | 2 1.8PF 25V C0G +/-0.1PF 201
- CW191 1 | 2 12PF 25V NP0-C0G 5% 0201
- CW192 1 | 2 3.0PF 25V NP0-C0G +/-0.1PF 0201

153 43 41 39 PPVDD_CIO_S2SW
- CW193 1 | 2 1.8PF 25V C0G +/-0.1PF 201
- CW194 1 | 2 12PF 25V NP0-C0G 5% 0201
- CW195 1 | 2 3.0PF 25V NP0-C0G +/-0.1PF 0201

153 47 45 39 PPVDD_SRAM_S1
- CW196 1 | 2 1.8PF 25V C0G +/-0.1PF 201 131S0198
- CW197 1 | 2 12PF 25V NP0-C0G 5% 0201
- CW198 1 | 2 3.0PF 25V NP0-C0G +/-0.1PF 0201

35 34 P3V8AON_DRVL1
- CW170 1 | 2 12PF 25V NP0-C0G 5% 0201 131S0445
- CW175 1 | 2 3.0PF 25V NP0-C0G +/-0.1PF 0201 131S0198
- CW176 1 | 2 1.8PF 25V C0G +/-0.1PF 201

PP5V_S2_HDMI Desense

150 103 99 PP5V_S2_HDMI
- CW230 1 | 2 3.0PF 25V NP0-C0G +/-0.1PF 0201 131S0198
- CW231 1 | 2 1.8PF 25V C0G +/-0.1PF 201

rdar://92307078 add Desense caps to SPI_TPAD

139 SPI_IPD_MOSI_CONN_R
- CW135 1 | 2 12PF 25V NP0-C0G 5% 0201 131S0445

144 140 139 SPI_IPD_MISO_CONN
- CW136 1 | 2 12PF 25V NP0-C0G 5% 0201 131S0445

139 SPI_IPD_CLK_CONN_R
- CW137 1 | 2 12PF 25V NP0-C0G 5% 0201 131S0445

139 13 SPI_IPD_CLK
- CW163 1 | 2 12PF 25V NP0-C0G 5% 0201 NOSTUFF 131S0445

139 13 SPI_IPD_MOSI
- CW164 1 | 2 12PF 25V NP0-C0G 5% 0201 NOSTUFF 131S0445

139 SPI_IPD_MISO_R
- CW165 1 | 2 12PF 25V NP0-C0G 5% 0201 NOSTUFF 131S0445

Added new DESENSE caps on 9/202022 per DESENSE comments

150 148 35 PP3V8_AON
- CW200 1 | 2 3.0PF 25V NP0-C0G +/-0.1PF 0201
- CW201 1 | 2 3.0PF 25V NP0-C0G +/-0.1PF 0201
- CW203 1 | 2 12PF 25V NP0-C0G 5% 0201
- CW204 1 | 2 3.0PF 25V NP0-C0G +/-0.1PF 0201
- CW205 1 | 2 1.8PF 25V C0G +/-0.1PF 201
- CW206 1 | 2 12PF 25V NP0-C0G 5% 0201
- CW207 1 | 2 3.0PF 25V NP0-C0G +/-0.1PF 0201
- CW208 1 | 2 1.8PF 25V C0G +/-0.1PF 201
- CW209 1 | 2 12PF 25V NP0-C0G 5% 0201
- CW210 1 | 2 1.8PF 25V C0G +/-0.1PF 201
- CW211 1 | 2 3.0PF 25V NP0-C0G +/-0.1PF 0201

151 148 35 34 PPVIN_P3V8AON
- CW212 1 | 2 3.0PF 25V NP0-C0G +/-0.1PF 0201
- CW213 1 | 2 3.0PF 25V NP0-C0G +/-0.1PF 0201
- CW214 1 | 2 1.8PF 25V C0G +/-0.1PF 201
- CW215 1 | 2 12PF 25V NP0-C0G 5% 0201
- CW216 1 | 2 3.0PF 25V NP0-C0G +/-0.1PF 0201
- CW217 1 | 2 1.8PF 25V C0G +/-0.1PF 201
- CW218 1 | 2 12PF 25V NP0-C0G 5% 0201
- CW219 1 | 2 3.0PF 25V NP0-C0G +/-0.1PF 0201

148 35 34 P3V8AON_SW3
- CW220 1 | 2 3.0PF 25V NP0-C0G +/-0.1PF 0201
- CW221 1 | 2 1.8PF 25V C0G +/-0.1PF 201

148 35 P3V8AON_VSW1
- CW223 1 | 2 3.0PF 25V NP0-C0G +/-0.1PF 0201
- CW224 1 | 2 1.8PF 25V C0G +/-0.1PF 201

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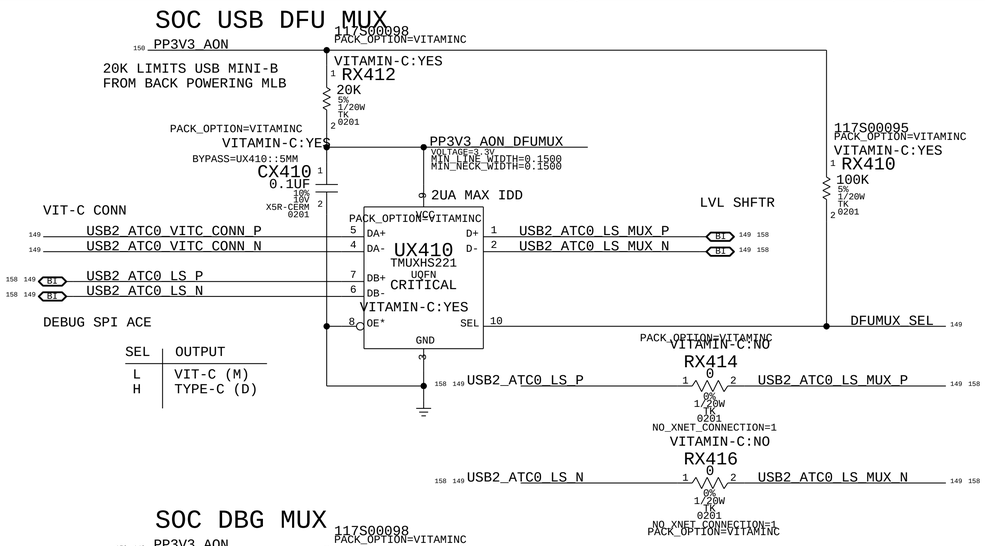

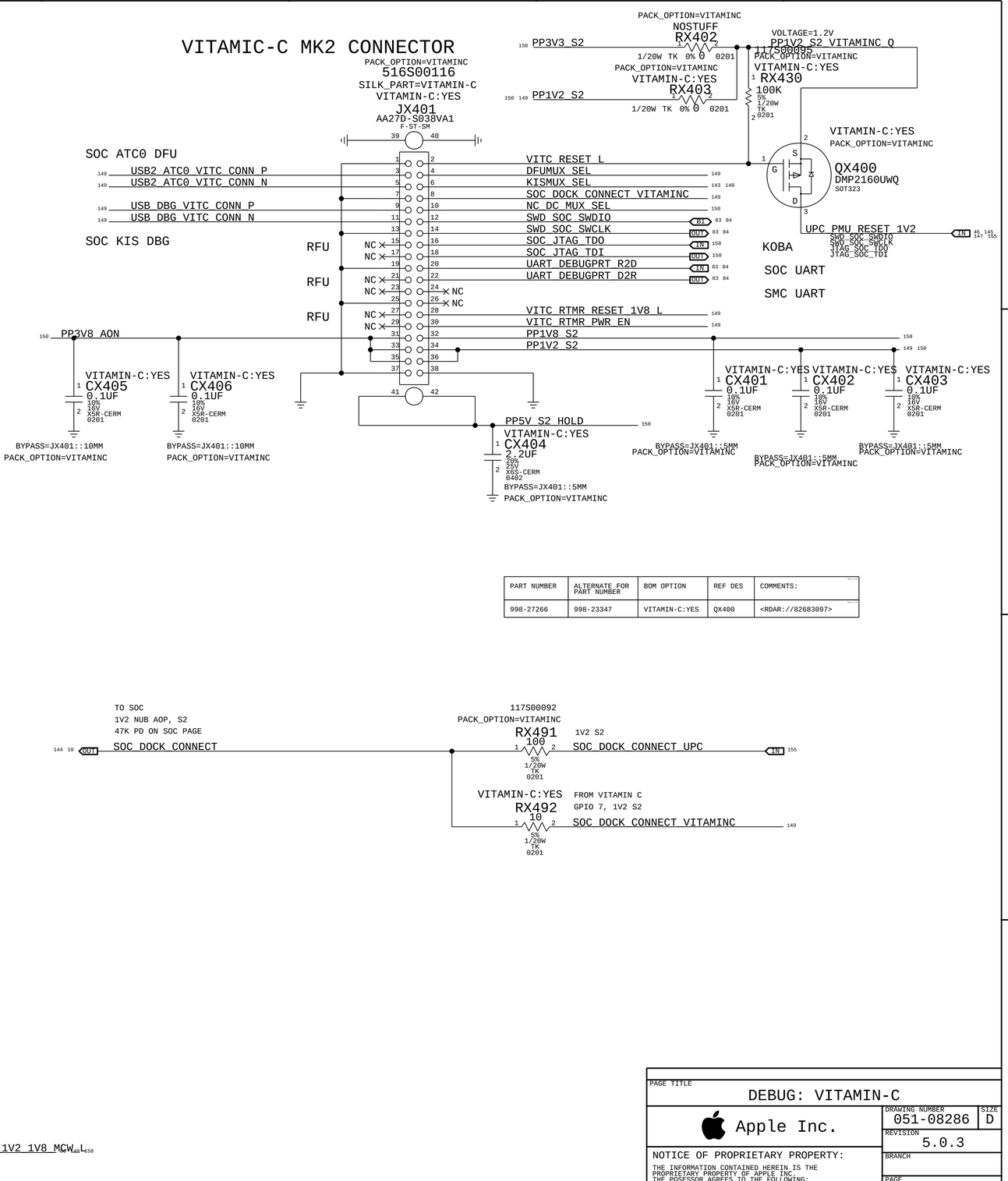

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
998-27266	998-23347	VITAMIN-C:YES	QX400	<RDAR://82683097>

BOM_COST_GROUP=DEBUG

PAGE TITLE
DEBUG: VITAMIN-C

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VBAT

PPVBAT_AON
- PPVBAT_AON — MAKE_BASE=TRUE, MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000 — 144
- PPVBAT_AON — 28 29

DCIN

82 PPDCIN_AON
91 PPDCIN_AON
33 PPDCIN_AON
- PPDCIN_AON — MAKE_BASE=TRUE, MIN_LINE_WIDTH=0.2500, MIN_NECK_WIDTH=0.1500 — 144
- PPDCIN_AON — 28 29
- PPDCIN_AON — 67

PBUS

144 29 PPBUS_AON
- PPBUS_AON — MAKE_BASE=TRUE, MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, VOLTAGE=13.5V — 63 144
- PPBUS_AON — 44
- PPBUS_AON
- PPBUS_AON — 67
- PPBUS_AON — 68
- PPBUS_AON — 68
- PPBUS_AON — 68
- PPBUS_AON — 68
- PPBUS_AON — 69
- PPBUS_AON — 69
- PPBUS_AON — 67
- PPBUS_AON — 67
- PPBUS_AON — 69
- PPBUS_AON — 69
- PPBUS_AON — 140
- PPBUS_AON — 76
- PPBUS_AON — 37
- PPBUS_AON
- PPBUS_AON
- PPBUS_AON
- PPBUS_AON — 67

ICEMAN VMAIN

148 35 PP3V8_AON
17 PP3V8_AON
89 PP3V8_AON
97 PP3V8_AON
PP3V8_AON
- PP3V8_AON — MAKE_BASE=TRUE, MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000 — 144 159
- PP3V8_AON
- PP3V8_AON — 68
- PP3V8_AON — 68
- PP3V8_AON — 70
- PP3V8_AON — 70
- PP3V8_AON — 70
- PP3V8_AON — 70
- PP3V8_AON — 131
- PP3V8_AON — 132
- PP3V8_AON — 132
- PP3V8_AON — 133
- PP3V8_AON — 133
- PP3V8_AON — 133
- PP3V8_AON — 69
- PP3V8_AON
- PP3V8_AON — 71
- PP3V8_AON — 103
- PP3V8_AON
- PP3V8_AON
- PP3V8_AON — 126
- PP3V8_AON — 71
- PP3V8_AON — 28
- PP3V8_AON — 146 147
- PP3V8_AON — 149
- PP3V8_AON — 37 72
- PP3V8_AON — 62
- PP3V8_AON — 103
- PP3V8_AON — 88
- PP3V8_AON
- PP3V8_AON
- PP3V8_AON
- PP3V8_AON
- PP3V8_AON

153 47 45 39 PPVDD_ECPU_AWAKESW — PPVDD_ECPU_AWAKESW — MAKE_BASE=TRUE
153 45 PPVDD_ECPU_AWAKESW — PPVDD_ECPU_AWAKESW — MAKE_BASE=TRUE
157 153 GND — GND — MAKE_BASE=TRUE

PP1V2 AWAKE SYSTEM LOADS

153 144 PP1V2_AWAKE — MAKE_BASE=TRUE
- PP1V2_AWAKE — 108
- PP1V2_AWAKE — 127
- PP1V2_AWAKE — 131
- PP1V2_AWAKE — 131 132
- PP1V2_AWAKE — 132 133
- PP1V2_AWAKE — 64
- PP1V2_AWAKE — 66
- PP1V2_AWAKE — 125
- PP1V2_AWAKE — 108

PP1V2 S2 SYSTEM LOADS

159 153 144 PP1V2_S2 — MAKE_BASE=TRUE
- PP1V2_S2 — 30
- PP1V2_S2 — 32 33
- PP1V2_S2
- PP1V2_S2 — 64 65 66
- PP1V2_S2 — 80 81 82 84 85 87 88
130 123 PP1V2_S2
- PP1V2_S2
- PP1V2_S2
- PP1V2_S2 — 90 91 93 104
- PP1V2_S2
86 PP1V2_S2
86 PP1V2_S2
94 PP1V2_S2
PP1V2_S2
PP1V2_S2
103 PP1V2_S2
75 PP1V2_S2
PP1V2_S2
PP1V2_S2
PP1V2_S2
PP1V2_S2
27 PP1V2_S2
- PP1V2_S2 — 110
- PP1V2_S2
- PP1V2_S2 — 135
- PP1V2_S2 — 136
- PP1V2_S2
- PP1V2_S2 — 139
- PP1V2_S2 — 102
- PP1V2_S2 — 147
- PP1V2_S2
- PP1V2_S2 — 131
- PP1V2_S2 — 76
- PP1V2_S2 — 14
- PP1V2_S2 — 141
- PP1V2_S2 — 142
- PP1V2_S2 — 149
- PP1V2_S2

FPMU 1V8 S2 SYSTEM LOADS

153 144 PP1V8_S2 — MAKE_BASE=TRUE
- PP1V8_S2 — 40
- PP1V8_S2
- PP1V8_S2 — 29 30
- PP1V8_S2
- PP1V8_S2
- PP1V8_S2 — 84 85 88
94 PP1V8_S2
- PP1V8_S2 — 86
- PP1V8_S2 — 86
- PP1V8_S2 — 110 148
- PP1V8_S2 — 116
- PP1V8_S2 — 121
- PP1V8_S2 — 125
- PP1V8_S2 — 135
- PP1V8_S2 — 135
- PP1V8_S2 — 14
- PP1V8_S2 — 75
- PP1V8_S2
- PP1V8_S2 — 64 65 66
93 PP1V8_S2
- PP1V8_S2 — 96
- PP1V8_S2 — 40
- PP1V8_S2 — 104
- PP1V8_S2
- PP1V8_S2 — 149
- PP1V8_S2 — 66
123 PP1V8_S2
PP1V8_S2
- PP1V8_S2 — 27

S2 SYSTEM LOADS

153 146 144 PP3V3_S2 — MAKE_BASE=TRUE
- PP3V3_S2 — 76
- PP3V3_S2 — 108
- PP3V3_S2 — 136
PP3V3_S2
- PP3V3_S2 — 102
- PP3V3_S2 — 147
- PP3V3_S2
- PP3V3_S2
150 86 PP3V3_S2
150 86 PP3V3_S2
150 94 PP3V3_S2
- PP3V3_S2
PP3V3_S2
- PP3V3_S2 — 149
86 PP3V3_S2
- PP3V3_S2 — 84 85 87 88
- PP3V3_S2 — 93
- PP3V3_S2 — 32
- PP3V3_S2 — 87
- PP3V3_S2 — 95
- PP3V3_S2 — 94 150
- PP3V3_S2 — 86 150
- PP3V3_S2 — 86 150
- PP3V3_S2
- PP3V3_S2 — 104

PP5V_S2

62 PP5V_S2_HOLD — MAKE_BASE=TRUE — 144 148 159
- PP5V_S2_HOLD — 34
- PP5V_S2_HOLD
- PP5V_S2_HOLD
- PP5V_S2_HOLD — 102
- PP5V_S2_HOLD — 127
- PP5V_S2_HOLD — 136 144
- PP5V_S2_HOLD — 136
- PP5V_S2_HOLD — 140
- PP5V_S2_HOLD — 62
- PP5V_S2_HOLD — 37 150
- PP5V_S2_HOLD — 149
- PP5V_S2_HOLD — 76
- PP5V_S2_HOLD — 37 150
- PP5V_S2_HOLD
- PP5V_S2_HOLD
- PP5V_S2_HOLD
- PP5V_S2_HOLD
- PP5V_S2_HOLD — 30
- PP5V_S2_HOLD — 71

40 38 PP1V8_AON_FPMU — MAKE_BASE=TRUE — PP1V8_AON_FPMU — 126
46 44 PP1V8_AON_LPMU — MAKE_BASE=TRUE — PP1V8_AON_LPMU — 28
145 103 PP5V_S2_HDMI — MAKE_BASE=TRUE — VOLTAGE=5V — PP5V_S2_HDMI — 99 103 148

3V3 AON SYSTEM LOADS

153 146 144 PP3V3_AON — MAKE_BASE=TRUE
- PP3V3_AON — 137
- PP3V3_AON
- PP3V3_AON — 129
- PP3V3_AON — 28
- PP3V3_AON — 149
- PP3V3_AON — 149
- PP3V3_AON
- PP3V3_AON

ACE Rails

PP1V8_AON SYSTEM LOADS

159 153 144 PP1V8_AON — MAKE_BASE=TRUE
- PP1V8_AON — 129
- PP1V8_AON — 147
- PP1V8_AON
- PP1V8_AON — 38
- PP1V8_AON
- PP1V8_AON — 130
- PP1V8_AON — 139
- PP1V8_AON — 28
- PP1V8_AON — 139 159
- PP1V8_AON — 14
- PP1V8_AON — 102 103

PP1V8 AWAKE SYSTEM LOADS

153 144 PP1V8_AWAKE — MAKE_BASE=TRUE
- PP1V8_AWAKE — 131
- PP1V8_AWAKE — 132 133
- PP1V8_AWAKE — 66

PP1V2 LPMU LDO3 AWAKE SYSTEM LOADS

40 PP1V2_AWAKESW_BLC — LPMU LDO3
- PP1V2_AWAKESW_BLC — MAKE_BASE=TRUE, MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000 — 128 144
- PP1V2_AWAKESW_BLC — 128

PP1V8 LPMU SW0 S2 SYSTEM LOADS

40 PP1V8_S2SW_SNS — LPMU SW0
- PP1V8_S2SW_SNS — MAKE_BASE=TRUE, MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000 — 145
- PP1V8_S2SW_SNS — 67 68 69 70 71

DISPLAY POWER SEQUENCER OUTPUT

126 PPBCON_AWAKESW_BKLTCONN_VIN
- PPBCON_AWAKESW_BKLTCONN_VIN — MAKE_BASE=TRUE, MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000
- PPBCON_AWAKESW_BKLTCONN_VIN — 71

126 PPMDB_AWAKESW_TCON
- PPMDB_AWAKESW_TCON — MAKE_BASE=TRUE, MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1500 — 144
- PPMDB_AWAKESW_TCON — 70

PP5V_AON_P3V8AON
- PP5V_AON_P3V8AON — MAKE_BASE=TRUE, MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000 — 34 145
- PP5V_AON_P3V8AON

PAGE TITLE: POWER ALIASES 1

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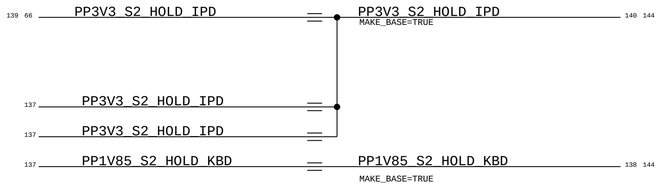
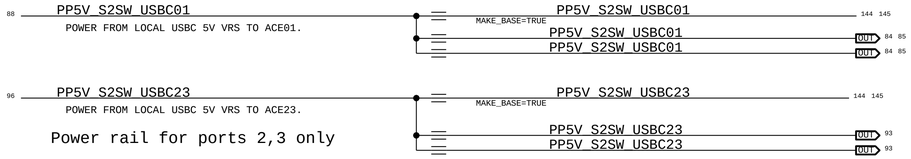
THIS PAGE WILL BE USED FOR SYSTEM / SUBSYSTEM ALIASES

IPD: KEYBOARD / TRACKPAD

PP3V3_S2_IPD (LDO) ALIASES

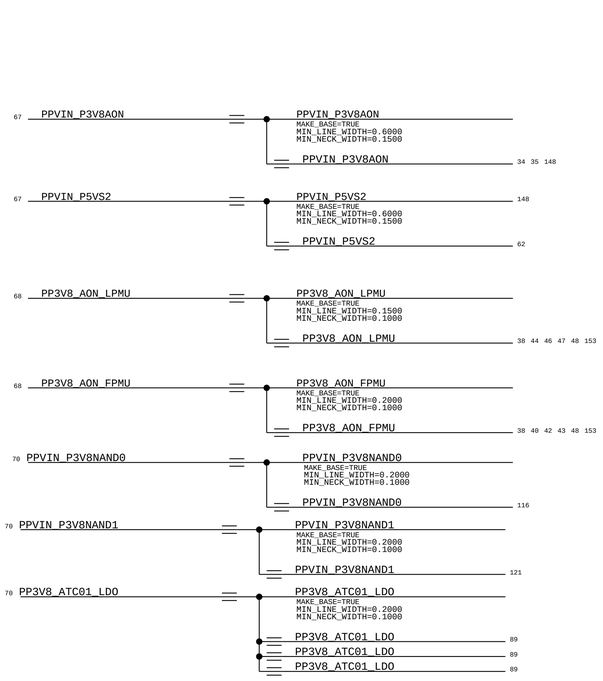


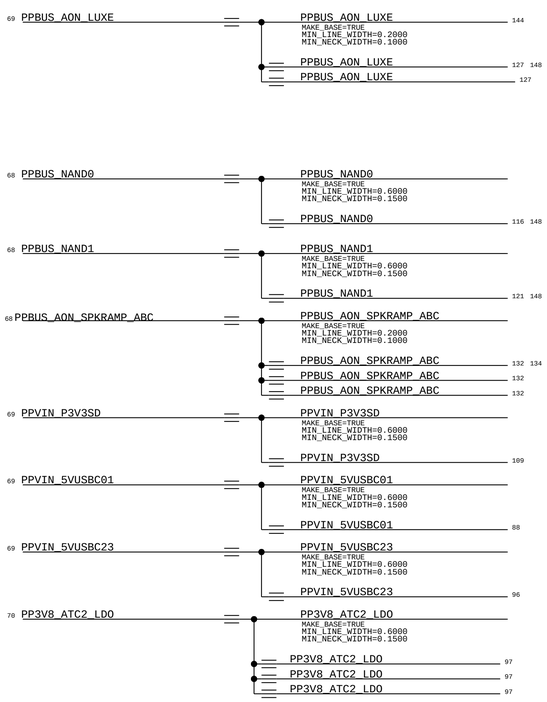


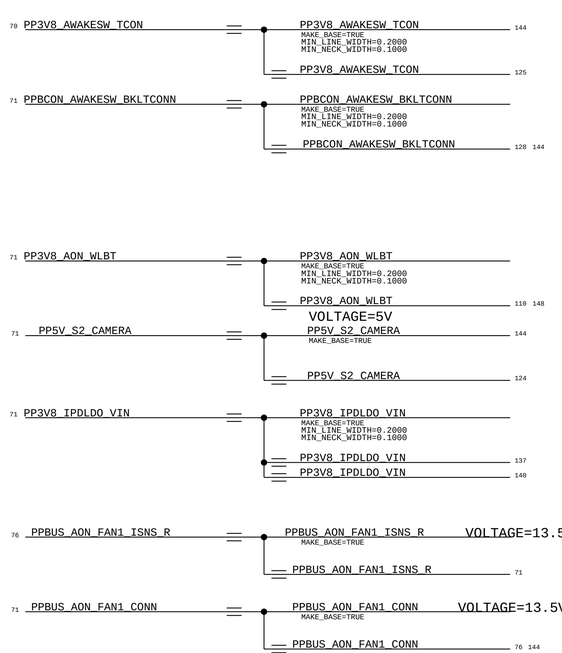
Power rail for ports 2,3 only

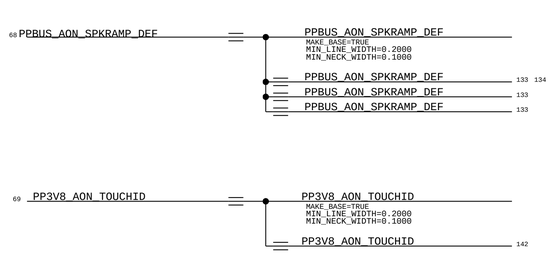
KEYBOARD BACKLIGHT

OUTPUT SENSOR ALIASES









PAGE TITLE

POWER ALIASES 2

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TODO_DT: Update VOLTAGE proporties for H14

CLVR0

61 56 PPVDD_ANE_AWAKESW = PPVDD_ANE_AWAKESW (MAKE_BASE=TRUE)
CLVR0 Buck0/HP0
= PPVDD_ANE_AWAKESW 19

56 PPVDD_ANE_SRAM_AWAKESW = PPVDD_ANE_SRAM_AWAKESW (MAKE_BASE=TRUE) 11
CLVR0 Buck1/LP0
= PPVDD_ANE_SRAM_AWAKESW 19

61 56 PPVDD_PCPU0_AWAKESW = PPVDD_PCPU0_AWAKESW (MAKE_BASE=TRUE)
CLVR0 Buck2/HP1
= PPVDD_PCPU0_AWAKESW 15

56 PPVDD_PCPU_SRAM0_AWAKESW = PPVDD_PCPU_SRAM0_AWAKESW (MAKE_BASE=TRUE)
CLVR0 Buck3/LP1
= PPVDD_PCPU_SRAM0_AWAKESW 15

CLVR1

61 57 PPVDD_GPU2_AWAKESW = PPVDD_GPU2_AWAKESW (MAKE_BASE=TRUE) 11
CLVR1 Buck0/HP0
= PPVDD_GPU2_AWAKESW 15

57 PPVDD_GPU_SRAM2_AWAKESW = PPVDD_GPU_SRAM2_AWAKESW (MAKE_BASE=TRUE) 11
CLVR1 Buck1/LP0
= PPVDD_GPU_SRAM2_AWAKESW 15

61 57 PPVDD_GPU1_AWAKESW = PPVDD_GPU1_AWAKESW (MAKE_BASE=TRUE) 11
CLVR1 Buck2/HP1
= PPVDD_GPU1_AWAKESW 15

57 PPVDD_GPU_SRAM1_AWAKESW = PPVDD_GPU_SRAM1_AWAKESW (MAKE_BASE=TRUE) 11
CLVR1 Buck3/LP1
= PPVDD_GPU_SRAM1_AWAKESW 15

CLVR2

61 58 PPVDD_GPU0_AWAKESW = PPVDD_GPU0_AWAKESW (MAKE_BASE=TRUE)
CLVR2 Buck0/HP0
= PPVDD_GPU0_AWAKESW 15

58 PPVDD_GPU_SRAM0_AWAKESW = PPVDD_GPU_SRAM0_AWAKESW (MAKE_BASE=TRUE) 11
CLVR2 Buck1/LP0
= PPVDD_GPU_SRAM0_AWAKESW 15

61 58 PPVDD_GPU3_AWAKESW = PPVDD_GPU3_AWAKESW (MAKE_BASE=TRUE) 11
CLVR2 Buck2/HP1
= PPVDD_GPU3_AWAKESW 15

58 PPVDD_GPU_SRAM3_AWAKESW = PPVDD_GPU_SRAM3_AWAKESW (MAKE_BASE=TRUE) 11
CLVR2 Buck3/LP1
= PPVDD_GPU_SRAM3_AWAKESW 15

CLVR3

CLVR3 Buck0/HP1: Unused on C platforms

61 59 PPVDD_FABRIC_S1 = PPVDD_FABRIC_S1 (MAKE_BASE=TRUE)
CLVR3 Buck2/HP1
= PPVDD_FABRIC_S1 20

CLVR4

61 60 PPVDD_AFR_CS_S1 = PPVDD_AFR_CS_S1 (MAKE_BASE=TRUE)
CLVR4 Buck0/HP0
= PPVDD_AFR_CS_S1 19

61 60 PPVDD_PCPU1_AWAKESW = PPVDD_PCPU1_AWAKESW (MAKE_BASE=TRUE) 11
CLVR4 Buck2/HP1
= PPVDD_PCPU1_AWAKESW 15

60 PPVDD_PCPU_SRAM1_AWAKESW = PPVDD_PCPU_SRAM1_AWAKESW (MAKE_BASE=TRUE) 11
CLVR4 Buck3/LP1
= PPVDD_PCPU_SRAM1_AWAKESW 15

CLVR0

56 PVDDANE_FB = PVDDANE_FB (MAKE_BASE=TRUE) 19
56 PVDDANESRAM_FB = PVDDANESRAM_FB (MAKE_BASE=TRUE) 19
56 PVDDPCPU0_FB = PVDDPCPU0_FB (MAKE_BASE=TRUE) 15
56 PVDDPCPUSRAM0_FB = PVDDPCPUSRAM0_FB (MAKE_BASE=TRUE) 15

CLVR1

57 PVDDGPU2_FB = PVDDGPU2_FB (MAKE_BASE=TRUE) 15
57 PVDDGPUSRAM2_FB = PVDDGPUSRAM2_FB (MAKE_BASE=TRUE) 15
57 PVDDGPU1_FB = PVDDGPU1_FB (MAKE_BASE=TRUE) 15
57 PVDDGPUSRAM1_FB = PVDDGPUSRAM1_FB (MAKE_BASE=TRUE) 15

CLVR2

58 PVDDGPU0_FB = PVDDGPU0_FB (MAKE_BASE=TRUE) 15
58 PVDDGPUSRAM0_FB = PVDDGPUSRAM0_FB (MAKE_BASE=TRUE) 15
58 PVDDGPU3_FB = PVDDGPU3_FB (MAKE_BASE=TRUE) 15
58 PVDDGPUSRAM3_FB = PVDDGPUSRAM3_FB (MAKE_BASE=TRUE) 15

CLVR3

59 NC_M3_BUCK0_FB = NC_M3_BUCK0_FB (MAKE_BASE=TRUE)
59 PVDDFABRIC_FB = PVDDFABRIC_FB (MAKE_BASE=TRUE) 20

CLVR4

60 PVDDAFRCS_FB = PVDDAFRCS_FB (MAKE_BASE=TRUE) 19
60 PVDDPCPU1_FB = PVDDPCPU1_FB (MAKE_BASE=TRUE) 15
60 PVDDPCPUSRAM1_FB = PVDDPCPUSRAM1_FB (MAKE_BASE=TRUE) 15

72 55 49 PPVDDH_S1_CLVR = PPVDDH_S1_CLVR (MAKE_BASE=TRUE)
VR -> CLVR VDDH
= PPVDDH_S1_CLVR 51
= PPVDDH_S1_CLVR 67
= PPVDDH_S1_CLVR 56 57 58 59 60 61

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POWER ALIASES CLVR

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44 GND
44 NC_LPMU_VLDO0
LPMU LDO0 (Unused)

GND — 150 153 157
NC_LPMU_VLDO0 MAKE_BASE=TRUE

44 PP3V8_AON_LPMU
44 PP3V3_S2
LPMU LDO1

PP3V8_AON_LPMU — 38 44 46 47 48 151 153
PP3V3_S2 — 144 146 150
VOLTAGE=3.3V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
All Loads wired on other pages

44 PP3V8_AON_LPMU
44 PP1V8_S2SW_CLVR_VDDC1
LPMU LDO2
Enabled in SLP_S2R and above
Remains enabled during CLVR-triggered CRASH

PP3V8_AON_LPMU — 38 44 46 47 48 151 153
PP1V8_S2SW_CLVR_VDDC1 — 145
VOLTAGE=1.8V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PP1V8_S2SW_CLVR_VDDC1 — 56 57 58 59 60

44 PP3V8_AON_LPMU
44 PP1V8_AON
LPMU LDO3
Disables momentarily during CRASH

PP3V8_AON_LPMU — 38 44 46 47 48 151 153
PP1V8_AON — 144 150 159
VOLTAGE=1.8V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.1000
MIN_NECK_WIDTH=0.1000
All Loads wired on other pages

44 PP3V8_AON_LPMU
44 PP3V3_AON
LPMU LDO4
Disables momentarily during CRASH

PP3V8_AON_LPMU — 38 44 46 47 48 151 153
PP3V3_AON — 144 146 150
VOLTAGE=3.3V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PP3V3_AON — 44
PP3V3_AON — 40

44 PP1V2_S2
44 PP0V8_S2SW_CLVR_VDDDIG
LPMU LDO5
Enabled in SLP_S2R and above

PP1V2_S2 — 44 46 153
PP0V8_S2SW_CLVR_VDDDIG — 145
VOLTAGE=0.8V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PP0V8_S2SW_CLVR_VDDDIG — 56 57 58 59 60

44 GND
44 NC_LPMU_SW0
LPMU SW0 (Unused)

GND — 150 153 157
NC_LPMU_SW0 MAKE_BASE=TRUE

44 GND
44 NC_LPMU_SW1
LPMU SW1 (Unused)

GND — 150 153 157
NC_LPMU_SW1 MAKE_BASE=TRUE

44 PP1V2_S2
44 PP1V2_S2SW_CLVR_VDDIO
44 39
LPMU SW2
Vboot = 1225mV
Enabled in SLP_S2R and above

PP1V2_S2 — 44 46 153
PP1V2_S2SW_CLVR_VDDIO — 145
VOLTAGE=1.225V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PP1V2_S2SW_CLVR_VDDIO — 56 57 58 59 60 61

40 PP1V2_S2
40 PPVDD_LOW_S2
FPMU LDO0
Vboot = 725mV for FuseRev>=3
850mV for FuseRev=2
800mV for FuseRev=1

PP1V2_S2 — 40 153
PPVDD_LOW_S2 — 145
VOLTAGE=0.8V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PPVDD_LOW_S2 — 16
PPVDD_LOW_S2 — 16

40 PP3V8_AON_FPMU
40 PP1V8_AWAKE_SEPROM_LDO
FPMU LDO1

PP3V8_AON_FPMU — 38 40 42 43 48 151
PP1V8_AWAKE_SEPROM_LDO — 143
VOLTAGE=1.8V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PP1V8_AWAKE_SEPROM_LDO — 11

FPMU LDO2 (Unused)

FPMU LDO3 (Project Specific)

FPMU LDO4 (Unused)

40 GND
40 NC_FPMU_LDO5
FPMU LDO5 (Unused)

GND — 150 153 157
NC_FPMU_LDO5 MAKE_BASE=TRUE

Vboot note is based on actual boot voltages of latest OTP, based on SOC Tunables Spec SOC Setup Voltage Table
* indicates 0V boot until iBoot DRAM enable; ^ indicates 0V boot until PMGR/Volman enable

VOLTAGE property for SOC rails is based on the max of OTP and "Design-intended voltage" in SOC Tunables Spec SOC Setup Voltage Table

47 45 39 PPVDD_SOC_S1
45 PPVDD_SOC_S1
LPMU Buck0 (PD#10)
Vboot = 775mV
DVFM 642~904mV

PPVDD_SOC_S1 — 144 145 146
VOLTAGE=0.944V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PPVDD_SOC_S1 — 16

47 45 39 PPVDD_SRAM_S1
45 PPVDD_SRAM_S1
LPMU Buck1 (PD#11)
Vboot = 850mV; 820mV w/overrides for FuseRev<3
815mV for FuseRev>=3

PPVDD_SRAM_S1 — 144
VOLTAGE=0.85V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PPVDD_SRAM_S1 — 16

47 45 39 PPVDD2H1_S2SW
45 PPVDD2H1_S2SW
LPMU Buck2 (PD#12)
Vboot = 1050mV*
DVFM 900~1100mV
Enabled in SLP_S2R and above

PPVDD2H1_S2SW — 23
VOLTAGE=1.06V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PPVDD2H1_S2SW — 23

47 45 39 PP1V8_S2SW
45 PP1V8_S2SW
LPMU Buck3 (PD#13)
Vboot = 1.8V
Enabled in SLP_S2R and above

PP1V8_S2SW — 146 148
VOLTAGE=1.8V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PP1V8_S2SW — 17
PP1V8_S2SW — 56 57 58 59 60
PP1V8_S2SW — 17

LPMU Buck4 (Unused)

150 47 45 39 PPVDD_ECPU_AWAKESW
150 45 PPVDD_ECPU_AWAKESW
LPMU Buck5 (PD#15)
Vboot = 725mV
DVFM 525~1060mV

PPVDD_ECPU_AWAKESW — 144
VOLTAGE=1.06V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PPVDD_ECPU_AWAKESW — 15

47 45 39 PPVDDQ1_S1
45 PPVDDQ1_S1
LPMU Buck6 (PD#16)
Vboot = 550mV*

PPVDDQ1_S1 — 144
VOLTAGE=0.55V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PPVDDQ1_S1 — 5 18

47 45 39 PPVDD_AMPH1_S2SW
45 PPVDD_AMPH1_S2SW
LPMU Buck7 (PD#17)
Vboot = 1120mV
Enabled in SLP_S2R and above

PPVDD_AMPH1_S2SW — 144
VOLTAGE=1.12V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PPVDD_AMPH1_S2SW — 19

47 46 39 PP1V2_S2
46 PP1V2_S2
LPMU Buck8 (PD#18)
Vboot = 1225mV

PP1V2_S2 — 144 150 159
VOLTAGE=1.225V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PP1V2_S2 — 10 21 148
PP1V2_S2 — 5
PP1V2_S2 — 44 46 153
PP1V2_S2 — 40 153

47 46 39 PPVDD_ECPU_SRAM_AWAKESW
46 PPVDD_ECPU_SRAM_AWAKESW
LPMU Buck9 (PD#19)
Vboot = 850mV
DVFM 770~1060mV

PPVDD_ECPU_SRAM_AWAKESW — 143 145
VOLTAGE=1.1V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PPVDD_ECPU_SRAM_AWAKESW — 15

FPMU SW0 (Project Specific)

40 PP1V8_S2
40 PP1V8_AWAKE
FPMU SW1

PP1V8_S2 — 40 153
PP1V8_AWAKE — 144 150
VOLTAGE=1.8V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PP1V8_AWAKE — 11

40 GND
40 NC_FPMU_SW2
FPMU SW2 (Unused)

GND — 150 153 157
NC_FPMU_SW2 MAKE_BASE=TRUE

42 NC_FABRIC_ILIMIT_L — MAKE_BASE=TRUE — NC_FABRIC_ILIMIT_L

43 41 39 PPVDD_DCS_S1
41 PPVDD_DCS_S1
FPMU Buck0 (PD#20)
Vboot = 700mV
DVFM 643~1060mV

PPVDD_DCS_S1 — 144
VOLTAGE=1.02V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PPVDD_DCS_S1 — 16

43 41 39 PPVDD_DISP_EXT_AWAKESW
41 PPVDD_DISP_EXT_AWAKESW
FPMU Buck1 (PD#21)
Vboot = 765mV^
DVFM 651~965mV

PPVDD_DISP_EXT_AWAKESW — 144
VOLTAGE=0.968V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PPVDD_DISP_EXT_AWAKESW — 16

43 41 39 PPVDD2H0_S2SW
41 PPVDD2H0_S2SW
FPMU Buck2 (PD#22)
Vboot = 1050mV*
DVFM 900~1100mV
Enabled in SLP_S2R and above

PPVDD2H0_S2SW — 144
VOLTAGE=0.965V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PPVDD2H0_S2SW — 22

43 41 39 PP1V8_S2
41 PP1V8_S2
FPMU Buck3 (PD#23)
Vboot = 1.8V

PP1V8_S2 — 144 150
VOLTAGE=1.8V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PP1V8_S2 — 44
PP1V8_S2 — 40 153

43 41 39 PPVDDQ0_S1
41 PPVDDQ0_S1
FPMU Buck4 (PD#24)
Vboot = 550mV*

PPVDDQ0_S1 — 144
VOLTAGE=0.55V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PPVDDQ0_S1 — 5 18

43 41 39 PPVDD_DISP_INT_AWAKESW
41 PPVDD_DISP_INT_AWAKESW
FPMU Buck5 (PD#25)
Vboot = 765mV^
DVFM 651~997mV

PPVDD_DISP_INT_AWAKESW — 144
VOLTAGE=1.1V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PPVDD_DISP_INT_AWAKESW — 16

148 43 41 39 PPVDD_CIO_S2SW
41 PPVDD_CIO_S2SW
FPMU Buck6 (PD#26)
Vboot = 855mV for FuseRev>=3
885mV for FuseRev<3
Enabled in AWAKE
Enabled in SLP_S2R/DDR if CIO device is attached

PPVDD_CIO_S2SW — 144
VOLTAGE=0.885V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PPVDD_CIO_S2SW — 19

43 41 39 PPVDD_FIXED_S1
41 PPVDD_FIXED_S1
FPMU Buck7 (PD#27)
Vboot = 805mV for FuseRev>=3
840mV for FuseRev<3

PPVDD_FIXED_S1 — 144
VOLTAGE=0.84V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PPVDD_FIXED_S1 — 20

43 42 39 PP1V2_AWAKE
42 PP1V2_AWAKE
FPMU Buck8 (PD#28)
Vboot = 1225mV

PP1V2_AWAKE — 144 150
VOLTAGE=1.225V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PP1V2_AWAKE — 4 5 8 9
PP1V2_AWAKE — 11
PP1V2_AWAKE — 15 19 21
PP1V2_AWAKE — 11
PP1V2_AWAKE — 46

43 42 39 PPVDD_AMPH0_S2SW
42 PPVDD_AMPH0_S2SW
FPMU Buck9 (PD#29)
Vboot = 1120mV
Enabled in SLP_S2R and above

PPVDD_AMPH0_S2SW — 144
VOLTAGE=1.12V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PPVDD_AMPH0_S2SW — 19

PACK_OPTIONS TO INCLUDE IN NETLIST
LBUCK1_5PH
LBUCK2:4PH
LBUCK5:Y
LBUCK6_2PH
FBUCK0_5PH
FBUCK4_2PH
FBUCK6_2PH
LPMU_LDO2
LPMU_LDO5
LPMU_SW2
FPMU_LDO0

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POWER ALIASES PMU (C)

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LPDPTX

LPDP_INT_DATA_C_P<0>	=	LPDP_INT_DATA_C_P<0>	7 125	MAKE_BASE=TRUE
LPDP_INT_DATA_C_N<0>	=	LPDP_INT_DATA_C_N<0>	7 125	MAKE_BASE=TRUE
LPDP_INT_DATA_C_P<1>	=	LPDP_INT_DATA_C_P<1>	7 125	MAKE_BASE=TRUE
LPDP_INT_DATA_C_N<1>	=	LPDP_INT_DATA_C_N<1>	7 125	MAKE_BASE=TRUE
LPDP_INT_DATA_C_P<2>	=	LPDP_INT_DATA_C_P<2>	7 125	MAKE_BASE=TRUE
LPDP_INT_DATA_C_N<2>	=	LPDP_INT_DATA_C_N<2>	7 125	MAKE_BASE=TRUE
LPDP_INT_DATA_C_P<3>	=	LPDP_INT_DATA_C_P<3>	7 125	MAKE_BASE=TRUE
LPDP_INT_DATA_C_N<3>	=	LPDP_INT_DATA_C_N<3>	7 125	MAKE_BASE=TRUE
LPDP_INT_AUX_C_P	=	LPDP_INT_AUX_C_P	7 125	MAKE_BASE=TRUE
LPDP_INT_AUX_C_N	=	LPDP_INT_AUX_C_N	7 125	MAKE_BASE=TRUE
156 LPDP_INT_HPD	=	LPDP_INT_HPD	7 125 144 156	MAKE_BASE=TRUE

NAND

8 NC_PCIE_CLK100M_NAND0_1P	=	NC_PCIE_CLK100M_NAND0_1P	MAKE_BASE=TRUE
8 NC_PCIE_CLK100M_NAND0_1N	=	NC_PCIE_CLK100M_NAND0_1N	MAKE_BASE=TRUE
8 NC_PCIE_CLK100M_NAND0_3P	=	NC_PCIE_CLK100M_NAND0_3P	MAKE_BASE=TRUE
8 NC_PCIE_CLK100M_NAND0_3N	=	NC_PCIE_CLK100M_NAND0_3N	MAKE_BASE=TRUE
8 NC_PCIE_CLK100M_NAND1_1P	=	NC_PCIE_CLK100M_NAND1_1P	MAKE_BASE=TRUE
8 NC_PCIE_CLK100M_NAND1_1N	=	NC_PCIE_CLK100M_NAND1_1N	MAKE_BASE=TRUE
8 NC_PCIE_CLK100M_NAND1_3P	=	NC_PCIE_CLK100M_NAND1_3P	MAKE_BASE=TRUE
8 NC_PCIE_CLK100M_NAND1_3N	=	NC_PCIE_CLK100M_NAND1_3N	MAKE_BASE=TRUE

USB3

112 SWD_NAND0_S5E0_S5E1_SWCLK	=	SWD_NAND0_S5E0_S5E1_SWCLK	12 MAKE_BASE=TRUE
113 SWD_NAND0_S5E0_S5E1_SWCLK	=		
114 SWD_NAND0_S5E2_S5E3_SWCLK	=	SWD_NAND0_S5E2_S5E3_SWCLK	12 MAKE_BASE=TRUE
115 SWD_NAND0_S5E2_S5E3_SWCLK	=		
112 SWD_NAND0_S5E0_S5E1_SWDIO	=	SWD_NAND0_S5E0_S5E1_SWDIO	12 MAKE_BASE=TRUE
113 SWD_NAND0_S5E0_S5E1_SWDIO	=		
114 SWD_NAND0_S5E2_S5E3_SWDIO	=	SWD_NAND0_S5E2_S5E3_SWDIO	12 MAKE_BASE=TRUE
115 SWD_NAND0_S5E2_S5E3_SWDIO	=		
117 SWD_NAND1_S5E0_S5E1_SWCLK	=	SWD_NAND1_S5E0_S5E1_SWCLK	12 MAKE_BASE=TRUE
118 SWD_NAND1_S5E0_S5E1_SWCLK	=		
119 SWD_NAND1_S5E2_S5E3_SWCLK	=	SWD_NAND1_S5E2_S5E3_SWCLK	12 MAKE_BASE=TRUE
120 SWD_NAND1_S5E2_S5E3_SWCLK	=		
117 SWD_NAND1_S5E0_S5E1_SWDIO	=	SWD_NAND1_S5E0_S5E1_SWDIO	12 MAKE_BASE=TRUE
118 SWD_NAND1_S5E0_S5E1_SWDIO	=		
119 SWD_NAND1_S5E2_S5E3_SWDIO	=	SWD_NAND1_S5E2_S5E3_SWDIO	12 MAKE_BASE=TRUE
120 SWD_NAND1_S5E2_S5E3_SWDIO	=		

ATC3 - HDMI

9 DP_DP2HDMI_DATA_P<2>	=	DP_DP2HDMI_DATA_P<2>	MAKE_BASE=TRUE
102 DP_DP2HDMI_DATA_P<2>	=		
9 DP_DP2HDMI_DATA_N<2>	=	DP_DP2HDMI_DATA_N<2>	MAKE_BASE=TRUE
102 DP_DP2HDMI_DATA_N<2>	=		
9 DP_DP2HDMI_DATA_P<3>	=	DP_DP2HDMI_DATA_P<3>	MAKE_BASE=TRUE
102 DP_DP2HDMI_DATA_P<3>	=		
9 DP_DP2HDMI_DATA_N<3>	=	DP_DP2HDMI_DATA_N<3>	MAKE_BASE=TRUE
102 DP_DP2HDMI_DATA_N<3>	=		
9 DP_DP2HDMI_DATA_P<1>	=	DP_DP2HDMI_DATA_P<1>	MAKE_BASE=TRUE
102 DP_DP2HDMI_DATA_P<1>	=		
9 DP_DP2HDMI_DATA_N<1>	=	DP_DP2HDMI_DATA_N<1>	MAKE_BASE=TRUE
102 DP_DP2HDMI_DATA_N<1>	=		
9 DP_DP2HDMI_DATA_P<0>	=	DP_DP2HDMI_DATA_P<0>	MAKE_BASE=TRUE
102 DP_DP2HDMI_DATA_P<0>	=		
9 DP_DP2HDMI_DATA_N<0>	=	DP_DP2HDMI_DATA_N<0>	MAKE_BASE=TRUE
102 DP_DP2HDMI_DATA_N<0>	=		
9 DP_DP2HDMI_AUX_P	=	DP_DP2HDMI_AUX_P	MAKE_BASE=TRUE
102 DP_DP2HDMI_AUX_P	=		
9 DP_DP2HDMI_AUX_N	=	DP_DP2HDMI_AUX_N	MAKE_BASE=TRUE
102 DP_DP2HDMI_AUX_N	=		

USBC

9 NC_USB_C0_HPD	=	NC_USB_C0_HPD	MAKE_BASE=TRUE
9 NC_USB_C1_HPD	=	NC_USB_C1_HPD	MAKE_BASE=TRUE
9 NC_USB_C2_HPD	=	NC_USB_C2_HPD	MAKE_BASE=TRUE

ENET

SD

8 PCIE_SD_UHS2_R2D_C_P	=	PCIE_SD_UHS2_R2D_C_P	MAKE_BASE=TRUE 106
8 PCIE_SD_UHS2_R2D_C_N	=	PCIE_SD_UHS2_R2D_C_N	MAKE_BASE=TRUE 106
8 PCIE_SD_UHS2_D2R_P	=	PCIE_SD_UHS2_D2R_P	MAKE_BASE=TRUE 106
8 PCIE_SD_UHS2_D2R_N	=	PCIE_SD_UHS2_D2R_N	MAKE_BASE=TRUE 106
8 PCIE_CLK100M_SD_UHS2_P	=	PCIE_CLK100M_SD_UHS2_P	MAKE_BASE=TRUE 106
8 PCIE_CLK100M_SD_UHS2_N	=	PCIE_CLK100M_SD_UHS2_N	MAKE_BASE=TRUE 106
8 SD_UHS2_RESET_L	=	SD_UHS2_RESET_L	MAKE_BASE=TRUE 108
8 SD_UHS2_CLKREQ_L	=	SD_UHS2_CLKREQ_L	MAKE_BASE=TRUE 108

Deleted SDEXP_RESET_L alias Checking with Harshi

			MAKE_BASE=TRUE
9 NC_EUSB_ATC3P	=	NC_EUSB_ATC3P	
9 NC_EUSB_ATC3N	=	NC_EUSB_ATC3N	

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Columbus_Redriver_Aliasing

104	IN	USBC_ATC2_R2D_LS_C_P<1>	MAKE_BASE=TRUE	USBC_ATC2_R2D_LS_C_P<1> 90
104	IN	USBC_ATC2_R2D_LS_C_N<1>	MAKE_BASE=TRUE	USBC_ATC2_R2D_LS_C_N<1> 90
104	IN	USBC_ATC2_R2D_LS_C_P<2>	MAKE_BASE=TRUE	USBC_ATC2_R2D_LS_C_P<2> 90
104	IN	USBC_ATC2_R2D_LS_C_N<2>	MAKE_BASE=TRUE	USBC_ATC2_R2D_LS_C_N<2> 90
104	BI	USBC_ATC2_D2R_LS_P<1>	MAKE_BASE=TRUE	USBC_ATC2_D2R_LS_P<1> 90
104	BI	USBC_ATC2_D2R_LS_N<1>	MAKE_BASE=TRUE	USBC_ATC2_D2R_LS_N<1> 90
104	BI	USBC_ATC2_D2R_LS_P<2>	MAKE_BASE=TRUE	USBC_ATC2_D2R_LS_P<2> 90
104	BI	USBC_ATC2_D2R_LS_N<2>	MAKE_BASE=TRUE	USBC_ATC2_D2R_LS_N<2> 90

Ace3 I2c Connections to Lifuka and Columbus.

145 84 82 80	I2C_UPC0_ATCRTMR0_SCL	MAKE_BASE=TRUE	I2C_UPC0_ATCRTMR0_SCL	BI 80
			I2C_UPC0_ATCRTMR0_SCL	BI 86
145 84 82 80	I2C_UPC0_ATCRTMR0_SDA	MAKE_BASE=TRUE	I2C_UPC0_ATCRTMR0_SDA	BI 80
			I2C_UPC0_ATCRTMR0_SDA	BI 86
145 85 82 81	I2C_UPC1_ATCRTMR1_SCL	MAKE_BASE=TRUE	I2C_UPC1_ATCRTMR1_SCL	BI 81
			I2C_UPC1_ATCRTMR1_SCL	BI 86
145 85 82 81	I2C_UPC1_ATCRTMR1_SDA	MAKE_BASE=TRUE	I2C_UPC1_ATCRTMR1_SDA	BI 81
			I2C_UPC1_ATCRTMR1_SDA	BI 86
145 93 91 90	I2C_UPC2_ATCRTMR2_SCL	MAKE_BASE=TRUE	I2C_UPC2_ATCRTMR2_SCL	BI 90
			I2C_UPC2_ATCRTMR2_SCL	BI 94
			I2C_UPC2_ATCRTMR2_SCL	BI 104
145 93 91 90	I2C_UPC2_ATCRTMR2_SDA	MAKE_BASE=TRUE	I2C_UPC2_ATCRTMR2_SDA	BI 90
			I2C_UPC2_ATCRTMR2_SDA	BI 94
			I2C_UPC2_ATCRTMR2_SDA	BI 104

Lifuka Controls

80	GND	MAKE_BASE=TRUE	
81	GND		
90	GND		

Connecting UPC01 & UPC5 I2C1s Together per radar://96085596

145 98	I2C_UPC015_3V3_SCL	MAKE_BASE=TRUE	I2C_UPC015_3V3_SCL	OUT 82 83
			I2C_UPC015_3V3_SCL	IN 32 33 145
145 98	I2C_UPC015_3V3_SDA	MAKE_BASE=TRUE	I2C_UPC015_3V3_SDA	BI 32 33 145
			I2C_UPC015_3V3_SDA	BI 82 83

Ace3 USB0-1 SWD - Alias for JF202 Disconnect change

12	IN SWD_UPC_SWCLK0	MAKE_BASE=TRUE	SWD_UPC_SWCLK0	OUT 82
			SWD_UPC_SWCLK0	OUT 12 84
12	IN SWD_UPC_SWDIO0	MAKE_BASE=TRUE	SWD_UPC_SWDIO0	OUT 82
			SWD_UPC_SWDIO0	OUT 12 84
12	IN SWD_UPC_SWCLK2	MAKE_BASE=TRUE	SWD_UPC_SWCLK2	OUT 91
			SWD_UPC_SWCLK2	OUT 12 93
12	IN SWD_UPC_SWDIO2	MAKE_BASE=TRUE	SWD_UPC_SWDIO2	OUT 91
			SWD_UPC_SWDIO2	OUT 12 93

NC MOGUL

87 84	NC_UPC0_AID0	MAKE_BASE=TRUE	NC_UPC0_AID0

HDMI ARKANOID ALIASING

155	I2C_DP2HDMI_SCL		I2C_DP2HDMI_SCL 101 103 156
155	I2C_DP2HDMI_SCL		
155	I2C_DP2HDMI_SDA		I2C_DP2HDMI_SDA 101 103 156
155	I2C_DP2HDMI_SDA		
155	DP2HDMI_RESET_R_L		DP2HDMI_RESET_R_L 101 102 103 150
		MAKE_BASE=TRUE	
155 103 102 101	DP2HDMI_RESET_R_L	MAKE_BASE=TRUE	DP2HDMI_RESET_R_L 155
155	I2C_DP2HDMI_SCL	MAKE_BASE=TRUE	I2C_DP2HDMI_SCL 155
155	I2C_DP2HDMI_SDA	MAKE_BASE=TRUE	I2C_DP2HDMI_SDA 155
103 102 101 99	HDMI_HPD_IN	MAKE_BASE=TRUE	HDMI_HPD_IN
156 103 101	DPRX_INT_HPD	MAKE_BASE=TRUE	DPRX_INT_HPD
103 102 101	DPRX_AUX_N	MAKE_BASE=TRUE	DPRX_AUX_N
		MAKE_BASE=TRUE	
103 102 101	DPRX_AUX_P	MAKE_BASE=TRUE	DPRX_AUX_P
103 101 99	HDMI_DDC_5V_SDA	MAKE_BASE=TRUE	HDMI_DDC_5V_SDA
103 101 99	HDMI_DDC_5V_SCL	MAKE_BASE=TRUE	HDMI_DDC_5V_SCL
		MAKE_BASE=TRUE	

	NC_HDMI_CECFET_EN	MAKE_BASE=TRUE	NC_HDMI_CECFET_EN 42
	CKPLUS_WAIVE=NC_CHECKS		

PMU Control

144 126 121 116 96 46	PMU_SYS_ALIVE	MAKE_BASE=TRUE	PMU_SYS_ALIVE 88
			PMU_SYS_ALIVE 102
147 143 38	IN PMU_UPC_FORCE_DFU	MAKE_BASE=TRUE	PMU_UPC_FORCE_DFU BI 87

Ace3 Control

149	SOC_DOCK_CONNECT_UPC	MAKE_BASE=TRUE	SOC_DOCK_CONNECT_UPC 87
84 83	UPC01_5V_EN		UPC01_5V_EN 88 145
85 83	UPC01_5V_EN		MAKE_BASE=TRUE
146 144 143 46 10 5	PMU_ACTIVE_READY	MAKE_BASE=TRUE	PMU_ACTIVE_READY 83
			PMU_ACTIVE_READY 92
84 82	IN INPUT_PWR_2LOW_L		
85	IN INPUT_PWR_2LOW_L		
93 91	IN INPUT_PWR_2LOW_L		
32	IN INPUT_PWR_2LOW_L		INPUT_PWR_2LOW_L OUT 28
			MAKE_BASE=TRUE
87	IN SOC_FORCE_DFU		SOC_FORCE_DFU OUT 5 143
			MAKE_BASE=TRUE
84	IN UPC_PMU_RESET_1V2		
85	IN UPC_PMU_RESET_1V2		
93	IN UPC_PMU_RESET_1V2		UPC_PMU_RESET_1V2 OUT 46 145 147 149
			MAKE_BASE=TRUE

Ace3 USB2 to Macaw

	USB2_ATC1_LS_P	MAKE_BASE=TRUE	USB2_ATC1_LS_P 86 98
	USB2_ATC1_LS_N	MAKE_BASE=TRUE	USB2_ATC1_LS_N 86 98
	USB2_ATC2_LS_P	MAKE_BASE=TRUE	USB2_ATC2_LS_P 94 98
	USB2_ATC2_LS_N	MAKE_BASE=TRUE	USB2_ATC2_LS_N 94 98

Ace3 SPMI Connections

12	IN SPMI_UPC0_CLK	MAKE_BASE=TRUE	SPMI_UPC0_CLK OUT 82 84
12	IN SPMI_UPC1_CLK	MAKE_BASE=TRUE	SPMI_UPC1_CLK OUT 85
144 12	IN SPMI_UPC5_CLK	MAKE_BASE=TRUE	SPMI_UPC5_CLK OUT 32
12	BI SPMI_UPC0_DATA	MAKE_BASE=TRUE	SPMI_UPC0_DATA BI 82 84
12	BI SPMI_UPC1_DATA	MAKE_BASE=TRUE	SPMI_UPC1_DATA BI 85
144 12	BI SPMI_UPC5_DATA	MAKE_BASE=TRUE	SPMI_UPC5_DATA BI 32
12	IN SPMI_UPC2_CLK	MAKE_BASE=TRUE	SPMI_UPC2_CLK OUT 93
12	IN SPMI_UPC2_CLK_R2	MAKE_BASE=TRUE	SPMI_UPC2_CLK_R2 OUT 91
12	BI SPMI_UPC2_DATA	MAKE_BASE=TRUE	SPMI_UPC2_DATA BI 93
12	BI SPMI_UPC2_DATA_R2	MAKE_BASE=TRUE	SPMI_UPC2_DATA_R2 BI 91

SoC USB2 Connections

98 9	EUSB_ATC0_P	MAKE_BASE=TRUE	EUSB_ATC0_P BI 86
98 9	EUSB_ATC0_N	MAKE_BASE=TRUE	EUSB_ATC0_N BI 86
98 9	EUSB_ATC1_P	MAKE_BASE=TRUE	EUSB_ATC1_P BI 86
98 9	EUSB_ATC1_N	MAKE_BASE=TRUE	EUSB_ATC1_N BI 86
98 9	EUSB_ATC2_P	MAKE_BASE=TRUE	EUSB_ATC2_P BI 94
98 9	EUSB_ATC2_N	MAKE_BASE=TRUE	EUSB_ATC2_N BI 94
9	EUSB_DBG_P	MAKE_BASE=TRUE	EUSB_DBG_P BI 86
9	EUSB_DBG_N	MAKE_BASE=TRUE	EUSB_DBG_N BI 86

TP Nets Alis to NC

	NC_VDDH_SPS_GL4	MAKE_BASE=TRUE	NC_VDDH_SPS_GL4 54
	NC_VDDH_SPS_GL3	MAKE_BASE=TRUE	NC_VDDH_SPS_GL3 53
	NC_VDDH_SPS_GL2	MAKE_BASE=TRUE	NC_VDDH_SPS_GL2 53
	NC_VDDH_SPS_GL1	MAKE_BASE=TRUE	NC_VDDH_SPS_GL1 52
	NC_VDDH_SPS_GL0	MAKE_BASE=TRUE	NC_VDDH_SPS_GL0 52
5	NC_T2T_TIME_SYNC_OUT	MAKE_BASE=TRUE	NC_T2T_TIME_SYNC_OUT
5	NC_T2T_TIME_SYNC_IN	MAKE_BASE=TRUE	NC_T2T_TIME_SYNC_IN
5	NC_T2T_CLK_24_OUT	MAKE_BASE=TRUE	NC_T2T_CLK_24_OUT
5	NC_T2T_CLK_24_IN	MAKE_BASE=TRUE	NC_T2T_CLK_24_IN
10	NC_SMC_UART0_R2D	MAKE_BASE=TRUE	NC_SMC_UART0_R2D
10	NC_SMC_UART0_D2R	MAKE_BASE=TRUE	NC_SMC_UART0_D2R
10	NC_SMC_I2CM0_SCL	MAKE_BASE=TRUE	NC_SMC_I2CM0_SCL
10	NC_SMC_I2CM0_SDA	MAKE_BASE=TRUE	NC_SMC_I2CM0_SDA
10	NC_SMC_GPIO9	MAKE_BASE=TRUE	NC_SMC_GPIO9
10	NC_SMC_GPIO8	MAKE_BASE=TRUE	NC_SMC_GPIO8
10	NC_SMC_GPIO7	MAKE_BASE=TRUE	NC_SMC_GPIO7
10	NC_NUB_SWD_TMS3	MAKE_BASE=TRUE	NC_NUB_SWD_TMS3
10	NC_NUB_SWD_TMS2	MAKE_BASE=TRUE	NC_NUB_SWD_TMS2
10	NC_NUB_SWD_TCK_OUT2	MAKE_BASE=TRUE	NC_NUB_SWD_TCK_OUT2
10	NC_NUB_SPMI_A2_DATA	MAKE_BASE=TRUE	NC_NUB_SPMI_A2_DATA
10	NC_NUB_SPMI_A2_CLK	MAKE_BASE=TRUE	NC_NUB_SPMI_A2_CLK
10	NC_NUB_SPI0_SSIN	MAKE_BASE=TRUE	NC_NUB_SPI0_SSIN
10	NC_NUB_SPI0_SCLK	MAKE_BASE=TRUE	NC_NUB_SPI0_SCLK
10	NC_NUB_SPI0_MOSI	MAKE_BASE=TRUE	NC_NUB_SPI0_MOSI
10	NC_NUB_SPI0_MISO	MAKE_BASE=TRUE	NC_NUB_SPI0_MISO
6	NC_MTP_FUNC7	MAKE_BASE=TRUE	NC_MTP_FUNC7
6	NC_MTP_FUNC6	MAKE_BASE=TRUE	NC_MTP_FUNC6
6	NC_MTP_FUNC2	MAKE_BASE=TRUE	NC_MTP_FUNC2
10	NC_JTAG_SLV_TRSTN	MAKE_BASE=TRUE	NC_JTAG_SLV_TRSTN
10	NC_JTAG_SLV_TMS	MAKE_BASE=TRUE	NC_JTAG_SLV_TMS
10	NC_JTAG_SLV_TDO	MAKE_BASE=TRUE	NC_JTAG_SLV_TDO
10	NC_JTAG_SLV_TDI	MAKE_BASE=TRUE	NC_JTAG_SLV_TDI
10	NC_JTAG_SLV_TCK	MAKE_BASE=TRUE	NC_JTAG_SLV_TCK
5	NC_CLVR_GPIO9	MAKE_BASE=TRUE	NC_CLVR_GPIO9
6	NC_AP_I2C00_SDA	MAKE_BASE=TRUE	NC_AP_I2C00_SDA
6	NC_AP_I2C00_SCL	MAKE_BASE=TRUE	NC_AP_I2C00_SCL
6	NC_AP_GPIO5	MAKE_BASE=TRUE	NC_AP_GPIO5
6	NC_AP_GPIO40	MAKE_BASE=TRUE	NC_AP_GPIO40
6	NC_AP_FPWM2	MAKE_BASE=TRUE	NC_AP_FPWM2
6	NC_AP_FPWM1	MAKE_BASE=TRUE	NC_AP_FPWM1
10	NC_AOP_SCM_IO1	MAKE_BASE=TRUE	NC_AOP_SCM_IO1
10	NC_AOP_I2CM2_SDA	MAKE_BASE=TRUE	NC_AOP_I2CM2_SDA
10	NC_AOP_I2CM2_SCL	MAKE_BASE=TRUE	NC_AOP_I2CM2_SCL
5	NC_A2A_WAKEUP	MAKE_BASE=TRUE	NC_A2A_WAKEUP
5	NC_A2A_SYNC_REQ	MAKE_BASE=TRUE	NC_A2A_SYNC_REQ
5	NC_A2A_SYNC_ACK	MAKE_BASE=TRUE	NC_A2A_SYNC_ACK
11	NC_PPVDD_PCPU1_AWAKESW	MAKE_BASE=TRUE	NC_PPVDD_PCPU1_AWAKESW
6	SOC_MASTER_SYNC_GEN_7	MAKE_BASE=TRUE	SOC_MASTER_SYNC_GEN_7
10	AON_TST_CLKOUT	MAKE_BASE=TRUE	AON_TST_CLKOUT

Alias to remove TP_ with PPs present

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REF_SECDIS_SAK

124 FTCAM_ENABLE_1V8_OUT — FTCAM_ENABLE_1V8_OUT (MAKE_BASE=TRUE) 123 144

SECDIS AND LAS REF DESIGN

130 AMR1_OR_ND_1V8 — AMR1_OR_ND_1V8 (MAKE_BASE=TRUE) 156
130 AMR1_OR_ND_1V8 — AMR1_OR_ND_1V8 (MAKE_BASE=TRUE) 156
129 144 AMR1_OR_ND_1V8 — AMR1_OR_ND_1V8 (MAKE_BASE=TRUE) 156
129 AMR1_OR_ND_1V8 — AMR1_OR_ND_1V8 (MAKE_BASE=TRUE) 156

CHARGER

CHGR_INT_L — CHGR_INT_L (MAKE_BASE=TRUE) 10 30 144
62 37 145 P5VS2HOLD_PGOOD — P5VS2HOLD_PGOOD (MAKE_BASE=TRUE) 159

HDMI

103 101 155 DPRX_INT_HPD (MAKE_BASE=TRUE) — DPRX_INT_HPD 9

LPDPTX

125 7 154 144 LPDP_INT_HPD (MAKE_BASE=TRUE) — LPDP_INT_HPD 154

NAND

112 NAND0_RESET_L — NAND0_RESET_L (MAKE_BASE=TRUE) 116 143
113 NAND0_RESET_L
114 NAND0_RESET_L
115 NAND0_RESET_L

117 NAND1_RESET_L — NAND1_RESET_L (MAKE_BASE=TRUE) 121 143
118 NAND1_RESET_L
119 NAND1_RESET_L
120 NAND1_RESET_L

IPD

12 SWD_IPD_DATA_R — SWD_IPD_DATA_R (MAKE_BASE=TRUE) 139
12 SWD_IPD_CLK_R — SWD_IPD_CLK_R (MAKE_BASE=TRUE) 139

SMC_I2C5

10 IN NC_I2C_SMC_SNS1_SCL — NC_I2C_SMC_SNS1_SCL (MAKE_BASE=TRUE)
10 BI NC_I2C_SMC_SNS1_SDA — NC_I2C_SMC_SNS1_SDA (MAKE_BASE=TRUE)

AP_I2C6

64 6 IN I2C_ATCRTMR_SCL (MAKE_BASE=TRUE)
I2C_ATCRTMR_SCL 80
I2C_ATCRTMR_SCL 81
I2C_ATCRTMR_SCL 90

64 6 BI I2C_ATCRTMR_SDA (MAKE_BASE=TRUE)
I2C_ATCRTMR_SDA 80
I2C_ATCRTMR_SDA 81
I2C_ATCRTMR_SDA 90

GND — GND (MAKE_BASE=TRUE)

GND — GND (MAKE_BASE=TRUE)
GND

129 SPI_AOP_LAS_MISO_1V8 — SPI_AOP_LAS_MISO_1V8 (MAKE_BASE=TRUE) 14

NC SPN'S

29 NC_CHGR_EN_VR1 — NC_CHGR_EN_VR1 (MAKE_BASE=TRUE)

NC_NAND0_OCARINA_WP_L — NC_NAND0_OCARINA_WP_L (MAKE_BASE=TRUE) 116

29 NC_CHGR_SMC_RST_L — NC_CHGR_SMC_RST_L (MAKE_BASE=TRUE)
29 NC_CHGR_CBC_ON — NC_CHGR_CBC_ON (MAKE_BASE=TRUE)

9 NC_CIO_ATC3_LSRX — NC_CIO_ATC3_LSRX (MAKE_BASE=TRUE)
9 NC_CIO_ATC3_LSTX — NC_CIO_ATC3_LSTX (MAKE_BASE=TRUE)

SE JUNO

27 NC_SE_SE_GPIO0 — NC_SE_SE_GPIO0 (MAKE_BASE=TRUE) (NO_TEST=1)
27 TP_SE_SE_GPIO1 — TP_SE_SE_GPIO1 (MAKE_BASE=TRUE)
27 TP_SE_SYS_GPIO0 — TP_SE_SYS_GPIO0 (MAKE_BASE=TRUE)
27 NC_SE_SYS_GPIO1 — NC_SE_SYS_GPIO1 (MAKE_BASE=TRUE) (NO_TEST=1)
27 NC_SE_SYS_GPIO2 — NC_SE_SYS_GPIO2 (MAKE_BASE=TRUE) (NO_TEST=1)
27 SE_IRQ_WAKE_R — SE_IRQ_WAKE_R (MAKE_BASE=TRUE) 14
27 NC_I2C_SE_SYS_SCL — NC_I2C_SE_SYS_SCL (MAKE_BASE=TRUE) (NO_TEST=1)
27 NC_I2C_SE_SYS_SDA — NC_I2C_SE_SYS_SDA (MAKE_BASE=TRUE) (NO_TEST=1)
27 NC_I2C_SE_SE_A_SCL — NC_I2C_SE_SE_A_SCL (MAKE_BASE=TRUE) (NO_TEST=1)
27 NC_I2C_SE_SE_A_SDA — NC_I2C_SE_SE_A_SDA (MAKE_BASE=TRUE) (NO_TEST=1)
27 NC_I2C_SE_SE_B_SCL — NC_I2C_SE_SE_B_SCL (MAKE_BASE=TRUE) (NO_TEST=1)
27 NC_I2C_SE_SE_B_SDA — NC_I2C_SE_SE_B_SDA (MAKE_BASE=TRUE) (NO_TEST=1)
27 GND — GND (MAKE_BASE=TRUE)

5 NC_SOC_MTR_TD_B — NC_SOC_MTR_TD_B (MAKE_BASE=TRUE)
5 NC_SOC_MTR_TD_BS — NC_SOC_MTR_TD_BS (MAKE_BASE=TRUE)
5 NC_SOC_MTR_TD_E — NC_SOC_MTR_TD_E (MAKE_BASE=TRUE)
5 NC_SOC_MTR_TD_ES — NC_SOC_MTR_TD_ES (MAKE_BASE=TRUE)
5 NC_SOC_MTR_TD_ESD — NC_SOC_MTR_TD_ESD (MAKE_BASE=TRUE)

56 NC_CLVR0_UT_L — NC_CLVR0_UT_L (MAKE_BASE=TRUE)
57 NC_CLVR1_UT_L — NC_CLVR1_UT_L (MAKE_BASE=TRUE)
58 NC_CLVR2_UT_L — NC_CLVR2_UT_L (MAKE_BASE=TRUE)
59 NC_CLVR3_UT_L — NC_CLVR3_UT_L (MAKE_BASE=TRUE)

145 IPD_MTP_FUNC_1 — IPD_MTP_FUNC_1 (MAKE_BASE=TRUE) 6 139

HDMI Debug I2C

155 103 101 I2C_DP2HDMI_SCL — I2C_DP2HDMI_SCL (MAKE_BASE=TRUE) 6 64
155 103 101 I2C_DP2HDMI_SDA — I2C_DP2HDMI_SDA (MAKE_BASE=TRUE) 6 64

12 SWD_NUB_ATCRTMR01_SWDIO (MAKE_BASE=TRUE)
SWD_NUB_ATCRTMR01_SWDIO 80
SWD_NUB_ATCRTMR01_SWDIO 81

145 12 SWD_NUB_ATCRTMR01_SWCLK (MAKE_BASE=TRUE)
SWD_NUB_ATCRTMR01_SWCLK 80
SWD_NUB_ATCRTMR01_SWCLK 81

12 SWD_NUB_ATCRTMR2_SWDIO (MAKE_BASE=TRUE) — SWD_NUB_ATCRTMR2_SWDIO 90
12 SWD_NUB_ATCRTMR2_SWCLK (MAKE_BASE=TRUE) — SWD_NUB_ATCRTMR2_SWCLK 90

HDMI

NC_HDMI_SAK_RESETB_2 (MAKE_BASE=TRUE) (NO_TEST=1) — NC_HDMI_SAK_RESETB_2 102

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ISP GPIO

AOP IO

10	NC_AOP_I2CM1_SCL	NC_AOP_I2CM1_SCL	MAKE_BASE=TRUE
10	NC_AOP_I2CM1_SDA	NC_AOP_I2CM1_SDA	MAKE_BASE=TRUE
10	NC_AOP_I2S0_MCK	NC_AOP_I2S0_MCK	MAKE_BASE=TRUE
10	NC_AOP_I2S0_LRCK	NC_AOP_I2S0_LRCK	MAKE_BASE=TRUE
10	NC_AOP_I2S0_DOUT	NC_AOP_I2S0_DOUT	MAKE_BASE=TRUE
10	NC_AOP_I2S0_DIN	NC_AOP_I2S0_DIN	MAKE_BASE=TRUE
10	NC_AOP_I2S0_BCLK	NC_AOP_I2S0_BCLK	MAKE_BASE=TRUE
10	NC_PDM_DMIC_CLK7	NC_PDM_DMIC_CLK7	MAKE_BASE=TRUE

SMC GPIO

MAKE_BASE=TRUE

10	SOC_DOMAIN_MGPIO_AOP1	SOC_DOMAIN_MGPIO_AOP1	157
10	NC_SMC_GPIO2	NC_SMC_GPIO2	
10	NC_SMC_GPIO3	NC_SMC_GPIO3	
10	NC_SMC_GPIO4	NC_SMC_GPIO4	
10	NC_SMC_GPIO5	NC_SMC_GPIO5	
10	NC_SMC_I2CM6_SCL	NC_SMC_I2CM6_SCL	
10	NC_SMC_I2CM6_SDA	NC_SMC_I2CM6_SDA	

SEP

MAKE_BASE=TRUE

6	SOC_DOMAIN_SGPIO_GRP1	SOC_DOMAIN_SGPIO_GRP1	157

ENET GPIO

NUB GPIO

MAKE_BASE=TRUE

10	SOC_DOMAIN_NGPIO_AOP1_0	SOC_DOMAIN_NGPIO_AOP1_0	157

6	NC_AP_UART3_R2D	NC_AP_UART3_R2D	MAKE_BASE=TRUE
6	NC_AP_UART3_D2R	NC_AP_UART3_D2R	MAKE_BASE=TRUE
6	NC_AP_UART3_R2D_RTS_L	NC_AP_UART3_R2D_RTS_L	MAKE_BASE=TRUE
6	NC_AP_UART3_D2R_CTS_L	NC_AP_UART3_D2R_CTS_L	MAKE_BASE=TRUE
6	NC_AP_UART4_D2R	NC_AP_UART4_D2R	MAKE_BASE=TRUE
6	NC_AP_UART4_R2D	NC_AP_UART4_R2D	MAKE_BASE=TRUE

NAND

8	SOC_DOMAIN_HGPIO_GRP0_0	SOC_DOMAIN_HGPIO_GRP0_0	MAKE_BASE=TRUE 157
8	SOC_DOMAIN_HGPIO_GRP0_1	SOC_DOMAIN_HGPIO_GRP0_1	MAKE_BASE=TRUE 157

NC SPN's

7	NC_DISP_TOUCH_BSYNC0	NC_DISP_TOUCH_BSYNC0	MAKE_BASE=TRUE
7	NC_DISP_TOUCH_BSYNC1	NC_DISP_TOUCH_BSYNC1	MAKE_BASE=TRUE
7	NC_DISP_TOUCH_EB	NC_DISP_TOUCH_EB	MAKE_BASE=TRUE

ISP SPMI

7	NC_ISP_SPMI0_CLK	NC_ISP_SPMI0_CLK	MAKE_BASE=TRUE
7	NC_ISP_SPMI0_DATA	NC_ISP_SPMI0_DATA	MAKE_BASE=TRUE

GND UNUSED PMU

153 150	GND	GND	MAKE_BASE=TRUE

D2D IO

NC SOC

6	NC_AP_UART1_R2D	NC_AP_UART1_R2D	MAKE_BASE=TRUE
6	NC_AP_UART1_D2R	NC_AP_UART1_D2R	MAKE_BASE=TRUE
6	NC_AP_UART1_R2D_RTS_L	NC_AP_UART1_R2D_RTS_L	MAKE_BASE=TRUE
6	NC_AP_UART1_D2R_CTS_L	NC_AP_UART1_D2R_CTS_L	MAKE_BASE=TRUE
6	NC_AP_UART5_R2D	NC_AP_UART5_R2D	MAKE_BASE=TRUE
6	NC_AP_SPI3_MOSI	NC_AP_SPI3_MOSI	MAKE_BASE=TRUE
6	NC_AP_SPI3_MISO	NC_AP_SPI3_MISO	MAKE_BASE=TRUE
6	NC_AP_SPI3_SCLK	NC_AP_SPI3_SCLK	MAKE_BASE=TRUE
6	NC_AP_SPI3_SSIN	NC_AP_SPI3_SSIN	MAKE_BASE=TRUE
6	NC_AP_SPI5_MOSI	NC_AP_SPI5_MOSI	MAKE_BASE=TRUE
6	NC_AP_SPI5_MISO	NC_AP_SPI5_MISO	MAKE_BASE=TRUE
6	NC_AP_SPI5_SCLK	NC_AP_SPI5_SCLK	MAKE_BASE=TRUE
6	NC_AP_SPI5_SSIN	NC_AP_SPI5_SSIN	MAKE_BASE=TRUE
6	NC_AP_SGPIO1	NC_AP_SGPIO1	MAKE_BASE=TRUE
6	NC_AP_SSPI0_MISO	NC_AP_SSPI0_MISO	MAKE_BASE=TRUE
6	NC_AP_SSPI0_SCLK	NC_AP_SSPI0_SCLK	MAKE_BASE=TRUE
7	NC_ISP_GPIO_1	NC_ISP_GPIO_1	MAKE_BASE=TRUE
7	NC_ISP_GPIO_2	NC_ISP_GPIO_2	MAKE_BASE=TRUE
7	NC_ISP_GPIO_3	NC_ISP_GPIO_3	MAKE_BASE=TRUE
6	NC_AP_GPIO2	NC_AP_GPIO2	MAKE_BASE=TRUE
6	NC_AP_GPIO6	NC_AP_GPIO6	MAKE_BASE=TRUE
6	NC_AP_GPIO11	NC_AP_GPIO11	MAKE_BASE=TRUE
6	NC_AP_GPIO12	NC_AP_GPIO12	MAKE_BASE=TRUE
6	NC_AP_GPIO18	NC_AP_GPIO18	MAKE_BASE=TRUE
6	NC_AP_GPIO19	NC_AP_GPIO19	MAKE_BASE=TRUE
6	NC_AP_GPIO20	NC_AP_GPIO20	MAKE_BASE=TRUE
6	NC_AP_GPIO23	NC_AP_GPIO23	MAKE_BASE=TRUE
6	NC_AP_GPIO24	NC_AP_GPIO24	MAKE_BASE=TRUE
6	NC_AP_GPIO25	NC_AP_GPIO25	MAKE_BASE=TRUE
6	NC_AP_GPIO26	NC_AP_GPIO26	MAKE_BASE=TRUE
6	NC_AP_GPIO27	NC_AP_GPIO27	MAKE_BASE=TRUE
6	NC_AP_GPIO28	NC_AP_GPIO28	MAKE_BASE=TRUE
6	NC_AP_GPIO30	NC_AP_GPIO30	MAKE_BASE=TRUE
6	NC_AP_GPIO31	NC_AP_GPIO31	MAKE_BASE=TRUE
6	NC_AP_GPIO32	NC_AP_GPIO32	MAKE_BASE=TRUE
6	NC_AP_GPIO33	NC_AP_GPIO33	MAKE_BASE=TRUE
6	NC_AP_GPIO22	NC_AP_GPIO22	MAKE_BASE=TRUE
10	NC_AOP_FUNC15	NC_AOP_FUNC15	MAKE_BASE=TRUE
10	NC_NUB_GPIO10	NC_NUB_GPIO10	MAKE_BASE=TRUE
10	NC_NUB_GPIO13	NC_NUB_GPIO13	MAKE_BASE=TRUE
10	NC_NUB_GPIO14	NC_NUB_GPIO14	MAKE_BASE=TRUE
10	NC_NUB_GPIO15	NC_NUB_GPIO15	MAKE_BASE=TRUE

8	NC_TP_GE_PCIE_TX0P	NC_TP_GE_PCIE_TX0P	MAKE_BASE=TRUE
8	NC_TP_GE_PCIE_TX0N	NC_TP_GE_PCIE_TX0N	MAKE_BASE=TRUE
8	NC_TP_GE_PCIE_RX0P	NC_TP_GE_PCIE_RX0P	MAKE_BASE=TRUE
8	NC_TP_GE_PCIE_RX0N	NC_TP_GE_PCIE_RX0N	MAKE_BASE=TRUE
8	NC_TP_GE_PCIE_TX1P	NC_TP_GE_PCIE_TX1P	MAKE_BASE=TRUE
8	NC_TP_GE_PCIE_TX1N	NC_TP_GE_PCIE_TX1N	MAKE_BASE=TRUE
8	NC_TP_GE_PCIE_RX1P	NC_TP_GE_PCIE_RX1P	MAKE_BASE=TRUE
8	NC_TP_GE_PCIE_RX1N	NC_TP_GE_PCIE_RX1N	MAKE_BASE=TRUE
8	NC_TP_GE_PCIE_REF_CLKP	NC_TP_GE_PCIE_REF_CLKP	MAKE_BASE=TRUE
8	NC_TP_GE_PCIE_REF_CLKN	NC_TP_GE_PCIE_REF_CLKN	MAKE_BASE=TRUE
8	NC_TP_GE_PCIE_CLKREQ_L	NC_TP_GE_PCIE_CLKREQ_L	MAKE_BASE=TRUE
8	NC_TP_GE_PCIE_PERST_L	NC_TP_GE_PCIE_PERST_L	MAKE_BASE=TRUE
8	NC_TP_GE_PCIE_TX2P	NC_TP_GE_PCIE_TX2P	MAKE_BASE=TRUE
8	NC_TP_GE_PCIE_TX2N	NC_TP_GE_PCIE_TX2N	MAKE_BASE=TRUE
8	NC_TP_GE_PCIE_RX2P	NC_TP_GE_PCIE_RX2P	MAKE_BASE=TRUE
8	NC_TP_GE_PCIE_RX2N	NC_TP_GE_PCIE_RX2N	MAKE_BASE=TRUE
8	NC_TP_GE_PCIE_TX3P	NC_TP_GE_PCIE_TX3P	MAKE_BASE=TRUE
8	NC_TP_GE_PCIE_TX3N	NC_TP_GE_PCIE_TX3N	MAKE_BASE=TRUE
8	NC_TP_GE_PCIE_RX3P	NC_TP_GE_PCIE_RX3P	MAKE_BASE=TRUE
8	NC_TP_GE_PCIE_RX3N	NC_TP_GE_PCIE_RX3N	MAKE_BASE=TRUE

8	NC_TP_GP_PCIE_REF_CLK3_P	NC_TP_GP_PCIE_REF_CLK3_P	MAKE_BASE=TRUE
8	NC_TP_GP_PCIE_REF_CLK3_N	NC_TP_GP_PCIE_REF_CLK3_N	MAKE_BASE=TRUE
8	NC_TP_GP_PCIE_CLKREQ3_L	NC_TP_GP_PCIE_CLKREQ3_L	MAKE_BASE=TRUE
8	NC_TP_GP_PCIE_PERST3_L	NC_TP_GP_PCIE_PERST3_L	MAKE_BASE=TRUE
8	NC_TP_GP_PCIE_TX3_P	NC_TP_GP_PCIE_TX3_P	MAKE_BASE=TRUE
8	NC_TP_GP_PCIE_TX3_N	NC_TP_GP_PCIE_TX3_N	MAKE_BASE=TRUE
8	NC_TP_GP_PCIE_RX3_P	NC_TP_GP_PCIE_RX3_P	MAKE_BASE=TRUE
8	NC_TP_GP_PCIE_RX3_N	NC_TP_GP_PCIE_RX3_N	MAKE_BASE=TRUE
8	NC_TP_GP_PCIE_TX2_P	NC_TP_GP_PCIE_TX2_P	MAKE_BASE=TRUE
8	NC_TP_GP_PCIE_TX2_N	NC_TP_GP_PCIE_TX2_N	MAKE_BASE=TRUE
8	NC_TP_GP_PCIE_RX2_P	NC_TP_GP_PCIE_RX2_P	MAKE_BASE=TRUE
8	NC_TP_GP_PCIE_RX2_N	NC_TP_GP_PCIE_RX2_N	MAKE_BASE=TRUE
8	NC_TP_GP_PCIE_REF_CLK2_P	NC_TP_GP_PCIE_REF_CLK2_P	MAKE_BASE=TRUE
8	NC_TP_GP_PCIE_REF_CLK2_N	NC_TP_GP_PCIE_REF_CLK2_N	MAKE_BASE=TRUE
8	NC_TP_GP_PCIE_CLKREQ2_L	NC_TP_GP_PCIE_CLKREQ2_L	MAKE_BASE=TRUE
8	NC_TP_GP_PCIE_PERST2_L	NC_TP_GP_PCIE_PERST2_L	MAKE_BASE=TRUE

NC SPN's

84	UPC_DFU_BOOTED_L	UPC_DFU_BOOTED_L	6
		MAKE_BASE=TRUE	
6	NC_AP_I2S0_MCK	NC_AP_I2S0_MCK	MAKE_BASE=TRUE
6	NC_AP_I2S1_MCK	NC_AP_I2S1_MCK	MAKE_BASE=TRUE
6	SOC_DOMAIN_GPIO_GRP1_1	SOC_DOMAIN_GPIO_GRP1_1	157 MAKE_BASE=TRUE
6	NC_AP_SPI2_SSIN	NC_AP_SPI2_SSIN	MAKE_BASE=TRUE
7	NC_DISP_POL	NC_DISP_POL	MAKE_BASE=TRUE

SOC GPIO TPs BY DOMAIN

Nonused SOC pins pulled out by functional/power domains

157 SOC_DOMAIN_GPIO_GRP1_1 — SM P2MM PLACE_SIDE=TOP 1 PP — PPZZ05

157 SOC_DOMAIN_MGPIO_AOP1 — SM P2MM PLACE_SIDE=TOP 1 PP — PPZZ11

157 SOC_DOMAIN_NGPIO_AOP1_0 — SM P2MM PLACE_SIDE=TOP 1 PP — PPZZ02

157 SOC_DOMAIN_HGPIO_GRP0_0 — SM P2MM PLACE_SIDE=TOP 1 PP — PPZZ08

157 SOC_DOMAIN_HGPIO_GRP0_1 — SM P2MM PLACE_SIDE=TOP 1 PP — PPZZ10

157 SOC_DOMAIN_SGPIO_GRP1 — SM P2MM PLACE_SIDE=TOP 1 PP — PPZZ12

Unrealized Test Points

6	NC_AP_GPIO35	NC_AP_GPIO35	MAKE_BASE=TRUE
6	NC_AP_GPIO36	NC_AP_GPIO36	MAKE_BASE=TRUE
6	NC_AP_UART2_R2D	NC_AP_UART2_R2D	MAKE_BASE=TRUE
6	NC_AP_UART2_D2R	NC_AP_UART2_D2R	MAKE_BASE=TRUE
6	NC_AP_UART2_R2D_RTS_L	NC_AP_UART2_R2D_RTS_L	MAKE_BASE=TRUE
6	NC_AP_UART2_D2R_CTS_L	NC_AP_UART2_D2R_CTS_L	MAKE_BASE=TRUE
6	NC_AP_I2S2_MCK	NC_AP_I2S2_MCK	MAKE_BASE=TRUE
6	NC_AP_I2S3_DIN	NC_AP_I2S3_DIN	MAKE_BASE=TRUE
6	NC_AP_I2S3_DOUT	NC_AP_I2S3_DOUT	MAKE_BASE=TRUE
6	NC_AP_I2S3_BCLK	NC_AP_I2S3_BCLK	MAKE_BASE=TRUE
6	NC_AP_I2S3_LRCK	NC_AP_I2S3_LRCK	MAKE_BASE=TRUE
7	NC_LPDPRX_AUX_D0P	NC_LPDPRX_AUX_D0P	MAKE_BASE=TRUE
7	NC_SENSOR0_CLK	NC_SENSOR0_CLK	MAKE_BASE=TRUE
10	NC_AOP_UART2_RXD	NC_AOP_UART2_RXD	MAKE_BASE=TRUE
10	NC_AOP_UART2_TXD	NC_AOP_UART2_TXD	MAKE_BASE=TRUE
10	NC_NUB_GPIO0	NC_NUB_GPIO0	MAKE_BASE=TRUE
10	NC_NUB_GPIO6	NC_NUB_GPIO6	MAKE_BASE=TRUE

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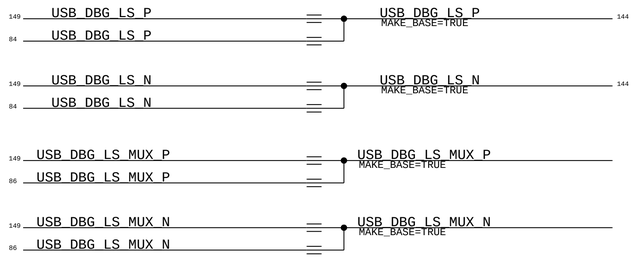
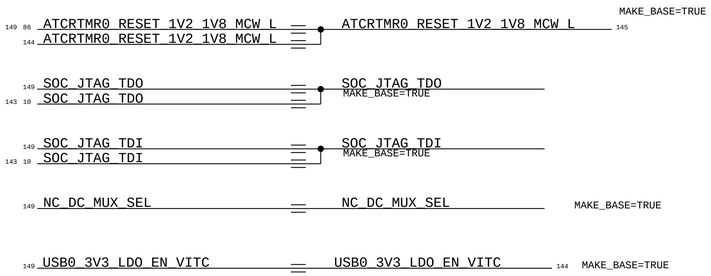
USB LEVEL SHIFTER

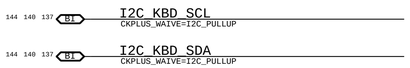


VITAMIN C

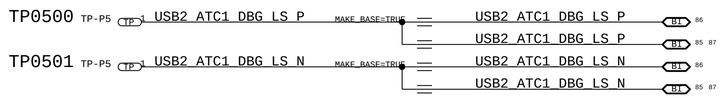


ATC3 NC NETS

I2C CKPLUS WAIVER



DUAL KIS ONLY aliases



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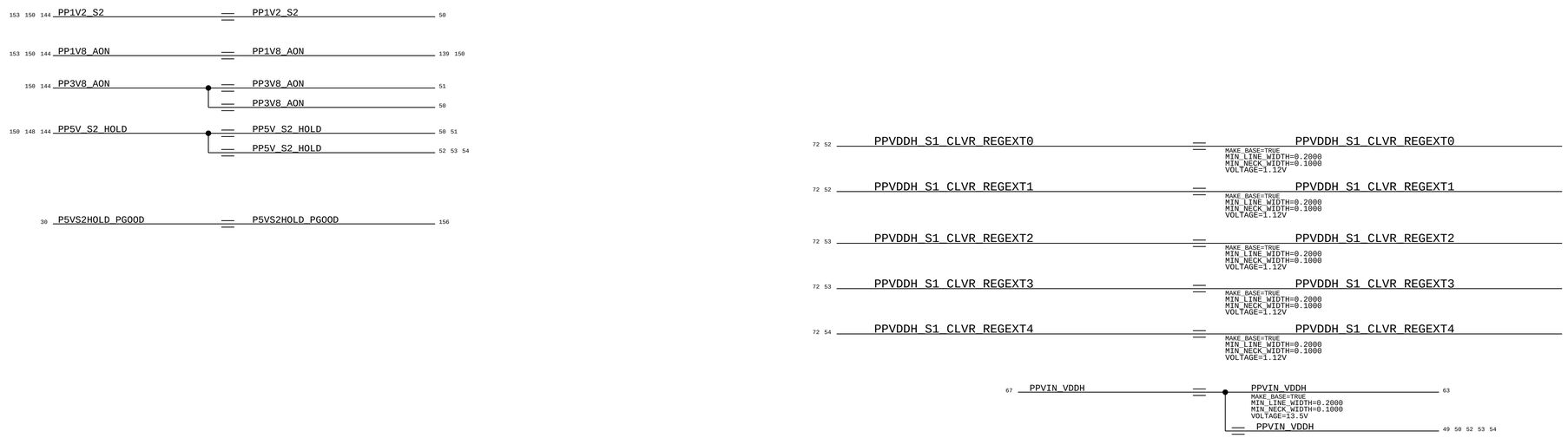

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SCSET RULES

DIELECTRIC BASED SPACING RULES	
RULE DEFINITION	LIST OF VALUES
A_DIELECTRIC_{N}X Calculates dielectric distance from stackup, shortest distance is used unless 'L' is defined	EXAMPLE: 1,3-5,7L,8L-10L 2-10
A_DIELECTRIC_{N}XD XV,XVL,X Calculates dielectric distance from hybrid table and stackup, shortest distance is used unless 'L' defined	EXAMPLE: 2,10,30,50,60,70,100 PLEASE USE HYBRID TABLE
A_DIELECTRIC_{N}XIN_{N}XOUT Calculates dielectric distance from stackup, shortest distance is used unless 'L' is defined	EXAMPLE: 2,4,5L,3L

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SOC Socket for DC-DC Tests

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
939-13907	1	PCBA,DUNHUANG,X2406	U0600	CRITICAL	SOC:SOCKET
998-28204	1	IC,PALMA CGA,DEV,BGA4550	U0600	CRITICAL	SOC:TEST

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:

SOC/CPU Palma-M

998-32491	1	SOC,PAM B1+36G,1A,10C,BIN4,LP,BX,M,B4550		U0600	CRITICAL	SOC:30FSTP_36G
998-32493	998-32491	ANY	ALL	B1,10C,36G,BIN7,HP.M		B1,10C,BIN7,HP,Micron 36GB DRAM
998-32495	998-32491	ANY	ALL	B1,10C,36G,BIN4,LP,S		B1,10C,BIN4,LP,Samsung 36GB DRAM
998-32497	998-32491	ANY	ALL	B1,10C,36G,BIN7,HP,S		B1,10C,BIN7,HP,Samsung 36GB DRAM
998-32505	998-32491	ANY	ALL	B1,10C,36G,BIN4,LP,H		B1,10C,BIN4,LP,Hynix 36GB DRAM
998-32507	998-32491	ANY	ALL	B1,10C,36G,BIN7,HP,H		B1,10C,BIN7,HP,Hynix 36GB DRAM
998-31759	998-32491	ANY	ALL	B0,10C,36G,BIN4,LP,M		B0,10C,BIN4,LP,Micron 36GB DRAM
998-31761	998-32491	ANY	ALL	B0,10C,36G,BIN7,HP,M		B0,10C,BIN7,HP,Micron 36GB DRAM
998-31763	998-32491	ANY	ALL	B0,10C,36G,BIN4,LP,S		B0,10C,BIN4,LP,Samsung 36GB DRAM
998-31765	998-32491	ANY	ALL	B0,10C,36G,BIN7,HP,S		B0,10C,BIN7,HP,Samsung 36GB DRAM
998-31129	998-32491	ANY	ALL	B0,10C,36G,BIN4,BX,M		B0,10C,BIN4,BX,V05x,Micron 36GB DRAM
998-32492	1	SOC,PAM B1+96G,1A,10C,BIN4,LP,BX,M,B4550		U0600	CRITICAL	SOC:30FSTP_96G
998-32494	998-32492	ANY	ALL	B1,10C,96G,BIN7,HP,M		B1,10C,BIN7,HP,Micron 96GB DRAM
998-32496	998-32492	ANY	ALL	B1,10C,96G,BIN4,LP,S		B1,10C,BIN4,LP,Samsung 96GB DRAM
998-32498	998-32492	ANY	ALL	B1,10C,96G,BIN7,HP,S		B1,10C,BIN7,HP,Samsung 96GB DRAM
998-32506	998-32492	ANY	ALL	B1,10C,96G,BIN4,LP,H		B1,10C,BIN4,LP,Hynix 96GB DRAM
998-32508	998-32492	ANY	ALL	B1,10C,96G,BIN7,HP,H		B1,10C,BIN7,HP,Hynix 96GB DRAM
998-31760	998-32492	ANY	ALL	B0,10C,96G,BIN4,LP,M		B0,10C,BIN4,LP,Micron 96GB DRAM
998-31762	998-32492	ANY	ALL	B0,10C,96G,BIN7,HP,M		B0,10C,BIN7,HP,Micron 96GB DRAM
998-31764	998-32492	ANY	ALL	B0,10C,96G,BIN4,LP,S		B0,10C,BIN4,LP,Samsung 96GB DRAM
998-31766	998-32492	ANY	ALL	B0,10C,96G,BIN7,HP,S		B0,10C,BIN7,HP,Samsung 96GB DRAM
998-31130	998-32492	ANY	ALL	B0,10C,96G,BIN4,BX,M		B0,10C,BIN4,BX,V05x,Micron 96GB DRAM

SOC/CPU Palma-C

998-32479	1	SOC,PAC B1+48G,1A,12C,BIN1,LP,BX,M,B4550		U0600	CRITICAL	SOC:40FSTP_48G
998-32482	998-32479	ANY	ALL	B1,12C,48G,BIN5,HP.M		B1,12C,BIN5,HP,Micron 48GB DRAM
998-32485	998-32479	ANY	ALL	B1,12C,48G,BIN1,LP,S		B1,12C,BIN1,LP,Samsung 48GB DRAM
998-32488	998-32479	ANY	ALL	B1,12C,48G,BIN5,HP,S		B1,12C,BIN5,HP,Samsung 48GB DRAM
998-32499	998-32479	ANY	ALL	B1,12C,48G,BIN1,LP,H		B1,12C,BIN1,LP,Hynix 48GB DRAM
998-32502	998-32479	ANY	ALL	B1,12C,48G,BIN5,HP,H		B1,12C,BIN5,HP,Hynix 48GB DRAM
998-31747	998-32479	ANY	ALL	B0,12C,48G,BIN1,LP,M		B0,12C,BIN1,LP,Micron 48GB DRAM
998-31750	998-32479	ANY	ALL	B0,12C,48G,BIN5,HP,M		B0,12C,BIN5,HP,Micron 48GB DRAM
998-31753	998-32479	ANY	ALL	B0,12C,48G,BIN1,LP,S		B0,12C,BIN1,LP,Samsung 48GB DRAM
998-31756	998-32479	ANY	ALL	B0,12C,48G,BIN5,HP,S		B0,12C,BIN5,HP,Samsung 48GB DRAM
998-31111	998-32479	ANY	ALL	B0,12C,48G,BIN1,BX,M		B0,12C,BIN1,V05x,Micron 48GB DRAM
998-31120	998-32479	ANY	ALL	B0,12C,48G,BIN1,BX,S		B0,12C,BIN1,V05x,Samsung 48GB DRAM
998-32480	1	SOC,PAC B1+64G,1A,12C,BIN1,LP,BX,M,B4550		U0600	CRITICAL	SOC:40FSTP_64G
998-32483	998-32480	ANY	ALL	B1,12C,64G,BIN5,HP,M		B1,12C,BIN5,HP,Micron 64GB DRAM
998-32486	998-32480	ANY	ALL	B1,12C,64G,BIN1,LP,S		B1,12C,BIN1,LP,Samsung 64GB DRAM
998-32489	998-32480	ANY	ALL	B1,12C,64G,BIN5,HP,S		B1,12C,BIN5,HP,Samsung 64GB DRAM
998-32500	998-32480	ANY	ALL	B1,12C,64G,BIN1,LP,H		B1,12C,BIN1,LP,Hynix 64GB DRAM
998-32503	998-32480	ANY	ALL	B1,12C,64G,BIN5,HP,H		B1,12C,BIN5,HP,Hynix 64GB DRAM
998-31748	998-32480	ANY	ALL	B0,12C,64G,BIN1,LP,M		B0,12C,BIN1,LP,Micron 64GB DRAM
998-31751	998-32480	ANY	ALL	B0,12C,64G,BIN5,HP.M		B0,12C,BIN5,HP,Micron 64GB DRAM
998-31754	998-32480	ANY	ALL	B0,12C,64G,BIN1,LP.S		B0,12C,BIN1,LP,Samsung 64GB DRAM
998-31757	998-32480	ANY	ALL	B0,12C,64G,BIN5,HP.S		B0,12C,BIN5,HP,Samsung 64GB DRAM
998-31112	998-32480	ANY	ALL	B0,12C,64G,BIN1,BX.M		B0,12C,BIN1,V05X,Micron 64GB DRAM
998-31121	998-32480	ANY	ALL	B0,12C,64G,BIN1,BX.S		B0,12C,BIN1,V05X,Samsung 64GB DRAM
998-32481	1	SOC,PAC B1+128G,1A,12C,BN1,LP,BX,M,B4550		U0600	CRITICAL	SOC:40FSTP_128G
998-32484	998-32481	ANY	ALL	B1,12C,128G,BIN5,HP,M		B1,12C,BIN5,HP,Micron 128GB DRAM
998-32487	998-32481	ANY	ALL	B1,12C,128G,BIN1,LP,S		B1,12C,BIN1,LP,Samsung 128GB DRAM
998-32490	998-32481	ANY	ALL	B1,12C,128G,BIN5,HP,S		B1,12C,BIN5,HP,Samsung 128GB DRAM
998-32501	998-32481	ANY	ALL	B1,12C,128G,BIN1,LP,H		B1,12C,BIN1,LP,Hynix 128GB DRAM
998-32504	998-32481	ANY	ALL	B1,12C,128G,BIN5,HP,H		B1,12C,BIN5,HP,Hynix 128GB DRAM
998-31749	998-32481	ANY	ALL	B0,12C,128G,BIN1,LP,M		B0,12C,BIN1,LP,Micron 128GB DRAM
998-31752	998-32481	ANY	ALL	B0,12C,128G,BIN5,HP.M		B0,12C,BIN5,HP,Micron 128GB DRAM
998-31755	998-32481	ANY	ALL	B0,12C,128G,BIN1,LP.S		B0,12C,BIN1,LP,Samsung 128GB DRAM
998-31758	998-32481	ANY	ALL	B0,12C,128G,BIN5,HP.S		B0,12C,BIN5,HP,Samsung 128GB DRAM
998-31113	998-32481	ANY	ALL	B0,12C,128G,BIN1,BX.M		B0,12C,BIN1,V05X, Micron 128GB DRAM
998-31122	998-32481	ANY	ALL	B0,12C,128G,BIN1,BX.S		B0,12C,BIN1,V05X,Samsung 128GB DRAM

NAND PARTS

512GB-4L

335S00551	4	NAND,BC5T,128GB,S5E,11.0,512G,K,ULGA315	UN000,UN100,UN200,UN300	CRITICAL	NAND:KX-512-4L
335S00619	4	NAND,BC5T,128GB,S5E,11.0,512G,W,ULGA315	UN000,UN100,UN200,UN300	CRITICAL	NAND:WD-512-4L

1TB-4L

335S00652	4	NAND,BICS5,256GB,S5E,XX.X,512G,K,SLGA315	UN000,UN100,UN200,UN300	CRITICAL	NAND:KX-1TB-4L
335S00581	4	NAND,3DV7T,256GB,S5E,17.0,512G,H,ULGA315	UN000,UN100,UN200,UN300	CRITICAL	NAND:HY-1TB-4L

2TB-4L

335S00653	4	NAND,BICS5,512GB,S5E,XX.X,512G,K,SLGA315	UN000,UN100,UN200,UN300	CRITICAL	NAND:KX-2TB-4L
335S00583	4	NAND,3DV7T,512GB,S5E,17.0,512G,H,ULGA315	UN000,UN100,UN200,UN300	CRITICAL	NAND:HY-2TB-4L

4TB-8L

335S00553	4	NAND,BC5T,512GB,S5E,XX.X,512G,K,ULGA315	UN000,UN100,UN200,UN300	CRITICAL	NAND:KX-4TB-8L
335S00553	4	NAND,BC5T,512GB,S5E,XX.X,512G,K,ULGA315	UN500,UN600,UN700,UN800	CRITICAL	NAND:KX-4TB-8L
335S00583	4	NAND,3DV7T,512GB,S5E,17.0,512G,H,ULGA315	UN000,UN100,UN200,UN300	CRITICAL	NAND:HY-4TB-8L
335S00583	4	NAND,3DV7T,512GB,S5E,17.0,512G,H,ULGA315	UN500,UN600,UN700,UN800	CRITICAL	NAND:HY-4TB-8L

8TB-8L

335S00643	4	NAND,BICS6,1TB,S5E,XX.X,1TB,K,ULGA315	UN000,UN100,UN200,UN300	CRITICAL	NAND:KX-8TB-8L
335S00643	4	NAND,BICS6,1TB,S5E,XX.X,1TB,K,ULGA315	UN500,UN600,UN700,UN800	CRITICAL	NAND:KX-8TB-8L
335S00610	4	NAND,3DV7T,1TB,S5E,17.0,512G,H,MLGA315	UN000,UN100,UN200,UN300	CRITICAL	NAND:HY-8TB-8L
335S00610	4	NAND,3DV7T,1TB,S5E,17.0,512G,H,MLGA315	UN500,UN600,UN700,UN800	CRITICAL	NAND:HY-8TB-8L

NAND SOCKET

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
939-11766	4	PCBA,MANAS,X2371	UN000	CRITICAL	NAND:SOCKET
939-11766	4	PCBA,MANAS,X2371	UN500	CRITICAL	NAND:SOCKET

1TB-4L-NONPOR

335S00552	4	NAND,BC5T,256GB,S5E,XX.X,512G,K,ULGA315	UN000,UN100,UN200,UN300	CRITICAL	NAND:KX-1TB-4L-NONPOR

2TB-4L-NONPOR

335S00553	4	NAND,BC5T,512GB,S5E,XX.X,512G,K,ULGA315	UN000,UN100,UN200,UN300	CRITICAL	NAND:KX-2TB-4L-NONPOR

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BOM OPTION - SOC,NAND

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SOC and Re-timer ROM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S00574	4	IC,FLASH,64MBIT,1.2V,QE=1,W,4X4MM,SON8	U1910,UF090,UF190,UG090	CRITICAL	SOC_ATCRTMR_ROM:WINDBOND_MP

SOC and Re-timer ROM ALT parts

PART NUMBER	ALTERNATE_FOR PART NUMBER	REFERENCE DESIGNATOR(S)	DESCRIPTION	BOM OPTION
335S00575	335S00574	U1910,UF090,UF190,UG090	MACRONIX FLASH	
335S00596	335S00574	U1910,UF090,UF190,UG090	MACRONIX FLASH	

ACE3

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S02973	4	IC,SN2012024,ACE3,A0,USB,PD	UF400,UF500,UG400	CRITICAL	USBCPC:ACE3_A0
353S03507	4	IC,SN2012024,ACE3,A1,USBPD W/28HV,BGA149	UF400,UF500,UG400	CRITICAL	USBCPC:ACE3_A1

ATC5 U5500 CSA55 BOM Table on CSA55

Programmble parts: ACE ROMs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	
341S02256	1	ROM,ACE-P0 (V2.124.0.1) PROTO-1,X2293	UF260	CRITICAL	ACE_ROM:P1BUA	<-LEFT
341S02257	1	ROM,ACE-P1 (V2.124.0.1) PROTO-1,X2293	UF250	CRITICAL	ACE_ROM:P1BUA	<-LEFT
341S02258	1	ROM,ACE-P2 (V2.124.0.1) PROTO-1,X2293	UG260	CRITICAL	ACE_ROM:P1BUA	<-RIGHT
341S02259	1	ROM,ACE-P5 (V2.124.0.1) PROTO-1,X2293	U5660	CRITICAL	ACE_ROM:P1BUA	<-MAGSAFE
335S00644	4	ROM,ACE,BLANK	UF250,UF260,UG260,U5660	CRITICAL	ACE_ROM:BLANK	

Update when available

ACE BOM BLANK ALT parts

PART NUMBER	ALTERNATE_FOR PART NUMBER	REFERENCE DESIGNATOR(S)	DESCRIPTION	BOM OPTION
335S00537	335S00644	UF250,UF260,UG260,U5660	BLANK FLASH	ACE_ROM:BLANK

Programmble parts: ACE ROMs (Build P2)

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	
341S02005	1	ROM,ACE-P0 (V2.124.0.1) PROTO-1,X2293	UF260	CRITICAL	ACE_ROM:P2	<-LEFT
341S02006	1	ROM,ACE-P1 (V2.124.0.1) PROTO-1,X2293	UF250	CRITICAL	ACE_ROM:P2	<-LEFT
341S02007	1	ROM,ACE-P2 (V2.124.0.1) PROTO-1,X2293	UG260	CRITICAL	ACE_ROM:P2	<-RIGHT
341S02008	1	ROM,ACE-P5 (V2.124.0.1) PROTO-1,X2293	U5660	CRITICAL	ACE_ROM:P2	<-MAGSAFE

HDMI COBRA

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-25553	1	IC,COBRA,A0,DP TO HDMI CNVTR,DEV,BGA120	UH700	CRITICAL	COBRA:A0_CFG1
338S00772	1	IC,COBRA,PS190,DP TO HDMI CONVTR,A0,BGA120	UH700	CRITICAL	COBRA:A0_CFG2
998-29948	1	IC,COBRA,A1,DP TO HDMI CNVTR,DEV,BGA120	UH700	CRITICAL	COBRA:A1_CFG1
338S00957	1	IC,COBRA,PS190,DP TO HDMI,A1,BGA120	UH700	CRITICAL	COBRA:A1_CFG2

SD CARD CONNECTOR

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
514-00180	1	CONN,RCPT,SD,X2094	JK600	CRITICAL	

OCARINA0

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S00600	1	IC,PMU,OCARINA,D2499A0,OPT-BC,WLCSP56	UN400	CRITICAL	OCARINA0:A0_OTPBC

OCARINA1

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S00600	1	IC,PMU,OCARINA,D2499A0,OPT-BC,WLCSP56	UN900	CRITICAL	OCARINA1:A0_OTPBC

IPD

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S00113	2	RES,TK,20 OHM,5%,1/20W,0201	RT36B,RT352,RT361,RT362	CRITICAL	IPD_SPI_CS_R:20_OHM
118S00521	5	RES,TK, 30K OHM,1%,1/20W,0201	RT350,RT363,RT341,RT371	CRITICAL	TPAD_SOC_PULLUP:30K

MANDOLA

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-28081	1	IC,RAA489901,PMIC,MANDOLA,OTP-1,WCSP40	U5200	CRITICAL	MANDOLA:3A_A0
998-31085	1	IC,RAA489901,PMIC,MANDOLA,OTP-3,WCSP40	U5200	CRITICAL	MANDOLA:3A_A1_OTP-3
998-31512	1	IC,RAA489901,PMIC,MANDOLA,OTP-4,WCSP40	U5200	CRITICAL	MANDOLA:3A_A1_OTP-4
998-32440	1	IC,RAA489901,PMIC,MANDOLA,OTP-8,WCSP40	U5200	CRITICAL	MANDOLA:3A_A1_OTP-8

Mandola/ Whamola AUX_SHORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S00090	1	RES,TK,10K OHM,5%,1/20W,0201	R5201	CRITICAL	AUX_SHORT_MANDOLA
117S00073	1	RES,TK,0 OHM,1A MAX,1/20W,0201	R5201	CRITICAL	AUX_SHORT_WHAMOLA

Multi-protocol Retimer (Lifuka)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
998-21959	3	IC,RTMR,A0,USB-C RETIMER,FCCSP154	UF000,UF100,UG000	CRITICAL	ATCRTMR:A0
998-25504	3	IC,RTMR,B0,USB-C RETIMER,CSP154	UF000,UF100,UG000	CRITICAL	ATCRTMR:B0
338S00773	3	IC,RTMR,B0,USB-C RETIMER,CSP154	UF000,UF100,UG000	CRITICAL	ATCRTMR:B0_MP
998-27476	3	IC,LIFUKA,B1,USB-C RETIMER,DEV,CSP154	UF000,UF100,UG000	CRITICAL	ATCRTMR:B1_DEV
998-30147	3	IC,LIFUKA,B2,USBC RETIMER,DEV,AXX,CSP154	UF000,UF100,UG000	CRITICAL	ATCRTMR:B2_DEV

eUSB level shifter

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S00908	3	IC,MACAW,CYUSB2402,A3,CSP24	UF600,UF650,UG650	CRITICAL	MACAW:A3

Re-timer Sequencer

UF790 - CSA157, UG790 - CSA167 Locally defined

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
131S0852	1	CAP,CER,C0G,12PF,5%,25V,0201	CR610,CR611	SPKRAMP_A_DESENSE
131S0852	1	CAP,CER,C0G,12PF,5%,25V,0201	CR640,CR641	SPKRAMP_B_DESENSE
131S0852	1	CAP,CER,C0G,12PF,5%,25V,0201	CR670,CR671	SPKRAMP_C_DESENSE
131S0852	1	CAP,CER,C0G,12PF,5%,25V,0201	CR710,CR711	SPKRAMP_D_DESENSE
131S0852	1	CAP,CER,C0G,12PF,5%,25V,0201	CR740,CR741	SPKRAMP_E_DESENSE
131S0852	1	CAP,CER,C0G,12PF,5%,25V,0201	CR770,CR771	SPKRAMP_F_DESENSE

SYNC_MASTER=MLB_S_0.64.4 SYNC_DATE=02/27/2023

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BOM OPTION TABLES

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MLB Common/Dev BOMs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
685-00481	1	COMMON PARTS,MLB-C,X2407	BASE	CRITICAL	BOM_BASE
985-01814	1	DEV PARTS,MLB-C,X2407	DEVEL	CRITICAL	BOM_DEV

MLB Common/Dev BOM Definitions

BOM NUMBER	BOM NAME	BOM OPTIONS
685-00481	COMMON PARTS,MLB-C,X2407	X2407_COMMON
985-01814	DEV PARTS,MLB-C,X2407	X2407_DEVEL:ENG,ALTERNATE
985-02025	DEV PARTS,SEPCIAL CONFIG,MLB-C,X2407	X2407_PVT,ALTERNATE

MLB Common BOM Groups

BOM GROUP	BOM OPTIONS
X2407_COMMON	SCH,PCB,COMMON,ALTERNATE:INSTANCE,X2407_COMMON1,X2407_COMMON2,X2407_COMMON3,X2407_PROGPARTS
X2407_COMMON1	BOARD_ID:0x06,BOARD_REV:4,X2407_SOC,X2407_USBC,X2407_HDMI,X2407_PWR,X2407_BLC
X2407_COMMON2	RF_CONN,X2407_SE,REFSECDIS_SOC_PU:30K,IPD_MTP_FUNC1_CIRCUIT:NO,VITAMIN-C:NO
X2407_COMMON3	REFIMU_RE400:30K,REFIMU_IC:BMI286,IPD_SPI_CS_R:20_OHM,TPAD_SOC_PULLUP:30K
X2407_PROGPARTS	ACE_ROM:BLANK,SOC_ATCRTMR_ROM:WINDBOND_MP,ATCRTMR:B2_DEV
X2407_SOC	DEV_DFU:TADFU,SEPROM_1V8:SYS,BOOTCFG2,BOOTCFG1
X2407_USBC	ACE3:28V,MACAW:A3,USBCPC:ACE3_A1,SYS_BOOT_PWR:DISABLED,STRAP2_LS:NO,LFKA_TEST_MODE:NO
X2407_HDMI	DATA_FILT,HDMI_CL_FILT:YES,HDMI_ROM:512,LDO_HDMI:5V,COBRAPART:0,COBRA:A1_CFG2,HDMICONN:PORTABLES_16_BTN2
X2407_BLC	BLC_KBD_BEN_IC:V4,BLC_KBD_5V_SERIES:10_OHM,BLC_KBD_5V_CAP:4P7_UF
X2407_SE	JUNO:A0_PROD
X2407_PWR	X2407_5VS2TPS,P5VUSB_DSCHG,X2407_SPITFIRE,X2407_CHAPEL,X2407_ICEMAN,X2407_MANDOLA
X2407_SPITFIRE	
X2407_CHAPEL	SOC:C,CHAPEL_PORTABLES
X2407_ICEMAN	P3V8AON_IC:A2_BOM2_R0C1,P3V8ILIM:BOM2_5V,P3V8AON_LPM
X2407_MANDOLA	MANDOLA:3A_A1_OTP-8,3V8_DLY:YES,ACEFWDB:POR,WHAMOLA_OPTION:NO,AUX_SHORT_MANDOLA
X2407_5VS2TPS	5VS2TPS_VOUT:5V232

Items to Load on PVT When X2407_DEVEL:ENG is not loaded

BOM GROUP	BOM OPTIONS
X2407_PVT	USBC_DUAL_DFU:NO,USBC_DUAL_KIS:NO

Dev BOM Groups

BOM GROUP	BOM OPTIONS
X2407_DEVEL:ENG	DBG:FAN,USBC_DBG,USBC_DUAL_KIS:YES,USBC_DUAL_DFU:YES

Board Revs

BOM GROUP	Build	BOM OPTIONS	Nibble
BOARD_REV:0	P0c	BOARDREV3,BOARDREV2,BOARDREV1,BOARDREV0	0x0000
BOARD_REV:1	P1c	BOARDREV3,BOARDREV2,BOARDREV1	0x0001
BOARD_REV:2	P2c	BOARDREV3,BOARDREV2,BOARDREV0	0x0010
BOARD_REV:3	EVTc	BOARDREV3,BOARDREV2	0x0011
BOARD_REV:4	DVTc	BOARDREV3,BOARDREV1,BOARDREV0	0x0100
BOARD_REV:5	PrePVTc	BOARDREV3,BOARDREV1	0x0101
BOARD_REV:6	PVTc	BOARDREV3,BOARDREV0	0x0110

Board ID

MLB_S Board ID is 0x06 (rdar://89371301)

BOM GROUP	BOM OPTIONS
BOARD_ID:0x06	BOARDID2,BOARDID1
BOARD_ID:0x1F	BOARDID4,BOARDID3,BOARDID2,BOARDID1,BOARDID0

**** No More 5 Landings. UPDATE

SSD Config Table

Controls NAND ICs and SSD support BOMs

BOM GROUP	Landings	BOM OPTIONS
SSD:KX-512-4L	4	NAND:KX-512-4L,OCARINA0:A0_OTPBC,BOM_SSD:4L
SSD:WD-512-4L	4	NAND:WD-512-4L,OCARINA0:A0_OTPBC,BOM_SSD:4L
SSD:KX-1TB-4L	4	NAND:KX-1TB-4L,OCARINA0:A0_OTPBC,BOM_SSD:4L
SSD:KX-1TB-4L-NONPOR	4	NAND:KX-1TB-4L-NONPOR,OCARINA0:A0_OTPBC,BOM_SSD:4L
SSD:WD-1TB-4L	4	NAND:WD-1TB-4L,OCARINA0:A0_OTPBC,BOM_SSD:4L
SSD:HY-1TB-4L	4	NAND:HY-1TB-4L,OCARINA0:A0_OTPBC,BOM_SSD:4L
SSD:KX-2TB-4L	4	NAND:KX-2TB-4L,OCARINA0:A0_OTPBC,BOM_SSD:4L
SSD:KX-2TB-4L-NONPOR	4	NAND:KX-2TB-4L-NONPOR,OCARINA0:A0_OTPBC,BOM_SSD:4L
SSD:HY-2TB-4L	4	NAND:HY-2TB-4L,OCARINA0:A0_OTPBC,BOM_SSD:4L
SSD:KX-4TB-8L	8	NAND:KX-4TB-8L,OCARINA0:A0_OTPBC,OCARINA1:A0_OTPBC,BOM_SSD:8L
SSD:HY-4TB-8L	8	NAND:HY-4TB-8L,OCARINA0:A0_OTPBC,OCARINA1:A0_OTPBC,BOM_SSD:8L
SSD:KX-8TB-8L	8	NAND:KX-8TB-8L,OCARINA0:A0_OTPBC,OCARINA1:A0_OTPBC,BOM_SSD:8L
SSD:HY-8TB-8L	8	NAND:HY-8TB-8L,OCARINA0:A0_OTPBC,OCARINA1:A0_OTPBC,BOM_SSD:8L
SSD:NOS5E	0	
SSD:8L-DCDC	8	OCARINA0:A0_OTPBC,OCARINA1:A0_OTPBC,BOM_SSD:8L

SSD Support BOMs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
685-00526	1	BOM,SSD_2_LAND,MLB_C,X2407	SSD	CRITICAL	BOM_SSD:2L
685-00527	1	BOM,SSD_4_LAND,MLB_C,X2407	SSD	CRITICAL	BOM_SSD:4L
685-00528	1	BOM,SSD_8_LAND,MLB_C,X2407	SSD	CRITICAL	BOM_SSD:8L

SSD Support BOM Definitions

BOM NUMBER	BOM NAME	BOM OPTIONS
685-00526	SSD_2L,MLB_C,X2407	ALTERNATE,SSD_SUPPORT:L2
685-00527	SSD_4L,MLB_C,X2407	ALTERNATE,SSD_SUPPORT:L4
685-00528	SSD_8L,MLB_C,X2407	ALTERNATE,SSD_SUPPORT:L8

SSD Support BOM Groups

BOM GROUP	BOM OPTIONS
SSD_SUPPORT:L2	SSD_2L
SSD_SUPPORT:L4	SSD_2L,SSD_4L,SSD_BRANCH_2L
SSD_SUPPORT:L8	SSD_OC1VR1,SSD_2L,SSD_4L,SSD_8L,SSD_BRANCH_2L

SYNC_MASTER=MLB_S_0.64.4 SYNC_DATE=02/27/2023

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BOM GROUPS

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BOM VARIANT TABLES

SOC 10C 36GB FSTP30

BOM NUMBER	BOM NAME	BOM OPTIONS
639-17779	PCBA,MLB-C,10C,36GB,FSTP-30,KX-512,X2407	BOM_BASE,BOM_DEV,ALTERNATE,SOC:30FSTP_36G,SSD:KX-512-4L
639-17780	PCBA,MLB-C,10C,36GB,FSTP-30,WD-512,X2407	BOM_BASE,BOM_DEV,ALTERNATE,SOC:30FSTP_36G,SSD:WD-512-4L
639-17781	PCBA,MLB-C,10C,36GB,FSTP-30,KX-1TB,X2407	BOM_BASE,BOM_DEV,ALTERNATE,SOC:30FSTP_36G,SSD:KX-1TB-4L
639-17783	PCBA,MLB-C,10C,36GB,FSTP-30,HY-1TB,X2407	BOM_BASE,BOM_DEV,ALTERNATE,SOC:30FSTP_36G,SSD:HY-1TB-4L
639-17784	PCBA,MLB-C,10C,36GB,FSTP-30,KX-2TB,X2407	BOM_BASE,BOM_DEV,ALTERNATE,SOC:30FSTP_36G,SSD:KX-2TB-4L
639-17785	PCBA,MLB-C,10C,36GB,FSTP-30,HY-2TB,X2407	BOM_BASE,BOM_DEV,ALTERNATE,SOC:30FSTP_36G,SSD:HY-2TB-4L
639-17786	PCBA,MLB-C,10C,36GB,FSTP-30,KX-4TB,X2407	BOM_BASE,BOM_DEV,ALTERNATE,SOC:30FSTP_36G,SSD:KX-4TB-8L
639-17787	PCBA,MLB-C,10C,36GB,FSTP-30,HY-4TB,X2407	BOM_BASE,BOM_DEV,ALTERNATE,SOC:30FSTP_36G,SSD:HY-4TB-8L
639-17789	PCBA,MLB-C,10C,36GB,FSTP-30,KX-8TB,X2407	BOM_BASE,BOM_DEV,ALTERNATE,SOC:30FSTP_36G,SSD:KX-8TB-8L
639-17791	PCBA,MLB-C,10C,36GB,FSTP-30,HY-8TB,X2407	BOM_BASE,BOM_DEV,ALTERNATE,SOC:30FSTP_36G,SSD:HY-8TB-8L

SOC 12C 48GB FSTP40

BOM NUMBER	BOM NAME	BOM OPTIONS
639-17803	PCBA,MLB-C,12C,48GB,FSTP-40,KX-512,X2407	BOM_BASE,BOM_DEV,ALTERNATE,SOC:40FSTP_48G,SSD:KX-512-4L
639-17804	PCBA,MLB-C,12C,48GB,FSTP-40,WD-512,X2407	BOM_BASE,BOM_DEV,ALTERNATE,SOC:40FSTP_48G,SSD:WD-512-4L
639-17805	PCBA,MLB-C,12C,48GB,FSTP-40,KX-1TB,X2407	BOM_BASE,BOM_DEV,ALTERNATE,SOC:40FSTP_48G,SSD:KX-1TB-4L
639-17807	PCBA,MLB-C,12C,48GB,FSTP-40,HY-1TB,X2407	BOM_BASE,BOM_DEV,ALTERNATE,SOC:40FSTP_48G,SSD:HY-1TB-4L
639-17808	PCBA,MLB-C,12C,48GB,FSTP-40,KX-2TB,X2407	BOM_BASE,BOM_DEV,ALTERNATE,SOC:40FSTP_48G,SSD:KX-2TB-4L
639-17809	PCBA,MLB-C,12C,48GB,FSTP-40,HY-2TB,X2407	BOM_BASE,BOM_DEV,ALTERNATE,SOC:40FSTP_48G,SSD:HY-2TB-4L
639-17810	PCBA,MLB-C,12C,48GB,FSTP-40,KX-4TB,X2407	BOM_BASE,BOM_DEV,ALTERNATE,SOC:40FSTP_48G,SSD:KX-4TB-8L
639-17811	PCBA,MLB-C,12C,48GB,FSTP-40,HY-4TB,X2407	BOM_BASE,BOM_DEV,ALTERNATE,SOC:40FSTP_48G,SSD:HY-4TB-8L
639-17812	PCBA,MLB-C,12C,48GB,FSTP-40,KX-8TB,X2407	BOM_BASE,BOM_DEV,ALTERNATE,SOC:40FSTP_48G,SSD:KX-8TB-8L
639-17813	PCBA,MLB-C,12C,48GB,FSTP-40,HY-8TB,X2407	BOM_BASE,BOM_DEV,ALTERNATE,SOC:40FSTP_48G,SSD:HY-8TB-8L

SOC 12C 64GB FSTP40

BOM NUMBER	BOM NAME	BOM OPTIONS
639-17814	PCBA,MLB-C,12C,64GB,FSTP-40,KX-512,X2407	BOM_BASE,BOM_DEV,ALTERNATE,SOC:40FSTP_64G,SSD:KX-512-4L
639-17815	PCBA,MLB-C,12C,64GB,FSTP-40,WD-512,X2407	BOM_BASE,BOM_DEV,ALTERNATE,SOC:40FSTP_64G,SSD:WD-512-4L
639-17816	PCBA,MLB-C,12C,64GB,FSTP-40,KX-1TB,X2407	BOM_BASE,BOM_DEV,ALTERNATE,SOC:40FSTP_64G,SSD:KX-1TB-4L
639-17818	PCBA,MLB-C,12C,64GB,FSTP-40,HY-1TB,X2407	BOM_BASE,BOM_DEV,ALTERNATE,SOC:40FSTP_64G,SSD:HY-1TB-4L
639-17819	PCBA,MLB-C,12C,64GB,FSTP-40,KX-2TB,X2407	BOM_BASE,BOM_DEV,ALTERNATE,SOC:40FSTP_64G,SSD:KX-2TB-4L
639-17820	PCBA,MLB-C,12C,64GB,FSTP-40,HY-2TB,X2407	BOM_BASE,BOM_DEV,ALTERNATE,SOC:40FSTP_64G,SSD:HY-2TB-4L
639-17821	PCBA,MLB-C,12C,64GB,FSTP-40,KX-4TB,X2407	BOM_BASE,BOM_DEV,ALTERNATE,SOC:40FSTP_64G,SSD:KX-4TB-8L
639-17822	PCBA,MLB-C,12C,64GB,FSTP-40,HY-4TB,X2407	BOM_BASE,BOM_DEV,ALTERNATE,SOC:40FSTP_64G,SSD:HY-4TB-8L
639-17823	PCBA,MLB-C,12C,64GB,FSTP-40,KX-8TB,X2407	BOM_BASE,BOM_DEV,ALTERNATE,SOC:40FSTP_64G,SSD:KX-8TB-8L
639-17824	PCBA,MLB-C,12C,64GB,FSTP-40,HY-8TB,X2407	BOM_BASE,BOM_DEV,ALTERNATE,SOC:40FSTP_64G,SSD:HY-8TB-8L

SOC 12C 128GB FSTP40

BOM NUMBER	BOM NAME	BOM OPTIONS
639-17825	PCBA,MLB-C,12C,128G,FSTP-40,KX-512,X2407	BOM_BASE,BOM_DEV,ALTERNATE,SOC:40FSTP_128G,SSD:KX-512-4L
639-17826	PCBA,MLB-C,12C,128G,FSTP-40,WD-512,X2407	BOM_BASE,BOM_DEV,ALTERNATE,SOC:40FSTP_128G,SSD:WD-512-4L
639-17827	PCBA,MLB-C,12C,128G,FSTP-40,KX-1TB,X2407	BOM_BASE,BOM_DEV,ALTERNATE,SOC:40FSTP_128G,SSD:KX-1TB-4L
639-17829	PCBA,MLB-C,12C,128G,FSTP-40,HY-1TB,X2407	BOM_BASE,BOM_DEV,ALTERNATE,SOC:40FSTP_128G,SSD:HY-1TB-4L
639-17830	PCBA,MLB-C,12C,128G,FSTP-40,KX-2TB,X2407	BOM_BASE,BOM_DEV,ALTERNATE,SOC:40FSTP_128G,SSD:KX-2TB-4L
639-17831	PCBA,MLB-C,12C,128G,FSTP-40,HY-2TB,X2407	BOM_BASE,BOM_DEV,ALTERNATE,SOC:40FSTP_128G,SSD:HY-2TB-4L
639-17832	PCBA,MLB-C,12C,128G,FSTP-40,KX-4TB,X2407	BOM_BASE,BOM_DEV,ALTERNATE,SOC:40FSTP_128G,SSD:KX-4TB-8L
639-17833	PCBA,MLB-C,12C,128G,FSTP-40,HY-4TB,X2407	BOM_BASE,BOM_DEV,ALTERNATE,SOC:40FSTP_128G,SSD:HY-4TB-8L
639-17834	PCBA,MLB-C,12C,128G,FSTP-40,KX-8TB,X2407	BOM_BASE,BOM_DEV,ALTERNATE,SOC:40FSTP_128G,SSD:KX-8TB-8L
639-17835	PCBA,MLB-C,12C,128G,FSTP-40,HY-8TB,X2407	BOM_BASE,BOM_DEV,ALTERNATE,SOC:40FSTP_128G,SSD:HY-8TB-8L

DEV BOMs

BOM NUMBER	BOM NAME	BOM OPTIONS
939-14302	PCBA,MLB-C,DCDC-1,X2407	BOM_BASE,BOM_DEV,ALTERNATE,SSD:NOS5E,SOC:SOCKET
939-14303	PCBA,MLB-C,DCDC-2,X2407	BOM_BASE,BOM_DEV,SSD:8L-DCDC,NAND:SOCKET

SOC 10C 96GB FSTP30

BOM NUMBER	BOM NAME	BOM OPTIONS
639-17792	PCBA,MLB-C,10C,96GB,FSTP-30,KX-512,X2407	BOM_BASE,BOM_DEV,ALTERNATE,SOC:30FSTP_96G,SSD:KX-512-4L
639-17793	PCBA,MLB-C,10C,96GB,FSTP-30,WD-512,X2407	BOM_BASE,BOM_DEV,ALTERNATE,SOC:30FSTP_96G,SSD:WD-512-4L
639-17794	PCBA,MLB-C,10C,96GB,FSTP-30,KX-1TB,X2407	BOM_BASE,BOM_DEV,ALTERNATE,SOC:30FSTP_96G,SSD:KX-1TB-4L
639-17796	PCBA,MLB-C,10C,96GB,FSTP-30,HY-1TB,X2407	BOM_BASE,BOM_DEV,ALTERNATE,SOC:30FSTP_96G,SSD:HY-1TB-4L
639-17797	PCBA,MLB-C,10C,96GB,FSTP-30,KX-2TB,X2407	BOM_BASE,BOM_DEV,ALTERNATE,SOC:30FSTP_96G,SSD:KX-2TB-4L
639-17798	PCBA,MLB-C,10C,96GB,FSTP-30,HY-2TB,X2407	BOM_BASE,BOM_DEV,ALTERNATE,SOC:30FSTP_96G,SSD:HY-2TB-4L
639-17799	PCBA,MLB-C,10C,96GB,FSTP-30,KX-4TB,X2407	BOM_BASE,BOM_DEV,ALTERNATE,SOC:30FSTP_96G,SSD:KX-4TB-8L
639-17800	PCBA,MLB-C,10C,96GB,FSTP-30,HY-4TB,X2407	BOM_BASE,BOM_DEV,ALTERNATE,SOC:30FSTP_96G,SSD:HY-4TB-8L
639-17801	PCBA,MLB-C,10C,96GB,FSTP-30,KX-8TB,X2407	BOM_BASE,BOM_DEV,ALTERNATE,SOC:30FSTP_96G,SSD:KX-8TB-8L
639-17802	PCBA,MLB-C,10C,96GB,FSTP-30,HY-8TB,X2407	BOM_BASE,BOM_DEV,ALTERNATE,SOC:30FSTP_96G,SSD:HY-8TB-8L

SOC 10C 36GB FSTP30 -- NONPOR

BOM NUMBER	BOM NAME	BOM OPTIONS
639-19537	MLB-C,10C,36GB,FSTP-30,KX-1TB,PRQ,X2407	BOM_BASE,BOM_DEV,ALTERNATE,SOC:30FSTP_36G,SSD:KX-1TB-4L-NONPOR
639-19542	MLB-C,10C,36GB,FSTP-30,KX-2TB,PRQ,X2407	BOM_BASE,BOM_DEV,ALTERNATE,SOC:30FSTP_36G,SSD:KX-2TB-4L-NONPOR

SOC 10C 96GB FSTP30 -- NONPOR

BOM NUMBER	BOM NAME	BOM OPTIONS
639-19538	MLB-C,10C,96GB,FSTP-30,KX-1TB,PRQ,X2407	BOM_BASE,BOM_DEV,ALTERNATE,SOC:30FSTP_96G,SSD:KX-1TB-4L-NONPOR
639-19543	MLB-C,10C,96GB,FSTP-30,KX-2TB,PRQ,X2407	BOM_BASE,BOM_DEV,ALTERNATE,SOC:30FSTP_96G,SSD:KX-2TB-4L-NONPOR

SOC 12C 48GB FSTP40 -- NONPOR

BOM NUMBER	BOM NAME	BOM OPTIONS
639-19539	MLB-C,12C,48GB,FSTP-40,KX-1TB,PRQ,X2407	BOM_BASE,BOM_DEV,ALTERNATE,SOC:40FSTP_48G,SSD:KX-1TB-4L-NONPOR
639-19544	MLB-C,12C,48GB,FSTP-40,KX-2TB,PRQ,X2407	BOM_BASE,BOM_DEV,ALTERNATE,SOC:40FSTP_48G,SSD:KX-2TB-4L-NONPOR

SOC 12C 64GB FSTP40 -- NONPOR

BOM NUMBER	BOM NAME	BOM OPTIONS
639-19540	MLB-C,12C,64GB,FSTP-40,KX-1TB,PRQ,X2407	BOM_BASE,BOM_DEV,ALTERNATE,SOC:40FSTP_64G,SSD:KX-1TB-4L-NONPOR
639-19545	MLB-C,12C,64GB,FSTP-40,KX-2TB,PRQ,X2407	BOM_BASE,BOM_DEV,ALTERNATE,SOC:40FSTP_64G,SSD:KX-2TB-4L-NONPOR

SOC 12C 128GB FSTP40 -- NONPOR

BOM NUMBER	BOM NAME	BOM OPTIONS
639-19541	MLB-C,12C,128G,FSTP-40,KX-1TB,PRQ,X2407	BOM_BASE,BOM_DEV,ALTERNATE,SOC:40FSTP_128G,SSD:KX-1TB-4L-NONPOR
639-19546	MLB-C,12C,128G,FSTP-40,KX-2TB,PRQ,X2407	BOM_BASE,BOM_DEV,ALTERNATE,SOC:40FSTP_128G,SSD:KX-2TB-4L-NONPOR

SYNC_MASTER=SKATPATH_MLB_C_0.39.2 SYNC_DATE=02/27/2023

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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
103S00248	103S00247	ANY	ALL	<RDAR://65854832>
103S00250	103S00249	ANY	ALL	<RDAR://65855215>
107S00015	107S00011	ANY	ALL	<RDAR://68783373>
107S00033	107S00034	ANY	ALL	<RDAR://55465318>
107S00041	107S00039	ANY	ALL	<RDAR://64239409>
107S00055	107S00090	ANY	ALL	<RDAR://64239505>
107S00493	107S00056	ANY	ALL	<RDAR://99049113>
107S00057	107S00100	ANY	ALL	<RDAR://64239601>
107S00071	107S00053	ANY	ALL	<RDAR://56380033>
107S00076	107S00044	ANY	ALL	<RDAR://64238938>
107S00087	107S00029	ANY	ALL	<RDAR://56380033>
107S00090	107S00055	ANY	ALL	<RDAR://56380033>
107S00443	107S00005	ANY	ALL	<RDAR://98860588>
107S00102	107S00017	ANY	ALL	<RDAR://64239315>
107S00494	107S00058	ANY	ALL	<RDAR://107278591>
107S00491	107S00061	ANY	ALL	<RDAR://98861129>
107S00440	107S00062	ANY	ALL	<RDAR://98861507>
107S00492	107S00234	ANY	ALL	<RDAR://98859848>
107S00297	107S00344	ANY	ALL	<RDAR://64239077>
107S00298	107S00460	ANY	ALL	<RDAR://68783859>
107S00346	107S00116	ANY	ALL	<RDAR://57135567>
107S00365	107S00373	ANY	ALL	<RDAR://64240682>
107S00391	107S00392	ANY	ALL	<RDAR://68783810>
107S00392	107S00391	ANY	ALL	<RDAR://68783826>
107S0150	107S00460	ANY	ALL	<RDAR://68783859>
107S0240	107S0255	ANY	ALL	<RDAR://69891889>
107S0276	107S00020	ANY	ALL	<RDAR://57126636>
107S0284	107S00021	ANY	ALL	<RDAR://64240943>
116S00007	116S00006	ANY	ALL	<RDAR://65855701>
117S00040	117S00012	ANY	ALL	<RDAR:73475063//>
118S00093	118S00092	ANY	ALL	<RDAR://65856806>
128S00009	128S00093	ANY	ALL	rdar://73509196
128S00119	128S00016	ANY	ALL	<RDAR://68780181>
128S00026	128S00011	ANY	ALL	<RDAR://56380033>
128S00031	128S00011	ANY	ALL	<RDAR://56380033>
128S00039	128S00038	ANY	ALL	<RDAR://56380033>
128S00058	128S00098	ANY	ALL	rdar://71999316
128S00069	128S00067	ANY	ALL	<RDAR://65153232>
128S00069	128S00094	ANY	ALL	<RDAR://68779373>
128S00087	128S00011	ANY	ALL	<RDAR://56380033>
128S00093	128S00009	ANY	ALL	<RDAR://68780181>
128S00094	128S00067	ANY	ALL	<RDAR://68779373>
128S00103	128S00009	ANY	ALL	<RDAR://68780181>
128S00103	128S00093	ANY	ALL	rdar://73509196
128S00105	128S00098	ANY	ALL	rdar://71999316
128S0364	128S0264	ANY	ALL	<RDAR://56380033>
128S0445	128S0436	ANY	ALL	<RDAR://68808630>
128S0487	128S00012	ANY	ALL	<RDAR://68780476>
131S0704	131S00328	ANY	ALL	<RDAR://69407017>
132S00064	132S0409	ANY	ALL	<RDAR://69816432>
132S00176	132S0640	ANY	ALL	<RDAR://65054797>
132S00229	132S00010	ANY	ALL	<RDAR://57135129>

ALTERNATES FROM REF_HDMI_COBRA

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
377S0077	377S0183		DZH505	
311S00279	311S00285		UH801	RDAR://88051825
311S0341	311S0536		UH802	RDAR://64195790
197S00371	197S00375		YH700	RDAR://95892403
197S00374	197S00375		YH700	RDAR://95892403

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
132S0409	132S00064	ANY	ALL	<RDAR://68809701>
138S00047	138S00073	ANY	ALL	<RDAR://56380033>
138S00084	138S00060	ANY	ALL	<RDAR://64425730>
138S00086	138S0884	ANY	ALL	<RDAR://65199790>
138S00087	138S1086	ANY	ALL	rdar://69510573
138S00097	138S0750	ANY	ALL	<RDAR://65198710>
138S00104	138S0978	ANY	ALL	<RDAR://65054584>
138S00116	138S00117	ANY	ALL	<RDAR://68809155>
138S00116	138S00071	ANY	ALL	<RDAR://64425485>
138S00117	138S00071	ANY	ALL	<RDAR://64425485>
138S00139	138S00138	ANY	ALL	<RDAR://64426076>
138S00164	138S00138	ANY	ALL	<RDAR://64426076>
138S00181	138S0835	ANY	ALL	<RDAR://57161300>
138S00229	138S00107	ANY	ALL	<RDAR://64381231>
138S00280	138S00138	ANY	ALL	<RDAR://64426076>
138S00284	138S00136	ANY	ALL	<RDAR://57134599>
138S00291	138S0835	ANY	ALL	<RDAR://57161300>
138S00330	138S00081	ANY	ALL	<RDAR://64425893>
138S00332	138S00328	ANY	ALL	<RDAR://57328643>
138S00343	138S00329	ANY	ALL	<RDAR://64426266>
138S00364	138S00290	ANY	ALL	<RDAR://64910444>
138S00385	138S00377	ANY	ALL	rdar://73670288
138S0715	138S0732	ANY	ALL	<RDAR://65198951>
138S0738	138S1101	ANY	ALL	<RDAR://55465318>
138S0746	138S0705	ANY	ALL	<RDAR://65194259>
138S0750	138S00097	ANY	ALL	<RDAR://57138474>
138S0772	138S00013	ANY	ALL	<RDAR://69408404>
138S0786	138S0705	ANY	ALL	<RDAR://65194259>
138S0789	138S0941	ANY	ALL	<RDAR://56380033>
138S0846	138S0811	ANY	ALL	<RDAR://55465318>
138S0852	138S0818	ANY	ALL	<RDAR://57137990>
138S0863	138S0853	ANY	ALL	<RDAR://56380033>
138S1068	138S00215	ANY	ALL	<RDAR://64909886>
138S1103	138S0719	ANY	ALL	<RDAR://65199121>
152S01788	152S00182	ANY	ALL	<RDAR://64435747>
152S00198	152S00680	ANY	ALL	<RDAR://56380033>
152S00343	152S00839	ANY	ALL	<RDAR://57238826>
152S00359	152S00253	ANY	ALL	<RDAR://55465318>
152S00367	152S01248	ANY	ALL	<RDAR://56380033>
152S00383	152S00680	ANY	ALL	<RDAR://56380033>
152S00398	152S00204	ANY	ALL	<RDAR://56380033>
152S01789	152S00265	ANY	ALL	<RDAR://98418608>
152S00785	152S00477	ANY	ALL	<RDAR://69846739>
152S00801	152S00695	ANY	ALL	<RDAR://64386631>
152S01780	152S00238	ANY	ALL	<RDAR://98416973>
152S00864	152S00851	ANY	ALL	<RDAR://57159654>
152S00963	152S00885	ANY	ALL	<RDAR://56380033>
152S00997	152S00476	ANY	ALL	<RDAR://56380033>
152S01023	152S00384	ANY	ALL	<RDAR://64458983>

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S01024	152S00386	ANY	ALL	NA
152S01037	152S00887	ANY	ALL	<RDAR://65152741>
152S01070	152S00887	ANY	ALL	<RDAR://65152741>
152S01090	152S01085	ANY	ALL	<RDAR://57230783>
152S01836	152S01268	ANY	ALL	<RDAR://102912630>
152S01344	152S00883	ANY	ALL	<RDAR://64434865>
152S01410	152S01300	ANY	ALL	rdar://64173241
152S01415	152S01280	ANY	ALL	<RDAR://64722980>
152S01451	152S00883	ANY	ALL	<RDAR://64434865>
152S01452	152S01248	ANY	ALL	<RDAR://67823644>
155S00097	155S0664	ANY	ALL	<RDAR://102911698>
155S00155	155S0441	ANY	ALL	<RDAR://65043740>
155S00204	155S0731	ANY	ALL	<RDAR://65054205>
155S00309	155S0831	ANY	ALL	<RDAR://65054290>
155S00512	155S0897	ANY	ALL	<RDAR://65045687>
155S00648	155S00647	ANY	ALL	<RDAR://68810066>
155S00885	155S00188	ANY	ALL	<RDAR://102886362>
155S0660	155S0513	ANY	ALL	<RDAR://68810203>
155S00867	155S0644	ANY	ALL	<RDAR://102911120>
155S0830	155S0316	ANY	ALL	<RDAR://70020267>
197S00046	197S00036	ANY	ALL	<RDAR://57229594>
197S00047	197S00036	ANY	ALL	<RDAR://57229594>
197S00048	197S00036	ANY	ALL	<RDAR://57229594>
197S00318	197S00323	ANY	ALL	rdar://73373069
197S0588	197S0591	ANY	ALL	rdar://78480268
197S0590	197S0588	ANY	ALL	<RDAR://65008354>
197S0590	197S0591	ANY	ALL	<RDAR://65008354>
197S0591	197S0588	ANY	ALL	<RDAR://65008354>
311S00013	311S0508	ANY	ALL	<RDAR://57211339>
311S00060	311S0273	ANY	ALL	<RDAR://57172430>
311S00076	311S0220	ANY	ALL	<RDAR://68811993>
311S00392	311S00129	ANY	ALL	<RDAR://106720001>
311S00176	311S00153	ANY	ALL	<RDAR://57133089>
311S00178	311S00177	ANY	ALL	<RDAR://68811202>
311S00258	311S00257	ANY	ALL	<RDAR://64195593>
311S00267	311S00244	ANY	ALL	<RDAR://63954013>
311S00268	311S00246	ANY	ALL	<RDAR://64048026>
311S00277	311S00276	ANY	ALL	<RDAR://63847873>
311S00279	311S00285	ANY	ALL	<RDAR://68811697>
311S00310	311S00306	ANY	ALL	<RDAR://69815666>
311S00312	311S0278	ANY	ALL	rdar://78128916
311S0649	311S0226	ANY	ALL	<RDAR://64237121>
335S00500	335S00494	ANY	ALL	<RDAR://68784737>
338S00753	338S00740	ANY	ALL	rdar://73369340
353S00852	353S4262	ANY	ALL	<RDAR://57244062>
353S00878	353S00599	ANY	ALL	<RDAR://57173083>
353S01181	353S02807	ANY	ALL	rdar://75236244
353S01346	353S01320	ANY	ALL	<RDAR://56390543>
353S01792	353S3901	ANY	ALL	<RDAR://73727836>
353S02030	353S01993	ANY	ALL	<RDAR://57133661>
353S02127	353S02184	ANY	ALL	<RDAR://71012596>
353S02175	353S00882	ANY	ALL	<RDAR://68820393>
353S02402	353S1429	ANY	ALL	<RDAR://73727544>

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S02407	353S02212	ANY	ALL	<RDAR://63861706>
353S02434	353S3332	ANY	ALL	<RDAR://68820512>
353S02465	353S2620	ANY	ALL	<RDAR://64236549>
353S02624	353S01595	ANY	ALL	rdar://73592667
353S02635	353S02395	ANY	ALL	<RDAR://69166318>
353S02789	353S3021	ANY	ALL	rdar://73885143
353S02811	353S02626	ANY	ALL	rdar://74562706
371S00077	371S00180	ANY	ALL	<RDAR://55465318>
371S00085	371S00190	ANY	ALL	<RDAR://64913914>
371S00217	371S00079	ANY	ALL	<RDAR://55465318>
371S00220	371S00307	ANY	ALL	<RDAR://73728616>
371S00302	371S00241	ANY	ALL	<RDAR://69526283>
371S00306	371S00305	ANY	ALL	<RDAR://73728520>
371S00311	371S00312	ANY	ALL	<RDAR://68821167>
371S00312	371S00311	ANY	ALL	<RDAR://69890674>
371S00322	371S00047	ANY	ALL	rdar://74200997
371S00328	371S00310	ANY	ALL	rdar://73627030
371S0602	371S00245	ANY	ALL	<RDAR://69900570>
371S0718	371S0531	ANY	ALL	<RDAR://57233043>
371S0730	371S00172	ANY	ALL	rdar://73629317
372S00040	372S00039	ANY	ALL	<RDAR://68821275>
372S0082	372S00023	ANY	ALL	<RDAR://65196180>
376S00007	376S1179	ANY	ALL	<RDAR://56380033>
376S00019	376S1137	ANY	ALL	<RDAR://57166351>
376S00146	376S1061	ANY	ALL	<RDAR://57198167>
376S00204	376S00203	ANY	ALL	<RDAR://56380033>
376S00226	376S00203	ANY	ALL	<RDAR://56380033>
376S00227	376S00203	ANY	ALL	<RDAR://56380033>
376S00228	376S1179	ANY	ALL	<RDAR://56380033>
376S00281	376S1147	ANY	ALL	<RDAR://56380033>
376S00292	376S00294	ANY	ALL	<RDAR://73731835>
376S00303	376S00012	ANY	ALL	<RDAR://56380033>
376S00321	376S00397	ANY	ALL	rdar://74354869
376S00399	376S0855	ANY	ALL	rdar://73599007
376S00466	376S00463	ANY	ALL	<RDAR://64047597>
376S00485	376S00455	ANY	ALL	rdar://74654584
376S00514	376S00510	ANY	ALL	rdar://73954493
376S1053	376S0604	ANY	ALL	<RDAR://55465318>
376S1080	376S0820	ANY	ALL	<RDAR://57125638>
376S1106	376S0678	ANY	ALL	<RDAR://55465318>
376S1112	376S00516	ANY	ALL	rdar://73777582
376S1147	376S00281	ANY	ALL	NA
377S00165	377S00031	ANY	ALL	<RDAR://64912300>
377S00166	377S00160	ANY	ALL	<RDAR://64047091>
377S00186	377S00060	ANY	ALL	<RDAR://68822222>
377S00210	377S00172	ANY	ALL	<RDAR://64899432>
377S0155	377S0184	ANY	ALL	<RDAR://57230484>
740S00041	740S0159	ANY	ALL	<RDAR://55465318>

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
740S00081	740S00053	ANY	ALL	<RDAR://69166742>
740S0118	740S00028	ANY	ALL	<RDAR://64196448>
107S0150	107S0208	ANY	ALL	rdar://82364397
107S00298	107S0208	ANY	ALL	rdar://82364397
335S00571	335S00644	ANY	ALL	rdar://102986961
335S00571	335S00537	ANY	ALL	rdar://82360599
353S4037	353S03251	ANY	ALL	rdar://95333373
353S00636	353S03251	ANY	ALL	rdar://95333373
353S03294	353S03251	ANY	ALL	rdar://95333373
128S00106	128S00107	ANY	ALL	rdar://95642483
128S00110	128S00107	ANY	ALL	rdar://95642483
376S00489	376S00605	ANY	ALL	rdar://96028611
376S00600	376S0761	ANY	ALL	rdar://95877768
376S00614	376S0761	ANY	ALL	rdar://98844391
377S00201	377S00240	ANY	ALL	rdar://97047594
377S00252	377S00251	ANY	ALL	rdar://97047268
128S00131	128S00094	ANY	ALL	rdar://98083341
128S00131	128S00069	ANY	ALL	rdar://98083341
138S00148	138S00149	ANY	ALL	rdar://98081899
138S00150	138S00149	ANY	ALL	rdar://98081899
138S00151	138S00149	ANY	ALL	rdar://98081899
138S00049	138S0831	ANY	ALL	rdar://97805043
138S00450	138S0831	ANY	ALL	rdar://97805043
152S00991	152S00984	ANY	ALL	rdar://98576326
377S00223	377S00040	ANY	ALL	rdar://98409280
376S00631	376S0636	ANY	ALL	rdar://98410095
152S01787	152S00285	ANY	ALL	rdar://98832388
376S00670	376S0659	ANY	ALL	rdar://101229424
376S00667	376S0659	ANY	ALL	rdar://101229424
376S00618	376S00544	ANY	ALL	rdar://101229110
376S00516	376S00544	ANY	ALL	rdar://101229110
138S00457	138S00377	ANY	ALL	rdar://101315569
138S00457	138S00385	ANY	ALL	rdar://101315569
138S00397	138S00035	ANY	ALL	rdar://101314206
138S00460	138S00035	ANY	ALL	rdar://101314206
138S00049	138S0831	ANY	ALL	rdar://97805043

Location specific alternatives for ICEMAN and BACKLIGHT FETs

PART NUMBER	ALTERNATE FOR PART NUMBER	REFERENCE DESIGNATOR(S)	DESCRIPTION	BOM OPTION
376S00627	376S00328	Q5820,Q5840	ICEMAN_FET	
376S00036	376S00328	Q5820,Q5840	ICEMAN_FET	
376S00328	376S00263	QP800,QP801,QP802,QP803	BACKLIGHT_FET	
376S00021	376S00263	QP800,QP801,QP802,QP803	BACKLIGHT_FET	

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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00396	138S00392	ANY	ALL	<RDAR://71453199>
138S00437	138S00392	ANY	ALL	<RDAR://102382417>
138S00458	138S00392	ANY	ALL	<RDAR://102382417>
138S00437	138S00396	ANY	ALL	<RDAR://102382417>
138S00458	138S00396	ANY	ALL	<RDAR://102382417>
152S00812	152S1701	ANY	ALL	<RDAR://55465318>
376S00378	376S00324	ANY	ALL	<RDAR://102443940>
376S00383	376S00324	ANY	ALL	<RDAR://102443940>
152S00801	152S00695	ANY	ALL	<RDAR://102517736>
518S00311	518S0818	ANY	ALL	<RDAR://102517736>
138S00482	138S1086	ANY	ALL	<RDAR://103316955>
138S00482	138S00087	ANY	ALL	<RDAR://103316955>
353S02897	353S1429	ANY	ALL	<RDAR://97641170>
353S02897	353S02402	ANY	ALL	<RDAR://97641170>
376S00633	376S00294	ANY	ALL	<RDAR://101778372>
311S00335	311S00155	ANY	ALL	<RDAR://101780944>
132S00412	132S00195	ANY	ALL	<RDAR://101823840>
138S00167	138S00237	ANY	ALL	<RDAR://101825417>
138S0734	138S0838	ANY	ALL	<RDAR://101825649>
138S00124	138S00123	ANY	ALL	<RDAR://101827487>
138S00022	138S00020	ANY	ALL	<RDAR://101827693>
131S00691	131S00365	ANY	ALL	<RDAR://101828122>
152S01461	152S01283	ANY	ALL	<RDAR://102783124>
152S00343	152S01325	ANY	ALL	<RDAR://102783389>
311S00271	311S00286	ANY	ALL	<RDAR://102885222>
311S00322	311S00321	ANY	ALL	<RDAR://102885370>
107S00056	107S00086	ANY	ALL	<RDAR://103036795>
107S00479	107S00478	ANY	ALL	<RDAR://103037622>
116S00014	116S00044	ANY	ALL	<RDAR://103038104>
107S0255	107S0240	ANY	ALL	<RDAR://103040094>
155S00754	155S00098	ANY	ALL	<RDAR://102886532>
155S0387	155S0694	ANY	ALL	<RDAR://102885760>
155S00737	155S0921	ANY	ALL	<RDAR://1102885560>
311S0460	311S0449	ANY	ALL	<RDAR://102833551>
131S00213	131S0556	ANY	ALL	<RDAR://101823351>
371S00385	371S0602	ANY	ALL	<RDAR://101821205>
371S00370	371S00062	ANY	ALL	<RDAR://101820709>
353S03084	353S02407	ANY	ALL	<RDAR://101820633>
377S00196	377S00185	ANY	ALL	<RDAR://101820439>
311S0341	311S0536	ANY	ALL	<RDAR://101820271>
371S00325	371S00085	ANY	ALL	<RDAR://101778779>
353S03028	353S01211	ANY	ALL	<RDAR://101714843>
353S02787	353S01211	ANY	ALL	<RDAR://101714843>
132S00415	132S00410	ANY	ALL	<RDAR://104439670>
197S00391	197S00323	ANY	ALL	<RDAR://102878691>
197S00391	197S00318	ANY	ALL	<RDAR://102878691>

Location specific Alternatives per rdar://102884705

PART NUMBER	ALTERNATE FOR PART NUMBER	REFERENCE DESIGNATOR(S)	DESCRIPTION	BOM OPTION
376S00224	376S00557	QE501,QE511	FAN_FET	

Location specific Alternatives per rdar://98349810

PART NUMBER	ALTERNATE FOR PART NUMBER	REFERENCE DESIGNATOR(S)	DESCRIPTION	BOM OPTION
376S00647	376S00078	QH900,QF910,QF940,QF960,QG910,QG940,QG960	GROUP0-RT13-COBRA	
376S00634	376S00078	QH900,QF910,QF940,QF960,QG910,QG940,QG960	GROUP0-RT13-COBRA	
376S00588	376S00078	QH900,QF910,QF940,QF960,QG910,QG940,QG960	GROUP0-RT13-COBRA	
376S00647	376S00074	QC280,QF850	GROUP1-5V_S2-5V_USBC	
376S00634	376S00074	QC280,QF850	GROUP1-5V_S2-5V_USBC	
376S00078	376S00074	QC280,QF850	GROUP1-5V_S2-5V_USBC	
376S00588	376S00074	QC280,QF850	GROUP1-5V_S2-5V_USBC	
376S00332	376S00074	QC280,QF850	GROUP1-5V_S2-5V_USBC	

335S00603	335S0915	ANY	ALL	<RDAR://107015591>
138S00489	138S00488	ANY	ALL	<RDAR://107155999>
371S00435	371S00079	ANY	ALL	<RDAR://107200952>
132S00429	132S00411	ANY	ALL	<RDAR://107857453>

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REF_WIRELESS

PACK_OPTIONS TO INCLUDE IN NETLIST
3X_ANTENNA
SUNWAY
WLBT_PP_D2R
WLBT_TP_0P4
BT_FILTER_1P5MM

REF_HDMI_COBRA

PACK_OPTIONS TO INCLUDE IN NETLIST
HDMICH744:THICK
HDMICONN:PORTABLES_16
HDMI14UF:THICK
HDMI_DEBUG_CONN:YES
HDMI_0V95_FASTER_DISCHARGE

MESA TOUCHID
CSA256

PACK_OPTIONS TO INCLUDE IN NETLIST
PKGS:TOUCH_LARGER_PITCH

REF_USBC_LFKA_3PRT_ACE3

PACK_OPTIONS TO INCLUDE IN NETLIST
USBC_LAPTOP
PKGS:BGA
KEEP_SMALL_ARKANOID_CONN
ACE2_SS_CAP
FLIPPED
UPC1_ROM:YES
UPC1_UART_PD:NO
UPC1_UART_DEBUG
ATC_RTMR_ROM:XSON
ATC01_VR_MLCC-REGULAR
ATC2_VR_MLCC-REGULAR
ATC_VR_DSCHG-EN-R:NO
ATC_VR_PG-RES
UPC_STRAP1_PD:NO
USBC_GATE_PACKAGE:SOT
LDCM:ENABLED
ATC_BOUNDARYSCAN:YES
SOC_FORCE_DFU:YES
SOC_FORCE_DFU_YES:SOT
UPC2_STRAP4:NC
CHIP_ID_0X2

REF_SPKRAMP_SN012776

PACK_OPTIONS TO INCLUDE IN NETLIST
SPKRAMP_A
SPKRAMP_B
SPKRAMP_C
SPKRAMP_D
SPKRAMP_E
SPKRAMP_F
SPKRAMP_ICC_GB

REF_SDCARD

PACK_OPTIONS TO INCLUDE IN NETLIST
SD_VR_3V3:THICKSTNCL

REF_STORAGE_S5E

PACK_OPTIONS TO INCLUDE IN NETLIST
2V5_NAND_PBUS-B12-18V

REF_MAGSAFE_ACE3
REF_DEBUG

PACK_OPTIONS TO INCLUDE IN NETLIST
USBC_DBG:IN
UPC5_STRAP3:RPD
VITAMINC

REF_BLC_BEN_KBD_ONLY
REF_DEBUG

PACK_OPTIONS TO INCLUDE IN NETLIST
BLC_KBD_IND_HGT:1P9

REF_CHARGER_MANDOLA_28V
CSA52
CSA53

PACK_OPTIONS TO INCLUDE IN NETLIST
27UF_CAPS
3V8_DELAY:YES
HPWR_EN:GND

REF_PMU_CHAPEL_H15

PACK_OPTIONS TO INCLUDE IN NETLIST
SOC:C
FBUCK5:Y

IPD / Trackpad

PACK_OPTIONS TO INCLUDE IN NETLIST
IPD_RESETS_LS:PASS_THRU
IPD_MCU_INT_WAKE_LS:X2SON_THK
IPD_TOUCH_CLK_SRC:MLB
IPD_PACK_MTP_FUNC1_FLEX:PULLDOWN

SPF_27UF STUFFING
CSA128

PACK_OPTIONS TO INCLUDE IN NETLIST
SPF_27UF

REF_VR_5V_TPS62130
CSA122

PACK_OPTIONS TO INCLUDE IN NETLIST
5VS2TPS_PBUS-18V
5VS2TPS_THICKSTNCL

REF_IMU_SOVEREIGN
CSA144
CSA144
CSA144

PACK_OPTIONS TO INCLUDE IN NETLIST
REFIMU_TP:P5MM
REFIMU_VDD:LCFILT
REFIMU_TEST:YES

SOC
CSA27

PACK_OPTIONS TO INCLUDE IN NETLIST
VDD1_DIRECT

SPITFIRE/EKARA

PACK_OPTIONS TO INCLUDE IN NETLIST
L:3MM
POLY_PBUS:18V

REF_VR_ICEMAN_HP
CSA57
CSA60

PACK_OPTIONS TO INCLUDE IN NETLIST
3V8_AON_I2C-DEV
P3V8ILIM_MUX:Y
3V8_AON_PBUS-18V
3V8_AON_RPH1_ORIG
3V8_AON_RPH2_ORIG
3V8_AON_RPH3_ORIG
3V8_AON_RG201

REF_VR_5V_LT8642_1

PACK_OPTIONS TO INCLUDE IN NETLIST
5VUSBC01_PBUS-18V
5VUSBC01_THICKSTNCL
5VUSBC01_AND:PP
5VUSBC23_PBUS-18V

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