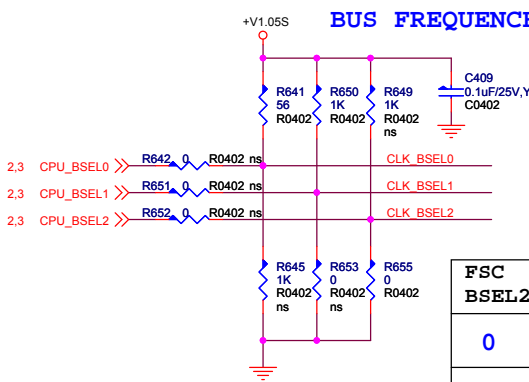
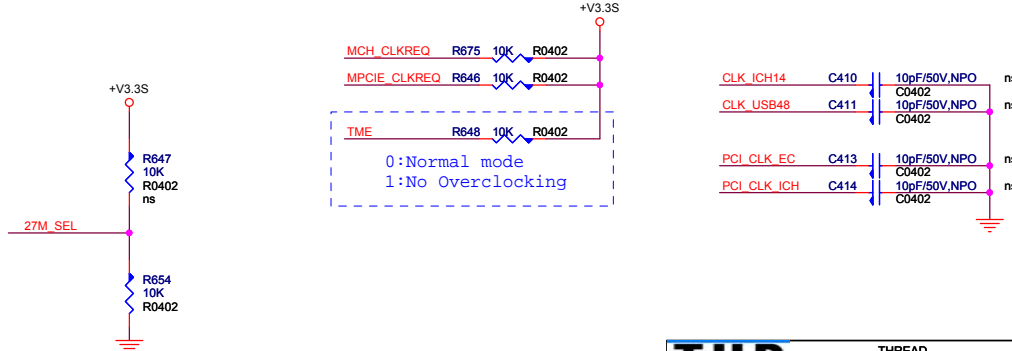


PCB
PX1 MB
PCB



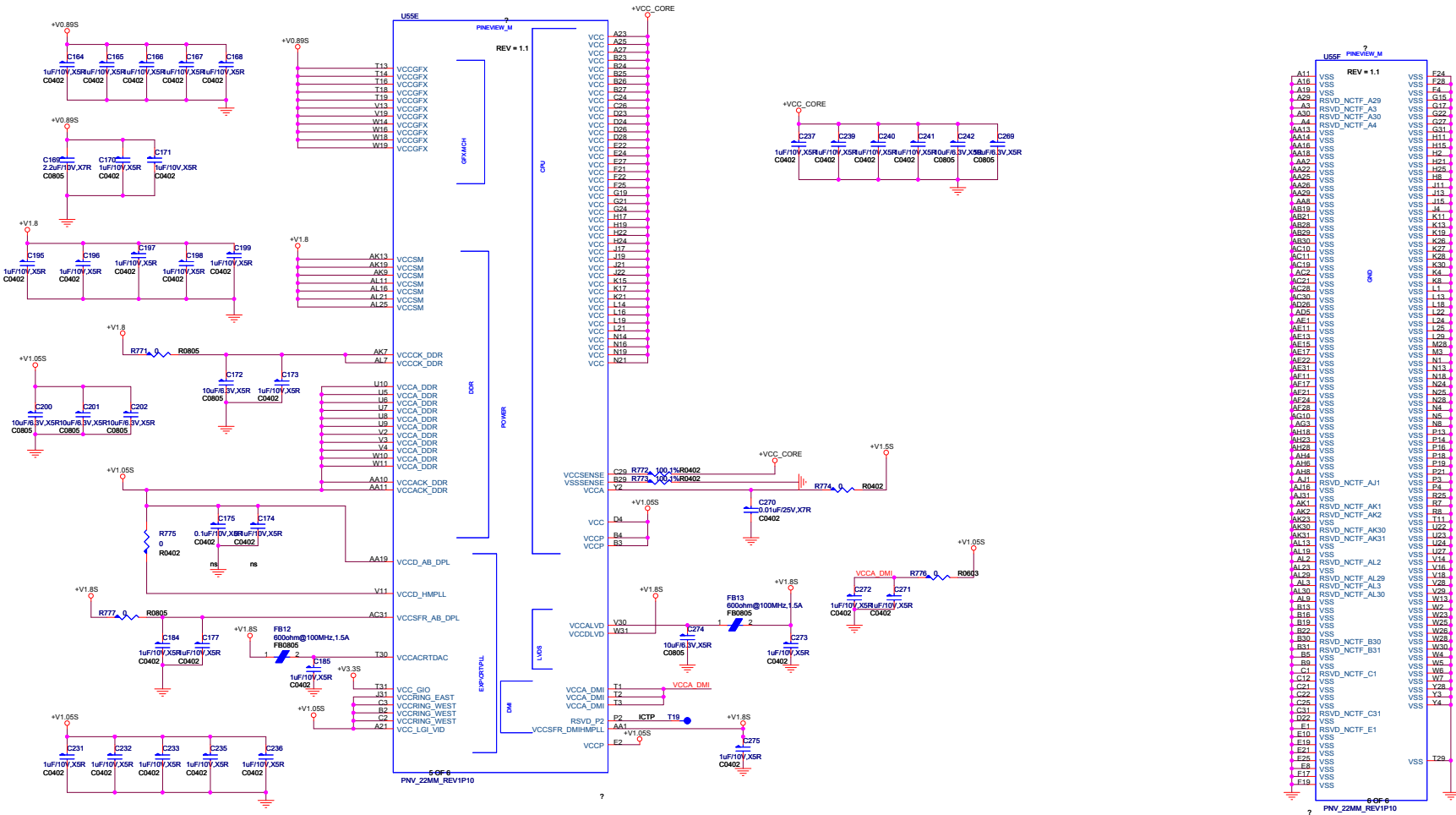
FSC BSEL2	FSB BSEL1	FSA BSEL0	HOST Clock frequency
0	0	1	133MHz
1	0	1	100MHz

0 1 1 166MHz 使用



THD		THREAD	
THD Inc. Co., Ltd.		HADS	
Page Name		CK505M	
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	PX1		
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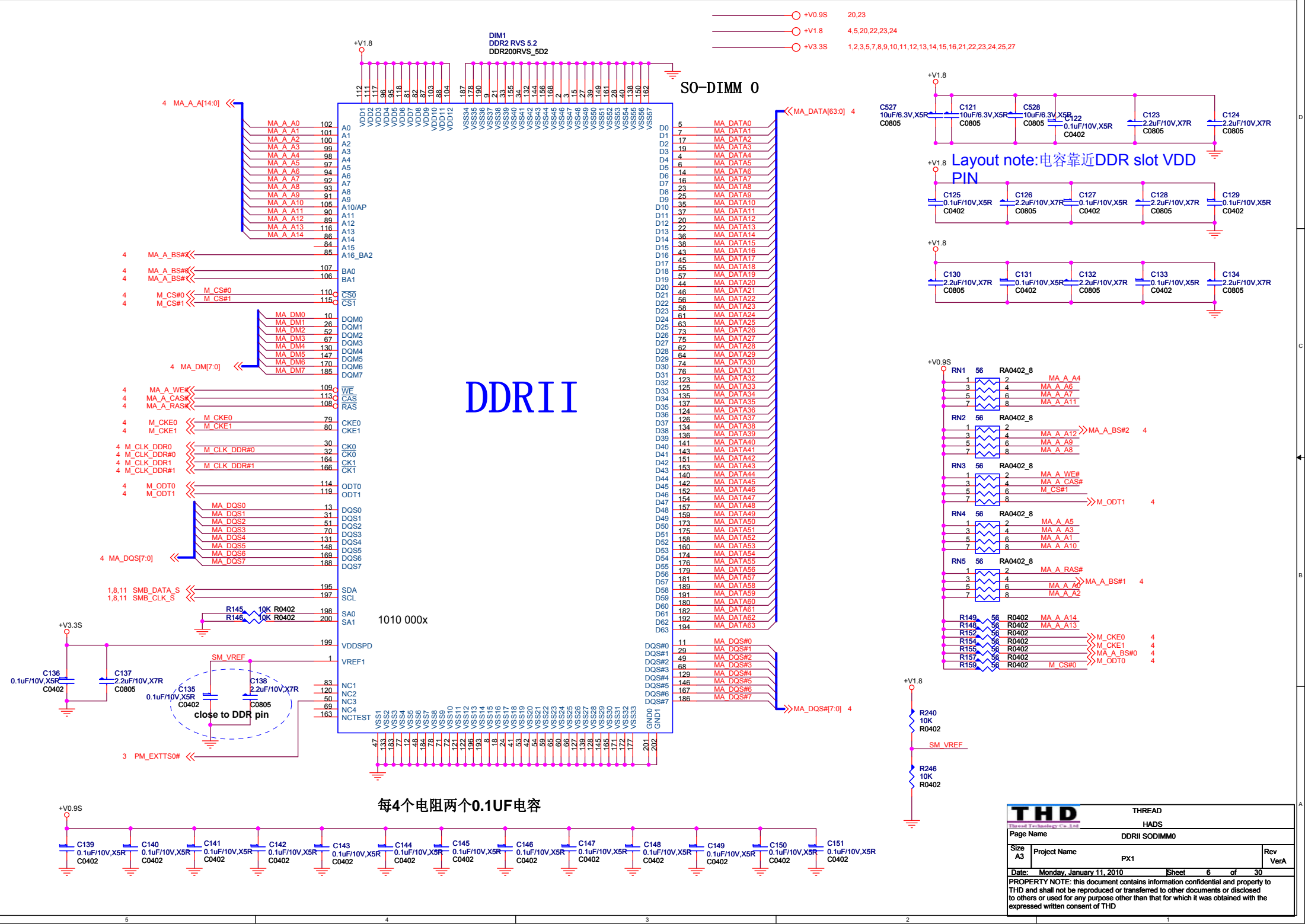
- +V3.3S 1,2,3,6,7,8,9,10,11,12,13,14,15,16,21,22,23,24,25,27
- +V1.0SS 1,2,3,8,10,12,14,21,22,23
- +V1.5S 9,10,11,12,13,15,21,22,23
- +V0.8SS 20,23
- +V1.8 4,6,20,22,23,24
- +VCC_CORE 25,29
- +V1.8S 24



USSE PINEVIEW_M REV = 1.1

USSE PINEVIEW_M REV = 1.1

A11	VSS	F24
A16	VSS	F28
A19	VSS	F4
A29	VSS	G15
A3	RSVD_NCTF_A3	G17
A30	RSVD_NCTF_A30	G22
A4	RSVD_NCTF_A4	G27
AA3	VSS	G31
AA14	VSS	H11
AA16	VSS	H15
AA18	VSS	H2
AA2	VSS	H21
AA22	VSS	H25
AA25	VSS	H8
AA3	VSS	H11
AA39	VSS	H13
AA8	VSS	H5
AB19	VSS	J4
AB21	VSS	K11
AB23	VSS	K13
AB29	VSS	K19
AB30	VSS	K28
AC10	VSS	K27
AC11	VSS	K28
AC2	VSS	K4
AC21	VSS	K8
AC39	VSS	L11
AC30	VSS	L13
AD5	VSS	L22
AE1	VSS	L24
AE11	VSS	L25
AE13	VSS	L29
AE22	VSS	L28
AE17	VSS	M3
AE23	VSS	N13
AE31	VSS	N1
AE11	VSS	N18
AE17	VSS	N24
AE21	VSS	N25
AE24	VSS	N28
AE28	VSS	N4
AG10	VSS	N5
AG3	VSS	N6
AH18	VSS	P13
AH3	VSS	P14
AH28	VSS	P16
AH4	VSS	P18
AH6	VSS	P19
AH8	VSS	P21
A11	RSVD_NCTF_A1	P4
AI18	VSS	R25
AI31	VSS	R25
AK1	RSVD_NCTF_AK1	R7
AK2	RSVD_NCTF_AK2	R8
AK3	VSS	T11
AK30	RSVD_NCTF_AK30	U22
AK31	RSVD_NCTF_AK31	U23
AL13	VSS	U24
AL19	VSS	U27
AL2	VSS	Y14
AL23	RSVD_NCTF_AL2	Y16
AL29	VSS	Y18
AL3	RSVD_NCTF_AL29	Y28
AL30	RSVD_NCTF_AL30	VSS
AL9	VSS	W13
B13	VSS	W2
B16	VSS	W23
B19	VSS	W25
B22	VSS	W28
B30	RSVD_NCTF_B30	W28
B31	RSVD_NCTF_B31	W30
B5	VSS	W4
B9	VSS	W5
C1	RSVD_NCTF_C1	W6
C12	VSS	W7
C21	VSS	Y28
C22	VSS	Y3
C25	VSS	Y4
C31	RSVD_NCTF_C31	VSS
D22	VSS	VSS
E1	RSVD_NCTF_E1	VSS
E10	VSS	VSS
E19	VSS	VSS
E21	VSS	VSS
E26	VSS	VSS
E8	VSS	VSS
F17	VSS	VSS
F19	VSS	VSS
T29	VSS	VSS



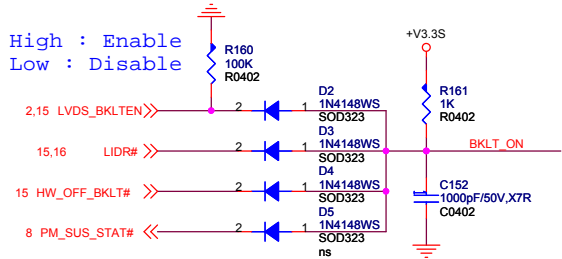
DDR I

每4个电阻两个0.1UF电容

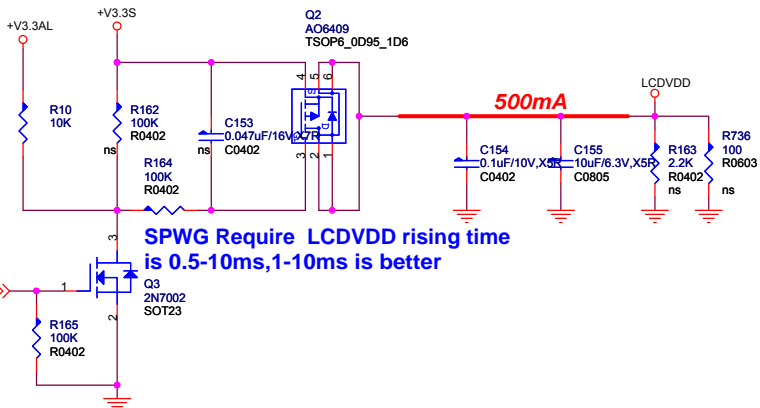
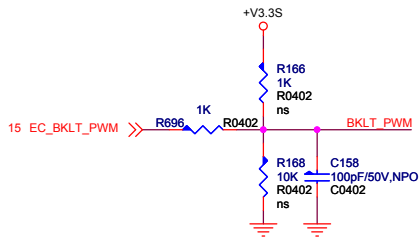
Layout note: 电容靠近DDR slot VDD PIN

THD THREAD Technology Co., Ltd.		THREAD	
Page Name		DDR I SODIMMO	
Size A3	Project Name	Rev VerA	
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High : Enable
Low : Disable

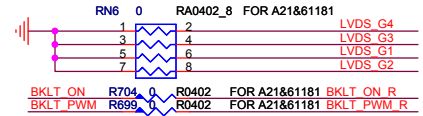
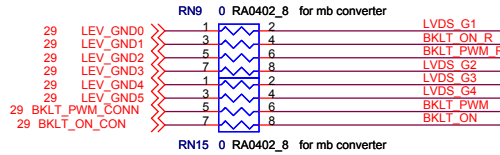
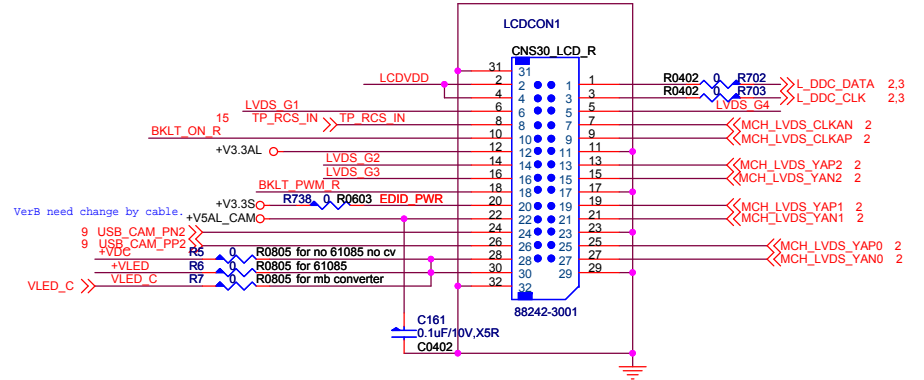


CLOSE TO INTCON

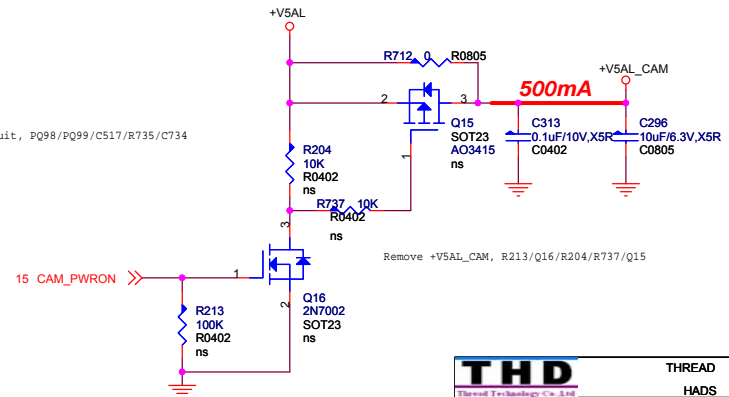


SPWG Require LCDVDD rising time
is 0.5-10ms, 1-10ms is better

Remove +V5S_LED, R208/Q14/R171/R3/Q13/C292/C275
R751/R752/R753/R754



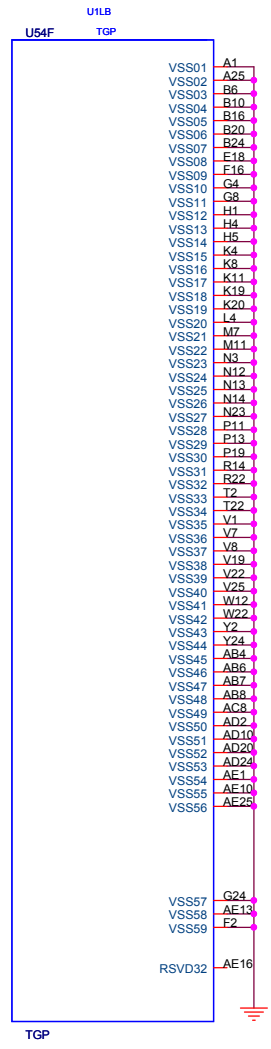
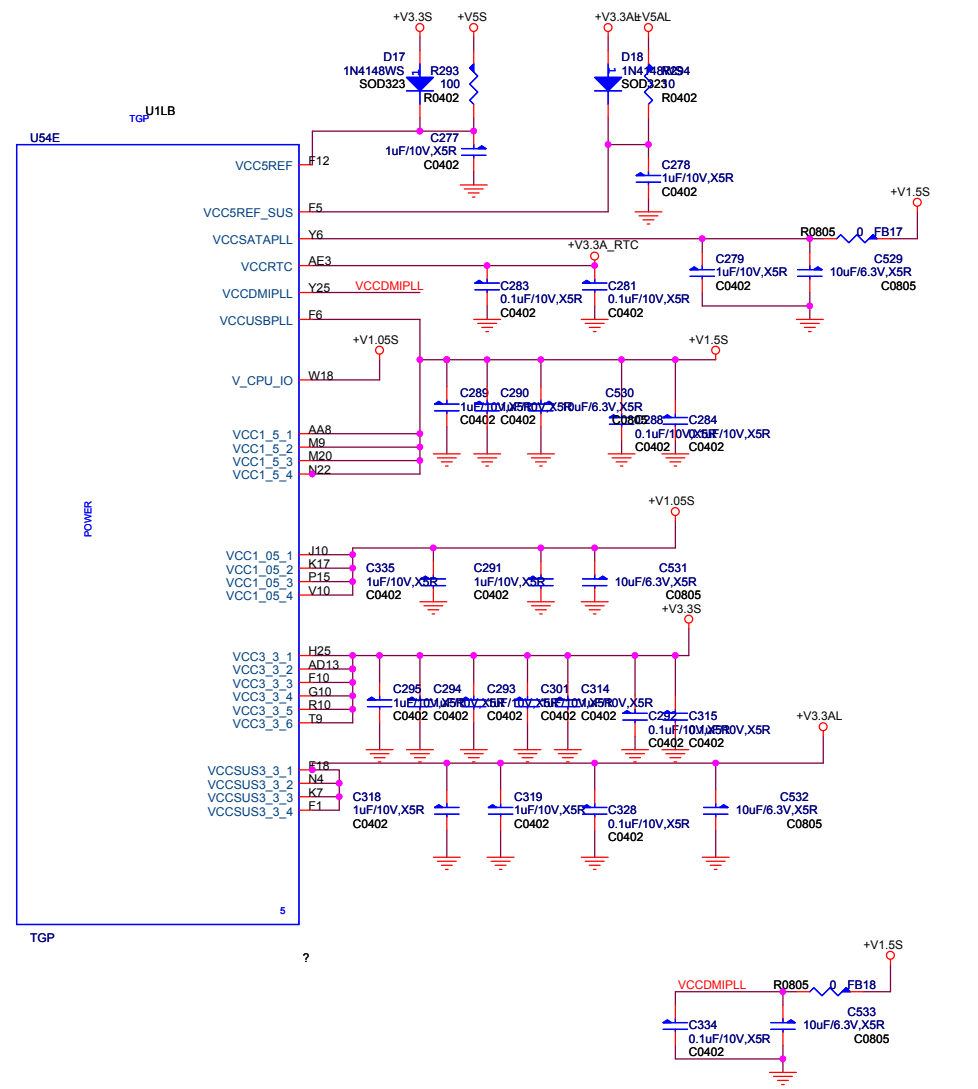
Remove discharge circuit, PQ98/PQ99/C517/R735/C734



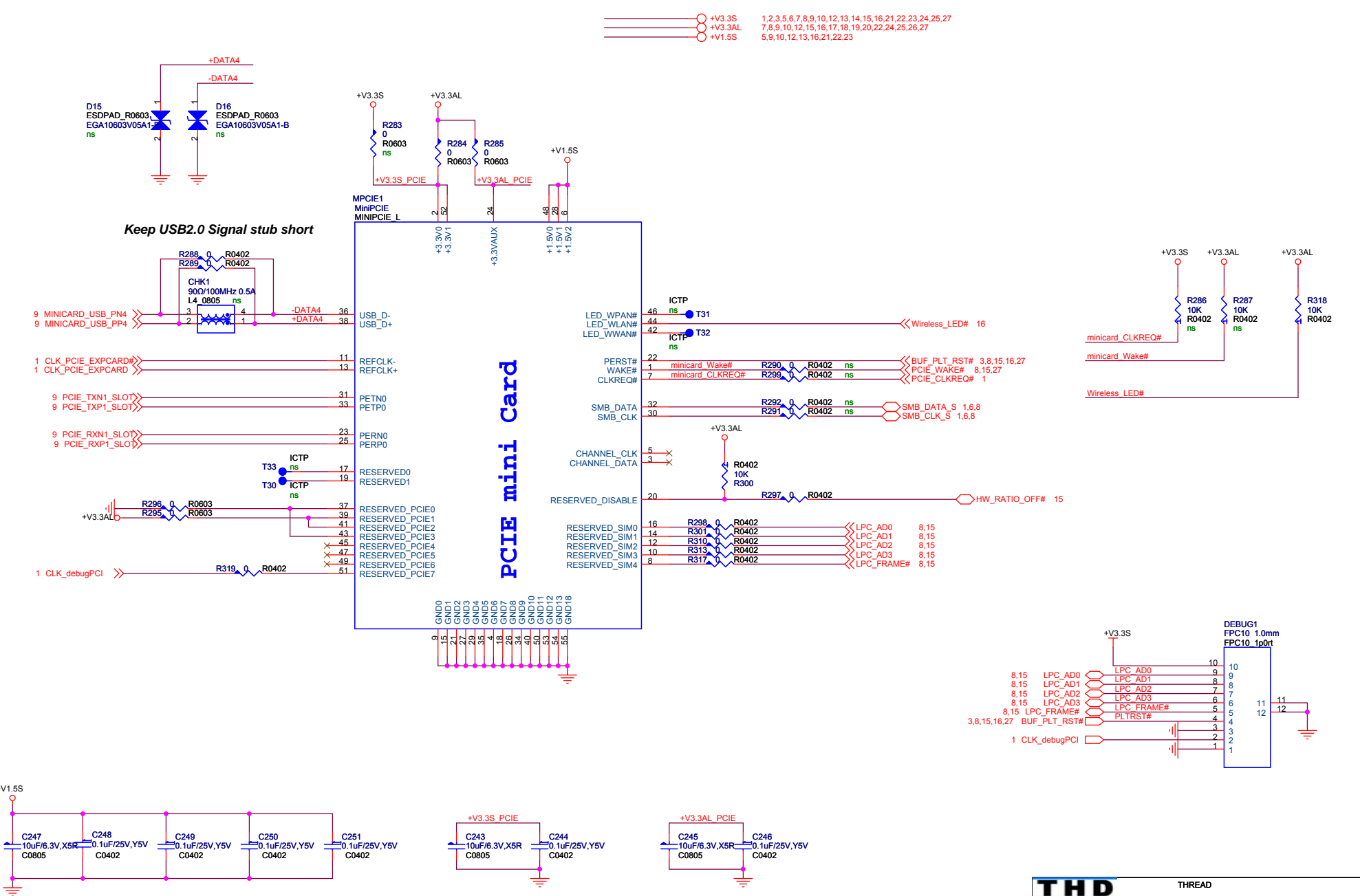
Remove +V5AL_CAM, R213/Q16/R204/R737/Q15

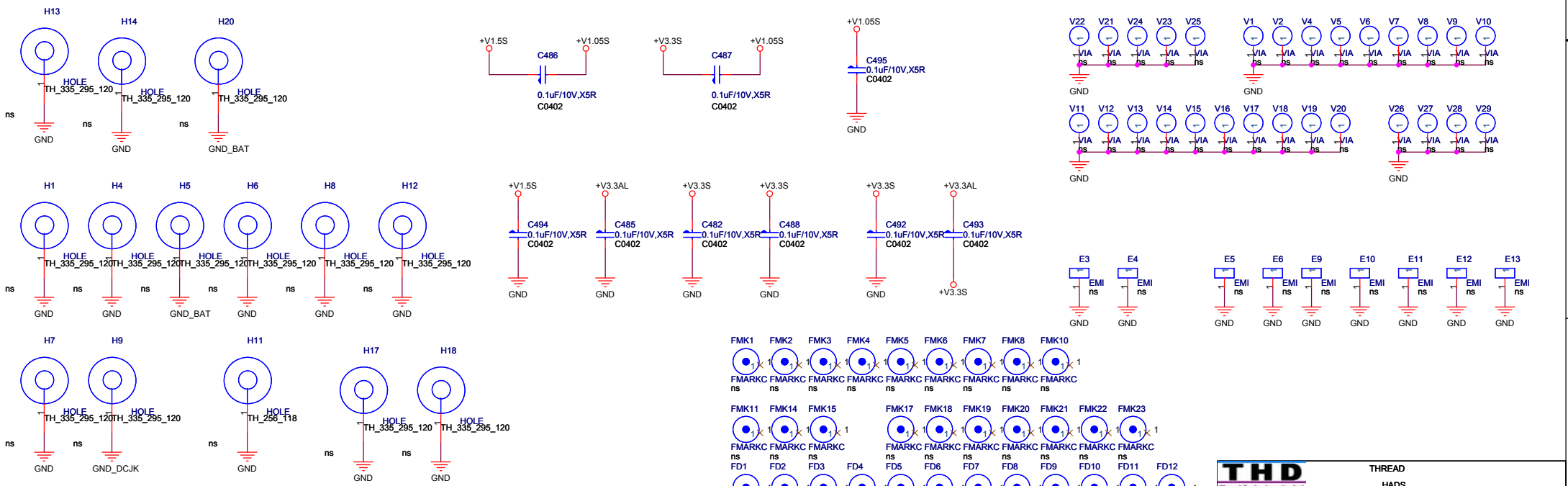
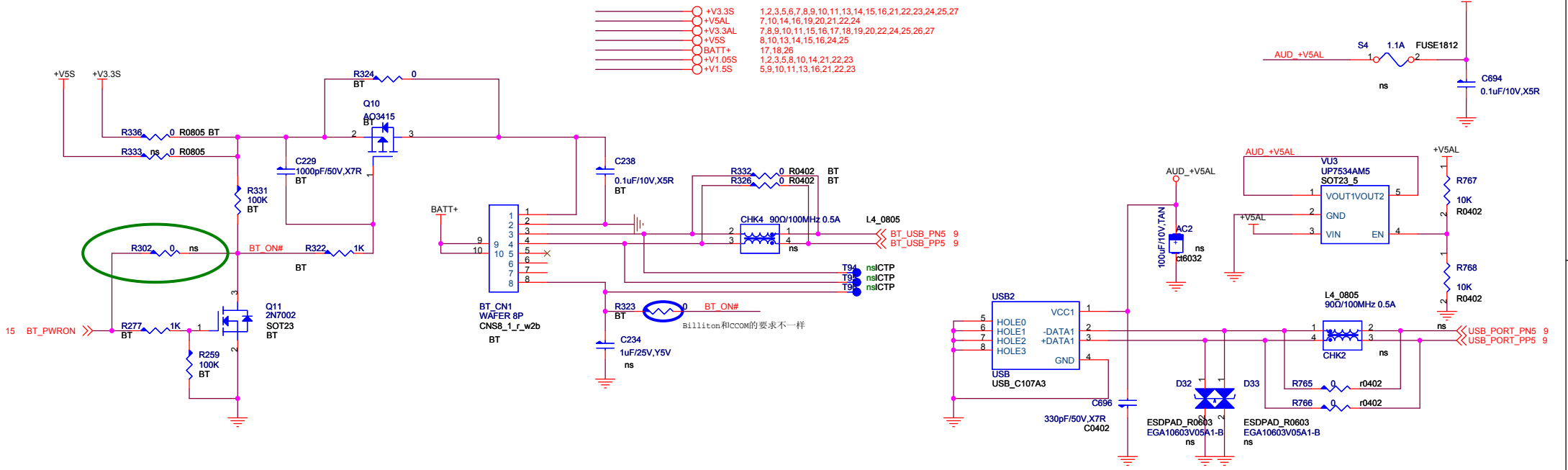
THD THREAD		HADS	
		Page Name	LVDS
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+V3.3AL	7,8,9,11,12,15,16,17,18,19,20,22,24,25,26,27
+V3.3S	1,2,3,5,6,7,8,9,11,12,13,14,15,16,21,22,23,24,25,27
+V1.05S	1,2,3,5,8,12,14,21,22,23
+V5AL	7,12,14,16,19,20,21,22,24
+V5S	8,12,13,14,15,16,24,25
+V1.5S	5,9,11,12,13,16,21,22,23
+V3.3A_RTC	8

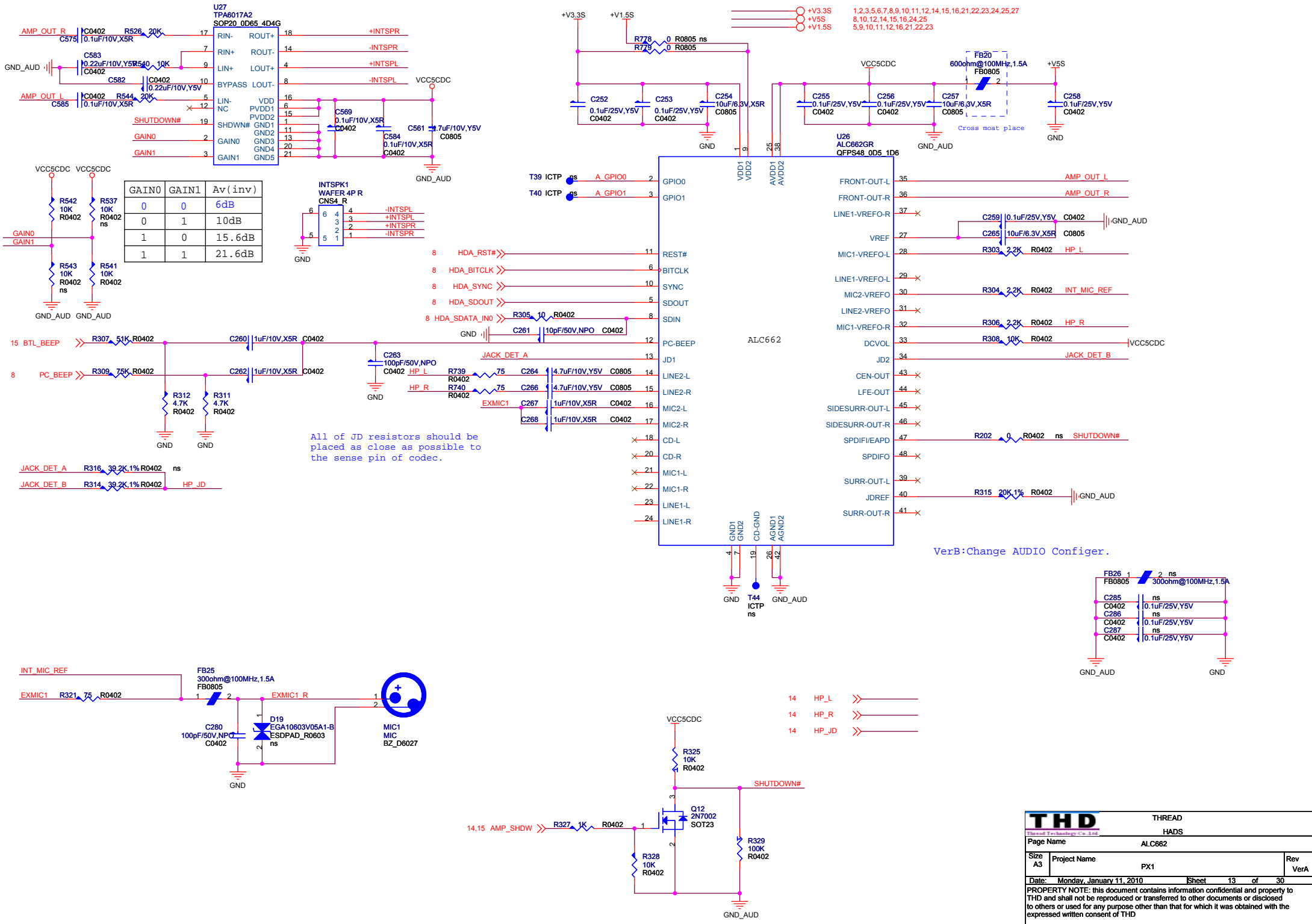


THD		THREAD	
HADS		HADS	
Page Name	ICH8		
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THD		THREAD	
		HADS	
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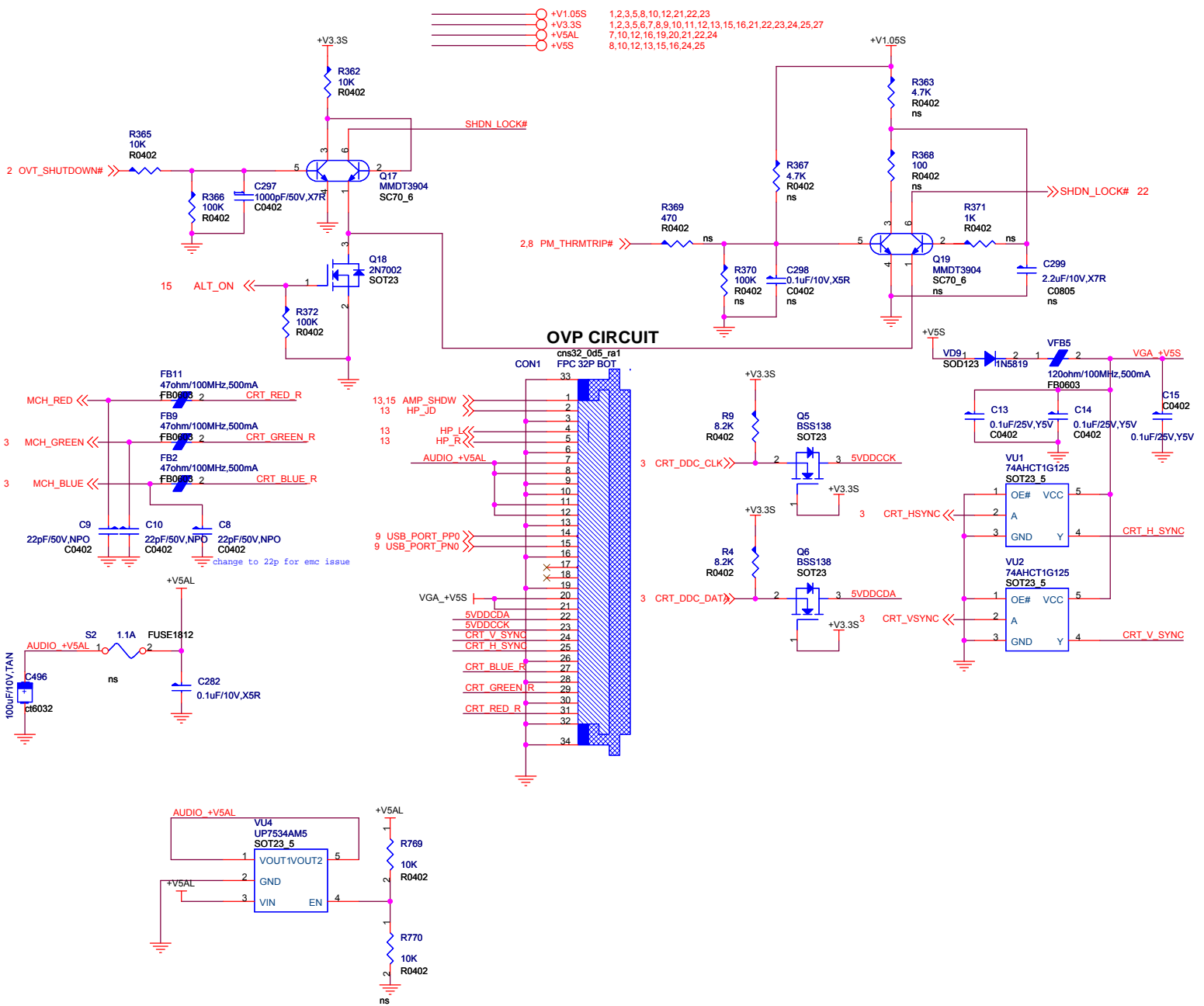


GAIN0	GAIN1	Av (inv)
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

All of JD resistors should be placed as close as possible to the sense pin of codec.

VerB:Change AUDIO Configur.

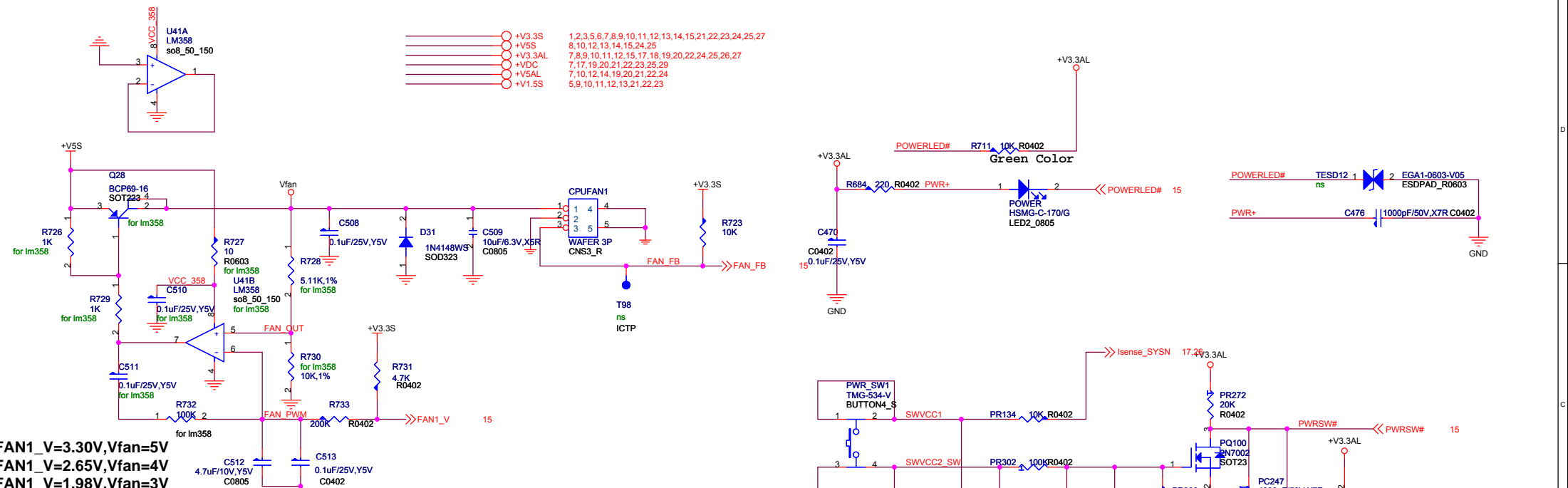
THD THREAD		HADS	
		Page Name	ALC662
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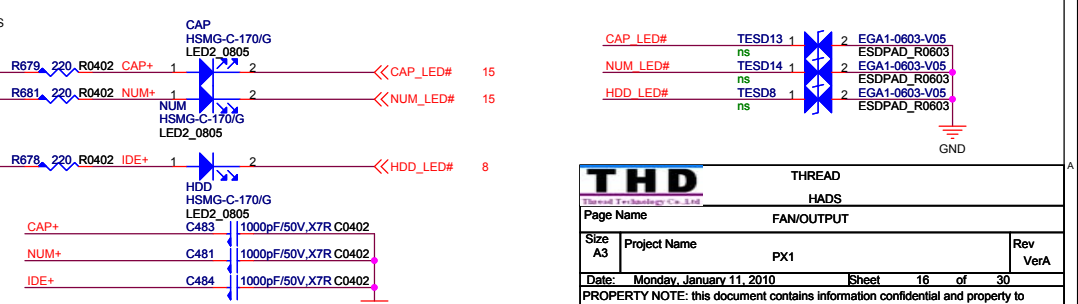
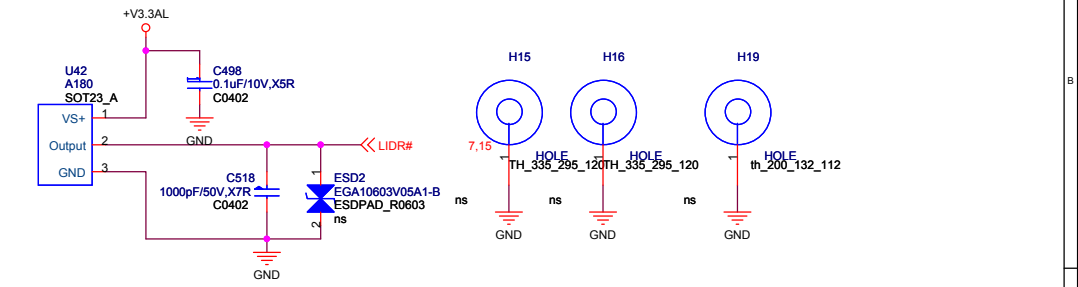
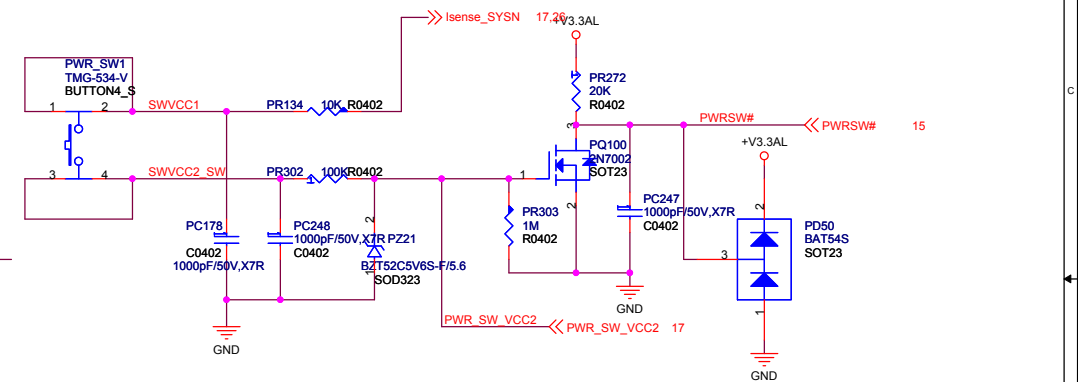
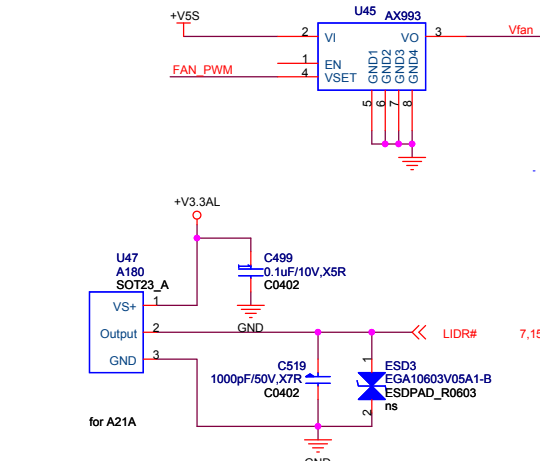
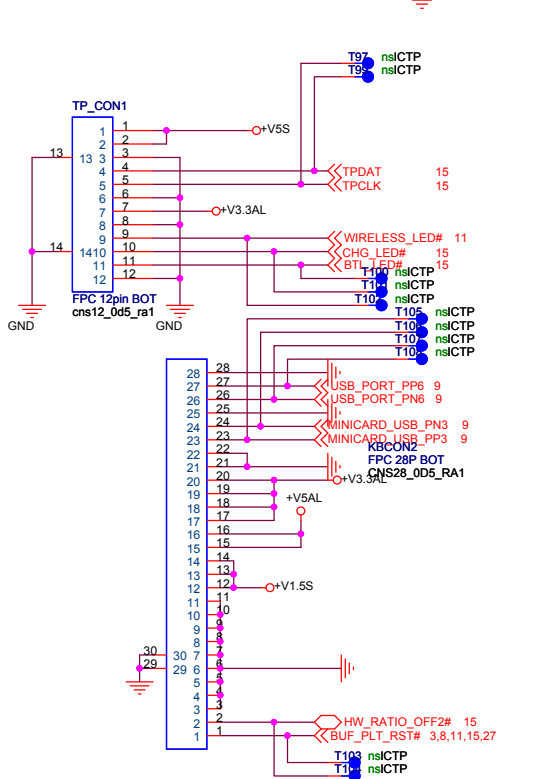
- +V1.05S 1,2,3,5,8,10,12,21,22,23
- +V3.3S 1,2,3,5,6,7,8,9,10,11,12,13,15,16,21,22,23,24,25,27
- +V5AL 7,10,12,16,19,20,21,22,24
- +V5S 8,10,12,13,15,16,24,25

THD Thread Technology Co., Ltd.		THREAD	
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+V3_3S	1,2,3,5,6,7,8,9,10,11,12,13,14,15,21,22,23,24,25,27
+V5S	8,10,12,13,14,15,24,25
+V3_3AL	7,8,9,10,11,12,15,17,18,19,20,22,24,25,26,27
+VDC	7,17,19,20,21,22,23,25,29
+V5AL	7,10,12,14,19,20,21,22,24
+V1.5S	5,9,10,11,12,13,21,22,23

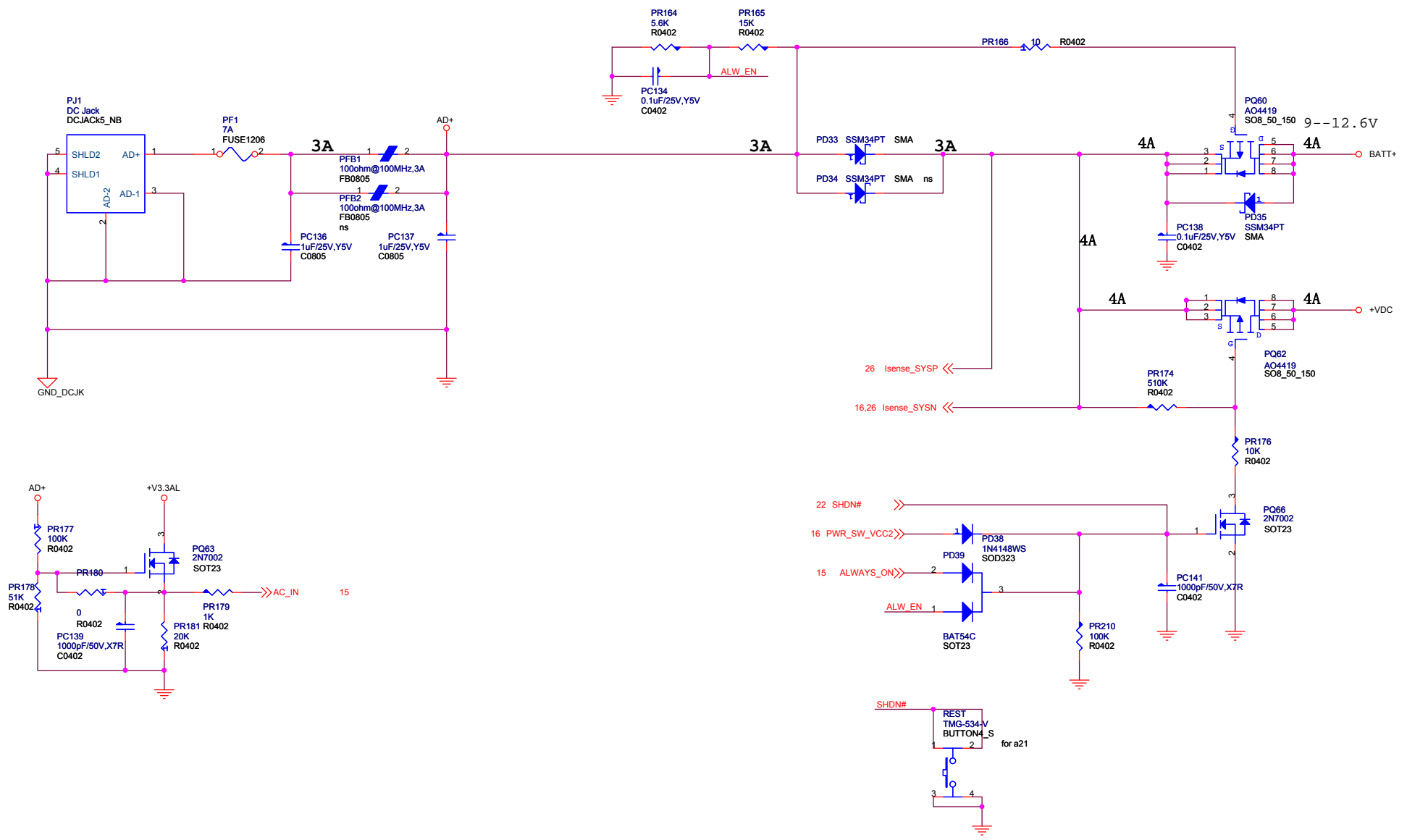


FAN1_V=3.30V, Vfan=5V
 FAN1_V=2.65V, Vfan=4V
 FAN1_V=1.98V, Vfan=3V



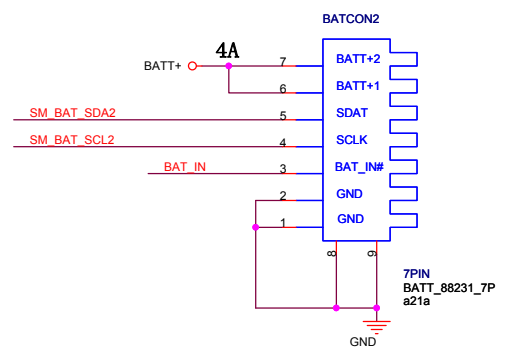
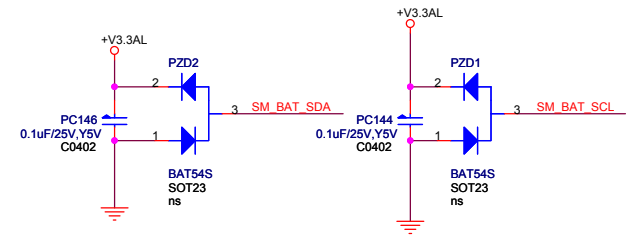
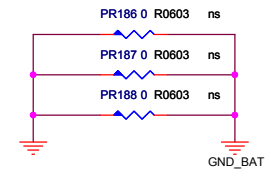
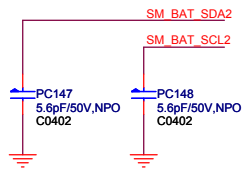
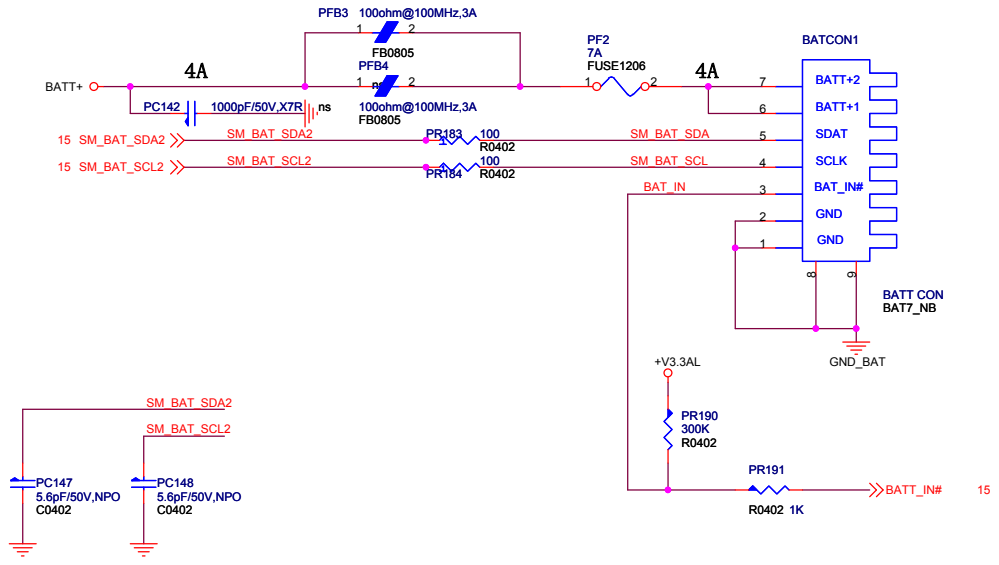
THD		THREAD	
THD		HADS	
Page Name		FAN/OUTPUT	
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BATT+ 12,18,26
 +VDC 7,19,20,21,22,23,25,29
 +V3.3AL 7,8,9,10,11,12,15,16,18,19,20,22,24,25,26,27

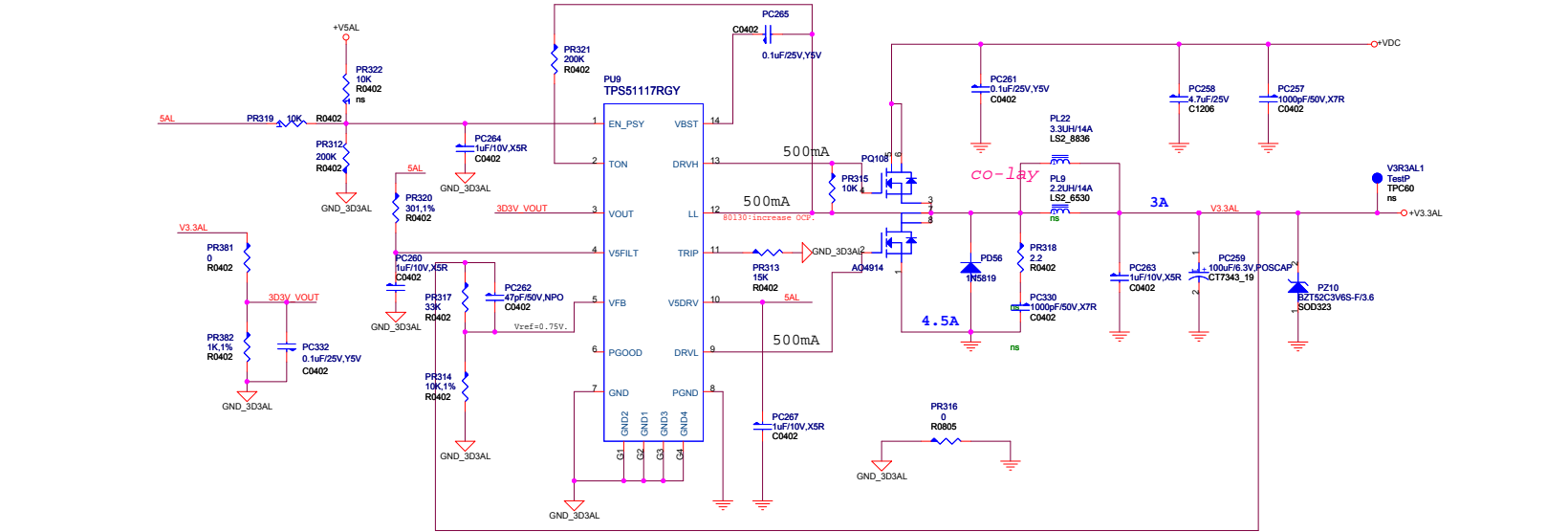
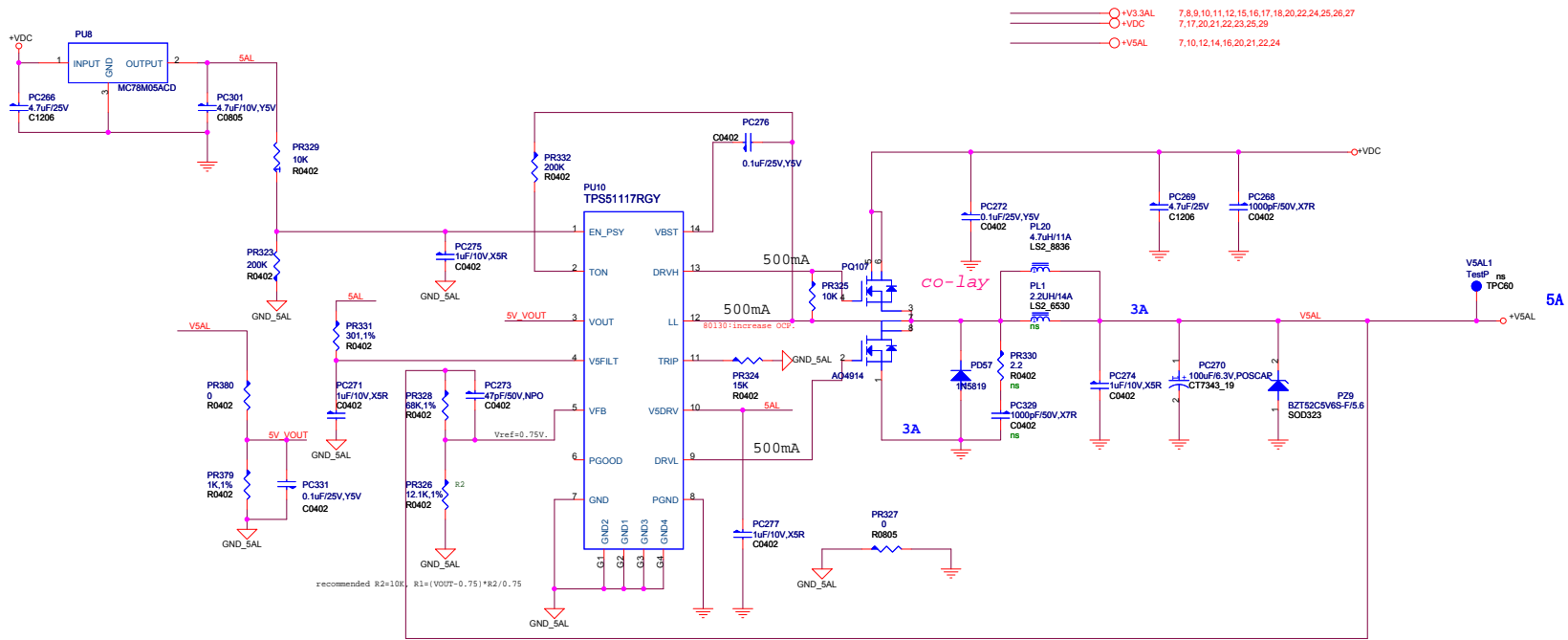


		THREAD HADS	
		Page Name AC_IN	
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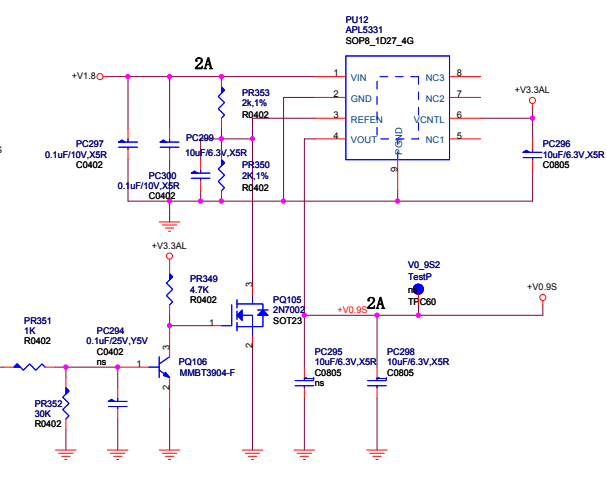
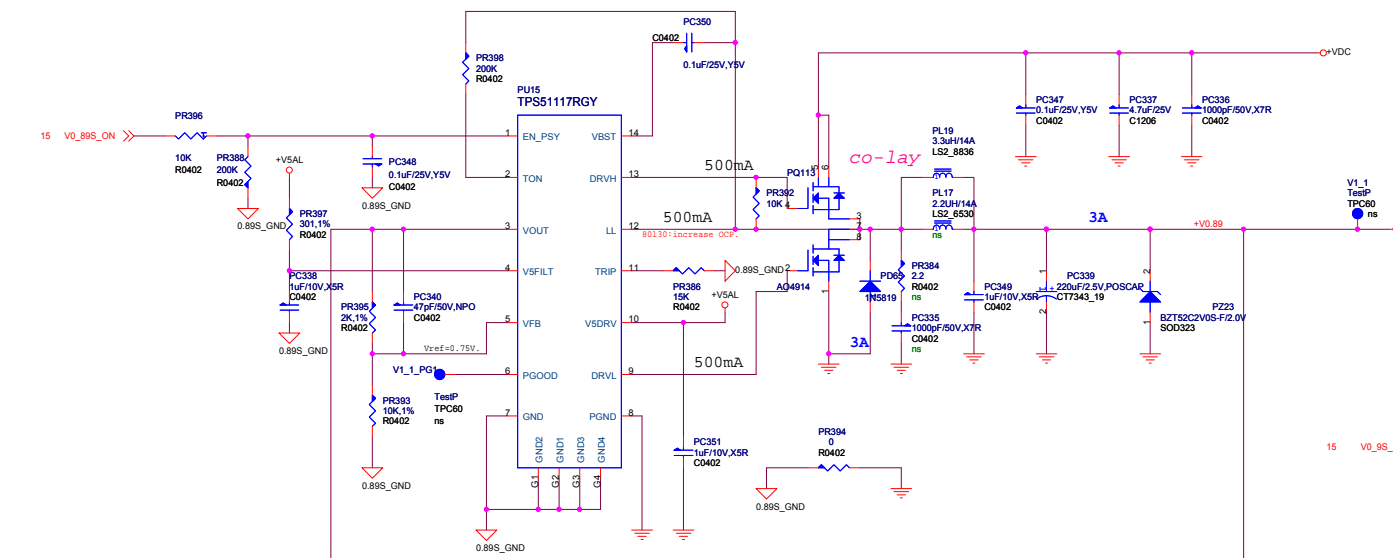
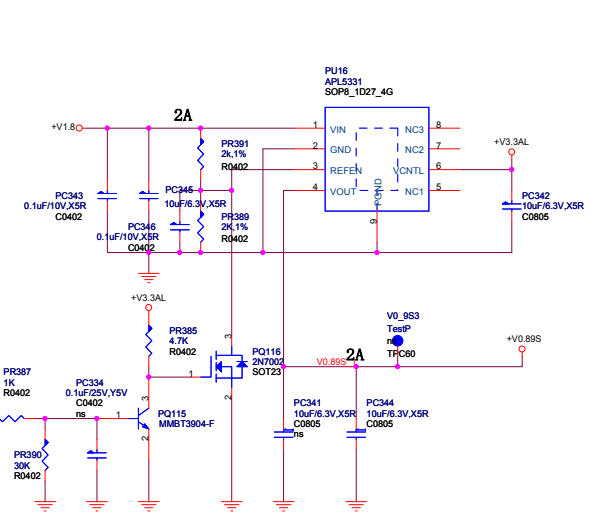
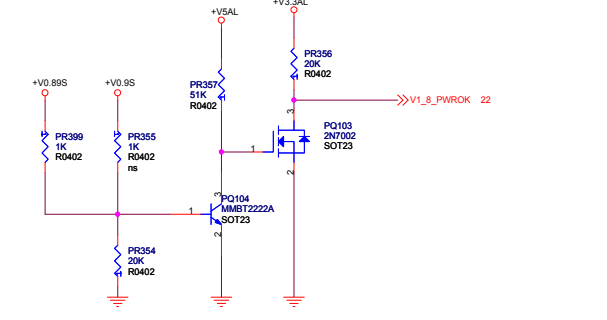
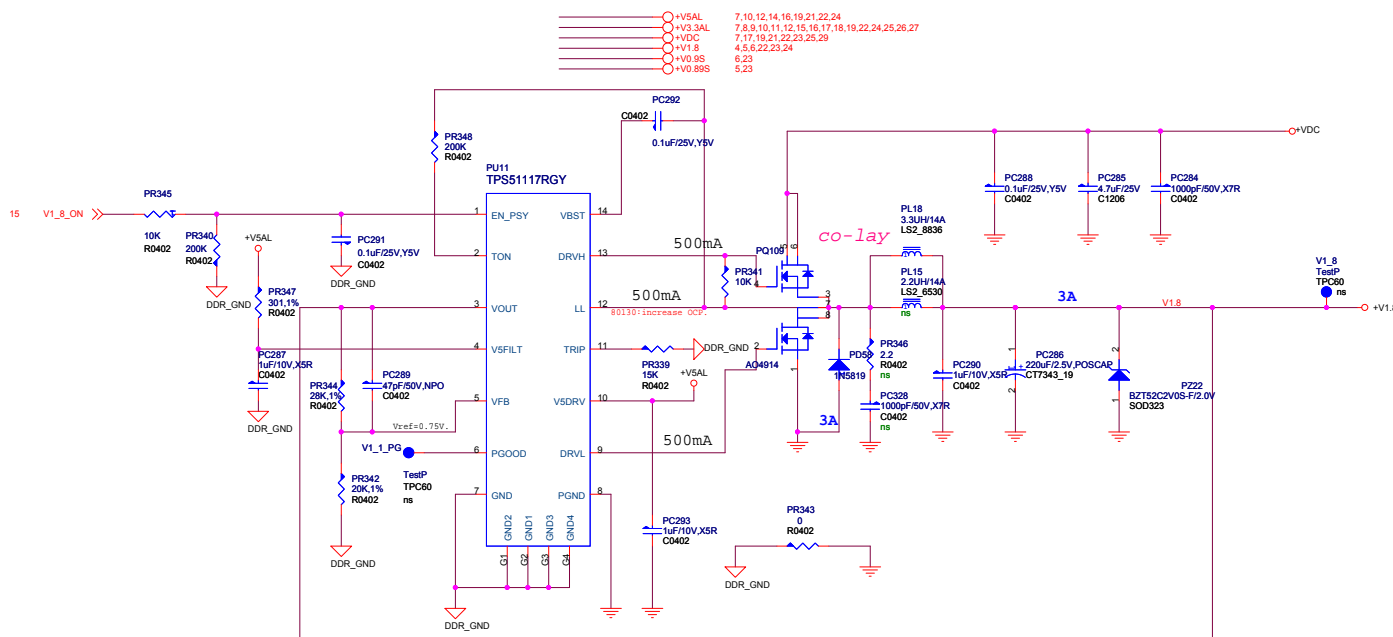
○ BATT+ 12,17,26
○ +V3.3AL 7,8,9,10,11,12,15,16,17,19,20,22,24,25,26,27



THD <small>Thread Technology Co., Ltd.</small>		THREAD HADS	
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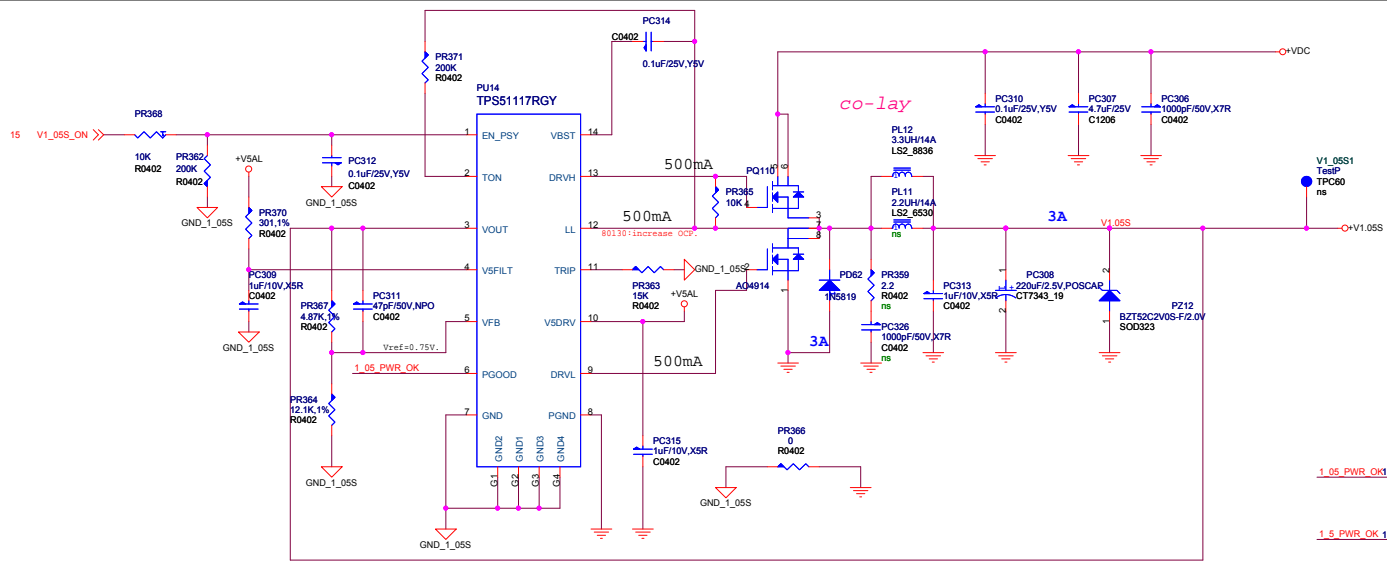


		THREAD	
		HADS	
Page Name		POWER OF ALWAYS	
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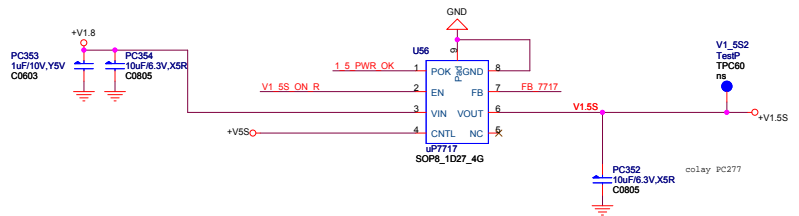
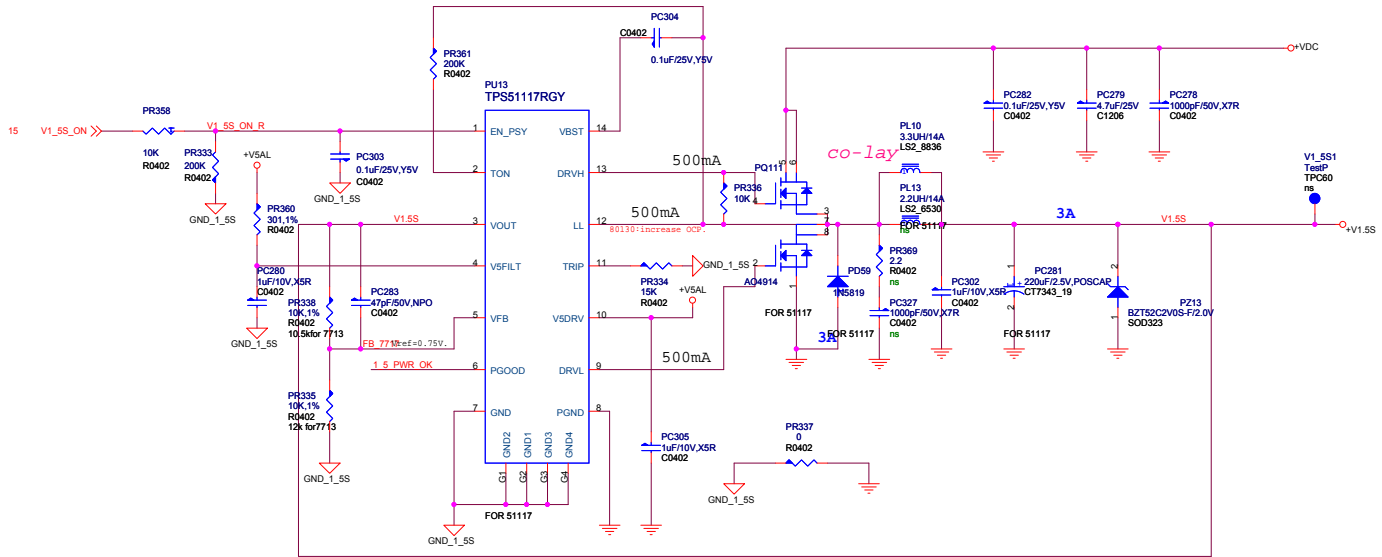
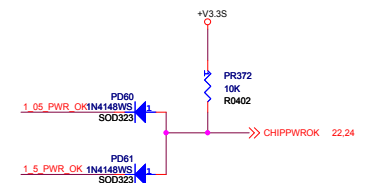
- +V5AL 7,10,12,14,16,19,21,22,24
- +V3.3AL 7,8,9,10,11,12,15,16,17,18,19,22,24,25,26,27
- +VDC 7,17,19,21,22,23,25,29
- +V1.8 4,5,6,22,23,24
- +V0.89S 6,23
- +V0.89S 5,23

THD The Hardware Design		THREAD	
		HADS	
Page Name	DDR2_POWER		
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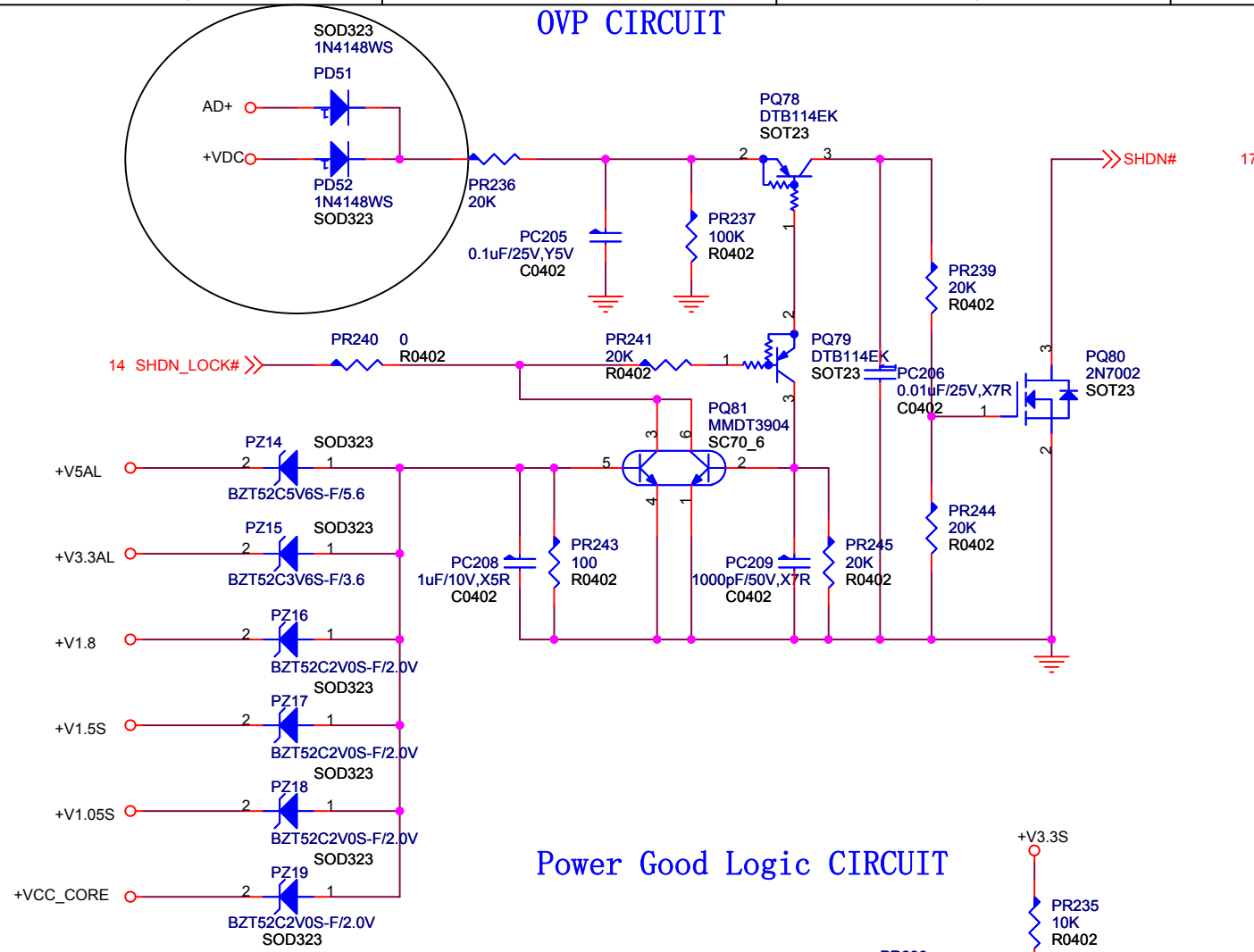
- +V1.8
- +V1.05S
- +V3.3S
- +V1.5S
- +V5AL
- +V5S

- 4,5,6,20,22,23,24
- 1,2,3,5,6,10,12,14,22,23
- 7,17,19,20,22,23,25,29
- 1,2,3,5,6,7,8,9,10,11,12,13,14,15,16,22,23,24,25,27
- 5,9,10,11,12,13,16,22,23
- 7,10,12,14,16,19,20,22,24
- 7,10,12,14,16,19,20,22,24



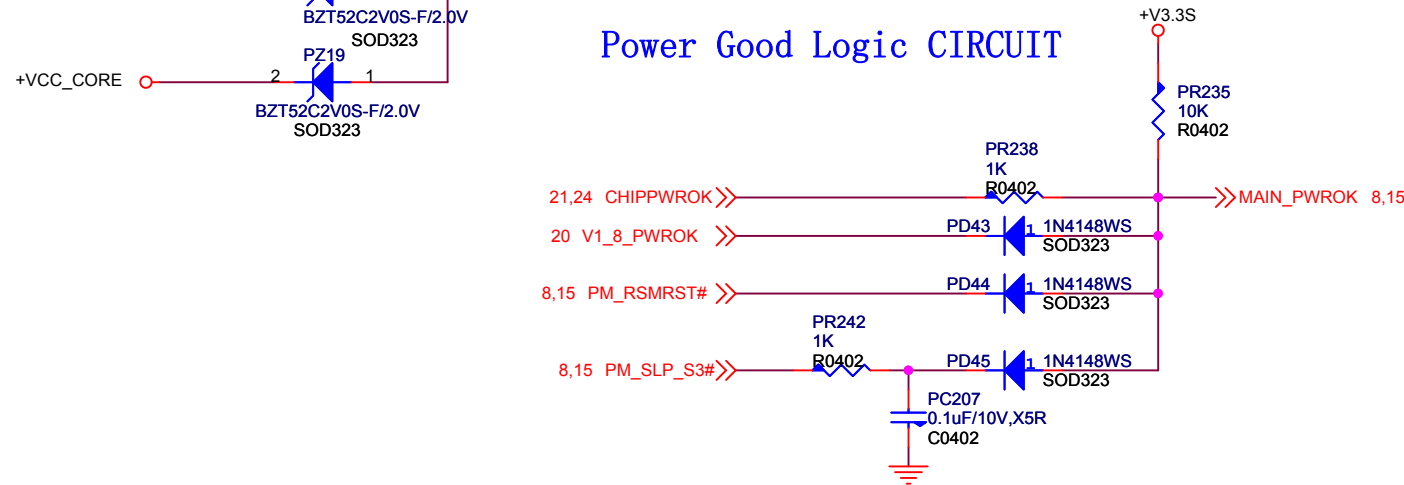
THD The High Definition Group		THREAD	
		HADS	
Page Name		POWER OF CHIPSET	
Size	Project Name	Rev	VerA
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OVP CIRCUIT

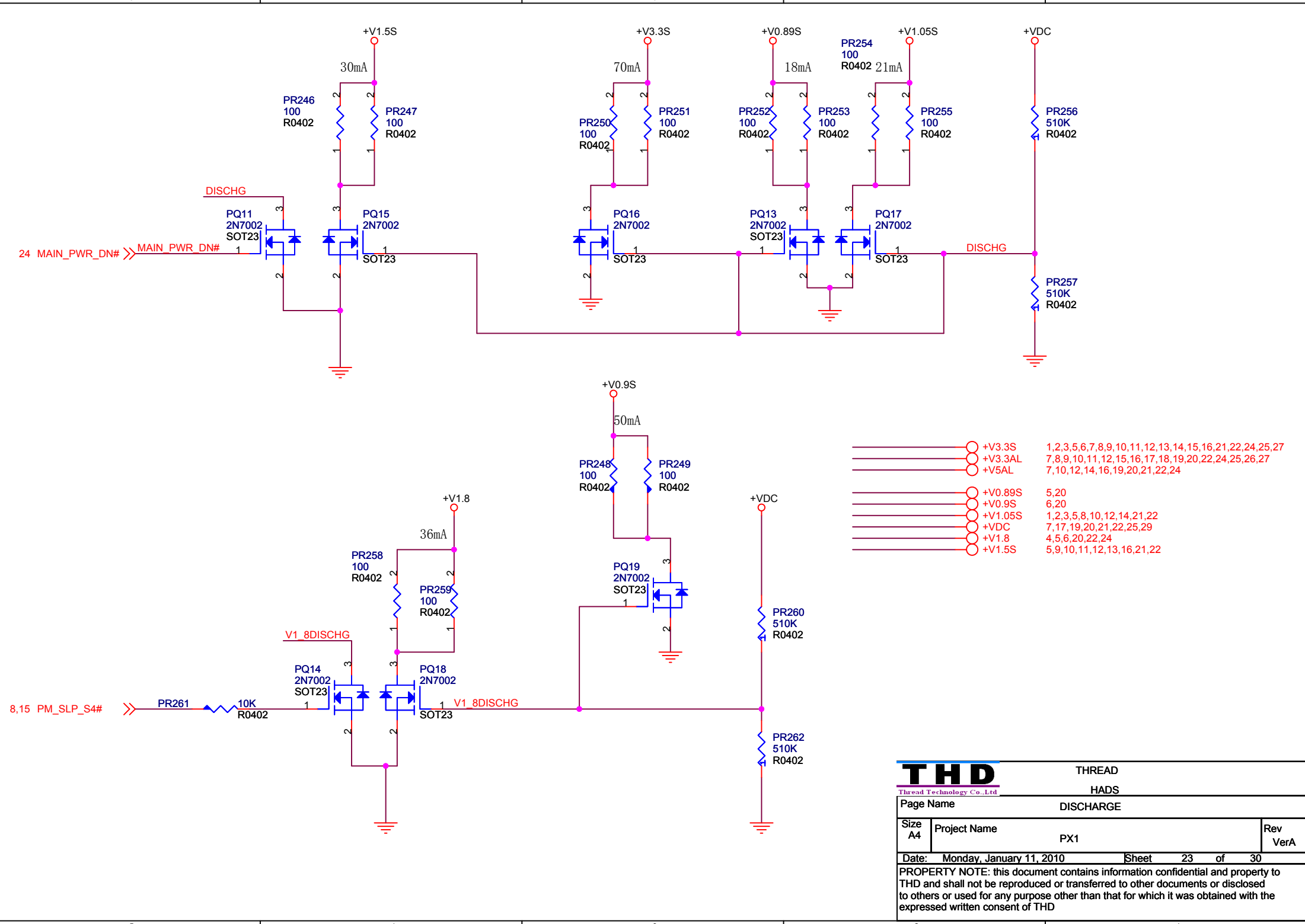


- +V3.3S 1,2,3,5,6,7,8,9,10,11,12,13,14,15,16,21,23,24,25,27
- +V5AL 7,10,12,14,16,19,20,21,24
- +V3.3AL 7,8,9,10,11,12,15,16,17,18,19,20,24,25,26,27
- +V1.05S 1,2,3,5,8,10,12,14,21,23
- +V1.5S 5,9,10,11,12,13,16,21,23
- +VCC_CORE 5,25
- +V1.8 4,5,6,20,23,24
- +VDC 7,17,19,20,21,23,25,29

Power Good Logic CIRCUIT



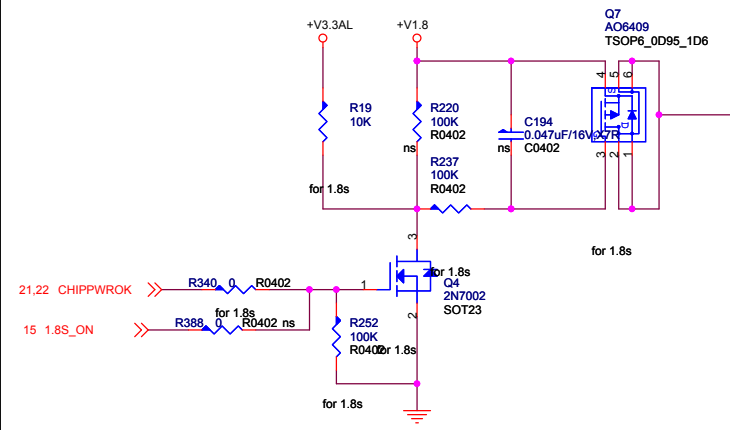
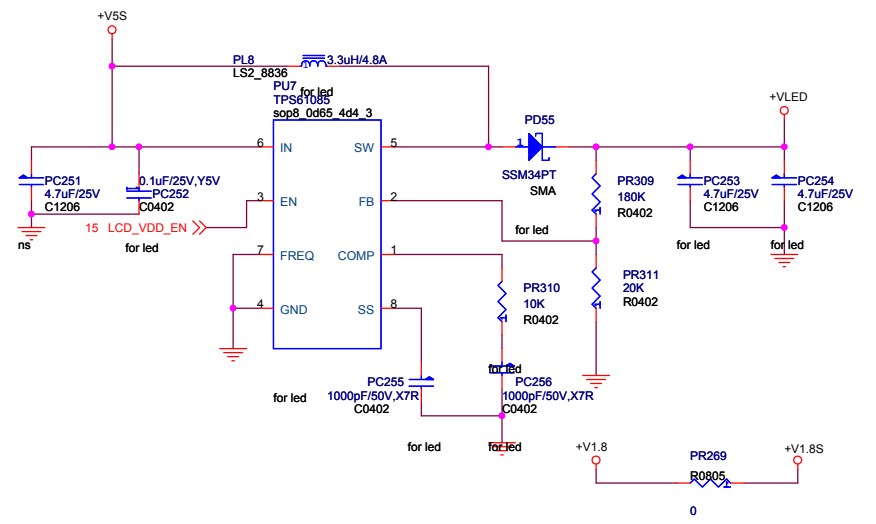
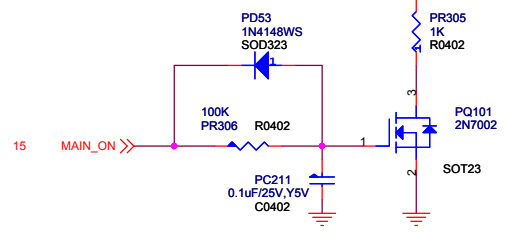
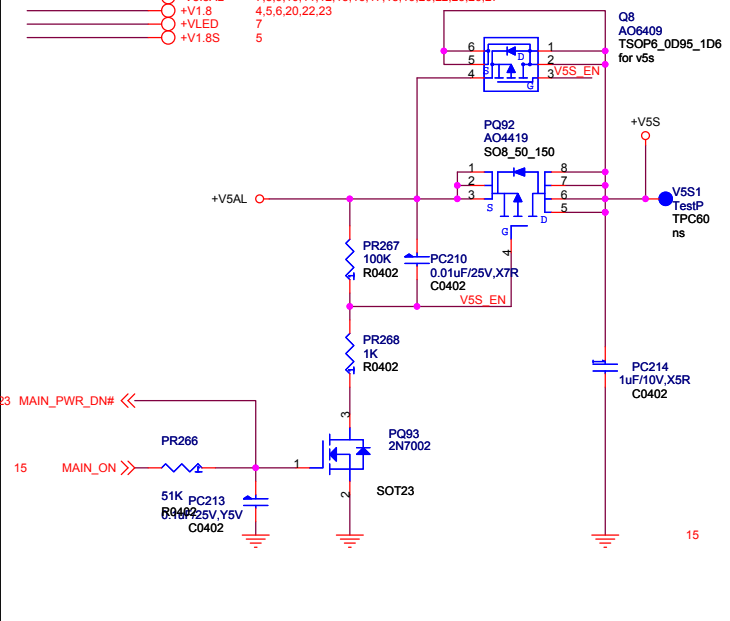
THD Thread Technology Co., Ltd.		THREAD	
		HADS	
Page Name		CHIPSET_POWER	
Size A4	Project Name	PX1	Rev VerA
Date:	Monday, January 11, 2010	Sheet	22 of 30
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- +V3.3S 1,2,3,5,6,7,8,9,10,11,12,13,14,15,16,21,22,24,25,27
- +V3.3AL 7,8,9,10,11,12,15,16,17,18,19,20,22,24,25,26,27
- +V5AL 7,10,12,14,16,19,20,21,22,24
- +V0.89S 5,20
- +V0.9S 6,20
- +V1.05S 1,2,3,5,8,10,12,14,21,22
- +VDC 7,17,19,20,21,22,25,29
- +V1.8 4,5,6,20,22,24
- +V1.5S 5,9,10,11,12,13,16,21,22

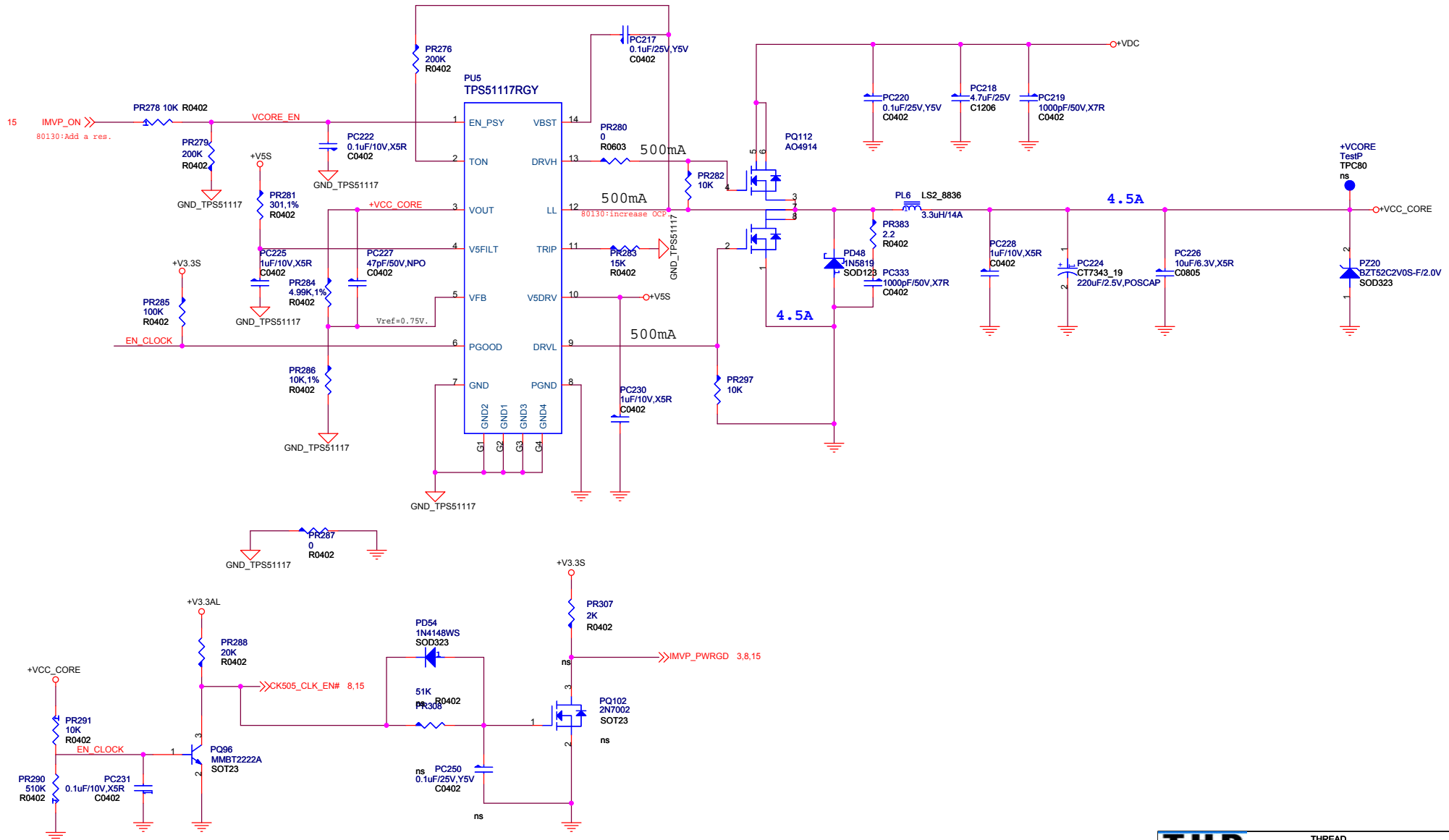
THD Thread Technology Co., Ltd.		THREAD	
		HADS	
Page Name		DISCHARGE	
Size A4	Project Name	PX1	Rev VerA
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- +V5S 8,10,12,13,14,15,16,25
- +V3.3S 1,2,3,5,6,7,8,9,10,11,12,13,14,15,16,21,22,23,25,27
- +V5AL 7,10,12,14,16,19,20,21,22
- +V3.3AL 7,8,9,10,11,12,15,16,17,18,19,20,22,25,26,27
- +V1.8 4,5,6,20,22,23
- +VLED 7
- +V1.8S 5

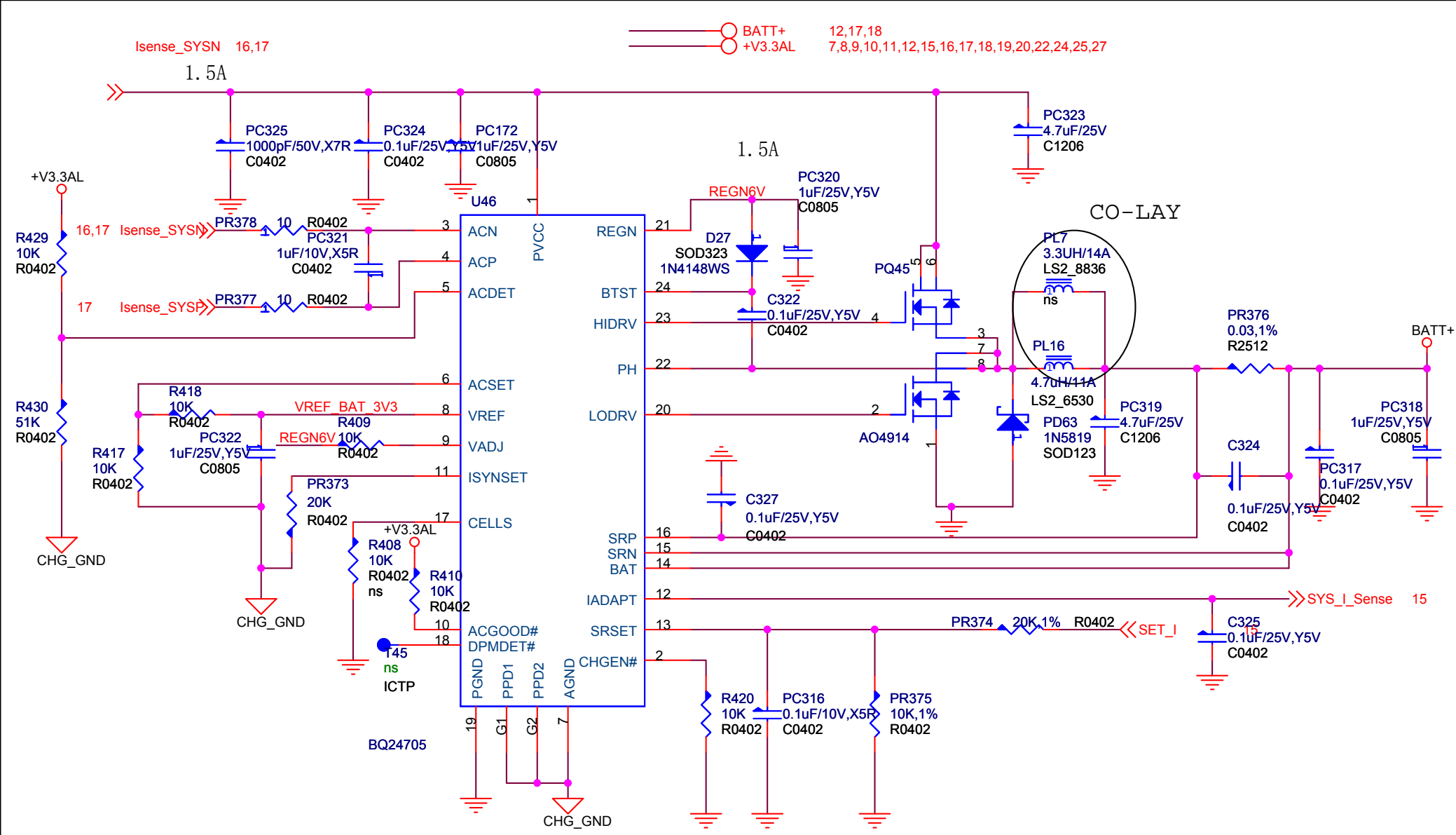


THD Thread Technology Co., Ltd.		THREAD	
		HADS	
Page Name		SYSTEM/VLED	
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- +VDC 7,17,19,20,21,22,23,29
- +V5S 8,10,12,13,14,15,16,24
- +VCC_CORE 5,22
- +V3.3S 1,2,3,5,6,7,8,9,10,11,12,13,14,15,16,21,22,23,24,27
- +V3.3AL 7,8,9,10,11,12,15,16,17,18,19,20,22,24,26,27

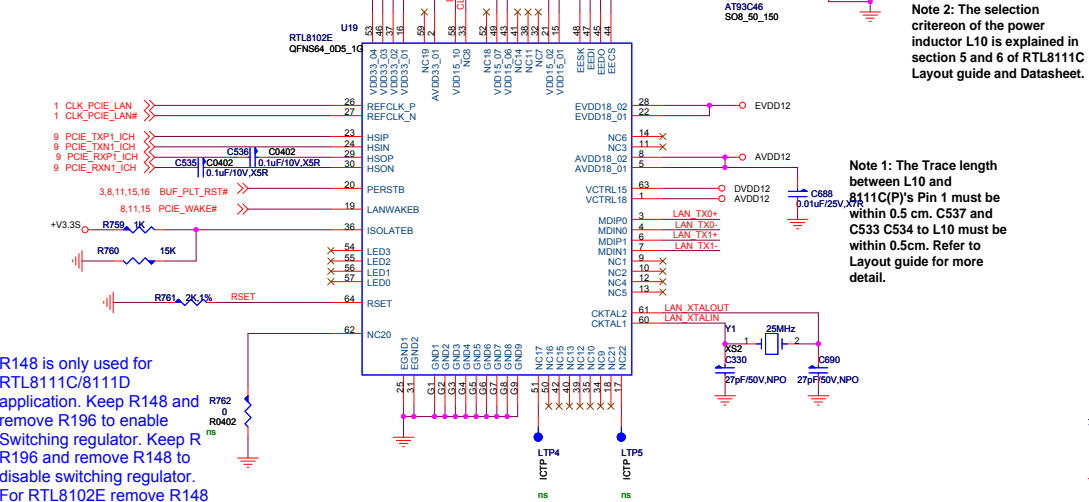


THD THREAD HADS		Page Name	VCCORE
		Size	A3
Date:	Monday, January 11, 2010	Sheet	25 of 30
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THD		THREAD	
Thread Technology Co.,Ltd		HADS	
Page Name		CHARGE	
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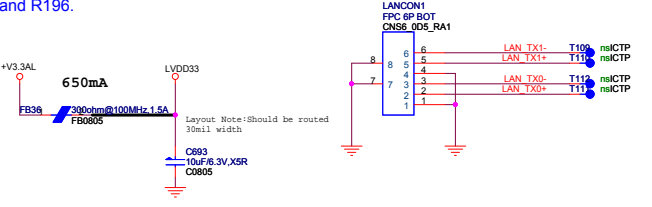
Power domain chart		RTL8111C
AVDD33		3.3V
AVDD18		1.2V
EVDD18		1.2V
DVDD15		1.2V



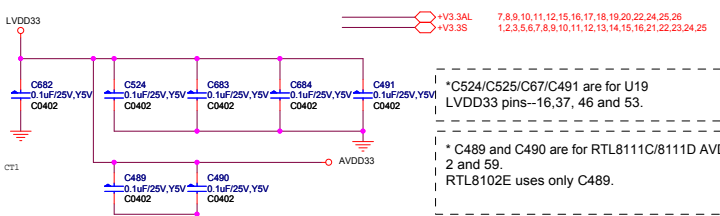
R148 is only used for RTL8111C/8111D application. Keep R148 and remove R196 to enable switching regulator. Keep R196 and remove R148 to disable switching regulator. For RTL8102E remove R148 and R196.

Note 1: The Trace length between L10 and 8111C(P)'s Pin 1 must be within 0.5 cm. C537 and C533 C534 to L10 must be within 0.5cm. Refer to Layout guide for more detail.

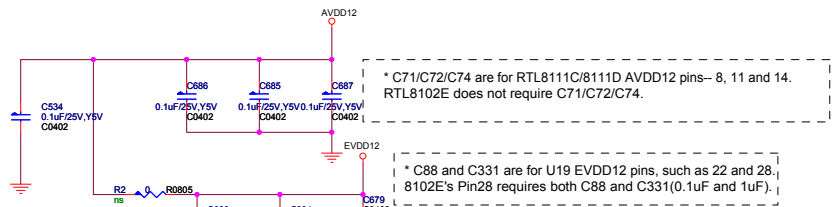
Note 2: The selection criterion of the power inductor L10 is explained in section 5 and 6 of RTL8111C Layout guide and Datasheet.



Layout Note: Should be routed 3mil width



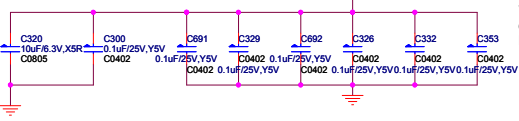
*C524/C525/C67/C491 are for U19 LVDD33 pins--16,37, 46 and 53.
*C489 and C490 are for RTL8111C/8111D AVDD33 pins--2 and 59.
RTL8102E uses only C489.



* C71/C72/C74 are for RTL8111C/8111D AVDD12 pins-- 8, 11 and 14. RTL8102E does not require C71/C72/C74.

* C88 and C331 are for U19 EVDD12 pins, such as 22 and 28. 8102E's Pin28 requires both C88 and C331(0.1uF and 1uF).

**** VERY IMPORTANT ****
Change C331 to 1uF in the 8102E application.
Co-Layout C331/C679 near PIN28.



*8111C and 8111D's Pin58 is AVDD which connects to DVDD because AVDD and DVDD are connected together.

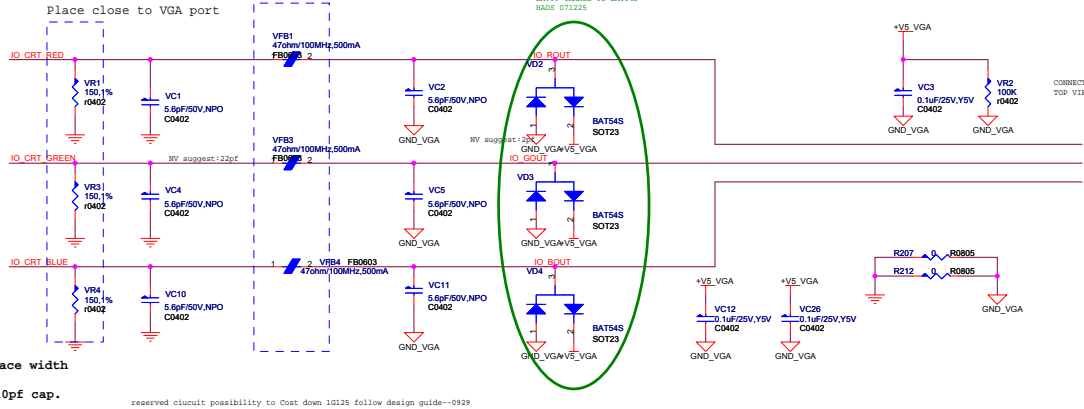
8111C/8111D uses only C300/C315/C329/C297/C326/C332/C353. (Pins-21,32,38,43,49,52,58)
8102E use only C26,C27,C28, C29 and C32. (Pins-15,21,43,49, 58)

CRT INTERFACE

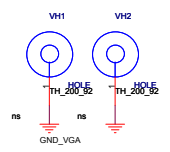
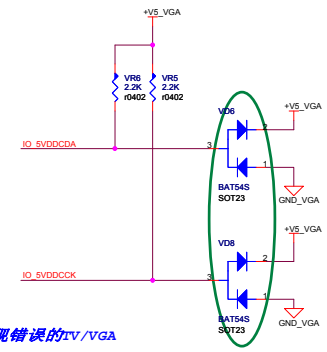
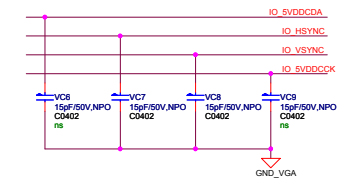
Cross moat place

Place close to VGA port

150ohm电阻前走线阻抗50ohm
(From GPU to CONN)
150ohm电阻到S_VIDEO CONN
走线阻抗75ohm

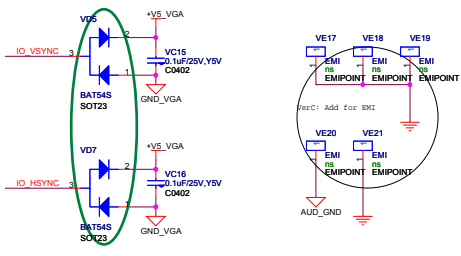


VGA CONNECTOR

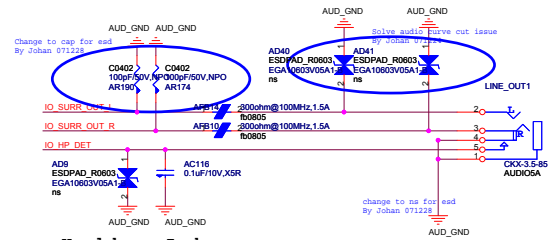
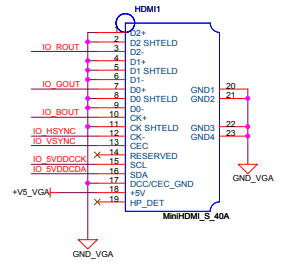
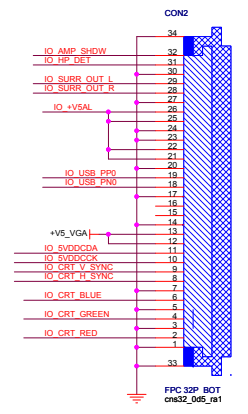


ESD:
NV suggest use +3.3V
Layout note:
1. +3.3V and GND Route >15mils trace width
2. No more than 75mils
3. ESD diode should no more than 10pf cap.

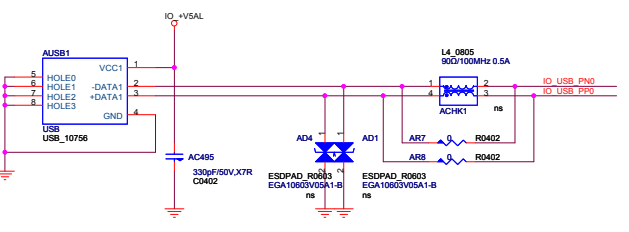
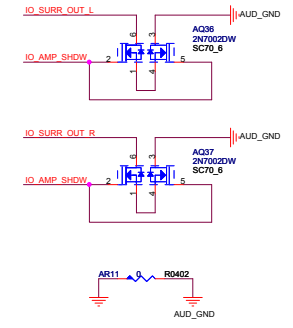
reserved circuit possibility to Cost down 10125 follow design guide--0929



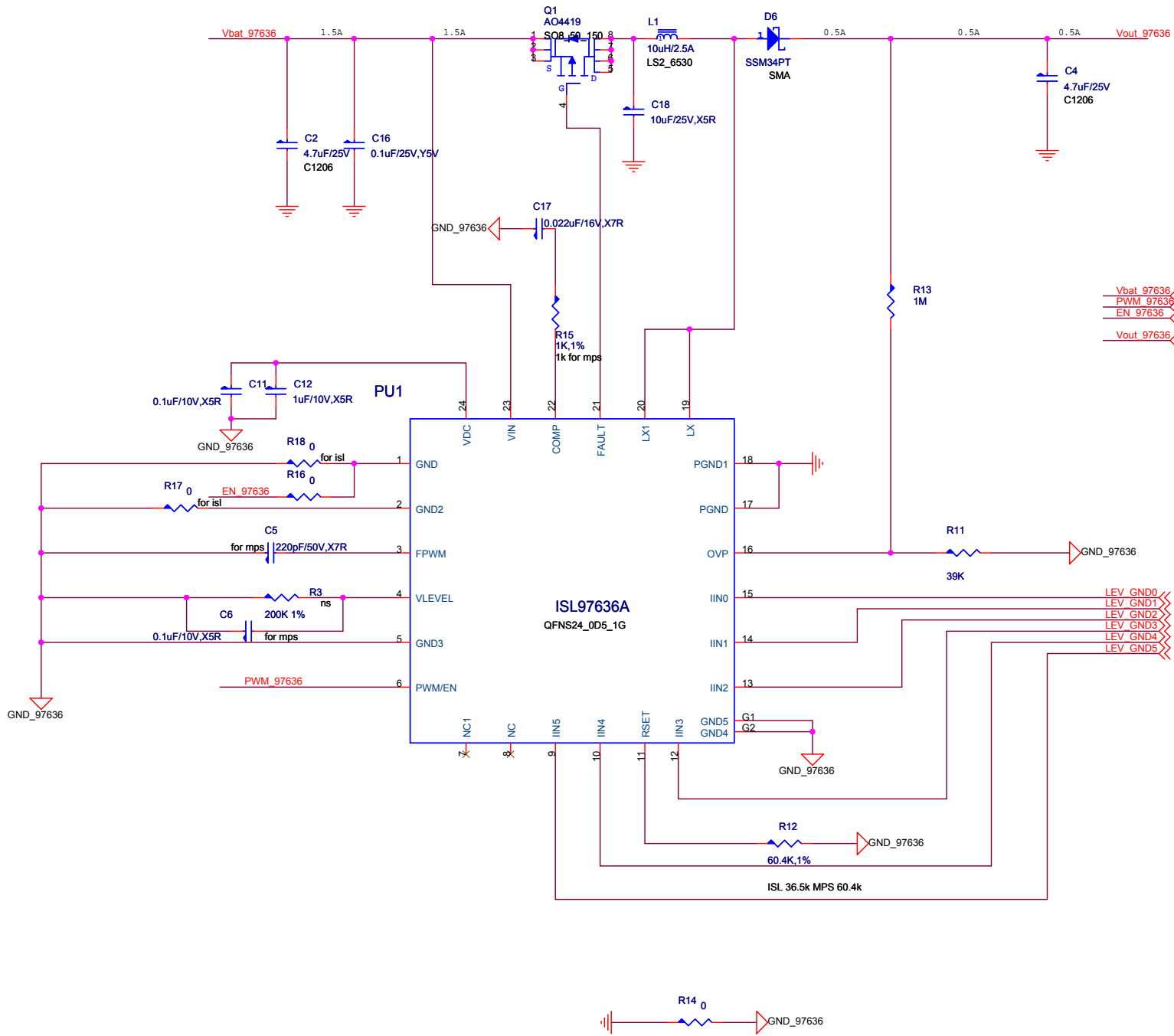
Note: VGA 注意阻抗控制, 否则易出现错误的TV/VGA monitor检测



Headphone Jack
INPUT: HEADPHONE/LINE-OUT
OUTPUT: FRONT L/R
used for enhancing Audio quality and ESD ability.



THD		THREAD	
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Vbat_97636 << +VDC 7,17,19,20,21,22,23,25
 PWM_97636 << BKL_PWM_CONN 7
 EN_97636 << BKL_ON_CON 7
 Vout_97636 << VLED_C 7

LEV_GND0 << LEV_GND0 7
 LEV_GND1 << LEV_GND1 7
 LEV_GND2 << LEV_GND2 7
 LEV_GND3 << LEV_GND3 7
 LEV_GND4 << LEV_GND4 7
 LEV_GND5 << LEV_GND5 7

THD		THREAD	
Thread Technology Co., Ltd		linux	
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