1. All resistance values are in ohms, 0.1 watt +/- 5%.
2. All capacitance values are in microfarads.
3. All crystals & oscillator values are in hertz.
### Design-Specific Rules

#### Layer-specific rules for 110-ohm differential impedance

<table>
<thead>
<tr>
<th>Rule</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.200 MM</td>
<td>Centered from edge</td>
<td>2.5 MMTOP, BOTTOM</td>
</tr>
</tbody>
</table>

#### Portable-specific Override Rules

<table>
<thead>
<tr>
<th>Rule</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.300 MM</td>
<td>Top Padding</td>
<td>TOP,BOTTOM</td>
</tr>
</tbody>
</table>

## Board Stack-Up and Construction

### Board Holes

#### Heatsink Mounts

<table>
<thead>
<tr>
<th>Mount</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ZT0200</td>
<td>Left CPU</td>
</tr>
<tr>
<td>ZT0201</td>
<td>Upper RT GPU</td>
</tr>
<tr>
<td>ZT0202</td>
<td>Lower Toscabar 1394</td>
</tr>
<tr>
<td>ZT0203</td>
<td>LMR CPU</td>
</tr>
</tbody>
</table>

#### Chassis Mounts

<table>
<thead>
<tr>
<th>Mount</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ZT0210</td>
<td>BATT.CHR</td>
</tr>
<tr>
<td>ZT0212</td>
<td>M3/4-0.7</td>
</tr>
</tbody>
</table>

#### Inverter

<table>
<thead>
<tr>
<th>Mount</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ZT0221</td>
<td>M3/4-0.7</td>
</tr>
</tbody>
</table>

#### Board Stack-Up and Construction

- **100% Area Defined Around BOMs to Ensure BGA祖国 by Fan-Out**
- **Layer-Specific Rules for 90-ohm differential impedance**
- **Layer-Specific Rules for 60-ohm single-ended impedance**

## BOM Options

<table>
<thead>
<tr>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>341S1736</td>
<td>IC, BOOTROM</td>
</tr>
<tr>
<td>338S0252</td>
<td>IC, GPU</td>
</tr>
<tr>
<td>337S3163</td>
<td>U36001</td>
</tr>
</tbody>
</table>

## Module Components

### Board Information

- **Fabrication Method**: Conventional Construction with FEI USA
- **Revision**: REV.
- **Material**: SHLD-SM
- **Surface Mount Technology**: 1999
- **Board Size**: 12345678
- **Chassis Mounts**: ZT0200, ZT0201, ZT0202, ZT0203
- **Hole-Via-P5RP25**: 1, 2, 3, 4, 5, 6, 7, 8
- **Common, Alternate**: gQ16C, gQ16C_BST, Q16C_BST_VRAM_S, VRAM_SAMSUNG
- **I2C Maxbus**: I244, I245, I246, I247
- **GND Chassis**: GND_CHASSIS_BATT, GND_CHASSIS_UPPER_DVI
- **CPU Vcore**: CPU_VCORE_3STATES, I2VCORE_1V5, I2VCORE_BURST

### BOM Options

<table>
<thead>
<tr>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>12.5 MM</td>
<td>0.1 MM 15.0 MM</td>
</tr>
</tbody>
</table>

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REVISION HISTORY

PRE-EVT
04/04/2005 - Made DDR2 and FB pin swaps as requested by CM
04/06/2005 - Chassis grounds partitioned as in previous products
04/06/2005 - Made additional FB pin swaps
04/11/2005 - Changed battery sense resistor to 0.006 ohm (R1250)
04/12/2005 - Corrected MIN_LINE_WIDTH properties on PP3V3_PWRON
04/13/2005 - Added 1.5V DVO option to GPU
04/14/2005 - Removed series R isolating VG from digital ground on FW ports (per design guide)
04/15/2005 - Moved FB series R to page 6
04/18/2005 - Corrected ENET power rail to PWRON from RUN (for Wake-on-LAN)
04/20/2005 - Added page 6 and modified pages 11,35,81 for design specific pin swaps
04/21/2005 - Corrected STOP_AGP_L net name (hooked to I2 now) and removed redundant pullup
04/22/2005 - Corrected pulldown resistor value for 0.006 ohm battery current sense
04/23/2005 - Changed 220uF CPU VCore caps to 330 uF LF caps
04/24/2005 - Corrected MIN_LINE_WIDTH property on GND to 0.2 mm for TMDS parts
04/25/2005 - Corrected line and neck width properties
04/26/2005 - Added extra cap at input to I2 USBAVDD
05/03/2005 - Added pulldown to Vesta LPWR_1394
05/04/2005 - Added pulldowns to unused serial debug signals (DTR/RTS)
05/05/2005 - Disconnected FW_POWERDOWN from Vesta LPWR_1394 pin
05/06/2005 - Various Pb-free component replacements
05/10/2005 - Various Pb-free component replacements
05/13/2005 - Pinswaps for I2 RPAKs to match up with Q41C style layout
05/14/2005 - Various Pb-free component replacements
05/18/2005 - Added TBEN sync circuit
05/19/2005 - Various Pb-free component replacements
05/20/2005 - Corrected AGP_INT_L connection between I2 and GPU
05/21/2005 - Corrected VGA sync connections at GPU
05/23/2005 - Release as REV 01 for Pre-EVT/EVT
05/24/2005 - Added NEC USB2 controller
05/25/2005 - Various Pb-free component replacements
05/26/2005 - Removed SMS PIC microcontroller
05/27/2005 - Various Pb-free component replacements
05/30/2005 - Various Pb-free component replacements
06/01/2005 - Corrected FireWire VP caps to 50V
06/02/2005 - Various Pb-free component replacements
06/03/2005 - Various Pb-free component replacements
06/04/2005 - Various Pb-free component replacements
06/05/2005 - Various Pb-free component replacements
06/06/2005 - Various Pb-free component replacements
06/07/2005 - Various Pb-free component replacements
06/08/2005 - Various Pb-free component replacements
06/09/2005 - Various Pb-free component replacements
06/10/2005 - Various Pb-free component replacements
06/11/2005 - Various Pb-free component replacements
06/12/2005 - Various Pb-free component replacements
06/13/2005 - Various Pb-free component replacements
06/14/2005 - Various Pb-free component replacements
06/15/2005 - Various Pb-free component replacements
06/16/2005 - Various Pb-free component replacements
06/17/2005 - Various Pb-free component replacements
06/18/2005 - Various Pb-free component replacements
06/19/2005 - Various Pb-free component replacements
06/20/2005 - Various Pb-free component replacements
06/21/2005 - Various Pb-free component replacements
06/22/2005 - Various Pb-free component replacements
06/23/2005 - Various Pb-free component replacements
06/24/2005 - Various Pb-free component replacements
06/25/2005 - Various Pb-free component replacements
06/26/2005 - Various Pb-free component replacements
Enhanced MAC-1 Test Coverage

Functional test points use a P6 pad placed on bottom side.

- Place within 25 mm of power supply.
- Place within 25 mm of ALS connector.
- Place within 25 mm of battery connector.
- Place within 25 mm of debug connector.
- Place within 25 mm of right USB connector.
- Place within 25 mm of left USB connector.

- Place 5-10 GND TPs.
Nets not requiring TP's due to JTAG
12.8V PBUS SUPPLY

PMU SUPPLY

BOOTSTRAP SYSTEM FROM ADAPTER, MAIN BATTERY, OR BACKUP BATTERY

www.vinafix.vn
POWERDOWN DELAY IS AROUND 4MS-15.6MS, VIA RC NETWORK
3V START TO TURN ON ~25MS AFTER =5V3V3PWRON_EN_L goes low
5V START TO TURN ON ~12.5MS =5V3V3PWRON_EN_L goes low

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2.5V SWITCHER

SW 
SGND 
PGND 
PAD 
THERM 
SVIN 
PVIN 
PGOOD 
VFB 
ITH 
SYNC/MODE 
RUN/SS 
RT 
G 
D 
S 

D 
SIZE 

OFSHT 

DRAWING NUMBER 

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12345678 

12345678 

CERM 
6.3V20% 
22UF 
1206 

C1700 
MF-LF 
1/16W 
1% 
15.0K 
4022 
1 
R1720 

100PF 
5% 
25V 
CERM 
603 
2 
1 
C1721 
SM 
21 
XW1700 

CRITICAL 

LTC3412 
TSSOP-LF 

4 
17 
6 
15 
14 
11 
10 

1 
8 
7 
5 
3 

16 
9 
2 
13 
12 
3 

U1700 

CERM 
50V5% 
100PF 
402 
2 
1 
C1720 

402K 
MF-LF 
1/16W 
1% 
110K 
4022 
1 
R1730 

MF-LF 
1/16W 
1% 
75K 
4022 
1 
R1732 

MF-LF 
1/16W 
1% 
309K 
4022 
1 
R1733 

CERM 
50V10% 
470PF 
402 
2 
1 
C1722 

4.7M 
5% 
1/16W 
MF-LF 
402 2 
1 
R1722 

MF-LF 
1/16W 
5% 
0 
4022 
1 
R1723 

MF-LF 
1/16W 
1% 
309K 
4022 
1 
R1733 

CRITICAL 
1.0uH-3.48A 
SM-LF 
21 
L1700 

22UF 
20% 
6.3V 
CERM 
1206 
2 
1 
C1701 

2N7002DW-X-F 
SOT-363 

4 
5 
3 
Q1740 

10% 
25V 
X7R 
402 
1000pF 
21 
C1780 

TSSOP 
SI6467BDQ-E3 
7632 
4 
8 
51 

Q1780 

X5R 
6.3V20% 
10UF 
603 
2 
1 
C1781 

22UF 
20% 
6.3V 
CERM 
1206 
2 
1 
C1711 

051-6929 

17 
03 
115 

SYNC_DATE=N/ASYNC_MASTER=N/A
2.5V Supply

LTC3412_GND 
VOLTAGE=0V 
MIN_LINE_WIDTH=0.5 mm 
MIN_NECK_WIDTH=0.25 mm 

LTC3412_ITH 
LTC3412_RUNSS 
LTC3412_ITH_RC 
LTC3412_VFB 
LTC3412_VFB_DIV 
LTC3412_SYNC 
LTC3412_RT 
LTC3412_SW 

=2V5PWRON_L 
=PP3V3_PWRON_LTC3412 
=PP2V5_PWRON_RUNFET 
=PP2V5_PWRON_REG 
2V5RUN_EN_L 
=PP2V5_RUN_RUNFET 
26 
10 
26 
10 
26 
10 
929 
10 
26 
10 
876 
278 

=2V5PWRON_EN_L 

2V5PWRON_PGOOD 
LTC3412_ITH 
LTC3412_RUNSS 
LTC3412_ITH_RC 
LTC3412_VFB 
LTC3412_VFB_DIV 
LTC3412_SYNC 
LTC3412_RT 
LTC3412_SW 

=2V5PWRON_L 
=PP3V3_PWRON_LTC3412 
=PP2V5_PWRON_RUNFET 
=PP2V5_PWRON_REG 
2V5RUN_EN_L 
=PP2V5_RUN_RUNFET 

www.vinafix.vn
Vout = 0.8V * (1 + (Rb2 / (Rb1 + Rb2)))

If I2VCORE_BURST is selected:

\[ \text{IBurst} = \frac{(V_{\text{burst}} - 0.2V)}{0.8V} \times \frac{3.75A}{V_{\text{burst}}} \]

I2 Power Supplies

I2 PLL LDO

Vout = 1.22V * (1 + (Ra / (Rb1 + Rb2)))

Iadj = 30nA at 25°C

Vout = 0.8V * (1 + (Ra / (Rb1 + Rb2)))

MIN_NECK_WIDTH = 0.15 mm

MIN_LINE_WIDTH = 0.20 mm

For BOM options provided by this page:

- I2VCORE_PGOOD

Signal aliases required by this page:

- =PP1V5_PWRON_I2PLL_LDO
- =PPVIN_PWRON_I2PLLVDD
- =PPVCORE_PWRON_I2_REG
- =PP2V7R5V5_PWRON_I2VCORE

Power aliases required by this page:

Page Notes

www.vinafix.vn
Page Notes

Power aliases required by this page:
- PP3V3_PWRON_I2_GPIO
- PP3V3_PCI_PCIE_SLOT1_GPIOS (PWRON or PCI)
- PP3V3_I2_PCIE_SLOT1_GPIOS

Signal aliases required by this page:
- I2_REV1_NOT

BOM options provided by this page:
- None

---

**PCI Clock Buffer**

- PCI_CLK33M_ZDB_IN
- PCI_CLK33M_ZDBOUT_R<0>
- PCI_CLK33M_ZDBOUT_R<1>
- PCI_CLK33M_ZDBOUT_R<2>
- PCI_CLK33M_ZDBOUT_R<3>

---

www.vinafix.vn
NOTE: All analog inputs to PMU should have TP_PMU_AN_Px_x signals. These pins are general-purpose spares.

NOTE: TP_PMU_Px_x signals are general-purpose spares (NONE) provided by this page.

Non-banger pins can be implemented as shown.

Non-banger pins are marked with.

NOTE: TP_PMU_AN_Px_x signals are general-purpose spares.

NOTE: TP_PMU_Px_x signals are general-purpose spares (NONE) provided by this page.

Non-banger pins can be implemented as shown.

Non-banger pins are marked with.

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NOTE: TP_PMU_Px_x signals are general-purpose spares (NONE) provided by this page.

Non-banger pins can be implemented as shown.

Non-banger pins are marked with.
**Fan Controller**

- **R3000**
- **C3000**
- **C3002**
- **C3003**

---

**Notes**

- **PLACE CLOSE TO CPU**
  - Q3001
  - Q3002

- **PLACE IN BETWEEN 3/5/1.5/2.5V PMR SUPPLY MAIN2**
  - Q3003

- **PLACE UNDERNEATH UPPER RAM ALTERNATE1**
  - Q3004

- **PLACE CLOSE TO BATTERY CHARGER/VCORE ALTERNATE2**
  - Q3005

---

**Electrical Constraints**

- **SPACING PHYSICAL DIFFERENTIALPAIR**
- **NO STUFF**
- **KEEP STUFFING RESISTORS CLOSE TO ADT7467 CONTROLLER**

---

**Placement**

- **PLACE UNDERNEATH UPPER RAM ALTERNATE1**
- **PLACE CLOSE TO BATTERY CHARGER/VCORE ALTERNATE2**
- **PLACE IN BETWEEN 3/5/1.5/2.5V PMR SUPPLY MAIN2**
- **PLACE CLOSE TO CPU**

---

**Notes on Component Placement**

- Components should be placed close to critical areas to ensure proper heat dissipation and signal integrity.

---

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**Revision Information**

- **REV.**
- **DRAWING NUMBER**
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---

**Device Connections**

- **VCCP**
- **TACH3**
- **THERM#/**
- **SMBALERT#/**
- **GPIO D1-**
- **D1+**
- **D2-**
- **D2+**
- **SCL**
- **VCC**
- **XTO**
- **TACH1**
- **SMBALERT#**
- **TACH2**
- **TACH4/**
- **PWM2/**
- **PWM1/**
- **GND**
- **SDA**
- **PWM3**
- **12345678**

---

**Schematic Labeling**

- **D**
- **SIZE**
- **OFSHT**
- **REV.**
- **APPLE COMPUTER INC.**
- **SCALE**
- **NONE**

---

**Fan Controller**

- **FAN CONTROLLER**
- **FAN1_TACH**
- **FAN2_TACH**
- **FAN2_PWM**
- **FAN1_PWM**

---

**Component Details**

- **R3000**
- **C3000**
- **C3002**
- **C3003**

---

**Fan Controller Details**

- **PP3V3_RUN_FAN**
- **PP5V_RUN_FAN**
- **ADT7467_ADR_ENABLE_L**
- **MIN_NECK_WIDTH=0.25 mm**
- **MIN_LINE_WIDTH=0.25 mm**
- **VOLTAGE=3.3V**

---

**Contact Information**

- **www.vinafix.vn**
CPU PLL POWER SUPPLY

AVDD = 0.59*(1+R4620/4621)

AVDD SUPPLY

SYNC_DATE=N/ASYNC_MASTER=N/A

VOLTAGE=1.22V

MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm

VOLTAGE=3.3V

MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm

www.vinafix.vn
Main Memory Series Termination

SERIES RESISTORS FOR CONTROL SIGNALS

PINS ARE SWAPPABLE FOR RPAKS RP4800-RP4804

SERIES RESISTORS FOR CLOCKS

SERIES RESISTORS FOR CS / CKE

Do not swap with other RPAKs

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SLOT "A"
LOWER SLOT
FACTORY SLOT

ADD ONE 0.1UF PER SLOT

RAM_VREF_A
RAM_VREF_B

ONE 0.1UF PER SLOT

ADB
NOTE: AGP 8x signals are not provided

BOM options provided by this page:
- =AGP_GPU_RESET_L - Active low reset for GPU
- =AGP_VREF - VRef divider output for

Signal aliases required by this page:
- =PP3V3_AGP

Power aliases required by this page:
- =PP1V5_AGP

R5700

=PP1V5_AGP

R5722

=PP3V3_AGP

Place C5731 at GPU
Place C5732 at NB
Place resistors midway between GPU and NB

Place C5731 at GPU
Place C5732 at NB
Place resistors midway between GPU and NB

Can also connect to NB if chips are co-located

0.1μF X5R 16V 10%

R5700

402 MF-LF 1/16W 5%

R5722

20K 402 MF-LF 1/16W 5%

R5725

47K 402 1/16W 5%

R5720

47K 402 1/16W 5%

R5721

47K 402 1/16W 5%

R5721

47K 402 1/16W 5%

R5721

47K 402 1/16W 5%

R5721

47K 402 1/16W 5%

R5721

47K 402 1/16W 5%

R5721

47K 402 1/16W 5%

R5721

47K 402 1/16W 5%

R5721

47K 402 1/16W 5%

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47K 402 1/16W 5%

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R5721

47K 402 1/16W 5%

R5721

47K 402 1/16W 5%

R5721

47K 402 1/16W 5%

R5721

47K 402 1/16W 5%

R5721

47K 402 1/16W 5%

R5721

47K 402 1/16W 5%
GPU VCORE SUPPLY

When VCORE_CNTL HIGH => 1.107V
0.107V = 0.6V + (1 + Rb/Ra) * (1.5V - 0.6V)

When VCORE_CNTL LOW => 1.054V
0.104V = 0.6V + (1 + Rb/Ra) * (1.5V - 0.6V)
Page Notes

BOM options provided by this page:

- DVO_1V5
- DVO_3V3
- GPU_VDDR4_3V3

Signal aliases required by this page:

- INV_ON_PWM
- 47
- R6680
- 1/16W
- 10K
- 402
- 2
- MF-LF
- 1/16W
- 10K
- 402
- 5%
- 53
- 2
- 402
- MF-LF
- 5%
- 1/16W
- 7
- GPU_DVOD_R<22>
- GPU_DVOD_R<18>
- GPU_DVOD_R<15>
- GPU_DVOD_R<9>
- GPU_DVOD_R<23>
- GPU_DVOD_R<20>
- GPU_DVOD_R<12>
- GPU_DVOD_R<2>
- GPU_DVOD_R<1>
- GPU_DVOD_R<5>
- CLKLVDS_L_P
- LVDS_U1_N
- LVDS_U1_P
- LVDS_L2_P
- LVDS_L0_N
- CLKLVDS_U_N
- CLKLVDS_U_P

www.vinafix.vn
Power aliases required by this page:
- I84
- I83
- I82
- I78
- I75
- I74
- I55
- I54

Upper Channel Series Termination

Upper Channel Common-mode Termination

Upper TMDS Transmitter
One resistor for each of:
- PCI_SLOTD_REQ_L
- PCI_SLOTA_REQ_L
- PCI_STOP_L
- PCI_FRAME_L

SLOT E REQ/GNT pull-ups
not provided by this page.
NOTE: This USB2 implementation supports PCI Devices implemented on this page:

- USB2_NEC

BOM options provided by this page:

- =PCI_USB2_INT_L
- =PCI_USB2_REQ_L
- =PP3V3_PCI_USB2 (D3cold rail)
- =PPVIO_PCI (to 3.3V or 5V)

Page Notes
NOTE: FireWire TPA/TPB pairs are NOT BOM options provided by this page:

- _GND_CHASSIS_FW_PORT2_
- _GND_CHASSIS_FW_PORT1_
- _PP3V3_FW_

NOTE: This page is expected to contain the BOM options listed above

- 0.1μF CERM 402 20%
- 21 1/16W 1%
- 21 MIN_LINE_WIDTH=0.25 mm
- 400-OHM-EMI

ESD Rail

3rd TPA/TPB pair unused

"Snapback" & "Late VG" Protection

Cable Power

PORT 1
BILINGUAL

PORT 2
1394A

FireWire Ports

Table of Frequency Property

- 3rd TPA/TPB pair unused (TPA-)
- 3rd TPA/TPB pair unused (TPA+)
- "Snapback" & "Late VG" Protection
- Cable Power

NOTE: Fast transient noise suppression (TPA) (to avoid ground offset issue)

BREF needs to be isolated from all local grounds per 1394b spec

When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

BREF should be hard-connected to logic ground for speed signaling and crosstalk detection currents per 1394b V1.33

有期徒刑
Place series terminators approximately halfway between Vesta and NB.
(They should probably be slightly closer to Vesta than the NB.).
USB2 data pairs is 90 ohms.

NOTE: Target differential impedance for

Secondary Length: 500 mils
Secondary Max Sep: 100 mils
Primary Max Sep: 7.5 mils
Length Tolerance: 50 mils
Line To Line: 19.5 mils

BOM options provided by this page:
- =RP92xxPy (pinswappable USB pulldowns)

Signal aliases required by this page:
=PP3V3_PWRON_USB

Power aliases required by this page:

---

Page Notes

Net Spacing Type: USB2

USB2_5 USB2 USB2
USB2_4 USB2 USB2
USB2_3 USB2 USB2
USB2_I2_P<2>
USB2_1 USB2 USB2
USB2_0 USB2 USB2

I2_CLK30M_USB2_XIN
I2_CLK30M_USB2_XOUT
XTAL XTAL_USB2_I2_XTAL
USB2_I2_N<5>
USB2_I2_P<5>
USB2_I2_N<4>
USB2_I2_P<4>
USB2_I2_N<3>
USB2_I2_P<3>
USB2_I2_N<2>
USB2_I2_P<2>
USB2_I2_N<1>
USB2_I2_P<1>
USB2_I2_N<0>
USB2_I2_P<0>

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Crystal load capacitance is 16pF

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Put crystal circuit close to I2

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www.vinafix.vn
USB2 data pairs is 90 ohms.

Net Spacing Type: USB2

Tie to GND at ball N11

VOLTAGE=0V
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Spacing & Physical Constraints 2

151 * = STAND 0.15 MM
= 50_OHM_SE

* = 100_OHM_DIFF

TV 151 * = 75_OHM_SE
= TV_CONN

DVO 0.15 MM
= STANDARD
= 50_OHM_SE

* = 100_OHM_DIFF

TMDS
= TMDS_CONN

* = 100_OHM_DIFF

LVDS
= 100_OHM_DIFF

= TMDS

= 100_OHM_DIFF

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