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- 1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
- 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
- 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

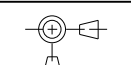
REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
03		384363	ENGINEERING RELEASED	06/03/05	?

STD MARIAS EVT

PDF	CSA	CONTENTS	SYNC MASTER	DATE
1	1	Table Of Contents	N/A	N/A
2	2	Board Information	N/A	N/A
3	3	System Block Diagram	N/A	N/A
4	4	Power Block Diagram	N/A	N/A
5	5	Revision History	N/A	N/A
6	6	Q16C Pin Swaps	N/A	N/A
7	7	Functional Test Points	N/A	N/A
8	8	I2C Connections	N/A	N/A
9	9	JTAG Connections	N/A	N/A
10	10	Power Synonyms	N/A	N/A
11	11	Signal Synonyms	N/A	N/A
12	12	Power Inputs	N/A	N/A
13	13	Battery Charger	N/A	N/A
14	14	12.8V PBUS/PMU Supplies	N/A	N/A
15	15	5V/3.3V Supplies	N/A	N/A
16	16	1.8V/1.5V Supplies	N/A	N/A
17	17	2.5V Supply	N/A	N/A
18	19	Vesta Power & Misc	N/A	N/A
19	21	I2 Power	N/A	N/A
20	22	I2 Power Supplies	N/A	N/A
21	23	I2 Supplemental	N/A	N/A
22	24	I2 Miscellaneous	N/A	N/A
23	25	PCI Clock Buffer	N/A	N/A
24	26	LEDs/Reset/Debug	N/A	N/A
25	27	Power Management Unit (PMU05)	N/A	N/A
26	29	Power Sequencing	N/A	N/A
27	30	Fan Controller	N/A	N/A
28	31	ALS Support	N/A	N/A
29	32	Sudden Motion Sensor	N/A	N/A
30	33	Q16C Internal I/O I	N/A	N/A
31	34	Q16C Internal I/O II	N/A	N/A
32	35	I2 Processor Interface	N/A	N/A
33	36	A8 MaxBus (CPU0)	MULLET	05/25/2005
34	37	A8 Configuration Straps	MULLET	05/25/2005
35	38	A8 Power (CPU0)	MULLET	05/25/2005
36	39	CPU VCore Supply	N/A	N/A
37	46	CPU AVDD Supply	N/A	N/A
38	47	I2 Memory Interface	N/A	N/A
39	48	Memory Series Termination	N/A	N/A
40	50	DDR2 SO-DIMM Slot A	N/A	N/A

PDF	CSA	CONTENTS	SYNC MASTER	DATE
41	52	DDR2 SO-DIMM Slot B	N/A	N/A
42	55	M11 Frame Buffer Constraints	N/A	N/A
43	56	I2 AGP Interface	N/A	N/A
44	57	GPU (M11) AGP Interface	N/A	N/A
45	58	GPU VCore Supply	N/A	N/A
46	59	GPU (M11) Core Power	N/A	N/A
47	60	GPU (M11) I/O Power	N/A	N/A
48	61	GPU (M11) Frame Buffer I/F	N/A	N/A
49	62	GPU Frame Buffer A	N/A	N/A
50	63	GPU Frame Buffer B	N/A	N/A
51	64	GPU (M11) GPIOs/Straps	N/A	N/A
52	65	GPU (M11) Clocks/Misc	N/A	N/A
53	66	GPU (M11) DVI/DAC Outputs	N/A	N/A
54	67	Lower TMDS Transmitter	N/A	N/A
55	68	Upper TMDS Transmitter	N/A	N/A
56	69	Internal Display Conns	N/A	N/A
57	70	External Display Conns	N/A	N/A
58	71	BootROM	N/A	N/A
59	72	I2 PCI Interface	N/A	N/A
60	73	Q85 Airport/BT Connector	N/A	N/A
61	74	Cardbus	N/A	N/A
62	75	NEC USB2	N/A	N/A
63	81	I2 UATA Interface	N/A	N/A
64	82	HDD/ODD Connectors	N/A	N/A
65	84	I2 Ethernet Interface	N/A	N/A
66	85	Vesta Ethernet PHY	N/A	N/A
67	86	Ethernet Connector	N/A	N/A
68	88	I2 FireWire Interface	N/A	N/A
69	89	Vesta FireWire PHY	N/A	N/A
70	90	FireWire Ports	N/A	N/A
71	91	FireWire Series Term	N/A	N/A
72	92	I2 USB Interface	N/A	N/A
73	93	NEC USB2 Interface	N/A	N/A
74	100	Audio Board Connector	N/A	N/A
75	110	Spacing & Physical Constraints	N/A	N/A
76	111	Spacing & Physical Constraints 2	N/A	N/A
77	112	Cross Reference Page		
78	113	Cross Reference Page		
79	114	Cross Reference Page		
80	115	Cross Reference Page		

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-6929	1	SCHEM,MARIAS-STD,Q16C	SCH1	
820-1875	1	PCBF,MARIAS,12L-STD,Q16C	PCB1	
826-4393	1	LBL,P/N LABEL,PCB,28MM x 6MM	[EEE:SYT]	Q16C_BTR_VRAM_S
826-4393	1	LBL,P/N LABEL,PCB,28MM x 6MM	[EEE:SYU]	Q16C_BST_VRAM_S
826-4393	1	LBL,P/N LABEL,PCB,28MM x 6MM	[EEE:TMJ]	Q16C_BTR_VRAM_H
826-4393	1	LBL,P/N LABEL,PCB,28MM x 6MM	[EEE:TMK]	Q16C_BST_VRAM_H

DIMENSIONS ARE IN MILLIMETERS		METRIC		Apple Computer Inc.	
XX :	_____	DRAPTER	/	DESIGN CK	/
X.XX :	_____	ENG APPD	/	MFG APPD	/
X.XXX :	_____	QA APPD	/	DESIGNER	/
ANGLES :	_____	RELEASE	/	SCALE	NONE
DO NOT SCALE DRAWING		MATERIAL/FINISH NOTED AS APPLICABLE		SIZE	D
 THIRD ANGLE PROJECTION		DRAWING NUMBER		051-6929	REV. 03
SHT 1 OF 115					

Design-Specific Rules

TABLE_SPACING_RULE	STANDARD	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT
TABLE_SPACING_RULE	STANDARD	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT
TABLE_SPACING_RULE	BGA_P1MM	10	0.10 MM	1.25 MM	0.1 MM	12.5 MM
TABLE_SPACING_RULE	BGA_P2MM	20	0.20 MM	1.25 MM	0.1 MM	12.5 MM
TABLE_SPACING_RULE	DEFAULT	*	0.1 MM	2.5 MM	0.15 MM	10.0 MM

"1MM" area defined around BGAs to reduce DRCs caused by fan-out.
 "BGA_P2MM" rule ensures these critical signals do not fan-out routed next to any other signals.

TABLE_PHYSICAL_RULE	STANDARD	DEFAULT	DEFAULT	DEFAULT	DEFAULT
TABLE_PHYSICAL_RULE	STANDARD	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT
TABLE_PHYSICAL_RULE	DEFAULT	*	Y	0.100 MM	0.100 mm

Layer-specific rules for 90-ohm differential impedance

TABLE_SPACING_RULE	90_OHM_DIFF	TOP,BOTTOM	2.5 MM	0.200 MM	2.5 MM	1.0 MM
TABLE_SPACING_RULE	90_OHM_DIFF	*	2.5 MM	0.200 MM	2.5 MM	1.0 MM

Layer-specific rules for 100-ohm differential impedance

TABLE_SPACING_RULE	100_OHM_DIFF	TOP,BOTTOM	2.5 MM	0.200 MM	2.5 MM	1.0 MM
TABLE_SPACING_RULE	100_OHM_DIFF	*	2.5 MM	0.200 MM	2.5 MM	1.0 MM

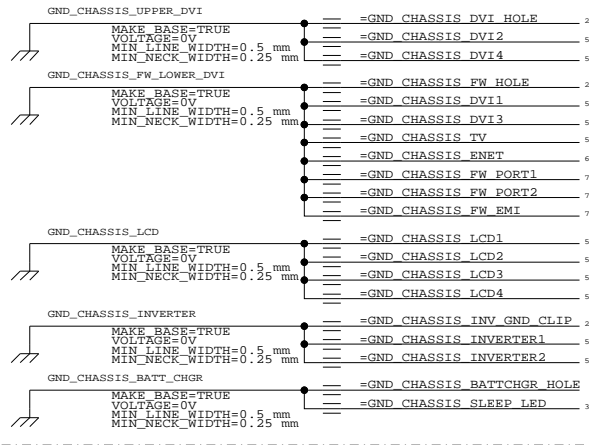
Layer-specific rules for 110-ohm differential impedance

TABLE_SPACING_RULE	110_OHM_DIFF	TOP,BOTTOM	2.5 MM	0.330 MM	2.5 MM	1.0 MM
TABLE_SPACING_RULE	110_OHM_DIFF	*	2.5 MM	0.330 MM	2.5 MM	1.0 MM

Portable-specific Override Rules

TABLE_SPACING_RULE	AGP	201	*	0.2 MM			
TABLE_SPACING_RULE	AGP	201	*	0.2 MM			
TABLE_SPACING_RULE	AGP_STB	251	*	0.25 MM			
TABLE_SPACING_RULE	VGA	151	*	0.15 MM	=DEFAULT	=DEFAULT	=DEFAULT
TABLE_SPACING_RULE	TV	151	*	0.15 MM	=DEFAULT	=DEFAULT	=DEFAULT

CHASSIS GND CONNECTIONS



Layer-specific rules for 60-ohm single-ended impedance

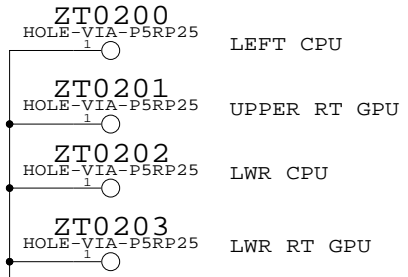
TABLE_PHYSICAL_RULE	60_OHM_SE	*	Y	0.076 MM	=50_OHM_SE	=50_OHM_SE
TABLE_PHYSICAL_RULE	60_OHM_SE	*	Y	0.076 MM	=50_OHM_SE	=50_OHM_SE

Layer-specific rules for 50-ohm single-ended impedance

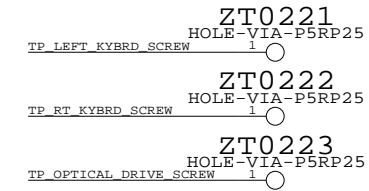
TABLE_SPACING_RULE	50_OHM_SE	*	2.5 MM	0.125 MM	2.5 MM	1.0 MM
TABLE_SPACING_RULE	50_OHM_SE	*	2.5 MM	0.125 MM	2.5 MM	1.0 MM

BOARD HOLES

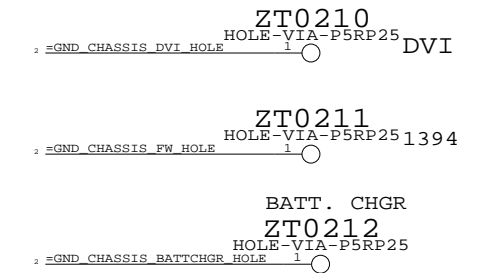
HEATSINK MOUNTS



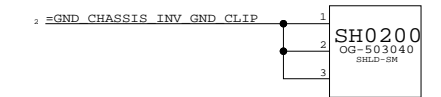
MECH. HOLES



CHASSIS MOUNTS



INVERTER



BOARD STACK-UP AND CONSTRUCTION

SEE BOARD FILE FOR DETAILED INFORMATION
 CONVENTIONAL CONSTRUCTION WITH Pxx TH VIA

Layer	Material	Thickness
1	SIGNAL (1/2 OZ + COPPER PLATING)	
2	PREPREG	
3	CORE	
4	PREPREG	
5	CORE	
6	PREPREG	
7	CORE	
8	PREPREG	
9	CORE	
10	PREPREG	
11	CORE	
12	PREPREG	
13	SIGNAL (1/2 OZ + COPPER PLATING)	

NO_TEST Properties

1778 ITH RC	45	NO_TEST=TRUE	TP VESTA DNC E9	18	NO_TEST=TRUE
1778 VRNG	45	NO_TEST=TRUE	TP VESTA F1000	66	NO_TEST=TRUE
GPU DVOD R<18>	6 53	NO_TEST=TRUE	TP VESTA PHYA<0>	66	NO_TEST=TRUE
LTC3412 RUNSS	17	NO_TEST=TRUE	TP VESTA REGSEN2	18	NO_TEST=TRUE
TMDS_CONN_CLKP	57	NO_TEST=TRUE	TP VESTA SPD0	66	NO_TEST=TRUE
TP NEC_SMC	62	NO_TEST=TRUE	USB_NEC_BT_N	6 31	NO_TEST=TRUE
TP NEC_SMI_L	62	NO_TEST=TRUE	USB_NEC_N<1>	73	NO_TEST=TRUE
TP NEC_SRCLK	62	NO_TEST=TRUE	USB_NEC_N<2>	73	NO_TEST=TRUE
TP USB2_PWREN<0>	73	NO_TEST=TRUE	USB_NEC_N<3>	73	NO_TEST=TRUE
TP USB2_PWREN<2>	73	NO_TEST=TRUE	USB_NEC_P<0>	73	NO_TEST=TRUE
TP USB2_PWREN<3>	73	NO_TEST=TRUE	USB_NEC_P<1>	73	NO_TEST=TRUE
UATA_DD_R<0>	6 43	NO_TEST=TRUE	SI_TMDS_DN<5>	55	NO_TEST=TRUE
UATA_DD_R<8>	6 43	NO_TEST=TRUE	SI_TMDS_DN<4>	55	NO_TEST=TRUE
UATA_DD_R<10>	6 43	NO_TEST=TRUE	SI_TMDS_DP<3>	55	NO_TEST=TRUE
UATA_DA_R<0>	6 43	NO_TEST=TRUE	SI_TMDS_DN<2>	54	NO_TEST=TRUE
UATA_DA_R<1>	6 43	NO_TEST=TRUE	SI_TMDS_DN<1>	54	NO_TEST=TRUE
			SI_TMDS_DN<0>	54	NO_TEST=TRUE
			SI_TMDS_CLKP	54	NO_TEST=TRUE

BOM OPTIONS

BOM NUMBER	BOM NAME	BOM OPTIONS
630-7015	PCBA, MLB, BETTERMHZ, MARIAS, VRAM_S, Q16C	COMMON, ALTERNATE, gQ16C, gQ16C_BTR, Q16C_BTR_VRAM_S, VRAM_SAMSUNG, gCommon
630-7016	PCBA, MLB, BESTMHZ, MARIAS, VRAM_S, Q16C	COMMON, ALTERNATE, gQ16C, gQ16C_BST, Q16C_BST_VRAM_S, VRAM_SAMSUNG, gCommon
630-7184	PCBA, MLB, BETTERMHZ, MARIAS, VRAM_H, Q16C	COMMON, ALTERNATE, gQ16C, gQ16C_BTR, Q16C_BTR_VRAM_H, VRAM_HYNIX, gCommon
630-7185	PCBA, MLB, BESTMHZ, MARIAS, VRAM_H, Q16C	COMMON, ALTERNATE, gQ16C, gQ16C_BST, Q16C_BST_VRAM_H, VRAM_HYNIX, gCommon

BOM GROUP	BOM OPTIONS
gCommon	5V_HD_LOGIC, BACKUP_BATT, CPU_A7PM, I2_FW_BETA, I2_MAXBUS_50OHM, MAXBUS_1V8, gCommon1
gCommon1	MMM_ACCEL_KIONIX, GPU_PWRPLAY, GPU_SS, GPU_LVDDR_2V8, GPU_MEMIO_1V8, gCommon2
gCommon2	I2_REV1_NOT, I2_MAXBUS_FBCLK_MATCHED, I2_AGP_FBCLK_MATCHED, I2_PCI_FBCLK_MATCHED, gCommon3
gCommon3	CPU_VCORE_3STATES, I2_MAXBUS_166MHZ, I2VCORE_1V5, I2VCORE_BURST, gCommon4
gCommon4	VESTA_PORT2_DISABLE, DVO_1V8, TMDS_DUAL, VCORE_OFFSET, VCORE_OFFSET_SW, gUSB
gUSB	USB2_NEC, USB1P1_I2
gQ16C	Q16C_PARTS, BOOTROM_PROG, PMU_PROG, DEVELOPMENT, MAXBUS_TBEN_SYNC
gQ16C_BTR	A7PM_1P5_LGA, CPU0_BUSRATIO_9.0X
gQ16C_BST	A7PM_1P67_LGA, CPU0_BUSRATIO_10.0X

Module Components

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
343S0325	1	IC, ASIC, I2, REV1.1, NB/SB, 974 BGA	U2100	CRITICAL	
337S3135	1	IC, PMU05, BLANK, QFP	U2700	CRITICAL	PMU_BLANK
341S1772	1	IC, PMU05, V1, QFP	U2700	CRITICAL	PMU_PROG
337S3162	1	IC, A7PM, R1.5, 1.67GHZ, LGA, 1.28V, 23W, 85C	U3600	CRITICAL	A7PM_1P67_LGA
337S3163	1	IC, A7PM, R1.5, 1.5GHZ, LGA, 1.28V, 23W, 85C	U3600	CRITICAL	A7PM_1P5_LGA
337S3077	1	IC, A8, xxxGHZ	U3600	CRITICAL	CPU_A8
338S0252	1	IC, GPU, M11P	U5700	CRITICAL	
335S0088	1	BOOTROM, BLANK	U7100	CRITICAL	BOOTROM_BLANK
341S1736	1	IC, BOOTROM, B, Q16C	U7100	CRITICAL	BOOTROM_PROG
343S0356	1	IC, ASIC, VESTA, V1.3, LF	U8500	CRITICAL	
333S0317	4	IC, GDDR SDRAM, 2MX32X4, 300MHZ, LF FBGA144	U6200, U6250, U6300, U6350	CRITICAL	VRAM_SAMSUNG
333S0314	4	IC, GDDR SDRAM, 2MX32X4, 300MHZ, LF FBGA144	U6200, U6250, U6300, U6350	CRITICAL	VRAM_HYNIX

Board Information

SYNC_MASTER=N/A SYNC_DATE=N/A

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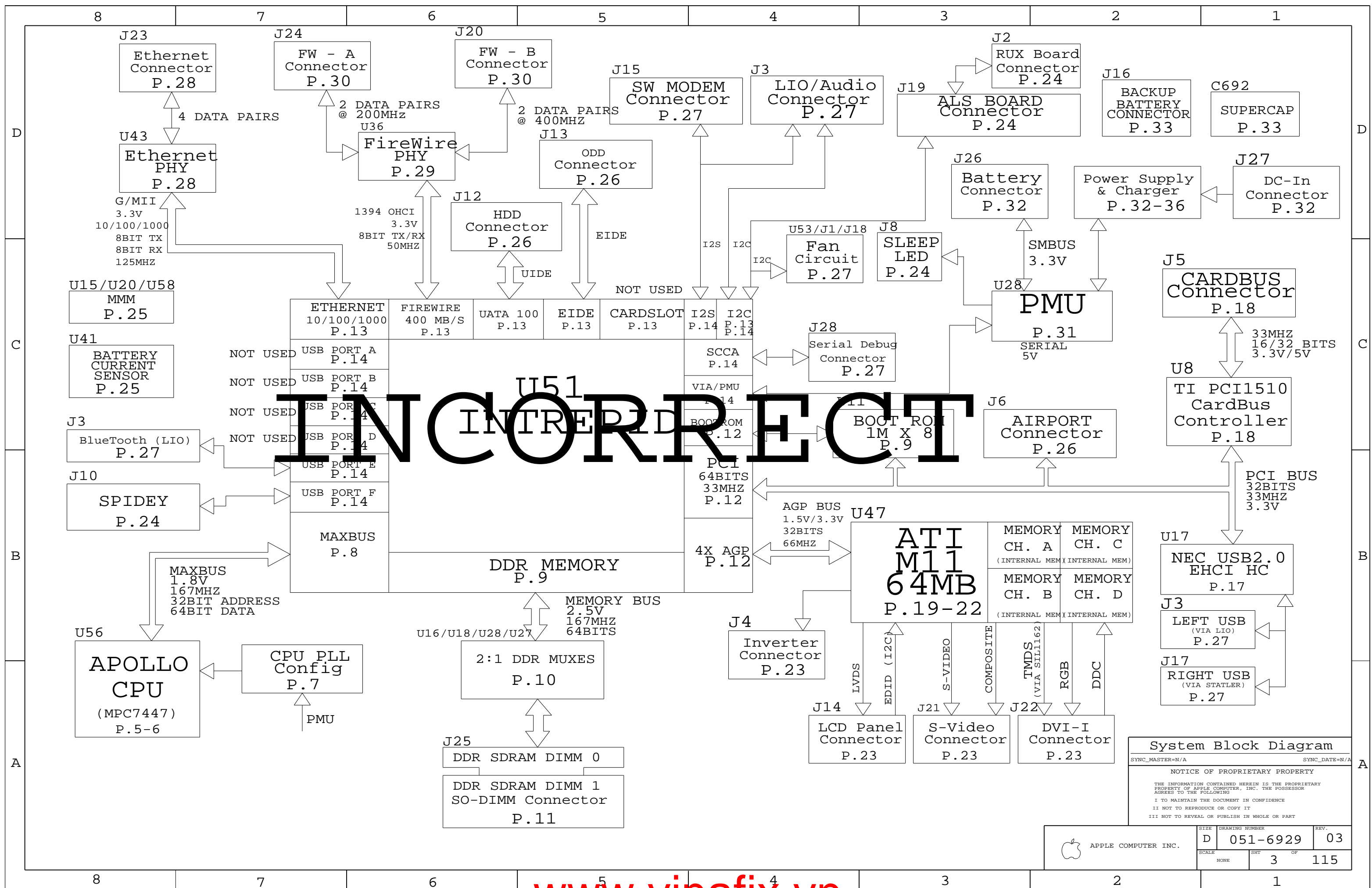
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INCORRECT

System Block Diagram

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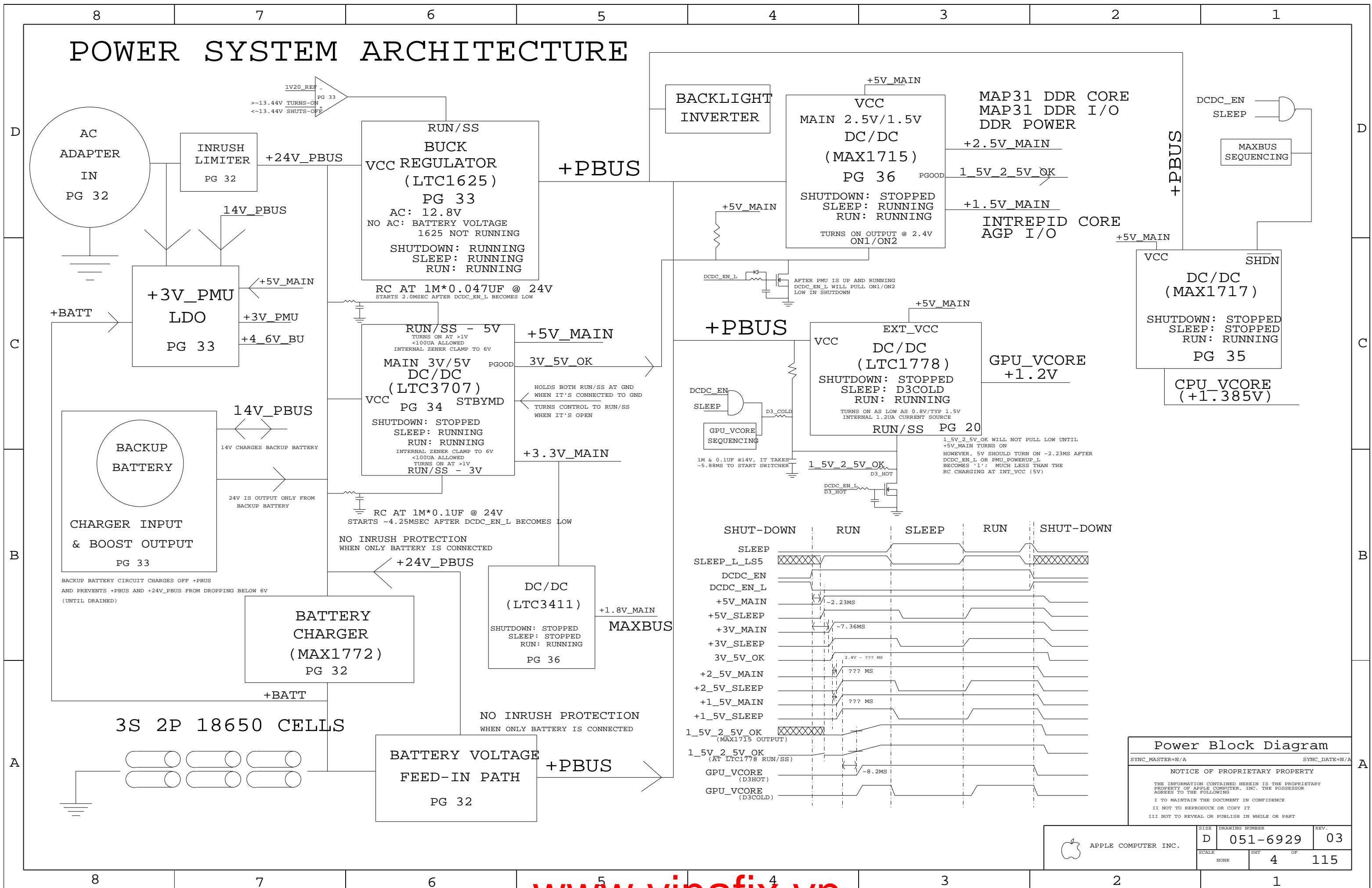
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POWER SYSTEM ARCHITECTURE



Power Block Diagram
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NONE	4		115

REVISION HISTORY

PRE-EVT

- 04/04/2005 - Beginning revision history
- 04/06/2005 - Made DDR2 and FB pin swaps as requested by CM
- 04/06/2005 - Modem connector moved to non-shared page
- 04/06/2005 - Chassis grounds partitioned as previous products
- 04/06/2005 - CPU Vcc select line hooked to I2 GP101
- 04/11/2005 - Made additional FB pin swaps
- 04/11/2005 - Changed DDR2 CS/CKE RPAKs to RPAK2P (added RP4871, RP4876)
- 04/11/2005 - Implemented more DDR2 pin swaps
- 04/11/2005 - Implemented FireWire pin swaps
- 04/11/2005 - Added remaining spacing and physical rule tables
- 04/12/2005 - Added upper LVDS channel to function/test pages
- 04/12/2005 - Changed battery sense resistor to 0.016 ohm (R1250)
- 04/12/2005 - Stuffed R2303 to disable FW port power when off on AC
- 04/12/2005 - Changed audio caps to XSR (CA035, CA050, CA051)
- 04/12/2005 - Corrected MIN LINE WIDTH properties on FP3V3_PWRON
- 04/12/2005 - Corrected TMS DIFFERENTIAL PAIR properties at DVI connector
- 04/12/2005 - Reduced MIN NECK WIDTH property on GND to 0.2 mm for TMS parts
- 04/12/2005 - Corrected line and neck width properties
- 04/12/2005 - Added high/low swing BOMOPTIONS for DVO on SI TMS parts
- 04/13/2005 - Added 1.5V DVO option to GPU
- 04/13/2005 - Removed series R isolating VG from digital ground on FW ports (per design guide)
- 04/14/2005 - Changed GPU to M11
- 04/15/2005 - Moved FB series R to page 61
- 04/18/2005 - Updated straps, VREF inputs and decoupling on GPU
- 04/18/2005 - Corrected system problems on PMU port usage
- 04/19/2005 - Added NO_RST properties to buses between JTAG enabled devices
- 04/20/2005 - Corrected ENER power rail
- 04/20/2005 - Fixed ENER LPWR and VESTA RESET circuits per Vesta design guide
- 04/20/2005 - Changed R5880 to 6.34k to take GPU Vcore to 1.3v/1.05v
- 04/21/2005 - Added page 6 and modified pages 11, 35, 81 for design specific pin swaps
- 04/22/2005 - Corrected STOP_AGP_L net name (hooked to I2 now) and removed redundant pullup
- 04/22/2005 - Added external pullups to replace missing internal I2 pullups
- 04/22/2005 - Added ADC caps at PMU
- 04/22/2005 - Corrected load capacitance for Vesta FireWire crystal (to 18pF)
- 04/22/2005 - Disconnected FW_POWERDOWN from Vesta LPWR_1394 pin
- 04/22/2005 - Corrected pull-down resistor value for 0.006 ohm battery current sense
- 04/22/2005 - Changed CPU Vcore caps to 330 uF caps
- 05/03/2005 - Changed GPU FB MYREFs into separate dividers
- 05/03/2005 - Flipped USTA I/F, DVO I/F, USB pull-downs
- 05/04/2005 - Added extra cap at input to I2 USBVDD
- 05/05/2005 - Added pull-downs to unused serial debug signals (DTR/RTS)
- 05/05/2005 - Added pull-down to Vesta LPWR_1394
- 05/05/2005 - Added PDAG signal between HDD and ODD connectors
- 05/10/2005 - Various Pb-free component replacements
- 05/13/2005 - Various Pb-free component replacements
- 05/13/2005 - Pin-swaps for I2 RPAKs to match up with Q41C style layout
- 05/16/2005 - Various Pb-free component replacements
- 05/16/2005 - Added DYNX VRAM option and PCBAs
- 05/19/2005 - Various Pb-free component replacements
- 05/19/2005 - Added FBEN sync circuit
- 05/20/2005 - Various Pb-free component replacements
- 05/20/2005 - Added DASP signal between HDD and ODD connectors
- 05/21/2005 - Corrected AGP_INT_L connection between I2 and GPU
- 05/21/2005 - Corrected VGA sync connections at GPU
- 05/23/2005 - Release as REV 01 for Pre-EVT/EVT
- 05/24/2005 - Added HGT USB2 controller
- 05/25/2005 - Added ZDB clock buffer for PCI clocks
- 05/26/2005 - Various Pb-free component replacements
- 05/31/2005 - Removed SMC I2C microcontroller
- 05/31/2005 - Added 2.0 uF caps to GPU Vcore regulator output
- 05/31/2005 - Corrected USB diff pair and spacing/physical rules on port connections
- 06/01/2005 - Corrected FireWire VP caps to 50V
- 06/01/2005 - Various Pb-free component replacements

03

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	SCALE	SHT OF	
	NONE	5 OF	115

	8	7	6	5	4	3	2	1														
D	<h3>I2S Series Rs</h3> <pre> MAKE_BASE=TRUE 22 I2S0_SB_TO_DEV.DTO.R == =RP1150P1 11 11 =RP1150P8 == I2S0_SB_TO_DEV.DTO 7 74 MAKE_BASE=TRUE MAKE_BASE=TRUE 22 I2S0_BITCLK.R == =RP1150P2 11 11 =RP1150P7 == I2S0_BITCLK 7 74 MAKE_BASE=TRUE MAKE_BASE=TRUE 22 I2S0_MCLK.R == =RP1150P3 11 11 =RP1150P6 == I2S0_MCLK 7 74 MAKE_BASE=TRUE MAKE_BASE=TRUE 22 I2S0_SYNC.R == =RP1150P4 11 11 =RP1150P5 == I2S0_SYNC 7 74 MAKE_BASE=TRUE MAKE_BASE=TRUE 22 I2S1_SB_TO_DEV.DTO.R == =RP1151P1 11 11 =RP1151P8 == I2S1_SB_TO_DEV.DTO 30 MAKE_BASE=TRUE MAKE_BASE=TRUE 22 I2S1_SYNC.R == =RP1151P2 11 11 =RP1151P7 == I2S1_SYNC 30 MAKE_BASE=TRUE MAKE_BASE=TRUE 22 I2S1_MCLK.R == =RP1151P3 11 11 =RP1151P6 == I2S1_MCLK 30 MAKE_BASE=TRUE MAKE_BASE=TRUE 22 I2S1_BITCLK.R == =RP1151P4 11 11 =RP1151P5 == I2S1_BITCLK 30 MAKE_BASE=TRUE </pre>				<h3>Lower DVO Series Rs</h3> <pre> MAKE_BASE=TRUE 53 GPU_DVOD_R<16> == =RP6720P1 54 54 =RP6720P8 == GPU_DVOD<16> 55 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<4> == =RP6720P2 54 54 =RP6720P7 == GPU_DVOD<4> 54 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<7> == =RP6720P3 54 54 =RP6720P6 == GPU_DVOD<7> 54 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<6> == =RP6720P4 54 54 =RP6720P5 == GPU_DVOD<6> 54 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<11> == =RP6721P1 54 54 =RP6721P8 == GPU_DVOD<11> 54 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<9> == =RP6721P2 54 54 =RP6721P7 == GPU_DVOD<9> 54 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<10> == =RP6721P3 54 54 =RP6721P6 == GPU_DVOD<10> 54 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVO_HSYNC.R == =RP6721P4 54 54 =RP6721P5 == GPU_DVO_HSYNC 54 55 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<3> == =RP6722P1 54 54 =RP6722P8 == GPU_DVOD<3> 54 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<5> == =RP6722P2 54 54 =RP6722P7 == GPU_DVOD<5> 54 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<13> == =RP6722P3 54 54 =RP6722P6 == GPU_DVOD<13> 55 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<12> == =RP6722P4 54 54 =RP6722P5 == GPU_DVOD<12> 55 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<2> == =RP6723P1 54 54 =RP6723P8 == GPU_DVOD<2> 54 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<1> == =RP6723P2 54 54 =RP6723P7 == GPU_DVOD<1> 54 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<0> == =RP6723P3 54 54 =RP6723P6 == GPU_DVOD<0> 54 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<14> == =RP6723P4 54 54 =RP6723P5 == GPU_DVOD<14> 55 MAKE_BASE=TRUE </pre>				D													
C	<h3>UATA Series Rs</h3> <pre> MAKE_BASE=TRUE 63 UATA_DD_R<12> == =RP8150P1 63 63 =RP8150P8 == UATA_DD<12> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_CS0.L.R == =RP8150P2 63 63 =RP8150P7 == UATA_CS0.L 7 63 64 MAKE_BASE=TRUE (IDE_CS1FX.L) MAKE_BASE=TRUE 63 UATA_DD_R<14> == =RP8150P3 63 63 =RP8150P6 == UATA_DD<14> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DD_R<11> == =RP8150P4 63 63 =RP8150P5 == UATA_DD<11> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DD_R<7> == =RP8151P1 63 63 =RP8151P8 == UATA_DD<7> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DD_R<2> == =RP8151P2 63 63 =RP8151P7 == UATA_DD<2> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DD_R<3> == =RP8151P3 63 63 =RP8151P6 == UATA_DD<3> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DD_R<15> == =RP8151P4 63 63 =RP8151P5 == UATA_DD<15> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DD_R<9> == =RP8152P1 63 63 =RP8152P8 == UATA_DD<9> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DD_R<4> == =RP8152P2 63 63 =RP8152P7 == UATA_DD<4> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DD_R<6> == =RP8152P3 63 63 =RP8152P6 == UATA_DD<6> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DD_R<5> == =RP8152P4 63 63 =RP8152P5 == UATA_DD<5> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DA_R<2> == =RP8153P1 63 63 =RP8153P8 == UATA_DA<2> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DD_R<8> == =RP8153P2 63 63 =RP8153P7 == UATA_DD<8> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DD_R<10> == =RP8153P3 63 63 =RP8153P6 == UATA_DD<10> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DA_R<0> == =RP8153P4 63 63 =RP8153P5 == UATA_DA<0> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DD_R<13> == =RP8154P1 63 63 =RP8154P8 == UATA_DD<13> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DD_R<0> == =RP8154P2 63 63 =RP8154P7 == UATA_DD<0> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DD_R<1> == =RP8154P3 63 63 =RP8154P6 == UATA_DD<1> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DA_R<1> == =RP8154P4 63 63 =RP8154P5 == UATA_DA<1> 7 63 64 MAKE_BASE=TRUE </pre>				<h3>Upper DVO Series Rs</h3> <pre> MAKE_BASE=TRUE 53 GPU_DVO_DE.R == =RP6821P1 55 55 =RP6821P8 == GPU_DVO_DE 54 55 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVO_VSYNC.R == =RP6821P2 55 55 =RP6821P7 == GPU_DVO_VSYNC 54 55 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVO_CLKP.R == =RP6821P3 55 55 =RP6821P6 == GPU_DVO_CLKP 54 55 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<8> == =RP6821P4 55 55 =RP6821P5 == GPU_DVOD<8> 54 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<21> == =RP6822P1 55 55 =RP6822P8 == GPU_DVOD<21> 55 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<19> == =RP6822P2 55 55 =RP6822P7 == GPU_DVOD<19> 55 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<17> == =RP6822P3 55 55 =RP6822P6 == GPU_DVOD<17> 55 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<15> == =RP6822P4 55 55 =RP6822P5 == GPU_DVOD<15> 55 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<20> == =RP6823P1 55 55 =RP6823P8 == GPU_DVOD<20> 55 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<22> == =RP6823P2 55 55 =RP6823P7 == GPU_DVOD<22> 55 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<23> == =RP6823P3 55 55 =RP6823P6 == GPU_DVOD<23> 55 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<18> == =RP6823P4 55 55 =RP6823P5 == GPU_DVOD<18> 55 MAKE_BASE=TRUE </pre>				C													
B	<h3>MAXBUS Pullups</h3> <pre> MAKE_BASE=TRUE 33 MAXBUS_TS.L == =RP3510P1 32 MAKE_BASE=TRUE MAKE_BASE=TRUE 32 MAXBUS_CPU1_BG.L == =RP3510P2 32 MAKE_BASE=TRUE MAKE_BASE=TRUE 31 MAXBUS_CPU0_DBG.L == =RP3510P3 32 MAKE_BASE=TRUE MAKE_BASE=TRUE 32 MAXBUS_TBN.I2 == =RP3510P4 32 MAKE_BASE=TRUE MAKE_BASE=TRUE 33 MAXBUS_CPU0_BG.L == =RP3511P1 32 MAKE_BASE=TRUE MAKE_BASE=TRUE 32 MAXBUS_CPU1_HIT.L == =RP3511P2 32 MAKE_BASE=TRUE MAKE_BASE=TRUE 33 MAXBUS_CPU0_HIT.L == =RP3511P3 32 MAKE_BASE=TRUE MAKE_BASE=TRUE 33 MAXBUS_CPU0_BR.L == =RP3511P4 32 MAKE_BASE=TRUE MAKE_BASE=TRUE 32 MAXBUS_CPU1_BR.L == =RP3512P1 32 MAKE_BASE=TRUE MAKE_BASE=TRUE 33 MAXBUS_TA.L == =RP3512P2 32 MAKE_BASE=TRUE MAKE_BASE=TRUE 34 MAXBUS_CPU0_INT.L == =RP3512P3 32 MAKE_BASE=TRUE MAKE_BASE=TRUE 32 MAXBUS_CPU1_INT.L == =RP3512P4 32 MAKE_BASE=TRUE MAKE_BASE=TRUE 33 MAXBUS_CPU0_DRDY.L == =RP3513P2 32 MAKE_BASE=TRUE MAKE_BASE=TRUE 32 MAXBUS_CPU1_DRDY.L == =RP3513P3 32 MAKE_BASE=TRUE MAKE_BASE=TRUE 33 MAXBUS_AACK.L == =RP3513P4 32 MAKE_BASE=TRUE MAKE_BASE=TRUE 33 MAXBUS_ARTRY.L == =RP3514P1 32 MAKE_BASE=TRUE MAKE_BASE=TRUE 32 MAXBUS_CPU1_DBG.L == =RP3514P2 32 MAKE_BASE=TRUE MAKE_BASE=TRUE 33 MAXBUS_TEA.L == =RP3514P3 32 MAKE_BASE=TRUE </pre>		<h3>AGP Pullups</h3> <pre> MAKE_BASE=TRUE 44 AGP_TRDY.L == =RP5610P1 43 MAKE_BASE=TRUE MAKE_BASE=TRUE 44 AGP_IRDY.L == =RP5610P2 43 MAKE_BASE=TRUE MAKE_BASE=TRUE 44 AGP_REQ.L == =RP5610P3 43 MAKE_BASE=TRUE MAKE_BASE=TRUE 44 AGP_RBF.L == =RP5610P4 43 MAKE_BASE=TRUE MAKE_BASE=TRUE 44 AGP_FRAME.L == =RP5611P1 43 MAKE_BASE=TRUE MAKE_BASE=TRUE 44 AGP_DEVSEL.L == =RP5611P2 43 MAKE_BASE=TRUE MAKE_BASE=TRUE 44 AGP_STOP.L == =RP5611P3 43 MAKE_BASE=TRUE MAKE_BASE=TRUE 44 AGP_GNT.L == =RP5611P4 43 MAKE_BASE=TRUE MAKE_BASE=TRUE 11 PCI_AIRPORT_GNT.L == =RP7250P1 59 MAKE_BASE=TRUE MAKE_BASE=TRUE 60 61 PCI_TRDY.L == =RP7250P2 59 MAKE_BASE=TRUE MAKE_BASE=TRUE 60 61 PCI_IRDY.L == =RP7250P3 59 MAKE_BASE=TRUE MAKE_BASE=TRUE 60 61 PCI_STOP.L == =RP7250P4 59 MAKE_BASE=TRUE MAKE_BASE=TRUE 11 PCI_CBUS_REQ.L == =RP7251P1 59 MAKE_BASE=TRUE MAKE_BASE=TRUE 11 PCI_AIRPORT_REQ.L == =RP7251P2 59 MAKE_BASE=TRUE MAKE_BASE=TRUE 11 PCI_CBUS_GNT.L == =RP7251P3 59 MAKE_BASE=TRUE MAKE_BASE=TRUE 60 61 PCI_FRAME.L == =RP7251P4 59 MAKE_BASE=TRUE </pre>		<h3>USB Pulldowns</h3> <pre> 72 =RP9210P8 == USB_I2_BT.P 11 MAKE_BASE=TRUE 72 =RP9210P7 == USB_I2_BT.N 11 MAKE_BASE=TRUE 72 =RP9210P6 == USB2_I2_RIGHT_PORT.N 11 MAKE_BASE=TRUE 72 =RP9210P5 == USB2_I2_RIGHT_PORT.P 11 MAKE_BASE=TRUE 72 =RP9211P8 == USB2_I2_P<1> 72 MAKE_BASE=TRUE 72 =RP9211P7 == USB2_I2_N<1> 72 MAKE_BASE=TRUE 72 =RP9211P6 == USB2_I2_N<3> 72 MAKE_BASE=TRUE 72 =RP9211P5 == USB2_I2_P<3> 72 MAKE_BASE=TRUE 72 =RP9212P8 == USB_I2_TPAD.N 11 MAKE_BASE=TRUE 72 =RP9212P7 == USB_I2_TPAD.P 11 MAKE_BASE=TRUE 72 =RP9212P6 == USB2_I2_LEFT_PORT.P 11 MAKE_BASE=TRUE 72 =RP9212P5 == USB2_I2_LEFT_PORT.N 11 MAKE_BASE=TRUE 71 =RP9300P8 == USB2_NEC_LEFT_PORT.P 11 MAKE_BASE=TRUE 71 =RP9300P7 == USB2_NEC_LEFT_PORT.N 11 MAKE_BASE=TRUE 71 =RP9300P6 == USB2_NEC_RIGHT_PORT.N 11 MAKE_BASE=TRUE 71 =RP9300P5 == USB2_NEC_RIGHT_PORT.P 11 MAKE_BASE=TRUE 71 =RP9301P8 == USB_NEC_BT.P 11 MAKE_BASE=TRUE 71 =RP9301P7 == USB_NEC_BT.N 2 11 MAKE_BASE=TRUE 71 =RP9301P6 == USB_NEC_TPAD.N 11 MAKE_BASE=TRUE 71 =RP9301P5 == USB_NEC_TPAD.P 11 MAKE_BASE=TRUE </pre>		B															
A	<h3>FW Series Rs</h3> <pre> MAKE_BASE=TRUE 68 FW_D_R<7> == =RP9100P1 71 71 =RP9100P8 == FW_D<7> 9 69 MAKE_BASE=TRUE MAKE_BASE=TRUE 68 FW_D_R<3> == =RP9100P2 71 71 =RP9100P7 == FW_D<3> 9 69 MAKE_BASE=TRUE MAKE_BASE=TRUE 68 FW_D_R<4> == =RP9100P3 71 71 =RP9100P6 == FW_D<4> 9 69 MAKE_BASE=TRUE MAKE_BASE=TRUE 68 FW_D_R<2> == =RP9100P4 71 71 =RP9100P5 == FW_D<2> 9 69 MAKE_BASE=TRUE MAKE_BASE=TRUE 68 FW_D_R<0> == =RP9101P1 71 71 =RP9101P8 == FW_D<0> 9 69 MAKE_BASE=TRUE MAKE_BASE=TRUE 68 FW_D_R<6> == =RP9101P2 71 71 =RP9101P7 == FW_D<6> 9 69 MAKE_BASE=TRUE MAKE_BASE=TRUE 68 FW_D_R<1> == =RP9101P3 71 71 =RP9101P6 == FW_D<1> 9 69 MAKE_BASE=TRUE MAKE_BASE=TRUE 68 FW_D_R<5> == =RP9101P4 71 71 =RP9101P5 == FW_D<5> 9 69 MAKE_BASE=TRUE </pre>				A																	
<div style="text-align: center;"> <h2>Q16C Pin Swaps</h2> <p>SYNC_MASTER=N/A SYNC_DATE=N/A</p> <p>NOTICE OF PROPRIETARY PROPERTY</p> <p>THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING</p> <p>I TO MAINTAIN THE DOCUMENT IN CONFIDENCE</p> <p>II NOT TO REPRODUCE OR COPY IT</p> <p>III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART</p> </div>																						
<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td rowspan="2" style="text-align: center; vertical-align: middle;"> APPLE COMPUTER INC. </td> <td style="text-align: center;">SIZE</td> <td style="text-align: center;">DRAWING NUMBER</td> <td style="text-align: center;">REV.</td> </tr> <tr> <td style="text-align: center;">D</td> <td style="text-align: center;">051-6929</td> <td style="text-align: center;">03</td> </tr> <tr> <td style="text-align: center;">SCALE</td> <td style="text-align: center;">SHEET</td> <td style="text-align: center;">OF</td> <td style="text-align: center;">TOTAL</td> </tr> <tr> <td style="text-align: center;">NONE</td> <td style="text-align: center;">6</td> <td style="text-align: center;">115</td> <td></td> </tr> </table>								APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.	D	051-6929	03	SCALE	SHEET	OF	TOTAL	NONE	6	115	
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.																			
	D	051-6929	03																			
SCALE	SHEET	OF	TOTAL																			
NONE	6	115																				
	8	7	6	5	4	3	2	1														

Enhanced MAC-1 Test Coverage

Functional test points use a P6 pad placed on bottom side.

Category	Test Point	Pin	FUNC_TEST=	Notes
POWER	PP24V_ADAPTER	10	FUNC_TEST=YES	Place 2 TPs @ connector.
	PP24V_ALL_PBUSA	10	FUNC_TEST=YES	
	PP12V8_ALL_PBUSB	10	FUNC_TEST=YES	
	PPVCORE_RUN_GPU	10	FUNC_TEST=YES	Place within 50 mm of power supply.
	PPVCORE_RUN_CPU	10	FUNC_TEST=YES	
	PP1V8_PWRON	10	FUNC_TEST=YES	
	PP2V5_PWRON	10	FUNC_TEST=YES	
	PP5V_PWRON	10	FUNC_TEST=YES	
	PP3V3_PWRON	10	FUNC_TEST=YES	Place 5-10 GND TPs.
	PP5V_RUN	10	FUNC_TEST=YES	
PP3V3_ALL	10	FUNC_TEST=YES		
	=FTP_GND	7 10	FUNC_TEST=YES	
LVDS	LVDS_U0_P	53 56	FUNC_TEST=YES	Place within 25 mm of LVDS connector.
	LVDS_U0_N	53 56	FUNC_TEST=YES	
	LVDS_U1_P	53 56	FUNC_TEST=YES	
	LVDS_U1_N	53 56	FUNC_TEST=YES	
	LVDS_U2_P	53 56	FUNC_TEST=YES	
	LVDS_U2_N	53 56	FUNC_TEST=YES	
	CLKLVDS_U_P	53 56	FUNC_TEST=YES	
	CLKLVDS_U_N	53 56	FUNC_TEST=YES	
	LVDS_L0_P	53 56	FUNC_TEST=YES	
	LVDS_L0_N	53 56	FUNC_TEST=YES	
	LVDS_L1_P	53 56	FUNC_TEST=YES	
	LVDS_L1_N	53 56	FUNC_TEST=YES	
	LVDS_L2_P	53 56	FUNC_TEST=YES	
	LVDS_L2_N	53 56	FUNC_TEST=YES	
	CLKLVDS_L_P	53 56	FUNC_TEST=YES	
	CLKLVDS_L_N	53 56	FUNC_TEST=YES	
	LVDS_DDC_CLK	51 56	FUNC_TEST=YES	
LVDS_DDC_DATA	51 56	FUNC_TEST=YES		
=PP3V3_DDC_LCD	10 56	FUNC_TEST=YES		
PP3V3_LCD_CONN	56	FUNC_TEST=YES		
INVERTER	PPBUS_INVERTER	56	FUNC_TEST=YES	Place within 25 mm of inverter connector.
	PP5V_INV_SW	56	FUNC_TEST=YES	
	BRIGHT_PWM	56	FUNC_TEST=YES	
	GND_INVERTER	56	FUNC_TEST=YES	
UATA	=PP5V_RUN_ODD	10 64	FUNC_TEST=YES	Place within 50 mm of ODD/HDD connector.
	=PP5V_RUN_HDD	10 64	FUNC_TEST=YES	
	PP3V3R5V_RUN_HDD_LOGIC	64	FUNC_TEST=YES	
	UATA_DD<15..0>	6 63 64	FUNC_TEST=YES	
	UATA_DMAR0	63 64	FUNC_TEST=YES	
	UATA_DSTROBE	63 64	FUNC_TEST=YES	
	UATA_DMACK_L	63 64	FUNC_TEST=YES	
	UATA_DA<2..0>	6 63 64	FUNC_TEST=YES	
	UATA_CS0_L	6 63 64	FUNC_TEST=YES	
	UATA_CS1_L	63 64	FUNC_TEST=YES	
	UATA_RESET_L	63 64	FUNC_TEST=YES	
	UATA_HSTROBE	63 64	FUNC_TEST=YES	
	UATA_STOP	63 64	FUNC_TEST=YES	
UATA_INTRO	63 64	FUNC_TEST=YES		
AUDIO	PP5V_PWRON_AUDIO_PVDD	74	FUNC_TEST=YES	Place within 25 mm of audio connector.
	PP5V_PWRON_AUDIO_AVDD	74	FUNC_TEST=YES	
	PP3V3_PWRON_AUDIO_AVDD	74	FUNC_TEST=YES	
	=PP3V3_RUN_AUDIO	10 74	FUNC_TEST=YES	
	=I2C_AUDIO_SCL	8 74	FUNC_TEST=YES	
	=I2C_AUDIO_SDA	8 74	FUNC_TEST=YES	
	I2S0_MCLK	6 74	FUNC_TEST=YES	
	I2S0_BITCLK	6 74	FUNC_TEST=YES	
	I2S0_SYNC	6 74	FUNC_TEST=YES	
	I2S0_SB_TO_DEV_DTO	6 74	FUNC_TEST=YES	
	I2S0_DEV_TO_SB_DTI	22 74	FUNC_TEST=YES	
	AUDIO_LO_MUTE_L	22 74	FUNC_TEST=YES	
	AUDIO_SPKR_MUTE_L	22 74	FUNC_TEST=YES	
	AUDIO_CODEC_RESET_L	22 74	FUNC_TEST=YES	
	AUDIO_SPDIFRX_RESET_L	22 74	FUNC_TEST=YES	
	AUDIO_LO_DET_L	22 74	FUNC_TEST=YES	
	AUDIO_LI_DET_L	22 74	FUNC_TEST=YES	
AUDIO_LO_OPTICAL_PLUG_L	22 74	FUNC_TEST=YES		
AUDIO_LI_OPTICAL_PLUG_L	22 74	FUNC_TEST=YES		
AUDIO_I2S_DTIB_SEL	22 74	FUNC_TEST=YES		
AUDIO_EXT_MCLK_SEL	22 74	FUNC_TEST=YES		
AUDIO_GPIO_11	22 74	FUNC_TEST=YES		
GND_AUDIO_AGND	74	FUNC_TEST=YES		
GND_AUDIO_PGND	74	FUNC_TEST=YES		

Category	Test Point	Pin	FUNC_TEST=	Notes
SYSTEM	PP5V_TPAD_F	10 30	FUNC_TEST=YES	Place within 25 mm of TPAD connector.
	USB_TPAD_P	11 30	FUNC_TEST=YES	
	USB_TPAD_N	11 30	FUNC_TEST=YES	
	PP3V3_PWRON_DS1775_R	10	FUNC_TEST=YES	
	SYS_OVERTEMP_L	11 25 30	FUNC_TEST=YES	
	PP3V3_ALL_HALL_EFFRCT_R	10	FUNC_TEST=YES	
	SYS_LID_OPEN_F	10	FUNC_TEST=YES	
	SYS_POWER_BUTTON_L_F	10	FUNC_TEST=YES	
	=FTP_SLEEP_LED	10	FUNC_TEST=YES	
	SYS_CHARGE_LED_L	24 74	FUNC_TEST=YES	
	SYS_ADAPTER_ANALOG_AC_DET	12 74	FUNC_TEST=YES	
	KBDLED_ANODE	28 30	FUNC_TEST=YES	
	KBDLED_RETURN	28 30	FUNC_TEST=YES	
=I2C_DS1775_SDA	8 30	FUNC_TEST=YES		
=I2C_DS1775_SCL	8 30	FUNC_TEST=YES		
CPU FAN	=PP5V_FAN1_PWR	10 31	FUNC_TEST=YES	Place within 25 mm of fan connector.
	FAN1_TACH	27 31	FUNC_TEST=YES	
	FAN1_PWM	27 31	FUNC_TEST=YES	
	=FTP_GND	7 10	FUNC_TEST=YES	
GPU FAN	=PP5V_FAN2_PWR	10 31	FUNC_TEST=YES	Place within 25 mm of fan connector.
	FAN2_TACH	27 31	FUNC_TEST=YES	
	FAN2_PWM	27 31	FUNC_TEST=YES	
	=FTP_GND	7 10	FUNC_TEST=YES	
ALS	=PP3V3_PWRON_LEFT_ALS	10 31	FUNC_TEST=YES	Place within 25 mm of ALS connector.
	ALS_0_OUT	25 31	FUNC_TEST=YES	
	ALS_GAIN_BOOST	25 28 31	FUNC_TEST=YES	
SCCA	SCCA_RXD	22 24	FUNC_TEST=YES	Place within 25 mm of debug connector.
	SCCA_TXD_L	22 24	FUNC_TEST=YES	
BACKUP BATT	=PPVIO_BU_BATT	10 31	FUNC_TEST=YES	Place within 25 mm of battery connector.
	=PPVOUT_BU_BATT	10 31	FUNC_TEST=YES	
RT USB	=PP5V_PWRON_RIGHT_USB	10 31	FUNC_TEST=YES	Place within 25 mm of right USB connector.
	USB2_RIGHT_PORT_P	11 31	FUNC_TEST=YES	
	USB2_RIGHT_PORT_N	11 31	FUNC_TEST=YES	
LT USB	=PP5V_PWRON_LEFT_USB	10 74	FUNC_TEST=YES	Place within 25 mm of left USB connector.
	USB2_LEFT_PORT_P	11 74	FUNC_TEST=YES	
	USB2_LEFT_PORT_N	11 74	FUNC_TEST=YES	

Functional Test Points

SYNC_MASTER=N/A SYNC_DATE=N/A

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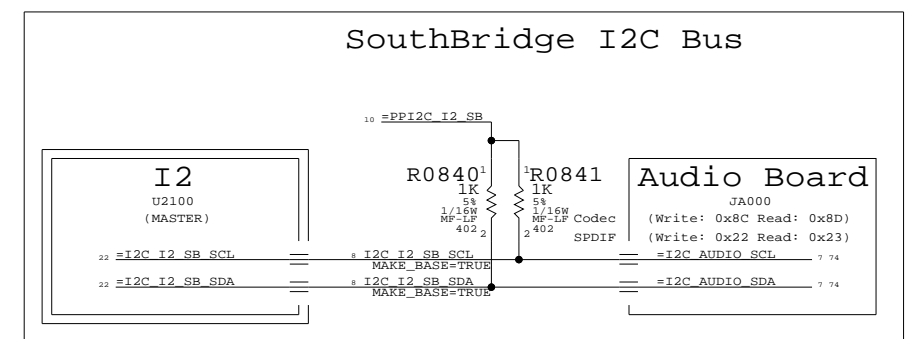
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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6929	03
SCALE	SHT	OF
NONE	7	115

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
	I2C	I2C		I2C_PMU_SMB_SCL
	I2C	I2C		I2C_PMU_SMB_SDA
	I2C	I2C		I2C_PMU_SCL
	I2C	I2C		I2C_PMU_SDA
I2C_NB	I2C	I2C		I2C_I2_NB_SCL
I2C_NB	I2C	I2C		I2C_I2_NB_SDA
	I2C	I2C		I2C_I2_SB_SCL
	I2C	I2C		I2C_I2_SB_SDA
	I2C	I2C		I2C_GPU_TMDS_SCL
	I2C	I2C		I2C_GPU_TMDS_SDA

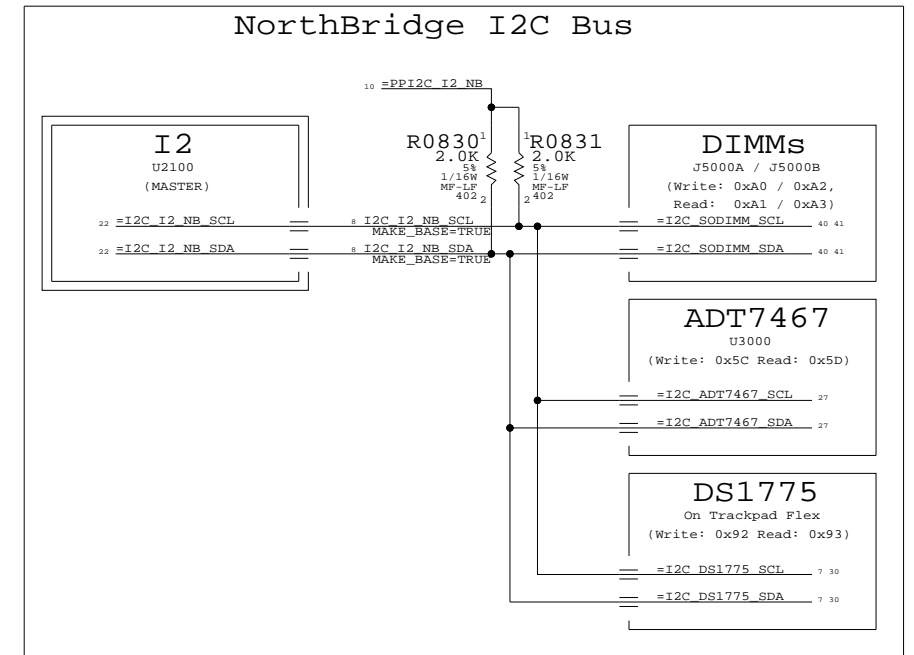
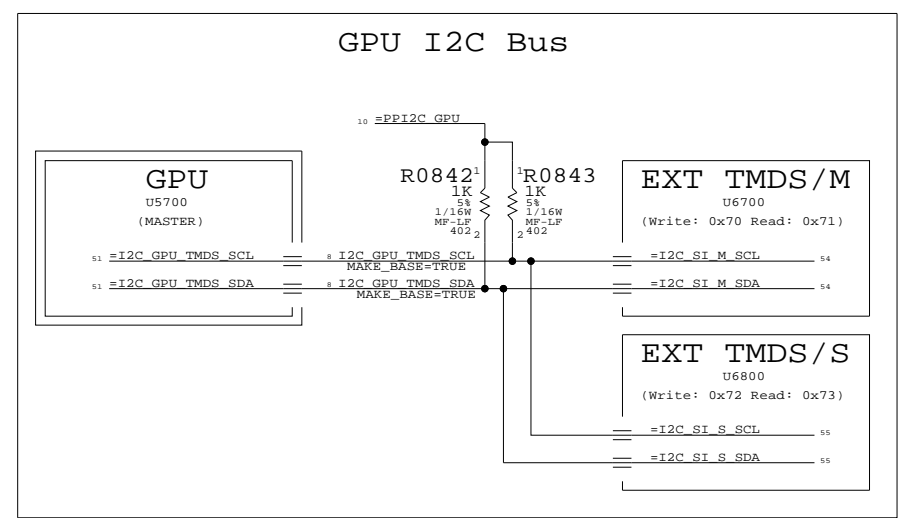
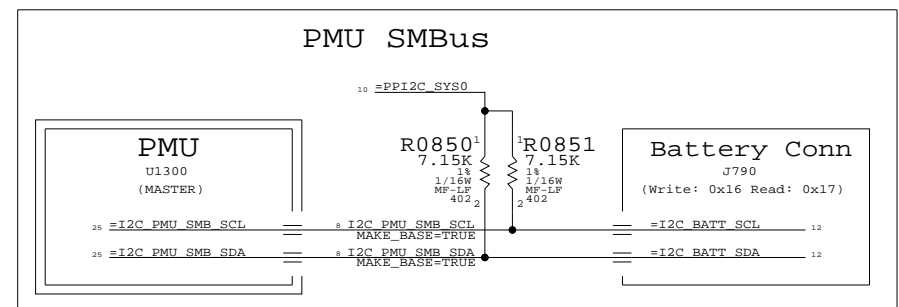
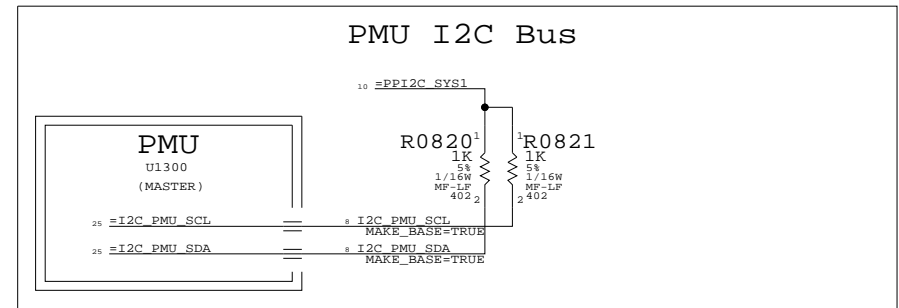


Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- GOV_I2C / GOV_I2C_BYPASS
Allows bypassing Governor I2C bus. Most devices are connected directly to PMU instead. One ADT7467 connects to NB I2C bus 1 to resolve address conflict.
- MMM_PWR_ALL / MMM_PWR_PWRON
Selects whether MMM MCU is powered all the time or only when the system is on. ALL moves the MCU to the PMU I2C bus so it can be monitored by in shutdown.
NOTE: Neither option is necessary when MMM_MCU_PMU BOM option is selected.



I2C Connections

SYNC_MASTER=N/A SYNC_DATE=N/A

NOTICE OF PROPRIETARY PROPERTY

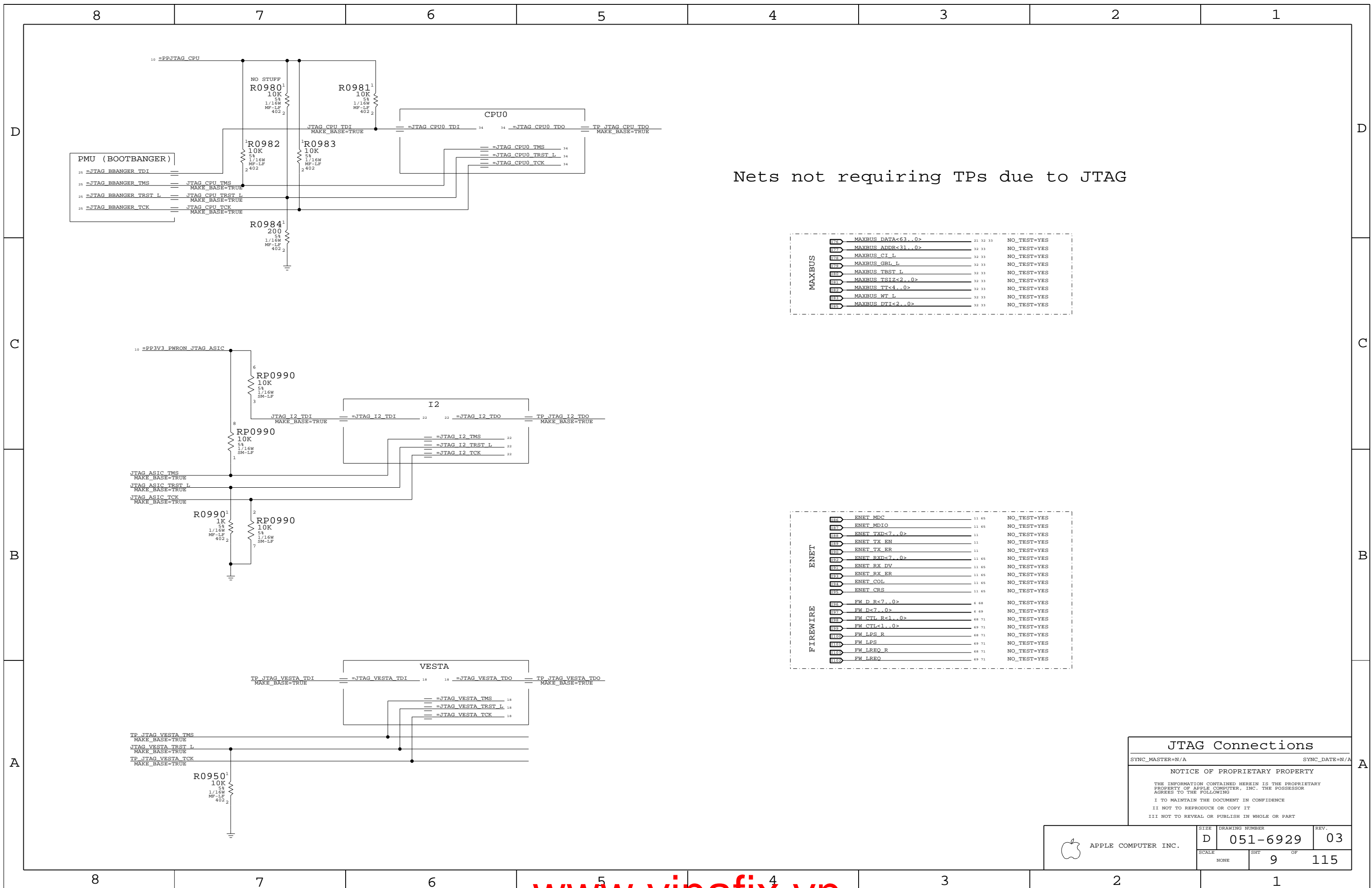
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	D	051-6929	03
SCALE	NONE	SHT	OF
		8	115



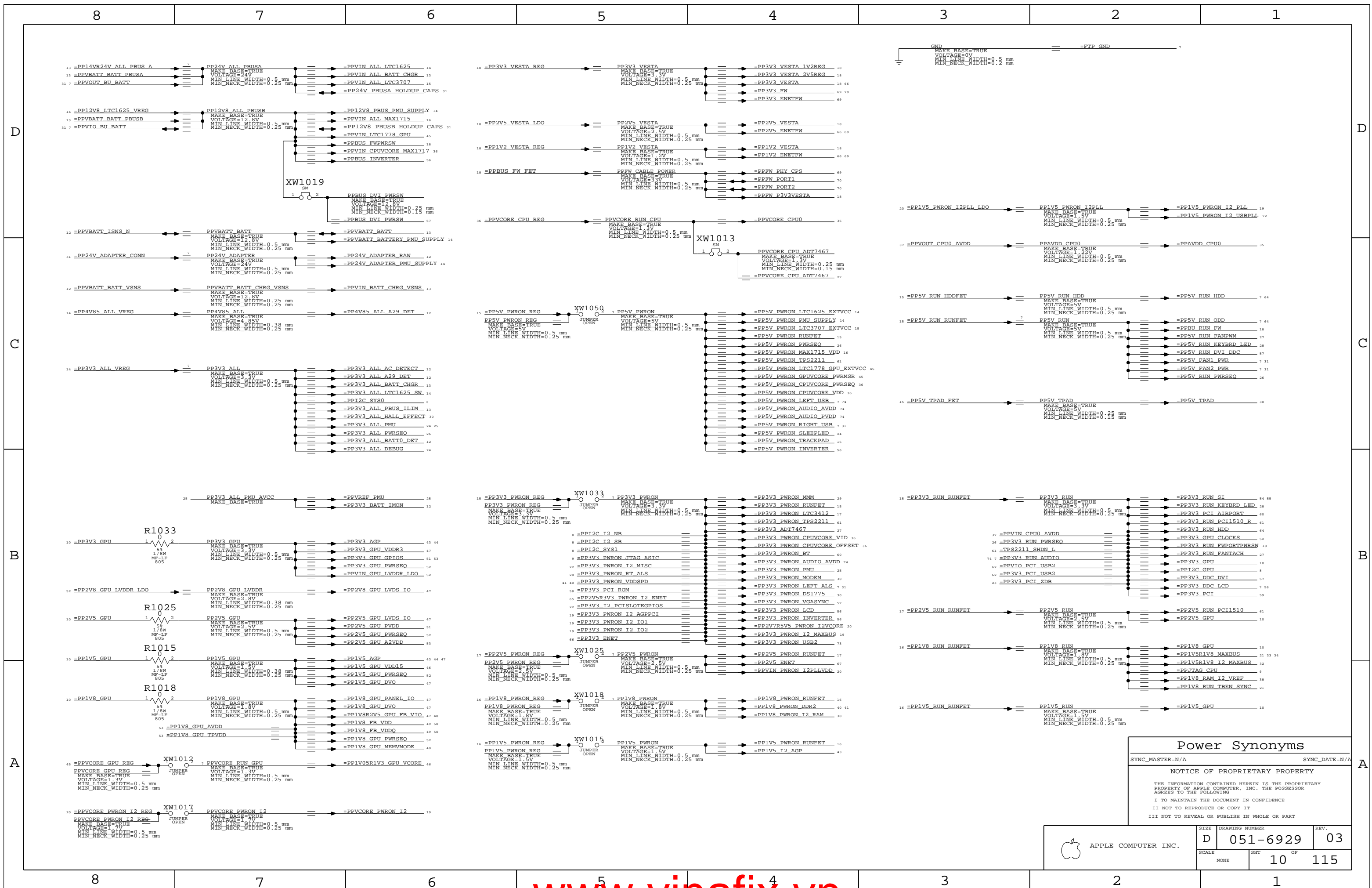
Nets not requiring TPs due to JTAG

NET	TEST POINT	TEST POINT VALUE	TEST POINT TYPE
MAXBUS	MAXBUS_DATA<63..0>	32 33	NO_TEST=YES
MAXBUS	MAXBUS_ADDR<31..0>	32 33	NO_TEST=YES
MAXBUS	MAXBUS_CE_L	32 33	NO_TEST=YES
MAXBUS	MAXBUS_GBL_L	32 33	NO_TEST=YES
MAXBUS	MAXBUS_TRST_L	32 33	NO_TEST=YES
MAXBUS	MAXBUS_TSIZ<2..0>	32 33	NO_TEST=YES
MAXBUS	MAXBUS_TT<4..0>	32 33	NO_TEST=YES
MAXBUS	MAXBUS_WT_L	32 33	NO_TEST=YES
MAXBUS	MAXBUS_DTI<2..0>	32 33	NO_TEST=YES

NET	TEST POINT	TEST POINT VALUE	TEST POINT TYPE
ENET	ENET_MDC	11 65	NO_TEST=YES
ENET	ENET_MDIO	11 65	NO_TEST=YES
ENET	ENET_TXD<7..0>	11	NO_TEST=YES
ENET	ENET_TX_EN	11	NO_TEST=YES
ENET	ENET_TX_ER	11	NO_TEST=YES
ENET	ENET_RXD<7..0>	11 65	NO_TEST=YES
ENET	ENET_RX_DV	11 65	NO_TEST=YES
ENET	ENET_RX_ER	11 65	NO_TEST=YES
ENET	ENET_COL	11 65	NO_TEST=YES
ENET	ENET_CRD	11 65	NO_TEST=YES
FW	FW_D_R<7..0>	6 69	NO_TEST=YES
FW	FW_D<7..0>	6 69	NO_TEST=YES
FW	FW_CTL_R<1..0>	48 71	NO_TEST=YES
FW	FW_CTL<1..0>	49 71	NO_TEST=YES
FW	FW_LPS_R	48 71	NO_TEST=YES
FW	FW_LPS	49 71	NO_TEST=YES
FW	FW_LREQ_R	48 71	NO_TEST=YES
FW	FW_LREQ	49 71	NO_TEST=YES

JTAG Connections
 SYNC_MASTER=N/A SYNC_DATE=N/A
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6929	03
SCALE	NONE	SHT	OF
		9	115

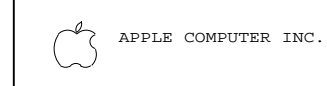


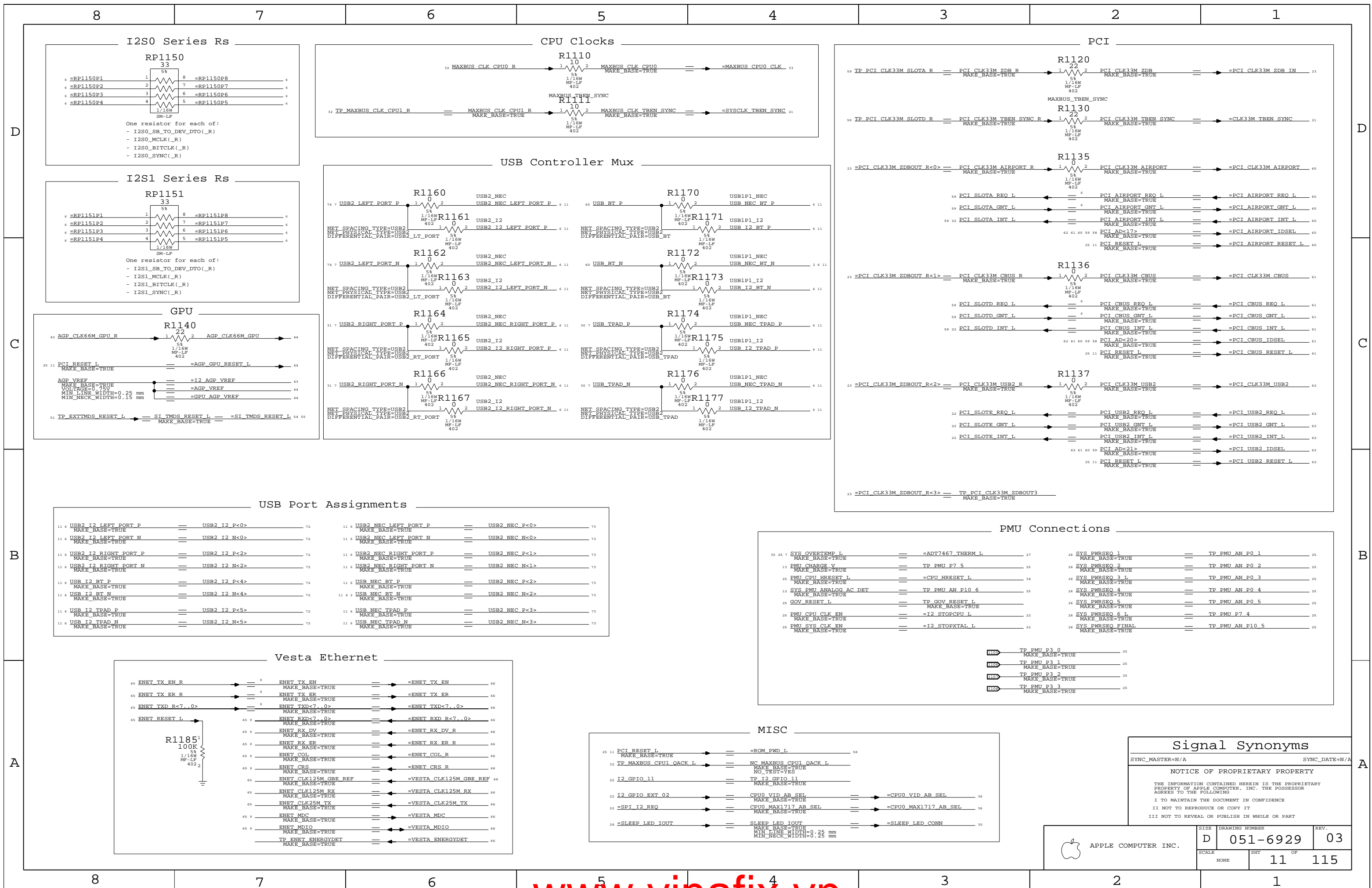
Power Synonyms

SYNC_MASTER=N/A SYNC_DATE=N/A

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SCALE NONE	DIT 10	OF 115	SIZE	DRAWING NUMBER	REV.
			D	051-6929	03





Signal Synonyms

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SCALE NONE	SHEET 11	OF 115	SIZE	DRAWING NUMBER	REV.
			D	051-6929	03

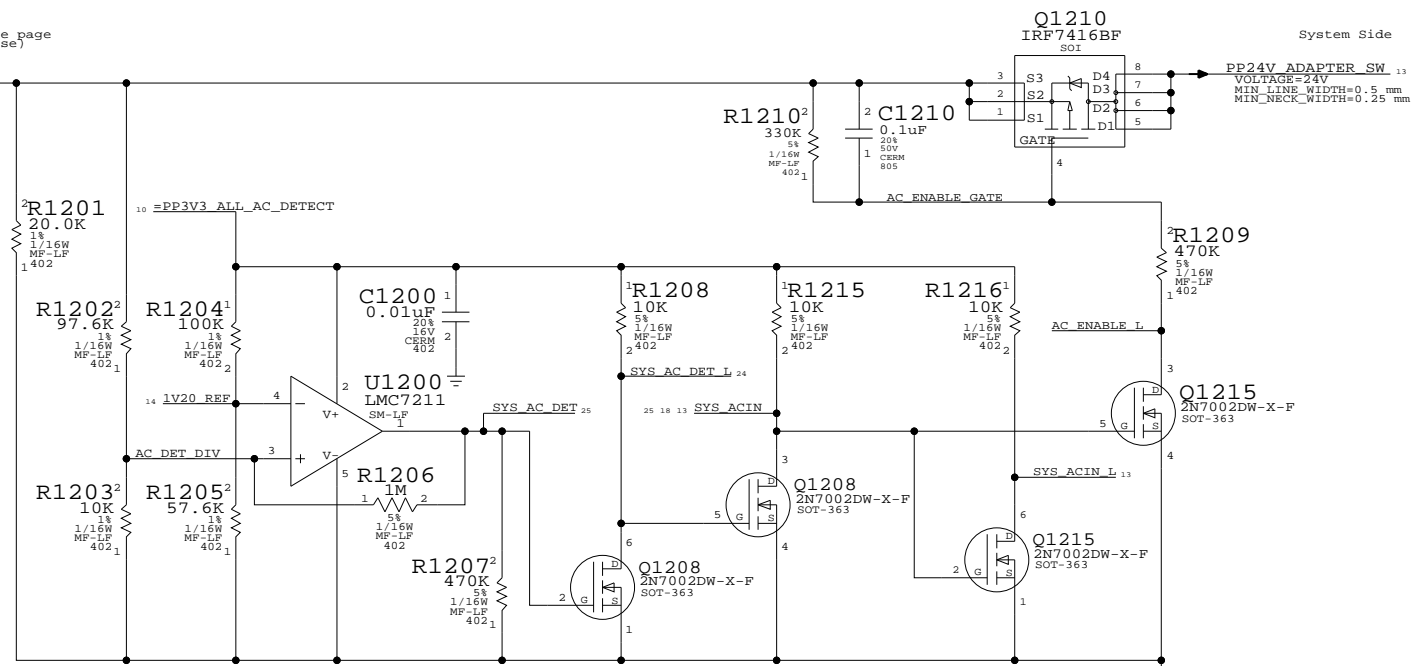


APPLE COMPUTER INC.

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
PP3V	THERM	THERM	BATTERY_ISNS
PP3V	THERM	THERM	BATTERY_ISNS

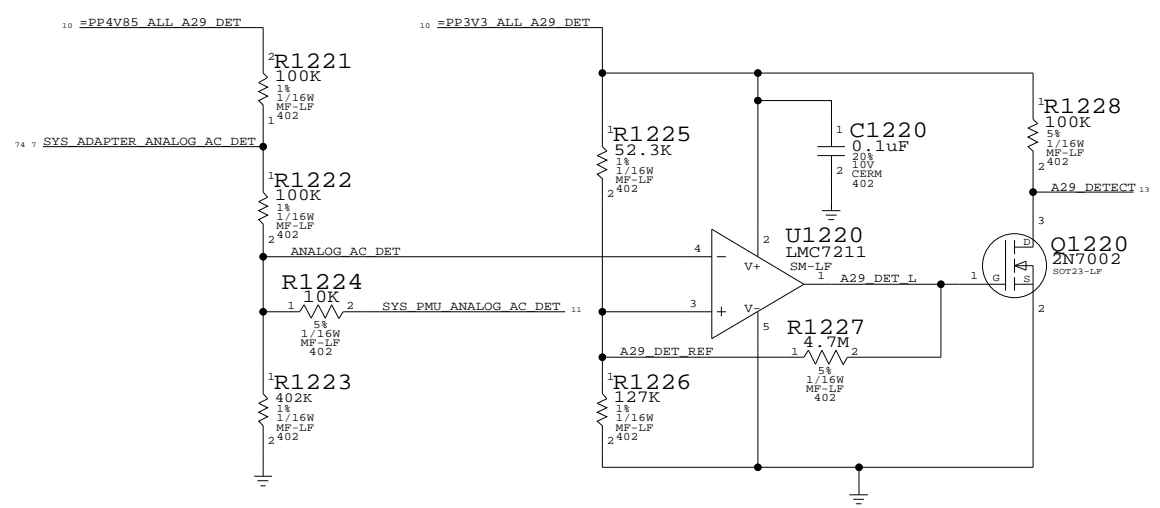
ADAPTER INPUT/INRUSH LIMITER

Adapter Connector Side
(Connector is on separate page to facilitate design reuse)



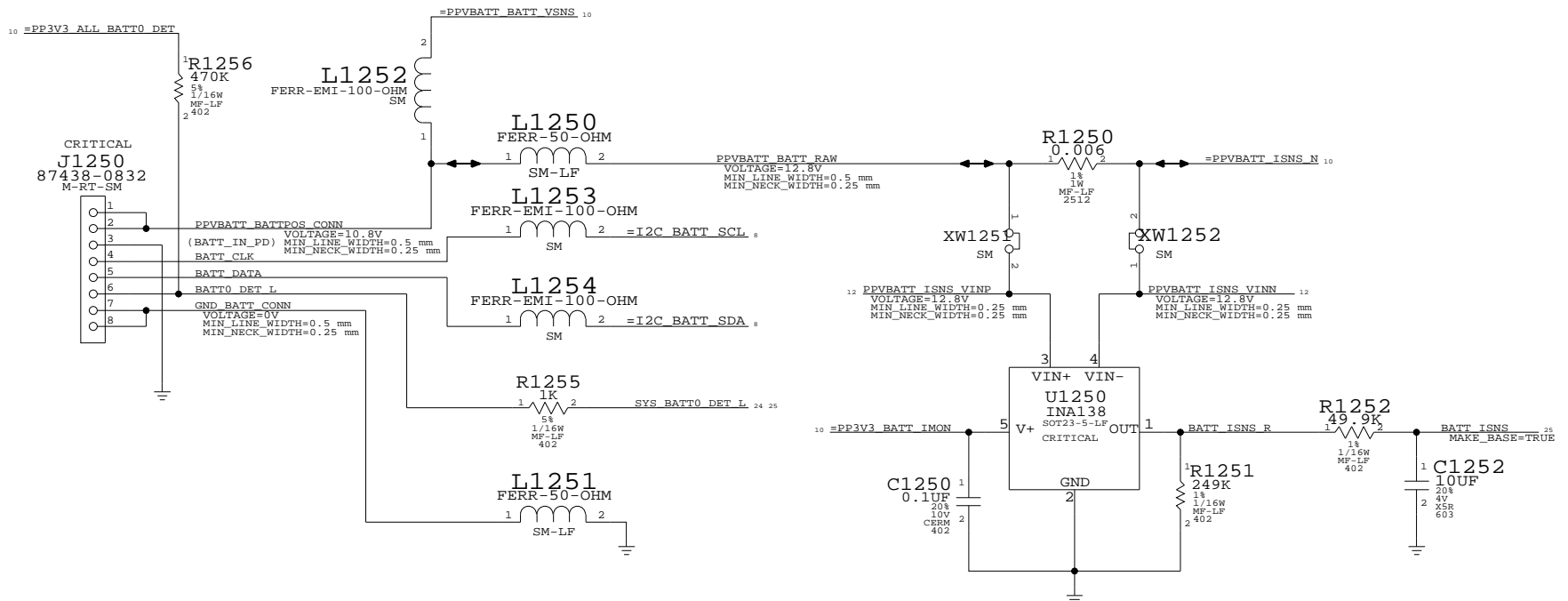
GREATER THAN 13.1V DETECT
SYS AC_DET indicates adapter presence. SYS ACIN is code-controlled signal to enable use of AC in system. Q1208 ensures SYS ACIN goes low as soon as SYS AC_DET goes low. Therefore, hardware immediately disables the AC upon removal but only software can enable AC after detection by the PMU.

A29 ADAPTER DETECTION



ADAPTER IDS		
ADAPTER	ID RANGE	PIN VOLTAGE
Q11 (65W)	1.65-2.31V	2.007-2.066V
A29 (45W)	2.31-2.97V	2.558-2.661V
AIRLINE	0.33-0.99V	0.589-0.663V

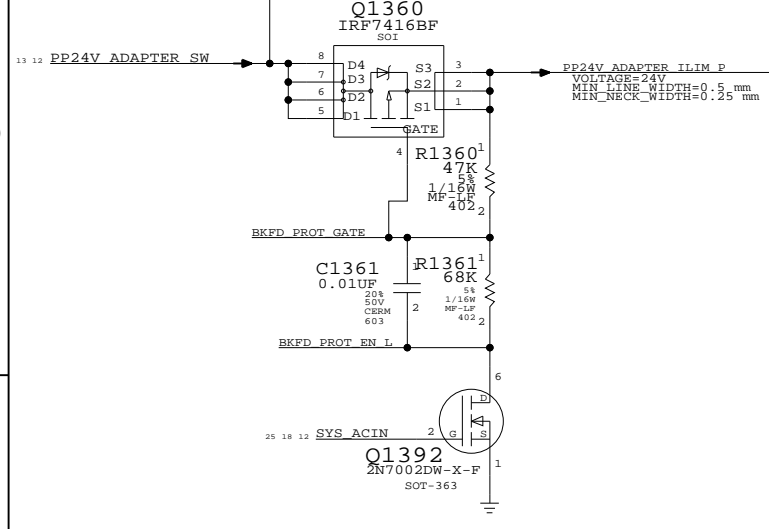
BATTERY INPUT/CURRENT SENSE



Power Inputs
 SYNC_MASTER=N/A SYNC_DATE=N/A
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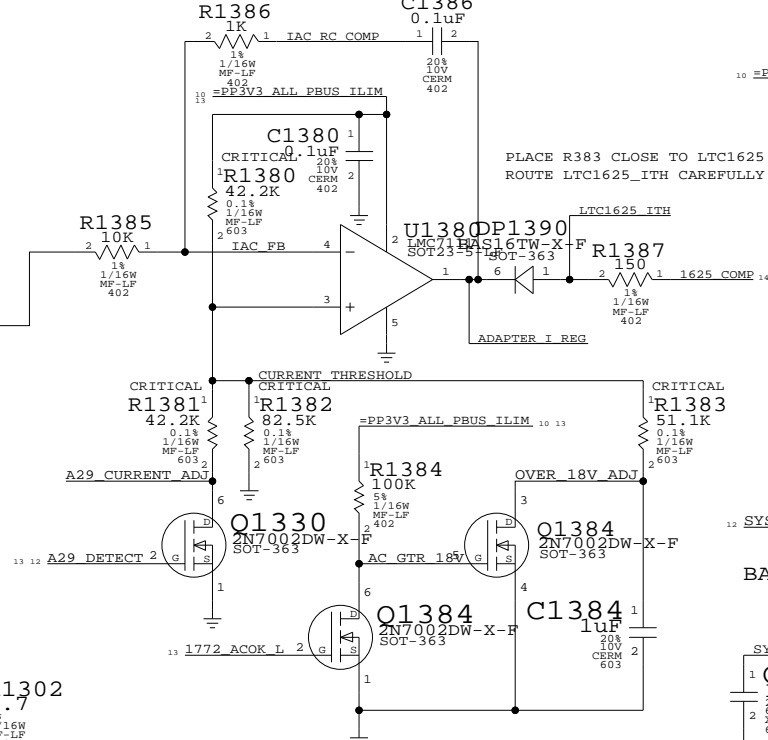
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	NONE	051-6929	03
SCALE		SHT	OF
NONE		12	115

BACKFEED PROTECTION

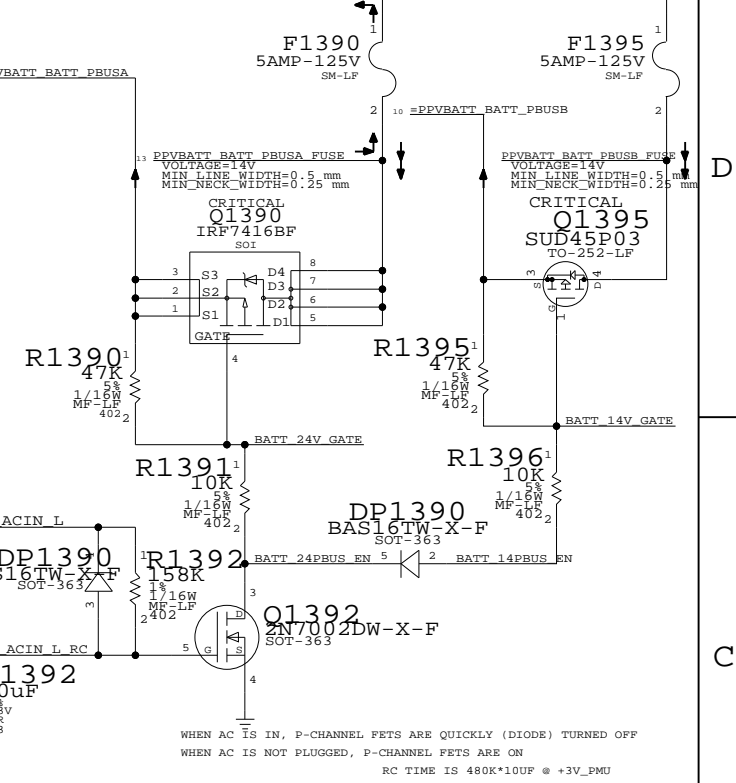


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
11480343	1	RES,20K,1%,1/16W,MF-LF,402	R1345	Q16C_PARTS
11480382	1	RES,48.7K,1%,1/16W,MF-LF,402	R1345	Q41C_PARTS

+PBUS CURRENT LIMIT

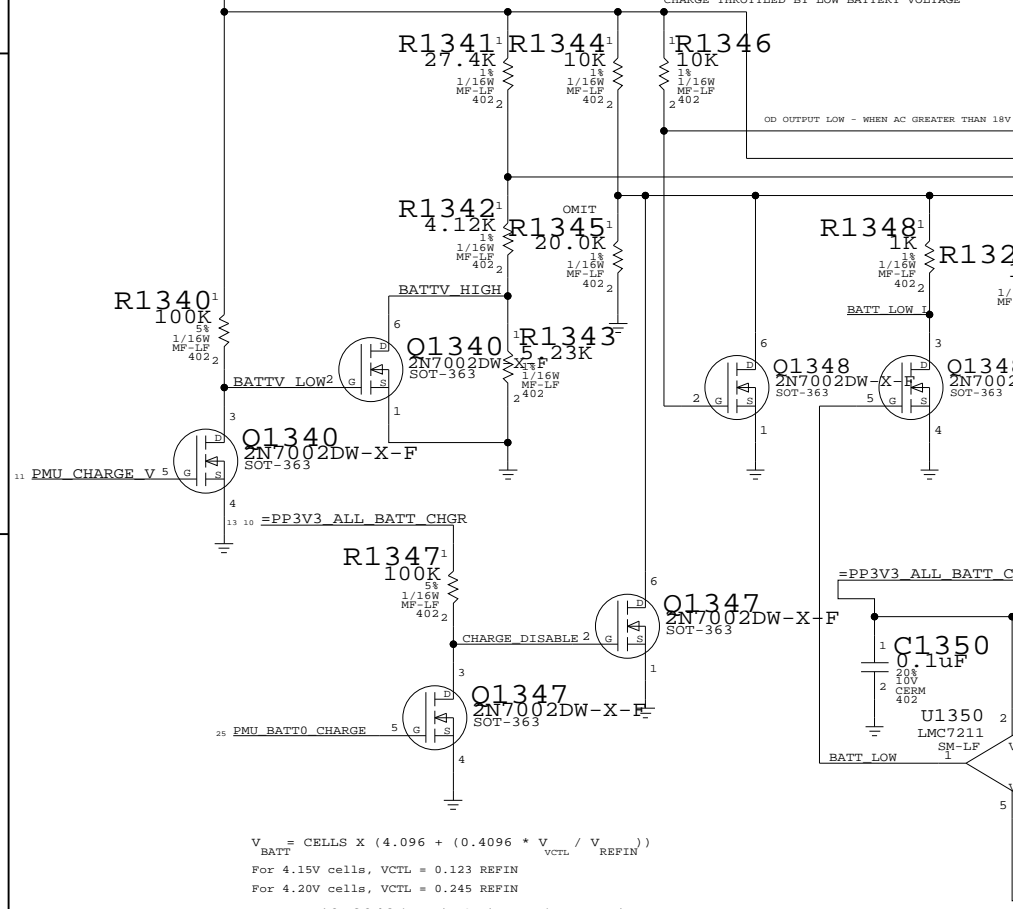


BATTERY SWITCH-OVER CIRCUIT

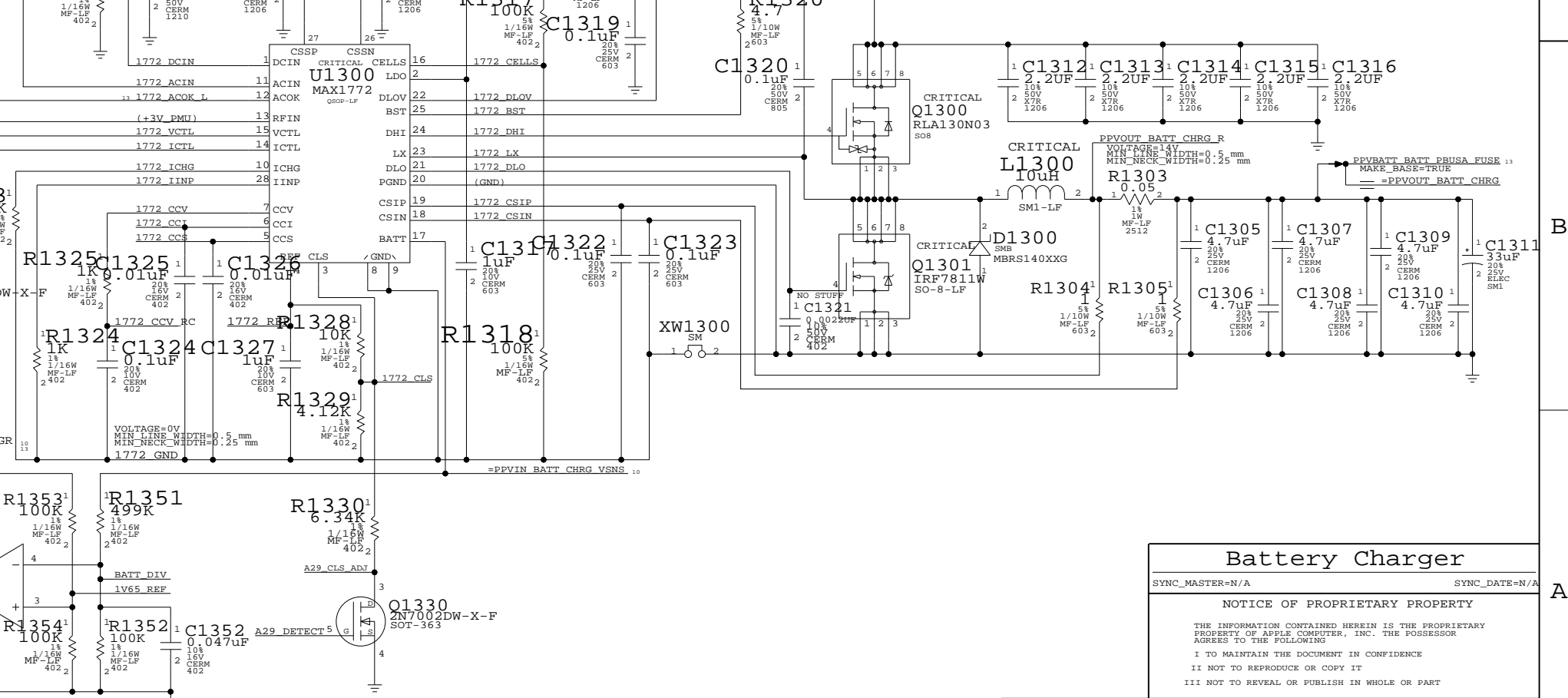


SWITCHER VOLTAGE CONTROL

SWITCHER CURRENT CONTROL



$V_{BATT} = CELLS \times (4.096 + (0.4096 \times V_{VCTL} / V_{REFIN}))$
 For 4.15V cells, VCTL = 0.123 REFIN
 For 4.20V cells, VCTL = 0.245 REFIN
 $I_{CHG} = (0.2048 / R_{62}) \times (V_{ICTL} / V_{REFIN})$



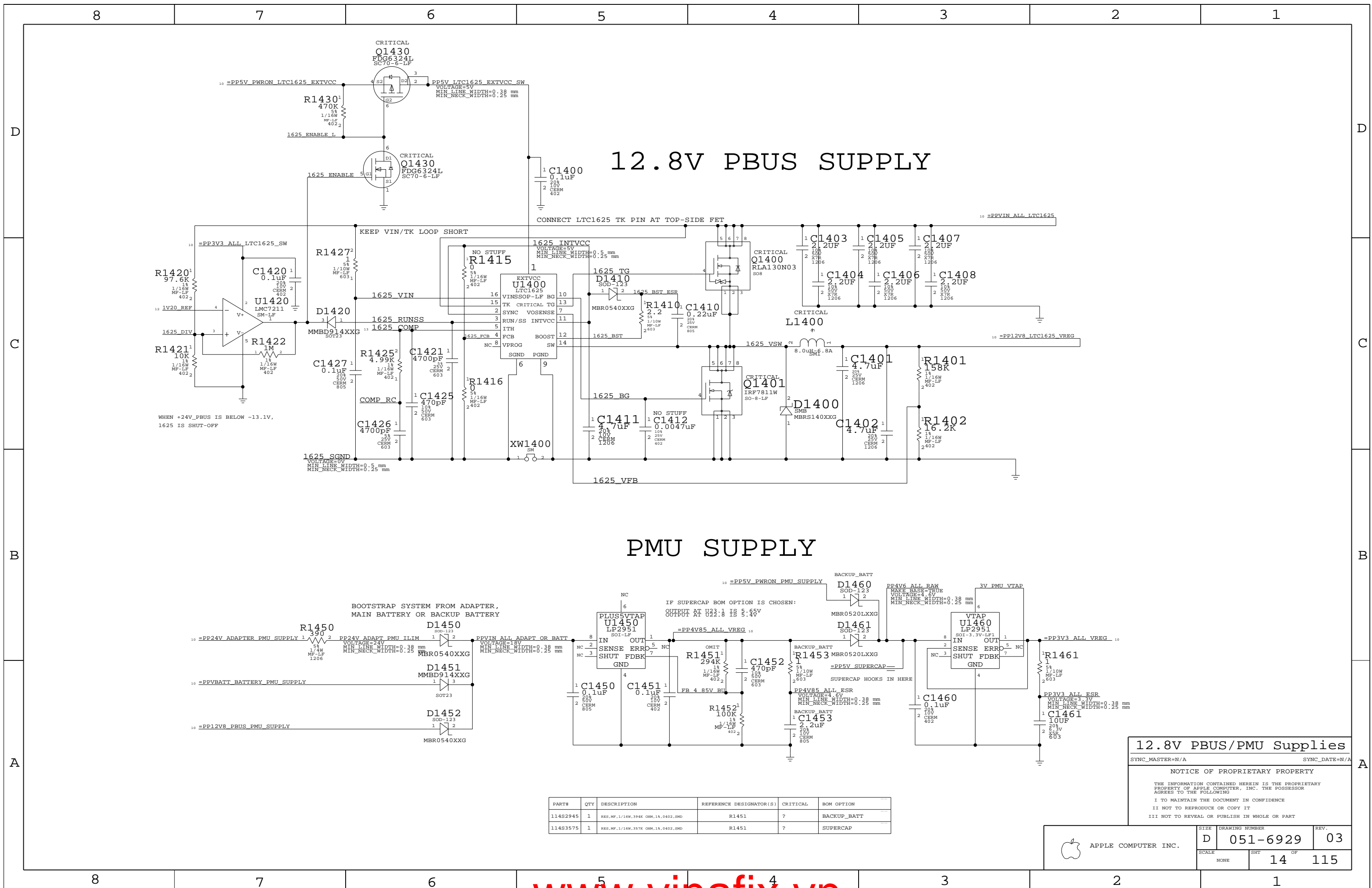
Battery Charger

SYNC_MASTER=N/A SYNC_DATE=N/A

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	DRAWING NUMBER		REV.
	D	051-6929	03
SCALE		SHT	OF
NONE		13	115



12.8V PBUS SUPPLY

PMU SUPPLY

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S2945	1	RES,MP,1/16W,394K OHM,1%,0402,SMD	R1451	?	BACKUP_BATT
114S3575	1	RES,MP,1/16W,357K OHM,1%,0402,SMD	R1451	?	SUPERCAP

12.8V PBUS/PMU Supplies

SYNC_MASTER=N/A SYNC_DATE=N/A

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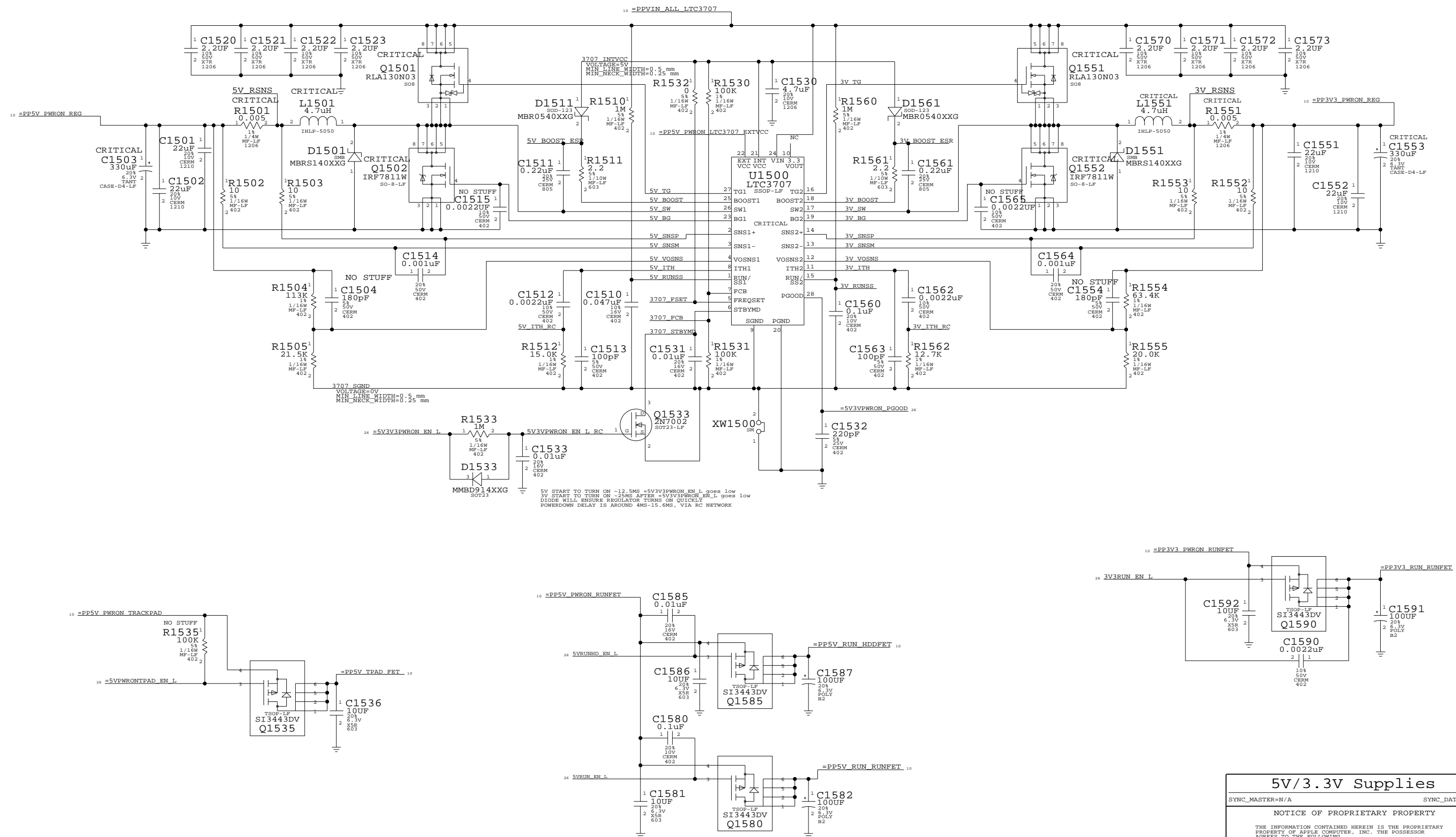
II NOT TO REPRODUCE OR COPY IT

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APPLE COMPUTER INC.

SCALE	DRAWING NUMBER	REV.
NONE	D 051-6929	03
	SHT	OF
	14	115

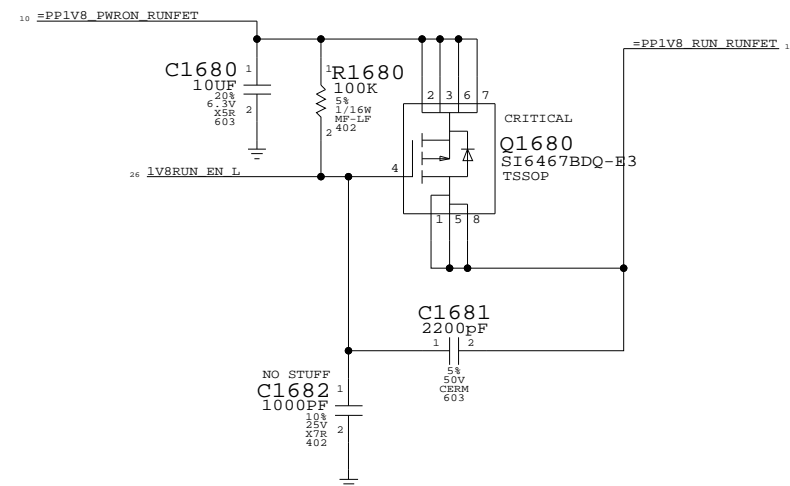
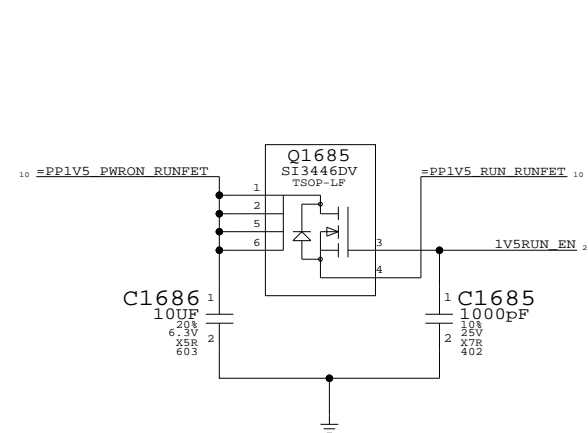
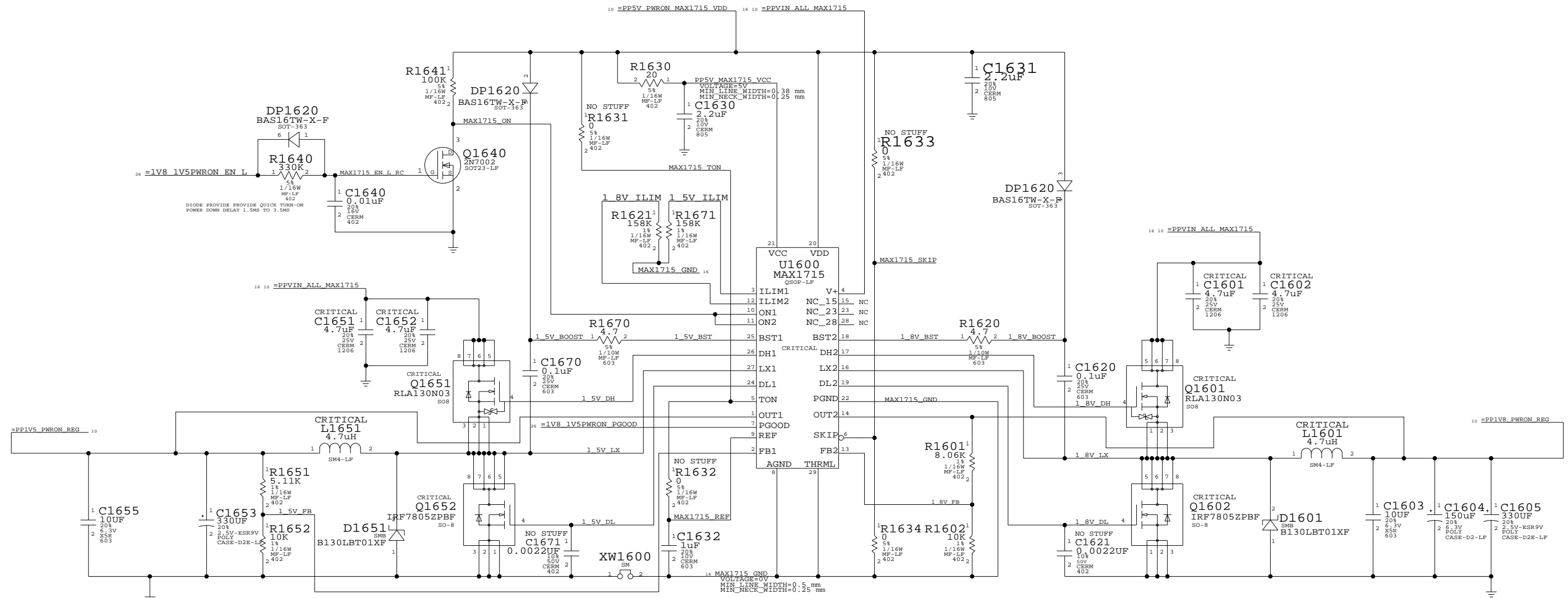
3.3V/5V SWITCHER



5V/3.3V Supplies
 SYNC_MASTER=N/A SYNC_DATE=N/A
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6929	03
SCALE	SHT	OF	
NONE	15	115	

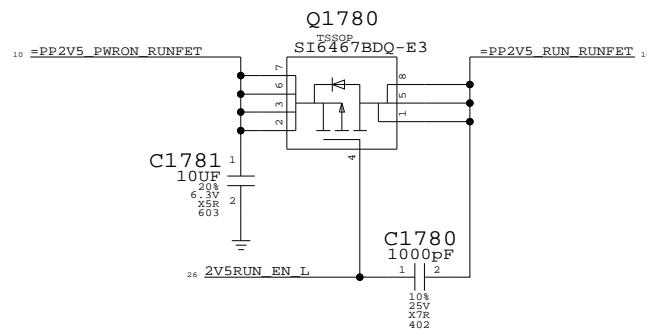
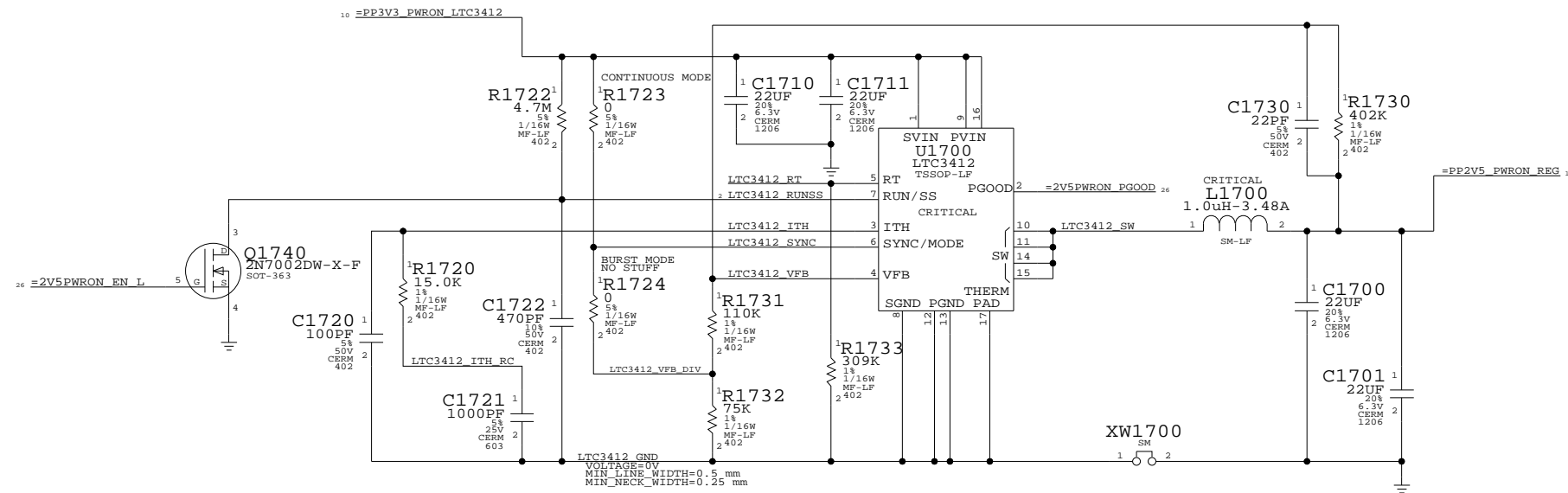
1.5V/1.8V SWITCHER



1.8V/1.5V Supplies		
SYNC_MASTER=N/A	SYNC_DATE=N/A	
NOTICE OF PROPRIETARY PROPERTY		
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6929	03
SCALE	SHT	OF	
NONE	16	115	

2.5V SWITCHER



2.5V Supply

SYNC_MASTER=N/A SYNC_DATE=N/A

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	D	051-6929	03
SCALE	NONE	SHT OF	17 OF 115

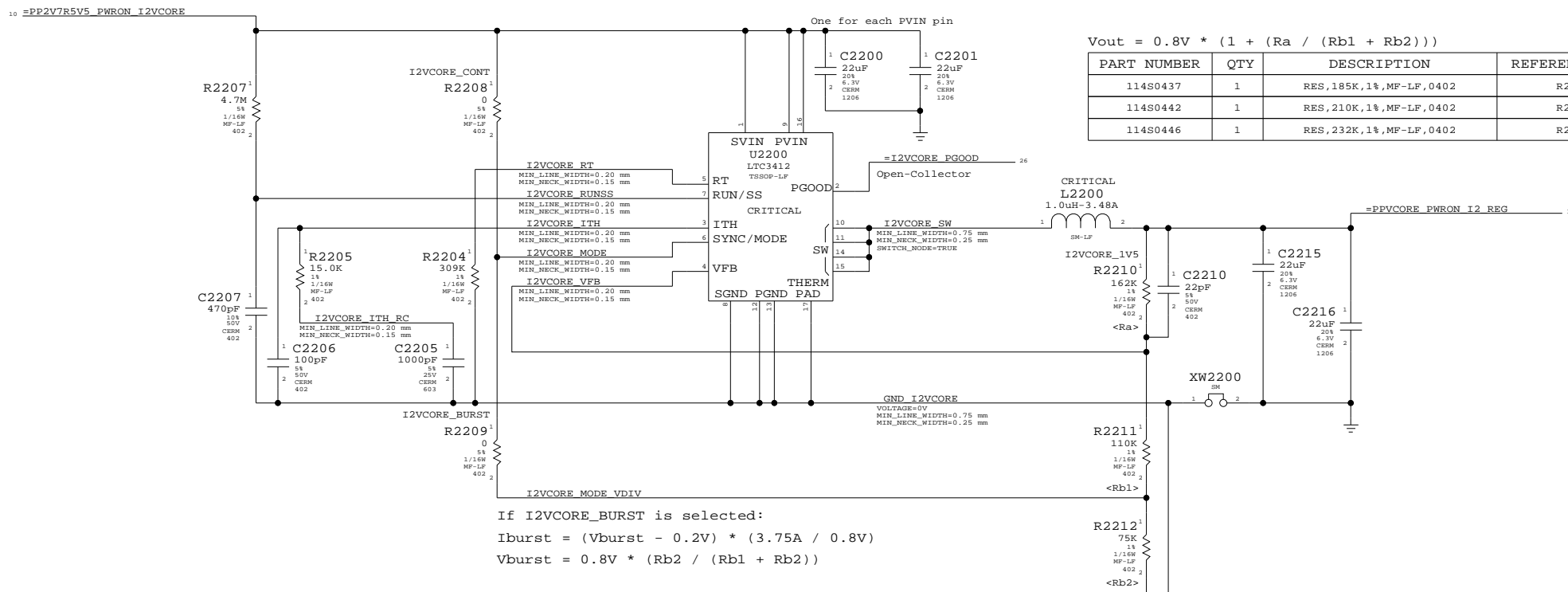
Page Notes

Power aliases required by this page:
 - =PP2V7R5V5_PWRON_I2VCORE
 - =PPVCORE_PWRON_I2_REG
 - =PPVIN_PWRON_I2PLLVD
 - =PP1V5_PWRON_I2PLLVD_LDO

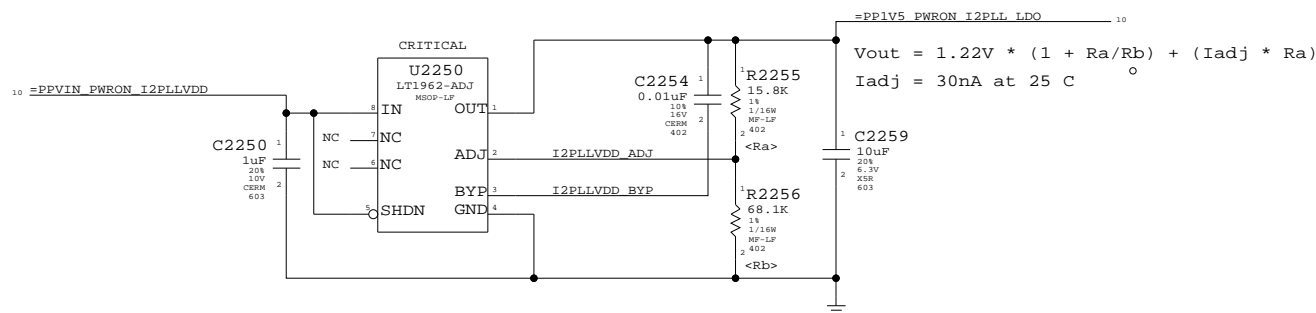
Signal aliases required by this page:
 - =I2VCORE_PGOOD

BOM options provided by this page:
 - I2VCORE_CONT / I2VCORE_BURST
 Selects between forced continuous and burst mode for LTC3412 regulator.
 - I2VCORE_XVX
 Selects appropriate resistor for the indicated LTC3412 output voltage.

I2 VCore Regulator



I2 PLL LDO



I2 Power Supplies

SYNC_MASTER=N/A SYNC_DATE=N/A

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	D	051-6929	03
SCALE	SHT	OF	
NONE	22	115	

ELECTRICAL_CONSTRAINT_SET	NET_TYPE	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
I2S0_DTT	I2S	128	128	I2S0_DEV_TO_SB_DTI
I2S0_DTT	I2S	128	128	I2S0_SB_TO_DEV_DTO_R
I2S0_MCLK	I2S	128	128	I2S0_MCLK_R
I2S0_BITCLK	I2S	128	128	I2S0_BITCLK_R
I2S0_SYNC	I2S	128	128	I2S0_SYNC_R
I2S1_DTT	I2S	128	128	I2S1_DEV_TO_SB_DTI
I2S1_DTT	I2S	128	128	I2S1_SB_TO_DEV_DTO_R
I2S1_MCLK	I2S	128	128	I2S1_MCLK_R
I2S1_BITCLK	I2S	128	128	I2S1_BITCLK_R
I2S1_SYNC	I2S	128	128	I2S1_SYNC_R
I2_CLK18M_XOUT	XTAL	XTAL	XTAL	I2_CLK18M_XOUT
I2_CLK18M_XOUT	XTAL	XTAL	XTAL	I2_CLK18M_XOUT
I2_CLK18M_XIN	XTAL	XTAL	XTAL	I2_CLK18M_XIN

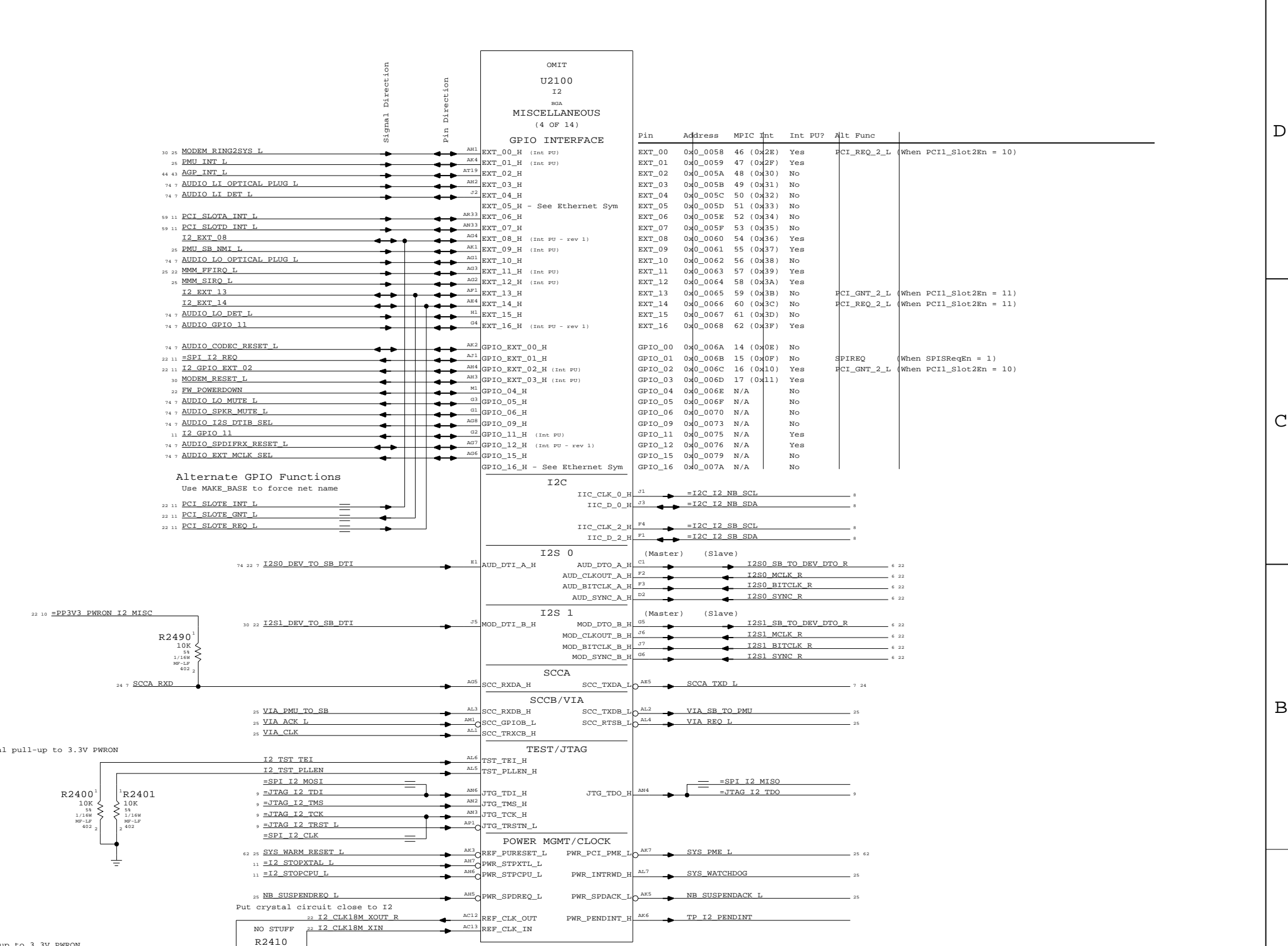
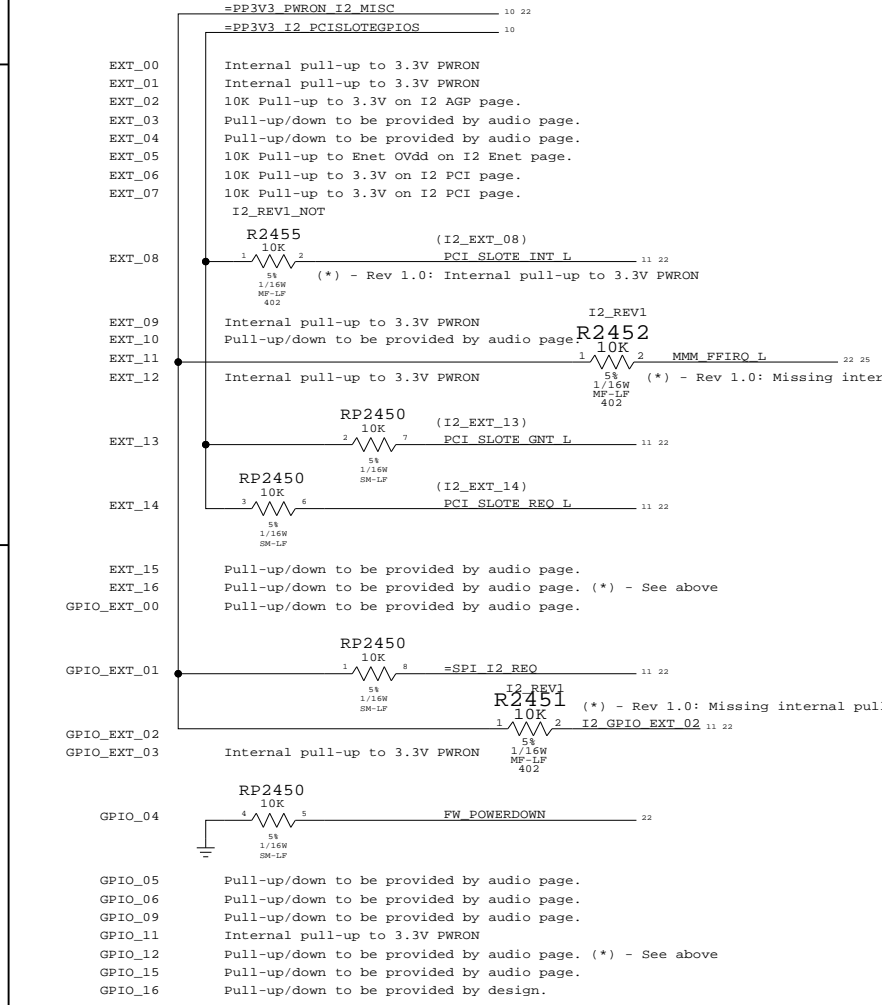
Page Notes

Power aliases required by this page:
 - =PP3V3_PWRON_I2_GPIO
 - =PP3V3_I2_PCISLOTGPIO (PWRON or PCI)
 Should be same as =PP3V3_PCI if slot E is used, or else =PP3V3_PWRON_I2_GPIO.

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 - I2_REV1_NOT
 Use for I2 revisions > 1.0

GPIO Pull-ups / Pull-downs



I2 Miscellaneous		
SYNC_MASTER=N/A		SYNC_DATE=N/A
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APPLE COMPUTER INC.	SCALE	DRAWING NUMBER	REV.
	NONE	D 051-6929	03
	SHEET	OF	
	24	115	

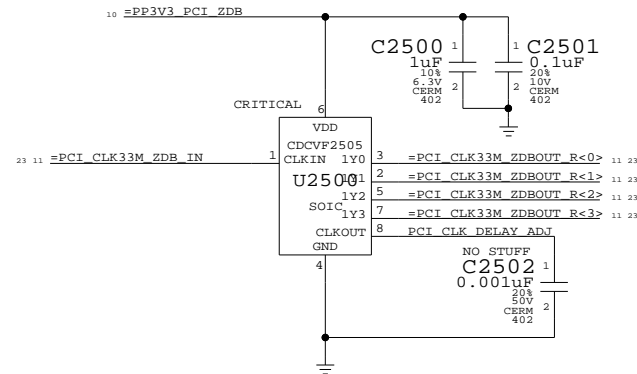
ELECTRICAL_CONSTRAINT_SET	NET_TYPE		DIFFERENTIAL_PAIR
	SPACING	PHYSICAL	
PCI_ZDBOUT0	CLOCK	CLOCK	
PCI_ZDBOUT1	CLOCK	CLOCK	
PCI_ZDBOUT2	CLOCK	CLOCK	
PCI_ZDBOUT3	CLOCK	CLOCK	

Page Notes

Power aliases required by this page:
 - =PP3V3_PWRON_I2_GPIO
 - =PP3V3_I2_PCISLOTGPIO (PWRON or PCI)
 Should be same as =PP3V3_PCI if slot E is used, or else =PP3V3_PWRON_I2_GPIO.

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 - I2_REV1_NOT
 Use for I2 revisions > 1.0



PCI Clock Buffer

SYNC_MASTER=N/A SYNC_DATE=N/A

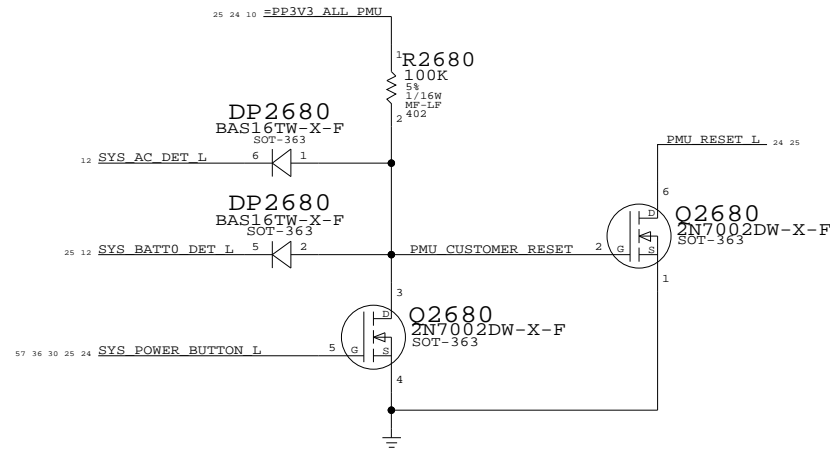
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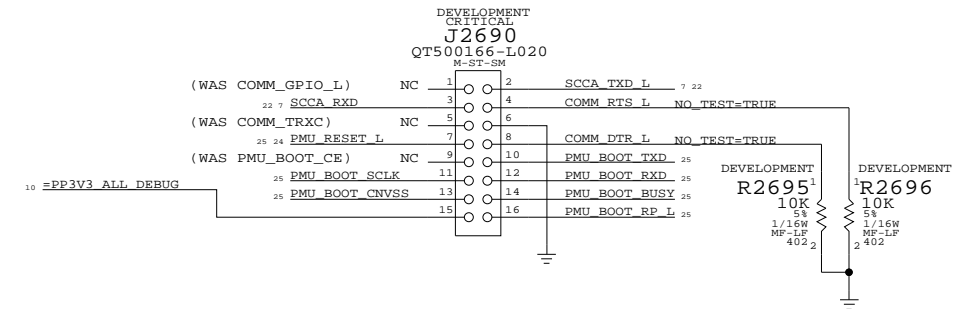
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	D	051-6929	03
SCALE	SHT	OF	
NONE	25	115	

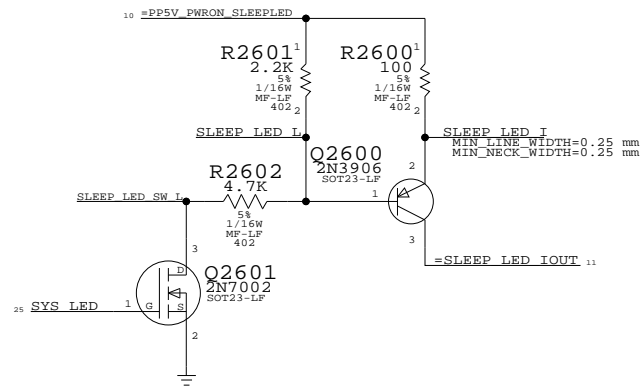
PMU RESET CIRCUIT



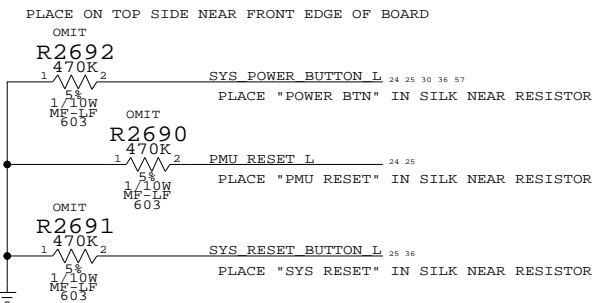
SERIAL DEBUG INTERFACE



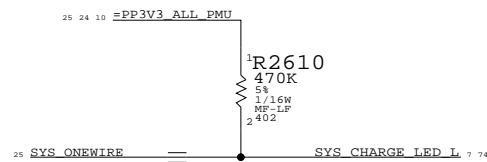
SLEEP LED



DEBUGGING AIDS



CHARGE LED



LEDs/Reset/Debug

SYNC_MASTER=N/A SYNC_DATE=N/A

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	D	051-6929	03
SCALE	SHT OF		
NONE	26		115

Power Management Unit

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		DIFFERENTIAL_PAIR	
SPACING	PHYSICAL	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
5x	1/16W	XTAL	XTAL		PMU_CLK10M_XIN
5x	1/16W	XTAL	XTAL		PMU_CLK10M_XOUT
5x	1/16W	XTAL	XTAL		PMU_CLK10M_XOUT_R
5x	1/16W	XTAL	XTAL		PMU_CLK32K_XIN
5x	1/16W	XTAL	XTAL		PMU_CLK32K_XOUT
5x	1/16W	XTAL	XTAL		PMU_CLK32K_XOUT_R

Page Notes

Power aliases required by this page:

- PP3V3_ALL_PMU
- PP3V3_PWRON_PMU
- PPVREF_PMU (PMU AVCC or 2.5V reference)

Signal aliases required by this page:

- I2C_PMU_SCL
- I2C_PMU_SDA
- I2C_PMU_SMB_SCL
- I2C_PMU_SMB_SDA
- JTAG_BBANGER_TCK
- JTAG_BBANGER_TDI
- JTAG_BBANGER_TMS
- JTAG_BBANGER_TRST_L

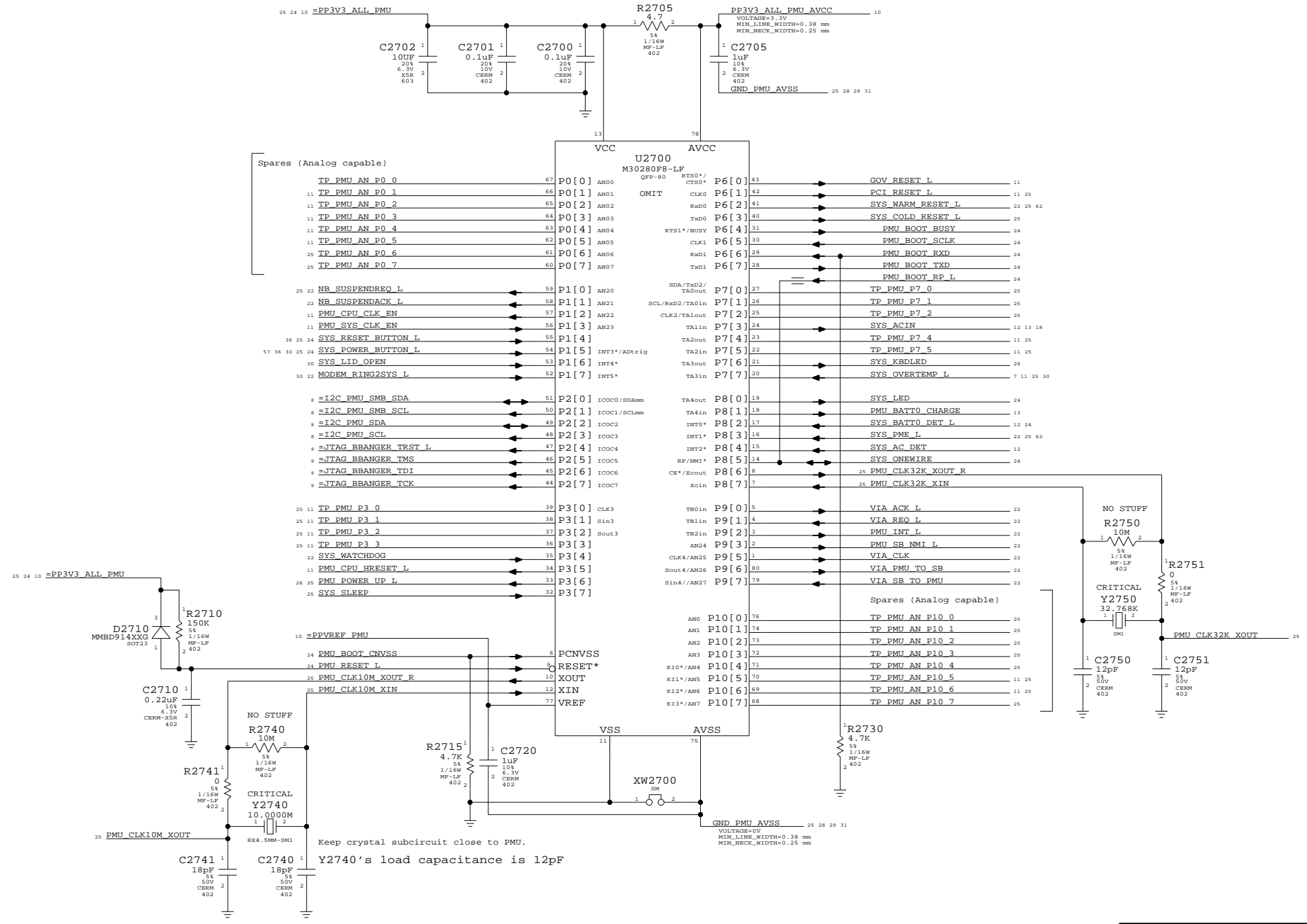
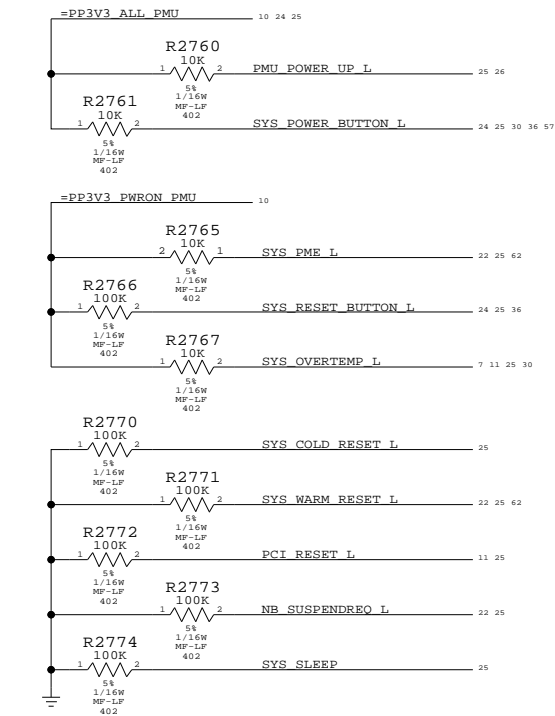
NOTE: Boot-banger pins can be aliased to TP_ or NC_ if not implemented.

BOM options provided by this page: (NONE)

NOTE: TP_PMU_Fx_x signals are general-purpose spares. Some pins are reserved for alternate functions. TP_PMU_AN_Fx_x signals are general-purpose spares that can also be used as analog inputs.

NOTE: All analog inputs to PMU should have a 100pF capacitor to the PMU AVSS signal (GND_PMU_AVSS). None of those capacitors are provided on this page.

PMU Pull-ups / pull-downs



Additional PMU05 "Modules"

MMM	ALS	SPI Dual Battery Charger	Battery Current Mon
TP_PMU_AN_P10_0	TP_PMU_AN_P10_3	TP_PMU_P3_0	TP_PMU_AN_P10_7
TP_PMU_AN_P10_1	TP_PMU_AN_P10_4	TP_PMU_P3_1	
TP_PMU_AN_P10_2	TP_PMU_P7_2	TP_PMU_P3_2	
TP_PMU_P7_0		TP_PMU_P3_3	
TP_PMU_P7_1		TP_PMU_P7_4	
TP_PMU_AN_P0_7		TP_PMU_P7_5	
TP_PMU_AN_P0_6			

Power Management Unit (PMU05)

SYNC_MASTER=N/A SYNC_DATE=N/A

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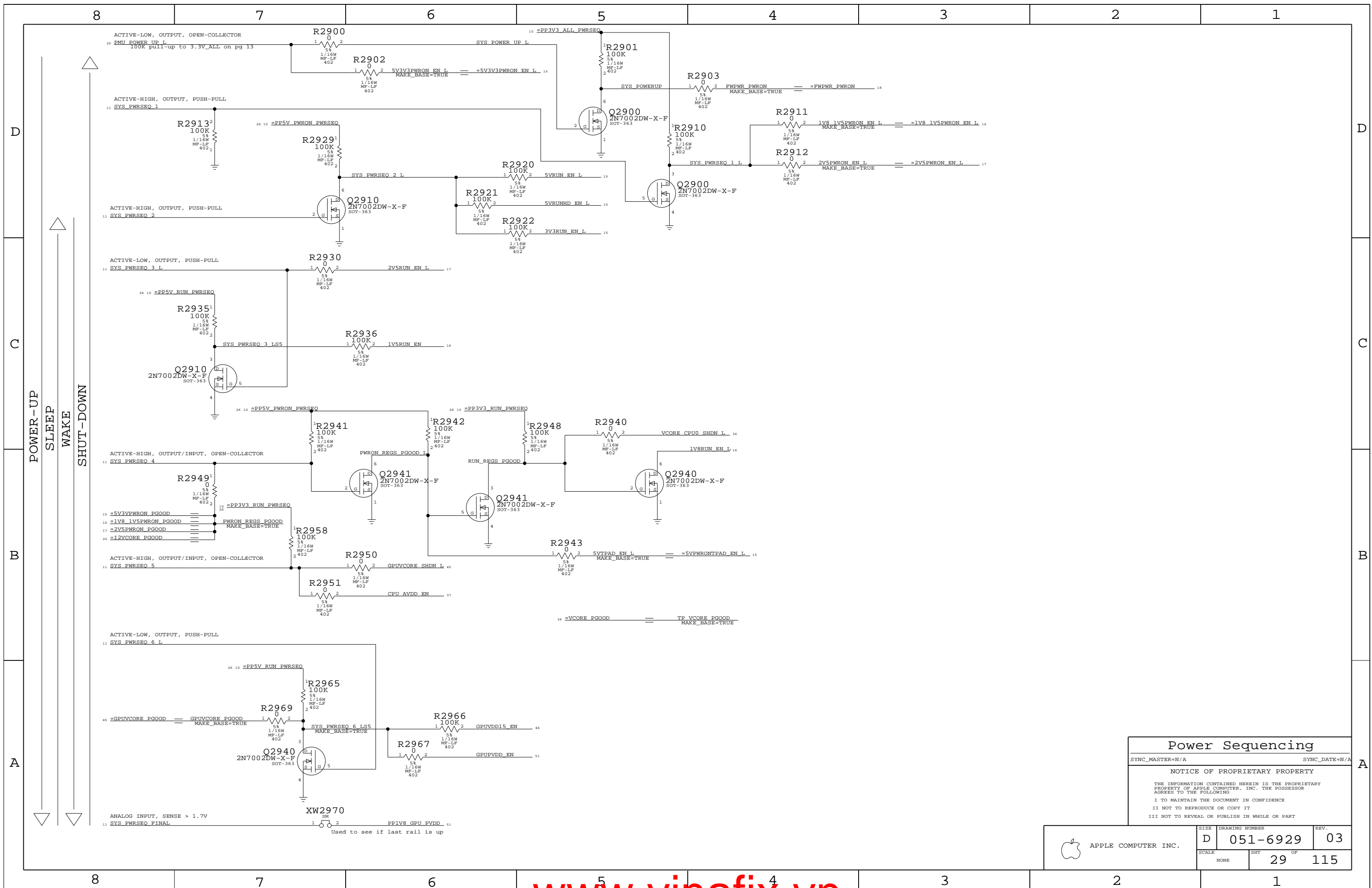
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NONE	D 051-6929	03
	SHEET	OF
	27	115



Power Sequencing

SYNC_MASTER=N/A SYNC_DATE=N/A

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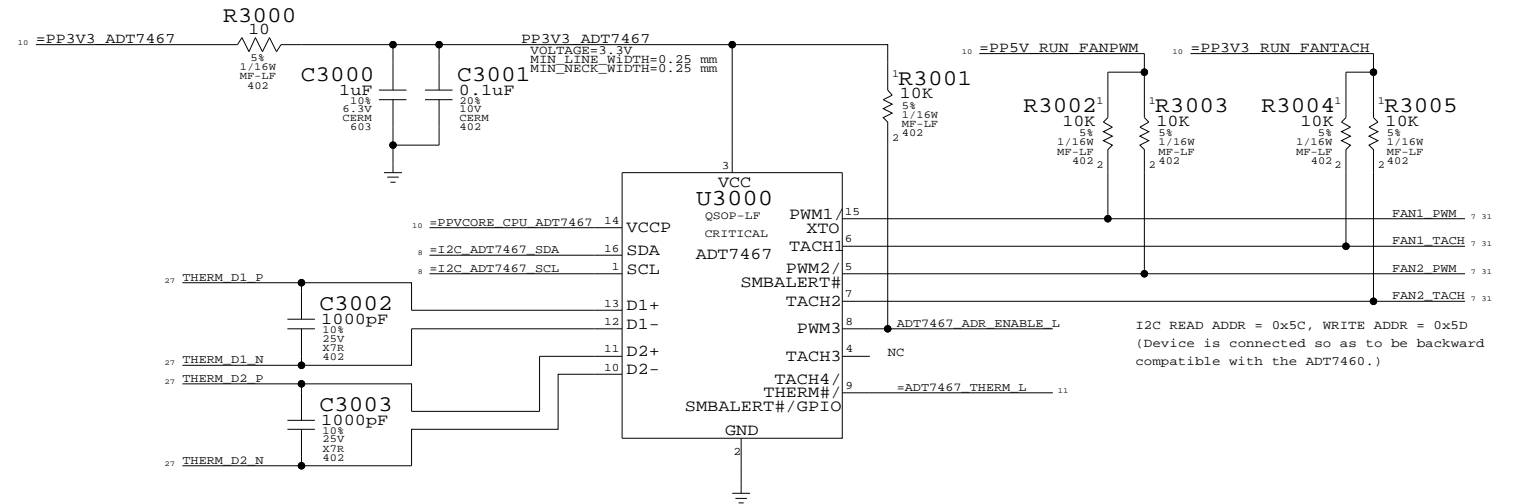
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SCALE	SHT	OF	REV.
NONE	29	115	

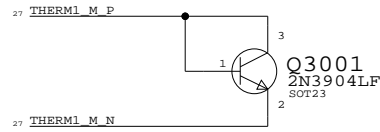
ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
ES2P	THERM	THERM	THERM1_M
ES2N	THERM	THERM	THERM1_M_N
ES3P	THERM	THERM	THERM2_M
ES3N	THERM	THERM	THERM2_M_N
ES3A	THERM	THERM	THERM1_A
ES3N	THERM	THERM	THERM1_A_N
ES3A	THERM	THERM	THERM2_A
ES3N	THERM	THERM	THERM2_A_N
ES3D	THERM	THERM	THERM_D1
ES3N	THERM	THERM	THERM_D1_N
ES3D	THERM	THERM	THERM_D2
ES3N	THERM	THERM	THERM_D2_N

FAN CONTROLLER

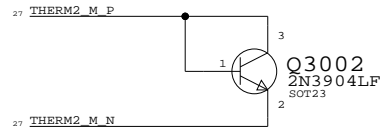


I2C READ ADDR = 0x5C, WRITE ADDR = 0x5D
(Device is connected so as to be backward compatible with the ADT7460.)

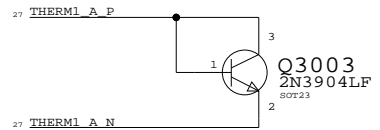
PLACE CLOSE TO CPU MAIN1



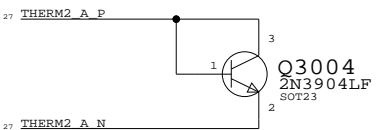
PLACE IN BETWEEN 3/5/1.5/2.5V PWR SUPPLY MAIN2



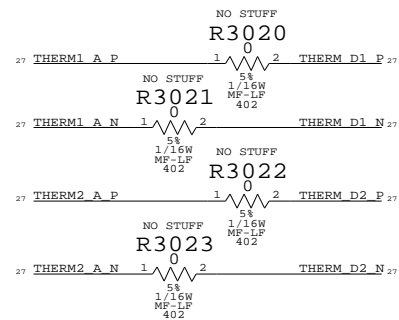
PLACE UNDERNEATH UPPER RAM ALTERNATE1



PLACE CLOSE TO BATTERY CHARGER/VCORE ALTERNATE2



KEEP STUFFING RESISTORS CLOSE TO ADT7467 CONTROLLER



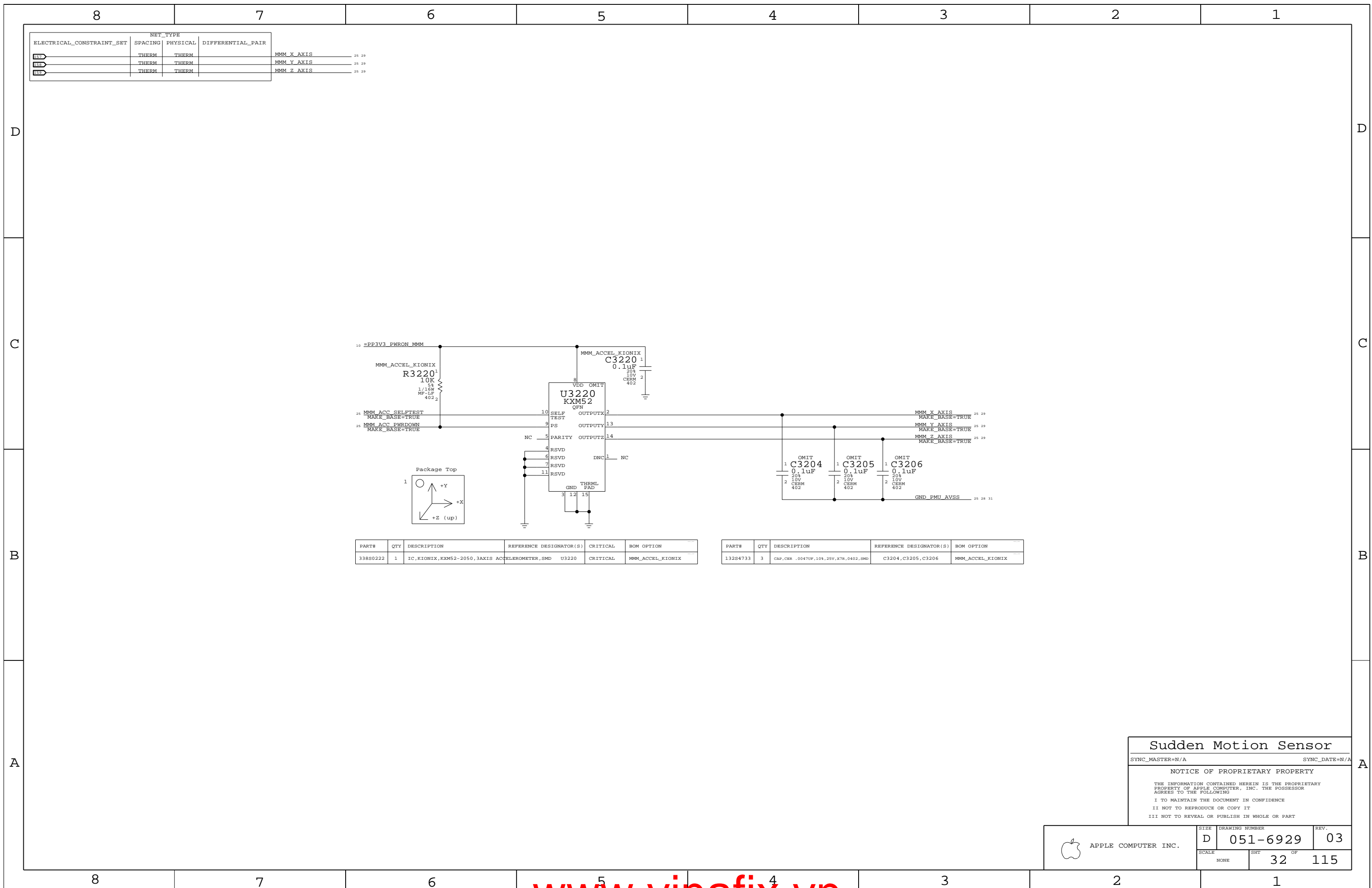
Fan Controller

SYNC_MASTER=N/A SYNC_DATE=N/A

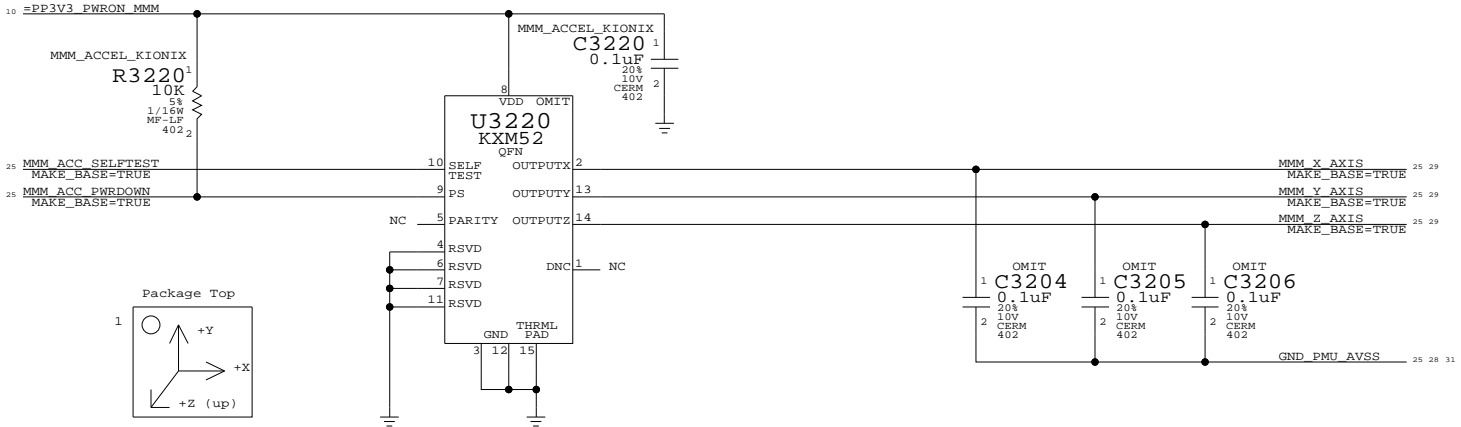
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SCALE	SHT OF		
NONE	30		115



ELECTRICAL_CONSTRAINT_SET	NET_TYPE		DIFFERENTIAL_PAIR
	SPACING	PHYSICAL	
ES7	THERM	THERM	MMM X AXIS
ES8	THERM	THERM	MMM Y AXIS
ES9	THERM	THERM	MMM Z AXIS



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0222	1	IC, KIONIX, KXM52-2050, 3AXIS ACCELEROMETER, SMD	U3220	CRITICAL	MMM_ACCEL_KIONIX

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S4733	3	CAP, CER, .0047UF, 10%, 25V, X7R, 0402, SMD	C3204, C3205, C3206	MMM_ACCEL_KIONIX

Sudden Motion Sensor

SYNC_MASTER=N/A SYNC_DATE=N/A

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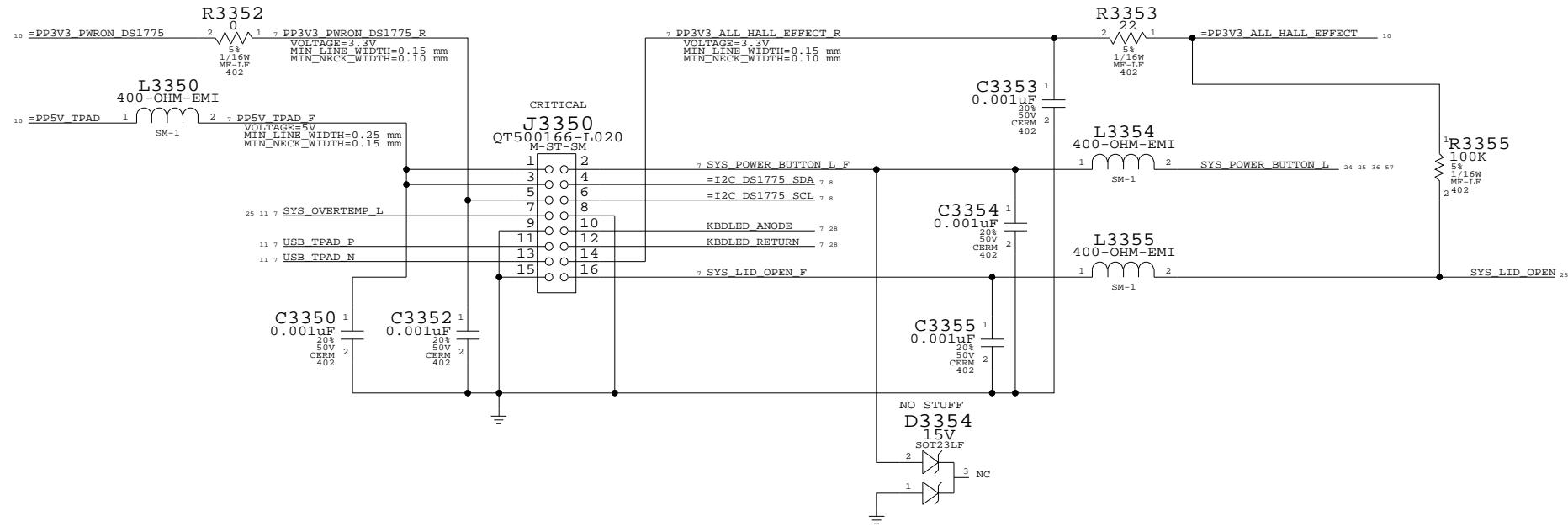
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II NOT TO REPRODUCE OR COPY IT

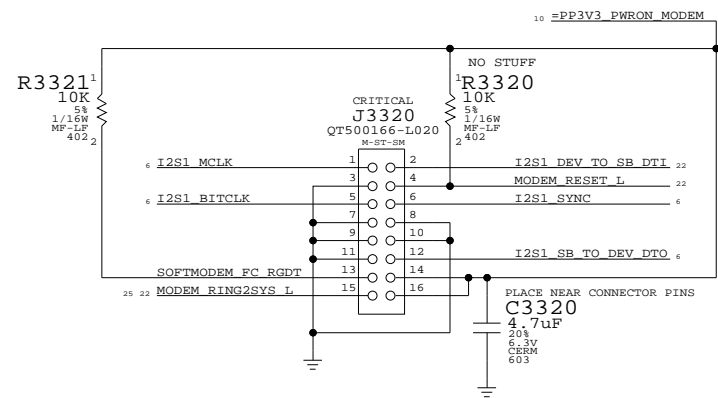
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6929	03
SCALE	SHT OF		
NONE	32 OF		115

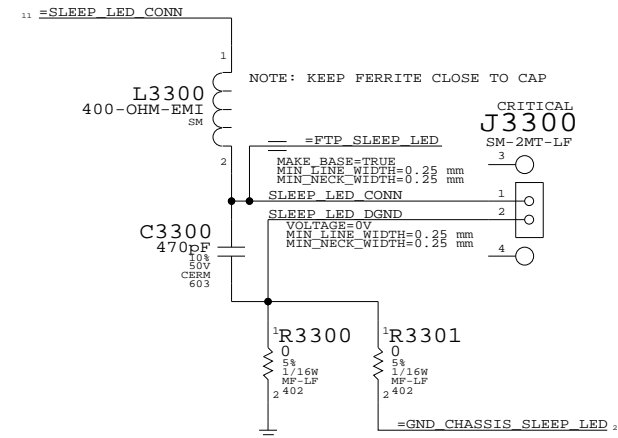
USB Trackpad Connector



SOFT MODEM CONN



SLEEP LED CONNECTOR



Q16C Internal I/O I

SYNC_MASTER=N/A SYNC_DATE=N/A

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	D	051-6929	03
SCALE	SHT	OF	
NONE	33	115	

8

7

6

5

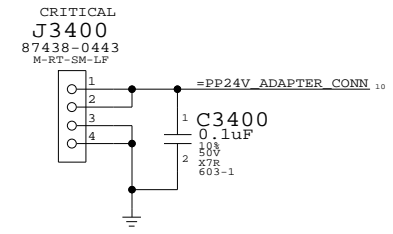
4

3

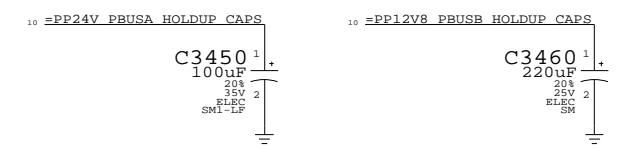
2

1

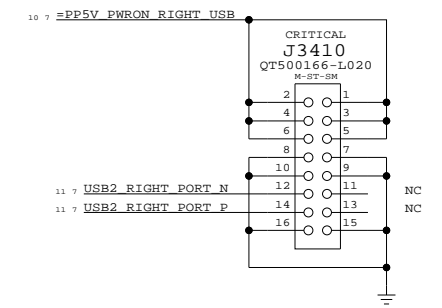
ADAPTER CONNECTOR



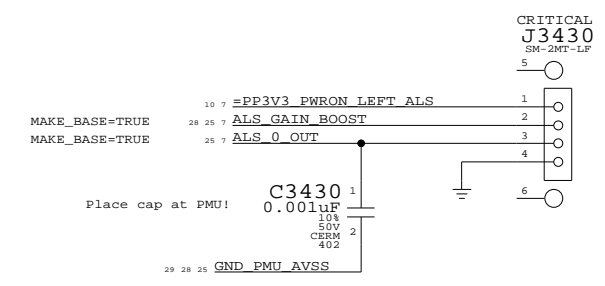
PBUS HOLD-UP CAPS



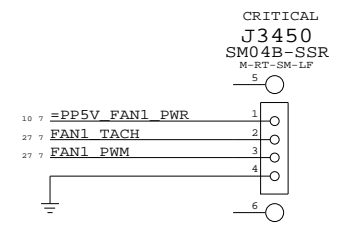
RIGHT USB BOARD



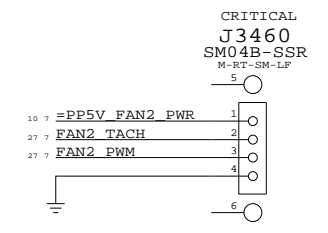
LEFT ALS CONNECTOR



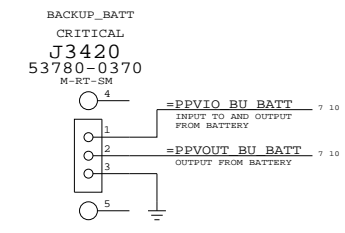
CPU FAN



GPU FAN



BACKUP BATTERY CONNECTOR



Q16C Internal I/O II

SYNC_MASTER=N/A SYNC_DATE=N/A

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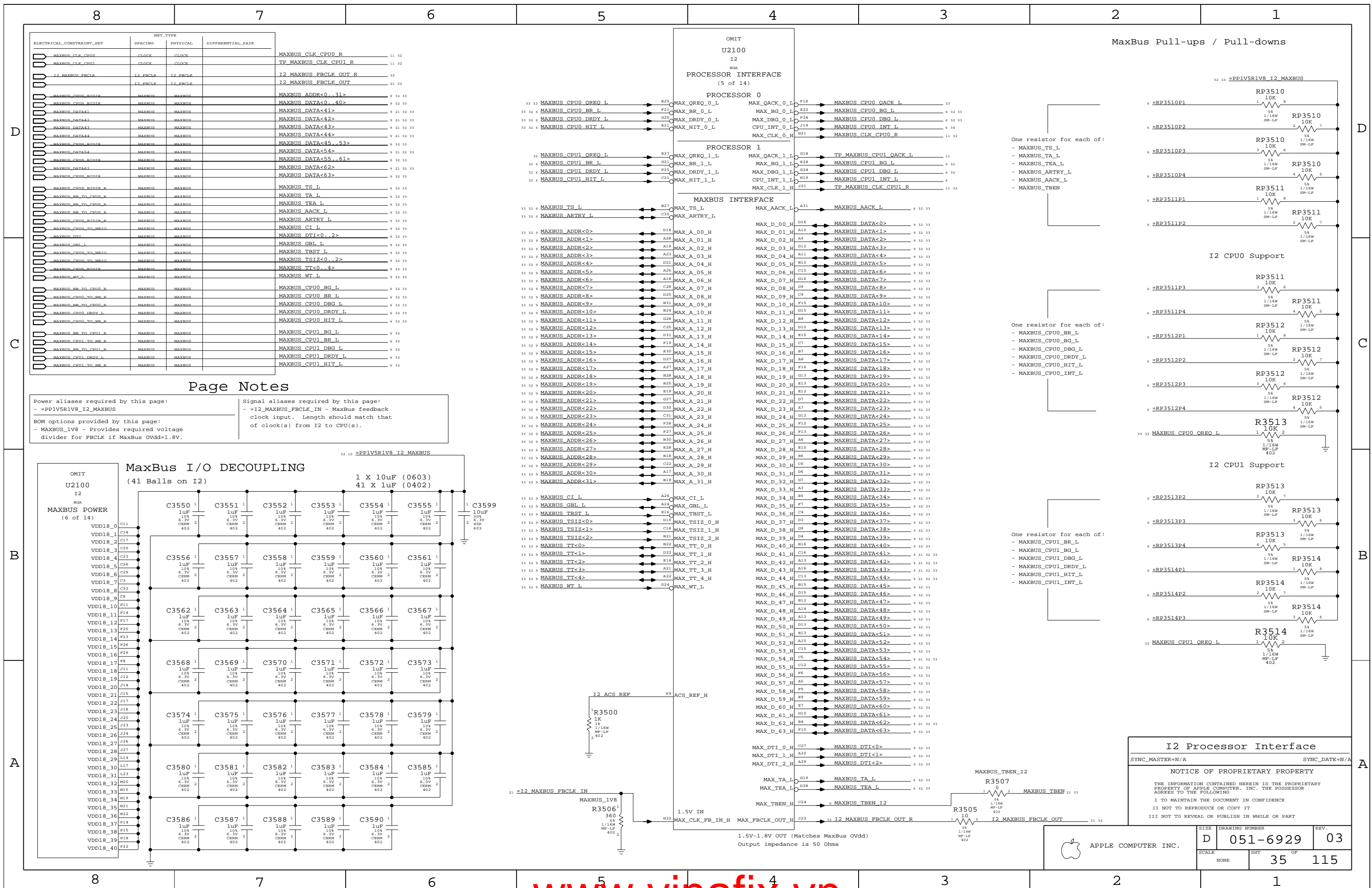
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	NONE	051-6929	03
SCALE		SHT	OF
NONE		34	115



Page Notes

Power aliases required by this page:
 - =PPIV5R1V8_I2_MAXBUS

BOM options provided by this page:
 - MAXBUS_1V8 - Provides required voltage divider for FBCLK if MaxBus Ovdd=1.8V.

Signal aliases required by this page:
 - =I2_MAXBUS_FBCLK_IN - MaxBus feedback clock input. Length should match that of clock(s) from I2 to CPU(s).

MaxBus I/O DECOUPLING

(41 Balls on I2) 1 X 10uF (0603) 41 X 1uF (0402)

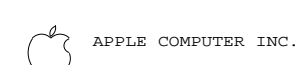
I2 Processor Interface

SYNC_MASTER=N/A SYNC_DATE=N/A

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D	051-6929	03
SCALE	SHT	OF
NONE	35	115



ELECTRICAL_CONSTRAINT_SET	NET_TYPE	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
MAXBUS	CLOCK	CLOCK		

Page Notes

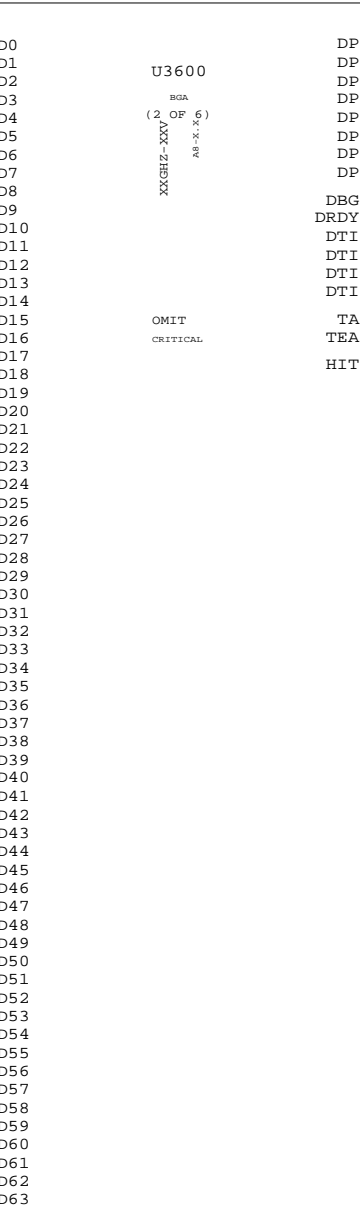
Power aliases required by this page:
 - =PPIV5R1V8_MAXBUS

Signal aliases required by this page:
 - =MAXBUS_CPU0_CLK

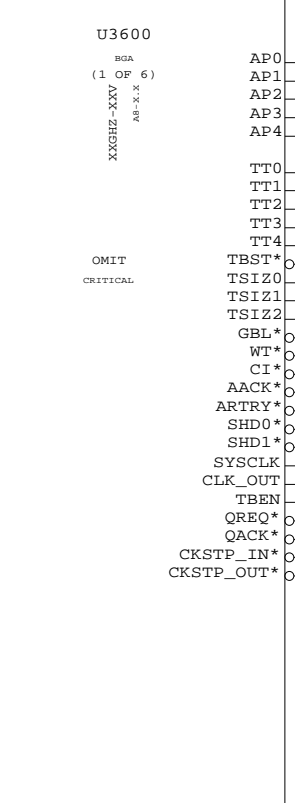
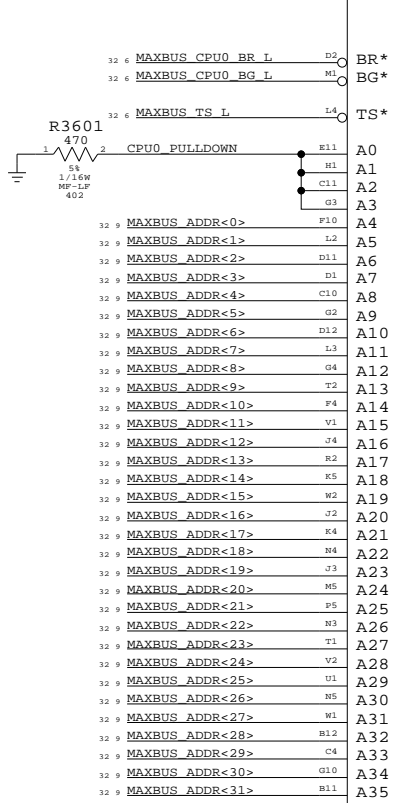
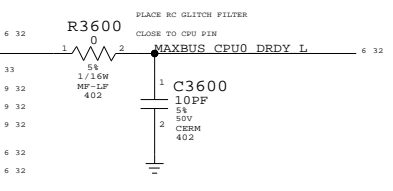
BOM options provided by this page:
 (NONE)

=MAXBUS_CPU0_CLK 11 33

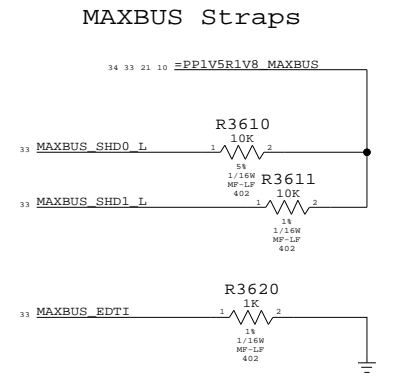
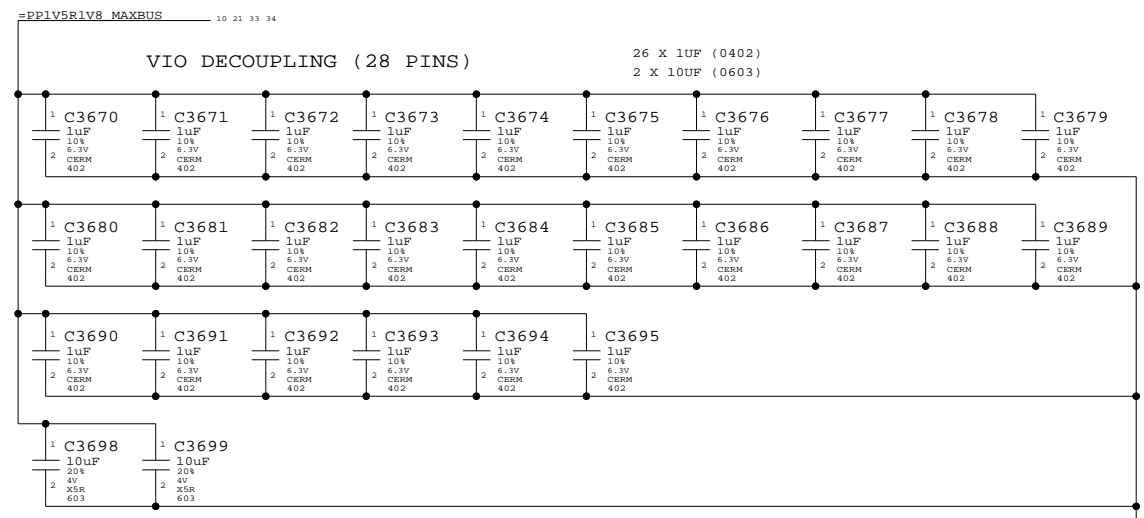
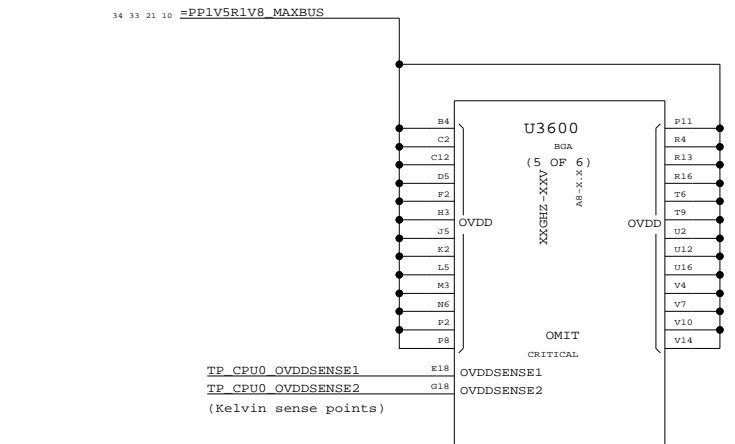
- 32 9 MAXBUS_DATA<0> R15 D0
- 32 9 MAXBUS_DATA<1> M15 D1
- 32 9 MAXBUS_DATA<2> T14 D2
- 32 9 MAXBUS_DATA<3> V16 D3
- 32 9 MAXBUS_DATA<4> W16 D4
- 32 9 MAXBUS_DATA<5> T15 D5
- 32 9 MAXBUS_DATA<6> U15 D6
- 32 9 MAXBUS_DATA<7> P14 D7
- 32 9 MAXBUS_DATA<8> V13 D8
- 32 9 MAXBUS_DATA<9> M13 D9
- 32 9 MAXBUS_DATA<10> T13 D10
- 32 9 MAXBUS_DATA<11> P13 D11
- 32 9 MAXBUS_DATA<12> U14 D12
- 32 9 MAXBUS_DATA<13> M14 D13
- 32 9 MAXBUS_DATA<14> R12 D14
- 32 9 MAXBUS_DATA<15> T12 D15
- 32 9 MAXBUS_DATA<16> M12 D16
- 32 9 MAXBUS_DATA<17> V12 D17
- 32 9 MAXBUS_DATA<18> M11 D18
- 32 9 MAXBUS_DATA<19> M10 D19
- 32 9 MAXBUS_DATA<20> R11 D20
- 32 9 MAXBUS_DATA<21> U11 D21
- 32 9 MAXBUS_DATA<22> M11 D22
- 32 9 MAXBUS_DATA<23> T11 D23
- 32 9 MAXBUS_DATA<24> R10 D24
- 32 9 MAXBUS_DATA<25> M9 D25
- 32 9 MAXBUS_DATA<26> P10 D26
- 32 9 MAXBUS_DATA<27> U10 D27
- 32 9 MAXBUS_DATA<28> R9 D28
- 32 9 MAXBUS_DATA<29> M10 D29
- 32 9 MAXBUS_DATA<30> U9 D30
- 32 9 MAXBUS_DATA<31> V9 D31
- 32 9 MAXBUS_DATA<32> W5 D32
- 32 9 MAXBUS_DATA<33> U6 D33
- 32 9 MAXBUS_DATA<34> T5 D34
- 32 9 MAXBUS_DATA<35> U5 D35
- 32 9 MAXBUS_DATA<36> W7 D36
- 32 9 MAXBUS_DATA<37> R6 D37
- 32 9 MAXBUS_DATA<38> P7 D38
- 32 9 MAXBUS_DATA<39> V6 D39
- 32 9 MAXBUS_DATA<40> P17 D40
- 32 21 MAXBUS_DATA<41> R19 D41
- 32 21 MAXBUS_DATA<42> V18 D42
- 32 21 MAXBUS_DATA<43> R18 D43
- 32 21 MAXBUS_DATA<44> V19 D44
- 32 9 MAXBUS_DATA<45> T19 D45
- 32 9 MAXBUS_DATA<46> U19 D46
- 32 9 MAXBUS_DATA<47> M19 D47
- 32 9 MAXBUS_DATA<48> U18 D48
- 32 9 MAXBUS_DATA<49> M17 D49
- 32 9 MAXBUS_DATA<50> M18 D50
- 32 9 MAXBUS_DATA<51> T18 D51
- 32 9 MAXBUS_DATA<52> T18 D52
- 32 9 MAXBUS_DATA<53> T17 D53
- 32 21 MAXBUS_DATA<54> M3 D54
- 32 9 MAXBUS_DATA<55> V17 D55
- 32 9 MAXBUS_DATA<56> U4 D56
- 32 9 MAXBUS_DATA<57> U8 D57
- 32 9 MAXBUS_DATA<58> U7 D58
- 32 9 MAXBUS_DATA<59> R7 D59
- 32 9 MAXBUS_DATA<60> P6 D60
- 32 9 MAXBUS_DATA<61> R8 D61
- 32 21 MAXBUS_DATA<62> W8 D62
- 32 9 MAXBUS_DATA<63> T8 D63



- DP0 T3 NC
- DP1 W4 NC
- DP2 T4 NC
- DP3 W5 NC
- DP4 M6 NC
- DP5 V3 NC
- DP6 N8 NC
- DP7 W6 NC
- DBG* M2 MAXBUS_CPU0_DBG_L 6 32
- DRDY* R3 MAXBUS_CPU0_DRDY_L_R 6 32
- DTIO G1 MAXBUS_EDTI 33
- DTI1 K1 MAXBUS_DTI<0> 9 32
- DTI2 P1 MAXBUS_DTI<1> 9 32
- DTI3 N1 MAXBUS_DTI<2> 9 32
- TA* K6 MAXBUS_TA_L 6 32
- TEA* L1 MAXBUS_TEA_L 6 32
- HIT* R2 MAXBUS_CPU0_HIT_L 6 32



- AP0 C1 NC
- AP1 E3 NC
- AP2 H6 NC
- AP3 F5 NC
- AP4 G7 NC
- TT0 R5 MAXBUS_TT<0> 9 32
- TT1 E6 MAXBUS_TT<1> 9 32
- TT2 F6 MAXBUS_TT<2> 9 32
- TT3 R9 MAXBUS_TT<3> 9 32
- TT4 C5 MAXBUS_TT<4> 9 32
- TBST* F11 MAXBUS_TBST_L 9 32
- TSIZ0 G6 MAXBUS_TSIZ<0> 9 32
- TSIZ1 F7 MAXBUS_TSIZ<1> 9 32
- TSIZ2 R7 MAXBUS_TSIZ<2> 9 32
- GBL* R2 MAXBUS_GBL_L 9 32
- WT* D3 MAXBUS_WT_L 9 32
- CI* J1 MAXBUS_CI_L 9 32
- AACK* R1 MAXBUS_AACK_L 6 32
- ARTRY* N2 MAXBUS_ARTRY_L 6 32
- SHD0* R4 MAXBUS_SHD0_L 33
- SHD1* H5 MAXBUS_SHD1_L 33
- SYSCLK A10 =MAXBUS_CPU0_CLK 11 33
- CLK_OUT H2 TP_CPU0_CLKOUT ADD GND TO NEAR CLKOUT TP 21 32
- TBEN R1 MAXBUS_TBEN 21 32
- QREQ* P4 MAXBUS_CPU0_QREQ_L 32
- QACK* G5 MAXBUS_CPU0_QACK_L 32
- CKSTP_IN* A3 33
- CKSTP_OUT* B1 CPU_CHKSTP_OUT_L 34



A8 MaxBus (CPU0)

SYNC_MASTER=MULLET SYNC_DATE=05/25/2005

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NONE	36	115	

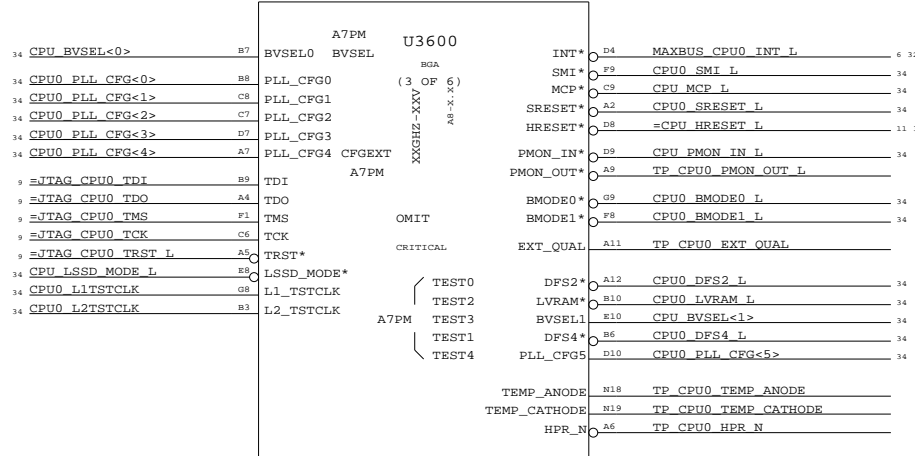
Page Notes

Power aliases required by this page:

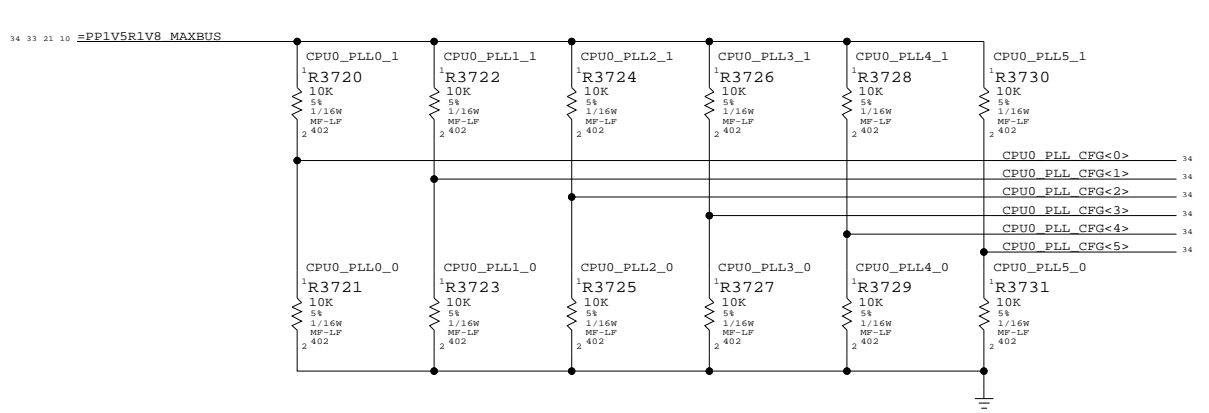
- =PPIV5R1V8_MAXBUS
- =PP3V3_PWRON_PLLSSEL
- =CPU0_JTAG_TDI
- =CPU0_JTAG_TDO
- =CPU0_JTAG_TMS
- =CPU0_JTAG_TCK
- =CPU0_JTAG_TRST_L
- =CPU_HRESET_L (Reset given to all processors)

BOM options provided by this page:

- CPU0_PLL0_0/1
- CPU0_PLL1_0/1
- CPU0_PLL2_0/1
- CPU0_PLL3_0/1
- CPU0_PLL4_0/1
- CPU0_PLL5_0/1
- These must be selected to set the CPU core to Maxbus frequency ratio to attain the desired spec
- MAXBUS_1V5 - MAXBUS_1V8
- One of these must be selected to set the Maxbus voltage
- * the MAXBUS_1V5 option does not exist for A7PM
- CPU_A7PM - CPU_A8
- One of these must be selected to ensure the the above strap is interpreted correctly

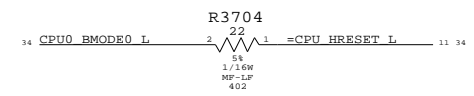


CPU0 PLL CONFIG CIRCUITRY

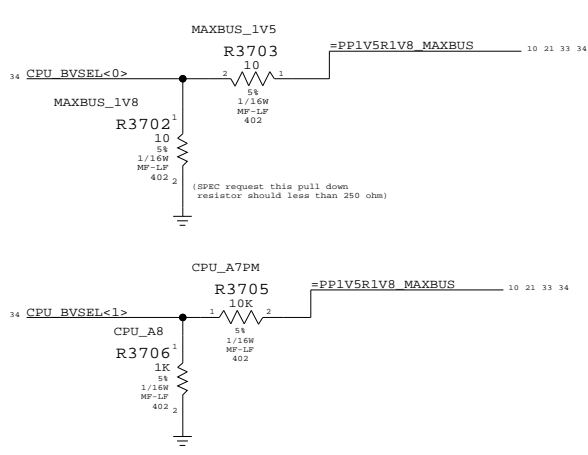


BUS TYPE SELECT

SIGNAL	TIED	MODE
CPU0_BMODE0_L (PROCESSOR)	HIGH	60X BUS MODE
	CPU_HRESET_L	MAX BUS MODE



MAXBUS VSEL

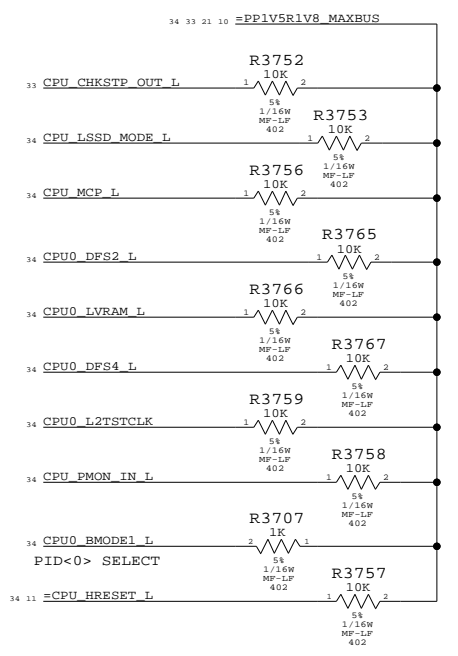


CPU0 FREQUENCY CONFIGURATION

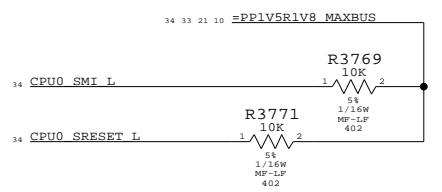
() Indicates DFS setting supported by A8 only

BOM GROUP	DFS SUPPORT	PLL BITS	BOM OPTIONS
CPU0_BUSRATIO_1.0X	-	012345	CPU0_PLL0_0, CPU0_PLL1_0, CPU0_PLL2_1, CPU0_PLL3_1, CPU0_PLL4_0, CPU0_PLL5_0
CPU0_BUSRATIO_2.0X	-	010000	CPU0_PLL0_0, CPU0_PLL1_1, CPU0_PLL2_0, CPU0_PLL3_0, CPU0_PLL4_0, CPU0_PLL5_0
CPU0_BUSRATIO_3.0X	-	100000	CPU0_PLL0_1, CPU0_PLL1_0, CPU0_PLL2_0, CPU0_PLL3_0, CPU0_PLL4_0, CPU0_PLL5_0
CPU0_BUSRATIO_4.0X	2.0X	101000	CPU0_PLL0_1, CPU0_PLL1_0, CPU0_PLL2_1, CPU0_PLL3_0, CPU0_PLL4_0, CPU0_PLL5_0
CPU0_BUSRATIO_5.0X	2.5X	101100	CPU0_PLL0_1, CPU0_PLL1_0, CPU0_PLL2_1, CPU0_PLL3_1, CPU0_PLL4_0, CPU0_PLL5_0
CPU0_BUSRATIO_5.5X	(2.75X)	-	CPU0_PLL0_1, CPU0_PLL1_0, CPU0_PLL2_0, CPU0_PLL3_1, CPU0_PLL4_0, CPU0_PLL5_0
CPU0_BUSRATIO_6.0X	3.0X	110100	CPU0_PLL0_1, CPU0_PLL1_1, CPU0_PLL2_0, CPU0_PLL3_0, CPU0_PLL4_0, CPU0_PLL5_0
CPU0_BUSRATIO_6.5X	(3.25X)	-	CPU0_PLL0_0, CPU0_PLL1_1, CPU0_PLL2_0, CPU0_PLL3_1, CPU0_PLL4_0, CPU0_PLL5_0
CPU0_BUSRATIO_7.0X	3.5X	001000	CPU0_PLL0_0, CPU0_PLL1_0, CPU0_PLL2_1, CPU0_PLL3_0, CPU0_PLL4_0, CPU0_PLL5_0
CPU0_BUSRATIO_7.5X	(3.75X)	-	CPU0_PLL0_0, CPU0_PLL1_0, CPU0_PLL2_0, CPU0_PLL3_1, CPU0_PLL4_0, CPU0_PLL5_0
CPU0_BUSRATIO_8.0X	4.0X	2.0X	110000
CPU0_BUSRATIO_8.5X	(4.25X)	-	011000
CPU0_BUSRATIO_9.0X	4.5X	(2.25X)	011110
CPU0_BUSRATIO_9.5X	(4.75X)	-	011100
CPU0_BUSRATIO_10.0X	5.0X	2.5X	101010
CPU0_BUSRATIO_10.5X	(5.25X)	-	100010
CPU0_BUSRATIO_11.0X	5.5X	(2.75X)	100110
CPU0_BUSRATIO_11.5X	(5.75X)	-	000000
CPU0_BUSRATIO_12.0X	6.0X	3.0X	101110
CPU0_BUSRATIO_12.5X	(6.25X)	-	111110
CPU0_BUSRATIO_13.0X	6.5X	(3.25X)	010110
CPU0_BUSRATIO_13.5X	(6.75X)	-	111000
CPU0_BUSRATIO_14.0X	7.0X	3.5X	110010
CPU0_BUSRATIO_15.0X	7.5X	(3.75X)	000110
CPU0_BUSRATIO_16.0X	8.0X	4.0X	110110
CPU0_BUSRATIO_17.0X	8.5X	(4.25X)	000010
CPU0_BUSRATIO_18.0X	9.0X	4.5X	001010
CPU0_BUSRATIO_20.0X	10.0X	5.0X	001110
CPU0_BUSRATIO_21.0X	10.5X	(5.25X)	010010
CPU0_BUSRATIO_24.0X	12.0X	6.0X	011010
CPU0_BUSRATIO_28.0X	14.0X	7.0X	111010

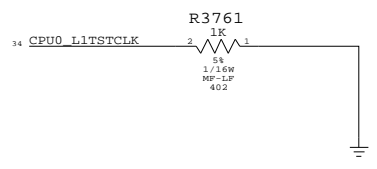
CPU PULLUPS



INTERRUPT PULL-UPS



CPU PULLDOWNS



A8 Configuration Straps

SYNC_MASTER=MULLET SYNC_DATE=05/25/2005

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SCALE	SHT	OF	
NONE	37	115	

Page Notes

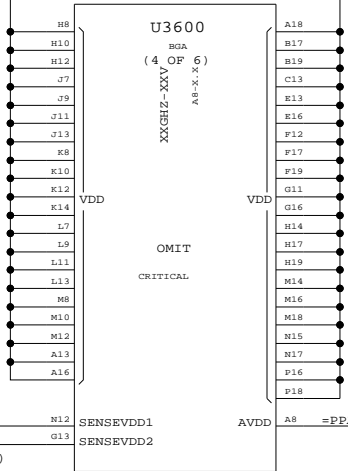
Power aliases required by this page:
 - =PPVCORE_CPU0

Signal aliases required by this page:
 (NONE)

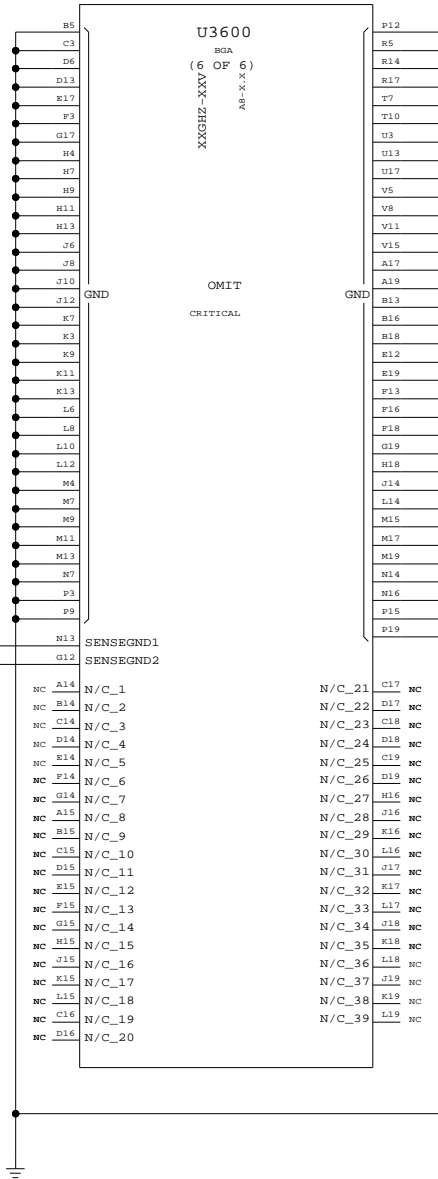
BOM options provided by this page:
 (NONE)

35 10 =PPVCORE_CPU0

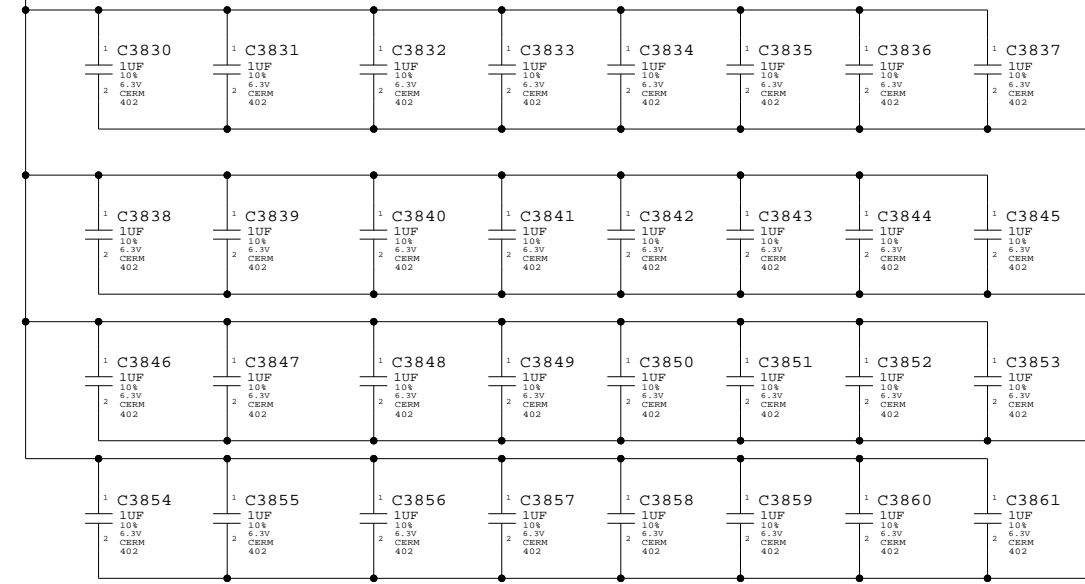
TP_CPU0_SENSEVDD1
 TP_CPU0_SENSEVDD2
 (Kelvin sense points)



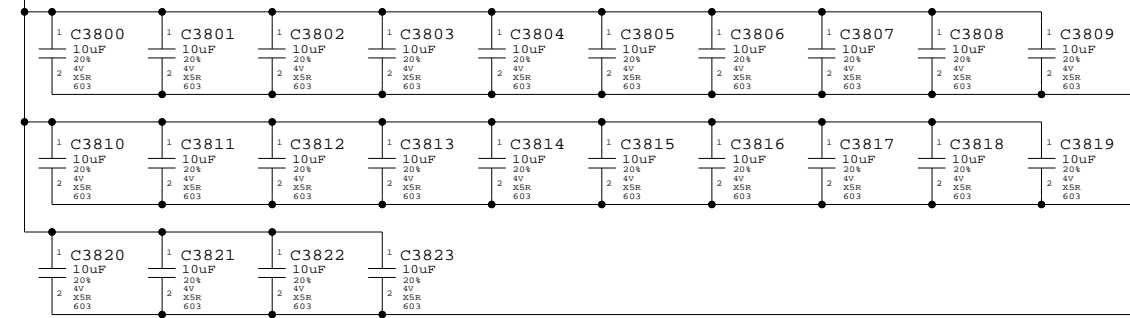
TP_CPU0_SENSEGND1
 TP_CPU0_SENSEGND2
 (Kelvin sense points)



VCORE BULK CAPS
 40 X 1 UF (0402)



24 X 10 UF (0603)



A8 Power (CPU0)

SYNC_MASTER=MULLET SYNC_DATE=05/25/2005

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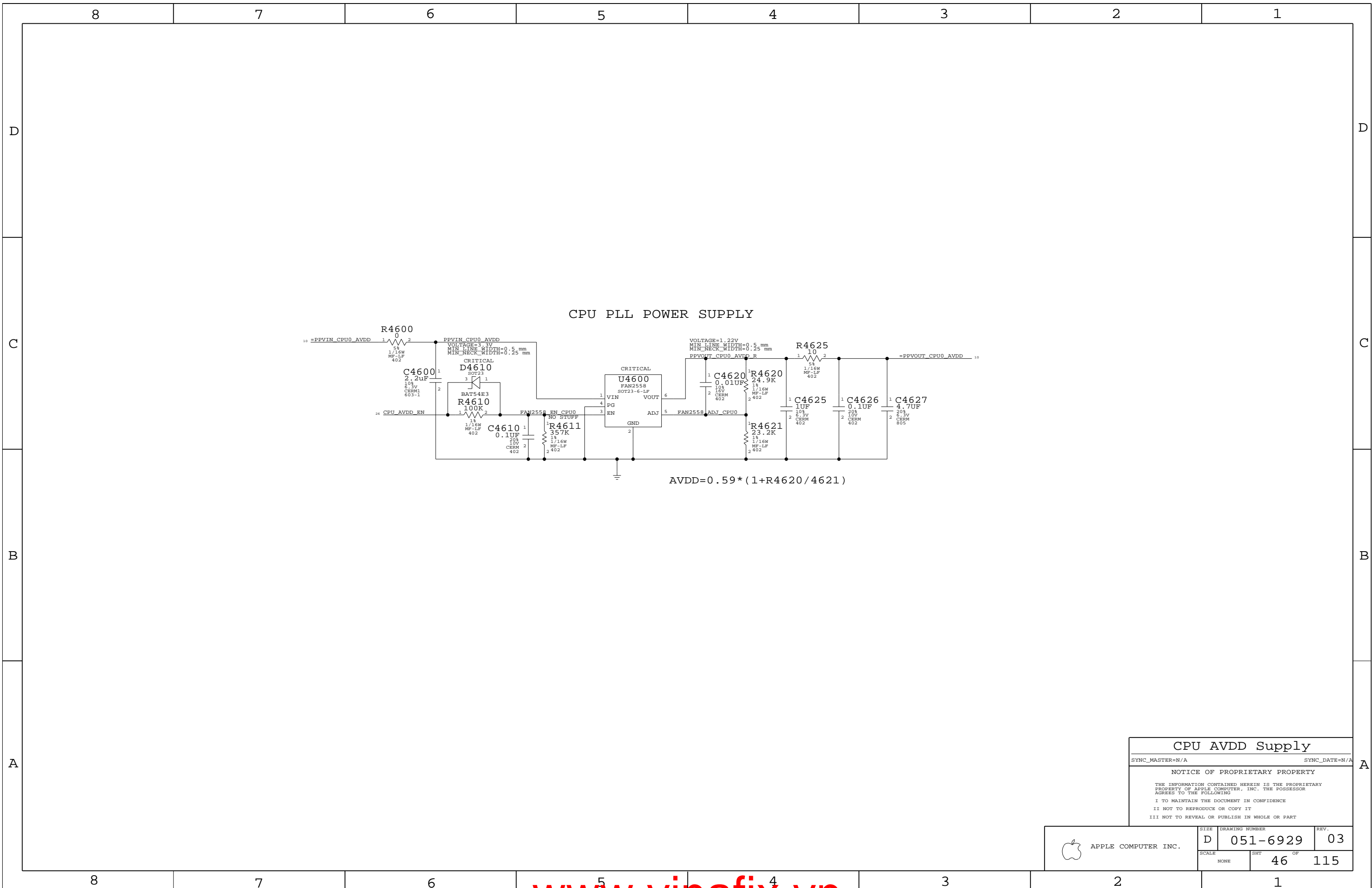
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SCALE	NONE	SHT	OF
		38	115



CPU AVDD Supply

SYNC_MASTER=N/A SYNC_DATE=N/A

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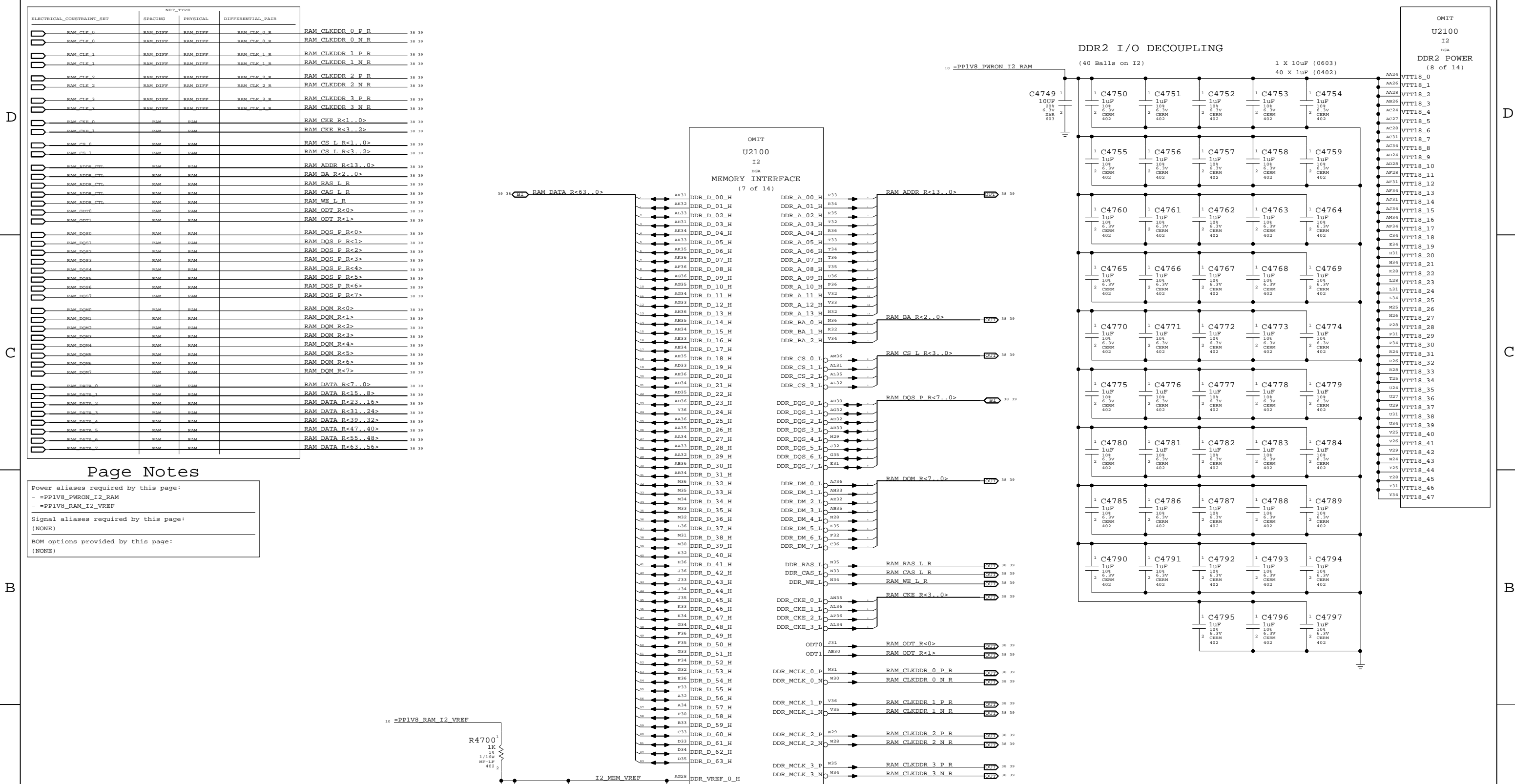
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SCALE		SHT	OF
NONE		46	115



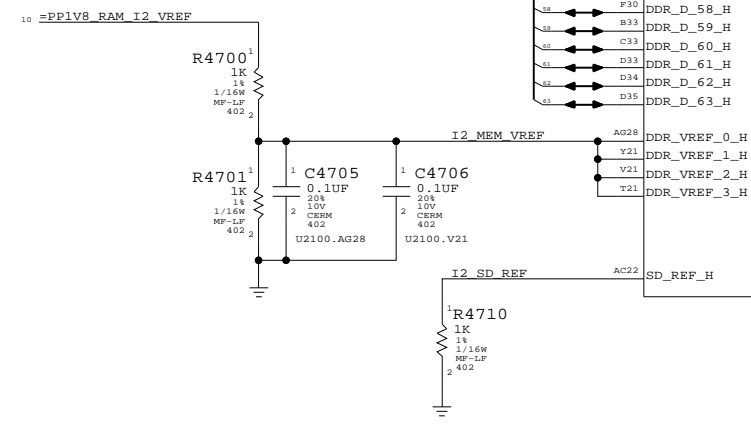
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	NET_TYPE	
				RAM_CLK_0	RAM_CLKDDR_0_P_R
				RAM_CLK_0	RAM_CLKDDR_0_N_R
				RAM_CLK_1	RAM_CLKDDR_1_P_R
				RAM_CLK_1	RAM_CLKDDR_1_N_R
				RAM_CLK_2	RAM_CLKDDR_2_P_R
				RAM_CLK_2	RAM_CLKDDR_2_N_R
				RAM_CLK_3	RAM_CLKDDR_3_P_R
				RAM_CLK_3	RAM_CLKDDR_3_N_R
				RAM_CKE_0	RAM_CKE_R<1..0>
				RAM_CKE_1	RAM_CKE_R<3..2>
				RAM_CS_0	RAM_CS_L_R<1..0>
				RAM_CS_1	RAM_CS_L_R<3..2>
				RAM_ADDR_CTT0	RAM_ADDR_R<13..0>
				RAM_ADDR_CTT1	RAM_BA_R<2..0>
				RAM_ADDR_CTT2	RAM_RAS_L_R
				RAM_ADDR_CTT3	RAM_CAS_L_R
				RAM_ADDR_CTT4	RAM_WE_L_R
				RAM_ODT0	RAM_ODT_R<0>
				RAM_ODT1	RAM_ODT_R<1>
				RAM_DQS0	RAM_DQS_P_R<0>
				RAM_DQS1	RAM_DQS_P_R<1>
				RAM_DQS2	RAM_DQS_P_R<2>
				RAM_DQS3	RAM_DQS_P_R<3>
				RAM_DQS4	RAM_DQS_P_R<4>
				RAM_DQS5	RAM_DQS_P_R<5>
				RAM_DQS6	RAM_DQS_P_R<6>
				RAM_DQS7	RAM_DQS_P_R<7>
				RAM_DM0	RAM_DM_R<0>
				RAM_DM1	RAM_DM_R<1>
				RAM_DM2	RAM_DM_R<2>
				RAM_DM3	RAM_DM_R<3>
				RAM_DM4	RAM_DM_R<4>
				RAM_DM5	RAM_DM_R<5>
				RAM_DM6	RAM_DM_R<6>
				RAM_DM7	RAM_DM_R<7>
				RAM_DATA_0	RAM_DATA_R<7..0>
				RAM_DATA_1	RAM_DATA_R<15..8>
				RAM_DATA_2	RAM_DATA_R<23..16>
				RAM_DATA_3	RAM_DATA_R<31..24>
				RAM_DATA_4	RAM_DATA_R<39..32>
				RAM_DATA_5	RAM_DATA_R<47..40>
				RAM_DATA_6	RAM_DATA_R<55..48>
				RAM_DATA_7	RAM_DATA_R<63..56>

Page Notes

Power aliases required by this page:
 - =PP1V8_PWRON_I2_RAM
 - =PP1V8_RAM_I2_VREF

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)



I2 Memory Interface

SYNC_MASTER=N/A SYNC_DATE=N/A

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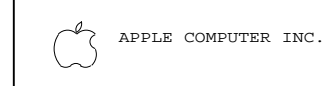
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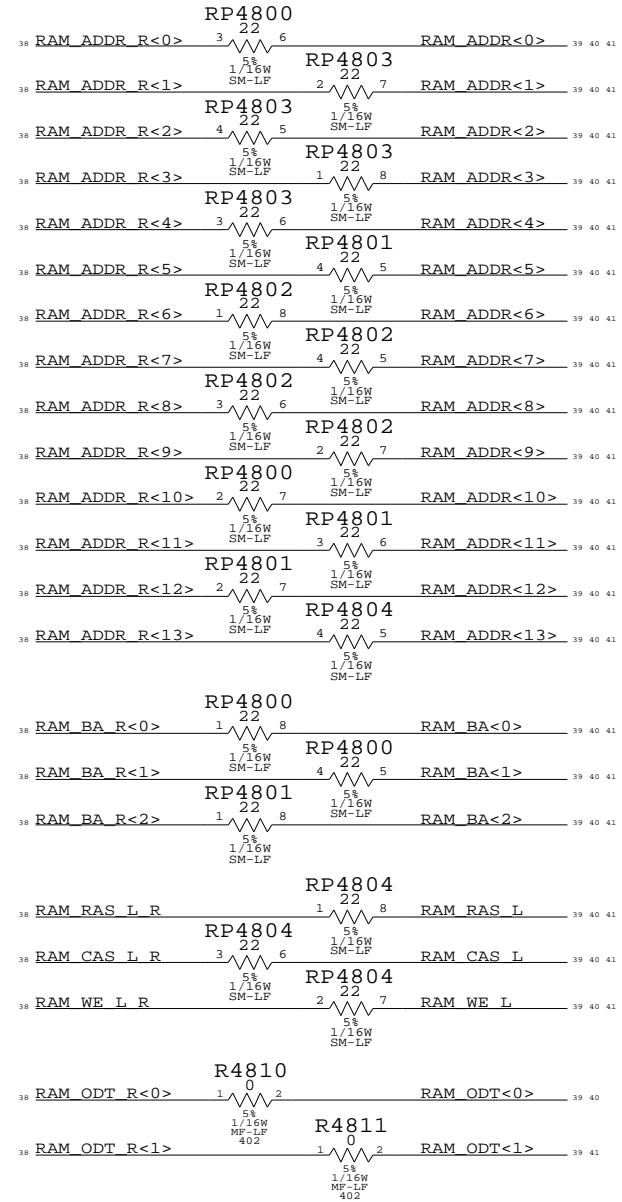
SIZE	DRAWING NUMBER	REV.
D	051-6929	03
SCALE	SHT	OF
NONE	47	115



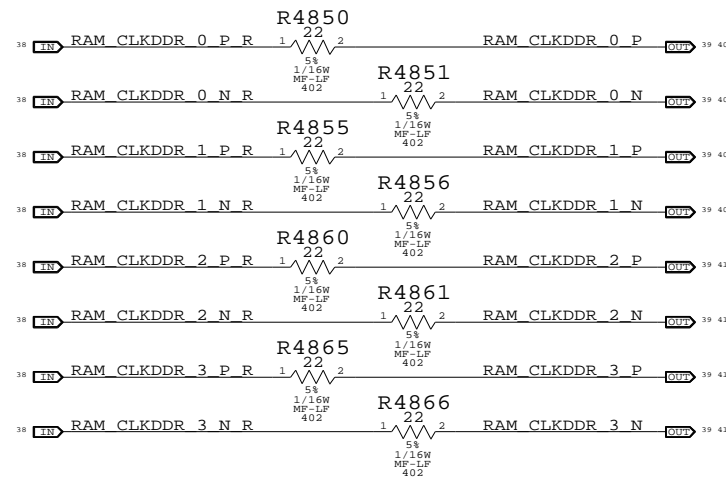
Main Memory Series Termination

SERIES RESISTORS FOR CONTROL SIGNALS

PINS ARE SWAPPABLE FOR RPAKS RP4800-RP4804

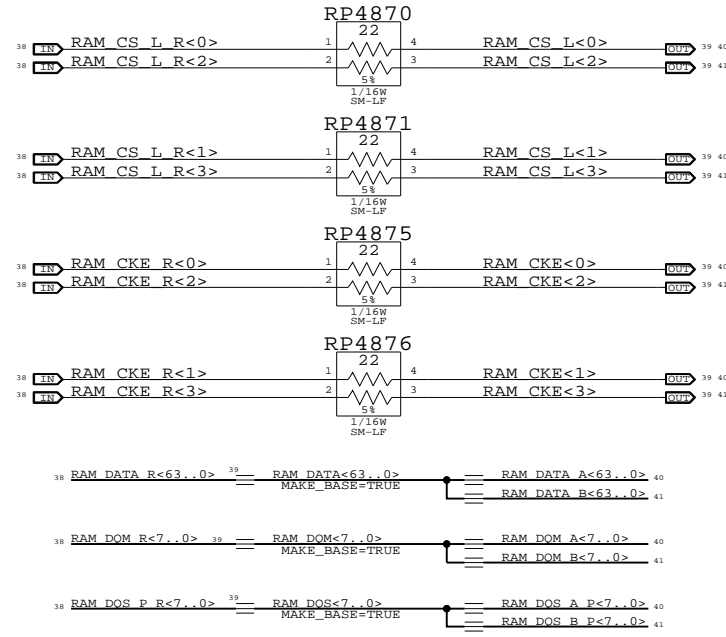


SERIES RESISTORS FOR CLOCKS

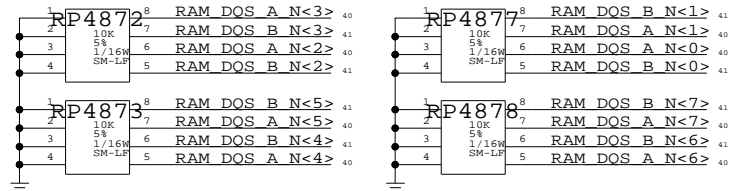


SERIES RESISTORS FOR CS / CKE

Do not swap with other RPAKs



ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
DIFF	RAM_DIFF	RAM_DIFF	RAM_CLK_0	RAM_CLKDDR 0 P 39 40
DIFF	RAM_DIFF	RAM_DIFF	RAM_CLK_0	RAM_CLKDDR 0 N 39 40
DIFF	RAM_DIFF	RAM_DIFF	RAM_CLK_1	RAM_CLKDDR 1 P 39 40
DIFF	RAM_DIFF	RAM_DIFF	RAM_CLK_1	RAM_CLKDDR 1 N 39 40
DIFF	RAM_DIFF	RAM_DIFF	RAM_CLK_2	RAM_CLKDDR 2 P 39 41
DIFF	RAM_DIFF	RAM_DIFF	RAM_CLK_2	RAM_CLKDDR 2 N 39 41
DIFF	RAM_DIFF	RAM_DIFF	RAM_CLK_3	RAM_CLKDDR 3 P 39 41
DIFF	RAM_DIFF	RAM_DIFF	RAM_CLK_3	RAM_CLKDDR 3 N 39 41
DIFF	RAM	RAM	RAM_CKE<3..0>	39 40 41
DIFF	RAM	RAM	RAM_CS L<3..0>	39 40 41
DIFF	RAM	RAM	RAM_ADDR<13..0>	39 40 41
DIFF	RAM	RAM	RAM_BA<2..0>	39 40 41
DIFF	RAM	RAM	RAM_RAS L	39 40 41
DIFF	RAM	RAM	RAM_CAS L	39 40 41
DIFF	RAM	RAM	RAM_WE L	39 40 41
DIFF	RAM	RAM	RAM_ODT<1..0>	39 40 41
DIFF	RAM	RAM	RAM_DOS<7..0>	39
DIFF	RAM	RAM	RAM_DOM<7..0>	39
DIFF	RAM	RAM	RAM_DATA<63..0>	39



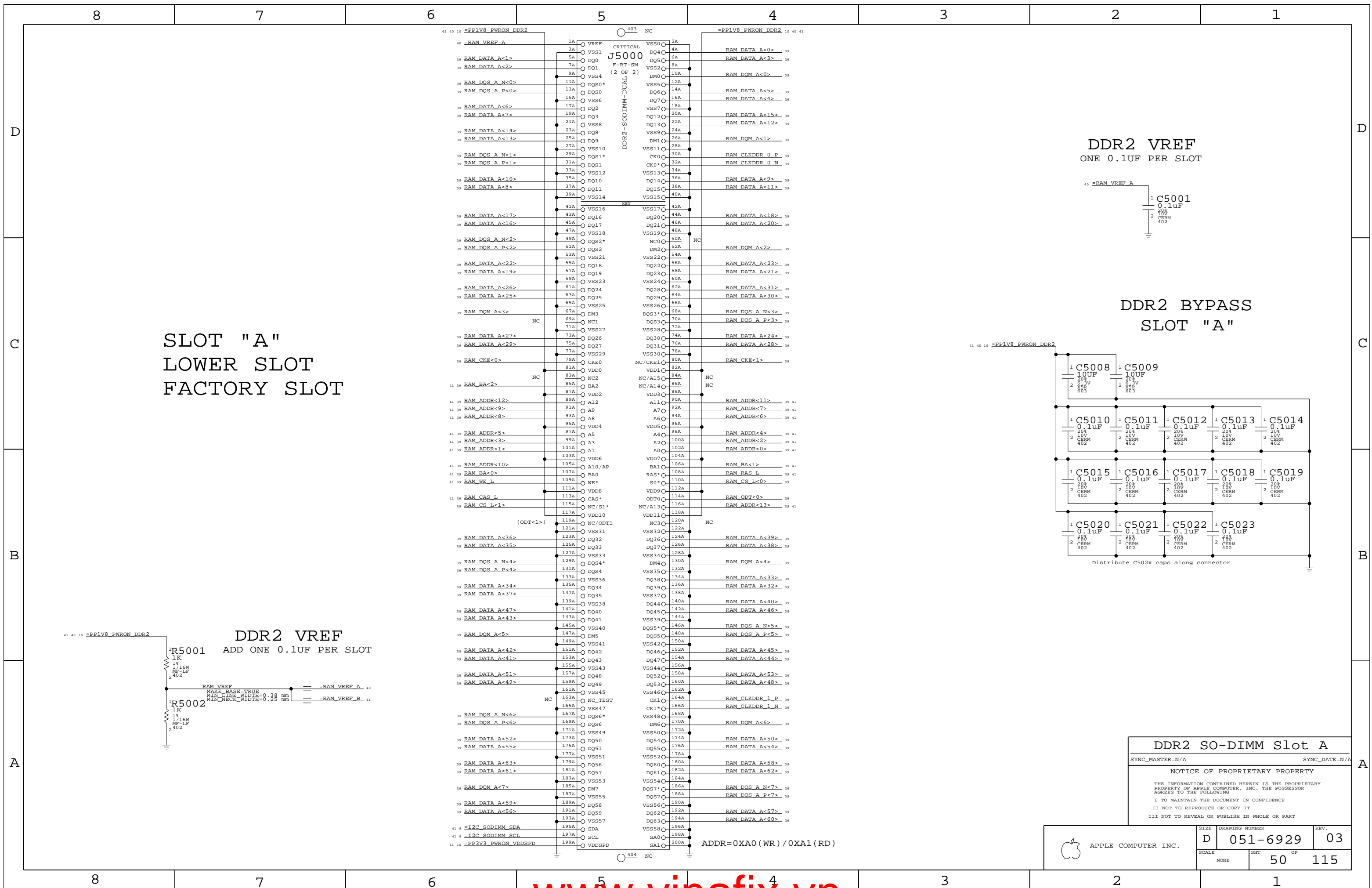
Memory Series Termination

SYNC_MASTER=N/A SYNC_DATE=N/A

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SCALE	NONE	SHT	OF
		48	115



SLOT "A"
LOWER SLOT
FACTORY SLOT

DDR2 VREF
ONE 0.1UF PER SLOT

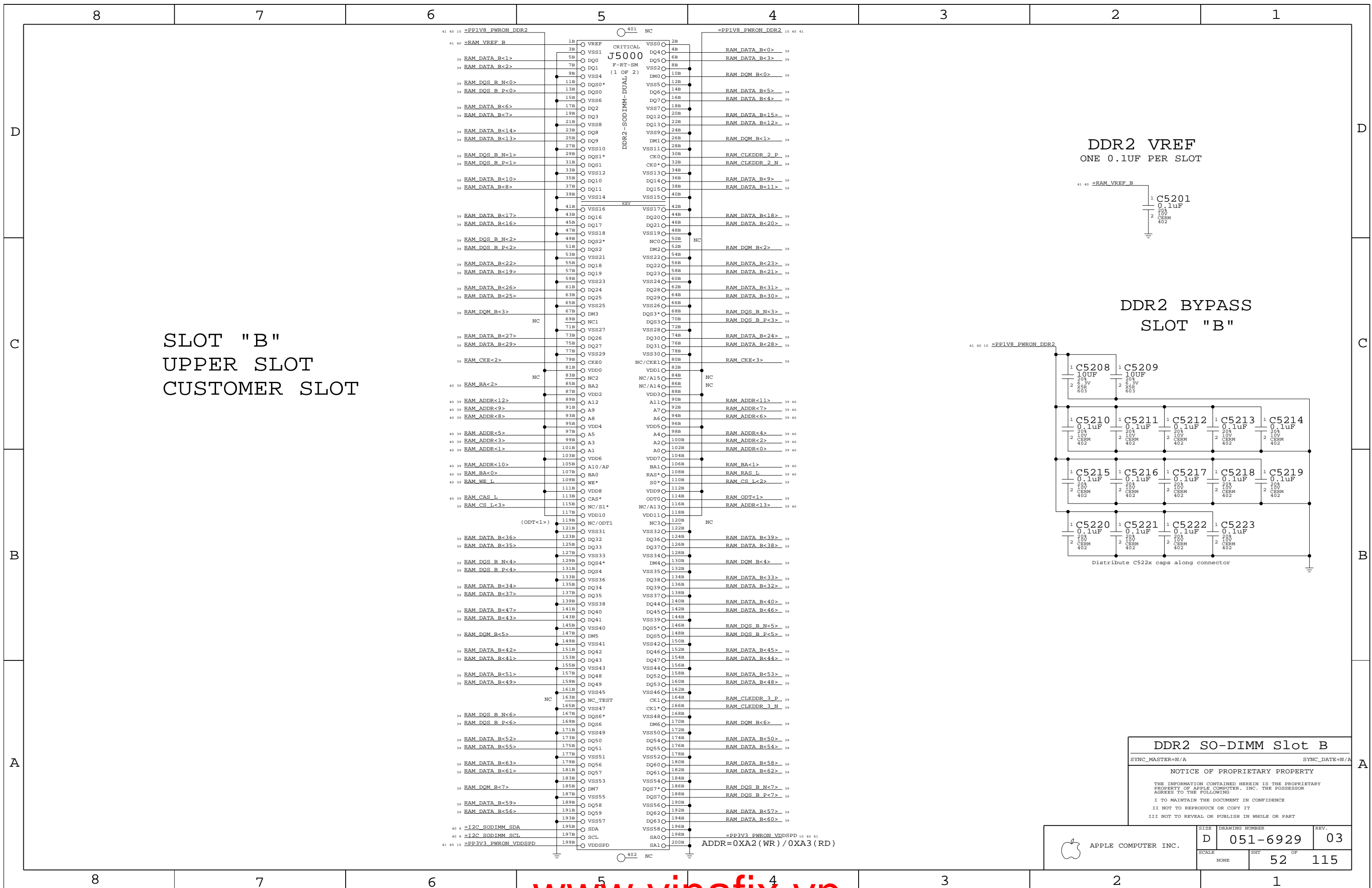
DDR2 BYPASS
SLOT "A"

DDR2 VREF
ADD ONE 0.1UF PER SLOT

Pin	Signal	Pin	Signal
41	=PP1V8_PWRON_DDR2	403	NC
40	=RAM VREF_A	1A	VREF
39	RAM_DATA_A<1>	3A	VSS1
38	RAM_DATA_A<2>	5A	DQ0
37	RAM_DATA_A<3>	7A	DQ1
36	RAM_DATA_A<4>	9A	VSS4
35	RAM_DATA_A<5>	11A	DQ0*
34	RAM_DATA_A<6>	13A	DQ0
33	RAM_DATA_A<7>	15A	VSS6
32	RAM_DATA_A<8>	17A	DQ2
31	RAM_DATA_A<9>	19A	DQ3
30	RAM_DATA_A<10>	21A	VSS8
29	RAM_DATA_A<11>	23A	DQ8
28	RAM_DATA_A<12>	25A	DQ9
27	RAM_DATA_A<13>	27A	VSS10
26	RAM_DATA_A<14>	29A	DQS1*
25	RAM_DATA_A<15>	31A	DQS1
24	RAM_DATA_A<16>	33A	VSS12
23	RAM_DATA_A<17>	35A	DQ10
22	RAM_DATA_A<18>	37A	DQ11
21	RAM_DATA_A<19>	39A	VSS14
20	RAM_DATA_A<20>	41A	VSS16
19	RAM_DATA_A<21>	43A	DQ16
18	RAM_DATA_A<22>	45A	DQ17
17	RAM_DATA_A<23>	47A	VSS18
16	RAM_DATA_A<24>	49A	DQS2*
15	RAM_DATA_A<25>	51A	DQS2
14	RAM_DATA_A<26>	53A	VSS21
13	RAM_DATA_A<27>	55A	DQ18
12	RAM_DATA_A<28>	57A	DQ19
11	RAM_DATA_A<29>	59A	VSS23
10	RAM_DATA_A<30>	61A	DQ24
9	RAM_DATA_A<31>	63A	DQ25
8	RAM_DATA_A<32>	65A	VSS25
7	RAM_DATA_A<33>	67A	DM3
6	RAM_DATA_A<34>	69A	NC1
5	RAM_DATA_A<35>	71A	VSS27
4	RAM_DATA_A<36>	73A	DQ26
3	RAM_DATA_A<37>	75A	DQ27
2	RAM_DATA_A<38>	77A	VSS29
1	RAM_DATA_A<39>	79A	CKE0
41	RAM_BA<2>	81A	VDD0
40	RAM_ADDR<12>	83A	NC2
39	RAM_ADDR<9>	85A	BA2
38	RAM_ADDR<8>	87A	VDD2
37	RAM_ADDR<5>	89A	A12
36	RAM_ADDR<3>	91A	A9
35	RAM_ADDR<1>	93A	A8
34	RAM_ADDR<10>	95A	VDD4
33	RAM_ADDR<0>	97A	A5
32	RAM_ADDR<11>	99A	A3
31	RAM_ADDR<7>	101A	A1
30	RAM_ADDR<6>	103A	VDD6
29	RAM_ADDR<4>	105A	A10/AP
28	RAM_ADDR<2>	107A	BA0
27	RAM_ADDR<13>	109A	WE*
26	RAM_ADDR<14>	111A	VDD8
25	RAM_ADDR<15>	113A	CAS*
24	RAM_ADDR<16>	115A	NC/S1*
23	RAM_ADDR<17>	117A	VDD10
22	RAM_ADDR<18>	119A	NC/ODT1
21	RAM_ADDR<19>	121A	VSS31
20	RAM_ADDR<20>	123A	DQ32
19	RAM_ADDR<21>	125A	DQ33
18	RAM_ADDR<22>	127A	VSS33
17	RAM_ADDR<23>	129A	DQS4*
16	RAM_ADDR<24>	131A	DQS4
15	RAM_ADDR<25>	133A	VSS36
14	RAM_ADDR<26>	135A	DQ34
13	RAM_ADDR<27>	137A	DQ35
12	RAM_ADDR<28>	139A	VSS38
11	RAM_ADDR<29>	141A	DQ40
10	RAM_ADDR<30>	143A	DQ41
9	RAM_ADDR<31>	145A	VSS40
8	RAM_ADDR<32>	147A	DM5
7	RAM_ADDR<33>	149A	VSS41
6	RAM_ADDR<34>	151A	DQ42
5	RAM_ADDR<35>	153A	DQ43
4	RAM_ADDR<36>	155A	VSS43
3	RAM_ADDR<37>	157A	DQ48
2	RAM_ADDR<38>	159A	DQ49
1	RAM_ADDR<39>	161A	VSS45
41	=I2C_SODIMM_SDA	163A	NC_TEST
40	=I2C_SODIMM_SCL	165A	VSS47
39	=PP3V3_PWRON_VDDSPD	167A	DQS6*
38		169A	DQS6
37		171A	VSS49
36		173A	DQ50
35		175A	DQ51
34		177A	VSS51
33		179A	DQ56
32		181A	DQ57
31		183A	VSS53
30		185A	DM7
29		187A	VSS55
28		189A	DQ58
27		191A	DQ59
26		193A	VSS57
25		195A	SDA
24		197A	SCL
23		199A	VDDSPD
22		404	NC

DDR2 SO-DIMM Slot A		
SYNC_MASTER=N/A	SYNC_DATE=N/A	
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	SHT	OF	
	50	115	



SLOT "B"
UPPER SLOT
CUSTOMER SLOT

DDR2 VREF
ONE 0.1uF PER SLOT

DDR2 BYPASS
SLOT "B"

DDR2 SO-DIMM Slot B

SYNC_MASTER=N/A SYNC_DATE=N/A

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SCALE	NONE	SHT	OF
		52	115

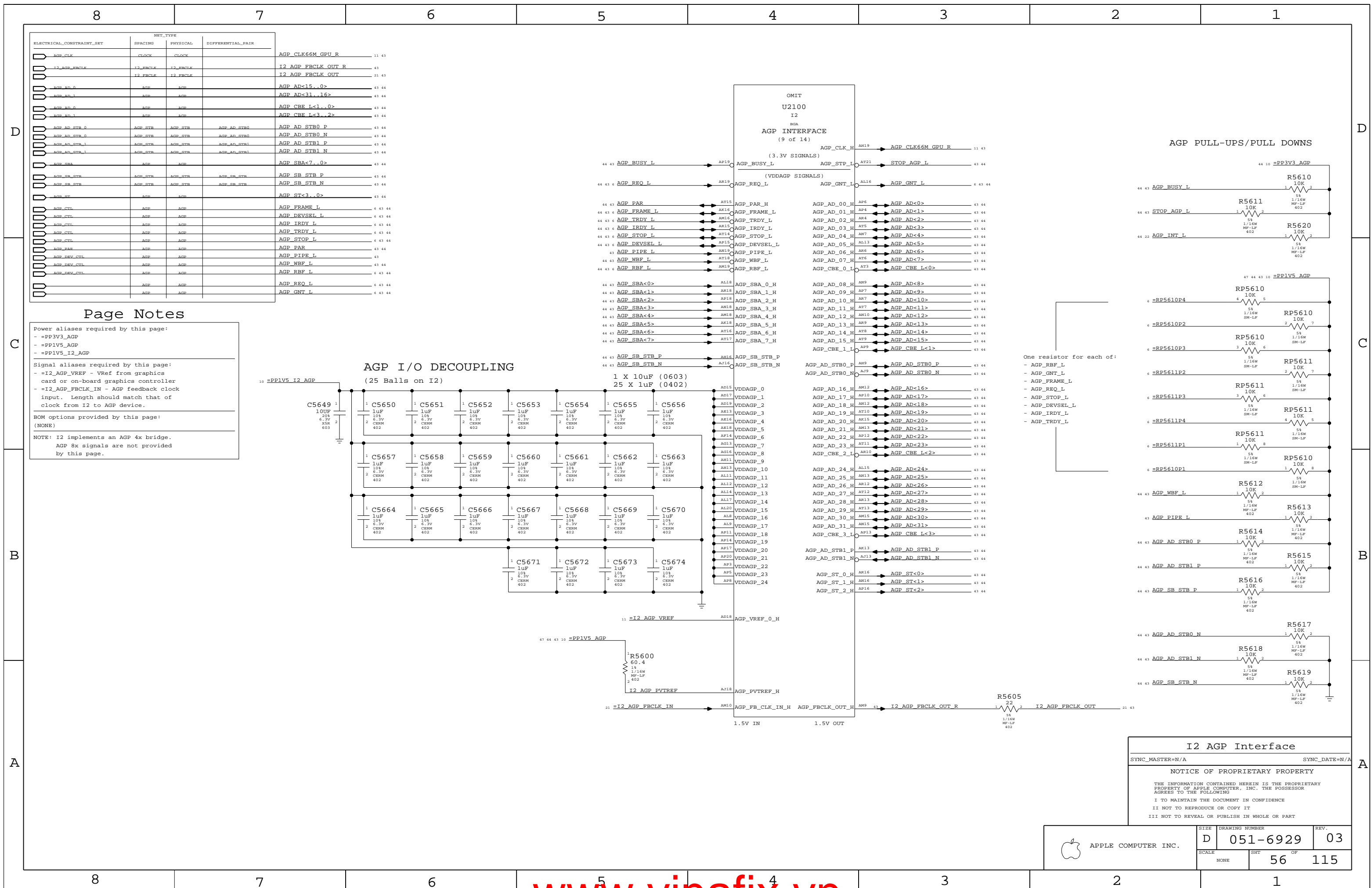


ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		SPACING	PHYSICAL	DIFFERENTIAL_PAIR
R100	FB_A_CLK_0	SAM DIFF	SAM DIFF	FB_A_CLK_0_P R
R100	(provided above)	SAM DIFF	SAM DIFF	FB_A_CLK_0_N R
R100	FB_A_CLK_1	SAM DIFF	SAM DIFF	FB_A_CLK_1_P R
R100	(provided above)	SAM DIFF	SAM DIFF	FB_A_CLK_1_N R
R100	FB_A_ADDR_CTL	SAM	SAM	FB_A_CKE_R
R100	FB_A_ADDR_CTL	SAM	SAM	FB_A_CS_L_R
R100	FB_A_ADDR_CTL	SAM	SAM	FB_A_ADDR_R<12..0>
R100	FB_A_ADDR_CTL	SAM	SAM	FB_A_BA_R<2..0>
R100	FB_A_ADDR_CTL	SAM	SAM	FB_A_RAS_L_R
R100	FB_A_ADDR_CTL	SAM	SAM	FB_A_CAS_L_R
R100	FB_A_ADDR_CTL	SAM	SAM	FB_A_WE_L_R
R100	FB_A_DQS0	SAM	SAM	FB_A_DQS_R<0>
R100	FB_A_DQS1	SAM	SAM	FB_A_DQS_R<1>
R100	FB_A_DQS2	SAM	SAM	FB_A_DQS_R<2>
R100	FB_A_DQS3	SAM	SAM	FB_A_DQS_R<3>
R100	FB_A_DQS4	SAM	SAM	FB_A_DQS_R<4>
R100	FB_A_DQS5	SAM	SAM	FB_A_DQS_R<5>
R100	FB_A_DQS6	SAM	SAM	FB_A_DQS_R<6>
R100	FB_A_DQS7	SAM	SAM	FB_A_DQS_R<7>
R100	FB_A_DQM0	SAM	SAM	FB_A_DQM_R<0>
R100	FB_A_DQM1	SAM	SAM	FB_A_DQM_R<1>
R100	FB_A_DQM2	SAM	SAM	FB_A_DQM_R<2>
R100	FB_A_DQM3	SAM	SAM	FB_A_DQM_R<3>
R100	FB_A_DQM4	SAM	SAM	FB_A_DQM_R<4>
R100	FB_A_DQM5	SAM	SAM	FB_A_DQM_R<5>
R100	FB_A_DQM6	SAM	SAM	FB_A_DQM_R<6>
R100	FB_A_DQM7	SAM	SAM	FB_A_DQM_R<7>
R100	FB_A_DO0	SAM	SAM	FB_A_DO_R<7..0>
R100	FB_A_DO1	SAM	SAM	FB_A_DO_R<15..8>
R100	FB_A_DO2	SAM	SAM	FB_A_DO_R<23..16>
R100	FB_A_DO3	SAM	SAM	FB_A_DO_R<31..24>
R100	FB_A_DO4	SAM	SAM	FB_A_DO_R<39..32>
R100	FB_A_DO5	SAM	SAM	FB_A_DO_R<47..40>
R100	FB_A_DO6	SAM	SAM	FB_A_DO_R<55..48>
R100	FB_A_DO7	SAM	SAM	FB_A_DO_R<63..56>

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		SPACING	PHYSICAL	DIFFERENTIAL_PAIR
R110	FB_B_CLK_0	SAM DIFF	SAM DIFF	FB_B_CLK_0_P R
R110	(provided above)	SAM DIFF	SAM DIFF	FB_B_CLK_0_N R
R110	FB_B_CLK_1	SAM DIFF	SAM DIFF	FB_B_CLK_1_P R
R110	(provided above)	SAM DIFF	SAM DIFF	FB_B_CLK_1_N R
R110	FB_B_ADDR_CTL	SAM	SAM	FB_B_CKE_R
R110	FB_B_ADDR_CTL	SAM	SAM	FB_B_CS_L_R
R110	FB_B_ADDR_CTL	SAM	SAM	FB_B_ADDR_R<12..0>
R110	FB_B_ADDR_CTL	SAM	SAM	FB_B_BA_R<2..0>
R110	FB_B_ADDR_CTL	SAM	SAM	FB_B_RAS_L_R
R110	FB_B_ADDR_CTL	SAM	SAM	FB_B_CAS_L_R
R110	FB_B_ADDR_CTL	SAM	SAM	FB_B_WE_L_R
R110	FB_B_DQS0	SAM	SAM	FB_B_DQS_R<0>
R110	FB_B_DQS1	SAM	SAM	FB_B_DQS_R<1>
R110	FB_B_DQS2	SAM	SAM	FB_B_DQS_R<2>
R110	FB_B_DQS3	SAM	SAM	FB_B_DQS_R<3>
R110	FB_B_DQS4	SAM	SAM	FB_B_DQS_R<4>
R110	FB_B_DQS5	SAM	SAM	FB_B_DQS_R<5>
R110	FB_B_DQS6	SAM	SAM	FB_B_DQS_R<6>
R110	FB_B_DQS7	SAM	SAM	FB_B_DQS_R<7>
R110	FB_B_DQM0	SAM	SAM	FB_B_DQM_R<0>
R110	FB_B_DQM1	SAM	SAM	FB_B_DQM_R<1>
R110	FB_B_DQM2	SAM	SAM	FB_B_DQM_R<2>
R110	FB_B_DQM3	SAM	SAM	FB_B_DQM_R<3>
R110	FB_B_DQM4	SAM	SAM	FB_B_DQM_R<4>
R110	FB_B_DQM5	SAM	SAM	FB_B_DQM_R<5>
R110	FB_B_DQM6	SAM	SAM	FB_B_DQM_R<6>
R110	FB_B_DQM7	SAM	SAM	FB_B_DQM_R<7>
R110	FB_B_DO0	SAM	SAM	FB_B_DO_R<7..0>
R110	FB_B_DO1	SAM	SAM	FB_B_DO_R<15..8>
R110	FB_B_DO2	SAM	SAM	FB_B_DO_R<23..16>
R110	FB_B_DO3	SAM	SAM	FB_B_DO_R<31..24>
R110	FB_B_DO4	SAM	SAM	FB_B_DO_R<39..32>
R110	FB_B_DO5	SAM	SAM	FB_B_DO_R<47..40>
R110	FB_B_DO6	SAM	SAM	FB_B_DO_R<55..48>
R110	FB_B_DO7	SAM	SAM	FB_B_DO_R<63..56>

M11 Frame Buffer Constraints
 SYNC_MASTER=N/A SYNC_DATE=N/A
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	NONE	D 051-6929	03
		SHT	OF
		55	115



Page Notes

Power aliases required by this page:
 - =PP3V3_AGP
 - =PP1V5_AGP
 - =PP1V5_I2_AGP

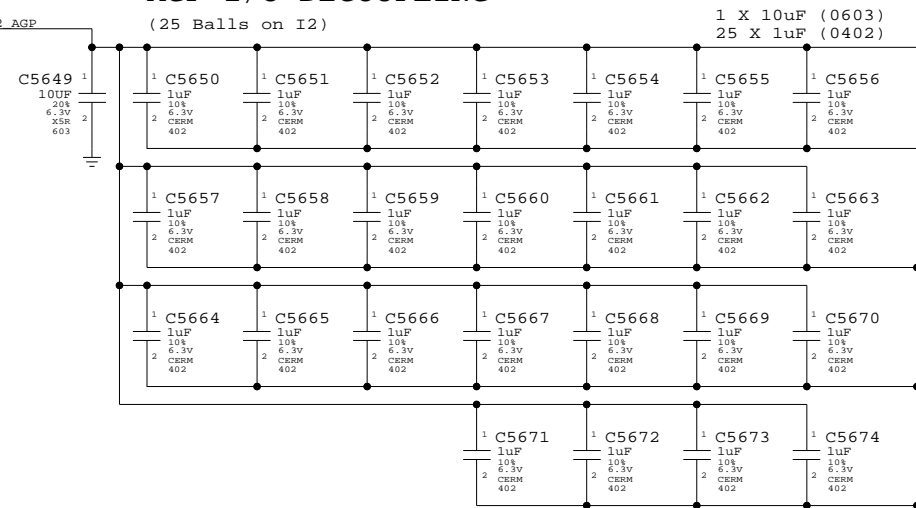
Signal aliases required by this page:
 - =I2_AGP_VREF - VRef from graphics card or on-board graphics controller
 - =I2_AGP_FBCLK_IN - AGP feedback clock input. Length should match that of clock from I2 to AGP device.

BOM options provided by this page:
 (NONE)

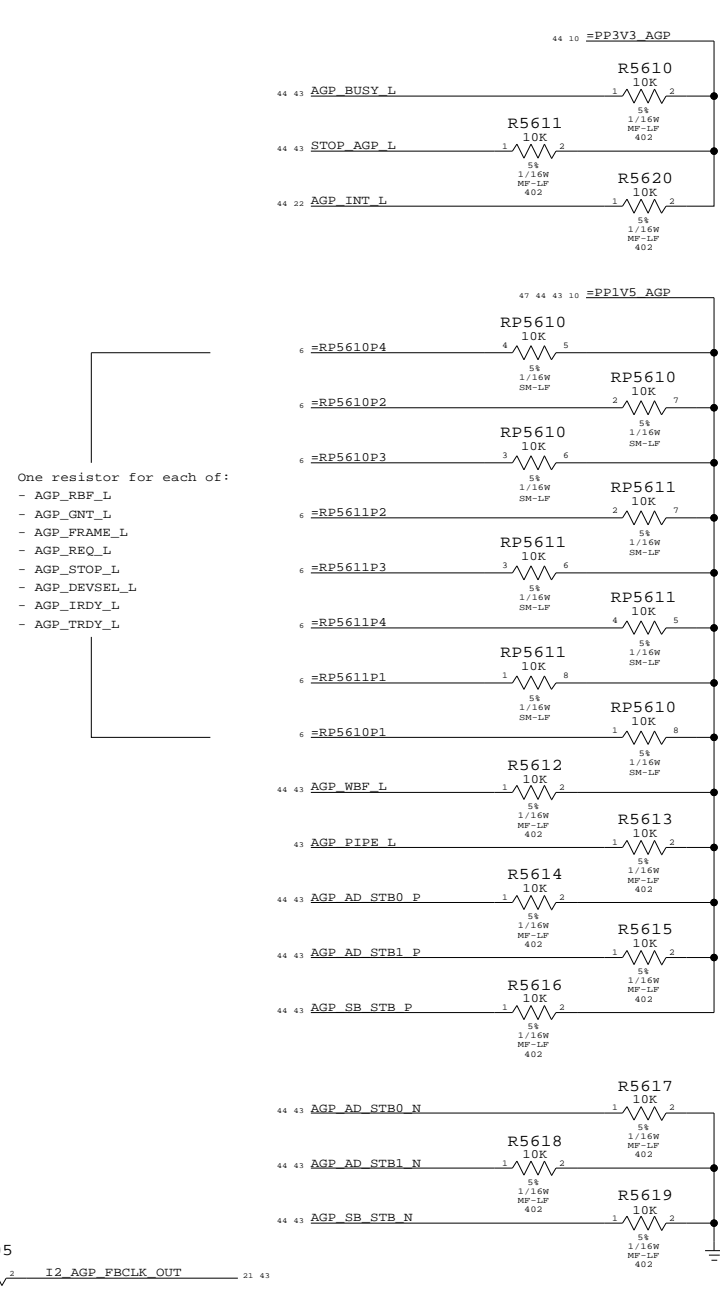
NOTE: I2 implements an AGP 4x bridge. AGP 8x signals are not provided by this page.

AGP I/O DECOUPLING

(25 Balls on I2)



AGP PULL-UPS/PULL-DOWNS



One resistor for each of:
 - AGP_RBF_L
 - AGP_GNT_L
 - AGP_FRAME_L
 - AGP_STOP_L
 - AGP_DEVSEL_L
 - AGP_IRDY_L

I2 AGP Interface

SYNC_MASTER=N/A SYNC_DATE=N/A

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	D	051-6929	03
SCALE	SHT	OF	
NONE	56	115	

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
770	CLOCK	CLOCK	

AGP_CLK66M_GPU 11 44

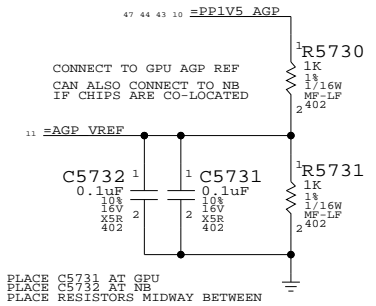
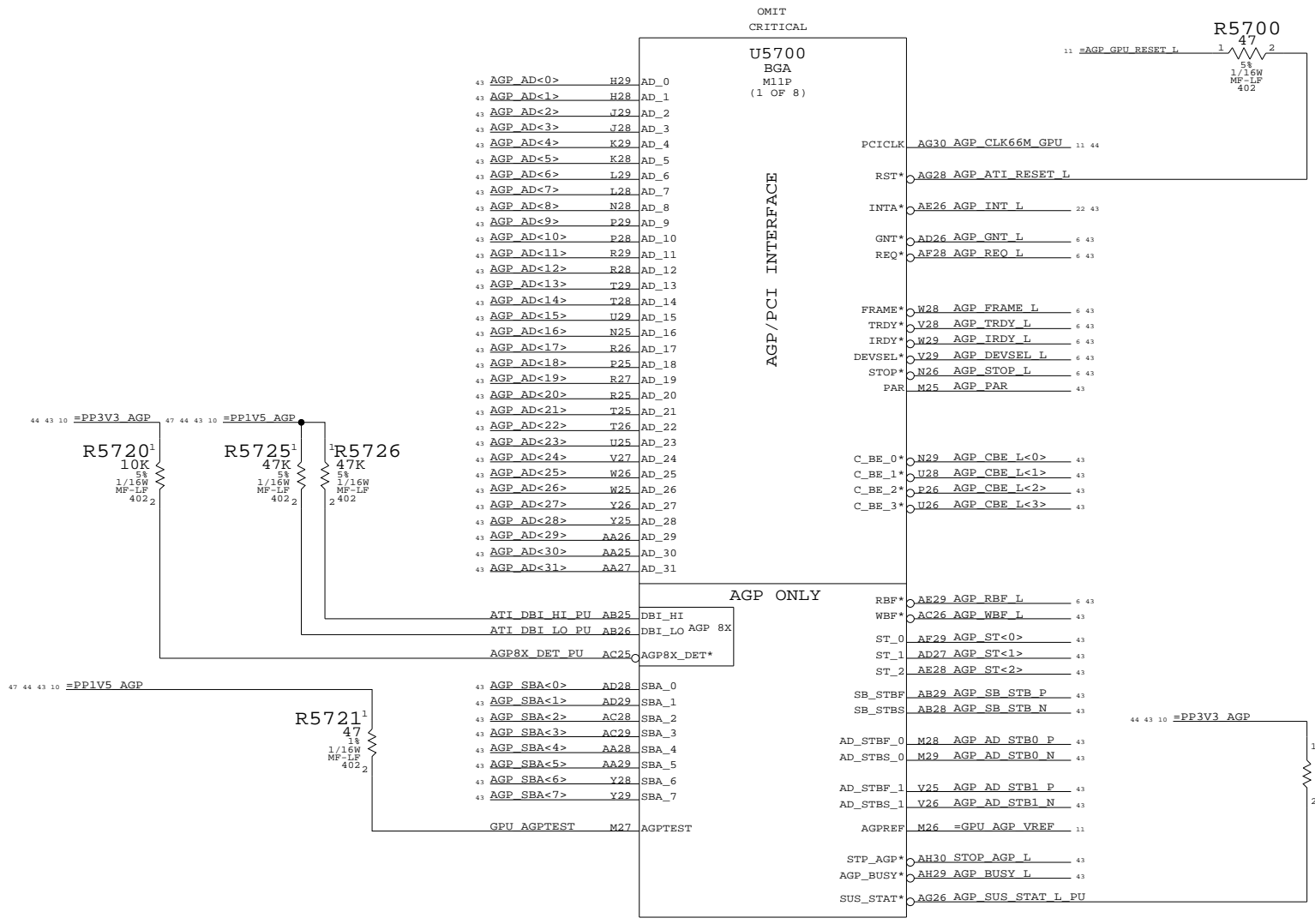
Page Notes

Power aliases required by this page:
 - =PP3V3_AGP
 - =PP1V5_AGP

Signal aliases required by this page:
 - =AGP_VREF - Vref divider output for both GPU and NB
 - =AGP_GPU_RESET_L - Active low reset for GPU

BOM options provided by this page:
 (NONE)

NOTE: AGP 8x signals are not provided by this page.



GPU (M11) AGP Interface

SYNC_MASTER=N/A SYNC_DATE=N/A

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6929	03
SCALE	NONE	SHT OF	57 115

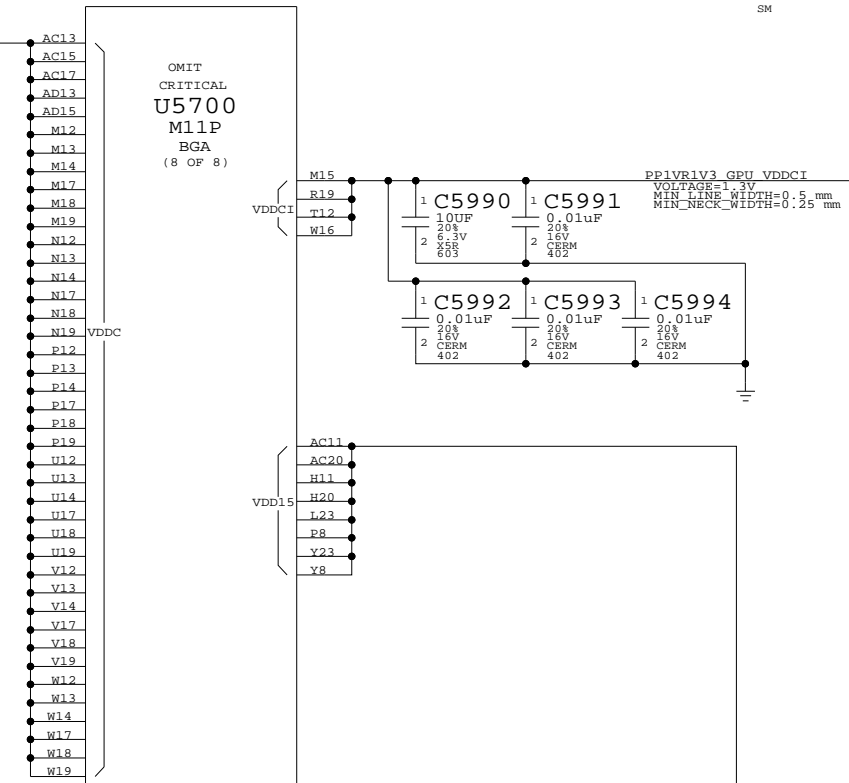
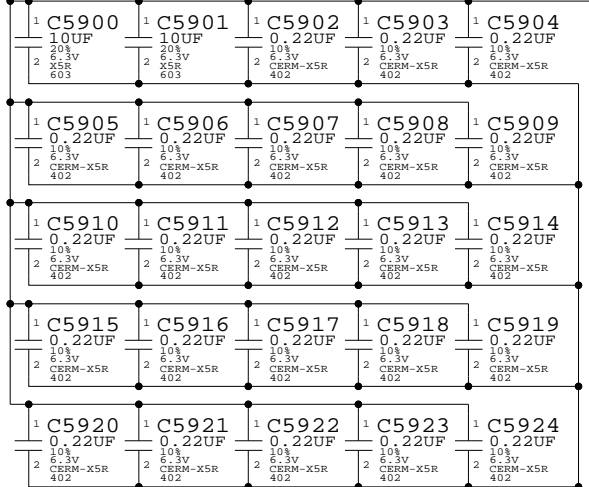
Power aliases required by this page:
 - =PPIV5_GPU_VDD15
 - =PPIV1V3_GPU_VCORE

Signal aliases required by this page:
 (NONE)

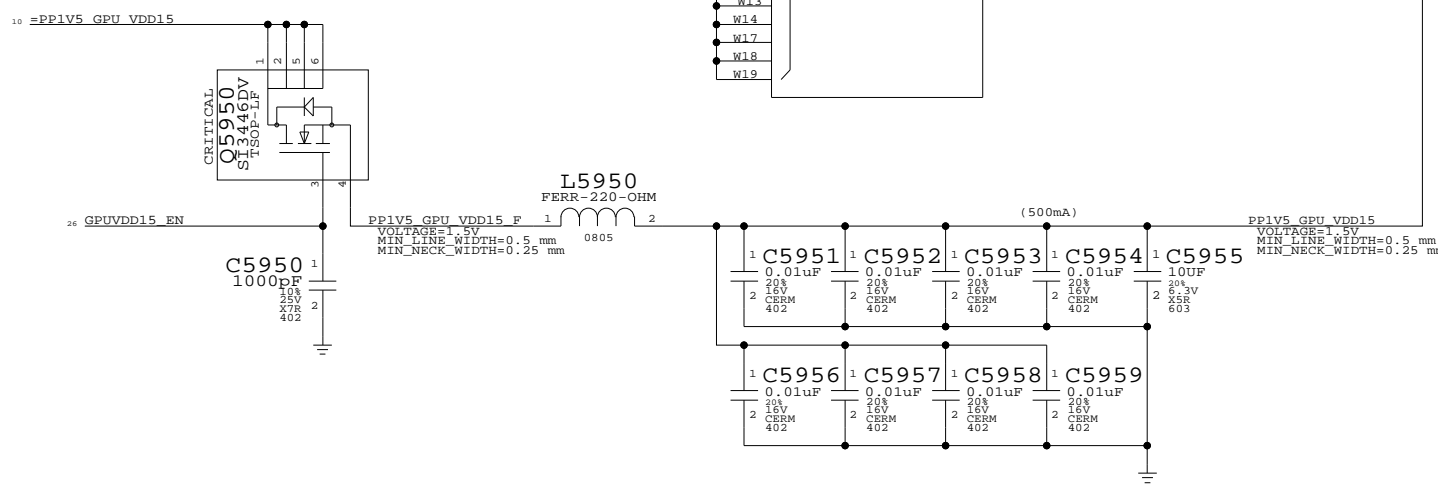
BOM options provided by this page:
 (NONE)

GPU VCORE - 1.3V/1.05V

Internal I/O - 1.3V/1.05V



Internal I/O - 1.5V



OMIT CRITICAL U5700 M11P BGA (6 OF 8)

HOST GROUND

CORE GND

I/O GROUND

GPU (M11) Core Power

SYNC_MASTER=N/A SYNC_DATE=N/A

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6929	03
SCALE	NONE	SHT	OF
		59	115

Page Notes

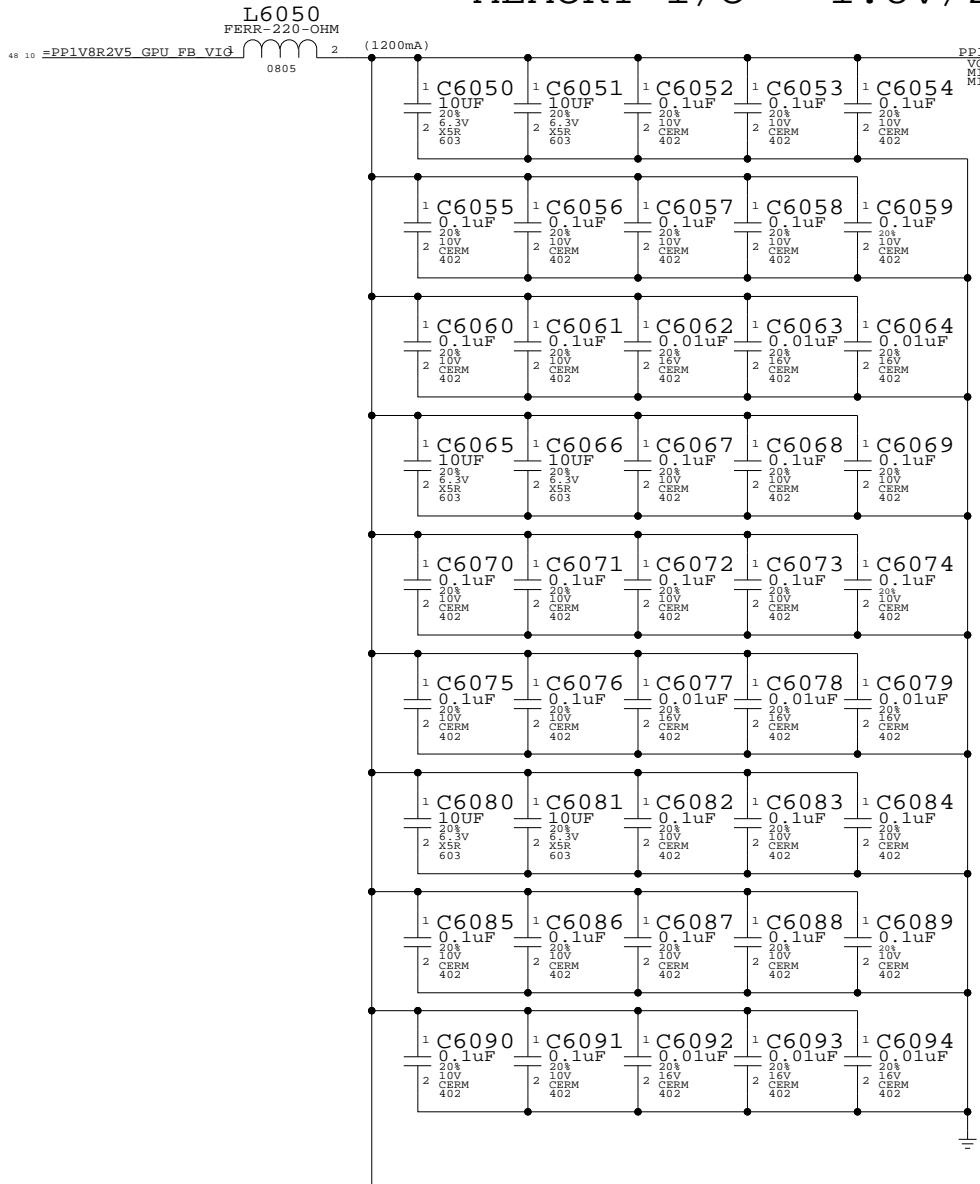
Power aliases required by this page:
 - =PP1V8R2V5_GPU_FB_VIO - =PP1V8_GPU_PANEL_IO
 - =PP3V3_GPU_VDDR3 - =PP1V8_GPU_LVDS_PLL
 - =PP1V5_GPU_DVO - =PP2V5_GPU_LVDS_IO
 - =PP1V8_GPU_DVO - =PP2V5_GPU_LVDS_IO
 - =PP1V5R3V3_DVO_VREF - =PP1V5_AGP

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 - DVO_1V5 - GPU_LVDDR_2V5
 - DVO_1V8 - GPU_LVDDR_2V8

NOTE: Implements a low-swing DVO bus only

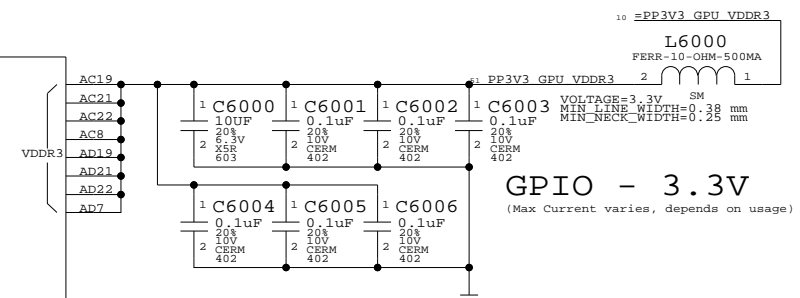
MEMORY I/O - 1.8V/2.5V



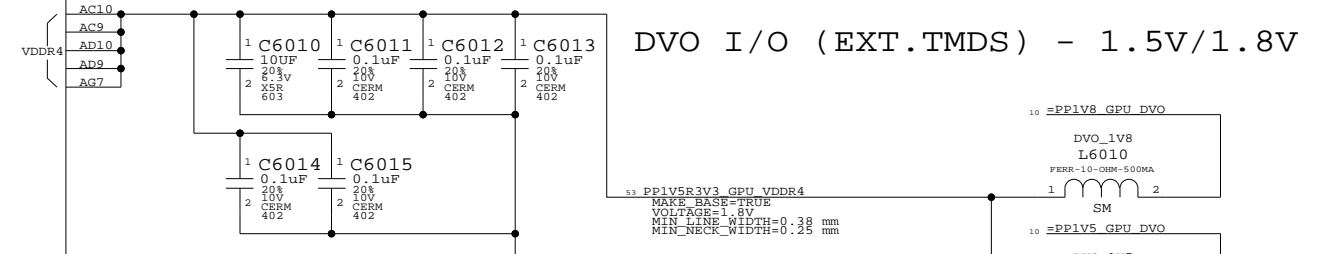
OMIT
 CRITICAL
 U5700
 M11P
 BGA
 (7 OF 8)

- A15
- A21
- A28
- A9
- AA1
- AA4
- AA7
- AA8
- AD4
- B1
- B30
- D11
- D13
- D14
- D17
- D19
- D20
- D23
- D26
- D5
- D8
- E27
- F4
- G10
- G13
- G15
- G19
- G22
- G27
- H7
- H10
- H13
- H15
- H17
- H19
- H22
- J1
- J23
- J24
- J4
- J7
- J8
- L27
- L8
- M4
- N4
- N7
- N8
- R1
- R4
- T4
- T7
- T8
- V4
- V7
- V8

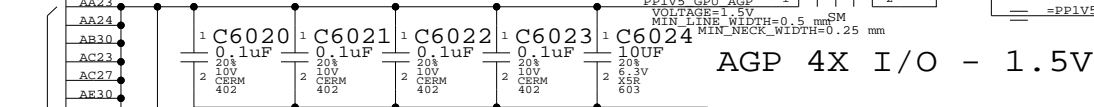
GPIO - 3.3V
 (Max Current varies, depends on usage)



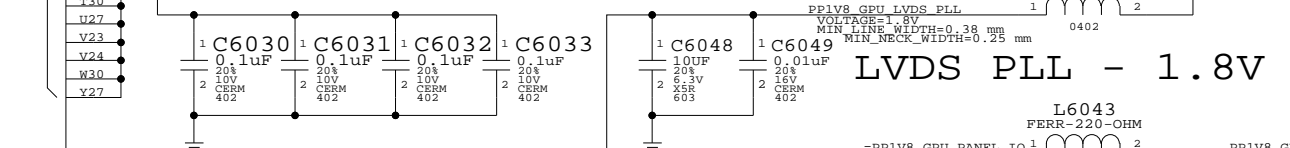
DVO I/O (EXT.TMDS) - 1.5V/1.8V



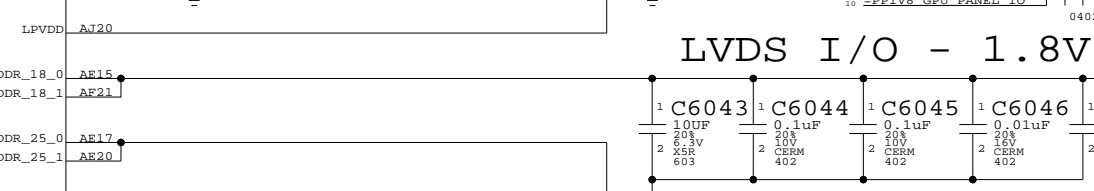
AGP 4X I/O - 1.5V



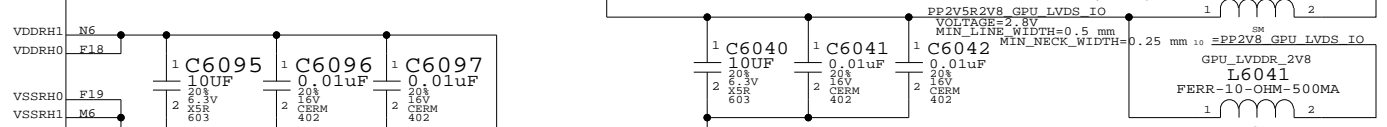
LVDS PLL - 1.8V



LVDS I/O - 1.8V



LVDS I/O - 2.5V/2.8V



GPU (M11) I/O Power

SYNC_MASTER=N/A SYNC_DATE=N/A

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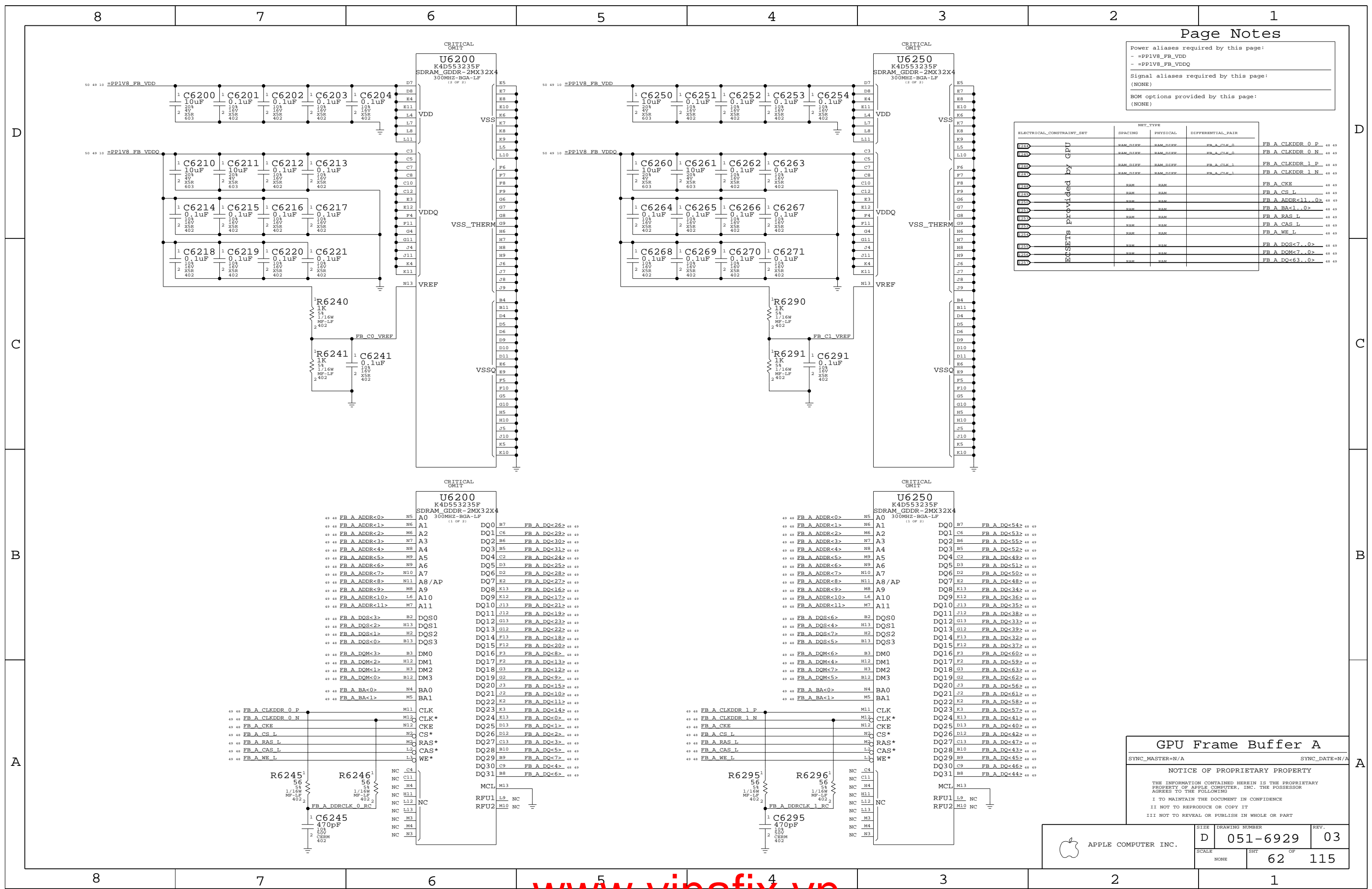
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6929	03
SCALE	SHT	OF	
NONE	60	115	

Power aliases required by this page:
 - =PPIV8_FB_VDD
 - =PPIV8_FB_VDDQ

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
FB00	RAM_DIFF	RAM_DIFF	FB_A_CLK_0
FB01	RAM_DIFF	RAM_DIFF	FB_A_CLK_0
FB02	RAM_DIFF	RAM_DIFF	FB_A_CLK_1
FB03	RAM_DIFF	RAM_DIFF	FB_A_CLK_1
FB04	RAM	RAM	FB_A_CKE
FB05	RAM	RAM	FB_A_CS_L
FB06	RAM	RAM	FB_A_ADDR<11..0>
FB07	RAM	RAM	FB_A_BA<1..0>
FB08	RAM	RAM	FB_A_RAS_L
FB09	RAM	RAM	FB_A_CAS_L
FB10	RAM	RAM	FB_A_WE_L
FB11	RAM	RAM	FB_A_DQS<7..0>
FB12	RAM	RAM	FB_A_DQM<7..0>
FB13	RAM	RAM	FB_A_DQ<63..0>



CRITICAL OMIT

U6200
K4D553235F
SDRAM_GDDR-2MX32X4
300MHZ-BGA-LF
(1 OF 2)

48 48 FB_A_ADDR<0>	N5	A0	DQ0	B7	FB_A_DQ<26>	48 48
48 48 FB_A_ADDR<1>	N6	A1	DQ1	C6	FB_A_DQ<29>	48 48
48 48 FB_A_ADDR<2>	N6	A2	DQ2	B6	FB_A_DQ<30>	48 48
48 48 FB_A_ADDR<3>	N7	A3	DQ3	B5	FB_A_DQ<31>	48 48
48 48 FB_A_ADDR<4>	N8	A4	DQ4	C2	FB_A_DQ<24>	48 48
48 48 FB_A_ADDR<5>	N9	A5	DQ5	D3	FB_A_DQ<25>	48 48
48 48 FB_A_ADDR<6>	N9	A6	DQ6	D2	FB_A_DQ<28>	48 48
48 48 FB_A_ADDR<7>	N10	A7	DQ7	E2	FB_A_DQ<27>	48 48
48 48 FB_A_ADDR<8>	N11	A8/AP	DQ8	K13	FB_A_DQ<16>	48 48
48 48 FB_A_ADDR<9>	M8	A9	DQ9	K12	FB_A_DQ<17>	48 48
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48 48 FB_A_DQS<2>	H13	DQS1	DQ13	G12	FB_A_DQ<22>	48 48
48 48 FB_A_DQS<1>	H2	DQS2	DQ14	F13	FB_A_DQ<18>	48 48
48 48 FB_A_DQS<0>	B13	DQS3	DQ15	F12	FB_A_DQ<20>	48 48
48 48 FB_A_DQM<3>	B3	DM0	DQ16	F3	FB_A_DQ<8>	48 48
48 48 FB_A_DQM<2>	H12	DM1	DQ17	F2	FB_A_DQ<13>	48 48
48 48 FB_A_DQM<1>	H3	DM2	DQ18	G3	FB_A_DQ<12>	48 48
48 48 FB_A_DQM<0>	B12	DM3	DQ19	G2	FB_A_DQ<9>	48 48
48 48 FB_A_BA<0>	N4	BA0	DQ20	J3	FB_A_DQ<15>	48 48
48 48 FB_A_BA<1>	M5	BA1	DQ21	J2	FB_A_DQ<10>	48 48
48 48 FB_A_CLKDDR_0_P	M11	CLK	DQ22	K2	FB_A_DQ<11>	48 48
48 48 FB_A_CLKDDR_0_N	M12	CLK*	DQ23	K3	FB_A_DQ<14>	48 48
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48 48 FB_A_CS_L	N2	CS*	DQ25	D13	FB_A_DQ<1>	48 48
48 48 FB_A_RAS_L	M2	RAS*	DQ26	D12	FB_A_DQ<2>	48 48
48 48 FB_A_CAS_L	L2	CAS*	DQ27	C13	FB_A_DQ<3>	48 48
48 48 FB_A_WE_L	L3	WE*	DQ28	B10	FB_A_DQ<5>	48 48
48 48 FB_A_DQ<3>	N1	DQ30	DQ29	B9	FB_A_DQ<7>	48 48
48 48 FB_A_DQ<4>	N1	DQ31	DQ30	C9	FB_A_DQ<4>	48 48
48 48 FB_A_DQ<5>	N1	DQ32	DQ31	B8	FB_A_DQ<6>	48 48
48 48 FB_A_DQ<6>	N1	DQ33	DQ32	M13	MCL	48 48
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48 48 FB_A_DQ<21>	N1	DQ48				48 48
48 48 FB_A_DQ<22>	N1	DQ49				48 48
48 48 FB_A_DQ<23>	N1	DQ50				48 48
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48 48 FB_A_DQ<25>	N1	DQ52				48 48
48 48 FB_A_DQ<26>	N1	DQ53				48 48
48 48 FB_A_DQ<27>	N1	DQ54				48 48
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48 48 FB_A_DQ<29>	N1	DQ56				48 48
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48 48 FB_A_DQ<31>	N1	DQ58				48 48

CRITICAL OMIT

U6250
K4D553235F
SDRAM_GDDR-2MX32X4
300MHZ-BGA-LF
(1 OF 2)

48 48 FB_A_ADDR<0>	N5	A0	DQ0	B7	FB_A_DQ<54>	48 48
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48 48 FB_A_ADDR<3>	N7	A3	DQ3	B5	FB_A_DQ<52>	48 48
48 48 FB_A_ADDR<4>	N8	A4	DQ4	C2	FB_A_DQ<49>	48 48
48 48 FB_A_ADDR<5>	N9	A5	DQ5	D3	FB_A_DQ<51>	48 48
48 48 FB_A_ADDR<6>	N9	A6	DQ6	D2	FB_A_DQ<50>	48 48
48 48 FB_A_ADDR<7>	N10	A7	DQ7	E2	FB_A_DQ<48>	48 48
48 48 FB_A_ADDR<8>	N11	A8/AP	DQ8	K13	FB_A_DQ<34>	48 48
48 48 FB_A_ADDR<9>	M8	A9	DQ9	K12	FB_A_DQ<36>	48 48
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48 48 FB_A_ADDR<11>	M7	A11	DQ11	J12	FB_A_DQ<38>	48 48
48 48 FB_A_DQS<6>	B2	DQS0	DQ12	G13	FB_A_DQ<33>	48 48
48 48 FB_A_DQS<4>	H13	DQS1	DQ13	G12	FB_A_DQ<39>	48 48
48 48 FB_A_DQS<7>	H2	DQS2	DQ14	F13	FB_A_DQ<32>	48 48
48 48 FB_A_DQS<5>	B13	DQS3	DQ15	F12	FB_A_DQ<37>	48 48
48 48 FB_A_DQM<6>	B3	DM0	DQ16	F3	FB_A_DQ<60>	48 48
48 48 FB_A_DQM<4>	H12	DM1	DQ17	F2	FB_A_DQ<59>	48 48
48 48 FB_A_DQM<7>	H3	DM2	DQ18	G3	FB_A_DQ<63>	48 48
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48 48 FB_A_BA<0>	N4	BA0	DQ20	J3	FB_A_DQ<56>	48 48
48 48 FB_A_BA<1>	M5	BA1	DQ21	J2	FB_A_DQ<61>	48 48
48 48 FB_A_CLKDDR_1_P	M11	CLK	DQ22	K2	FB_A_DQ<58>	48 48
48 48 FB_A_CLKDDR_1_N	M12	CLK*	DQ23	K3	FB_A_DQ<57>	48 48
48 48 FB_A_CKE	N12	CKE	DQ24	E13	FB_A_DQ<41>	48 48
48 48 FB_A_CS_L	N2	CS*	DQ25	D13	FB_A_DQ<40>	48 48
48 48 FB_A_RAS_L	M2	RAS*	DQ26	D12	FB_A_DQ<42>	48 48
48 48 FB_A_CAS_L	L2	CAS*	DQ27	C13	FB_A_DQ<47>	48 48
48 48 FB_A_WE_L	L3	WE*	DQ28	B10	FB_A_DQ<43>	48 48
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48 48 FB_A_DQ<4>	N1	DQ31	DQ30	C9	FB_A_DQ<46>	48 48
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48 48 FB_A_DQ<6>	N1	DQ33	DQ32	M13	MCL	48 48
48 48 FB_A_DQ<7>	N1	DQ34	RFU1	L9	NC	48 48
48 48 FB_A_DQ<8>	N1	DQ35	RFU2	M10	NC	48 48
48 48 FB_A_DQ<9>	N1	DQ36				48 48
48 48 FB_A_DQ<10>	N1	DQ37				48 48
48 48 FB_A_DQ<11>	N1	DQ38				48 48
48 48 FB_A_DQ<12>	N1	DQ39				48 48
48 48 FB_A_DQ<13>	N1	DQ40				48 48
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48 48 FB_A_DQ<15>	N1	DQ42				48 48
48 48 FB_A_DQ<16>	N1	DQ43				48 48
48 48 FB_A_DQ<17>	N1	DQ44				48 48
48 48 FB_A_DQ<18>	N1	DQ45				48 48
48 48 FB_A_DQ<19>	N1	DQ46				48 48
48 48 FB_A_DQ<20>	N1	DQ47				48 48
48 48 FB_A_DQ<21>	N1	DQ48				48 48
48 48 FB_A_DQ<22>	N1	DQ49				48 48
48 48 FB_A_DQ<23>	N1	DQ50				48 48
48 48 FB_A_DQ<24>	N1	DQ51				48 48
48 48 FB_A_DQ<25>	N1	DQ52				48 48
48 48 FB_A_DQ<26>	N1	DQ53				48 48
48 48 FB_A_DQ<27>	N1	DQ54				48 48
48 48 FB_A_DQ<28>	N1	DQ55				48 48
48 48 FB_A_DQ<29>	N1	DQ56				48 48
48 48 FB_A_DQ<30>	N1	DQ57				48 48
48 48 FB_A_DQ<31>	N1	DQ58				48 48

GPU Frame Buffer A

SYNC_MASTER=N/A SYNC_DATE=N/A

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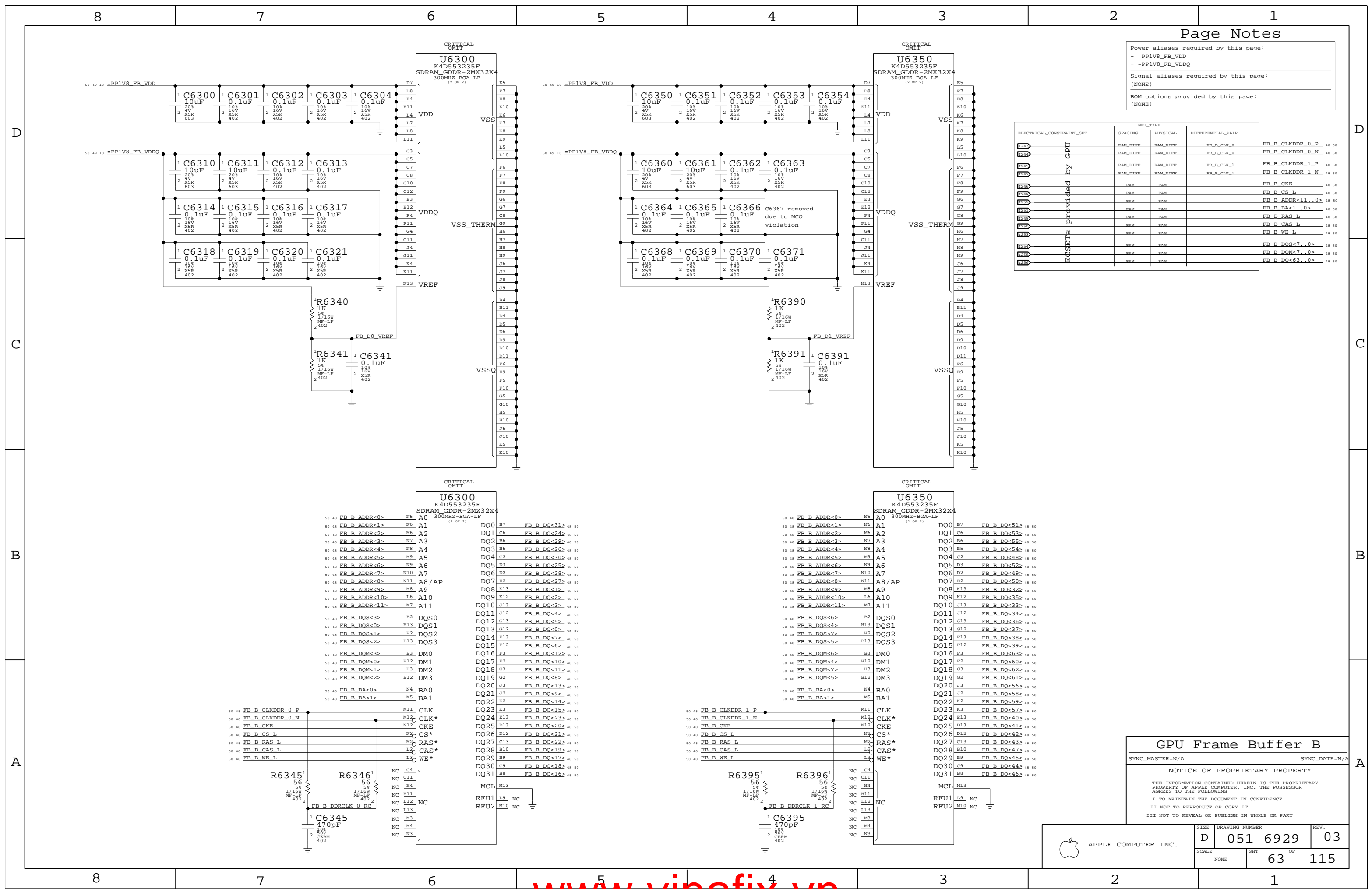
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6929	03
SCALE	NONE	SHT	OF
		62	115

Power aliases required by this page:
 - =PPIV8_FB_VDD
 - =PPIV8_FB_VDDQ

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
FB00	RAM_DIFF	RAM_DIFF	FB_B_CLK_0
FB01	RAM_DIFF	RAM_DIFF	FB_B_CLK_0
FB02	RAM_DIFF	RAM_DIFF	FB_B_CLK_1
FB03	RAM_DIFF	RAM_DIFF	FB_B_CLK_1
FB04	RAM	RAM	FB_B_CKE
FB05	RAM	RAM	FB_B_CKE
FB06	RAM	RAM	FB_B_CKE
FB07	RAM	RAM	FB_B_CKE
FB08	RAM	RAM	FB_B_CKE
FB09	RAM	RAM	FB_B_CKE
FB10	RAM	RAM	FB_B_CKE
FB11	RAM	RAM	FB_B_CKE
FB12	RAM	RAM	FB_B_CKE
FB13	RAM	RAM	FB_B_CKE
FB14	RAM	RAM	FB_B_CKE
FB15	RAM	RAM	FB_B_CKE
FB16	RAM	RAM	FB_B_CKE
FB17	RAM	RAM	FB_B_CKE
FB18	RAM	RAM	FB_B_CKE
FB19	RAM	RAM	FB_B_CKE
FB20	RAM	RAM	FB_B_CKE
FB21	RAM	RAM	FB_B_CKE
FB22	RAM	RAM	FB_B_CKE
FB23	RAM	RAM	FB_B_CKE
FB24	RAM	RAM	FB_B_CKE
FB25	RAM	RAM	FB_B_CKE
FB26	RAM	RAM	FB_B_CKE
FB27	RAM	RAM	FB_B_CKE
FB28	RAM	RAM	FB_B_CKE
FB29	RAM	RAM	FB_B_CKE
FB30	RAM	RAM	FB_B_CKE
FB31	RAM	RAM	FB_B_CKE
FB32	RAM	RAM	FB_B_CKE
FB33	RAM	RAM	FB_B_CKE
FB34	RAM	RAM	FB_B_CKE
FB35	RAM	RAM	FB_B_CKE
FB36	RAM	RAM	FB_B_CKE
FB37	RAM	RAM	FB_B_CKE
FB38	RAM	RAM	FB_B_CKE
FB39	RAM	RAM	FB_B_CKE
FB40	RAM	RAM	FB_B_CKE
FB41	RAM	RAM	FB_B_CKE
FB42	RAM	RAM	FB_B_CKE
FB43	RAM	RAM	FB_B_CKE
FB44	RAM	RAM	FB_B_CKE
FB45	RAM	RAM	FB_B_CKE
FB46	RAM	RAM	FB_B_CKE
FB47	RAM	RAM	FB_B_CKE
FB48	RAM	RAM	FB_B_CKE
FB49	RAM	RAM	FB_B_CKE
FB50	RAM	RAM	FB_B_CKE



GPU Frame Buffer B

SYNC_MASTER=N/A SYNC_DATE=N/A

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	D	051-6929	03
SCALE	NONE	SHT	OF
		63	115

Page Notes

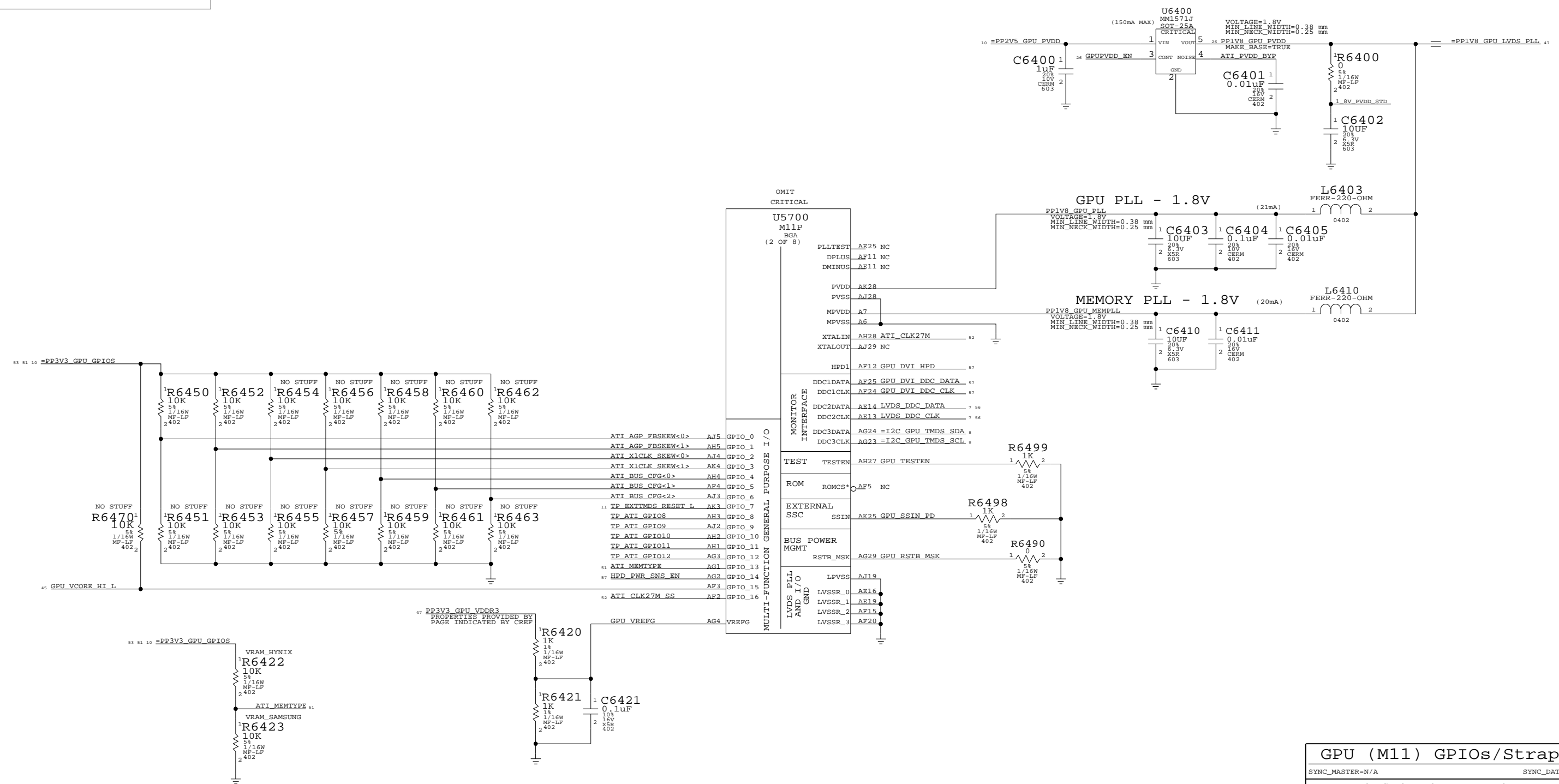
Power aliases required by this page:
 - =PP3V3_GPU_GPIOS
 - =PP2V5_PVDD
 - =PP1V8_GPU_LVDS_PLL

Signal aliases required by this page:
 - =I2C_GPU_TMDS_SDA - I2C data line for external TMDS transmitters
 - =I2C_GPU_TMDS_SCL - I2C clock line for external TMDS transmitters

BOM options provided by this page:
 (NONE)

D
C
B
A

D
C
B
A



GPU (M11) GPIOs/Straps

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6929	03
SCALE	NONE	SHT OF	64 OF 115

Page Notes

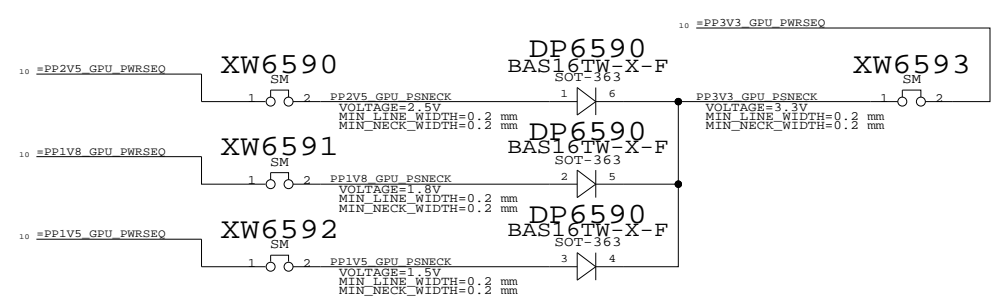
Power aliases required by this page:
 - =PP3V3_GPU_CLOCKS - =PP3V3_GPU_PWRSEQ
 - =PPVIN_GPU_LVDDR_LDO - =PP2V5_GPU_PWRSEQ
 - =PP2V5_GPU_LVDDR_LDO - =PP1V8_GPU_PWRSEQ
 - =PP1V5_GPU_PWRSEQ

Signal aliases required by this page:
 (NONE)

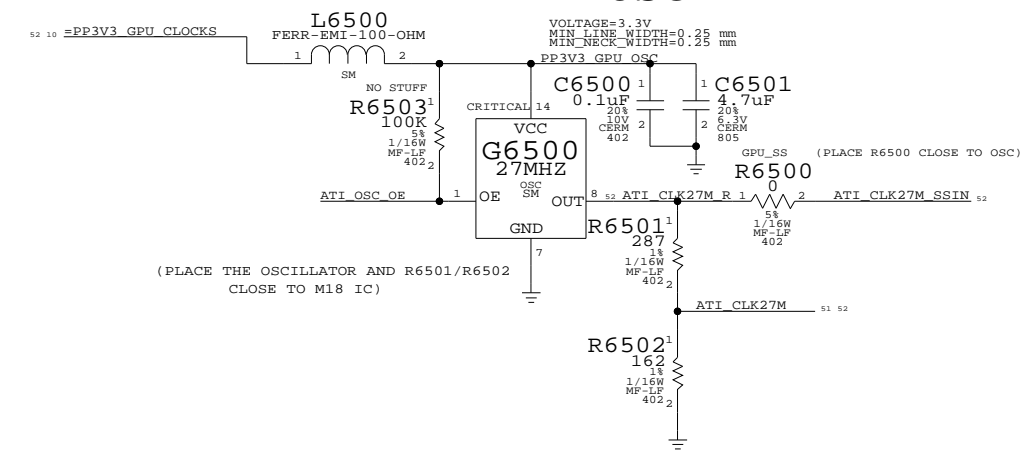
BOM options provided by this page:
 - GPU_SS - GPU_LVDDR_2V8

ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
R60	ATI_CLK27M	CLOCK	CLOCK
R64	ATI_CLK27M	CLOCK	CLOCK
R65	ATI_CLK27M	CLOCK	CLOCK
R61	ATI_CLK27M_SS	CLOCK	CLOCK
R62	ATI_CLK27M_SS	CLOCK	CLOCK

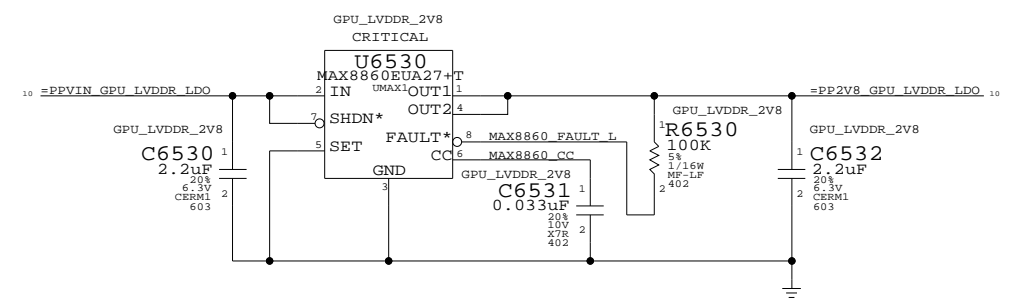
M11 Power Shutdown Sequencing



27M OSC

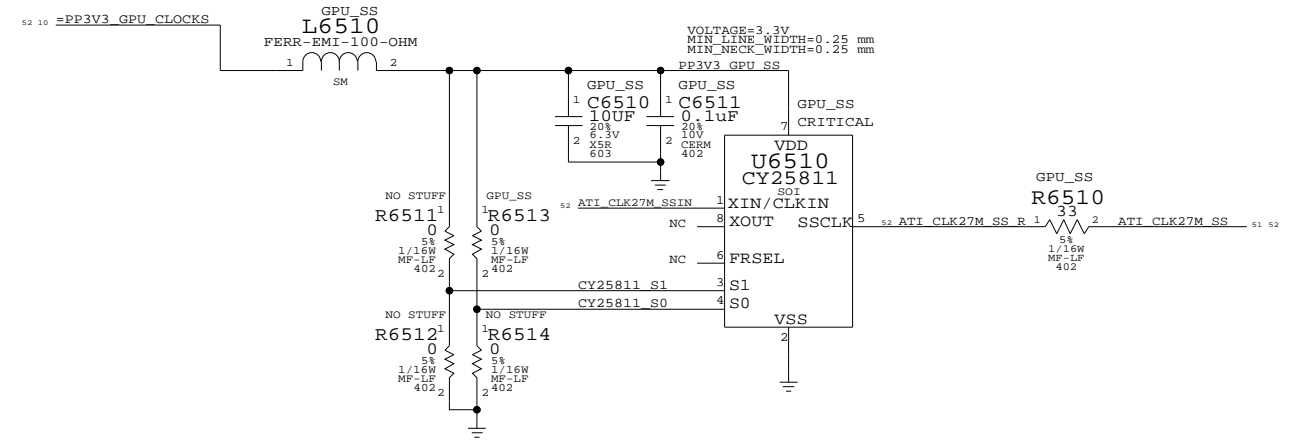


LVDDR 2.8V LDO



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S0647	353S1140	GPU_LVDDR_2V8	U6530	2.82V instead of 2.77V

SPREAD SPECTRUM SUPPORT
 S0=1;S1=M => -1.5% DOWN-SPREAD



GPU (M11) Clocks/Misc

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NONE	65	115	

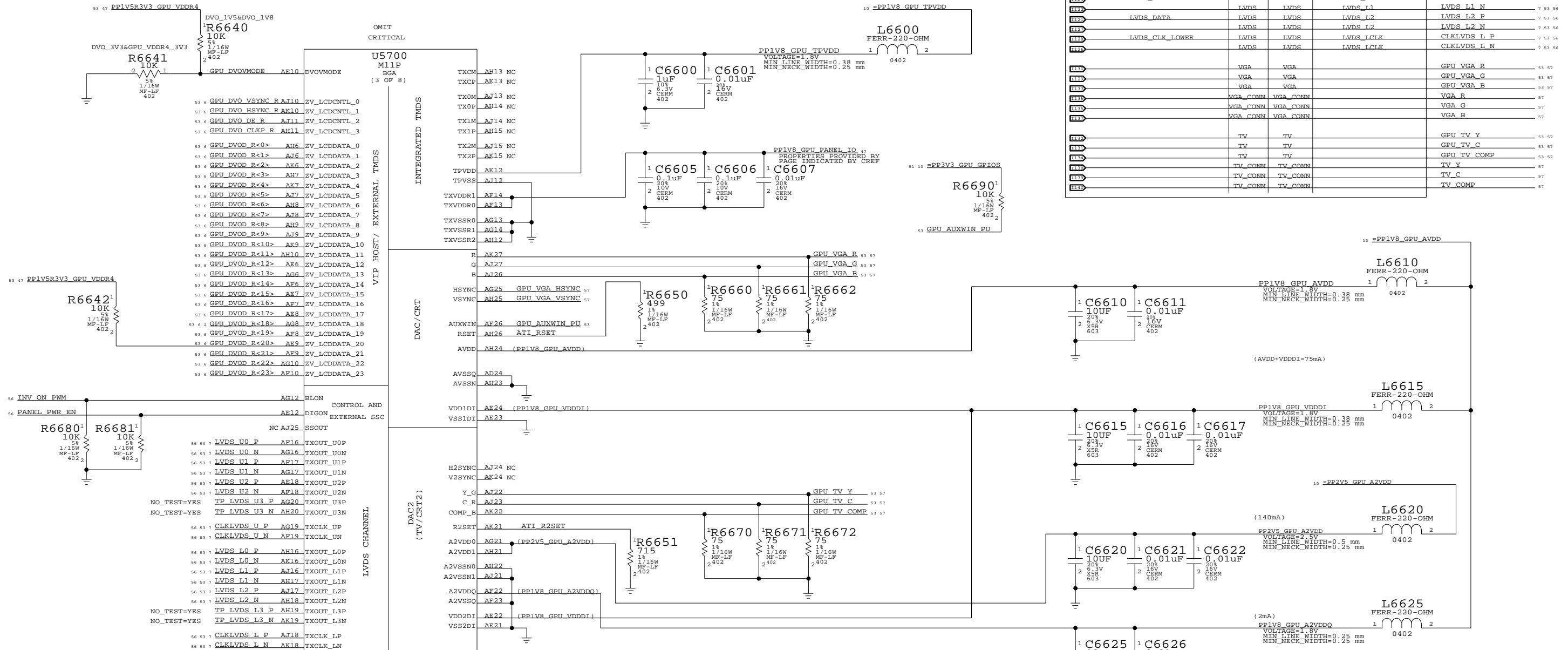
Page Notes

Power aliases required by this page:
 - =PP2V5_GPU_A2VDD - =PP1V8_GPU_AVDD
 - =PP1V8_GPU_TPVDV - =PP3V3_GPU_GPIOS

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 - DVO_1V5 - GPU_VDDR4_3V3
 - DVO_1V8 - DVO_3V3

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		DIFFERENTIAL_PAIR	
	SPACING	PHYSICAL		
R6600	DVO	DVO		GPU DVOD R<23..0>
R6601	DVO	DVO		GPU DVO HSYNC R
R6602	DVO	DVO		GPU DVO VSYNC R
R6603	DVO	DVO		GPU DVO DE R
R6604	DVO	DVO		GPU DVO CLKP R
R6605	LVDS_DATA	LVDS	LVDS_U0	LVDS U0_P
R6606	LVDS_DATA	LVDS	LVDS_U0	LVDS U0_N
R6607	LVDS_DATA	LVDS	LVDS_U1	LVDS U1_P
R6608	LVDS_DATA	LVDS	LVDS_U1	LVDS U1_N
R6609	LVDS_DATA	LVDS	LVDS_U2	LVDS U2_P
R6610	LVDS_DATA	LVDS	LVDS_U2	LVDS U2_N
R6611	LVDS_CLK_UPPER	LVDS	LVDS_UCLK	CLKLVDS_U_P
R6612	LVDS_CLK_UPPER	LVDS	LVDS_UCLK	CLKLVDS_U_N
R6613	LVDS_DATA	LVDS	LVDS_L0	LVDS L0_P
R6614	LVDS_DATA	LVDS	LVDS_L0	LVDS L0_N
R6615	LVDS_DATA	LVDS	LVDS_L1	LVDS L1_P
R6616	LVDS_DATA	LVDS	LVDS_L1	LVDS L1_N
R6617	LVDS_DATA	LVDS	LVDS_L2	LVDS L2_P
R6618	LVDS_DATA	LVDS	LVDS_L2	LVDS L2_N
R6619	LVDS_CLK_LOWER	LVDS	LVDS_LCLK	CLKLVDS_L_P
R6620	LVDS_CLK_LOWER	LVDS	LVDS_LCLK	CLKLVDS_L_N
R6621	VGA	VGA		GPU VGA_R
R6622	VGA	VGA		GPU VGA_G
R6623	VGA	VGA		GPU VGA_B
R6624	VGA_CONN	VGA_CONN		VGA_R
R6625	VGA_CONN	VGA_CONN		VGA_G
R6626	VGA_CONN	VGA_CONN		VGA_B
R6627	TV	TV		GPU TV_Y
R6628	TV	TV		GPU TV_C
R6629	TV	TV		GPU TV_COMP
R6630	TV_CONN	TV_CONN		TV_Y
R6631	TV_CONN	TV_CONN		TV_C
R6632	TV_CONN	TV_CONN		TV_COMP



GPU (M11) DVI/DAC Outputs

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SCALE	SIZE	DRAWING NUMBER	REV.
	NONE	D 051-6929	03
SCALE		SHT	OF
NONE		66	115

Page Notes

Power aliases required by this page:
 - =PP3V3_RUN_SI - =PP1V5R3V3_DVO_VREF

Signal aliases required by this page:
 - =SI_TMDS_RESET_L - =RP67xxPy (pinswappable series R)
 - =SI_I2C_CLK
 - =SI_I2C_DATA

BOM options provided by this page:
 - TMDS_EXT - DVO_V15 - DVO_V3V3
 - TMDS_DUAL - DVO_V18

Net Spacing Type: TMDS
 Net Physical Type: TMDS

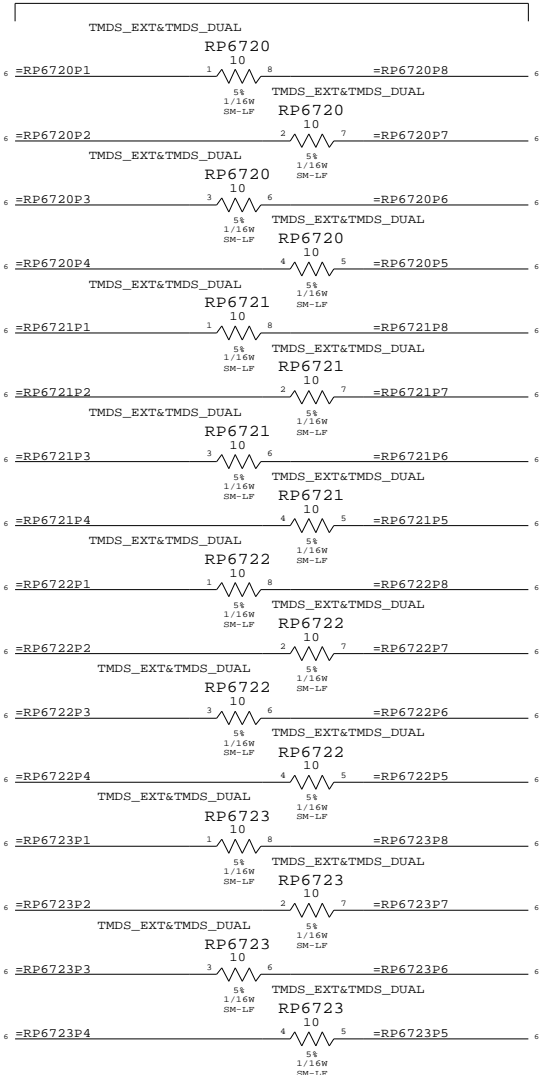
NOTE: Target differential impedance for TMDS data pairs is 100 ohms.

ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
GPU_DVO_LOWER	DVO	DVO	GPU_DVOD<0..11>
GPU_DVO_BOTH	DVO	DVO	GPU_DVO_HSYNC
GPU_DVO_BOTH	DVO	DVO	GPU_DVO_VSYNC
GPU_DVO_BOTH	DVO	DVO	GPU_DVO_DE
GPU_DVO_CLKP	DVO	DVO	GPU_DVO_CLKP
TMDS_CLK	TMDS	TMDS	SI_TMDS_CLK
TMDS_DATA	TMDS	TMDS	SI_TMDS_D0
TMDS_DATA	TMDS	TMDS	SI_TMDS_D1
TMDS_DATA	TMDS	TMDS	SI_TMDS_D2

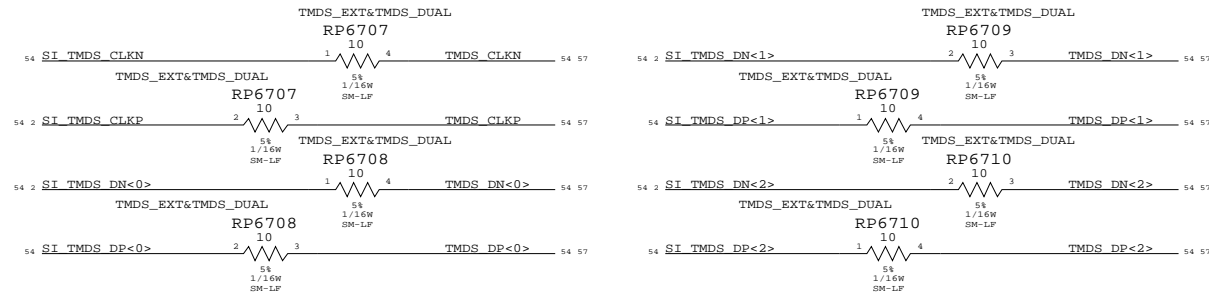
Lower DVO Termination

Place close to GPU

One each for: GPU_DVOD<0..11>
 GPU_DVO_HSYNC
 GPU_DVO_VSYNC
 GPU_DVO_DE
 GPU_DVO_CLKP

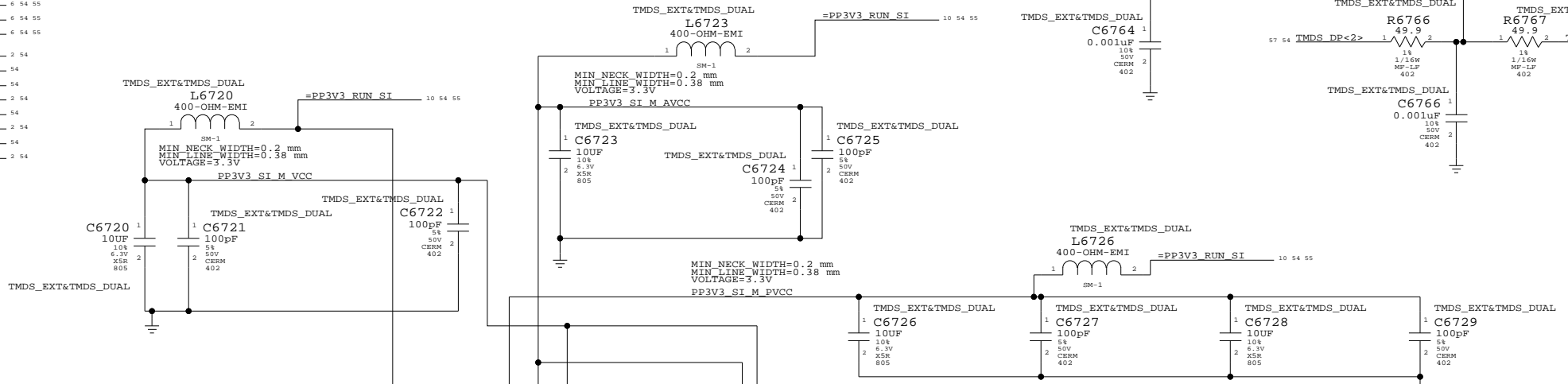
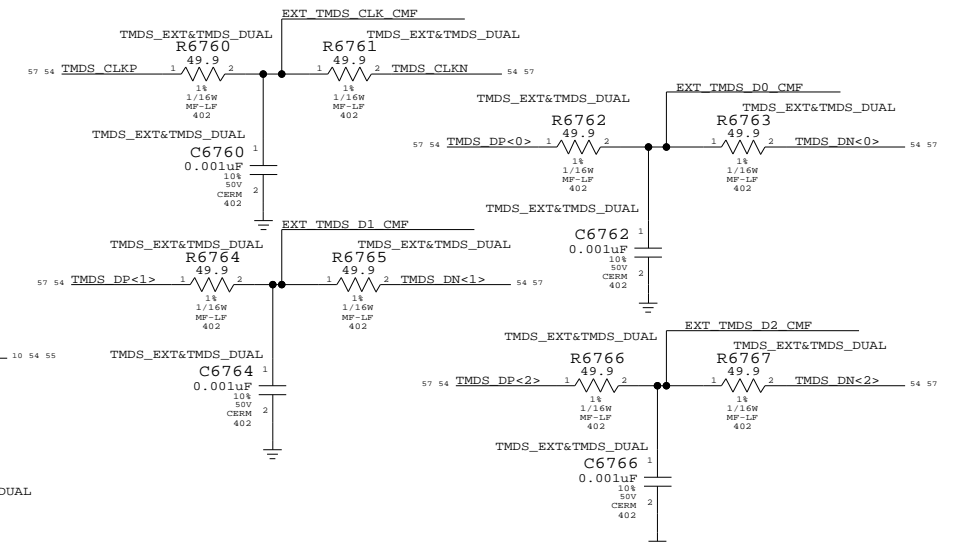


SILICON IMAGE TMDS

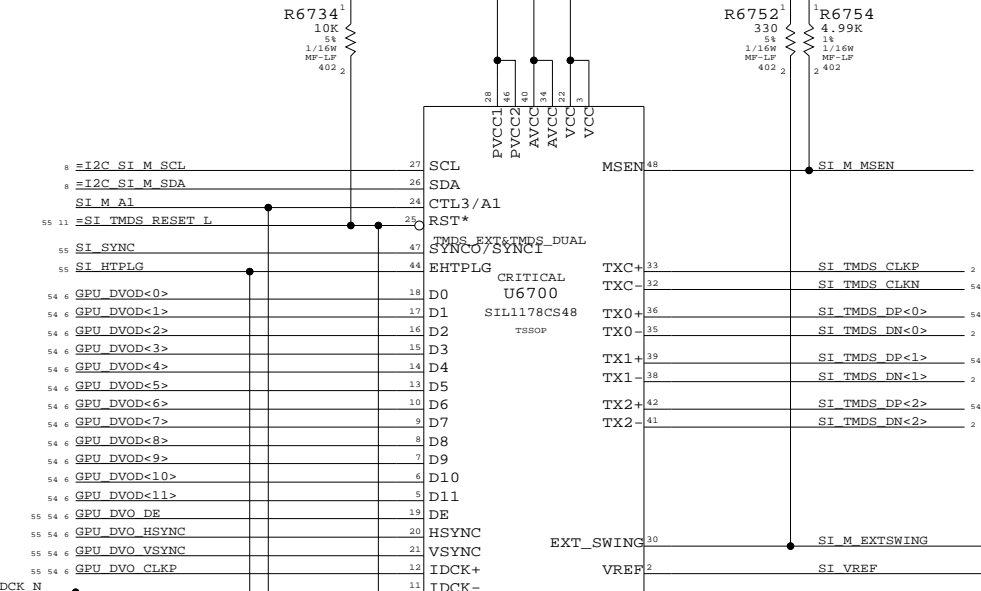


EXTERNAL TMDS TERMINATION

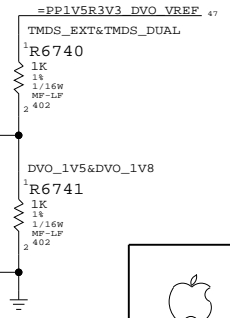
TERMINATION NETWORK SHOULD BE CONNECTED AS SHOWN



ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
TMDS	TMDS	TMDS	TMDS_CLK
TMDS	TMDS	TMDS	TMDS_CLKP
TMDS	TMDS	TMDS	TMDS_D0
TMDS	TMDS	TMDS	TMDS_D0
TMDS	TMDS	TMDS	TMDS_D1
TMDS	TMDS	TMDS	TMDS_D1
TMDS	TMDS	TMDS	TMDS_D2
TMDS	TMDS	TMDS	TMDS_D2



The DVO bus can be run with 3.3V or 1.5V/1.8V signaling. The power rail for the reference should be connected to the GPU DVO rail.



Lower TMDS Transmitter
 SYNC_MASTER=N/A SYNC_DATE=N/A

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SCALE	SHT	OF
NONE	67	115

Page Notes

Power aliases required by this page:
 - =PP3V3_RUN_SI

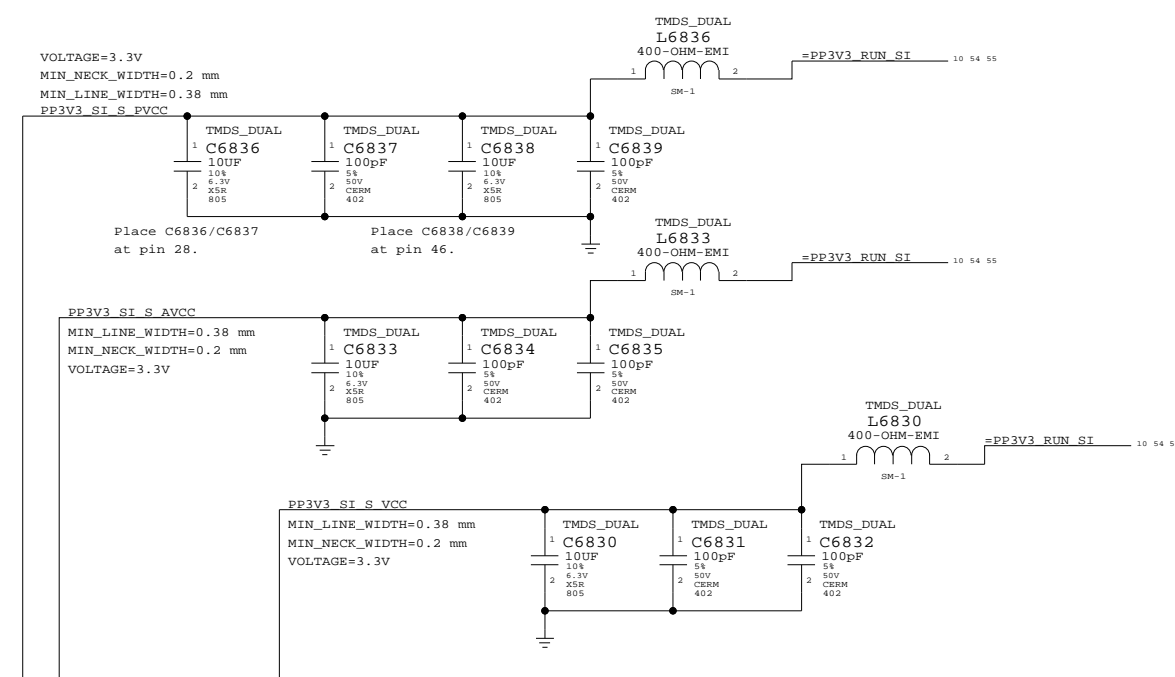
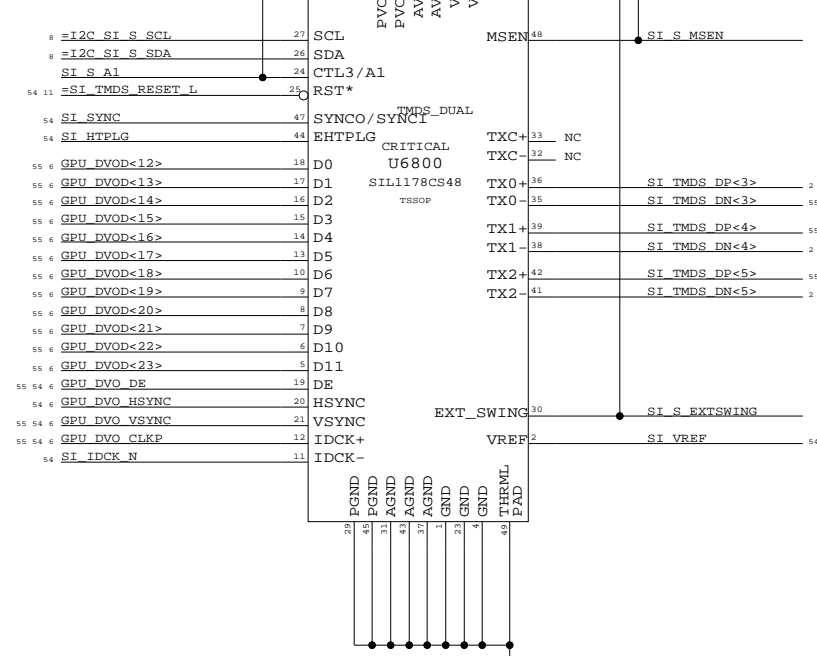
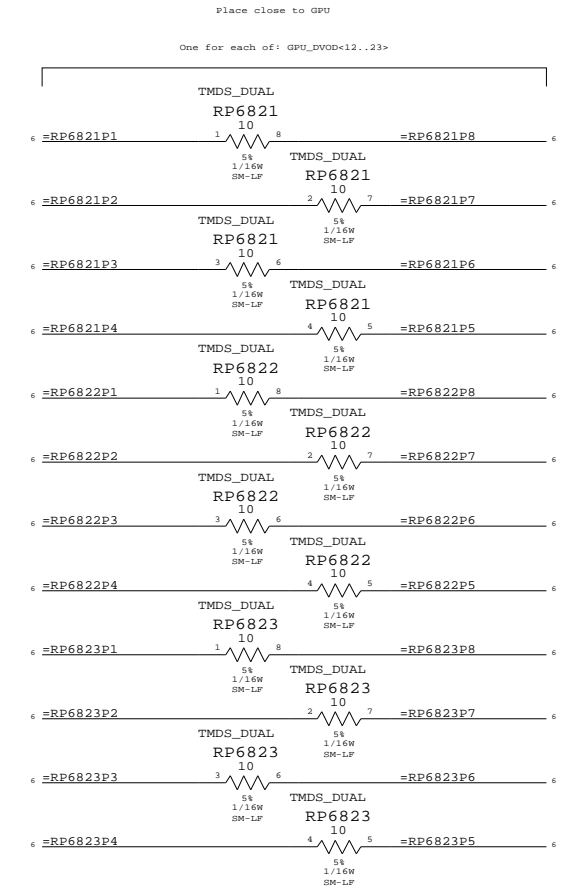
Signal aliases required by this page:
 - =SI_I2C_CLK - =SI_TMDS_RESET_L
 - =SI_I2C_DATA - =RP68xxPy (pin-swappable series R)

BOM options provided by this page:
 - TMDS_DUAL

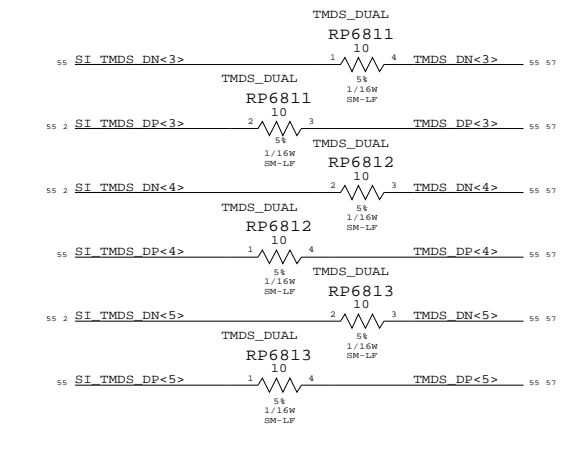
Net Spacing Type: TMDS
 Net Physical Type: TMDS
 NOTE: Target differential impedance for TMDS data pairs is 100 ohms.

ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
GPU_DVO_UPPER	DVO	DVO	
GPU_DVOD20	DVO	DVO	
GPU_DVO_UPPER	DVO	DVO	
GPU_DVO_VSYNC	PROVIDED BY LOWER TXMR		
GPU_DVO_DE	PROVIDED BY LOWER TXMR		
GPU_DVO_CLKP	PROVIDED BY LOWER TXMR		
TMDS_DATA	TMDS	TMDS	SI_TMDS_D3
TMDS_DATA	TMDS	TMDS	SI_TMDS_D3
TMDS_DATA	TMDS	TMDS	SI_TMDS_D4
TMDS_DATA	TMDS	TMDS	SI_TMDS_D4
TMDS_DATA	TMDS	TMDS	SI_TMDS_D5
TMDS_DATA	TMDS	TMDS	SI_TMDS_D5
TMDS_D3	TMDS	TMDS	TMDS_D3
TMDS_D3	TMDS	TMDS	TMDS_D3
TMDS_D4	TMDS	TMDS	TMDS_D4
TMDS_D4	TMDS	TMDS	TMDS_D4
TMDS_D5	TMDS	TMDS	TMDS_D5
TMDS_D5	TMDS	TMDS	TMDS_D5

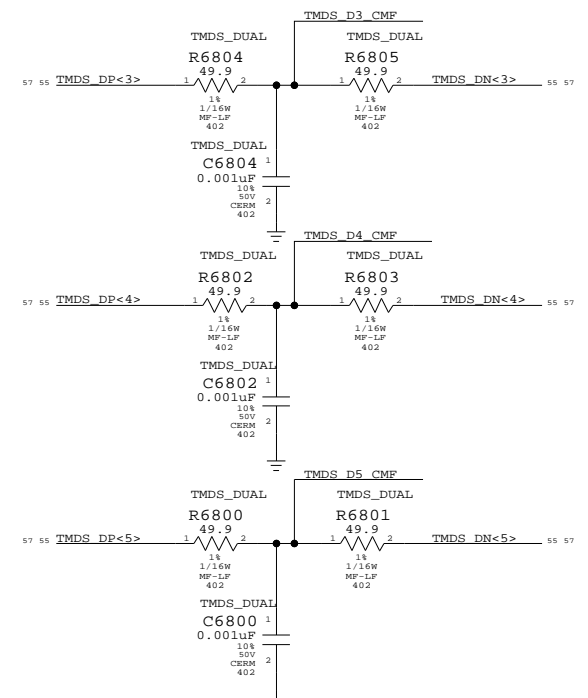
Upper DVO series termination



Upper Channel Series Termination



Upper Channel Common-mode Termination



Upper TMDS Transmitter

SYNC_MASTER=N/A SYNC_DATE=N/A

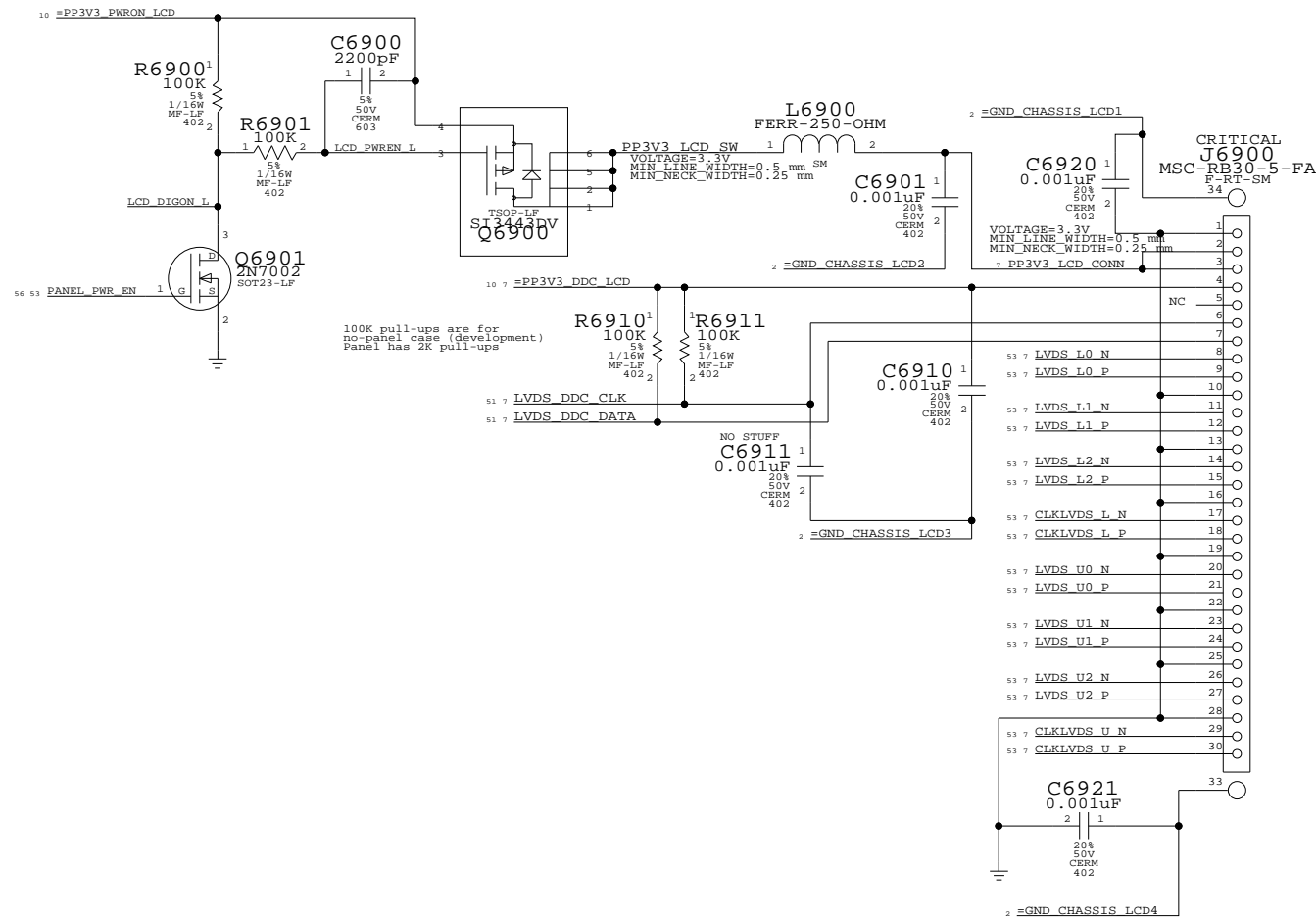
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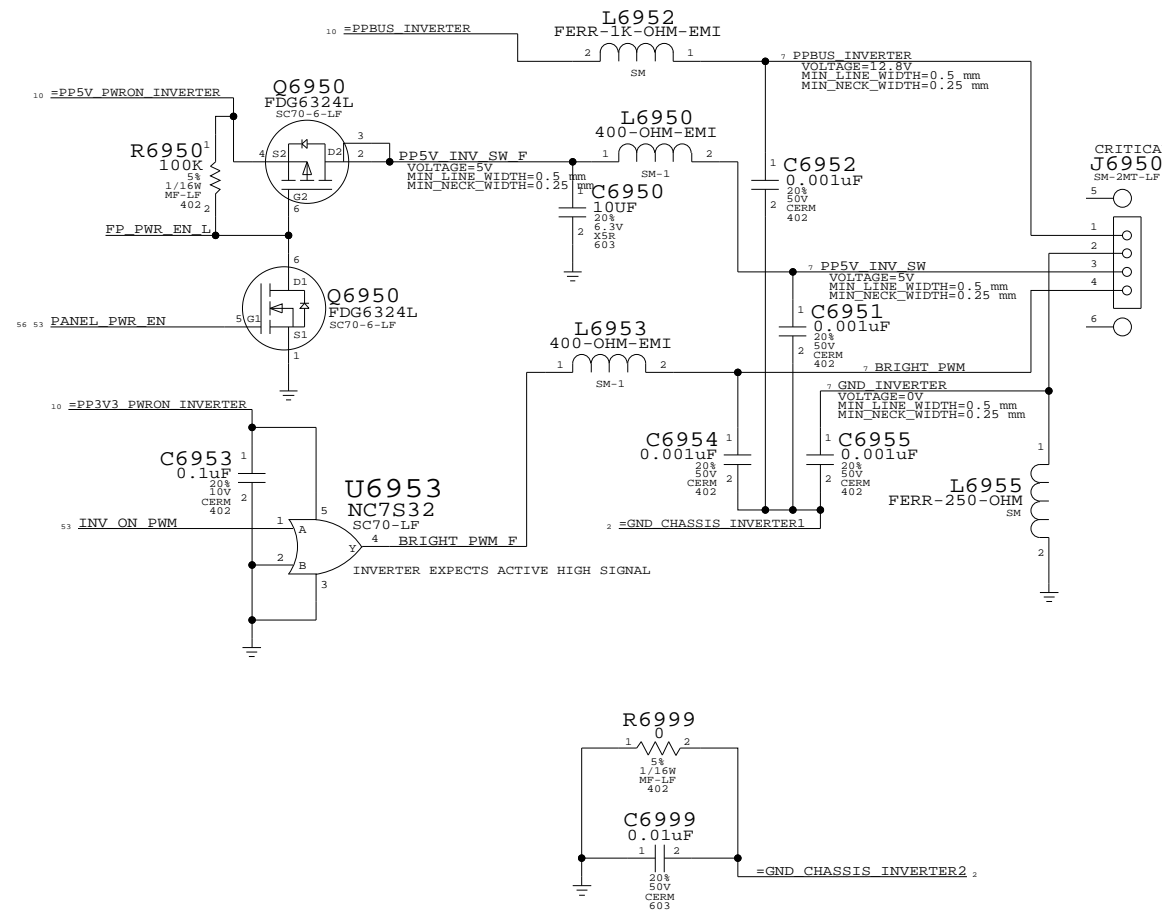
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LCD (LVDS) INTERFACE



INVERTER INTERFACE



Internal Display Conns

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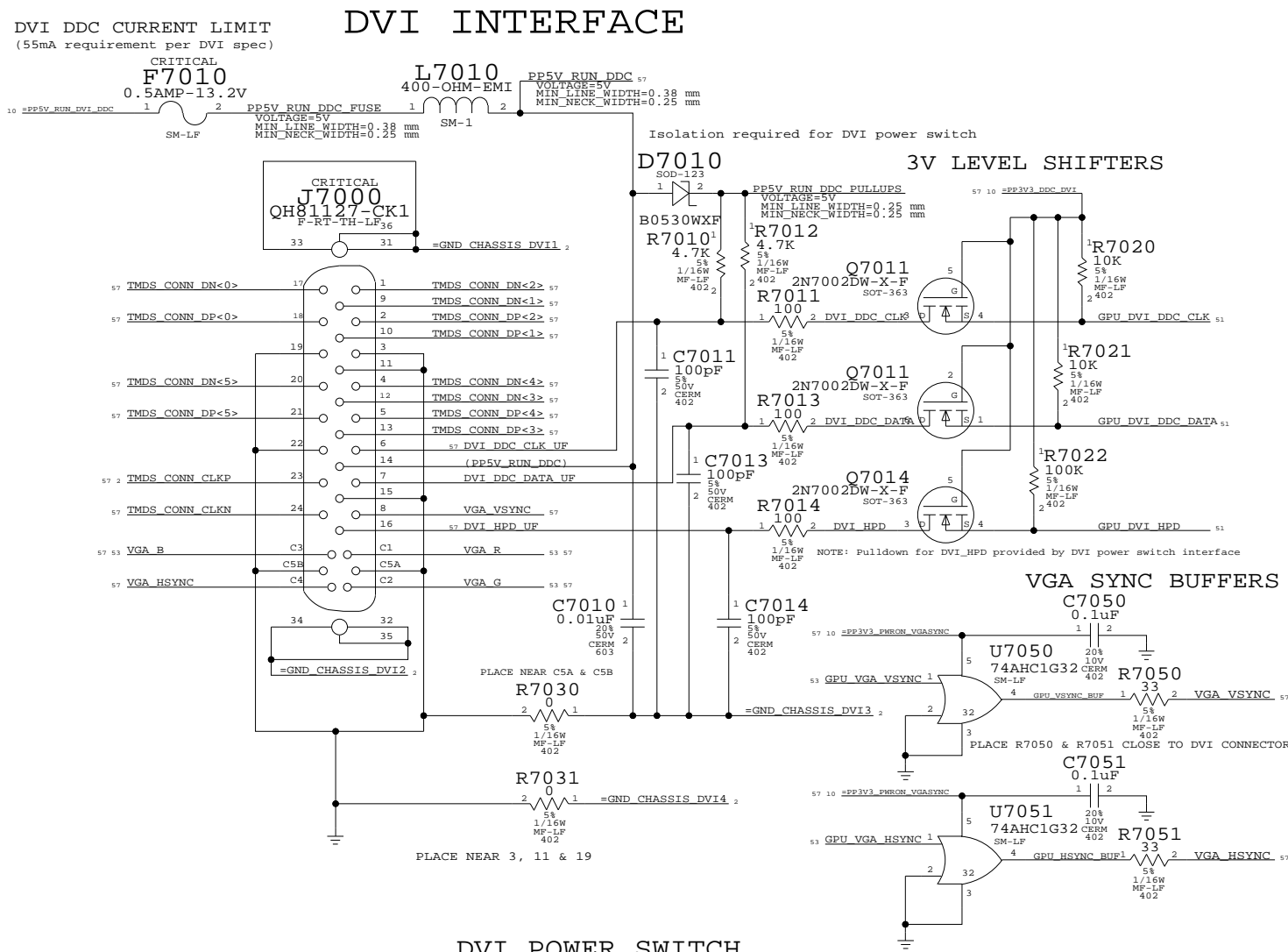
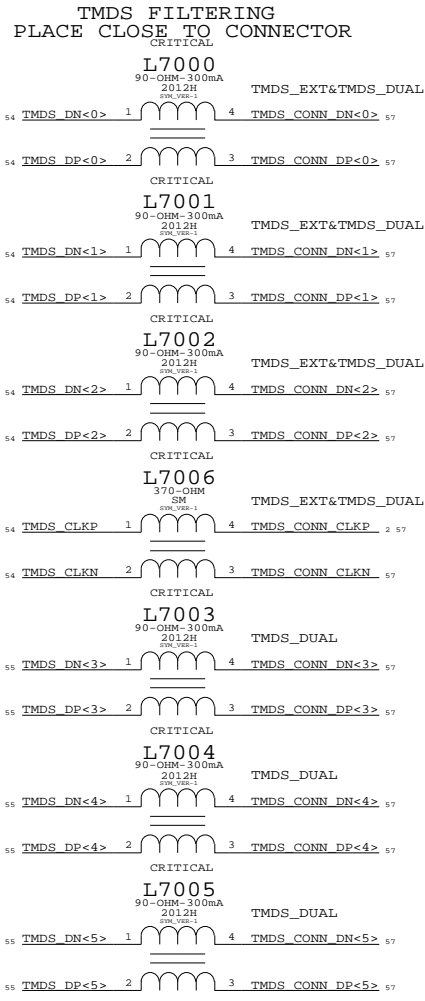
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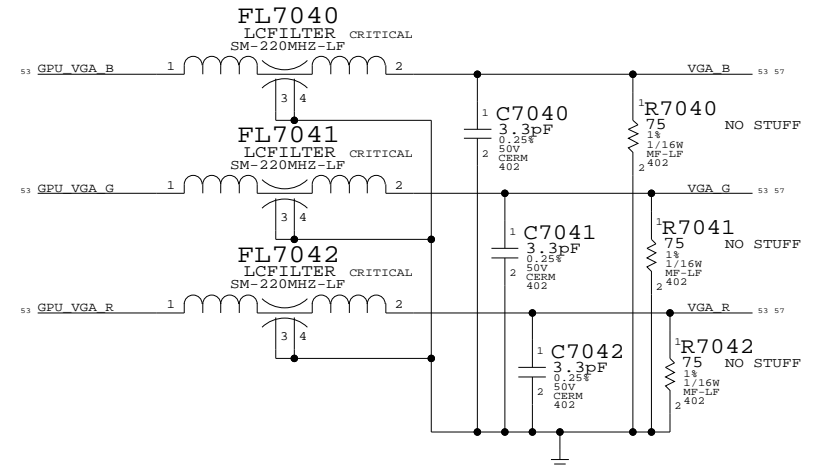
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6929	03
SCALE	NONE	SHT OF	69 OF 115

ELECTRICAL_CONSTRAINT_SET	NET_TYPE	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
E540	TMDS_CONN_TMDS_CONN		TMDS_CONN_CLK	TMDS_CONN_CLK
E540	TMDS_CONN_TMDS_CONN		TMDS_CONN_CLKN	TMDS_CONN_CLKN
E540	TMDS_CONN_TMDS_CONN		TMDS_CONN_D0	TMDS_CONN_DP<0>
E540	TMDS_CONN_TMDS_CONN		TMDS_CONN_D0	TMDS_CONN_DN<0>
E540	TMDS_CONN_TMDS_CONN		TMDS_CONN_D1	TMDS_CONN_DP<1>
E540	TMDS_CONN_TMDS_CONN		TMDS_CONN_D1	TMDS_CONN_DN<1>
E540	TMDS_CONN_TMDS_CONN		TMDS_CONN_D2	TMDS_CONN_DP<2>
E540	TMDS_CONN_TMDS_CONN		TMDS_CONN_D2	TMDS_CONN_DN<2>
E540	TMDS_CONN_TMDS_CONN		TMDS_CONN_D3	TMDS_CONN_DP<3>
E540	TMDS_CONN_TMDS_CONN		TMDS_CONN_D3	TMDS_CONN_DN<3>
E540	TMDS_CONN_TMDS_CONN		TMDS_CONN_D4	TMDS_CONN_DP<4>
E540	TMDS_CONN_TMDS_CONN		TMDS_CONN_D4	TMDS_CONN_DN<4>
E540	TMDS_CONN_TMDS_CONN		TMDS_CONN_D5	TMDS_CONN_DP<5>
E540	TMDS_CONN_TMDS_CONN		TMDS_CONN_D5	TMDS_CONN_DN<5>

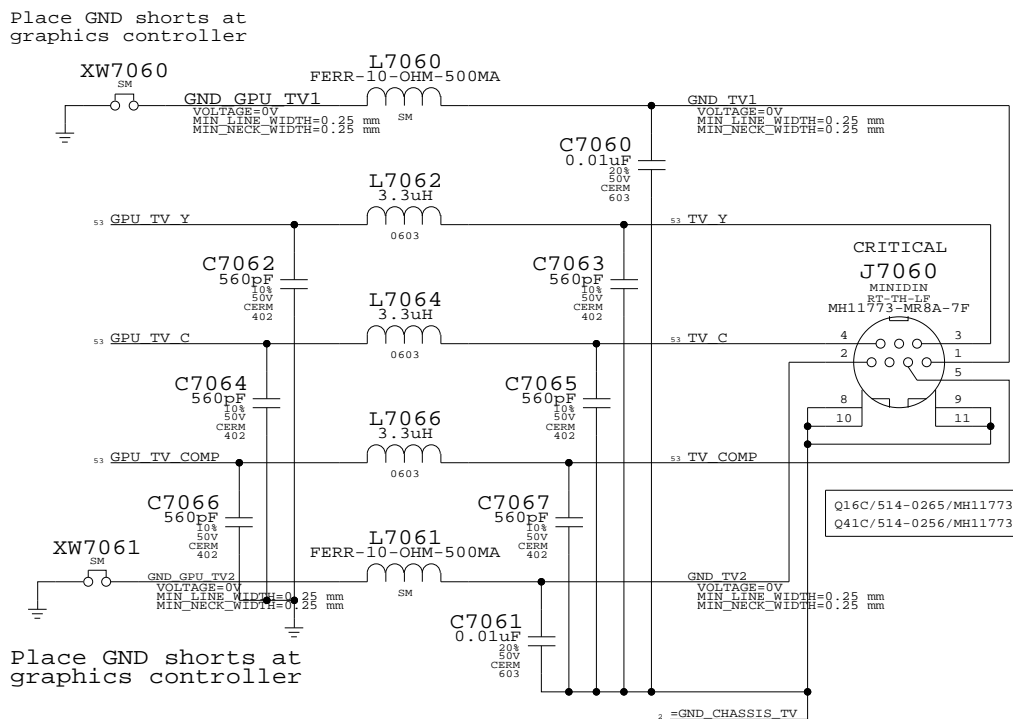


ANALOG FILTERING

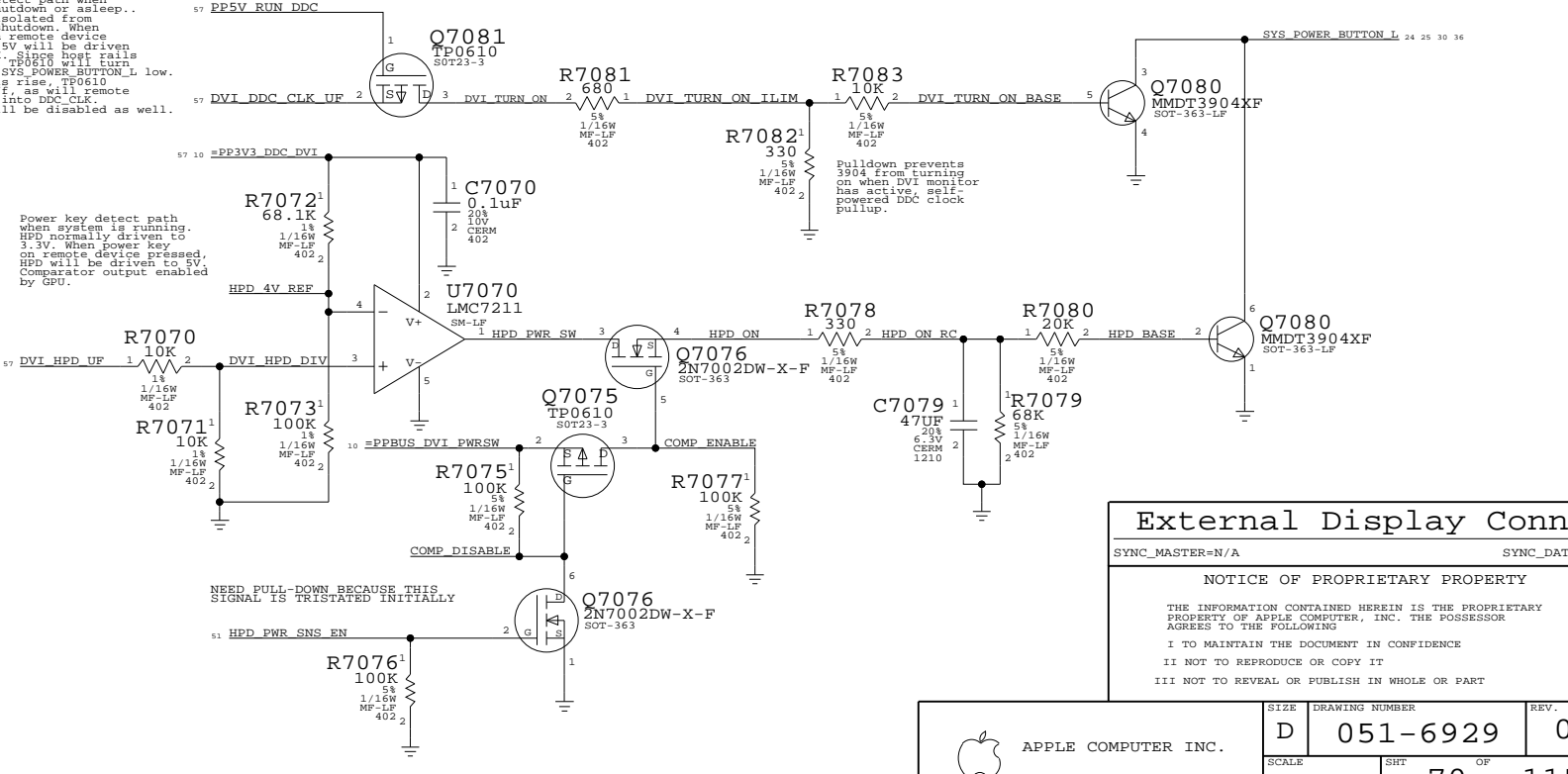
PLACE CLOSE TO CONNECTOR



S-VIDEO/COMP OUT INTERFACE



Power key detect path when system is shutdown or asleep... DDC CLK is isolated from GPU during shutdown. When power key on, remote device is pressed, 5V will be driven into DDC CLK. Stand by rail will be low. TP0610 will turn on, driving SYS_POWER_BUTTON_L low. As host rails rise, TP0610 will turn off, as will remote device path into DDC CLK. Isolation will be disabled as well.



External Display Conns

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6929	03
SCALE	SHT	OF	
NONE	70	115	

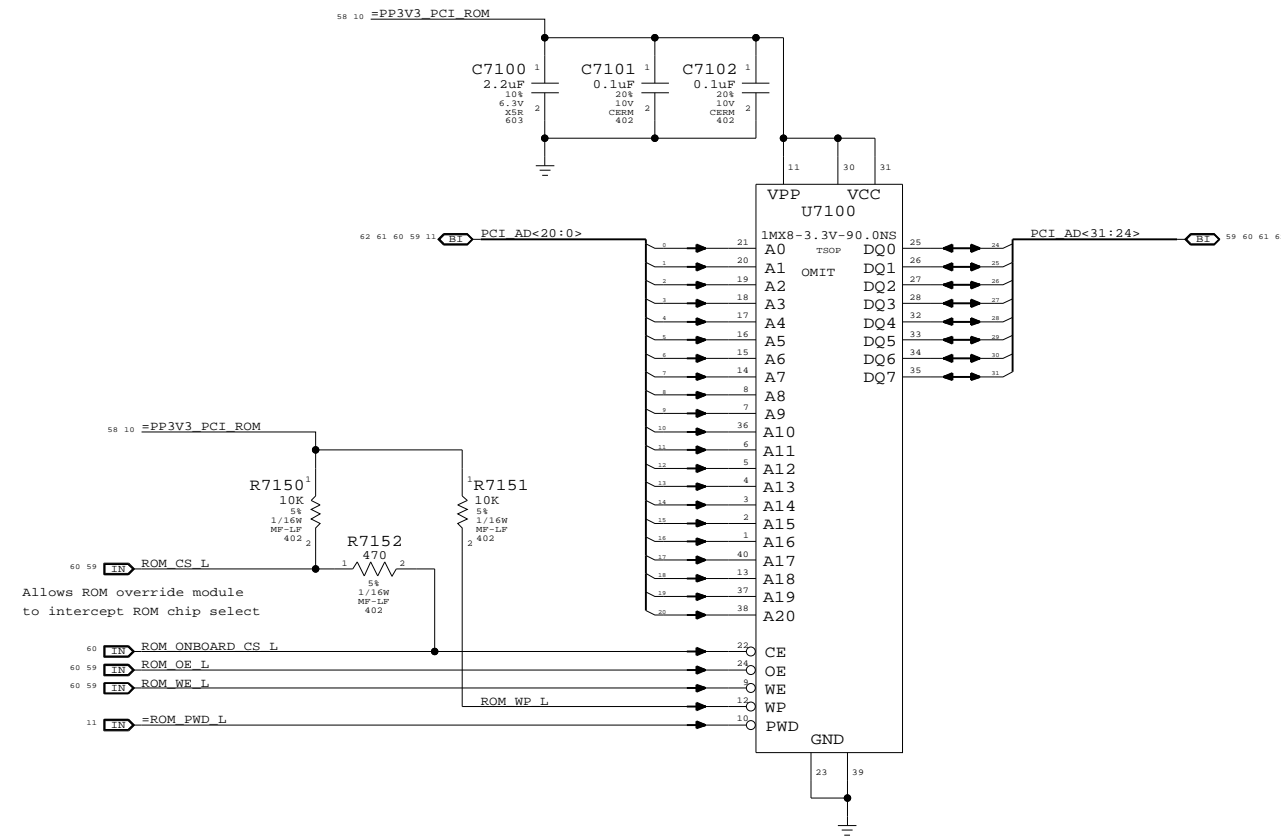
Page Notes

Power aliases required by this page:
 - =PP3V3_PCI_ROM

Signal aliases required by this page:
 - =ROM_PWD_L

BOM options provided by this page:
 (NONE)

NOTE: This page does not specify a BootROM part number. Must use a TABLE_X_ITEM symbol to declare U7100 part number.



BootROM

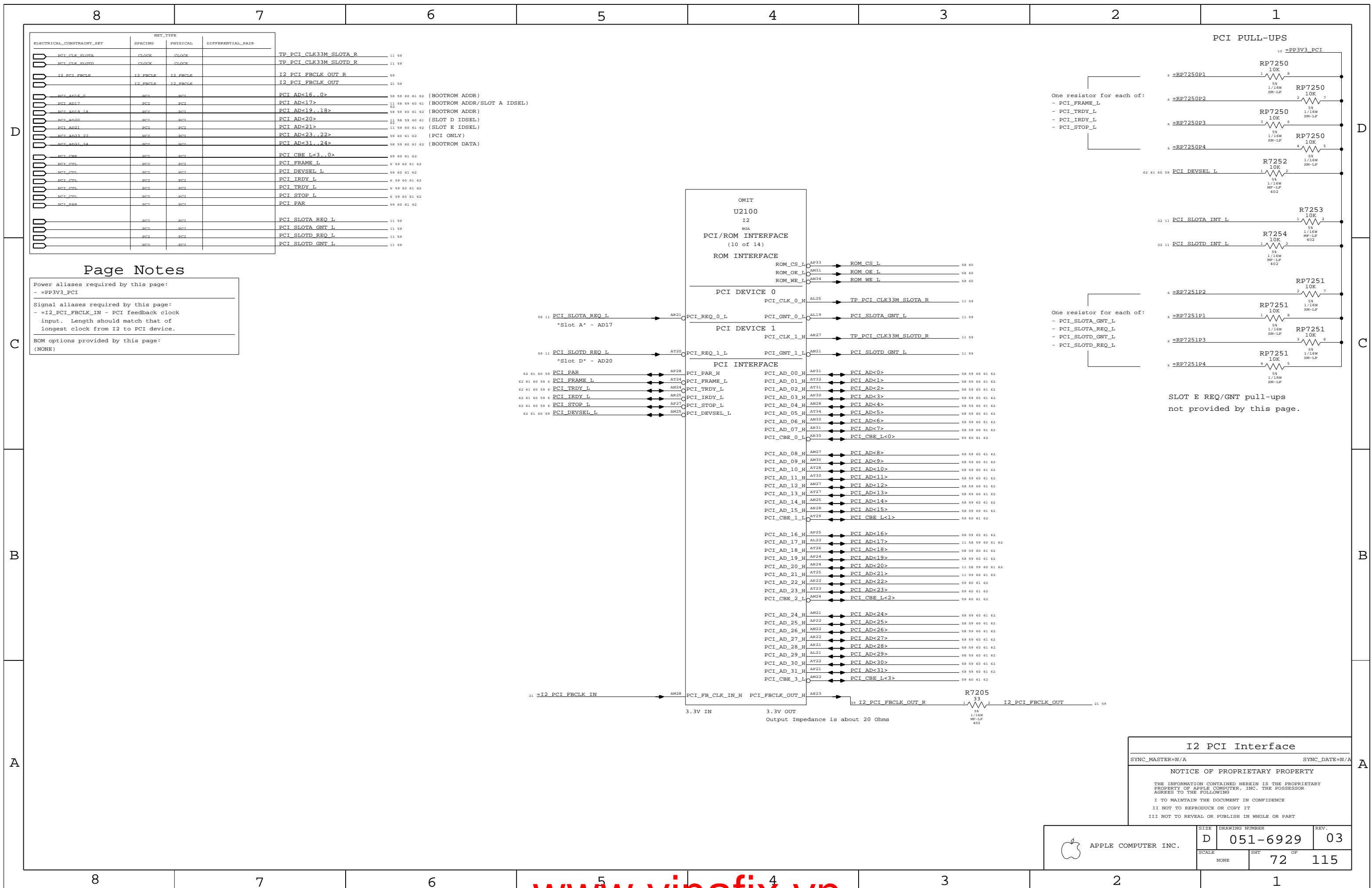
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	D	051-6929	03
SCALE	SHT OF		
NONE	71 OF		115



Page Notes

Power aliases required by this page:
 - =PP3V3_PCI

Signal aliases required by this page:
 - =I2_PCI_FBCLK_IN - PCI feedback clock input. Length should match that of longest clock from I2 to PCI device.

BOM options provided by this page:
 (NONE)

I2 PCI Interface

SYNC_MASTER=N/A SYNC_DATE=N/A

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	D	051-6929	03
SCALE	SHT	OF	
NONE	72	115	

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		DIFFERENTIAL_PAIR
	SPACING	PHYSICAL	
MEM	CLOCK	CLOCK	

=PCI_CLK33M_AIRPORT 11 60

Page Notes

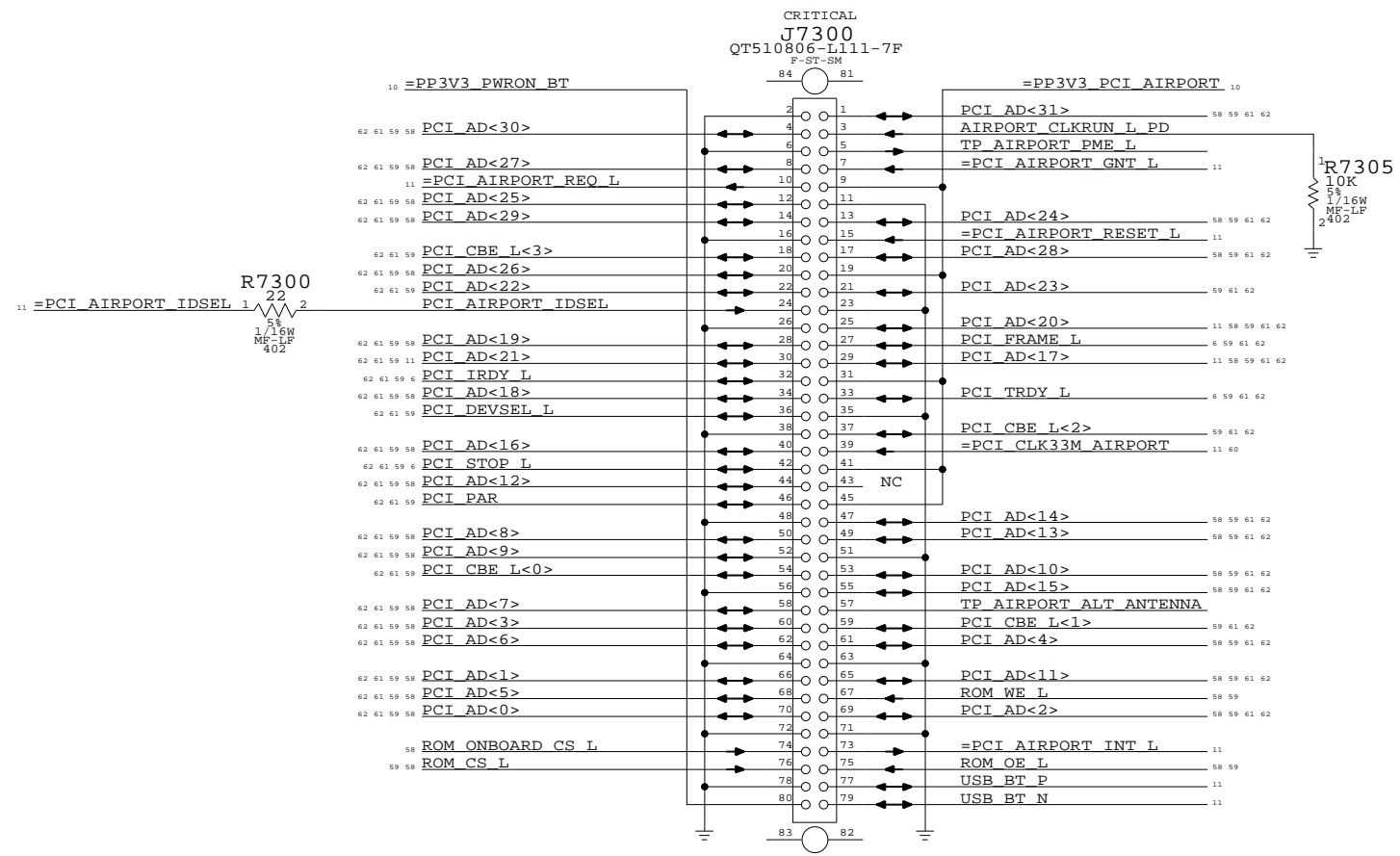
Power aliases required by this page:
 - =PP3V3_PCI (802.11g Power)
 - =PP3V3_PWRON_BT (Bluetooth Power)

Signal aliases required by this page:
 - =PCI_CLK33M_AIRPORT (33MHz PCI clock)
 - =PCI_AIRPORT_RESET_L (PCI Reset)
 - =USB_BT_P (Bluetooth USB D+)
 - =USB_BT_N (Bluetooth USB D-)

BOM options provided by this page:
 (NONE)

PCI Devices implemented on this page:
 ADL7 (Slot "A") - AirPort (0x????/0x????)

NOTE: This AirPort implementation does not support PME#.



Q85 Connector
 Q16C/516S0361/F-ST-SM
 Q41C/516S0352/M-ST-SM-LF

Q85 Airport/BT Connector

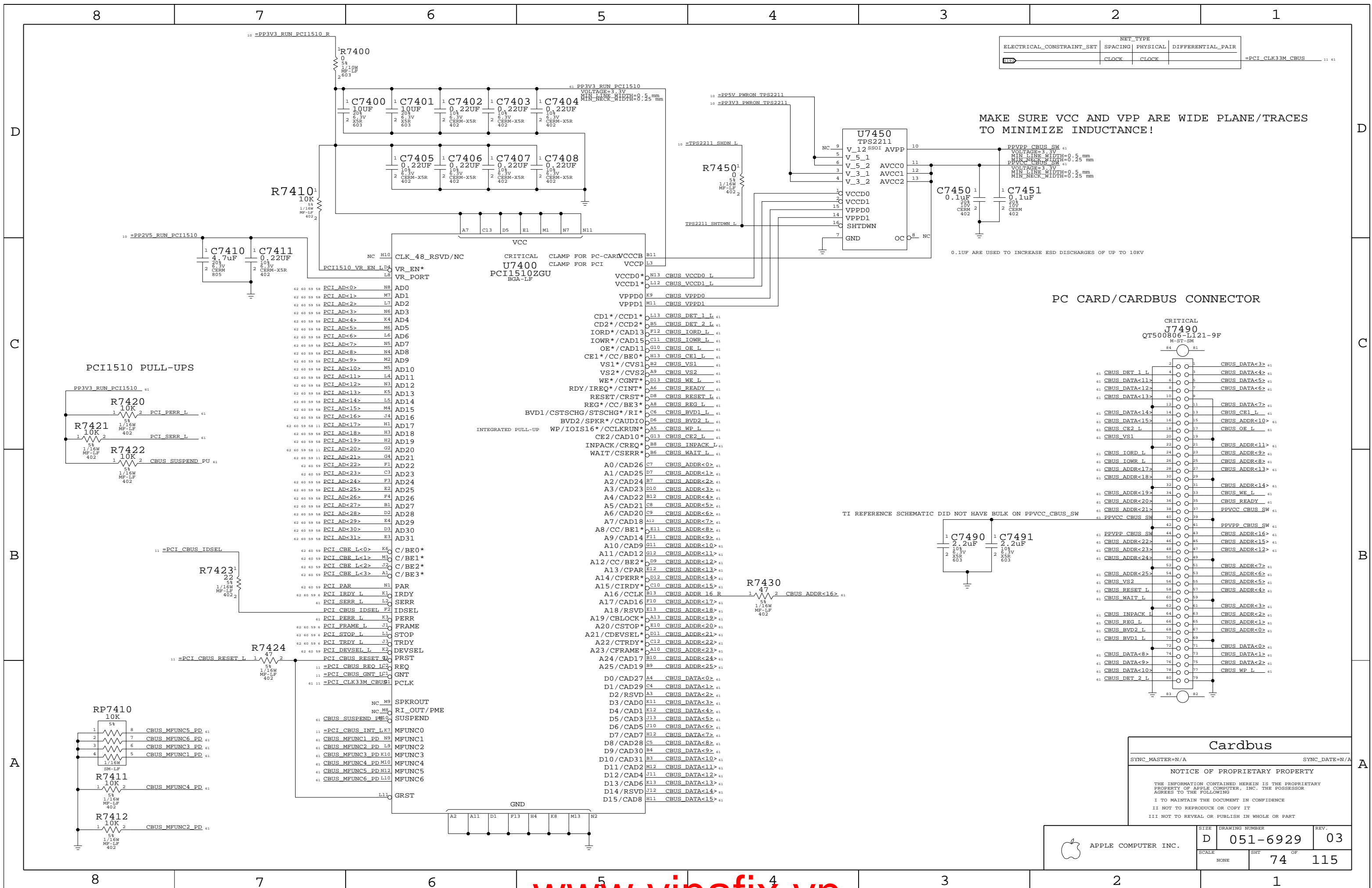
SYNC_MASTER=N/A SYNC_DATE=N/A

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	D	051-6929	03
SCALE	NONE	SHT OF	73 OF 115



ELECTRICAL_CONSTRAINT_SET	NET_TYPE		DIFFERENTIAL_PAIR
	SPACING	PHYSICAL	
	CLOCK	CLOCK	

=PCI_CLK33M_USB2 11 62

Page Notes

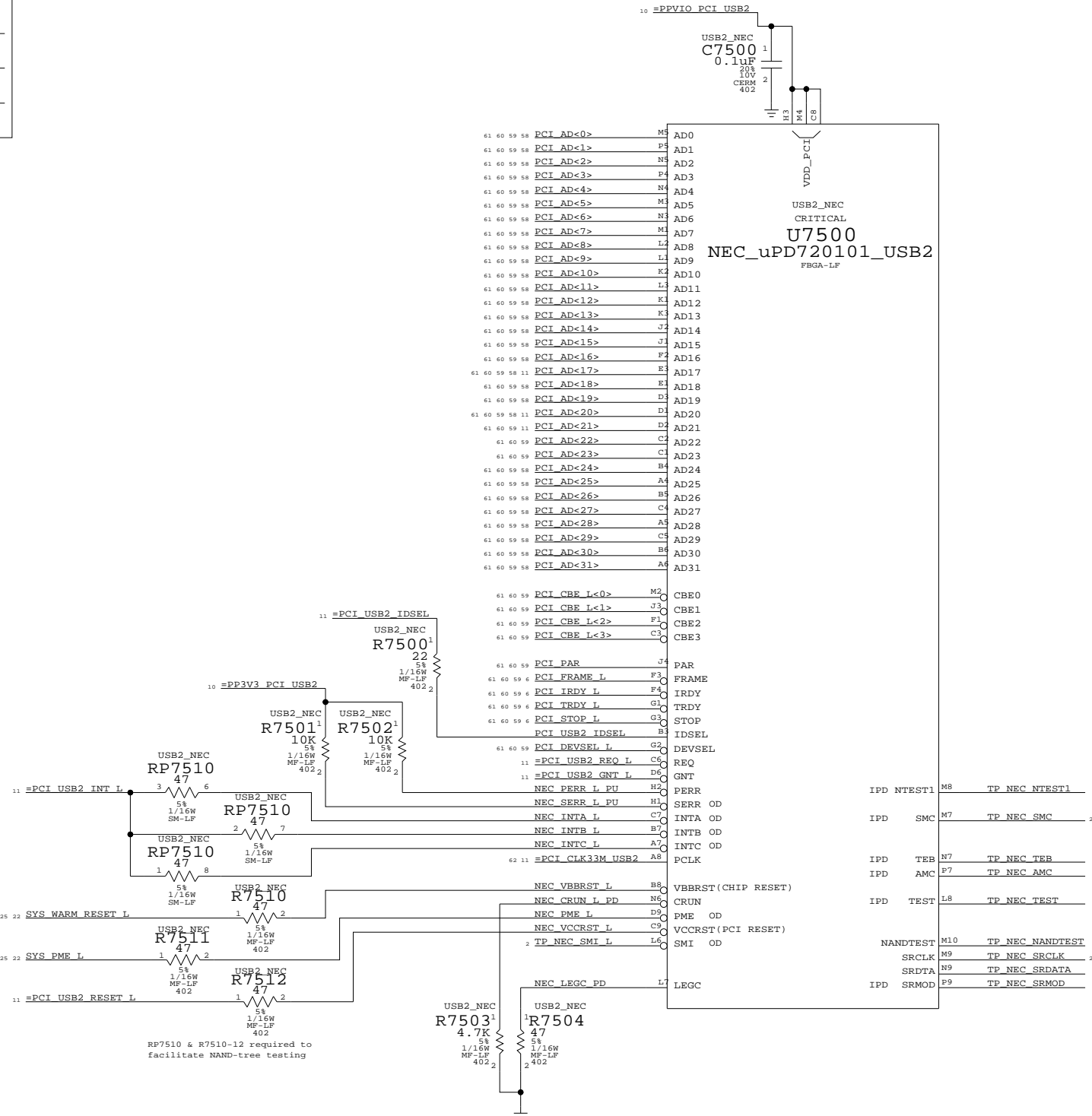
Power aliases required by this page:
 - =PPVIO_PCI (to 3.3V or 5V)
 - =PP3V3_PCI_USB2 (D3cold rail)

Signal aliases required by this page:
 - =PCI_CLK33M_USB2
 - =PCI_USB2_REQ_L - =PCI_USB2_IDSEL
 - =PCI_USB2_GNT_L - =PCI_USB2_RESET_L
 - =PCI_USB2_INT_L

BOM options provided by this page:
 - USB2_NEC

PCI Devices implemented on this page:
 AD27 (Slot "G") - USB2 (0x1033/0x0035)

NOTE: This USB2 implementation supports D3cold.



NEC USB2

SYNC_MASTER=N/A SYNC_DATE=N/A

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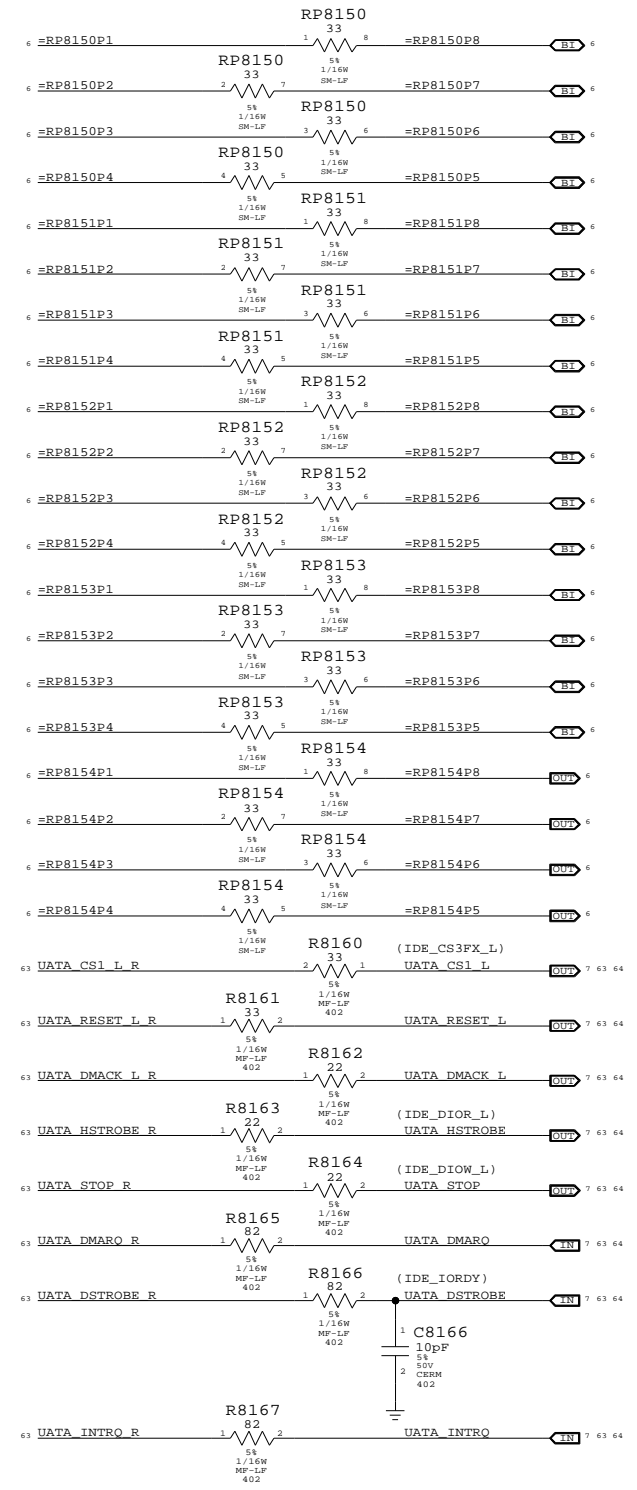
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	D	051-6929	03
SCALE	SHEET OF		
NONE	75 OF 115		

ELECTRICAL_CONSTRAINT_SET	NET_TYPE				
	SPACING	PHYSICAL	DIFFERENTIAL_PAIR		
UATA_DD R<15..8>	DATA	DATA		2 6 63	
UATA_DD R<7>	DATA	DATA		6 63	
UATA_DD R<6..0>	DATA	DATA		2 6 63	
UATA_DA R<2..0>	DATA	DATA		2 6 63	
UATA_CS0 L R	DATA	DATA		6 63	
UATA_CS1 L R	DATA	DATA		63	
UATA_HSTROBE R	DATA	DATA		63	
UATA_STOP R	DATA	DATA		63	
UATA_DMACK L R	DATA	DATA		63	
UATA_RESET L R	DATA	DATA		63	
UATA_DSTROBE R	DATA	DATA		63	
UATA_DMARQ R	DATA	DATA		63	
UATA_INTRO R	DATA	DATA		63	
UATA_DD<15..0>	DATA	DATA		6 7 64	
UATA_DA<2..0>	DATA	DATA		6 7 64	
UATA_CS0 L	DATA	DATA		6 7 64	
UATA_CS1 L	DATA	DATA		7 63 64	
UATA_HSTROBE	DATA	DATA		7 63 64	
UATA_STOP	DATA	DATA		7 63 64	
UATA_DMACK L	DATA	DATA		7 63 64	
UATA_RESET L	DATA	DATA		7 63 64	
UATA_DSTROBE	DATA	DATA		7 63 64	
UATA_DMARQ	DATA	DATA		7 63 64	
UATA_INTRO	DATA	DATA		7 63 64	

UATA100 SERIES TERMINATION

PLACE CLOSE TO I2



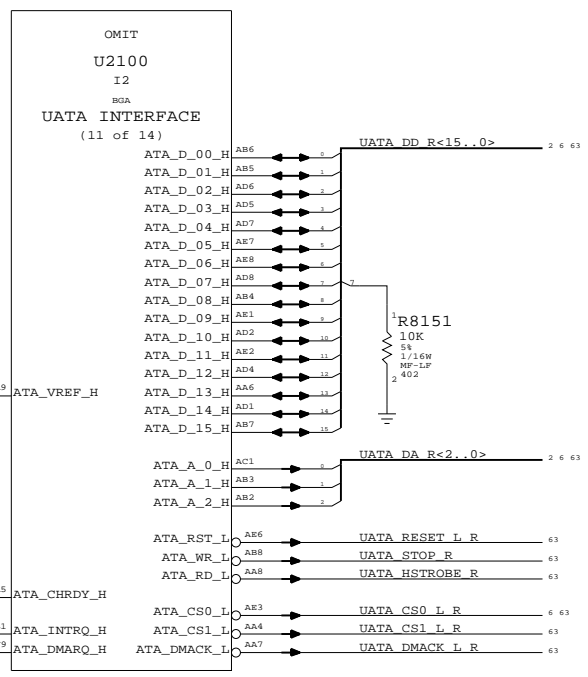
One resistor for each of:
 - UATA_DD<15..0>(_R)
 - UATA_DA<2..0>(_R)
 - UATA_CS0 L(_R)
 (IDE_CS1FX_L)

Page Notes

Power aliases required by this page:
 (NONE)

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)



I2 UATA Interface

SYNC_MASTER=N/A SYNC_DATE=N/A

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SCALE	NONE	SHT	OF
		81	115

D

D

C

C

B

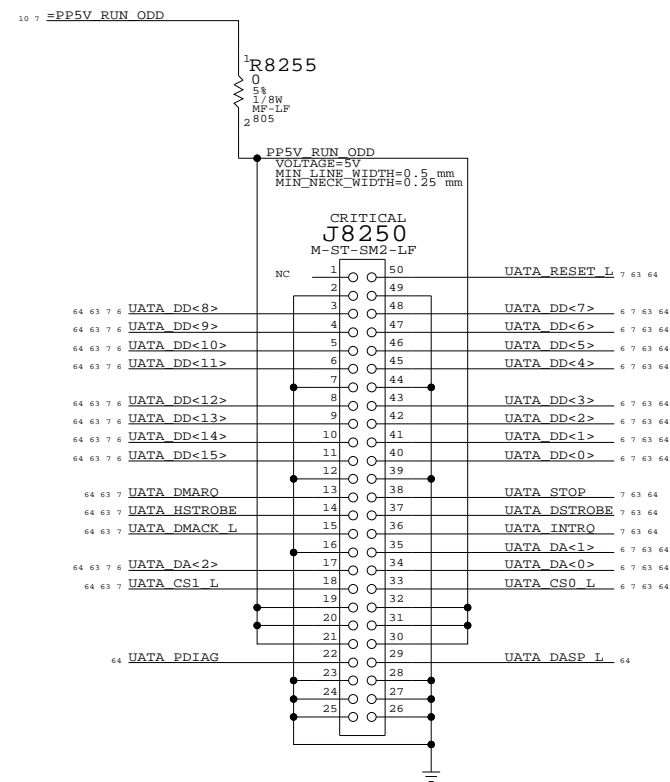
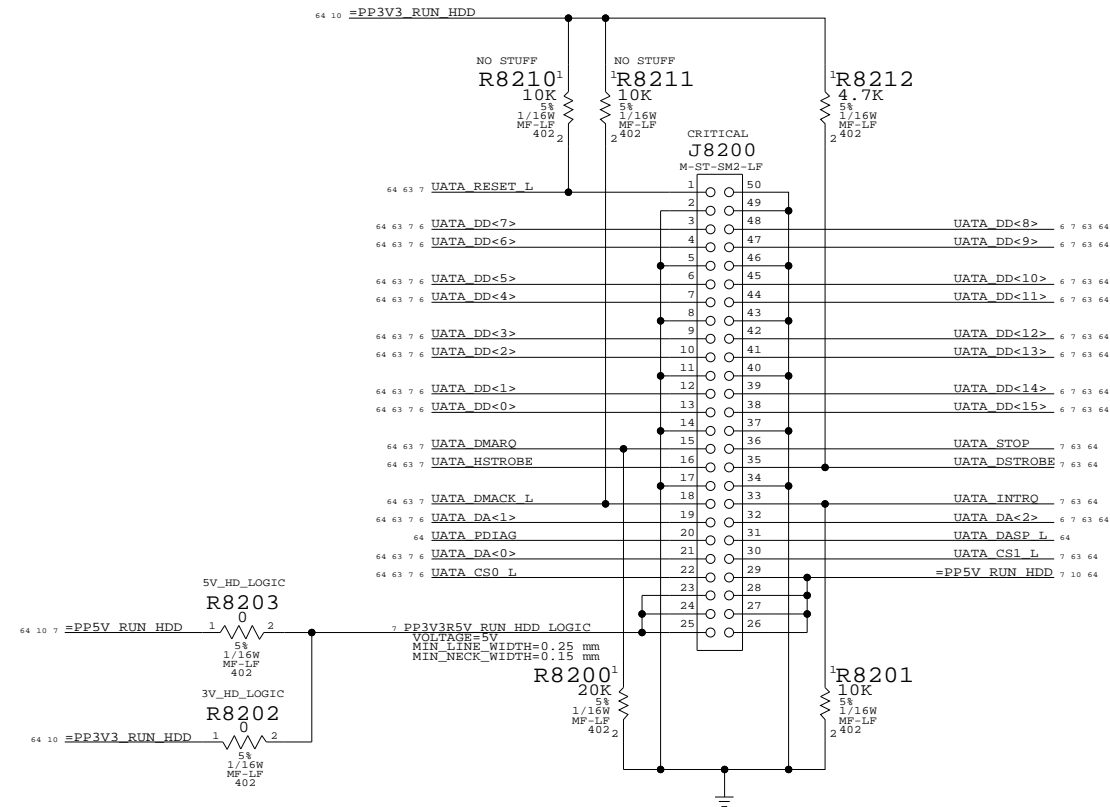
B

A

A

HDD CONNECTOR

ODD CONNECTOR



ATA Connectors
 Q16C/516S0357/M-ST-SM2-LF
 Q41C/516S0335/M-ST-SM1-LF

HDD/ODD Connectors
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	D	051-6929	03
SCALE	SHT OF		
NONE	82		115

ELECTRICAL_CONSTRAINT_SET	NET_TYPE	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
ENET_RX_CLK25M	CLOCK	CLOCK		
ENET_RX_CLK125M	CLOCK	CLOCK		
ENET_GBE_REF	CLOCK	CLOCK		
ENET_TX_CLK	CLOCK	CLOCK		
ENET_RXD<0>	ENET			
ENET_RXD<1>	ENET			
ENET_RXD<2>	ENET			
ENET_RXD<3>	ENET			
ENET_RXD<4>	ENET			
ENET_RXD<5>	ENET			
ENET_RXD<6>	ENET			
ENET_RXD<7>	ENET			
ENET_RX_DV	ENET			
ENET_RX_ER	ENET			
ENET_TXD<0>	ENET			
ENET_TXD<1>	ENET			
ENET_TXD<2>	ENET			
ENET_TXD<3>	ENET			
ENET_TXD<4>	ENET			
ENET_TXD<5>	ENET			
ENET_TXD<6>	ENET			
ENET_TXD<7>	ENET			
ENET_TX_EN_R	ENET			
ENET_TX_ER_R	ENET			
ENET_COL	ENET			
ENET_CR_S	ENET			
ENET_MDC	ENET			
ENET_MDIO	ENET			

Page Notes

Power aliases required by this page:
 - =PP2V5R3V3_PWRON_I2_ENET

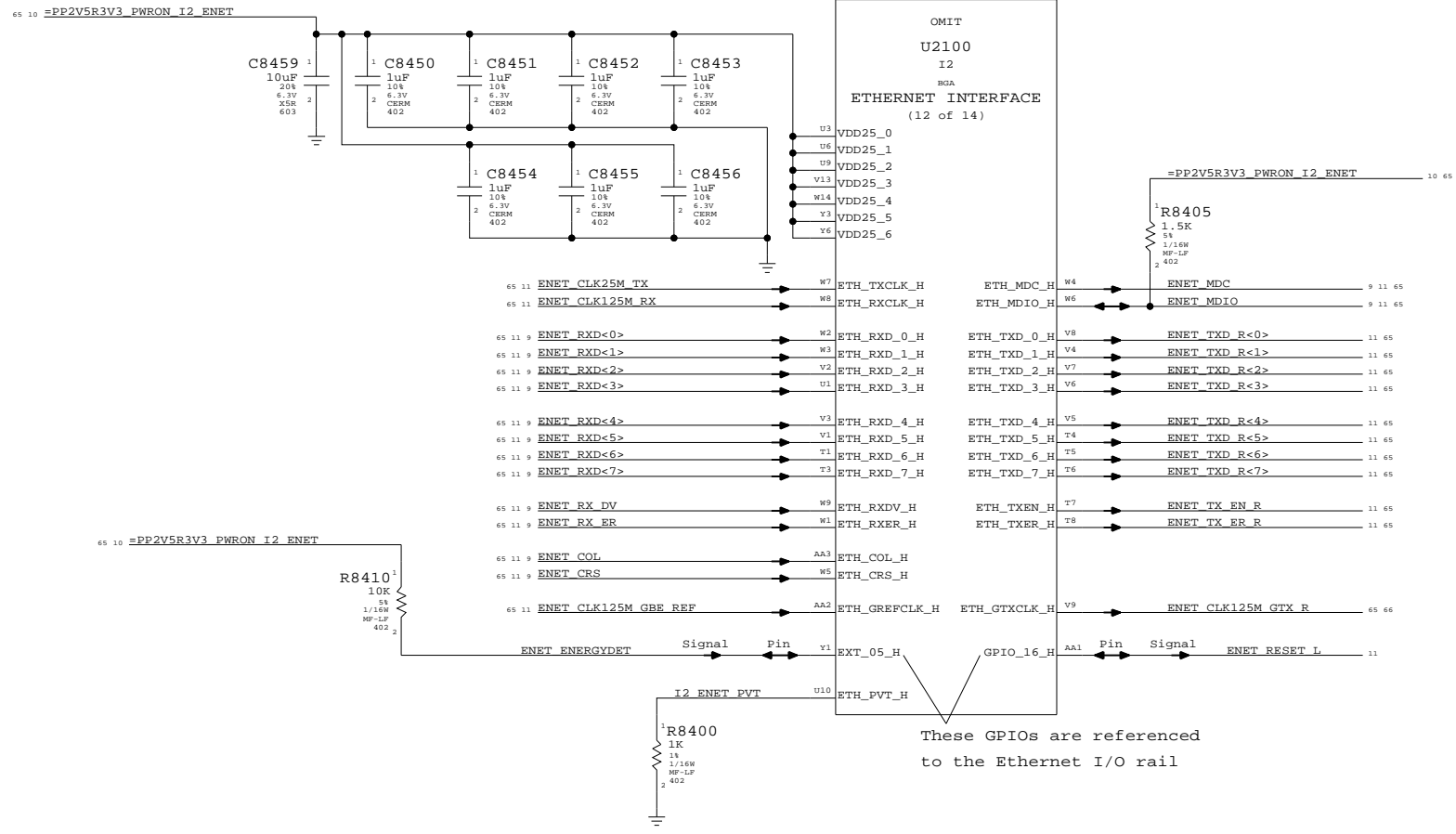
Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

NOTE: This page does not provide any series termination. Any termination, including clock signals, should be provided by the PHY page or a non-shared schematic page.

NOTE: All I2 GPIOs should have a pull-up or pull-down resistor. This page does not provide a resistor for GPIO 16. It must be provided by the PHY page or a non-shared schematic page.

NOTE: ENET_RX_DV has a hold spec violation on I2. May want to lengthen net by -250ps. Net has a unique ECSet name to allow this.



These GPIOs are referenced to the Ethernet I/O rail

I2 Ethernet Interface
 SYNC_MASTER=N/A SYNC_DATE=N/A

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	D	051-6929	03
SCALE	NONE	SHT	OF
		84	115

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
[Symbol]	CLOCK	CLOCK	
[Symbol]	CLOCK	CLOCK	
[Symbol]	CLOCK	CLOCK	
[Symbol]	ENETCONN	ENETCONN	ENETCONN_0
[Symbol]	ENETCONN	ENETCONN	ENETCONN_0
[Symbol]	ENETCONN	ENETCONN	ENETCONN_1
[Symbol]	ENETCONN	ENETCONN	ENETCONN_1
[Symbol]	ENETCONN	ENETCONN	ENETCONN_2
[Symbol]	ENETCONN	ENETCONN	ENETCONN_2
[Symbol]	ENETCONN	ENETCONN	ENETCONN_3
[Symbol]	ENETCONN	ENETCONN	ENETCONN_3
[Symbol]	VESTA_CLK25M_XTAL	XTAL	XTAL
[Symbol]	XTAL	XTAL	
[Symbol]	XTAL	XTAL	

Page Notes

Power aliases required by this page:
 - =PP2V5_ENETFW
 - =PP1V2_ENETFW

Signal aliases required by this page:
 (NONE)

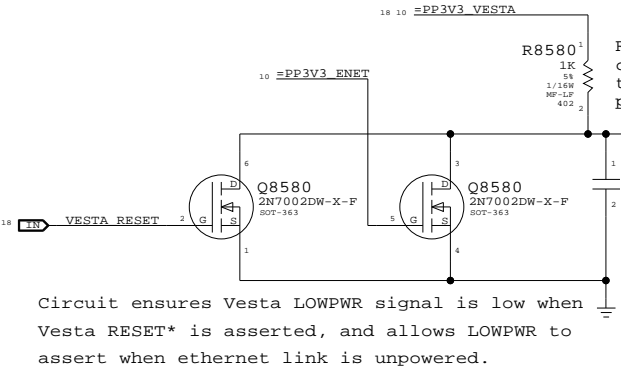
BOM options provided by this page:
 (NONE)

Net Spacing Type: ENET_MDI

Time to Line: 0.38 nms
 Length Tolerance: 50 mils
 Primary Max Sep: 5 mils
 Secondary Max Sep: 100 mils
 Secondary Length: 500 mils

NOTE: Target differential impedance for ENET data pairs is 100 ohms.

Vesta Ethernet LowPwr Disables Vesta Ethernet Circuit

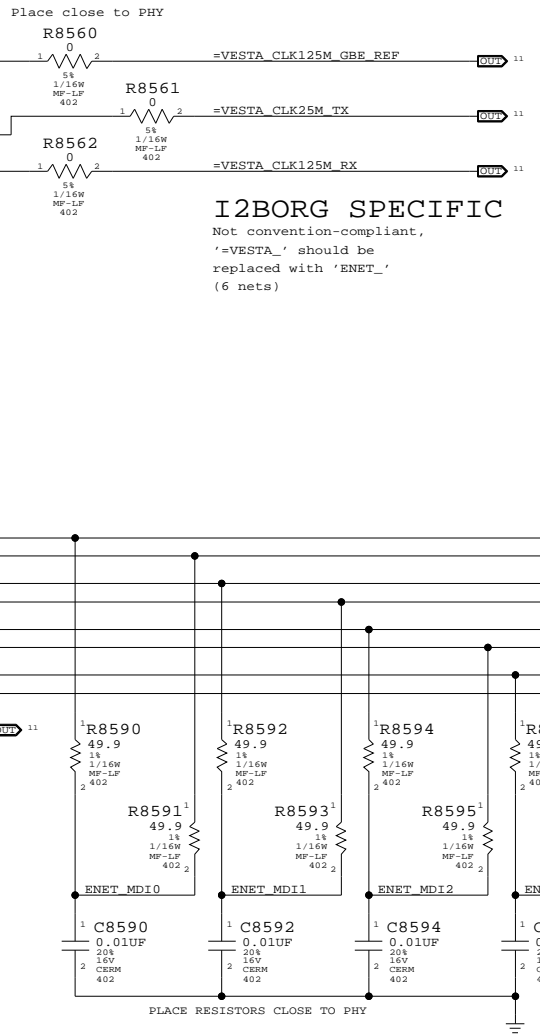
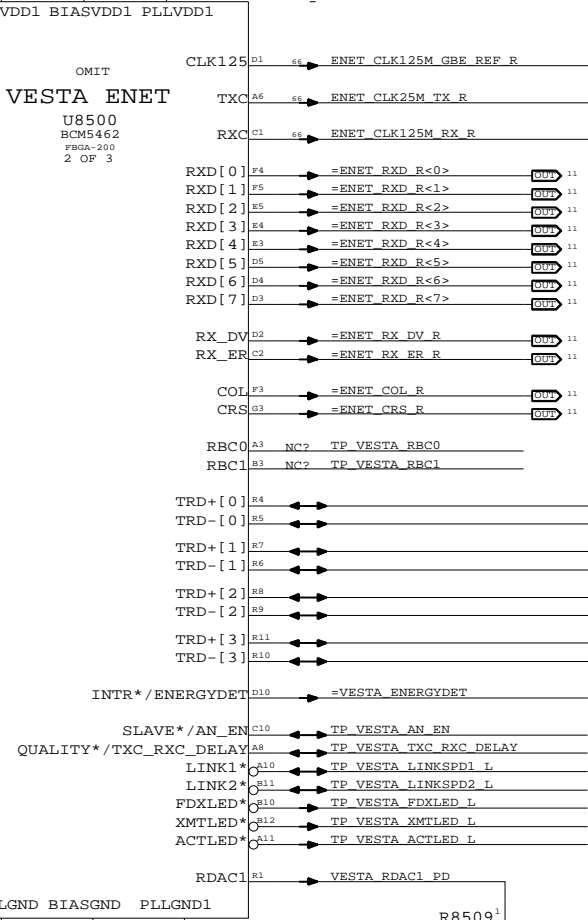
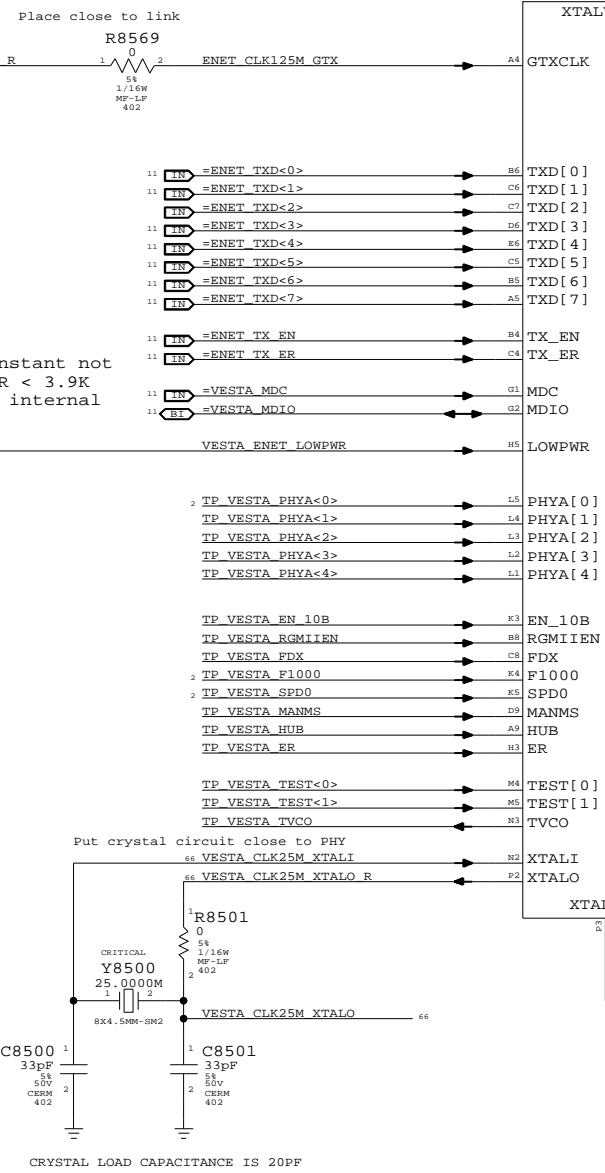


Circuit ensures Vesta LOWPWR signal is low when Vesta RESET* is asserted, and allows LOWPWR to assert when ethernet link is unpowered.

Vesta Config Straps:

PHYA<4..0>	PHY Address Select (Internal Pull-downs)	MANMS	Manual Master/Slave Configuration Select (Internal Pull-down)
EM_10B	TBI Interface Select (Internal Pull-down)	HUB	Repeater Select (Internal Pull-down)
RGMIEN	RGMI Enable (Internal Pull-down)	ER	Edge Rate Select (Internal Pull-down)
FDX	Full-Duplex Select (Internal Pull-up)	AN_EN	Auto-Negotiation Select (Internal Pull-up)
F1000	Speed Select (Internal Pull-up)	TXC_RXC_DELAY	TXC/RXC Delay (Internal Pull-up)
SPD0	Speed Select (Internal Pull-down)		

AN_EN	F1000	SPD0	Description
0	0	0	Force 10BASE-T
0	0	1	Force 100BASE-TX
0	1	X	Force 1000BASE-T (test use only)
1	0	0	Auto-negotiate advertise 10BASE-T
1	0	1	Auto-negotiate advertise 10/100BASE-TX
1	1	0	Auto-negotiate advertise 10/100/1000BASE-T
1	1	1	Auto-negotiate advertise 1000BASE-T



Vesta Ethernet PHY

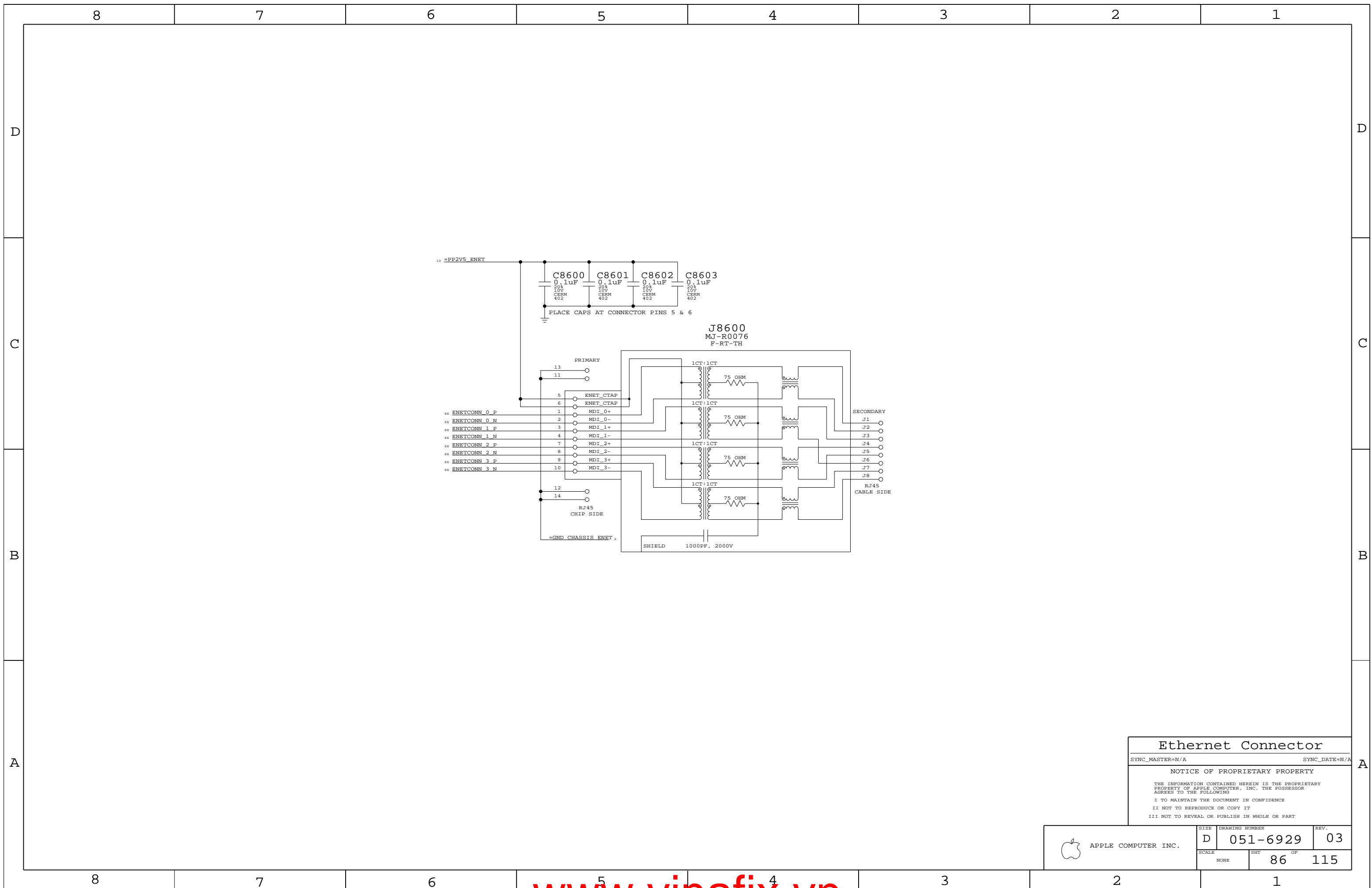
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NONE	85	115	



Ethernet Connector

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	D	051-6929	03
SCALE	SHT	OF	REV.
NONE	86	115	1

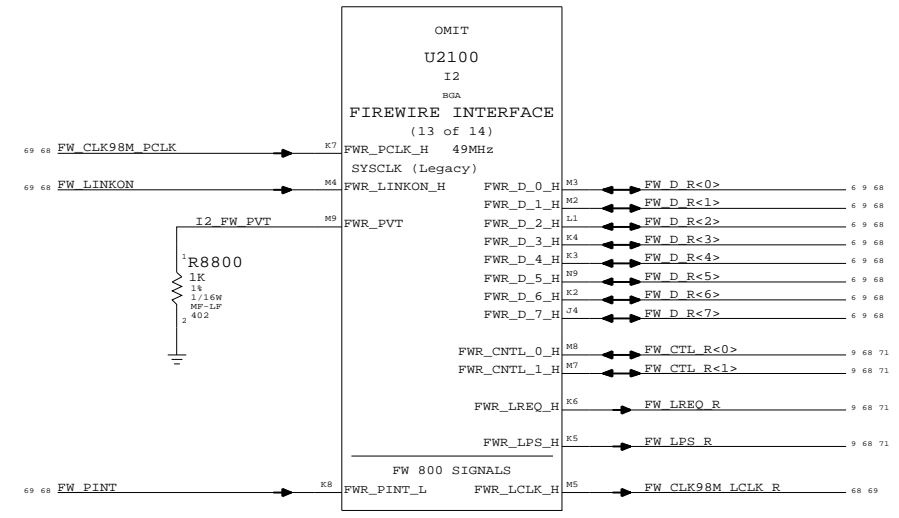
ELECTRICAL_CONSTRAINT_SET	NET_TYPE				
	SPACING	PHYSICAL	DIFFERENTIAL_PAIR		
FW_D<7..0>	FW	FW		FW D R<7..0>	6 9 68
FW_CTL R<1..0>	FW	FW		FW CTL R<1..0>	9 68 71
FW_LREQ	FW	FW		FW LREQ R	9 68 71
	FW	FW		FW LPS R	9 68 71
	FW	FW		FW LINKON	68 69
FW_CLK	CLOCK	CLOCK		FW CLK98M_PCLK	68 69
FW_LCLK	CLOCK	CLOCK		FW CLK98M_LCLK R	68 69
FW_PINT	FW	FW		FW PINT	68 69

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



I2 FireWire Interface

SYNC_MASTER=N/A SYNC_DATE=N/A

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	D	051-6929	03
SCALE	NONE	SHT	OF
		88	115

ELECTRICAL_CONSTRAINT_SET	NET_TYPE	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
PROVIDED BY LINK PAGE1	CLOCK	CLOCK		
	CLOCK	CLOCK		
FW_TPA0	FW_TP	FW_TP	FW_TPA0	FW_TPA0_P
FW_TPA0	FW_TP	FW_TP	FW_TPA0	FW_TPA0_N
FW_TPB0	FW_TP	FW_TP	FW_TPB0	FW_TPB0_P
FW_TPB0	FW_TP	FW_TP	FW_TPB0	FW_TPB0_N
FW_TPA1	FW_TP	FW_TP	FW_TPA1	FW_TPA1_P
FW_TPA1	FW_TP	FW_TP	FW_TPA1	FW_TPA1_N
FW_TPB1	FW_TP	FW_TP	FW_TPB1	FW_TPB1_P
FW_TPB1	FW_TP	FW_TP	FW_TPB1	FW_TPB1_N
FW_TPA2	FW_TP	FW_TP	FW_TPA2	FW_TPA2_P
FW_TPA2	FW_TP	FW_TP	FW_TPA2	FW_TPA2_N
FW_TPB2	FW_TP	FW_TP	FW_TPB2	FW_TPB2_P
FW_TPB2	FW_TP	FW_TP	FW_TPB2	FW_TPB2_N
VESTA_CLK24M_XTAL	XTAL	XTAL		VESTA_CLK24M_XTALI
	XTAL	XTAL		VESTA_CLK24M_XTALO
	XTAL	XTAL		VESTA_CLK24M_XTALO_R

Page Notes

Power aliases required by this page:
 - =PPFW_PHY_CPS
 - =PP3V3_FW
 - =PP3V3_ENETFW
 - =PP2V5_ENETFW
 - =PP1V2_ENETFW

Signal aliases required by this page:
 - NONE

BOM options provided by this page:
 - VESTA_BILINGUAL_EN12
 If stuffed, adds external pull-down to counter internal pull-up in Vesta. See straps table for more information.
 - VESTA_DS_ONLY_EN0
 If stuffed, adds external pull-up to counter internal pull-down in Vesta. See straps table for more information.
 - VESTA_PORT1_DISABLE
 If stuffed, adds external pull-down to counter internal pull-up in Vesta. See straps table for more information.
 - VESTA_PORT2_DISABLE
 If stuffed, adds external pull-down to counter internal pull-up in Vesta. See straps table for more information.
 - VESTA_PWR_CLASS_0
 If stuffed, adds external pull-down to counter internal pull-up in Vesta. See straps table for more information.

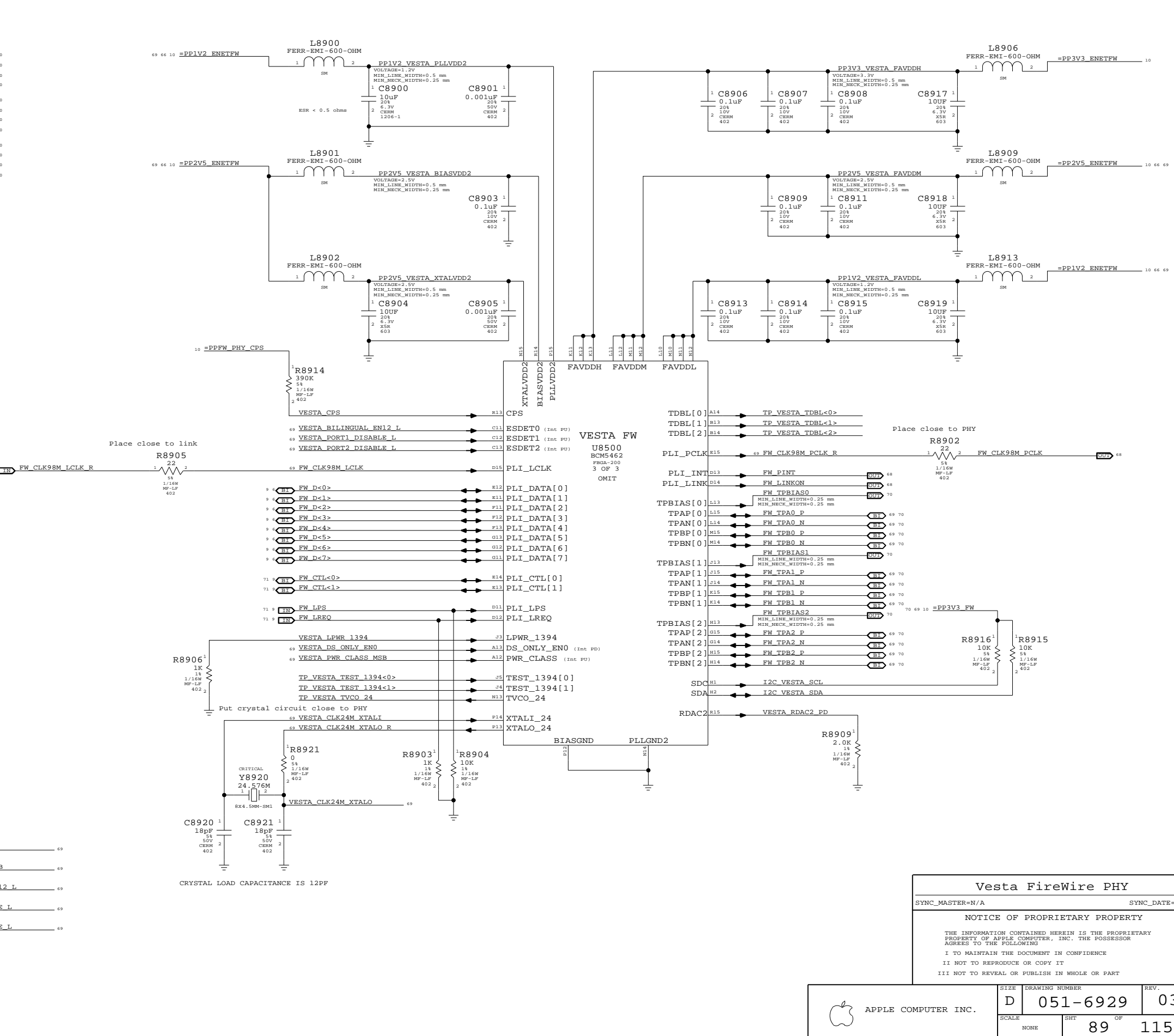
Net Spacing Type: FW_TP

Line to Line:	0.38 mms
Length Tolerance:	100 mils
Primary Max Sep:	7.5 mils
Secondary Max Sep:	100 mils
Secondary Length:	500 mils

NOTE: Target differential impedance for FW data pairs is 110 ohms.

Vesta Config Straps:

DS_ONLY_EN12 - Port 1&2 Data/Strobe	1 - Port 1&2 Data/Strobe mode only
DS_ONLY_EN0 - Port 0 Data/Strobe	0 - Port 0 Bilingual mode
PORT1_ENABLE - Port 1 Enable	1 - Port 1 Enabled
PORT1_DISABLE - Port 1 Disabled	0 - Port 1 Disabled (saves power)
PORT2_ENABLE - Port 2 Enable	1 - Port 2 Enabled
PORT2_DISABLE - Port 2 Disabled	0 - Port 2 Disabled (saves power)
PWR_CLASS - FireWire Power Class	1 - Sets Power Class to 0x4
	0 - Sets Power Class to 0x0



Vesta FireWire PHY

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	SHEET: 89	OF: 115	

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
PROVIDED	FW	FW	FW_PORT1_TPA_P_FL
	FW	FW	FW_PORT1_TPA_N_FL
	FW	FW	FW_PORT1_TPB_P_FL
	FW	FW	FW_PORT1_TPB_N_FL
BY	FW	FW	FW_PORT2_TPA_P_FL
	FW	FW	FW_PORT2_TPA_N_FL
	FW	FW	FW_PORT2_TPB_P_FL
	FW	FW	FW_PORT2_TPB_N_FL
PHY	FW	FW	FW_PORT2_TPA_P_FL
	FW	FW	FW_PORT2_TPA_N_FL
	FW	FW	FW_PORT2_TPB_P_FL
	FW	FW	FW_PORT2_TPB_N_FL
PAGE	FW	FW	FW_PORT2_TPA_P_FL
	FW	FW	FW_PORT2_TPA_N_FL
	FW	FW	FW_PORT2_TPB_P_FL
	FW	FW	FW_PORT2_TPB_N_FL

Page Notes

Power aliases required by this page:
 - _PPFW_PORT1
 - _PPFW_PORT2
 - _PPFW_PORT3
 - _PP3V3_FW
 - _GND_CHASSIS_FW_PORT1
 - _GND_CHASSIS_FW_PORT2
 - _GND_CHASSIS_FW_PORT3

Signal aliases required by this page:
 (NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

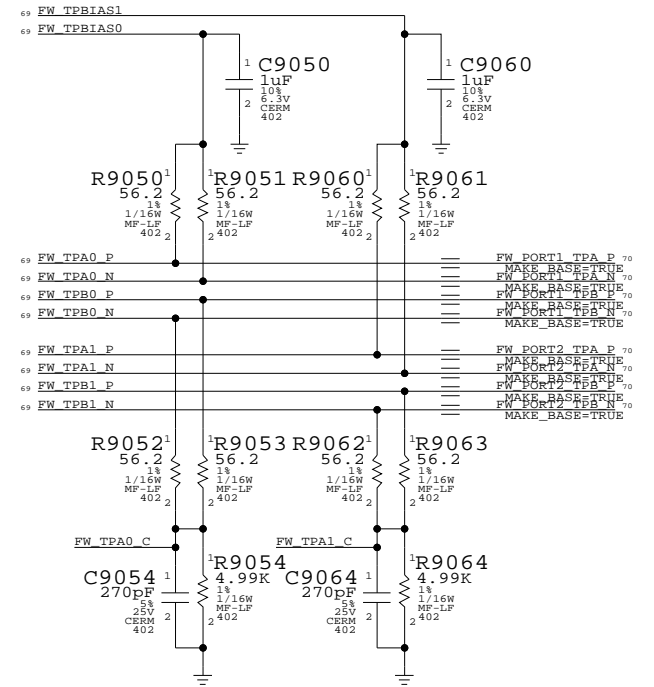
BOM options provided by this page:
 (NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

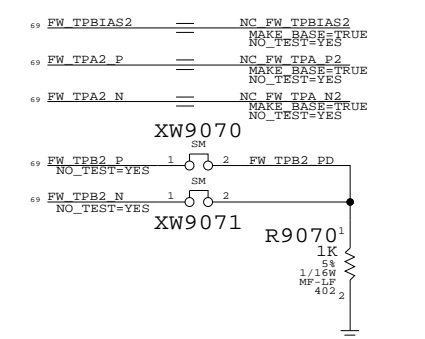
1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

Termination

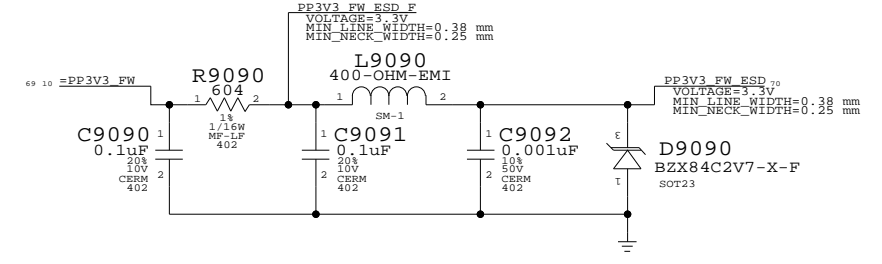
Place close to FireWire PHY



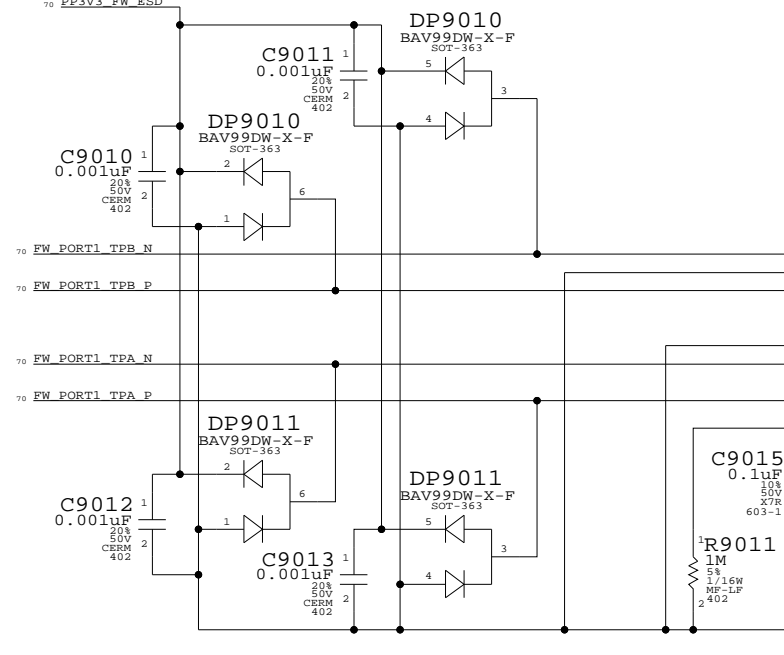
3rd TPA/TPB pair unused



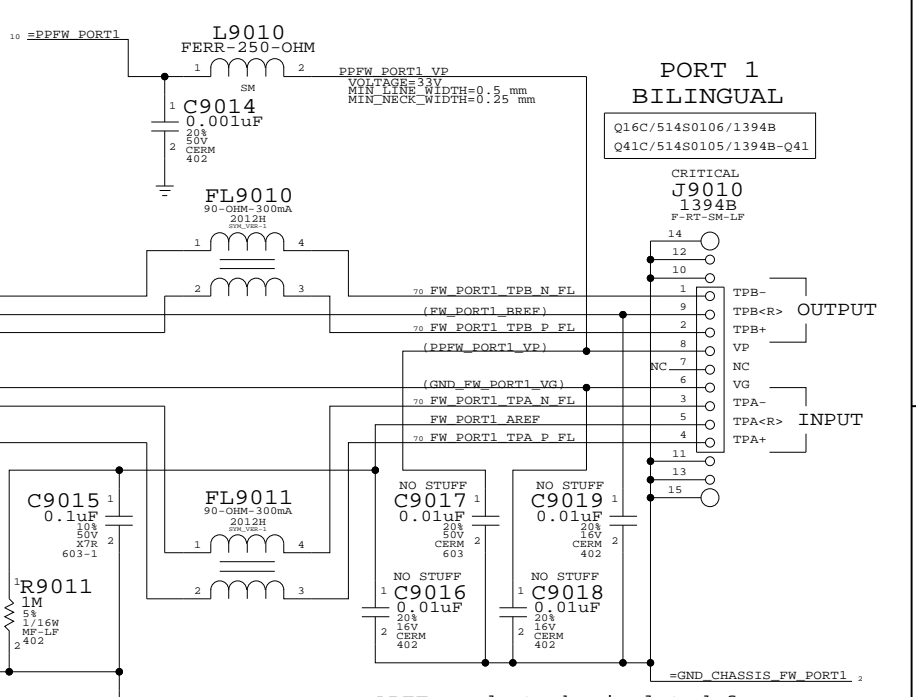
ESD Rail



"Snapback" & "Late VG" Protection



Cable Power

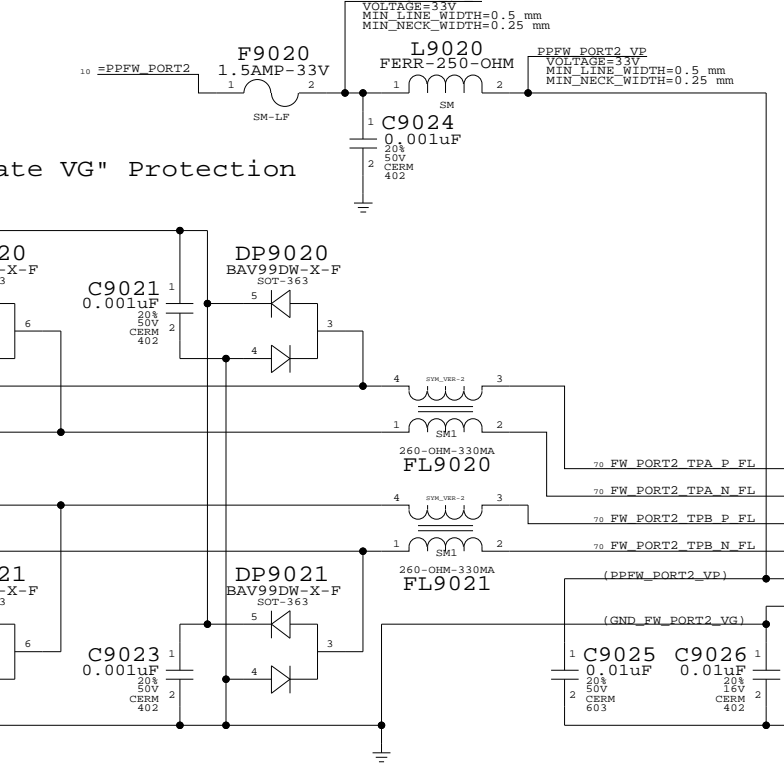


AREF needs to be isolated from all local grounds per 1394b spec

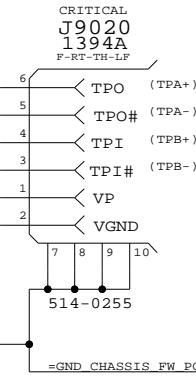
When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

BREF should be hard-connected to logic ground for speed signaling and connection detection currents per 1394b V1.33

Cable Power



PORT 2 1394A



FireWire Ports

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NONE	90	115

8

7

6

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D

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C

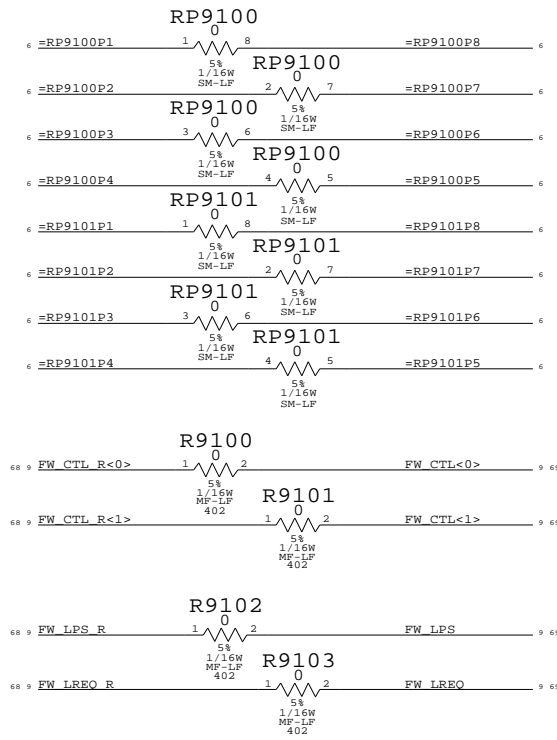
B

B

A

A

Place series terminators approximately halfway between Vesta and NB.
(They should probably be slightly closer to Vesta than the NB.)




FireWire Series Term

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NONE	91 OF		115

8

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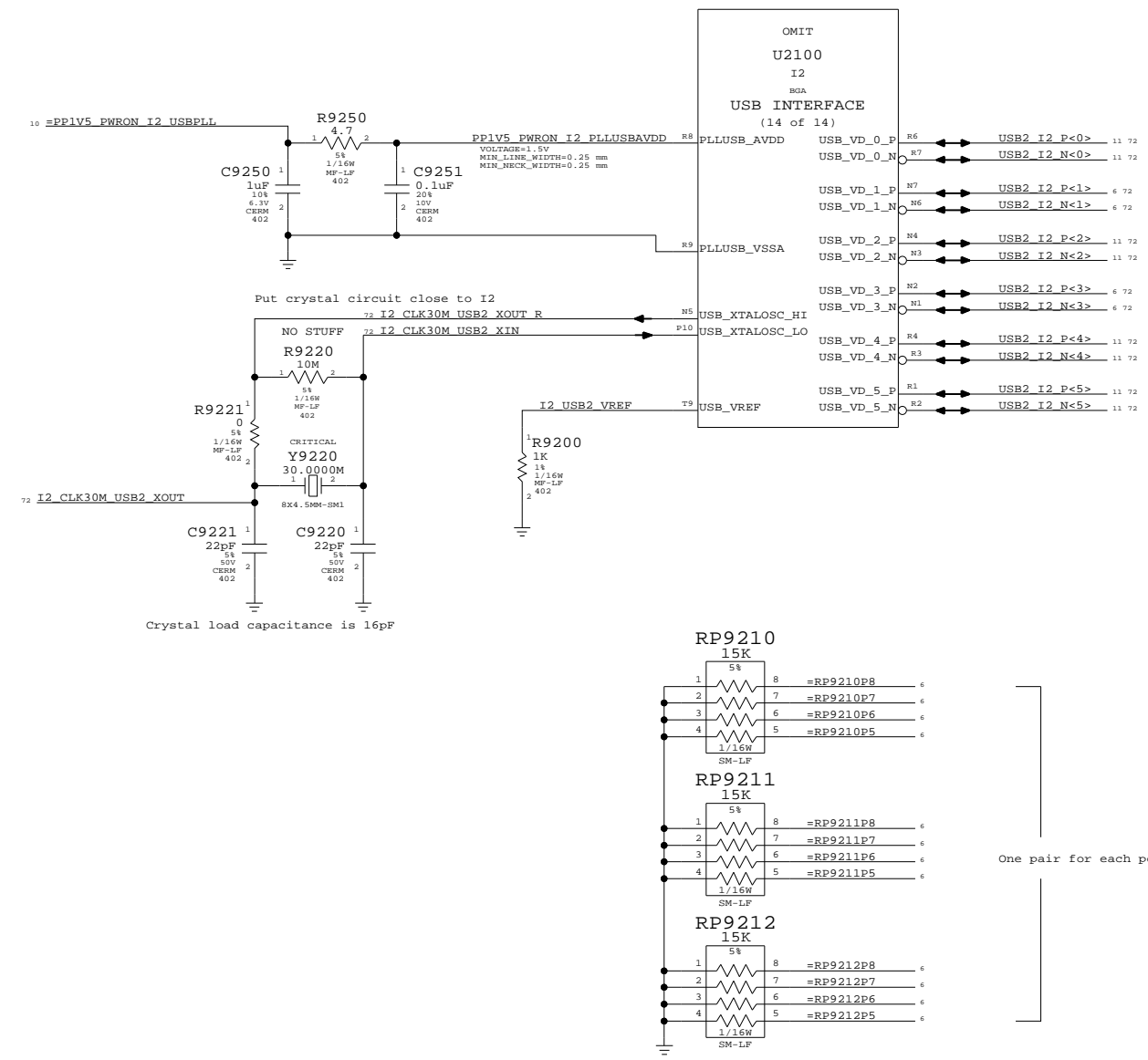
1

ELECTRICAL_CONSTRAINT_SET	NET_TYPE	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
USB2_0	USB2	USB2	USB2	USB2_I2_0	USB2_I2 P<0> 11 72
USB2_0	USB2	USB2	USB2	USB2_I2_N<0>	USB2_I2 N<0> 11 72
USB2_1	USB2	USB2	USB2	USB2_I2_1	USB2_I2 P<1> 6 72
USB2_1	USB2	USB2	USB2	USB2_I2_N<1>	USB2_I2 N<1> 6 72
USB2_2	USB2	USB2	USB2	USB2_I2_2	USB2_I2 P<2> 11 72
USB2_2	USB2	USB2	USB2	USB2_I2_N<2>	USB2_I2 N<2> 11 72
USB2_3	USB2	USB2	USB2	USB2_I2_3	USB2_I2 P<3> 6 72
USB2_3	USB2	USB2	USB2	USB2_I2_N<3>	USB2_I2 N<3> 6 72
USB2_4	USB2	USB2	USB2	USB2_I2_4	USB2_I2 P<4> 11 72
USB2_4	USB2	USB2	USB2	USB2_I2_N<4>	USB2_I2 N<4> 11 72
USB2_5	USB2	USB2	USB2	USB2_I2_5	USB2_I2 P<5> 11 72
USB2_5	USB2	USB2	USB2	USB2_I2_N<5>	USB2_I2 N<5> 11 72
USB2_I2_XTAL	XTAL	XTAL	XTAL	I2_CLK30M_USB2_XOUT_R	72
(USB2_I2_XTAL)	XTAL	XTAL	XTAL	I2_CLK30M_USB2_XOUT	72
(USB2_I2_XTAL)	XTAL	XTAL	XTAL	I2_CLK30M_USB2_XIN	72

Page Notes

Power aliases required by this page:
 - =PP1V5_PWRON_USB
 Signal aliases required by this page:
 - =RP92xxPy (pinswappable USB pulldowns)
 BOM options provided by this page:
 (NONE)

Net Spacing Type: USB2
 Line To Line: 19.5 mils
 Length Tolerance: 50 mils
 Primary Max Sep: 7.5 mils
 Secondary Max Sep: 100 mils
 Secondary Length: 500 mils
 NOTE: Target differential impedance for USB2 data pairs is 90 ohms.



One pair for each port USB2_*<0..5>

I2 USB Interface
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		92	115

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
E30	USB2	USB2	USB2_NEC_0
E31	USB2	USB2	USB2_NEC_0
E32	USB2	USB2	USB2_NEC_1
E33	USB2	USB2	USB2_NEC_1
E34	USB2	USB2	USB2_NEC_2
E35	USB2	USB2	USB2_NEC_2
E36	USB2	USB2	USB2_NEC_3
E37	USB2	USB2	USB2_NEC_3

PROVIDED BY 12 PAGES

E40	USB2_NEC_XTAL	XTAL	XTAL	NEC_CLK30M_XT1
E41	USB2_NEC_XTAL	XTAL	XTAL	NEC_CLK30M_XT2
E42	USB2_NEC_XTAL	XTAL	XTAL	NEC_CLK30M_XT2_R

Page Notes

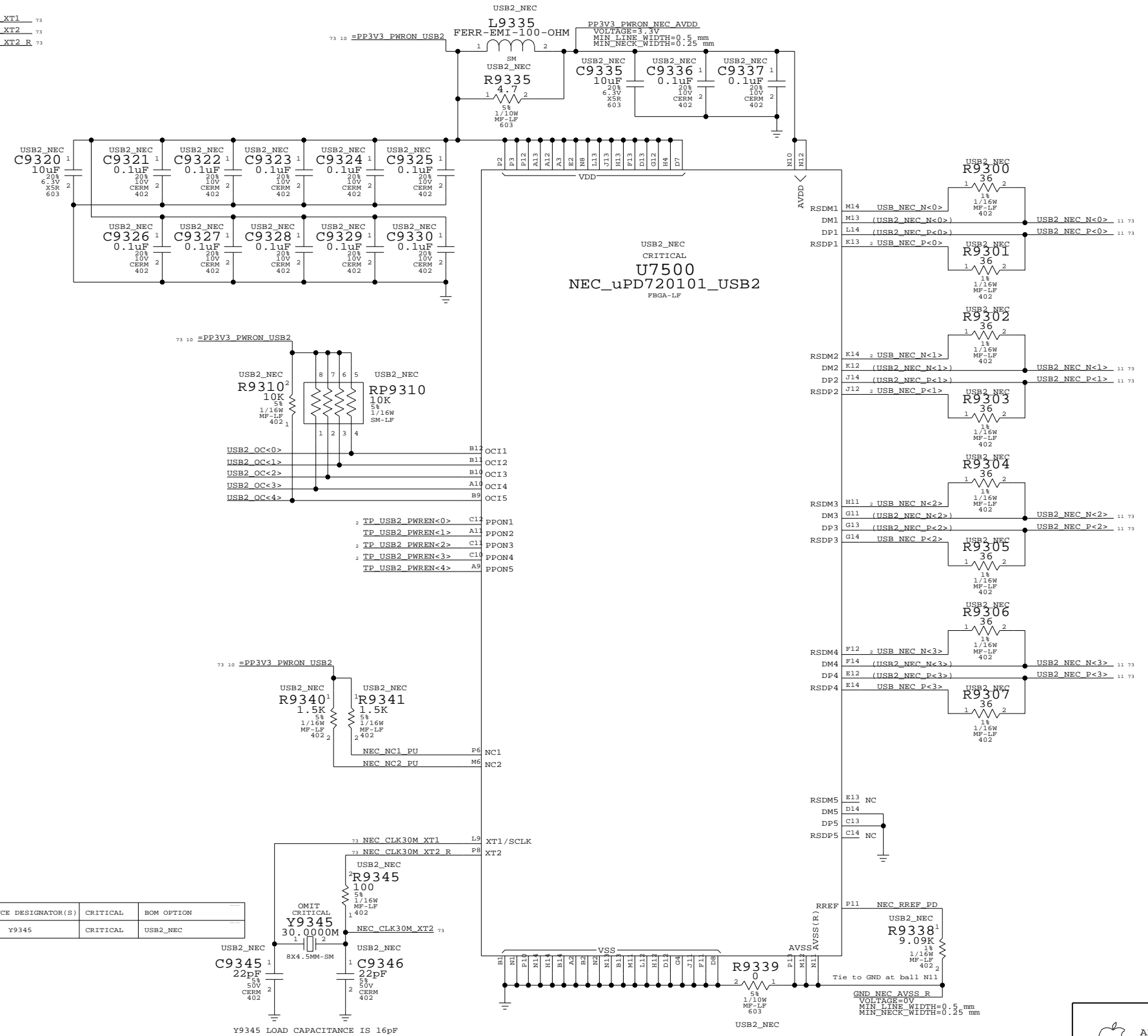
Power aliases required by this page:
 - =PP3V3_PWRON_USB2

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 USB2_NEC

Net Spacing Type: USB2

NOTE: Target differential impedance for USB2 data pairs is 90 ohms.



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
19750087	1	XTAL_CER.30.000MHZ.LW PROF.8X4.5MM.SMD	Y9345	CRITICAL	USB2_NEC

NEC USB2 Interface

SYNC_MASTER=N/A SYNC_DATE=N/A

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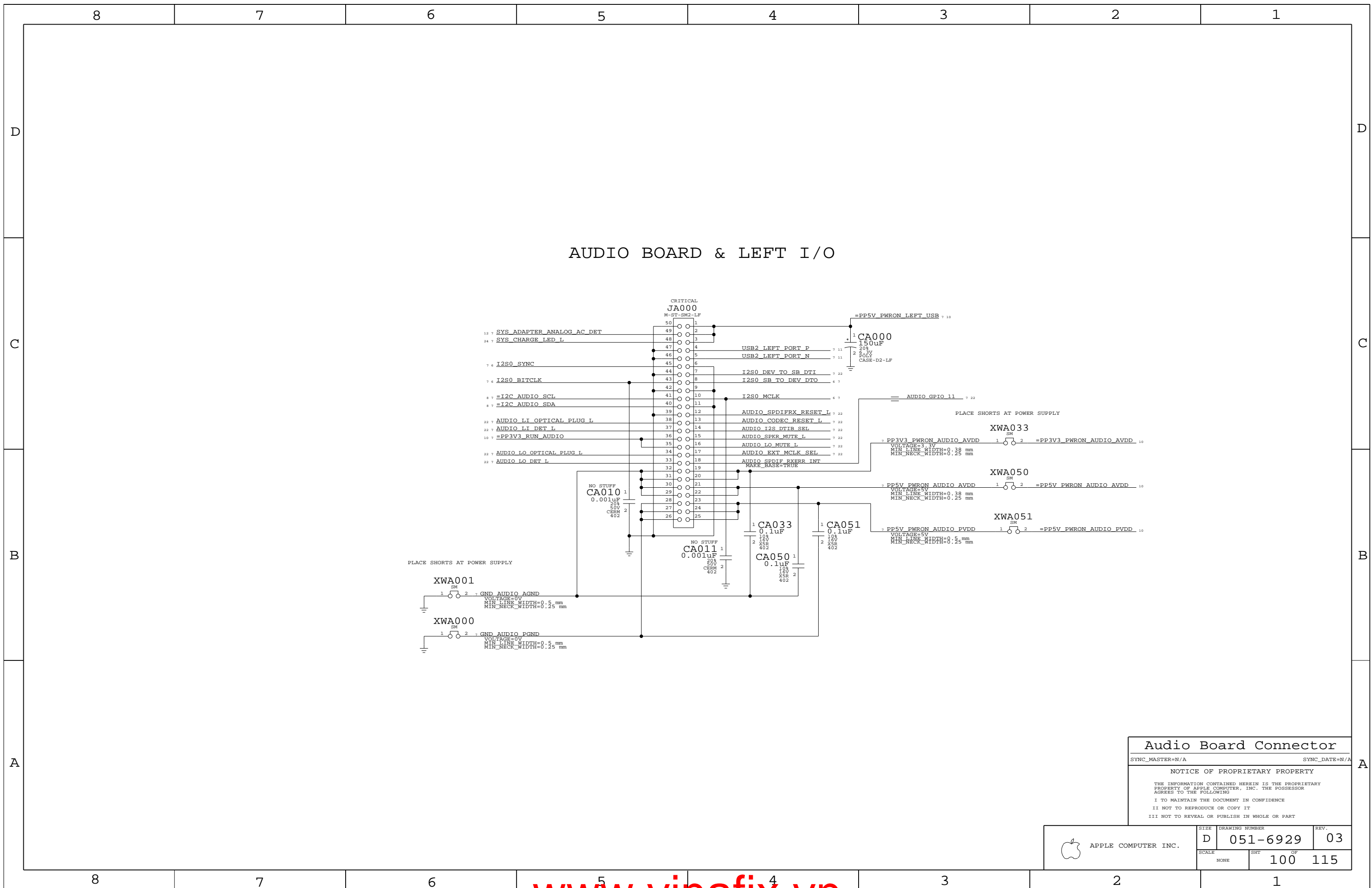
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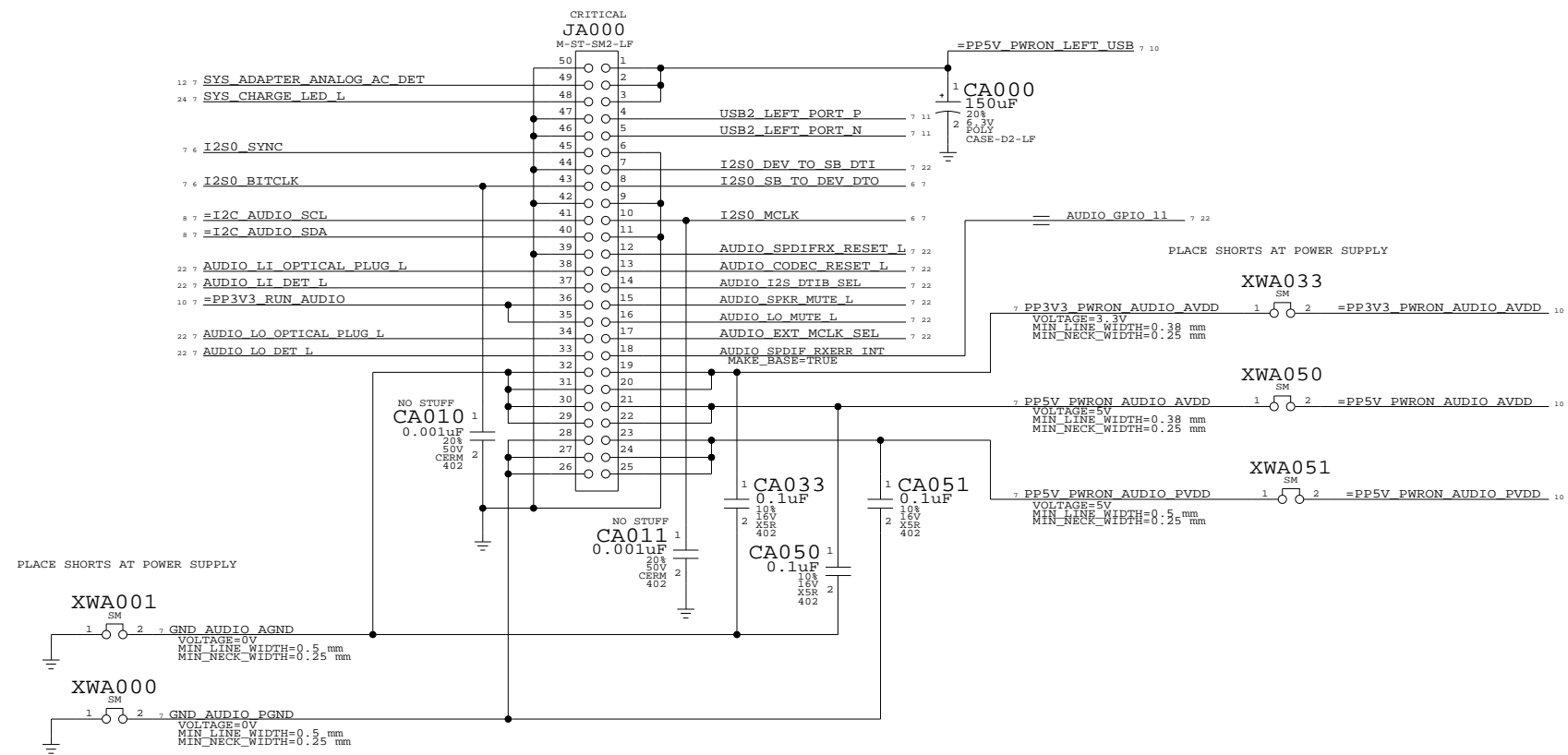
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NONE	93	115	



AUDIO BOARD & LEFT I/O



Audio Board Connector
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SCALE	SHT OF		
NONE	100		115

	8	7	6	5	4	3	2	1						
D	AGP TABLE_SPACING_RULE TABLE_SPACING_RULE AGP 401 * 0.4 MM =STANDARD =STANDARD =STANDARD =STANDARD TABLE_SPACING_RULE AGP_STB 601 * 0.6 MM 2.5 MM =100_OHM_DIFF =100_OHM_DIFF =100_OHM_DIFF TABLE_PHYSICAL_RULE TABLE_PHYSICAL_RULE AGP * =STANDARD =60_OHM_SE =60_OHM_SE =60_OHM_SE TABLE_PHYSICAL_RULE AGP_STB * =STANDARD =100_OHM_DIFF =100_OHM_DIFF =100_OHM_DIFF					AUDIO TABLE_SPACING_RULE TABLE_SPACING_RULE AUDIO 251 * 0.25 MM =STANDARD =STANDARD =STANDARD =STANDARD TABLE_PHYSICAL_RULE TABLE_PHYSICAL_RULE AUDIO * =50_OHM_SE =50_OHM_SE =50_OHM_SE =50_OHM_SE								
	CLOCK TABLE_SPACING_RULE TABLE_SPACING_RULE CLOCK 251 * 0.25 MM =STANDARD =STANDARD =STANDARD =STANDARD TABLE_PHYSICAL_RULE TABLE_PHYSICAL_RULE CLOCK * =STANDARD =50_OHM_SE =50_OHM_SE =50_OHM_SE					I2S TABLE_SPACING_RULE TABLE_SPACING_RULE I2S 251 * 0.25 MM =STANDARD =STANDARD =STANDARD =STANDARD TABLE_PHYSICAL_RULE TABLE_PHYSICAL_RULE I2S * =50_OHM_SE =50_OHM_SE =50_OHM_SE =50_OHM_SE								
	ENET (Ethernet Digital) TABLE_SPACING_RULE TABLE_SPACING_RULE ENET_SELF =STANDARD * =STANDARD =STANDARD =STANDARD =STANDARD =STANDARD TABLE_SPACING_RULE ENET 201 * 0.2 MM =STANDARD =STANDARD =STANDARD =STANDARD TABLE_PHYSICAL_RULE TABLE_PHYSICAL_RULE ENET * =STANDARD =50_OHM_SE =50_OHM_SE =50_OHM_SE					ENETCONN TABLE_SPACING_RULE TABLE_SPACING_RULE ENETCONN 501 * 0.50 MM 3.81 MM =100_OHM_DIFF =100_OHM_DIFF =100_OHM_DIFF TABLE_PHYSICAL_RULE TABLE_PHYSICAL_RULE ENETCONN * =100_OHM_DIFF =100_OHM_DIFF =100_OHM_DIFF =100_OHM_DIFF								
	FW (FireWire Digital) TABLE_SPACING_RULE TABLE_SPACING_RULE FW_SELF =STANDARD * =STANDARD =STANDARD =STANDARD =STANDARD =STANDARD TABLE_SPACING_RULE FW 201 * 0.2 MM =STANDARD =STANDARD =STANDARD =STANDARD TABLE_PHYSICAL_RULE TABLE_PHYSICAL_RULE FW * =STANDARD =50_OHM_SE =50_OHM_SE =50_OHM_SE					FW_TP TABLE_SPACING_RULE TABLE_SPACING_RULE FW_TP 501 * 0.50 MM 3.81 MM =110_OHM_DIFF =110_OHM_DIFF =110_OHM_DIFF TABLE_PHYSICAL_RULE TABLE_PHYSICAL_RULE FW_TP * =110_OHM_DIFF =110_OHM_DIFF =110_OHM_DIFF =110_OHM_DIFF								
	C	I2C TABLE_SPACING_RULE TABLE_SPACING_RULE I2C 201 * 0.2 MM =STANDARD =STANDARD =STANDARD =STANDARD TABLE_PHYSICAL_RULE TABLE_PHYSICAL_RULE I2C * =STANDARD =50_OHM_SE =50_OHM_SE =50_OHM_SE					I2_FBCLK / XTAL TABLE_SPACING_ASSIGNMENT TABLE_SPACING_ASSIGNMENT I2_FBCLK * * CLOCK TABLE_SPACING_ASSIGNMENT XTAL * * CLOCK TABLE_PHYSICAL_ASSIGNMENT TABLE_PHYSICAL_ASSIGNMENT I2_FBCLK * * CLOCK TABLE_PHYSICAL_ASSIGNMENT XTAL * * CLOCK							
		MaxBus TABLE_SPACING_RULE TABLE_SPACING_RULE MAXBUS 151 * 0.15 MM =STANDARD =STANDARD =STANDARD =STANDARD TABLE_PHYSICAL_RULE TABLE_PHYSICAL_RULE MAXBUS * =STANDARD =50_OHM_SE =50_OHM_SE =50_OHM_SE												
	B	PCI TABLE_SPACING_RULE TABLE_SPACING_RULE PCI =STANDARD * =STANDARD =STANDARD =STANDARD =STANDARD =STANDARD TABLE_PHYSICAL_RULE TABLE_PHYSICAL_RULE PCI * =STANDARD =50_OHM_SE =50_OHM_SE =50_OHM_SE												
		RAM TABLE_SPACING_RULE TABLE_SPACING_RULE RAM 201 * 0.2 MM =STANDARD =STANDARD =STANDARD =STANDARD TABLE_SPACING_RULE RAM_DIFF 251 * 0.25 MM 2.5 MM =100_OHM_DIFF =100_OHM_DIFF =100_OHM_DIFF TABLE_PHYSICAL_RULE TABLE_PHYSICAL_RULE RAM * =50_OHM_SE =50_OHM_SE =50_OHM_SE =50_OHM_SE TABLE_PHYSICAL_RULE RAM_DIFF * =100_OHM_DIFF =100_OHM_DIFF =100_OHM_DIFF =100_OHM_DIFF												
	A	UATA TABLE_SPACING_RULE TABLE_SPACING_RULE UATA 151 * 0.15 MM =STANDARD =STANDARD =STANDARD =STANDARD TABLE_PHYSICAL_RULE TABLE_PHYSICAL_RULE UATA * =50_OHM_SE =50_OHM_SE =50_OHM_SE =50_OHM_SE												
		USB2 TABLE_SPACING_RULE TABLE_SPACING_RULE USB2 501 * 0.50 MM 3.81 MM =90_OHM_DIFF =90_OHM_DIFF =90_OHM_DIFF TABLE_PHYSICAL_RULE TABLE_PHYSICAL_RULE USB2 * =90_OHM_DIFF =90_OHM_DIFF =90_OHM_DIFF =90_OHM_DIFF												
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Spacing & Physical Constraints

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	8	7	6	5	4	3	2	1
D								
C								
B								
A								
	8	7	6	5	4	3	2	1

TABLE_SPACING_RULE								
TABLE_SPACING_RULE	DVO	151	*	0.15 MM	=STANDARD	=STANDARD	=STANDARD	=STANDARD
TABLE_PHYSICAL_RULE	DVO		*					
TABLE_SPACING_RULE	DVO		*		=STANDARD	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE
TABLE_SPACING_RULE	TV	151	*	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE
TABLE_SPACING_RULE	TV_CONN	151	*	=TV	=TV	=TV	=TV	=TV
TABLE_PHYSICAL_RULE	TV		*					
TABLE_PHYSICAL_RULE	TV_CONN		*					
TABLE_SPACING_RULE	VGA	151	*	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE
TABLE_SPACING_RULE	VGA_CONN	151	*	=VGA	=VGA	=VGA	=VGA	=VGA
TABLE_PHYSICAL_RULE	VGA		*					
TABLE_PHYSICAL_RULE	VGA_CONN		*					
TABLE_SPACING_RULE	LVDS	151	*		=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
TABLE_PHYSICAL_RULE	LVDS		*					
TABLE_SPACING_RULE	TMDS	251	*	0.25 MM	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
TABLE_SPACING_RULE	TMDS_CONN		*	=TMDS	=TMDS	=TMDS	=TMDS	=TMDS
TABLE_PHYSICAL_RULE	TMDS		*					
TABLE_PHYSICAL_RULE	TMDS_CONN		*					
TABLE_SPACING_RULE	THERM	251	*	0.25 MM	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
TABLE_PHYSICAL_RULE	THERM		*	Y	0.25 MM	=100_OHM_DIFF	=100_OHM_DIFF	

DVO

S-VIDEO

VGA

LVDS

TMDS

THERM

Spacing & Physical Constraints 2

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