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- 1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
- 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
- 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
B		35889	2PRODUCTION RELEASED	01/07/05	05


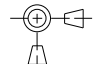
PAGE HIERARCHY CONTENTS

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4		REVISION NOTES
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9		SPEAKER AMPLIFIER
10		HEADPHONE AMPLIFIER AND CONNECTOR
11		LINE IN FILTER AND CONNECTOR
12		SPDIF RECEIVER
13		SIGNAL LOCATIONS
14		PART LOCATIONS

SCHEM, AUDIO BRD, PB17"

01/07/2005

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOH OPTION
051-6752	1	SCHEM, AUDIO BRD, PB17	SCH1	
820-1733	1	PCBF, AUDIO BRD, PB17	PCB1	

DIMENSIONS ARE IN MILLIMETERS		METRIC		 Apple Computer Inc.	
XX : _____	_____	DRAPFER	DESIGN CK	NOTICE OF PROPRIETARY PROPERTY THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING I TO MAINTAIN THE DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART	
X.XX : _____	_____	ENG APPD	MFG APPD		
X.XXX : _____	_____	QA APPD	DESIGNER		
ANGLES : _____	_____	RELEASE	SCALE		
DO NOT SCALE DRAWING		SCALE NONE		TITLE	
 THIRD ANGLE PROJECTION		MATERIAL/FINISH NOTED AS APPLICABLE		SIZE D	DRAWING NUMBER 051-6752 REV. B
				SHT 1 OF 14	

PCB SPECS

THICKNESS : 1.2 MM / 0.047 IN
 1/2 OZ CU THICKNESS: 0.7 MILS
 1.0 OZ CU THICKNESS: 1.4 MILS

IMPEDANCE : 50 OHMS +/- 10%
 DIELECTRIC : FR-4
 LAYER COUNT: 12
 SIGNAL TRACE WIDTH: 4 MILS
 SIGNAL TRACE SPACING: 4 MILS
 PREPREG THICKNESS: 2-3 MILS

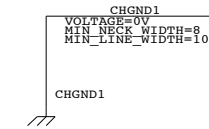
SEE PCB CAD FILES FOR MORE SPECIFIC INFO.

BOARD STACK-UP AND CONSTRUCTION

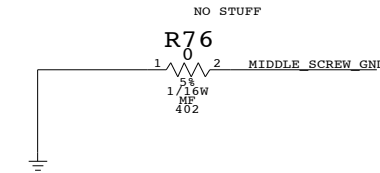
1	SIGNAL
2 PREPREG	GROUND
3 LAMINATE	SIGNAL
4 PREPREG	SIGNAL
5 LAMINATE	GROUND
6 PREPREG	CUT POWER PLANE
7 LAMINATE	CUT POWER PLANE
8 PREPREG	GROUND
9 LAMINATE	SIGNAL
10 PREPREG	SIGNAL
11 LAMINATE	GROUND
12 PREPREG	SIGNAL

BOARD HOLES

PAD ON SLOT IN BETWEEN J4 AND J5 (LAYER 1 AND LAYER 12)



PAD ON MIDDLE HOLE (LAYER 1 AND LAYER 12)



PCB BOARD STANDOFFS

BOARD INFORMATION

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BLOCK DIAGRAM

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REVISION NOTES

9/18/03
 1) REMOVED R34 (PULLDOWN ON I2S1ERROR) ON SPDIF RECEIVER)
 2) ADDED R37 AND R38 (100K 402) TO PUEDO-DIFF INPUT
 3) CHANGED AUD_SPDIF TO AUD_SPDIF_OUT ON U4 (CODEC)
 4) CHANGED C23, C25, C28 TO 10UF SMB
 5) ADDED C33||R41 AND C32||R40 AS RC FILTER BETWEEN LEFT AND INPUT AND OUTPUT OF U6, RESPECTIVELY
 6) CHANGED R43 TO PULLDOWN ON MUTE INPUT TO U6 (SPEAKER AMP)
 7) ADDED R39 AND R40 IN SERIES ON INPUTS TO U6
 8) CHANGED AUD_OUT_AMP_GND TO AUD_AMP_GND ON PGND OF U6
 9) ADDED R56 (100K 402) AS PULLDOWN ON SHDN_L ON U5
 10) ADDED C35 (1UF 805) BETWEEN C1P AND C1N (CHARGE PUMP) OF U5
 9/19/03
 11) RE-PINNED J1
 12) ADDED C36 AS BYPASS ON AUD_5V_PWRON1 AT U6 (SPEAKER AMP)
 13) ADDED 0 OHM 402 BETWEEN I2S0_MCLK AND AUD_CODEC_MCLK TO BYPASS U1 (NO STUFF)
 14) ADDED L4-L23,C38-C39, AND C61-C68 FOR LINE IN HP OUT FILTER
 15) ADDED D21 AND D22 ESD DIODES FOR LINE IN AND HP OUT
 16) ADDED Q1, R58, R59,R61,R62,R68,R64,C71 AND C69 FOR HP ANALOG AND OPTICAL DETECT BUFFER
 17) ADDED Q2, R63, R60,R67,R66,R65,R69,C72 AND C70 FOR LINE IN ANALOG AND OPTICAL DETECT BUFFER
 18) ADDED C74,C73,C76,C75 10UF 10V CAPS IN PSEUDO-DIFF FILTER
 9/19/03
 19) FIXED MISSING CONNECTIONS IN HP AND LINE IN EMI FILTERS
 20) ADDED ZT1 PLATED MOUNTING HOLE
 21) MOVED CIRCUITS AROUND TO CONFORM TO HIERARCHY
 9/22/03
 22) CHANGED C20 AND C22 TO 10UF
 23) ADDED C44 AS BYPASS ON OUTPUT OF 4.5V REGULATOR
 24) ADDED R34 AS PULLDOWN ON SHDN_L PIN OF U6 (SPEAKER AMP)
 25) CHANGED J1 TO CORRECT CONNECTOR (514S0159)
 9/24/03
 26) REMOVED L9,L19, AND C68 ON OPTICAL IN PLUG DETECT
 27) REMOVED U2,U1, AND U3 (SPDIF RECEIVER) AND ALL SURROUNDING COMPONENTS (PG 8)
 28) MIRRORRED J1 (MLB CONNECTOR) TO CORRECT PINOUT
 29) CORRECTED UNNAMED NETS IN LINE IN AND HP FILTERS
 30) ADDED HEADPHONE CONNECTOR WITH OPTICAL TRANSMITTER (J4) 514-0137
 31) ADDED LINE IN CONNECTOR (J5) 514-0061
 9/25/03
 32) REVERSED ALL CHANGES LISTED ABOVE ON 9/24/03
 33) ADDED L27 AND L28 FOR POWER SUPPLY FILTERING ON U5 (HP AMP)
 34) CHANGED L7,L8,L17,L18 TO 0402 1000OHM EMI FERRITES
 35) ADDED L24, L25, AND L26 FOR INPUT FILTERING ON SPEAKER AMP INPUTS
 36) CHANGED L9-L13 AND L19-L23 TO 1000OHM 0402 EMI FERRITES
 37) UPDATED MLB CONNECTOR PINOUT
 38) FIXED UNAMED NETS IN LINE IN (PG7) AND HP (PG6) EMI FILTERS
 39) CHANGED MLB CONNECTOR (J1) FROM 516S0159 TO 516S0160 (CORRECTED FOR GENDER CONSISTENCY)
 40) CHANGED R35,R36,R45,R46 TO 603 14 OHM FROM 805
 9/26/03
 41) FIXED MLB CONNECTOR PINT (MIRRORRED SYMBOL)
 42) CHANGED ZT1 TO 195R106 PLATED THRU-HOLE
 43) REMOVED C51-C54 FROM FILTERS ON SPEAKER AMP OUTPUTS
 44) CHANGED MUTE INPUT OF U6 (SPEAKER AMP) FROM AUD_5V_PWRON1 TO AUD_SPA_MUTE
 45) CHANGED L1 TO 0402 1000OHM EMI FERRITE
 46) UPDATED SCHEMATIC CONSTRAINTS
 9/27/03
 47) MIRRORRED J1 (MLB CONNECTOR) TO FIX FLEX ROUTING
 9/29/03
 48) CHANGED C73-C76 TO 10UF ELECTROLYTIC 128S1010
 49) CHANGED L2 AND L7-L26 TO 155S0137 TO CORRECT BOM PROBLEM
 9/30/03
 50) MOVED GND IN J1 TO IN BEWTEEN AUD_LO_DET_L AND AUD_LO_METAL_PLUG_L
 51) CHANGED C73-C76 TO 10UF SMB CAPS
 52) ADDED PAGE 9 FOR FUNCTIONAL TEST POINTS
 53) CORRECTED PINOUT OF J4 AND J5 FOR NEW CONNECTORS
 54) CORRECTED OPTICAL/METAL DETECT PINOUT FOR J4 AND J5
 10/1/03
 55) ADDED MISSING LINE WIDTH CONSTRAINTS ON HP OUTPUT NETS
 56) REPACKAGED TO PULL IN UPDATED FOOTPRINT FOR U5 (ADDED THERMAL VIAS)
 57) CHANGED R52-R55 FROM 14K 1% TO 10K 1%
 58) REMOVED XW1
 59) CHANGED AUG_GND ON DAC FILTER TO AUD_AMP_STARGND
 60) CHANGED AUD_GND ON C49 TO AUD_AMP_STARGND
 61) CHANGED GND ON HP AMP (U5) TO AUD_AMP_STARGND
 62) REMOVED Q2 AND R62 FROM AUD_LO_METAL_PLUG_L CIRCUIT
 63) REMOVED Q2 AND R65 FROM AUD_LI_METAL_PLUG_L CIRCUIT
 64) CHANGED AUD_AMP_GND ON XW4 TO AUD_AMP_STARGND
 65) CHANGED AUD_AMP_GND TO AUD_AMP_STARGND ON J3
 66) REPACKAGE TO PULL IN UPDATED I/O CONNECTOR SYMBOLS
 67) CHANGED AUD_GND TO AUD_CODEC_GND ON XW6
 68) CHANGED MIN_NECK_WIDTH PROPERTIES TO BE DIFFERENT THAN MIN_LINE_WIDTH
 69) CHANGED MIN_LINE_WIDTH TO 10 AND MIN_NECK_WIDTH TO 8 ON AUD_5V_PWRON1_HPAMP_PVDD
 10/3/03
 70) REMOVED Q1 AND R58 TO CORRECT SENSE OF AUDIO_LO_DET_L
 71) MOVED R67 TO AUD_IN_METAL SIDE OF R63 TO AVOID DIVIDER ON OUTPUT
 72) MOVED R69 TO AUD_IN_FIBER SIDE OF R66 TO AVOID DIVIDER ON OUTPUT
 73) MOVED R61 TO AUD_OUT_METAL SIDE OF R59 TO AVOID DIVIDER ON OUTPUT
 74) MOVED R64 TO AUD_OUT_FIBER SIDE OF R64 TO AVOID DIVIDER ON OUTPUT
 75) ADDED Q1 AND R58 TO CORRECT SENSE OF AUDIO_LO_DET_L
 76) ADDED Q1 AND R60 TO CORRECT SENSE OF AUDIO_LI_DET_L
 77) MOVED R67 TO AUDIO_LI_DET_L SIDE OF R63 TO AVOID DIVIDER ON OUTPUT
 78) MOVED R69 TO AUDIO_LI_METAL_PLUG_L SIDE OF R66 TO AVOID DIVIDER ON OUTPUT
 79) MOVED R61 TO AUDIO_LO_DET_L SIDE OF R59 TO AVOID DIVIDER ON OUTPUT
 80) MOVED R64 TO AUDIO_LO_METAL_PLUG_L SIDE OF R64 TO AVOID DIVIDER ON OUTPUT
 *** RELEASED FOR PROTO 1 ***

10/16/03
 81) CHANGED U5 TO REFLECT UPDATED SYMBOL FOR MAX9722 (3X3)
 10/27/03
 82) ADDED R72-R75 TO SELECT POWER INPUT TO SPDIF TRANSMITTER AND RECEIVER
 83) CHANGED VCC (PIN 2A) ON J4 (SPDIF TRANSMITTER) TO AUD_SPDIF_TRANS_RUN
 84) CHANGED VCC (PIN 1A) ON J5 (SPDIF RECEIVER) TO AUD_SPDIF_RECVR_RUN
 85) CHANGED R44 TO 113S1470 FOR BOM CONSOLIDATION WITH LINK
 86) CHANGED C37,C69,C71,C70,C72 TO 132S0045 FOR BOM CONSOLIDATION WITH LINK
 10/31/03
 87) REPACKAGED TO PULL IN UPDATED CONNECTOR FOOTPRINTS
 11/4/03
 88) ADDED MISSING CONSTRAINTS ON GND NETS
 89) FIXED UNNAMED NETS
 11/6/03
 90) CHANGED C15 AND C16 TO 131S2723 TO REMOVE OEM PART FROM BOM
 91) REMOVED ZT1 FROM SCHEMATIC TO IMPROVE GND HOLE TOLERANCE
 92) ADDED R76 (NO STUFF) FOR OPTION OF GROUNDING MIDDLE SCREW HOLE TO FRAME
 11/12/03
 93) CHANGED J4 TO FINAL FOXCONN CONNECTOR (514-0140)
 94) CHANGED J5 TO FINAL FOXCONN CONNECTOR (514-0144)
 11/13/03
 95) CHANGED C38,C39,C62,C64,C66,C68,C63,C65,C67,C61 FROM 603 100PF CERAMICS TO 402 100PF CERAMICS
 96) ADDED Q2, R77, AND R78 TO ADJUST FOR PLUG DETECT SCHEME DIFFERENCE WITH NEW CONNECTORS
 97) REMOVED L8, L7, L19, AND L23 IN T FILTERS BECAUSE SERIES R OF HIGHER VALUE MADE THEM REDUNDANT
 98) ADDED C54 (1UF 603) TO VDD OF U6 AND MOVED C36 TO BETWEEN AUD_5V_PWRON1 AND AUD_GND
 99) CHANGED SGND (PIN 6) OF U5 TO AUD_CODEC_STARGND
 100) CHANGED AUD_AMP_STARGND IN DAC FILTER TO AUD_HP_STARGND AND ADDED XW5 TO SHORT TO AUD_GND
 101) MOVED R63 TO INPUT SIDE OF R60 AND CHANGED TO 10K
 102) MOVED R66 TO INPUT SIDE OF R78 AND CHANGED TO 10K
 103) MOVED R59 TO INPUT SIDE OF R58 AND CHANGED TO 10K
 104) MOVED R64 TO INPUT SIDE OF R77 AND CHANGED TO 10K
 2/3/04
 105) ADDED R81 AS 100K PULLUP TO AUD_3V_RUN ON U2 PIN 17 (AUDIO_GPIO_11)
 2/4/04
 106) CHANGED R80 TO NO STUFF TO REMOVE DIVIDER ON OUTPUT OF OPTICAL RECEIVER
 107) CHANGED R74 TO NO STUFF AND R74 TO STUFFED TO CHANGE TO 3V3_RUN FOR SPDIF RECEIVER
 2/19/04
 108) CHANGED R7 TO NO STUFF
 3/14/04
 109) REMOVED R72-R75 AS SPDIF OPTICS ARE 3V ONLY
 110) CHANGED PIN 15 OF J1 TO AUD_3V_RUN
 111) REMOVED R79 AND R80 TO REMOVED 5V SPDIF COMPATIBILITY
 112) ADDED 22UF C55 AND C56 TO CLEAN UP AUD_3V_RUN FOR SPDIF
 113) SWAPPED INPUTS TO SPEAKER AMP AFTER THE L'S TO CORRECT CHANNEL SWAP ERROR
 114) FIXED NAMING CONFLICT ON PSEUDO-DIFF INPUT
 6/8/04
 115) CHANGED C73-C76 TO 10UF 10V 1206 TO SAVE SPACE IN PSEUDO-DIFF CIRCUIT
 116) CHANGED C2 TO 0.02UF X5R 402, C7 TO 0.001UF 402, AND R1 TO 3K 5% 402 TO FIX SPDIF PLL FILTER
 117) CHANGED AD1 INPUT ON SPDIF RCVR (U2) TO AUD_3V_RUN_F TO CHANGE I2C ADDR TO 010
 6/16/04
 118) REARRANGED SCHEMATIC PAGES TO BE MORE DESIGN REUSE COMPLIANT
 119) RENAMED POWER NETS TO BE DESIGN REUSE COMPLIANT
 6/28/04
 120) REASSIGNED CS4816 (U2) TO I2C ADDRESS 0X22 (AD=001) ON I2S-B BUS FOR Q41B/Q51 COMPATIBILITY
 7/02/04
 **** RELEASED FOR Q41B EVT

 **** SCHEMATIC UNDER Q41B PROJECT, NAME CHANGED TO SCHEM,CRYSTAL,Q41B
 9/22/04
 121> CHANGED PCM3052 TO PCM3052A WITH NEW FOOTPRINT
 10/12/04
 122> ADD 2 1KOHM FROM L AND R CHANNEL OUTPUT OF MAX9722 TO AUD_GND
 123> ADD 100KOHM ON PIN 15 OF CS8416 TO PULL-UP, NO STUFF THE PULL-DOWN
 124> REPLACE R48, R49, R50, R51 WITH 20.5KOHM
 125> CHANGE 2 FEEDBACK RESISTORS R41, R42 ON LM4866LQ TO 20.5OHM
 126> CHANGE C42, C43 TO 0.1UF
 127> CHANGE SPEAKER AMP TO NATIONAL SEMI. LM4866LQ
 128> ADD MAX9510 AS LDO FOR CS8416
 10/15/04
 129> CHANGE SIGNAL: AUDIO_GPIO_11 TO SPDIF_GPO0
 130> CHANGE SIGNAL: AUDIO_LO_METAL_PLUG_L TO AUDIO_LO_OPTICAL_PLUG_L
 131> CHANGE SIGNAL: AUDIO_LI_METAL_PLUG_L TO AUDIO_LI_OPTICAL_PLUG_L

 12/16/04
 132> SCHEMATIC RELEASE FOR PRODUCTION
 01/07/05
 133> CHANGE ALL 138S0518 TO 138S0550
 134> SCHEMATIC RELEASE FOR PRODUCTION (BOM REV B)

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SIGNAL & POWER ALIASES


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NONE	5	14	

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FUNCTIONAL TEST POINTS

	SIG_NAME	FUNC_TEST	FUNC_QTY	
E1	AUDIO_LO_DET_L	TRUE		7 10
E2	AUDIO_LO OPTICAL PLUG L	TRUE		7 10
E3	AUDIO_LI_DET_L	TRUE		7 11
E4	AUDIO_LI OPTICAL PLUG L	TRUE		7 11
E5	I2S0_RESET_L	TRUE		7 8
E6	I2S1_RESET_L	TRUE		7 12
E7	PP3V3_RUN_AUDIO	TRUE		7 8 10 11 12
E8	I2C_SDA	TRUE		7 8 12
E9	I2C_SCL	TRUE		7 8 12
E10	SLEEP_LED	TRUE		7
E11	SLEEP_LED_GND	TRUE		7
E12	I2S1_DEV_TO_SB_DTI	TRUE		7 12
E13	I2S1_SYNC	TRUE		7 12
E14	I2S1_BITCLK	TRUE		7 12
E15	I2S0_DEV_TO_SB_DTI	TRUE		7 8
E16	I2S0_SB_TO_DEV_DTO	TRUE		7 8
E17	I2S0_BITCLK	TRUE		7 8 12
E18	I2S0_MCLK	TRUE		7 12
E19	AUDIO_SPKR_MUTE	TRUE		7 9
E20	AUDIO_LO_MUTE_L	TRUE		7 10
E21	AUDIO_EXT_MCLK_SEL	TRUE		7 12
E22	SPDIF_GPO0	TRUE		7 12
E23	AUD_GND	TRUE	4	7 8 9
E24	PP5V_PWRON_AUDIO1	TRUE	3	7 9 10
E25	PP5V_PWRON_AUDIO0	TRUE		7 8 12
		TRUE	3	7 8 12

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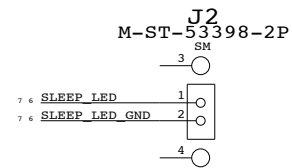
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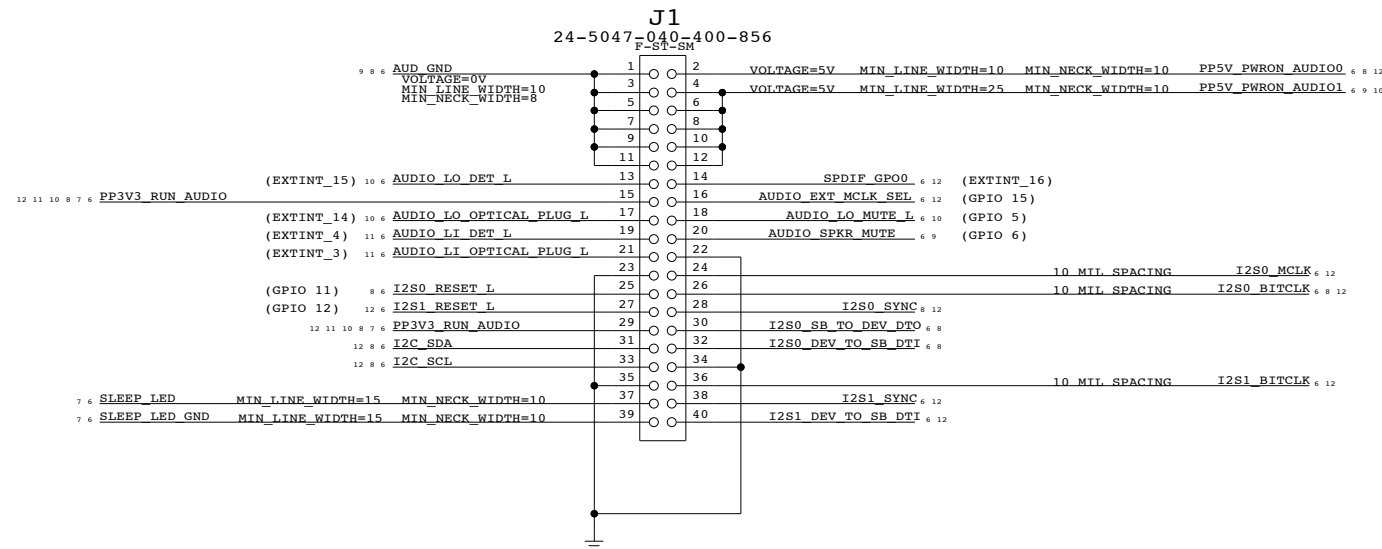
SLEEP LED CONNECTOR

CRITICAL



AUDIO CONNECTOR (TO MLB)

CRITICAL



AUDIO CONNECTORS

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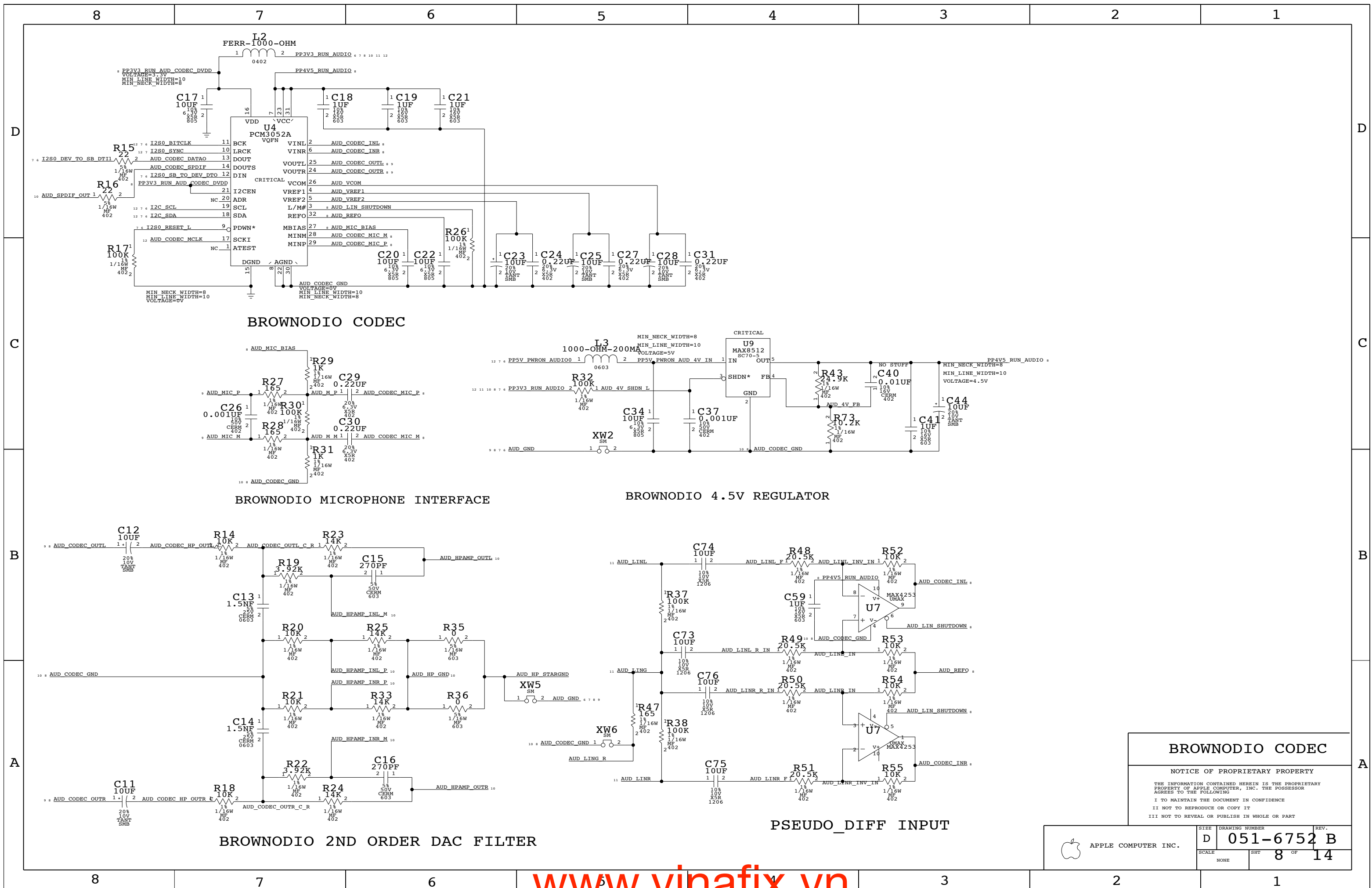
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BROWNODIO CODEC

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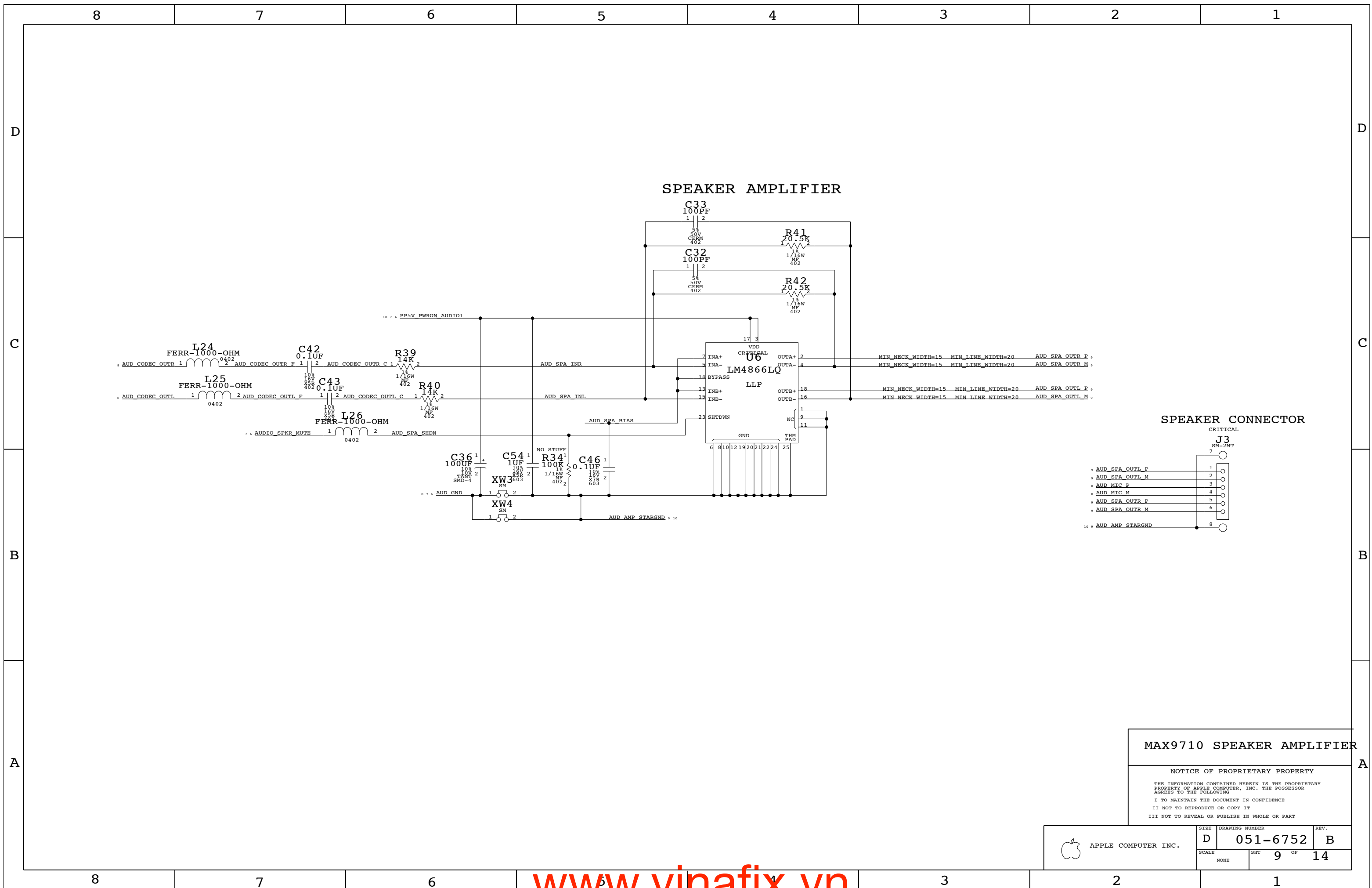
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	SCALE	8	14



SPEAKER AMPLIFIER

SPEAKER CONNECTOR

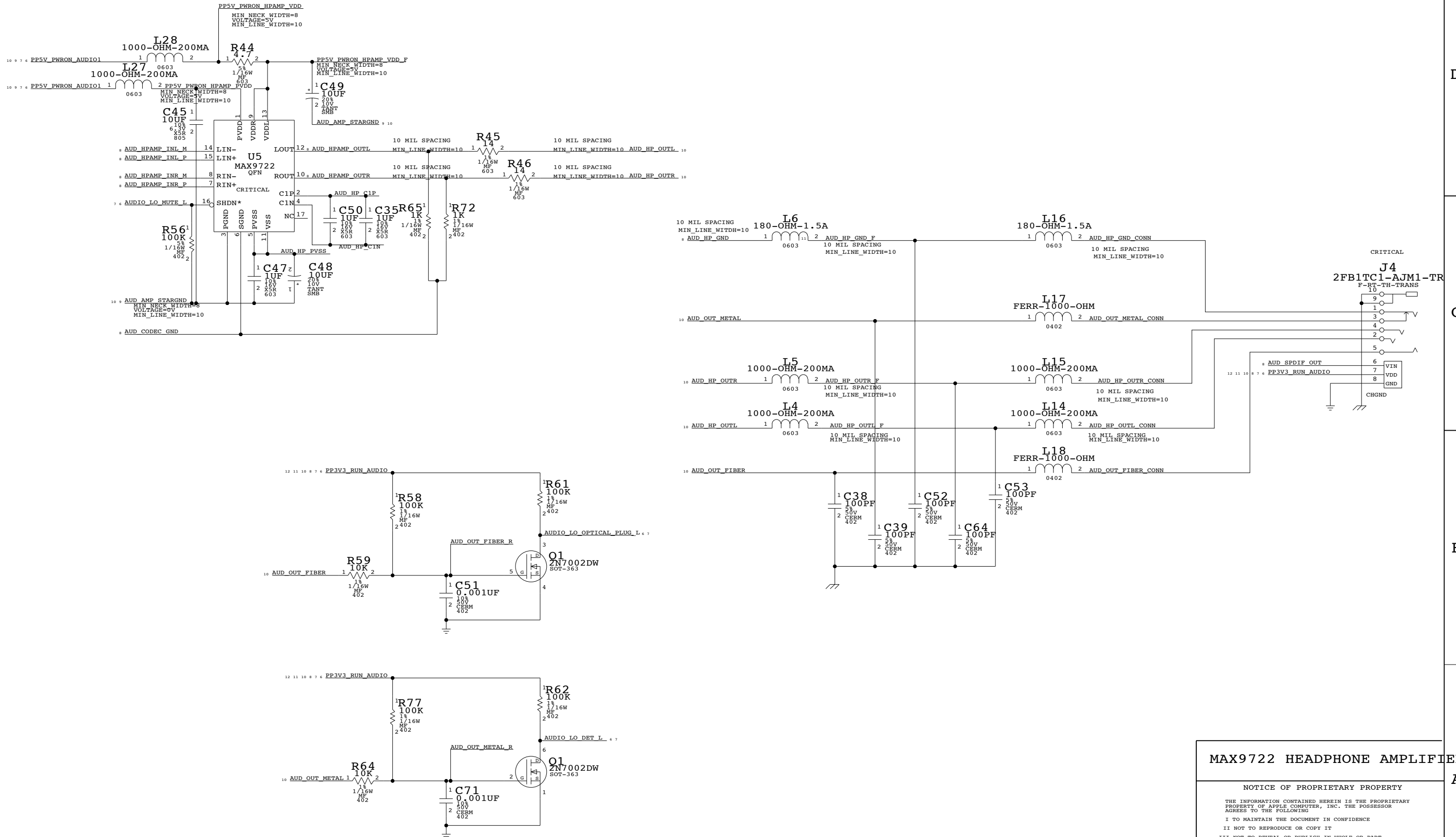
MAX9710 SPEAKER AMPLIFIER

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HEADPHONE AMPLIFIER



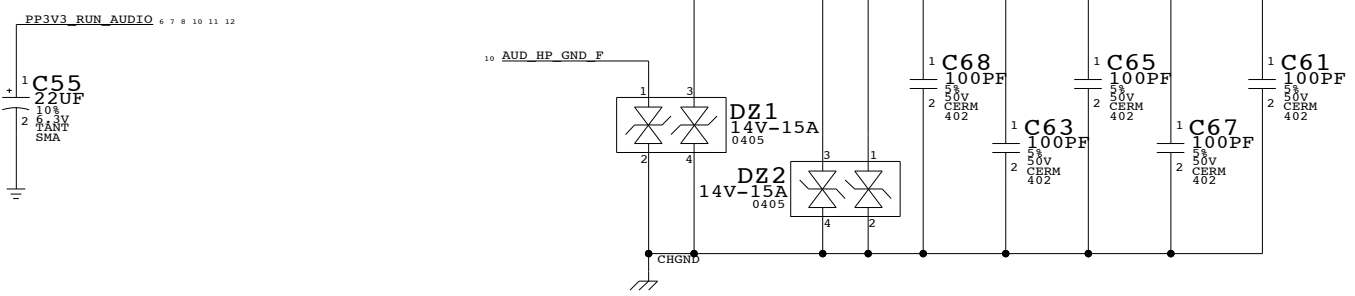
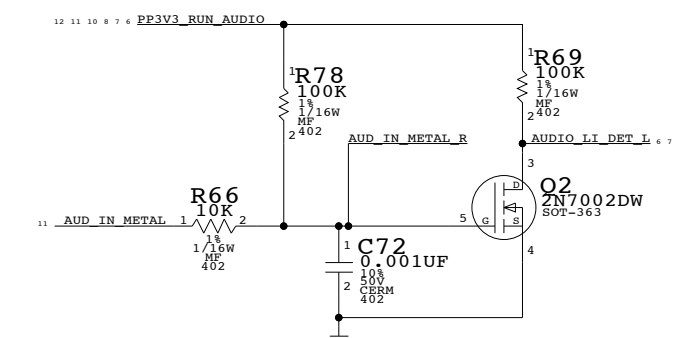
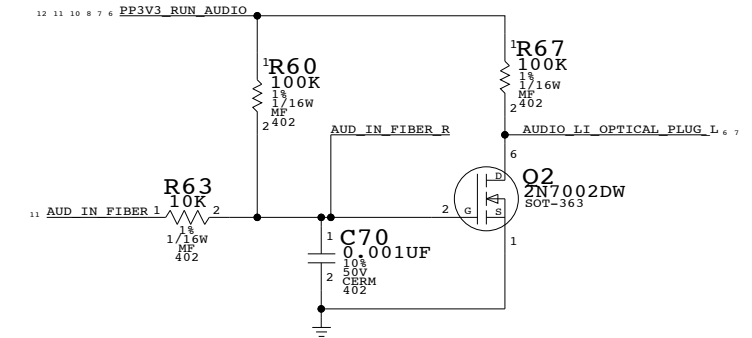
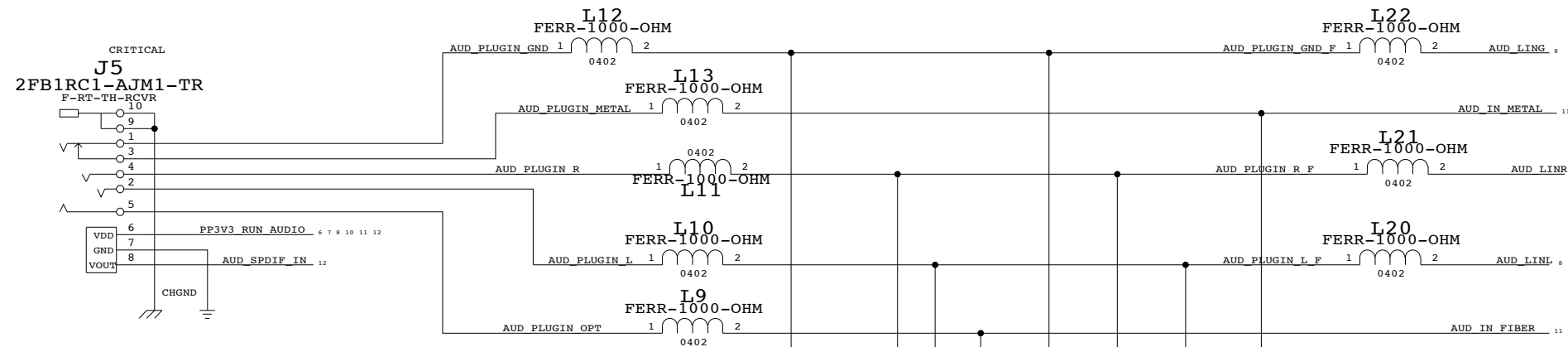
MAX9722 HEADPHONE AMPLIFIER

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NONE			

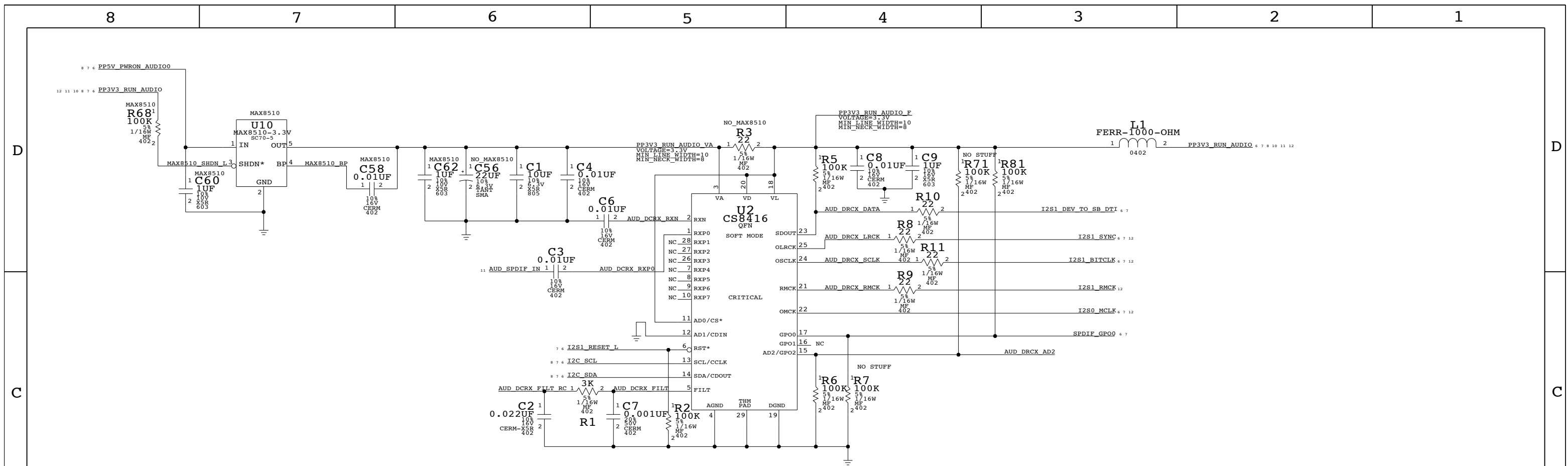
LINE IN FILTER (PSEUDO-DIFF INPUT) ON CODEC PAGE MIC PREAMP INCLUDED IN PCM3052A CODEC



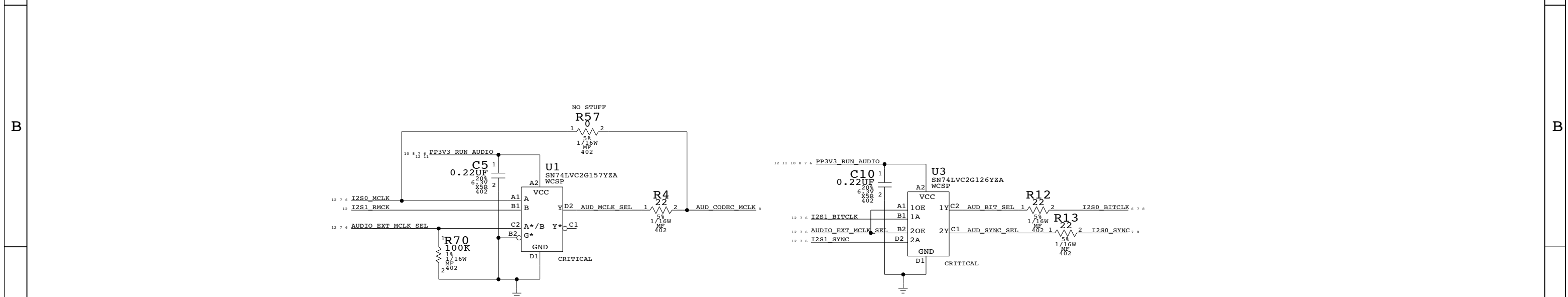
LINE IN

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APPLE COMPUTER INC.	SIZE D SCALE NONE	DRAWING NUMBER 051-6752	REV. B
	SHEET 11 OF 14		



SPDIF RECEIVER



CS8416 SPDIF RECEIVER

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6752	B
SCALE	NONE	SHT	12 OF 14

	8	7	6	5	4	3	2	1	
D	<pre> *** Signal Cross-Reference for the entire design *** AUDIO_EXT_MCLK_SEL 6C5> 7B4<> 12A4<> 12A7<> AUDIO_L1_DET_L 4D5> 7B5<> 11B1<> AUDIO_L1_OPTICAL_PLUG_L 6D5> 7B5<> 11C1<> AUDIO_L0_DET_L 6D5> 7B5<> 10A5<> AUDIO_L0_MUTE_L 6C5> 7B4<> 10C3<> AUDIO_L0_OPTICAL_PLUG_L 6D5> 7B5<> 10B5<> AUDIO_SFRM_MUTE 6C5> 7B4<> 9B7< AUD_AV_FB 8C4<> AUD_AV_SDRN_L 8C5<> AUD_AHP_STARGND 9B2<> 9B5<> 10C8< 10D6< AUD_BIT_SEL 12B4<> AUD_CODEC_DATA0 8D8<> AUD_CODEC_GND 8A4< 8A5<> 8A8< 8B4<> 8B7< 8C7< 10C6< AUD_CODEC_HP_OUTL_C 8B8< AUD_CODEC_HP_OUTR_C 8A8< AUD_CODEC_INL 8B3<> 8D6< AUD_CODEC_INR 8A3<> 8D6< AUD_CODEC_MCLK 8C8< 12B5< AUD_CODEC_MIC_M 8B6< 8C6< AUD_CODEC_MIC_P 8C6< 8C6< AUD_CODEC_OUTL 8B8< 8D6< 9C8< AUD_CODEC_OUTL_C 9C7< AUD_CODEC_OUTL_C_R 8B7< AUD_CODEC_OUTL_F 9C7< AUD_CODEC_OUTR 8A6< 8D6< 9C8< AUD_CODEC_OUTR_C 9C7< AUD_CODEC_OUTR_C_R 8A7< AUD_CODEC_OUTR_F 9C7< AUD_CODEC_SPOIF 8D8<> AUD_DCKR_FILL 12C3<> AUD_DCKR_FILL_RC 12C6< AUD_DCKR_RSN 12D5< AUD_DCKR_SFRM 12C5< AUD_DCKR_AD2 12C3<> AUD_DCKR_DATA 12D4<> AUD_DCKR_LACK 12D4<> AUD_DCKR_BMCK 12C4<> AUD_DCKR_SCLK 12C4<> AUD_GND 6C5> 7B5<> 8A5<> 8B6<> 9B6<> AUD_HPAMP_INL_M 8B6< 10D8< AUD_HPAMP_INL_P 8A6< 10D8< AUD_HPAMP_INR_M 8A6< 10C8< AUD_HPAMP_INR_P 8A6< 10C8< AUD_HPAMP_OUTL 8B6< 10D7<> AUD_HPAMP_OUTR 8A6< 10C7<> AUD_HP_C1N 10C6<> AUD_HP_C1P 10C6<> AUD_HP_GND 8A6< 10C3< AUD_HP_GND_CONN 10C2<> AUD_HP_GND_F 10C4< 11B6< AUD_HP_OUTL 10B5< 10D5< AUD_HP_OUTL_CONN 10B2<> AUD_HP_OUTL_F 10B4< AUD_HP_OUTR 10C3< 10C5< AUD_HP_OUTR_CONN 10C2<> AUD_HP_OUTR_F 10C4< AUD_HP_PRES 10C4< AUD_HP_STARGND 8A5<> AUD_IN_FIBER 11C3<> 11C3< AUD_IN_FIBER_R 11C2<> AUD_IN_METAL 11B3< 11C3< AUD_IN_METAL_R 11B2<> AUD_LING 8A5< 11C3< AUD_LING_R 8A5<> AUD_LINL 8B5< 11C3< AUD_LINL_F 8B4< AUD_LINL_IN 8A4<> AUD_LINL_INV_IN 8B4<> AUD_LINL_R_IN 8A4< AUD_LINR 8A5< 11C3< AUD_LINR_F 8A4< AUD_LINR_IN 8A4<> AUD_LINR_INV_IN 8A4<> AUD_LINR_IN 8A4< AUD_LIN_SHUTDOWN 8A3<> 8B3<> 8D7<> AUD_MCLK_SEL 12B6< AUD_MIC_BIAS 8C7< 8C7<> AUD_MIC_M 8B7< 9B2<> AUD_MIC_P 8C7< 9B2<> AUD_M_M 8B7< AUD_M_P 8C7< AUD_OUT_FIBER 10B5< 10B7< AUD_OUT_FIBER_CONN 10B5<> AUD_OUT_FIBER_R 10B5<> AUD_OUT_METAL 10A7< 10C5< AUD_OUT_METAL_CONN 10C2<> AUD_OUT_METAL_R 10A5<> AUD_PLUGIN_GND 11C7<> AUD_PLUGIN_GND_F 11C4< AUD_PLUGIN_L 11C7<> AUD_PLUGIN_L_F 11C4< AUD_PLUGIN_METAL 11C7<> AUD_PLUGIN_OPT 11C7<> AUD_PLUGIN_R 11C7<> AUD_PLUGIN_R_F 11C4< AUD_SFO 8A3< 8D7<> AUD_SPA_BIAS 9C5<> AUD_SPA_INL 9C5< AUD_SPA_INR 9C5< AUD_SPA_OUTL_M 9B2<> 9C2<> AUD_SPA_OUTL_P 9B2<> 9C2< AUD_SPA_OUTR_M 9B2<> 9C2<> AUD_SPA_OUTR_P 9B2<> 9C2< AUD_SPA_SHDN 9B6< AUD_SPOIF_IN 11C7< 12C6< AUD_SPOIF_OUT 8D8< 10C3< AUD_SYNC_SEL 12A4<> AUD_VCOM 8D7<> AUD_VREF1 8D7<> AUD_VREF2 8D7<> CORG01 2D2> 12C_SCL 6D5> 7A5<> 8D6< 12C6< 12C_SDA 6D5> 7A5<> 8D6<> 12C6<> 12B0_B1CTRL 6C3> 7B3<> 8D8< 12B3< 12B0_DVY_PO_BB_DTI 6C5> 7A6<> 8D8< 12B0_MCLK 6C5> 7B3<> 12B7<> 12C3< 12B0_RESET_L 6D5> 7B5<> 8C8< 12B0_SB_TO_DVY_VDD 6C5> 7A6<> 8D8< 12B0_SYNC 7B4<> 8D8< 12A3< 12B1_B1CTRL 6C5> 7A3<> 12B4<> 12C3< 12B1_DVY_PO_BB_DTI 6C5> 7A6<> 12D3< 12B1_RESET_L 6D5> 7B5<> 12C6< 12B1_BMCK 12B7<> 12C3< 12B1_SYNC 6C5> 7A6<> 12A4<> 12D3< MAX9310_BP 12D7<> MAX9310_BSDI_L 12D8<> MIDDLE_SCHW_GND 2C2< PP3V3_BUN_AUDIO 6D5> 7A5<> 7B6<> 8C6< 8D6< 10A7< 10B7< 10C8< 11B3< 11B7< 11C3< 11C7< 12B4< 12B6< 12D2< 12D8< PP3V3_BUN_AUDIO_F 12D4< PP3V3_BUN_AUDIO_RA 12D8<> PP3V3_BUN_AUDIO_VDD0 8D8< 8D8< PP4V5_BUN_AUDIO 8B4< 8C2<> 8D6< PP5V_PERSON_AUDIO0 6C5> 7B3<> 8C4< 12D8< PP5V_PERSON_AUDIO1 6C5> 7B3<> 9C4< 10D8< 10D8< PP5V_PERSON_AUDIO_AV_IN 8C5< PP5V_PERSON_HPAMP_VDD 10D7< PP5V_PERSON_HPAMP_VDD 10D7< PP5V_PERSON_HPAMP_VDD_F 10D6< SLEEP_LED 6C5> 7A6<> 7C6<> SLEEP_LED_GND 6C5> 7A6<> 7C6<> SDIF_GP00 6C5> 7B4<> 12C3<> </pre>								C
B									B
A									A
	8	7	6	5	4	3	2	1	

	8	7	6	5	4	3	2	1	
D	<p>*** Part Cross-Reference for the entire design ***</p> <pre> C1 CAP 12 C2 CAP 12 C3 CAP 12 C4 CAP 12 C5 CAP 12 C6 CAP 12 C7 CAP 12 C8 CAP 12 C9 CAP 12 C10 CAP 12 C11 CAP_P 8 C12 CAP_P 8 C13 CAP 8 C14 CAP 8 C15 CAP 8 C16 CAP 8 C17 CAP 8 C18 CAP 8 C19 CAP 8 C20 CAP 8 C21 CAP 8 C22 CAP 8 C23 CAP_P 8 C24 CAP 8 C25 CAP_P 8 C26 CAP 8 C27 CAP 8 C28 CAP_P 8 C29 CAP 8 C30 CAP 8 C31 CAP 8 C32 CAP 9 C33 CAP 9 C34 CAP 8 C35 CAP 10 C36 CAP_P 9 C37 CAP 8 C38 CAP 10 C39 CAP 10 C40 CAP 8 C41 CAP 8 C42 CAP 9 C43 CAP 9 C44 CAP_P 8 C45 CAP 10 C46 CAP 9 C47 CAP 10 C48 CAP_P 10 C49 CAP_P 10 C50 CAP 10 C51 CAP 10 C52 CAP 10 C53 CAP 10 C54 CAP 9 C55 CAP_P 11 C56 CAP_P 12 C58 CAP 12 C59 CAP 8 C60 CAP 12 C61 CAP 11 C62 CAP 12 C63 CAP 11 C64 CAP 10 C65 CAP 11 C66 CAP 11 C67 CAP 11 C68 CAP 11 C70 CAP 11 C71 CAP 10 C72 CAP 11 C73 CAP 8 C74 CAP 8 C75 CAP 8 C76 CAP 8 D81 SUPP9_TRANSIENT_4P1 11 D82 SUPP9_TRANSIENT_4P1 11 J1 COM_F408T_D_SM 7 J2 COM_H29T_S2HT_SM 7 J3 COM_H49T_W218 9 J4 COM_F88T_S8D1PFRAN_TH1 10 J5 COM_F88T_S8D1PFCVR_TH1 11 L1 IND 12 L2 IND 8 L3 IND 8 L4 IND 10 L5 IND 10 L6 IND 10 L9 IND 11 L10 IND 11 L11 IND 11 L12 IND 11 L13 IND 11 L14 IND 10 L15 IND 10 L16 IND 10 L17 IND 10 L18 IND 10 L20 IND 11 L21 IND 11 L22 IND 11 L24 IND 9 L25 IND 9 L26 IND 9 L27 IND 10 L28 IND 10 Q1 TRA_2H7002DW 10 Q2 TRA_2H7002DW 11 R1 RES 12 R2 RES 12 R3 RES 12 R4 RES 12 R5 RES 12 R6 RES 12 R7 RES 12 R8 RES 12 R9 RES 12 R10 RES 12 R11 RES 12 R12 RES 12 R13 RES 12 R14 RES 8 R15 RES 8 R16 RES 8 R17 RES 8 R18 RES 8 R19 RES 8 R20 RES 8 R21 RES 8 R22 RES 8 R23 RES 8 R24 RES 8 R25 RES 8 R26 RES 8 R27 RES 8 R28 RES 8 R29 RES 8 R30 RES 8 R31 RES 8 R32 RES 8 R33 RES 8 R34 RES 9 R35 RES 8 R36 RES 8 R37 RES 8 R38 RES 8 R39 RES 9 R40 RES 9 R41 RES 9 R42 RES 9 R43 RES 8 R44 RES 10 R45 RES 10 R46 RES 10 R47 RES 8 R48 RES 8 R49 RES 8 R50 RES 8 R51 RES 8 R52 RES 8 R53 RES 8 R54 RES 8 R55 RES 8 R56 RES 10 R57 RES 12 R58 RES 10 R59 RES 10 R60 RES 11 </pre>								D
C									C
B									B
A									A
	8	7	6	5	4	3	2	1	