3. All crystals & oscillator values are in hertz.
2. All capacitance values are in microfarads.
### Revision Notes

<table>
<thead>
<tr>
<th>Number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Moved Q3001-Q3004, D3001, D3002, R3044, R3046, R3048, R3070, R3050, R3052, R3054 from Page 27 to page 16 to allow sync with Gila</td>
</tr>
<tr>
<td>2</td>
<td>Moved AGP Vref (R4802, R4803, C4818) circuit to M11 specific page (49)</td>
</tr>
<tr>
<td>3</td>
<td>Changed R2191 to pulldown on SYS_LED</td>
</tr>
<tr>
<td>4</td>
<td>Added 10 mil MIN_LINE_WIDTH and MIN_NECK_WIDTH to BKFD_PROT_EN_L</td>
</tr>
<tr>
<td>5</td>
<td>Changed MIN_LINE_WIDTH of PP5V4_CHGR_LDO to 10 mils</td>
</tr>
<tr>
<td>6</td>
<td>Moved J790 (backup battery/R USB connector) to page 18 for syncing with Logic</td>
</tr>
<tr>
<td>7</td>
<td>Moved J1600 (BT/USB connector) to page 18 for syncing with Logic</td>
</tr>
<tr>
<td>8</td>
<td>Moved C860-C865 (PBus hold-up caps) to page 18 for syncing with Logic</td>
</tr>
<tr>
<td>9</td>
<td>Moved ZT9900-ZT9903 (EMI vias) to page 18 for syncing with Logic</td>
</tr>
<tr>
<td>10</td>
<td>Moved SP500-SP505 and SP9900 to (speaker wire clips) to page 18 for syncing with Logic</td>
</tr>
<tr>
<td>11</td>
<td>Moved ZT500-ZT505, ZT510, and ZT511 (plated screw holes) to page 18 for syncing with Logic</td>
</tr>
<tr>
<td>12</td>
<td>Moved BS510 to page 18 for syncing with Logic</td>
</tr>
<tr>
<td>13</td>
<td>Moved J2130 (trackpad connector) to page 18 for syncing with Logic</td>
</tr>
<tr>
<td>14</td>
<td>Changed C2150 to 20%</td>
</tr>
<tr>
<td>15</td>
<td>Added 10 mil MIN_LINE_WIDTH and MIN_NECK_WIDTH to KBDLED_ANODE and KDBLED_RETURN</td>
</tr>
<tr>
<td>16</td>
<td>Changed C2115 to R2116 (3.32K 1% 402) to divide ALS output to 2.5V</td>
</tr>
<tr>
<td>17</td>
<td>Changed PCI from shasta to PCI_SB to allow desktops to insert series R's</td>
</tr>
<tr>
<td>18</td>
<td>Changed R2150 to 8.25 to reduce LED drive current to 20mA</td>
</tr>
<tr>
<td>19</td>
<td>Changed R2150 to 8.25 to reduce LED drive current to 20mA</td>
</tr>
<tr>
<td>20</td>
<td>Changed Q2113 to second FET in Q5909</td>
</tr>
<tr>
<td>21</td>
<td>Changed SMU_ADAPTER_ID to SMU_ONEWIRE</td>
</tr>
<tr>
<td>22</td>
<td>Added R1620 and R1621 to divide ALS output down to 2.5V</td>
</tr>
<tr>
<td>23</td>
<td>Added alias from TP_SATA_CLK25M to SATA_CLK25M</td>
</tr>
<tr>
<td>24</td>
<td>Changed PPVCORE_RUN_CPU connection to XW592 to _PP1V5_RUN_FET</td>
</tr>
<tr>
<td>25</td>
<td>Changed C720 to 0.22uF</td>
</tr>
<tr>
<td>26</td>
<td>Changed R800 and R810 to 1/2W 1206 10mohm</td>
</tr>
<tr>
<td>27</td>
<td>Changed C1068 to NO STUFF</td>
</tr>
<tr>
<td>28</td>
<td>Removed Q1117 and C1114</td>
</tr>
<tr>
<td>29</td>
<td>Changed L1115 to 2.2uH IHLP5050CE (152S0152)</td>
</tr>
<tr>
<td>30</td>
<td>Changed C1121 to 680pF 402</td>
</tr>
<tr>
<td>31</td>
<td>Changed R1102 to 20K 1% 402</td>
</tr>
<tr>
<td>32</td>
<td>Changed R800 and R810 to 1/2W 1206 10mohm</td>
</tr>
<tr>
<td>33</td>
<td>Changed C720 to 0.22uF</td>
</tr>
<tr>
<td>34</td>
<td>Changed PPVCORE_RUN_CPU connection to XW592 to _PP1V5_RUN_FET</td>
</tr>
<tr>
<td>35</td>
<td>Sync with Gila (Q45) to fix several power disconnects</td>
</tr>
<tr>
<td>36</td>
<td>Added aliases on page 5 to set unused CKE, CS, and MUX controls back to TP</td>
</tr>
<tr>
<td>37</td>
<td>Sync with Logic (Q43) to get DVO contraints</td>
</tr>
<tr>
<td>38</td>
<td>Changed R3671 to 100K 0.1% to adjust the Tdiode range</td>
</tr>
<tr>
<td>39</td>
<td>Changed C3671 to 10uF 20% 6.3V to adjust the Tdiode range</td>
</tr>
<tr>
<td>40</td>
<td>Changed R3672 to 40.2K 0.1% to adjust the Tdiode range</td>
</tr>
<tr>
<td>41</td>
<td>Changed R3676 to 100K 0.1% to adjust the Tdiode range</td>
</tr>
<tr>
<td>42</td>
<td>Changed C3676 to 10uF 20% 6.3V to adjust the Tdiode range</td>
</tr>
<tr>
<td>43</td>
<td>Changed R3677 to 40.2K 0.1% to adjust the Tdiode range</td>
</tr>
<tr>
<td>44</td>
<td>Mirrored FL9020 and FL9021 to fix layout</td>
</tr>
<tr>
<td>45</td>
<td>Changed L970 to 152S0154 (10uH) to reduce size</td>
</tr>
<tr>
<td>46</td>
<td>Removed 197S0703 as alternate for 197S0037 (25MHz Vesta crystal)</td>
</tr>
<tr>
<td>47</td>
<td>Changed all references to SMU_MANUAL_RESET_L to SMU_RESET_L</td>
</tr>
<tr>
<td>48</td>
<td>Removed DC current limit circuit (U870 and associated discretes)</td>
</tr>
<tr>
<td>49</td>
<td>Added BOMOPTION for 2.8V CPU Avdd LDO</td>
</tr>
<tr>
<td>50</td>
<td>Changed R4800 to 2.2 ohm 603, C4811 to 1uF 402, and C4816 to 0.1uF 402 in U3Lite AGP Avdd filter.</td>
</tr>
<tr>
<td>51</td>
<td>Changed R1610 (series R on SMU_ONEWIRE output) to 0 ohm</td>
</tr>
<tr>
<td>52</td>
<td>Added R1611 (1k pullup to PP3V3_ALL) on ADAPTER_ID to power SMU_ONEWIRE interface</td>
</tr>
<tr>
<td>53</td>
<td>Changed C8160-C8160 (SATA AC coupling caps) to 0.01uF per Marvell recommendation</td>
</tr>
<tr>
<td>54</td>
<td>Added NO_TEST properties to CPUVCORE_GNDSENSE and CPUVCORE_SENSE</td>
</tr>
<tr>
<td>55</td>
<td>Changed MIN_LINE_WIDTH of PP5V4_CHGR_LDO to 10 mils</td>
</tr>
<tr>
<td>56</td>
<td>Added 10 mil MIN_LINE_WIDTH and MIN_NECK_WIDTH properties to ALS1_PHOTODIODE and ALS1_OP_IN</td>
</tr>
<tr>
<td>57</td>
<td>Added 10 mil MIN_LINE_WIDTH and MIN_NECK_WIDTH properties to CPUVCORE_CM_N and CPUVCORE_CS_N</td>
</tr>
<tr>
<td>58</td>
<td>Changed R5019 to 26.7K 1% to increase GPU Vcore current limit (rdar://3510721)</td>
</tr>
<tr>
<td>59</td>
<td>Changed C3676 to 10uF 20% 6.3V to adjust the Tdiode range</td>
</tr>
<tr>
<td>60</td>
<td>Changed C3677 to 40.2K 0.1% to adjust the Tdiode range</td>
</tr>
</tbody>
</table>

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### Preliminary
3.3V Regulator

Vesta Core / Misc

Power Supply: 12V (System supply for bus power)
- VESTA-BV (Default 12V power)

Regulator will be in continuous mode.

- VBA1V2_BURST / VESTA1V2_PULSE

1/16W 1% Resistor

SMU_ACIN

R1261 1/16W 1% 10K

C1265 402 MF 5%

MIN_NECK_WIDTH=10 mil

VOLTAGE=19V

DP1260 1.5A-24V

52 SOT-363

F1265 12

R1265 324K 1/16W 1%

VESTA_ENET_LOWPWR

100K 402 MF 5%

R1295 402 22uF 6.3V 20%

C1271 402 100uF POLY 6.3V 20%

C1281 402 0.1uF 10V 20%

MIN_NECK_WIDTH=8 mil

MIN_LINE_WIDTH=25 mil

Ethernet LowPwr

VIN

1/16W 5%

R1292 324K 1/16W 1%

TP_VESTA_DNC_E9

TP_VESTA_DNC_C9

TP_VESTA_DNC_B9

Schmitt trigger

VESTA_RESET_L

VESTA_MISC

3.3V Regulator

2.5V LDO

1.2V Regulator

Port Power Switch
NOTE: CPU current/voltage monitoring

SYS_KBDLED

SYS_POWERFAIL_L

SYS_DOOR_AJAR_L

SYS_DRIVE_BAY_INT_L

FAN_RPM4 ALS1_OUT

FAN_RPM5

PP3V3_ALL_RTC

Portable

1.7

15 MIL SPACING

SMU_PWRSEQ_P9_6

SMU_PWRSEQ_P1_3

SMU_PWRSEQ_P1_2

SMU_PWRSEQ_P1_1

SMU_CHARGE_BATT

I2C_SMU_D_SCL

I2C_SMU_D_SDA

MIN_NECK_WIDTH=10 mil

Master: Link

Alternate Functions

Portable

Consumer

Tower & Server

8

7

6

5

4

3

2

1

System Management Unit

Real Time Clock

SMU Pull-ups / pull-down

SMU_CLK10M_XOUT

SMU_VREF

PP3V3_ALL_SMU

PP3V3_ALL_RTC

Power alias required by this page:
- PP3V3_ALL_RTC
- PP3V3_ALL_SMU
Remote Temperature Sensors
Place each cap close to associated transistor

Sensor Selection
Place 3 MAX1989 inputs can connect to two different sensors. These sensors should be close to MAX1989 minimizing stubs.
other Shasta supplies.

Power Sequencing:

Must power Shasta VCore rail before any

Power Sequencing:

Must power Shasta rail before any other Shasta supplies.
Req = R3a + R3b
Vout = 2V * (Req / (R1+Req)) = 1.2V
When GPUVCORE_CNTL_L = 0, Vout = 1.2V
Vout = 2V * (R2 / (R1+R2)) = 1.0V
to get 1.2V at the high input
Changed R5050 from 30.1K to 37.4K
NOTE: This page does not specify a BootROM part number. Mark use a TABLE_ITEM expect to declare 07500 part number.

Signal aliases required by this page:
- _PP3V3_PCI

Power aliases required by this page:
- _PP3V3_PCI

.bootrom

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Power Sequencing:

- _PPVIO_PCI can be same as _PP3V3_PCI

**Page Notes**

- Power aliases required by this page:
  - _PPVIO_PCI
  - _PP3V3_PCI
  - _PPVIO_PCI (to_PPVIO_PCI or _PP3V3_PCI
  - Note: All rails MUST implement the same power state (PPVIO or PP3V3) for
  - 3.3V Vpp support
  - Not provide _PME or _PME support.

- BOM options provided by this page:
  - _PP2V5_PCI
  - _PP3V3_PCI

- Power Sequencing:

  1. Assert RESET
     - _PCI_CLK33M_CBUS
     - PCI_DEVSEL_L
     - PCI_CBE_L<0>
     - PCI_AD<23>
     - PCI_AD<14>
     - PCI_AD<4>
     - PCI_AD<3>
     - CBUS_VR_EN_L_PU

- CardBus Implementation Data:

  - This CardBus Implementation Data
  - Not provide _PPVIO or 12V Vpp support.

- 10K

- 402

- 2

- 1/16W

- MF

- 5%

- 45

- 46

- 47

- CBUS_VR_EN_L_PU

- 49

- 2. _PPVIO_PCI
  - 1. Assert RESET

- **PC Card Power Switch**

  - Make sure Vcc and Vpp are wide
gain/planes to minimize inductance.

- **PC Card/CardBus Connector**

- **CardBus Interface**

- **Master: Fizzy**

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- Property of Apple Computer, Inc. The possessor

- Agrees to the following

- WARNING: Do not to expose to excess heat of up to 125C.

- **PCB Dimensions**

  - www.vinafix.vn
NOTE: Target differential impedance for Secondary Length:
- Line To Line: 15 mils

BOM options provided by this page:
- (NONE)

Signal aliases required by this page:
- Power aliases required by this page:

Page Notes

Net Spacing Type: SATA

Line To Line: 15 mils
Length Tolerance: 50 mils outer
Primary Max Resp: 100 kOhms inner
Secondary Max Resp: 100 kOhms
Secondary Tolerance: 100 mils

NOTE: Leave differential impedance for SATA data pairs to 100 ohms.

All coupling required for any BGA part must:
- Recommend 2.0uf at primary side to Shasta.
- (Cap provided by device page)
Page Notes

Power aliases required by this page:

- (NONE)
- (NONE)

Power aliases required by this page:

(SHRT)

BOM options provided by this page:

(SHRT)

Place one cap at each pin of transformer

Ethernet Connector

C8700  C8701  C8702  C8703

ENET_CTAP<0>  ENET_CTAP<1>  ENET_CTAP<2>  ENET_CTAP<3>

ENET_MDI_P<0>  ENET_MDI_P<1>  ENET_MDI_P<2>  ENET_MDI_P<3>

ENET_MDI_N<0>  ENET_MDI_N<1>  ENET_MDI_N<2>  ENET_MDI_N<3>

ENET_RJ45_P<0>  ENET_RJ45_P<1>  ENET_RJ45_P<2>  ENET_RJ45_P<3>

ENET_RJ45_N<0>  ENET_RJ45_N<1>  ENET_RJ45_N<2>  ENET_RJ45_N<3>

C8705

ENET_RJ45_0

ENET_RJ45_1

ENET_RJ45_2

ENET_RJ45_3

R8705

75 402 MF 1/16W 5%

R8706

5% 1/16W 402 75

R8707

5% 402 75

R8708

402 MF 1/16W 5%

C8705

1808 3KV 10% 100pF CERM

C8701

10V 0.1uF CERM 402

C8702

20% 10V 0.1uF CERM 402

C8703

20% 10V 0.1uF CERM 402

C8704

20% 10V 0.1uF CERM 402

C8706

20% 10V 0.1uF CERM 402

C8707

20% 10V 0.1uF CERM 402

C8708

20% 10V 0.1uF CERM 402

R8710

NO STUFF 5% 1/10W 805 0

C8700

ENET_CTAP_COMMON

ENET_MDI_N<0>

ENET_MDI_P<0>

ENET_RJ45_P<0>

ENET_RJ45_N<0>

ENET_RJ45_P<1>

ENET_RJ45_N<1>

ENET_RJ45_P<2>

ENET_RJ45_N<2>

ENET_RJ45_P<3>

ENET_RJ45_N<3>

ENET_CTAP<0>

ENET_CTAP<1>

ENET_CTAP<2>

ENET_CTAP<3>

ENET_RJ45_P<0>  ENET_RJ45_N<0>
Page Notes

Power aliases required by this page:
- 3.3V, 5V, 12V
- 5VSB, 3.3VSB active, 5mA auxiliary

Signal aliases required by this page:
- (none)

Net aliases provided by this page:
- (none)

---

Modem Connector

Supports both The Last Dash and Q52 Modems

Removed 10uF bulk cap because modem connector is close to V5 power supply output cap.

---

Modem Interface

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Electrical Constraints

No series termination on PCI signals