1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

LINK

02/23/2004

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
03		316008	ENGINEERING RELEASED	02/23/04	?

EVT1

BOM Option Table

630-4843
630-4902

PCBA,LINK,Q51

BOM Options	STUFF	NO STUFF
DEVELOPMENT	√	
GPU_SS	√	
MPIC_NB		√
MPIC_SB	√	
PATA_3V3_LOGIC		√
PATA_5V_LOGIC	√	
PCI_64BIT		√
SMU_CPU_I2C	√	
SMU_CPU_JTAG		√
THERM_1	√	
THERM_1B		√
THERM_2	√	
THERM_2B		√
THERM_3	√	
THERM_3B		√
VESTA1V2_BURST		√
VESTA1V2_PULSE		√
VESTA_DS_ONLY_EN0	√	
VESTA_PWR_CLASS_0		√
AGP_BUSYSTOP		√
NO_SMU_I2C_D		√
EI_3TO1	√	
CPU_PLL_MEDIUM	√	
CPU_AVDD_2V8	√	
SB_HT_200M		√
M11CSP64	630-4843	
M11CSP128	630-4902	
INT_TMDS	√	
EXT_TMDS		√

Module Components

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S2835	1	IC,PPC970,1.8GHz,1.1V,80C,25W,576CBGA	U2900	CRITICAL	
343S0284	1	IC,U3LITE,V1.1,300MM,PBGA	U3	CRITICAL	
343S0283	1	IC,ASIC,SHASTA,V1.1,484BALL,PBGA	U2300	CRITICAL	
338S0154	1	IC,ATI,M11-CSP64,NO HEATSPREADER	U4900	CRITICAL	M11CSP64
338S0158	1	IC,ATI,M11-CSP128,NO HEATSPREADER	U4900	CRITICAL	M11CSP128
343S0288	1	IC,ASIC,VESTA,V1.1	U8600	CRITICAL	
341S1340	1	BOOTROM,PROTO,Q51	U7500	CRITICAL	
341S1394	1	SMU,PROTO,Q51	U1300	CRITICAL	

Alternates Components

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
343S0282	343S0284		U3	U3L,V1.1,200MM,PBGA

Schematic / PCB #'s

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-6532	1	SCHEM,LINK,Q51	SCH1	
820-1573	1	PCBF,LINK,Q51	PCB1	

DRAWING
TITLE=LINK
ABBREV=DRAWING
LAST_MODIFIED=Mon Feb 23 18:35:53 2004

DIMENSIONS ARE IN MILLIMETERS
XX ± _____
X.XX ± _____
X.XXX ± _____
ANGLES ± _____
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER / DESIGN CK /
ENG APPD / MFG APPD /
QA APPD / DESIGNER /
RELEASE / SCALE NONE

MATERIAL/FINISH NOTED AS APPLICABLE

SIZE D

Apple Computer Inc.

TITLE
SCHEM,LINK,Q51

DRAWING NUMBER 051-6532 REV. 03

SHT 1 OF 103

SYSTEM BLOCK DIAGRAM

J700
Nicky (PWR) Connector
P.7

Power Supply & Charger
P.7-12

J750
Battery Connector
P.7

U2900
CPU
NEO 10S
P.26-29

ELASTIC INTERFACE
44-BIT/Directional
APPLE PI
1.2V/600MHz

AGP BUS
4X/8X
1.5V/0.8V
32BITS
267/533MHZ

U3
U3LITE
CORE
PAGE 19
APPLE PI PAGE 25
AGP PAGE 35
HYPERTRANSPORT PAGE 42
MISC PAGE 21
MAIN MEMORY PAGE 32

U1300
SMU
P.13

I2C buses

RTC
P.13

Max1668
Thermal
P.15

I2C
Level shifting
P.17

MEMORY BUS
2.5V
333MHz
128BITS

J4010/J4020
DDR SDRAM DIMM 0

DDR SDRAM DIMM 1
SODIMM Connector
P.34

HYPERTRANSPORT
8-BIT/Direction
1.2V/400MHZ
CONTROL = 2.5V

U4900
ATI
M11
64/128MB
P.36,38-40

MEMORY CH. A (INTERNAL MEM)
MEMORY CH. C (INTERNAL MEM)
MEMORY CH. B (INTERNAL MEM)
MEMORY CH. D (INTERNAL MEM)

TMDS
RGB
DDC
J5900
DVI-I Connector
P.41

S-Video/Comp
J5960
S-Video Connector
P.41

LVDS
J5980
Inverter Connector
P.41

J5970
LCD Panel Connector
P.41

U2600
Pulsar Clock Gen
P.23-24
EI Clocks
VSP Clock
HT Clocks
AGP Clocks
PCI Clocks
SATA Clock

J1600
LEFT USB Bluetooth Connector
P.16

J8700
Gigabit Ethernet Connector
P.54

ENET Pairs
4 Datapairs @125MHz

U8600
VESTA
Core PAGE 12
ETHERNET PAGE 53
FIREWIRE PAGE 56

J8350
Hard DRIVE Connector
P.51

133MHz/3.3V/16 Bit

U8150
Serial ATA Bridge
P.50

1.5Gbps/1.2V/1 Bit/Directonal

Not Used

U2300
SHASTA
HYPERTRANSPORT PAGE 43
SATA1 SATA2 SATA PAGE 49
UATA PAGE 49
ETHERNET PAGE 52
FIREWIRE PAGE 55
CORE PAGE 20
PCI PAGE 44
GPIO/PCI64 PAGE 22
I2S PAGE 22 I2S0 SCCA I2S1 SCCB I2S2

8-bit TX & 8-bit RX
GMII (3.3V/125MHz)

1394 OHCI (3.3V/98MHz)

FW-A Pairs
2 Datapairs @200MHz
J9010
Firewire A Connector
P.57

FW-B pairs
2 Datapairs @400MHz
J9020
Firewire B Connector
P.57

J8300
OPTICAL DRIVE Connector
P.51

133MHz/3.3V/16 Bit

J7800
Cardbus Connector
P.48

33MHZ
16/32 BITS
3.3V/5V

PCI BUS
32BITS
33MHZ
3.3V

J7600
Airport Extreme Connector
PAGE 46

U7800
Cardbus
PCI1510
PAGE 48

U7700
USB 2.0
uPD720101
PAGE 47

U7500
BOOTROM
PAGE 45

J1699
SMU/JR Debug Connector
P.16

J790
Backup Battery
Right USB Connector
P.7

J9500
Sound (Kazoo) Connector
P.60

Sleep LED
P.18

J9400
Modem Connector
P.59

USB 1.1 (Low/Full Speed)

USB 2.0 (Low/Full/High Speed)

PORT = USB 2.0 (Low/Full/High Speed)

Bluetooth = USB 1.1 (Low/Full Speed)

USB 1.1

J2130
USB Trackpad Connector
P.18

KB LED
P.18

SYSTEM BLOCK DIAGRAM

NOTICE OF PROPRIETARY PROPERTY

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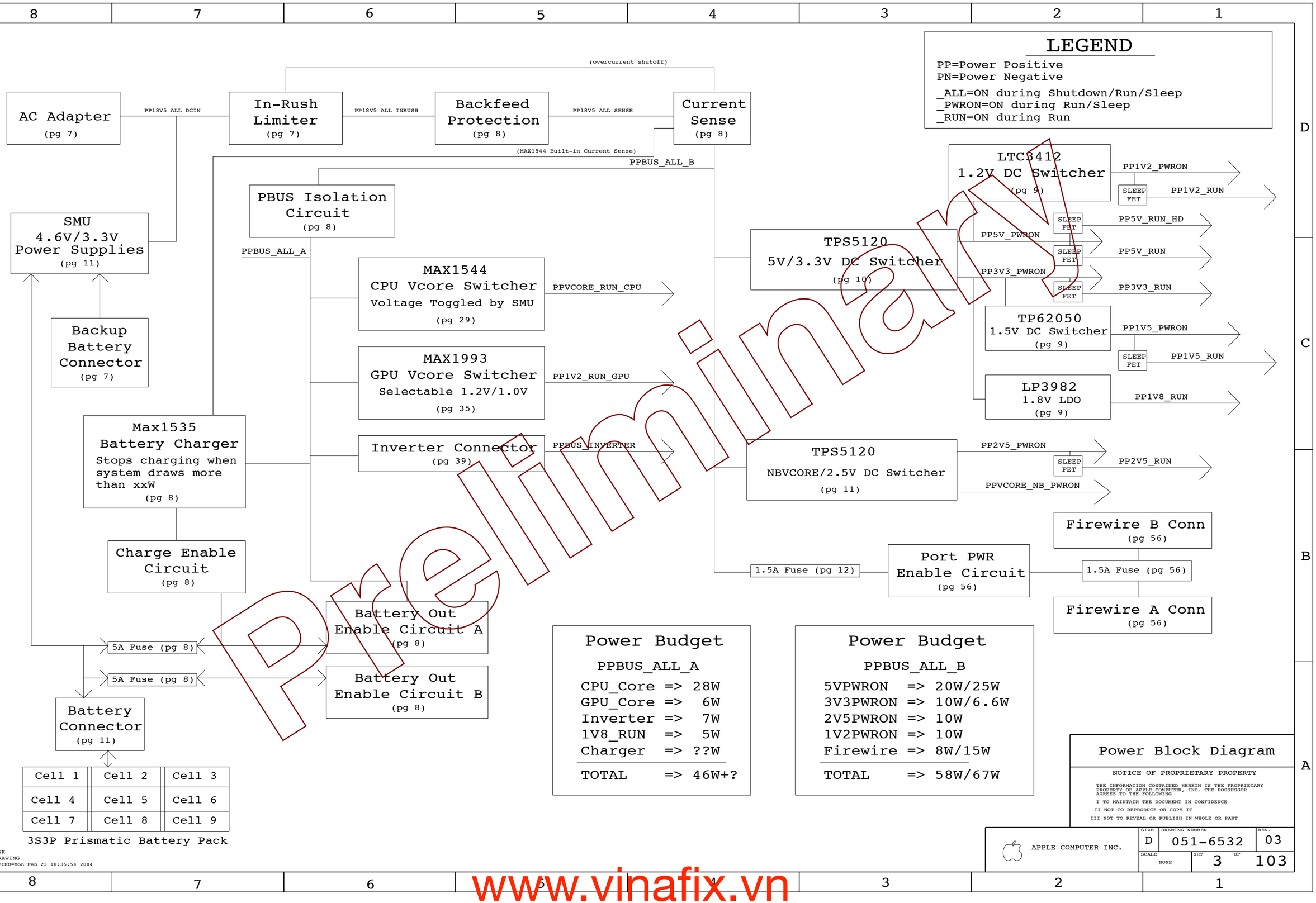
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03

SCALE NONE

SHT 2 OF 103



Revision Notes

1/14/04
1) moved Q3001-Q3004,D3001,D3002,R3044,R3046,R3048,R3070,R3050,R3052,R3054 from Page 27 to page 16 to allow sync with Gila
2) moved AGP_Vref (R4802,R4803,C4818) circuit to M11 specific page (49)
3) changed R2191 to pulldown on SYS_LED
*** sync with Gila ***
1/20/04
4) added 10 mil MIN_LINE_WIDTH and MIN_NECK_WIDTH to BKFD_PROT_EN_L
5) changed MIN_LINE_WIDTH of PP5V_CHGR_LDO to 10 mils
6) moved J790 (backup battery/R USB connector) to page 18 for syncing with Logic
7) moved J1600 (BT/USB connector) to page 18 for syncing with Logic
8) moved C860-C865 (Mbus hold-up caps) to page 18 for syncing with Logic
9) moved ZT9900-ZT9903 (EMI vias) to page 18 for syncing with Logic
10) moved SP500-SP505 and SP9900 to (Speaker wire clips) to page 18 for syncing with Logic
11) moved ZT500-ZT505, ZTm10, and ZT511 (plated screw holes) to page 18 for syncing with Logic
12) moved BS510 to page 18 for syncing with Logic
13) moved J2130 (trackpad connector) to page 18 for syncing with Logic
14) changed C2150 to 20%
15) added 10 mil MIN_LINE_WIDTH and MIN_NECK_WIDTH to KBDLED_ANODE and KDBLED_RETURN
16) changed C2115 to R2116 (3.32K 1% 40Z) to divide ALS output to 2.5V
*** sync with Logic ***
2/2/04
17) changed PCI_ from shasta to PCI_SB to allow desktops to insert series R's
18) added pp 75 to alias PCI_SB_nets back to PCI to reconnect
19) changed R2150 to 8.25 to reduce LED drive current to 20mA
20) changed Q2113 to second FET in Q5909
21) changed SMU_ADAPTER_ID to SMU_ONEWIRE
22) added R1620 and R1621 to divide ALS output down to 2.5V
23) added alias from TP_SATA_CLKZ5M to SATA_CLK25M
2/3/04
24) changed PPVCORE_RUN_CPU connection to XW592 to _PP1V5_RUN_FET
2/6/04
25) changed C720 to 0.22uF
26) changed R800 and R810 to 1/2W 1206 10mohm
27) changed C1068 to NO STUFF
28) removed Q1117 and C1114
29) changed L1115 to 2.2uH IHLP5050CE (152S0152)
30) changed C1121 to 680pF 402
31) changed R1102 to 20K 1% 402
32) added MIN_LINE_WIDTH and MIN_NECK_WIDTH properties to CPUVCORE_CM_N and CPUVCORE_CS_N
33) added MIN_LINE_WIDTH and MIN_NECK_WIDTH properties to ALS1_PHOTODIODE and ALS1_OP_IN
2/7/04
34) changed R5019 to 26.7K 1% to increase GPU Vcore current limit (rdar://3510721)
35) sync with Gila (Q45) to fix several power disconnects
36) added aliases on page 5 to set unused CKE, CS, and MUX controls back to TP
37) sync with Logic (Q43) to get DVO contraints
2/10/04
38) changed R3671 to 100K 0.1% to adjust the Tdiode range
39) changed C3671 to 10uF 20% 6.3V to adjust the Tdiode range
40) changed R3672 to 40.2K 0.1% to adjust the Tdiode range
41) changed R3676 to 100K 0.1% to adjust the Tdiode range
42) changed C3676 to 10uF 20% 6.3V to adjust the Tdiode range
43) changed R3677 to 40.2K 0.1% to adjust the Tdiode range
44) mirrored FL9020 and FL9021 to fix layout
2/11/04
45) changed L970 to 152S0154 (10uH) to reduce size
2/12/04
46) removed 197S0703 as alternate for 197S0037 (25MHz Vesta crystal)
47) changed all references to SMU_MANUAL_RESET_L to SMU_RESET_L

2/19/04
48) removed DC current limit circuit (U870 and associated discretes)
49) added BOMOPTION for 2.8V CPU Avdd LDO
50) changed R4800 to 2.2 ohm 603, C4811 to 1uF 402, and C4816 to 0.1uF 402 in U3Lite AGP Avdd filter.
51) changed R1610 (series R on SMU_ONEWIRE output) to 0 ohm
52) added R1611 (1K pullup to PP3V3_ALL) on ADAPTER_ID to power SMU_ONEWIRE interface
2/23/04
53) changed C8160-C8160 (SATA AC coupling caps) to 0.01uF per Marvell recommendation
54) added NO_TEST properties to CPUVCORE_GNDSENSE and CPUVCORE_SENSE

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03

SCALE	SHT	OF
NONE	4	103

Page Notes

Power aliases required by this page:
N/A (Most aliases are on this page)

Signal aliases required by this page:
N/A (Most aliases are on this page)

BOM options provided by this page:
(NONE)

AGP Signal Aliasing

GPU is D3cold

48 47 46 45 5 PCI_RESET_L — MAKE_BASE=TRUE — ALIAS — GPU_RESET_L — 37 41

PCI Signal Aliasing

CardBus is D3cold

48 47 46 45 5 PCI_RESET_L — MAKE_BASE=TRUE — ALIAS — PCI_CBUS_RESET_L — 49

6 PCI_CLK33M_AIRPORT — MAKE_BASE=TRUE — ALIAS — PCI_CLK_P3 — 25
PCI_CLK33M_AIRPORT — 47

PCI_CLK33M_CBUS — MAKE_BASE=TRUE — ALIAS — PCI_CLK_GP1 — 25
PCI_CLK33M_CBUS — 49

PCI_CLK33M_USB2 — MAKE_BASE=TRUE — ALIAS — PCI_CLK_GP0 — 25
PCI_CLK33M_USB2 — 48

SATA_CLK25M — MAKE_BASE=TRUE — ALIAS — PCI_CLK_P4 — 25
SATA_CLK25M — 51

45 25 PCI_CLK33M_SB_EXT — MAKE_BASE=TRUE — ALIAS — PCI_CLK_P1 — 25

USB Signal Aliasing

USB "0": Left USB Port

59 6 USB2_N<0> — ALIAS — USB2_LT_N — MAKE_BASE=TRUE — 17
59 6 USB2_P<0> — ALIAS — USB2_LT_P — MAKE_BASE=TRUE — 17
59 6 USB2_PWREN<0> — ALIAS — LTUSB_PWREN — MAKE_BASE=TRUE — 17
59 6 USB2_OC<0> — ALIAS — LTUSB_OVERCURRENT — MAKE_BASE=TRUE — 17

USB "1": Right USB Port

59 6 USB2_N<1> — ALIAS — USB2_RT_N — MAKE_BASE=TRUE — 17
59 6 USB2_P<1> — ALIAS — USB2_RT_P — MAKE_BASE=TRUE — 17
59 6 USB2_PWREN<1> — ALIAS — RTUSB_PWREN — MAKE_BASE=TRUE — 17
59 6 USB2_OC<1> — ALIAS — RTUSB_OVERCURRENT — MAKE_BASE=TRUE — 17

USB "2": BlueTooth

59 6 USB2_N<2> — ALIAS — USB_BT_N — MAKE_BASE=TRUE — 17
59 6 USB2_P<2> — ALIAS — USB_BT_P — MAKE_BASE=TRUE — 17
59 USB2_PWREN<2> — ALIAS — TP_USB2_PWREN2 — MAKE_BASE=TRUE
59 USB2_OC<2> — ALIAS — USB2_OC2_PU — MAKE_BASE=TRUE

USB "3": MicroDash Modem

59 6 USB2_N<3> — ALIAS — USB_MODEM_N — MAKE_BASE=TRUE — 60
59 6 USB2_P<3> — ALIAS — USB_MODEM_P — MAKE_BASE=TRUE — 60
59 USB2_PWREN<3> — ALIAS — TP_USB2_PWREN3 — MAKE_BASE=TRUE
59 USB2_OC<3> — ALIAS — USB2_OC3_PU — MAKE_BASE=TRUE

USB "4": Trackpad/Keyboard

59 6 USB2_N<4> — ALIAS — USB_TPAD_N — MAKE_BASE=TRUE — 17
59 6 USB2_P<4> — ALIAS — USB_TPAD_P — MAKE_BASE=TRUE — 17
59 USB2_PWREN<4> — ALIAS — TP_USB2_PWREN4 — MAKE_BASE=TRUE
59 USB2_OC<4> — ALIAS — USB2_OC4_PU — MAKE_BASE=TRUE

SMU Signal Aliasing

13 SMU_SLEEP — ALIAS — SYS_SLEEP — MAKE_BASE=TRUE — 10 11 25
22 13 SMU_WARM_RESET_L — SYS_WARM_RESET_L — MAKE_BASE=TRUE — 22 23 25 48

Test Point Aliasing

EXT_LED_L — ALIAS — TP_EXT_LED_L — MAKE_BASE=TRUE
13 FAN_RPM2 — ALIAS — TP_FAN_RPM2 — MAKE_BASE=TRUE
13 FAN_TACH2 — ALIAS — TP_FAN_TACH2 — MAKE_BASE=TRUE
13 FAN_TACH3 — ALIAS — TP_FAN_TACH3 — MAKE_BASE=TRUE
13 FAN_TACH4 — ALIAS — TP_FAN_TACH4 — MAKE_BASE=TRUE
13 FAN_TACH5 — ALIAS — TP_FAN_TACH5 — MAKE_BASE=TRUE
13 I2C_SMU_D_SCL — ALIAS — TP_I2C_SMU_D_SCL — MAKE_BASE=TRUE
22 NB_PMR_OBSV — ALIAS — TP_NB_PMR_OBSV — MAKE_BASE=TRUE
22 NB_THMI — ALIAS — TP_NB_THMI — MAKE_BASE=TRUE
22 NB_THMO — ALIAS — TP_NB_THMO — MAKE_BASE=TRUE
50 SATA_RXD_P2_C — ALIAS — TP_SATA_RXD_P2 — MAKE_BASE=TRUE
50 SATA_RXD_N2_C — ALIAS — TP_SATA_RXD_N2 — MAKE_BASE=TRUE
50 SATA_TXD_P2 — ALIAS — TP_SATA_TXD_P2 — MAKE_BASE=TRUE
50 SATA_TXD_N2 — ALIAS — TP_SATA_TXD_N2 — MAKE_BASE=TRUE

PBUS PWR

6 PPBUS_ALL_A — VOLTAGE=18.5V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil
ALIAS — PPBUS_ALL_A — 8 17 42
ALIAS — PPVIN_CPUVCORE — 31
ALIAS — PPVIN_GPUVCORE — 38
ALIAS — PPBUS_INV — 42
ALIAS — PPBUSA_BBATT — 17

6 PPBUS_ALL_B — VOLTAGE=18.5V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil
ALIAS — PPBUS_ALL_B — 8 17
ALIAS — PPVIN_5V3VPWRON — 10
ALIAS — PPVIN_2V5_NBVCORE_PWRON — 11
ALIAS — PPBUS_FW — 12
ALIAS — PPBUSB_BBATT — 17

CPU/GPU Core PWR

32 31 PPVCORE_CPU_REG — ALIAS — PPVCORE_RUN_CPU 6 — MAKE_BASE=TRUE, VOLTAGE=1.1V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil — ALIAS — PPVCORE_CPU — 27 29 30 31 32

38 PPVCORE_GPU_REG — ALIAS — XW510 2 — JUMPER OPEN — PP1V2_RUN_GPU 6 — MAKE_BASE=TRUE, VOLTAGE=1.2V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil — ALIAS — PPVCORE_GPU — 37 39
PPVCORE_GPU_REG — MAKE_BASE=TRUE, VOLTAGE=1.2V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil

Graphic PWR

5 PP2V5_RUN — R505 1 — 0, 5%, 1/10W, FF, 805 2 — PP2V5_GPU — 40
ALIAS — PP2V5_GPU — MAKE_BASE=TRUE, VOLTAGE=2.5V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil

6 PP3V3_RUN — R502 1 — 0, 5%, 1/10W, FF, 805 2 — PP3V3_GPU — 37 39 40
ALIAS — PP3V3_GPU — MAKE_BASE=TRUE, VOLTAGE=3.3V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil
ALIAS — PP3V3_AGP — 35, VOLTAGE=3.3V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil

5 PP2V5_RUN
6 5 PP1V8_RUN
ATI_MEMIO_1V8 — R503 1 — 0, 5%, 1/4W, FF, 1210 2
ATI_MEMIO_2V5 — R501 1 — 0, 5%, 1/4W, FF, 1210 2
PPVCORE_GPUFB — MAKE_BASE=TRUE, VOLTAGE=1.8V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil

PP3V3_PWRON
R599 — 100K, 5%, 1/16W, MF, 402 2
SYS_WARM_RESET_L — MAKE_BASE=TRUE

6 5 PP1V8_RUN — R504 1 — 0, 5%, 1/10W, FF, 805 2 — PP1V8_GPU — 37 39 40 41
ALIAS — PP1V8_GPU — MAKE_BASE=TRUE, VOLTAGE=1.8V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil

PP1V5_RUN — R500 1 — 0, 5%, 1/10W, FF, 805 2 — PP1V5_GPU_AGP — 37 39 40
ALIAS — PP1V5_GPU — MAKE_BASE=TRUE, VOLTAGE=1.5V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil

More Test Point Aliasing

25 EI_CPU1_CLK_N_R — ALIAS — TP_EI_CPU1_CLK_N — MAKE_BASE=TRUE
25 EI_CPU1_CLK_P_R — ALIAS — TP_EI_CPU1_CLK_P — MAKE_BASE=TRUE
25 CPU1_HTBEN_R — ALIAS — TP_CPU1_HTBEN_R — MAKE_BASE=TRUE
25 EI_CPU1_SYNC_R — ALIAS — TP_EI_CPU1_SYNC_R — MAKE_BASE=TRUE
33 RAM_CKE_R<2> — ALIAS — TP_RAM_CKE_R<2>
33 RAM_CKE_R<3> — ALIAS — TP_RAM_CKE_R<3>
33 RAM_CKE_R<6> — ALIAS — TP_RAM_CKE_R<6>
33 RAM_CKE_R<7> — ALIAS — TP_RAM_CKE_R<7>
33 RAM_CS_L_R<2> — ALIAS — TP_RAM_CS_L_R<2>
33 RAM_CS_L_R<3> — ALIAS — TP_RAM_CS_L_R<3>
33 RAM_CS_L_R<10> — ALIAS — TP_RAM_CS_L_R<10>
33 RAM_CS_L_R<11> — ALIAS — TP_RAM_CS_L_R<11>

33 RAM_MUXEN0 — ALIAS — TP_RAM_MUXEN0
33 RAM_MUXEN4 — ALIAS — TP_RAM_MUXEN4

_PWRON PWR

10 _PP5V_PWRON_REG — ALIAS — XW520 2 — JUMPER OPEN — PP5V_PWRON — VOLTAGE=5V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil
PP5V_PWRON_REG — MAKE_BASE=TRUE, VOLTAGE=5V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil
ALIAS — PP5V_PWRON_AUDIO — 61
ALIAS — PP5V_PWRON_MODEM — 60
ALIAS — PP5V_PWRON_LTUSB — 17
ALIAS — PP5V_PWRON_RTUSB — 17
ALIAS — PP5V_PWRON_SLEEPLED — 19
ALIAS — PP5V_PWRON_TPAD — 17
ALIAS — PP5V_PWRON_3V3ALL — 11
ALIAS — PP5V_PWRON_FAN — 15
ALIAS — PP5V_PWRON_GPUVCORE — 38
ALIAS — PP5V_PWRON_SERIAL — 16
ALIAS — PPVIN_1V2PWRON — 9
ALIAS — PP5V_PWRON_5VRUN — 10
ALIAS — PP5V_CBUS — 49
ALIAS — PP5V_CPUVCORE_VDD — 31
ALIAS — PP5V_CPUTHERM — 32

10 _PP3V3_PWRON_REG — ALIAS — XW530 2 — JUMPER OPEN — PP3V3_PWRON — VOLTAGE=3.3V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil
PP3V3_PWRON_REG — MAKE_BASE=TRUE, VOLTAGE=3.3V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil
ALIAS — PP3V3_PWRON_AUDIO — 61
ALIAS — PP3V3_PWRON_MODEM — 60
ALIAS — PP3V3_PWRON_SB — 10 21 23 [illegible]
ALIAS — PPPCI64_PWRON_SB — 21
ALIAS — PPPCI32_PWRON_SB — 21
ALIAS — PP3V3_PWRON_USB — 59
ALIAS — PP3V3_PWRON_BT — 17
ALIAS — PP3V3_PWRON_ALS1 — 15
ALIAS — PPVIN_1V5PWRON — 9
ALIAS — PP3V3_PWRON_THERM — 15
ALIAS — PP3V3_PWRON_3V3RUN — 10
ALIAS — PP3V3_CBUS — 49
ALIAS — PP3V3_CPUTHERM — 32
ALIAS — PP3V3_PWRON_1V8RUN — 9

11 _PP2V5_PWRON_REG — ALIAS — XW540 2 — JUMPER OPEN — PP2V5_PWRON — VOLTAGE=2.5V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil
PP2V5_PWRON_REG — MAKE_BASE=TRUE, VOLTAGE=2.5V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil
ALIAS — PP2V5_PWRON_SB — 21 23 45 56
ALIAS — PP2V5_PWRON_HT — 44
ALIAS — PP2V5_PWRON_DIMM — 35
ALIAS — PP2V5_ENET — 55
ALIAS — PP2V5_HT — 43
ALIAS — PP5V_D_DIMM — 35
ALIAS — PP2V5_PWRON_2V5RUN — 11
ALIAS — PP2V5_PWRON_1V8RUN — 9
ALIAS — PP2V5_PWRON_RAM — 24 33

9 _PP1V5_PWRON_REG — ALIAS — XW560 2 — JUMPER OPEN — PP1V5_PWRON — VOLTAGE=1.5V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil
PP1V5_PWRON_REG — MAKE_BASE=TRUE, VOLTAGE=1.5V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil
ALIAS — PPVCORE_PWRON_PULSAR — 24
ALIAS — PP1V5_PWRON_1V5RUN — 9
ALIAS — PP1V5_PWRON_NB_AVDD — 26 33 36 43

9 _PP1V2_PWRON_REG — ALIAS — XW561 — JUMPER OPEN — PP1V2_PWRON — VOLTAGE=1.2V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil
PP1V2_PWRON_REG — MAKE_BASE=TRUE, VOLTAGE=1.2V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil
ALIAS — PP1V2_PWRON_DISK_SB — 50
ALIAS — PP1V2_PWRON_HT — 44
ALIAS — PP1V2_PWRON_SB — 23
ALIAS — PPVCORE_PWRON_SB — 21
ALIAS — PP1V2_PWRON_1V2RUN — 9

ONLY ONE CAN BE CLOSED Between XW560/XW561!!!

11 _PPVCORE_NB_REG — ALIAS — XW552 2 — JUMPER OPEN — PPVCORE_PWRON_NB — VOLTAGE=1.3V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil
PPVCORE_NB_REG — MAKE_BASE=TRUE, VOLTAGE=1.3V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil
ALIAS — PPVCORE_PWRON_NB — 20

ONLY ONE CAN BE CLOSED Between XW550/XW551!!!

XW552 Always close

GND — VOLTAGE=0V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil

_RUN PWR

PP3V3_ALL — VOLTAGE=3.3V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil
11 _PP3V3_ALL_LDO — ALIAS
ALIAS — PP3V3_ALL_ACIN — 7
ALIAS — PP3V3_ALL_DCILIM — 13
ALIAS — PP3V3_ALL_HALLEFFECT — 17
ALIAS — PP3V3_ALL_RTC — 13
ALIAS — PP3V3_ALL_SMU — 13 16 18

2.5V SMU VRef
32 PP2V5_SMU_VREF — MAKE_BASE=TRUE
ALIAS — PPVREF_SMU — 13

PP5V_RUN — VOLTAGE=5V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil
10 _PP5V_RUN_FET — ALIAS
ALIAS — PP5V_RUN_KBDLED — 19
ALIAS — PP5V_UATA — 52
ALIAS — PPBU_RUN_FW — 12
ALIAS — PP5V_RUN_CPU — 16 29

PP5V_RUN_HD — VOLTAGE=5V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil
10 _PP5V_RUN_HD_FET — ALIAS
ALIAS — PP5V_PATA — 52
ALIAS — PP5V_RUN_AUDIO — 61

PP3V3_RUN — VOLTAGE=3.3V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil
10 _PP3V3_RUN_FET — ALIAS
ALIAS — PP3V3_SATABR — 51
ALIAS — PP3V3_PATA — 52
ALIAS — PPVIO_PCI_USB2 — 48
ALIAS — PPVIO_PCI_CBUS — 49
ALIAS — PP3V3_PCI — 23 45 46 47 48 49
ALIAS — PP3V3_SB_PCI — 45
ALIAS — PP3V3_CPUVCORE — 31
ALIAS — PP3V3_RUN_FAN — 15
ALIAS — PP3V3_RUN_SI — 41

PP2V5_RUN — VOLTAGE=2.5V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil
11 _PP2V5_RUN_FET — ALIAS
ALIAS — PP2V5_PCI — 49
ALIAS — PP2V5_RUN_CPU — 29

PP1V8_RUN — VOLTAGE=1.8V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil
9 _PP1V8_RUN_LDO — ALIAS — XW518 2 — JUMPER OPEN — _PP1V8_SATABR — 51
PP1V8_RUN_LDO — MAKE_BASE=TRUE, VOLTAGE=1.8V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil

PP1V5_RUN — VOLTAGE=1.5V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil
9 5 _PP1V5_RUN_FET — ALIAS
ALIAS — PP1V5_AGP — 36 37
ALIAS — PPVCORE_PULSAR — 24

PP1V2_RUN — VOLTAGE=1.2V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil
9 _PP1V2_RUN_FET — ALIAS
ALIAS — PP1V2_HT — 22 43
ALIAS — PP1V2_PULSAR — 24

ONLY ONE CAN BE CLOSED Between XW590/XW591!!!

XW590 2 — JUMPER OPEN — PP1V2_EI_NB — 18 26 — VOLTAGE=1.2V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil
XW591 2 — JUMPER OPEN

9 5 _PP1V5_RUN_FET — XW592 2 — JUMPER OPEN — PP1V2_EI_CPU — 18 27 28 29 — VOLTAGE=1.2V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil

Chassis Grounds

17 GND_CHASSIS_DVI — VOLTAGE=0V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil — ALIAS — GND_CHASSIS_DVI_TOP — 42
17 GND_CHASSIS_INVERTER — VOLTAGE=0V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil — ALIAS — GND_CHASSIS_INV — 42
6 GND_CHASSIS_LVDS — VOLTAGE=0V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil — ALIAS — GND_CHASSIS_LVDS — 42

ALIAS — GND_CHASSIS_ENET — 55
ALIAS — GND_CHASSIS_FW_PORT1 — 58
ALIAS — GND_CHASSIS_FW_PORT2 — 58
ALIAS — GND_CHASSIS_DVI_BOTTOM — 42
6 GND_CHASSIS_IO — ALIAS — GND_CHASSIS_SVIDEO — 42
17 VOLTAGE=0V, MIN_LINE_WIDTH=25 mil, MIN_NECK_WIDTH=10 mil

Power Connections

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 5 OF	103

FUNCTIONAL TEST POINTS

Wireless
Within 1" of connector

FUNC_TEST=TRUE
PCI_AD<0> 45 46 47 48 49 62
FUNC_TEST=TRUE
PCI_AD<1> 45 46 47 48 49 62
FUNC_TEST=TRUE
PCI_AD<2> 45 46 47 48 49 62
FUNC_TEST=TRUE
PCI_AD<3> 45 46 47 48 49 62
FUNC_TEST=TRUE
PCI_AD<4> 45 46 47 48 49 62
FUNC_TEST=TRUE
PCI_AD<5> 45 46 47 48 49 62
FUNC_TEST=TRUE
PCI_AD<6> 45 46 47 48 49 62
FUNC_TEST=TRUE
PCI_AD<7> 45 46 47 48 49 62
FUNC_TEST=TRUE
PCI_AD<8> 45 46 47 48 49 62
FUNC_TEST=TRUE
PCI_AD<9> 45 46 47 48 49 62
FUNC_TEST=TRUE
PCI_AD<10> 45 46 47 48 49 62
FUNC_TEST=TRUE
PCI_AD<11> 45 46 47 48 49 62
FUNC_TEST=TRUE
PCI_AD<12> 45 46 47 48 49 62
FUNC_TEST=TRUE
PCI_AD<13> 45 46 47 48 49 62
FUNC_TEST=TRUE
PCI_AD<14> 45 46 47 48 49 62
FUNC_TEST=TRUE
PCI_AD<15> 45 46 47 48 49 62
FUNC_TEST=TRUE
PCI_AD<16> 45 46 47 48 49 62
FUNC_TEST=TRUE
PCI_AD<17> 45 46 47 48 49 62
FUNC_TEST=TRUE
PCI_AD<18> 45 46 47 48 49 62
FUNC_TEST=TRUE
PCI_AD<19> 45 46 47 48 49 62
FUNC_TEST=TRUE
PCI_AD<20> 45 46 47 48 49 62
FUNC_TEST=TRUE
PCI_AD<21> 45 47 48 49 62
FUNC_TEST=TRUE
PCI_AD<22> 45 47 48 49 62
FUNC_TEST=TRUE
PCI_AD<23> 45 47 48 49 62
FUNC_TEST=TRUE
PCI_AD<24> 45 46 47 48 49 62
FUNC_TEST=TRUE
PCI_AD<25> 45 46 47 48 49 62
FUNC_TEST=TRUE
PCI_AD<26> 45 46 47 48 49 62
FUNC_TEST=TRUE
PCI_AD<27> 45 46 47 48 49 62
FUNC_TEST=TRUE
PCI_AD<28> 45 46 47 48 49 62
FUNC_TEST=TRUE
PCI_AD<29> 45 46 47 48 49 62
FUNC_TEST=TRUE
PCI_AD<30> 45 46 47 48 49 62
FUNC_TEST=TRUE
PCI_AD<31> 45 46 47 48 49 62
FUNC_TEST=YES
PCI_FRAME_L 45 47 48 49 62
FUNC_TEST=YES
PCI_TRDY_L 45 47 48 49 62
FUNC_TEST=YES
PCI_IRDY_L 45 47 48 49 62
FUNC_TEST=YES
PCI_DEVSEL_L 45 47 48 49 62
FUNC_TEST=YES
PCI_STOP_L 45 47 48 49 62
FUNC_TEST=YES
PCI_PAR 45 47 48 49 62
FUNC_TEST=TRUE
PCI_CBE_L<0> 45 47 48 49 62
FUNC_TEST=TRUE
PCI_CBE_L<1> 45 47 48 49 62
FUNC_TEST=TRUE
PCI_CBE_L<2> 45 47 48 49 62
FUNC_TEST=TRUE
PCI_CBE_L<3> 45 47 48 49 62
FUNC_TEST=YES
PCI_SLOTA_REQ_L 45 47
FUNC_TEST=YES
PCI_SLOTA_GNT_L 45 47
FUNC_TEST=YES
PCI_SLOTA_INT_L 23 47
FUNC_TEST=YES
PCI_SLOTA_IDSEL 47
FUNC_TEST=YES
PCI_CLK33M_AIRPORT 5
FUNC_TEST=YES
TP_AIRPORT_PME_L 47
FUNC_TEST=YES
TP_AIRPORT_RF_DISABLE 47
FUNC_TEST=YES
AIRPORT_CLKRUN_L_PD 47
FUNC_TEST=YES
PP3V3_RUN 5 6 X 4

GND x 4

DVI/VGA
Within 1" of connector

FUNC_TEST=TRUE
TMDS_DN<0> 41 42 62
FUNC_TEST=TRUE
TMDS_DP<0> 41 42 62
FUNC_TEST=TRUE
TMDS_DN<1> 41 42 62
FUNC_TEST=TRUE
TMDS_DP<1> 41 42 62
FUNC_TEST=TRUE
TMDS_DN<2> 41 42 62
FUNC_TEST=TRUE
TMDS_DP<2> 41 42 62
FUNC_TEST=YES
TMDS_CONN_CLKN 42 62
FUNC_TEST=YES
TMDS_CONN_CLKP 42 62
FUNC_TEST=YES
VGA_R 42
FUNC_TEST=YES
VGA_G 42
FUNC_TEST=YES
VGA_B 42
FUNC_TEST=YES
VGA_VSYNC 42
FUNC_TEST=YES
VGA_HSYNC 42
FUNC_TEST=YES
DVI_DDC_CLK_UF 42
FUNC_TEST=YES
DVI_DDC_DATA_UF 42
FUNC_TEST=YES
DVI_HPD_UF 42
FUNC_TEST=YES
PP5V_RUN_DDC 42
FUNC_TEST=YES
GND_CHASSIS_IO 5 17

GND x 1

LVDS
Within 1" of connector

FUNC_TEST=YES
LVDS_L0N 39 42
FUNC_TEST=YES
LVDS_L0P 39 42
FUNC_TEST=YES
LVDS_L1N 39 42
FUNC_TEST=YES
LVDS_L1P 39 42
FUNC_TEST=YES
LVDS_L2N 39 42
FUNC_TEST=YES
LVDS_L2P 39 42
FUNC_TEST=YES
CLKLVDS_LN 39 42
FUNC_TEST=YES
CLKLVDS_LP 39 42
FUNC_TEST=YES
LVDS_U0N 39 42
FUNC_TEST=YES
LVDS_U0P 39 42
FUNC_TEST=YES
LVDS_U1N 39 42
FUNC_TEST=YES
LVDS_U1P 39 42
FUNC_TEST=YES
LVDS_U2N 39 42
FUNC_TEST=YES
LVDS_U2P 39 42
FUNC_TEST=YES
CLKLVDS_UN 39 42
FUNC_TEST=YES
CLKLVDS_UP 39 42
FUNC_TEST=YES
LVDS_DDC_CLK 39 42
FUNC_TEST=YES
LVDS_DDC_DATA 39 42
FUNC_TEST=YES
PP3V3_LCD 42
FUNC_TEST=YES
GND_CHASSIS_LVDS 5

2 x GND

INVERTER
Within 1" of connector

FUNC_TEST=YES
PPBUS_ALL_A 5 6
FUNC_TEST=YES
PP5V_INVERTER 42
FUNC_TEST=YES
BRIGHT_PWM 42

1 x GND

S-Video
Within 1 of connector

FUNC_TEST=YES
TV_GND1 42
FUNC_TEST=YES
TV_GND2 42
FUNC_TEST=YES
TV_C 42
FUNC_TEST=YES
TV_Y 42
FUNC_TEST=YES
TV_COMP 42

PATA (SATA Bridge)
Within 1" of connector

FUNC_TEST=TRUE
PATA_DD<0> 51 52
FUNC_TEST=TRUE
PATA_DD<1> 51 52
FUNC_TEST=TRUE
PATA_DD<2> 51 52
FUNC_TEST=TRUE
PATA_DD<3> 51 52
FUNC_TEST=TRUE
PATA_DD<4> 51 52
FUNC_TEST=TRUE
PATA_DD<5> 51 52
FUNC_TEST=TRUE
PATA_DD<6> 51 52
FUNC_TEST=TRUE
PATA_DD<7> 51 52
FUNC_TEST=TRUE
PATA_DD<8> 51 52
FUNC_TEST=TRUE
PATA_DD<9> 51 52
FUNC_TEST=TRUE
PATA_DD<10> 51 52
FUNC_TEST=TRUE
PATA_DD<11> 51 52
FUNC_TEST=TRUE
PATA_DD<12> 51 52
FUNC_TEST=TRUE
PATA_DD<13> 51 52
FUNC_TEST=TRUE
PATA_DD<14> 51 52
FUNC_TEST=TRUE
PATA_DD<15> 51 52
FUNC_TEST=TRUE
PATA_DMARQ_R 52
FUNC_TEST=TRUE
PATA_DMACK_L 51 52
FUNC_TEST=TRUE
PATA_DA<0> 51 52
FUNC_TEST=TRUE
PATA_DA<1> 51 52
FUNC_TEST=TRUE
PATA_DA<2> 51 52
FUNC_TEST=TRUE
PATA_CS0_L 51 52
FUNC_TEST=TRUE
PATA_CS1_L 51 52
FUNC_TEST=TRUE
PATA_RESET_L 51 52
FUNC_TEST=TRUE
PATA_DSTROBE_R 52
FUNC_TEST=TRUE
PATA_HSTROBE 51 52
FUNC_TEST=TRUE
PATA_STOP 51 52
FUNC_TEST=TRUE
PATA_INTRQ_R 52
FUNC_TEST=TRUE
PP5V_RUN_HD 5 x4
FUNC_TEST=TRUE
PPLOGIC_PATA 52 x3

GND x 5

Battery Conn
Within 1" of connector

FUNC_TEST=YES
PPBATT_ALL_F 7 x2
FUNC_TEST=YES
I2C_SMU_E_SCL 13 18 (I2C_BATT_SCL)
FUNC_TEST=YES
I2C_SMU_E_SDA 13 18 (I2C_BATT_SDA)
FUNC_TEST=YES
BATT_DET_L 7
FUNC_TEST=YES
GND_BATT 7 x2

DC-in Connectors
Within 1" of connector

FUNC_TEST=YES
PP18V5_ALL_DCIN 7 11 x 3

GND x 3

UATA (Optical)
Within 2" of connector

FUNC_TEST=TRUE
UATA_DD<0> 50 52
FUNC_TEST=TRUE
UATA_DD<1> 50 52
FUNC_TEST=TRUE
UATA_DD<2> 50 52
FUNC_TEST=TRUE
UATA_DD<3> 50 52
FUNC_TEST=TRUE
UATA_DD<4> 50 52
FUNC_TEST=TRUE
UATA_DD<5> 50 52
FUNC_TEST=TRUE
UATA_DD<6> 50 52
FUNC_TEST=TRUE
UATA_DD<7> 50 52
FUNC_TEST=TRUE
UATA_DD<8> 50 52
FUNC_TEST=TRUE
UATA_DD<9> 50 52
FUNC_TEST=TRUE
UATA_DD<10> 50 52
FUNC_TEST=TRUE
UATA_DD<11> 50 52
FUNC_TEST=TRUE
UATA_DD<12> 50 52
FUNC_TEST=TRUE
UATA_DD<13> 50 52
FUNC_TEST=TRUE
UATA_DD<14> 50 52
FUNC_TEST=TRUE
UATA_DD<15> 50 52
FUNC_TEST=TRUE
UATA_DMARQ_R 52
FUNC_TEST=TRUE
UATA_DMACK_L 50 52
FUNC_TEST=TRUE
UATA_DA<0> 50 52
FUNC_TEST=TRUE
UATA_DA<1> 50 52
FUNC_TEST=TRUE
UATA_DA<2> 50 52
FUNC_TEST=TRUE
UATA_CS0_L 50 52
FUNC_TEST=TRUE
UATA_CS1_L 50 52
FUNC_TEST=TRUE
UATA_RESET_L 50 52
FUNC_TEST=TRUE
UATA_DSTROBE_R 52
FUNC_TEST=TRUE
UATA_HSTROBE 50 52
FUNC_TEST=TRUE
UATA_STOP 50 52
FUNC_TEST=TRUE
UATA_INTRQ_R 52
FUNC_TEST=TRUE
PP5V_RUN x4

GND x 5

Trackpad
Within 3" of connector

FUNC_TEST=YES
I2C_SMU_B_SCL 13 18 (I2C_DS1775_SCL)
FUNC_TEST=YES
I2C_SMU_B_SDA 13 18 (I2C_DS1775_SDA)
FUNC_TEST=YES
SYS_OVERTEMP_L 13 15 17 23 25
FUNC_TEST=YES
USB2_N<4> 5 59
FUNC_TEST=YES
USB2_P<4> 5 59
FUNC_TEST=YES
KBDLED_ANODE 17 19
FUNC_TEST=YES
KBDLED_RETURN 17 19
FUNC_TEST=YES
SYS_DOOR_AJAR (SYS_LID_OPEN)
FUNC_TEST=YES
SYS_POWER_BUTTON_L 6 13 16 17 42
FUNC_TEST=YES
PP3V3_PWRON 17 25
FUNC_TEST=YES
PP5V_PWRON 6 11
FUNC_TEST=YES
PP3V3_ALL 6
FUNC_TEST=YES
PP3V3_RUN 5 6

Firewire B
Within 1" of connector

FUNC_TEST=YES
FW_PORT1_TPA_P_FL 58
FUNC_TEST=YES
FW_PORT1_TPA_N_FL 58
FUNC_TEST=YES
FW_PORT1_TPB_P_FL 58
FUNC_TEST=YES
FW_PORT1_TPB_N_FL 58
FUNC_TEST=YES
FW_PORT1_AREF 58
FUNC_TEST=YES
GND_FW_PORT1_VG 58
FUNC_TEST=YES
PPFW_PORT1_VP 58

Firewire A
Within 1" of connector

FUNC_TEST=YES
FW_PORT2_TPA_P_FL 58
FUNC_TEST=YES
FW_PORT2_TPA_N_FL 58
FUNC_TEST=YES
FW_PORT2_TPB_P_FL 58
FUNC_TEST=YES
FW_PORT2_TPB_N_FL 58
FUNC_TEST=YES
PPFW_PORT2_VP 58
FUNC_TEST=YES
GND_FW_PORT2_VG 58

Fan Connectors
Within 2" of connector

FUNC_TEST=YES
FAN_RPM0 13 15
FUNC_TEST=YES
FAN_TACH0 13 15
FUNC_TEST=YES
FAN_RPM1 13 15
FUNC_TEST=YES
FAN_TACH1 13 15
FUNC_TEST=YES
PP5V_PWRON 6 11 x 2 one by each fan

GND x 2 - one by each fan

BT/USB Flex
Within 2" of connector

FUNC_TEST=YES
USB2_N<2> 5 59 (USB_BT_N)
FUNC_TEST=YES
USB2_P<2> 5 59 (USB_BT_P)
FUNC_TEST=YES
USB2_N<0> 5 59 (USB2_LT_N)
FUNC_TEST=YES
USB2_P<0> 5 59 (USB2_LT_P)
FUNC_TEST=YES
USB2_PWREN<0> 5 59 (LTUSB_PWREN)
FUNC_TEST=YES
ALS0_OUT 13 17
FUNC_TEST=YES
USB2_OC<0> 5 59 (LTUSB_OVERCURRENT)
FUNC_TEST=YES
ALS_GAIN_BOOST 13 17 19
FUNC_TEST=YES
ADAPTER_ID 17

PP3V3_PWRON x 1
PP5V_PWRON x 1
GND x 1

Backup Battery/USB Flex
Within 2" of connector

FUNC_TEST=YES
PPBUS_ALL_B 5 6
FUNC_TEST=YES
PPBUS_ALL_A 5 6
FUNC_TEST=YES
SYS_POWERUP 14
FUNC_TEST=YES
USB2_N<1> 5 59 (USB2_RT_N)
FUNC_TEST=YES
USB2_P<1> 5 59 (USB2_RT_P)
FUNC_TEST=YES
USB2_PWREN<1> 5 59 (RTUSB_PWREN)
FUNC_TEST=YES
USB2_OC<1> 5 59 (RTUSB_OVERCURRENT)

PP5V_PWRON x 1
GND x 1

Sound Connector
Within 2" of connector

FUNC_TEST=YES
I2S0_DEV_TO_SB_DTI_F 61
FUNC_TEST=YES
I2S0_BITCLK_F 61
FUNC_TEST=YES
I2S0_MCLK_F 61
FUNC_TEST=YES
I2S0_SYNC_F 61
FUNC_TEST=YES
I2S0_SB_TO_DEV_DTO_F 61
FUNC_TEST=YES
I2S2_DEV_TO_SB_DTI_F 61
FUNC_TEST=YES
I2S2_BITCLK_F 61
FUNC_TEST=YES
I2S2_SYNC_F 61
FUNC_TEST=YES
AUDIO_GPIO_11 23 61
FUNC_TEST=YES
AUDIO_EXT_MCLK_SEL 23 61
FUNC_TEST=YES
AUDIO_LO_MUTE_L 23 61
FUNC_TEST=YES
AUDIO_SPKR_MUTE_L 23 61
FUNC_TEST=YES
AUDIO_LO_DET_L 23 61
FUNC_TEST=YES
AUDIO_LO_OPTICAL_PLUG_L 23 61
FUNC_TEST=YES
AUDIO_LI_DET_L 23 61
FUNC_TEST=YES
AUDIO_LI_OPTICAL_PLUG_L 23 61
FUNC_TEST=YES
I2S0_RESET_L_F 61
FUNC_TEST=YES
I2S2_RESET_L_F 61
FUNC_TEST=YES
SLEEPLED_ANODE 19 61 x4
FUNC_TEST=YES
GND_AUDIO 61 x3
FUNC_TEST=YES
PP5V_PWRON_AUDIO 61 x2
FUNC_TEST=YES
PP3V3_PWRON_AUDIO 61

GND x 2

Modem Connector
Within 3" of connector

FUNC_TEST=YES
I2S1_SB_TO_DEV_DTO 16 23 60
FUNC_TEST=YES
I2S1_BITCLK 16 23 60
FUNC_TEST=YES
I2S1_SYNC 16 23 60
FUNC_TEST=YES
I2S1_RESET_L 16 23 60
FUNC_TEST=YES
I2S1_MCLK 16 23 60
FUNC_TEST=YES
I2S1_DEV_TO_SB_DTI 16 23 60
FUNC_TEST=YES
USB2_N<3> 5 59 (USB_MODEM_N)
FUNC_TEST=YES
USB2_P<3> 5 59 (USB_MODEM_P)
FUNC_TEST=YES
MODEM_RINGZSYS_L 23 60
FUNC_TEST=YES
UDASH_SDOWN 23 60
FUNC_TEST=YES
I2C_SB_SCL 18 23 (I2C_MODEM_SCL)
FUNC_TEST=YES
I2C_SB_SDA 18 23 (I2C_MODEM_SDA)

ROM Control
Within 2" of U7500

FUNC_TEST=YES
ROM_ONBOARD_CS_L 46 47
FUNC_TEST=YES
ROM_OE_L 45 46 47
FUNC_TEST=YES
ROM_CS_L 45 46 47
FUNC_TEST=YES
ROM_WE_L 45 46 47

MISC

FUNC_TEST=YES
JTAG_NB_TMS 22
FUNC_TEST=YES
JTAG_NB_TDI 22
FUNC_TEST=YES
JTAG_NB_TDO 22
FUNC_TEST=YES
JTAG_NB_TCK 22
FUNC_TEST=YES
JTAG_NB_TRST_L 22
FUNC_TEST=YES
JTAG_SB_TMS 18 23
FUNC_TEST=YES
JTAG_SB_TDI 18 23
FUNC_TEST=YES
JTAG_SB_TDO 23
FUNC_TEST=YES
JTAG_SB_TCK 18 23
FUNC_TEST=YES
JTAG_SB_TRST_L 18 23
FUNC_TEST=YES
JTAG_VESTA_TMS 12
FUNC_TEST=YES
JTAG_VESTA_TDI 12
FUNC_TEST=YES
JTAG_VESTA_TDO 12
FUNC_TEST=YES
JTAG_VESTA_TCK 12
FUNC_TEST=YES
JTAG_VESTA_TRST_L 12
FUNC_TEST=YES
JTAG_CPU_TMS 18 27 28
FUNC_TEST=YES
JTAG_CPU_TDI 18 27 28
FUNC_TEST=YES
JTAG_CPU_TDO 18 27 28
FUNC_TEST=YES
JTAG_CPU_TCK 18 27 28
FUNC_TEST=YES
JTAG_CPU_TRST_L 27 28
FUNC_TEST=YES
SMU_RESET_L 13 16 19
FUNC_TEST=YES
SYS_POWER_BUTTON_L 6 13 16 17 42
FUNC_TEST=YES
SYS_RESET_BUTTON_L 13 16
FUNC_TEST=YES
PP1V8_RUN 5
FUNC_TEST=YES
PP2V5_PWRON 5
FUNC_TEST=YES
PPBUS_ALL_B 5 6
FUNC_TEST=YES
PP3V3_ALL 6
FUNC_TEST=YES
PPVCORE_RUN_CPU 5
FUNC_TEST=YES
PP1V2_RUN_GPU 5
FUNC_TEST=YES
CPU_VID<4> 13 31 (SMU_BOOT_BUSY)
FUNC_TEST=YES
CPU_VID<5> 13 (SMU_BOOT_SCLK)
FUNC_TEST=YES
SMU_BOOT_CNVSS 13 16
FUNC_TEST=YES
SMU_BOOT_TXD 13 16
FUNC_TEST=YES
SMU_BOOT_RXD 13 16
FUNC_TEST=YES
SYS_POWERUP_L 13 14 (SMU_BOOT_CE)

Functional Testpoints

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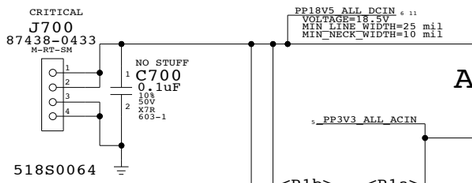
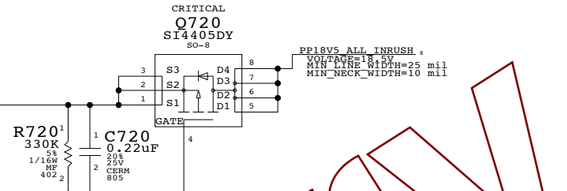
D	051-6532	03
SCALE: NONE	SHT 6 OF 103	

DC Power Input

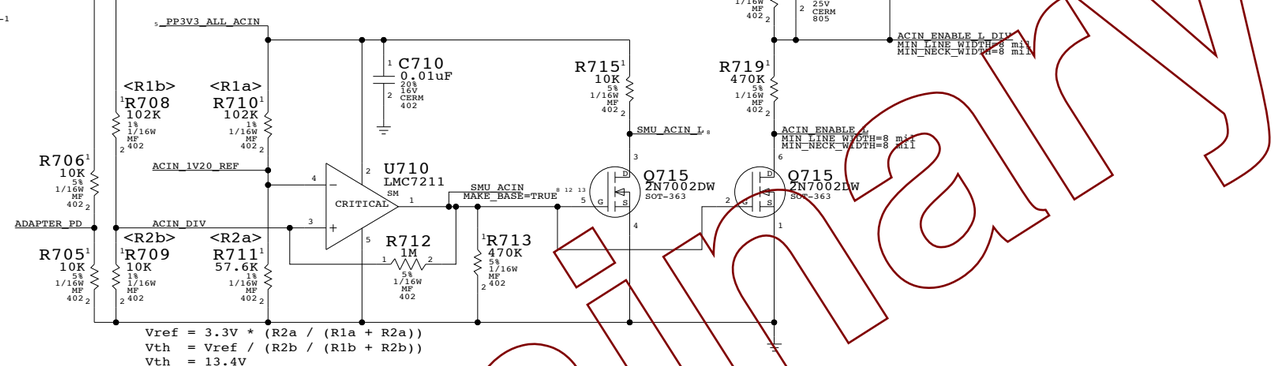
(DC-In jack and associated circuit are on separate baord)



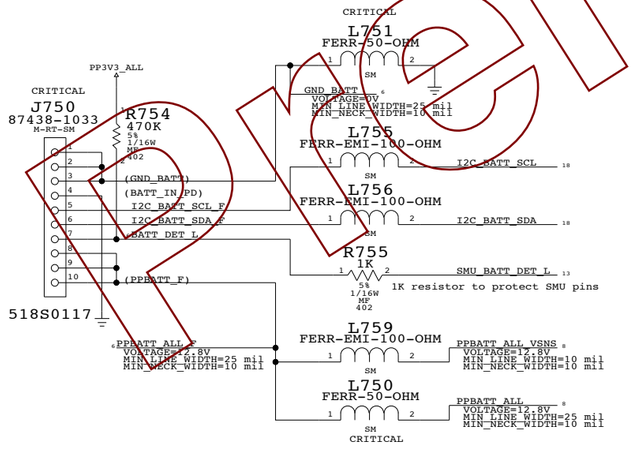
DC Inrush Limiter



ACIN Detection



Main Battery Connector



Place L759 as close to J750 as possible

Power Connectors

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 7 OF 103	

DC-IN Input Current Limiter

Place U800 and U870 near R800

CRITICAL
Q850
SI4405DY
SO-8

PP18V5_ALL_INRUSH
PP18V5_ALL_SENSE
VOLTAGE=18.5V
MIN_LINE_WIDTH=25 mil
MIN_NECK_WIDTH=10 mil

R850 49.9K 1% 1/16W MF 402
R851 68K 5% 1/16W MF 402
C851 0.1uF 20% 25V CERM 603
BKFD_PROT_EN_L_DIV
MIN_LINE_WIDTH=10 mil
MIN_NECK_WIDTH=10 mil
BKFD_PROT_EN_L
MIN_LINE_WIDTH=10 mil
MIN_NECK_WIDTH=10 mil
Q800 2N7002DW SOT-363
SMU_ACIN

CRITICAL
R800 0.010 1% 1/2W MF 1206
PPBUS_ALL_B

CRITICAL
Q880
SI4435DY
SOI

PPBUS_ALL_A
R880 470K 5% 1/16W MF 402
CHGR_PBUS_EN_L_DIV
MIN_LINE_WIDTH=10 mil
MIN_NECK_WIDTH=10 mil
R881 330K 5% 1/16W MF 402
CHGR_PBUS_EN_L
SMU_ACIN
R882 100K 5% 1/16W MF 402
DP800 BAS16TW SOT-363
Q882 2N7002DW SOT-363
CHGR_ACIN_RC
C882 0.01UF 10% 16V CERM 402

Keep short and route as pair

(PP18V5_ALL_SENSE)
(PP18V5_ALL)
R801 4.7 5% 1/16W MF 402
R802 4.7 5% 1/16W MF 402

SMBus Battery Charger

CHGR_REF
R824 100K 1% 1/16W MF 402
R820 100K 1% 1/16W MF 402
C801 0.47UF 20% 50V CERM 1206
C802 0.47UF 20% 50V CERM 1206
C830 0.1UF 20% 10V CERM 402
C825 1uF 20% 10V CERM 603
R830 100K 5% 1/16W MF 402
R826 33 5% 1/16W MF 402
PP5V4_CHGR_LDO
VOLTAGE=5.4V
MIN_LINE_WIDTH=10 mil
MIN_NECK_WIDTH=10 mil
PPBUS_ALL_A
C831 0.1UF 20% 10V CERM 402
C805 4.7uF 20% 25V CERM 1206
C806 4.7uF 20% 25V CERM 1206
C807 4.7uF 20% 25V CERM 1206
C808 4.7uF 20% 25V CERM 1206

NO STUFF
D800 1N914 SOT23
NO STUFF
R805 100K 1% 1/16W MF 402
NO STUFF
R806 13K 1% 1/16W MF 402
C800 1uF 20% 25V CERM 805

CHGR_CSSP
CHGR_CSSN
CHGR_DCIN
CHGR_ACIN
I2C_CHGR_SCL
I2C_CHGR_SDA
CHGR_IMAX
CHGR_VMAX
CHGR_CCS
CHGR_CCI
CHGR_CCV
CHGR_CSIP
CHGR_CSIN

U800 MAX1535A QFN CRITICAL
VDD LDO
SRC
PDS
PDL
REF
DHIV
DHI
DLOV
DLO
ACOK*
DAC
I.C.
BATT
THM
GND
THM PAD
PGND

R823 0 5% 1/16W MF 402
CHGR_DHIV
MIN_LINE_WIDTH=20 mil
MIN_NECK_WIDTH=10 mil
CHGR_DHI
MIN_LINE_WIDTH=25 mil
MIN_NECK_WIDTH=10 mil
CHGR_DLOV_RC
MIN_LINE_WIDTH=20 mil
MIN_NECK_WIDTH=10 mil
CHGR_DLO
MIN_LINE_WIDTH=25 mil
MIN_NECK_WIDTH=10 mil
CHGR_DAC
CHGR_THM

CRITICAL
Q810
SI4835BDY
SOI

R827 0 5% 1/16W MF 402
R828 0 5% 1/16W MF 402
CHGR_CCS_RC
CHGR_CCI_RC
C824 0.01UF 20% 16V CERM 402
C823 0.01UF 20% 16V CERM 402
GND_CHGR
VOLTAGE=0V
MIN_LINE_WIDTH=15 mil
MIN_NECK_WIDTH=10 mil
R825 20.5K 1% 1/16W MF 402
R821 169K 1% 1/16W MF 402
R822 30K 1% 1/16W MF 402
CHGR_CCV_RC
C822 0.01uF 20% 16V CERM 402
R829 100K 1% 1/16W MF 402
C826 1UF 20% 10V CERM 603
C820 0.1UF 20% 10V CERM 402
XW800 SM
C829 1UF 20% 10V CERM 603
NO STUFF
C811 0.001uF 10% 50V CERM 402

CRITICAL
Q811
SI4336DY
SO-8

D810 SM MBRS140T3

CRITICAL
L810 10uH SM1
PPBATT_CHGR_SW
MIN_LINE_WIDTH=25 mil
MIN_NECK_WIDTH=10 mil
R811 1 5% 1/16W MF 603
C827 0.1UF 20% 25V CERM 603
PPBATT_CHGR_RSNS
MIN_LINE_WIDTH=25 mil
MIN_NECK_WIDTH=10 mil
CRITICAL
R810 0.010 1% 1/2W MF 1206
PPBATT_CHGR_OUT
VOLTAGE=12.6V
MIN_LINE_WIDTH=25 mil
MIN_NECK_WIDTH=10 mil
R812 1 5% 1/16W MF 603
C828 0.1UF 20% 25V CERM 603
C812 4.7uF 20% 25V CERM 1206
C813 4.7uF 20% 25V CERM 1206
C814 4.7uF 20% 25V CERM 1206
C815 4.7uF 20% 25V CERM 1206
C816 4.7uF 20% 25V CERM 1206
C817 4.7uF 20% 25V CERM 1206
CRITICAL
C818 33uF 20% 25V ELEC SM1

SMU_CHARGE_BATT
Q877 2N7002DW SOT-363
PPBATT_ALL_VSNS

Battery Switch-over Circuit

Battery Charge Path

Battery charge FET is open when not charging

PPBATT_ALL
F895 5AMP-125V SM-2
F899 5AMP-125V SM-2
PPBATT_ALL_FUSEA
VOLTAGE=12.6V
MIN_LINE_WIDTH=25 mil
MIN_NECK_WIDTH=10 mil
PPBATT_ALL_FUSEB
VOLTAGE=12.6V
MIN_LINE_WIDTH=25 mil
MIN_NECK_WIDTH=10 mil

CRITICAL
Q890
SI4435DY
SOI

PPBATT_CHGR_OUT
R890 470K 5% 1/16W MF 402
PPBUS_ALL_A
CHGR_CHARGE_EN_L_DIV
R891 100K 5% 1/16W MF 402
CHGR_CHARGE_EN_L
Q882 2N7002DW SOT-363
SMU_CHARGE_BATT
R892 100K 5% 1/16W MF 402

CRITICAL
Q895 SUD45P03 TO-252
R895 470K 5% 1/16W MF 402
BATT_PBUSA_EN_L
MIN_LINE_WIDTH=10 mil
MIN_NECK_WIDTH=10 mil
R896 100K 5% 1/16W MF 402

CRITICAL
Q899 SUD45P03 TO-252
PPBUS_ALL_B
R899 470K 5% 1/16W MF 402
BATT_PBUS_EN_L
R898 100K 5% 1/16W MF 402
SMU_ACIN_L
R897 158K 1% 1/16W MF 402
DP800 BAS16TW SOT-363
BATT_ACIN_L_RC
C897 10uF 20% 6.3V CERM 805
Q800 2N7002DW SOT-363

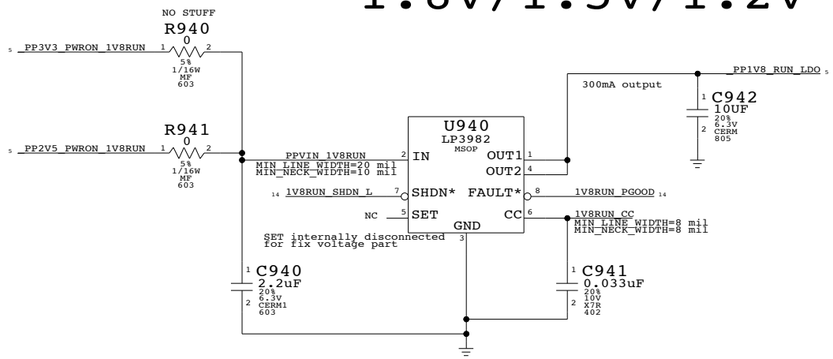
When AC is disconnected, P-channel FETs turn on
RC time is 480K * 10uF @ 3.3V
When AC is connected, P-channel
FETs are quickly turned off (diode)

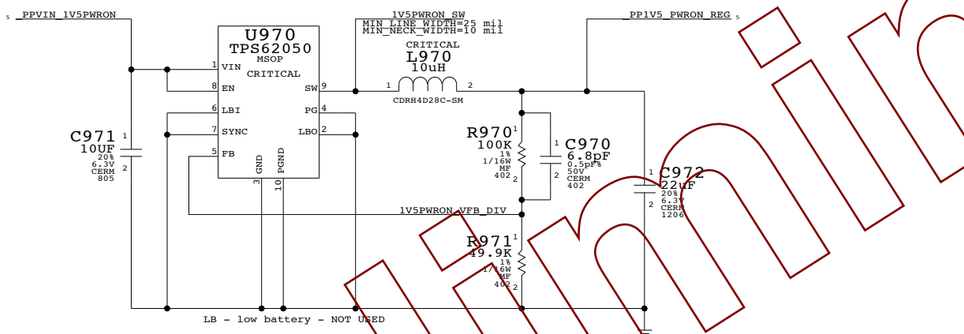
SMBus Battery Charger

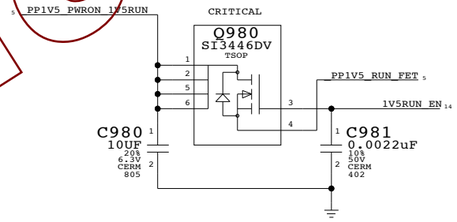
APPLE COMPUTER INC.

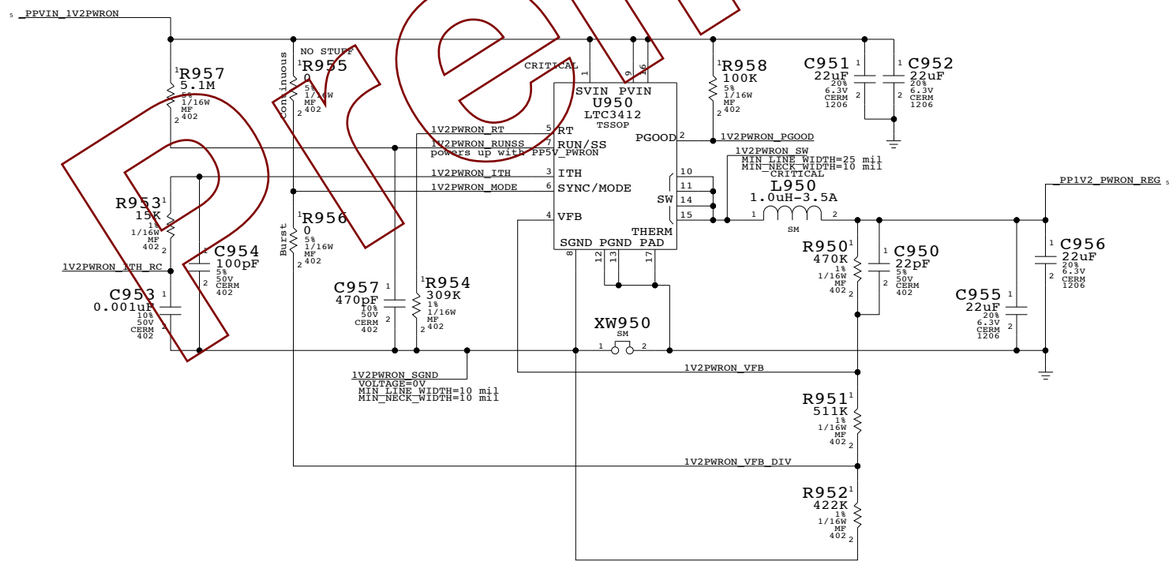
SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 8 OF 103	

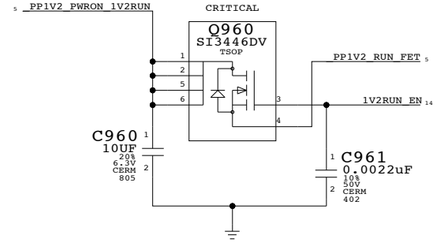
1.8V/1.5V/1.2V MAIN SUPPLIES











1.8V/1.5V Supplies

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6532	03
	SCALE: NONE	SHT 9 OF 103	

3.3V/5V MAIN SUPPLY

PPVIN_5V3VPWRON

PPVCC_ALL_3V5V
VOLTAGE=18.5V
MIN_LINE_WIDTH=15 mil
MIN_NECK_WIDTH=10 mil

PP5V_5V3V_VREF5
VOLTAGE=5V
MIN_LINE_WIDTH=20 mil
MIN_NECK_WIDTH=10 mil

5VPWRON_BOOST_ESR
MIN_LINE_WIDTH=20 mil
MIN_NECK_WIDTH=10 mil

3V3PWRON_BOOST_ESR
MIN_LINE_WIDTH=20 mil
MIN_NECK_WIDTH=10 mil

5VPWRON_SW
MIN_LINE_WIDTH=25 mil
MIN_NECK_WIDTH=10 mil

3V3PWRON_SW
MIN_LINE_WIDTH=25 mil
MIN_NECK_WIDTH=10 mil

PP5V_PWRON_REG

PP3V3_PWRON_REG

5VPWRON_TRIP
5VPWRON_LH
5VPWRON_LL
5VPWRON_FB
5VPWRON_INV
5VPWRON_SS
5V3VPWRON_SKIP
5V3VPWRON_PGOOD
(PP5V_PWRON)

3V3PWRON_TRIP
3V3PWRON_LH
3V3PWRON_LL
3V3PWRON_FB
3V3PWRON_INV
3V3PWRON_SS
5V3VPWRON_REF
5V3VPWRON_CT
5V3VPWRON_FLT

5V_STBY_L
3V3_STBY_L

5VPWRON_INV_RC
5VPWRON_FB_RC
3V3PWRON_INV_RC
3V3PWRON_FB_RC

U1000
TPS5120
TSOP
5V_STBY VREF5 VCC
STBY2 TRIP2 OUT2_U LL2 OUT2_D GUNGD2 FB2 INV2 SOFTSTART2 PWM/SKIP POWERGOOD REG5V_IN GND
STBY1 TRIP1 LH1 OUT1_U LL1 OUT1_D OUTGND1 FB1 INV1 SOFTSTART1 REF CT FLT
>2V = SKIP
<0.5V = PWM

Q1060 IRF7821 SO-8
Q1061 SI4336DY SO-8
Q1065 SI4816DY SOI-8

D1030 SOT23 30V-200MA
D1031 SM MBR0540
D1060 SM MBRS140T3
D1035 SOT23 30V-200MA
D1036 SM MBR0540

L1060 4.7UH IHLP-5050
L1065 10uH SM

R1050 10 5% 1/16W MF 402
R1052 11K 1% 1/16W MF 402
R1053 15K 1% 1/16W MF 402
R1031 3.3 5% 1/16W MF 402
R1032 0 5% 1/16W MF 402
R1036 0 5% 1/16W MF 402
R1035 3.3 5% 1/16W MF 402
R1070 100K 1% 1/16W MF 402
R1071 17.4K 1% 1/16W MF 402
R1072 10K 5% 1/16W MF 402
R1073 20.5K 1% 1/16W MF 402
R1080 100K 1% 1/16W MF 402
R1081 10K 1% 1/16W MF 402
R1082 10K 5% 1/16W MF 402
R1083 34.8K 1% 1/16W MF 402
R1033 100K 5% 1/16W MF 402

C1052 0.01uF 20% 16V CERM 402
C1050 0.1uF 20% 25V CERM 603
C1053 0.01uF 20% 16V CERM 402
C1060 4.7uF 20% 25V CERM 1206
C1061 4.7uF 20% 25V CERM 1206
C1062 4.7uF 20% 25V CERM 1206
C1051 4.7UF 20% 10V CERM 1206
C1031 0.1uF 20% 10V CERM 402
C1065 4.7uF 20% 25V CERM 1206
C1066 4.7uF 20% 25V CERM 1206
C1067 4.7uF 20% 25V CERM 1206
C1035 0.1uF 20% 10V CERM 402
C1075 330uF 20% 6.3V POLY CASE-D
C1074 100uF 20% 6.3V TANT CASE-B2
C1077 22uF 20% 6.3V CERM 1206
C1071 0.001uF 10% 50V CERM 402
C1076 22uF 20% 6.3V CERM 1206
C1063 0.001uF 10% 50V CERM 402
C1081 0.001uF 10% 50V CERM 402
C1085 22uF 20% 6.3V CERM 1206
C1087 330uF 20% 6.3V POLY CASE-D
C1086 22uF 20% 6.3V CERM 1206
C1088 0.001uF 10% 50V CERM 402
C1082 0.01uF 10% 16V CERM 402
C1080 100pF 5% 50V CERM 402
C1072 0.01uF 10% 16V CERM 402
C1070 47pF 5% 50V CERM 402
C1054 0.0047uF 10% 50V CERM 402
C1059 220pF 5% 25V CERM 402
C1055 0.1uF 20% 10V CERM 402
C1056 47pF 5% 50V CERM 402
C1057 0.1uF 20% 10V CERM 402
C1058 0.0047uF 10% 25V CERM 402
C1003 0.01uF 20% 16V CERM 402
C1011 10uF 20% 6.3V CERM 805
C1005 0.1uF 20% 10V CERM 402
C1006 10UF 20% 6.3V CERM 805
C1012 10UF 20% 6.3V CERM 805
C1009 0.0022uF 10% 50V CERM 402
C1001 100uF 20% 6.3V POLY CASE-B-3528
C1004 100uF 20% 6.3V POLY CASE-B-3528
C1013 100uF 20% 6.3V TANT CASE-B2

Q1003 SI2443DV TSOP
Q1004 SI3443DV TSOP
Q1007 SI3443DV TSOP

XW1003 SM

5V START TO TURN ON ~12.5MS AFTER DCDC_EN_L
3V START TO TURN ON ~25MS AFTER DCDC_EN_L
DIODE WILL ENSURE DCDC_EN_L IS QUICKLY DISCHARGED DURING SHUT-DOWN
POWERDOWN DELAY IS AROUND 4MS-15.6MS

is 10K necessary?
another 0.1uF needed?

GND_5V3V
VOLTAGE=0V
MIN_LINE_WIDTH=15 mil
MIN_NECK_WIDTH=10 mil

SYS_SLEEP
5VRUNHD_EN
5VRUN_EN_L
3V3RUN_EN_L
PP5V_PWRON_5VRUN
PP3V3_PWRON_3V3RUN
PP5V_RUN_HD_FET
PP3V3_RUN_FET

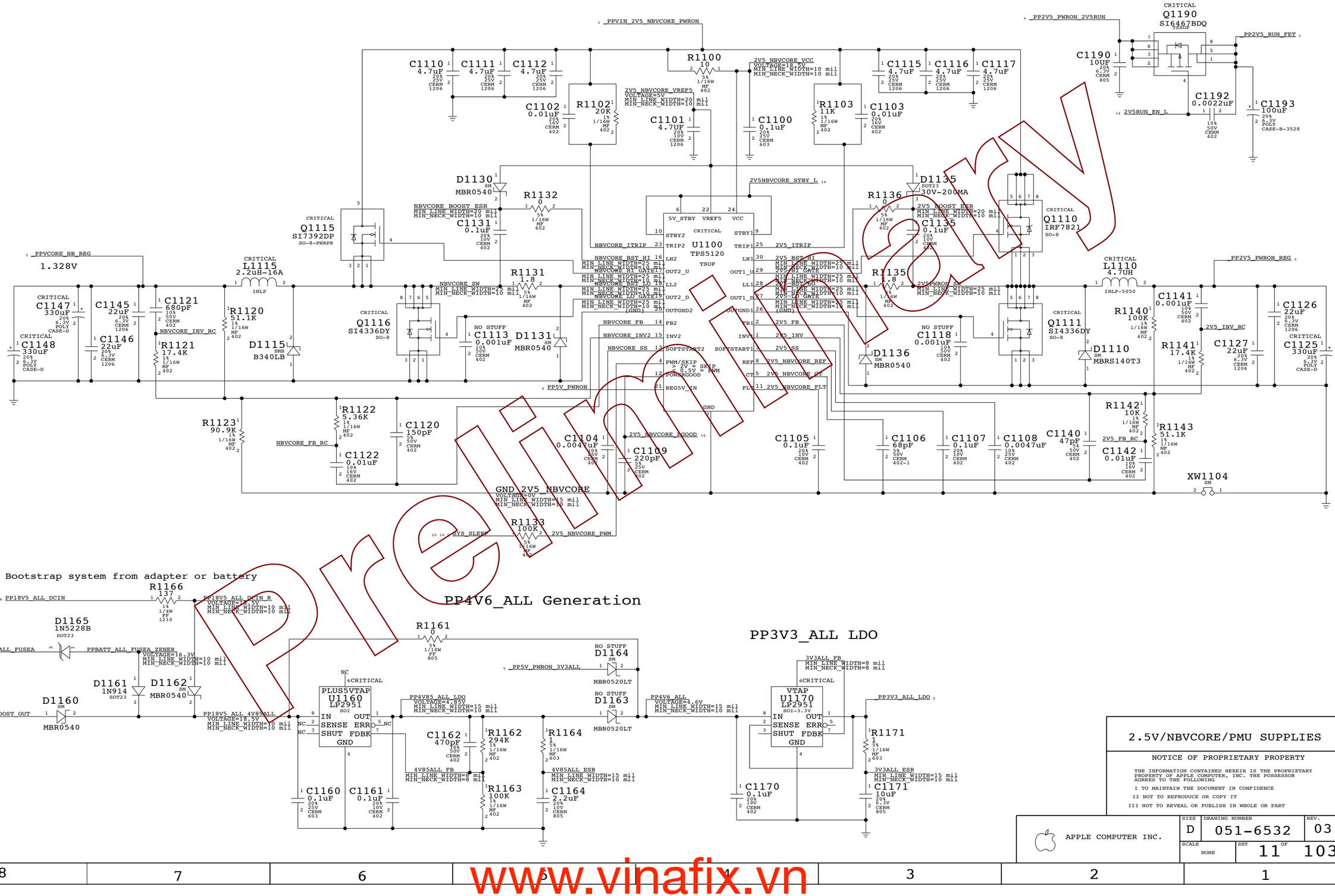
3.3V/5V REGULATOR

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03

SCALE	SHT
NONE	10 OF 103

2.5V/NBVCORE MAIN SUPPLIES



2.5V/NBVCORE/PMU SUPPLIES

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03

SCALE	SHT	OF
NONE	11	103

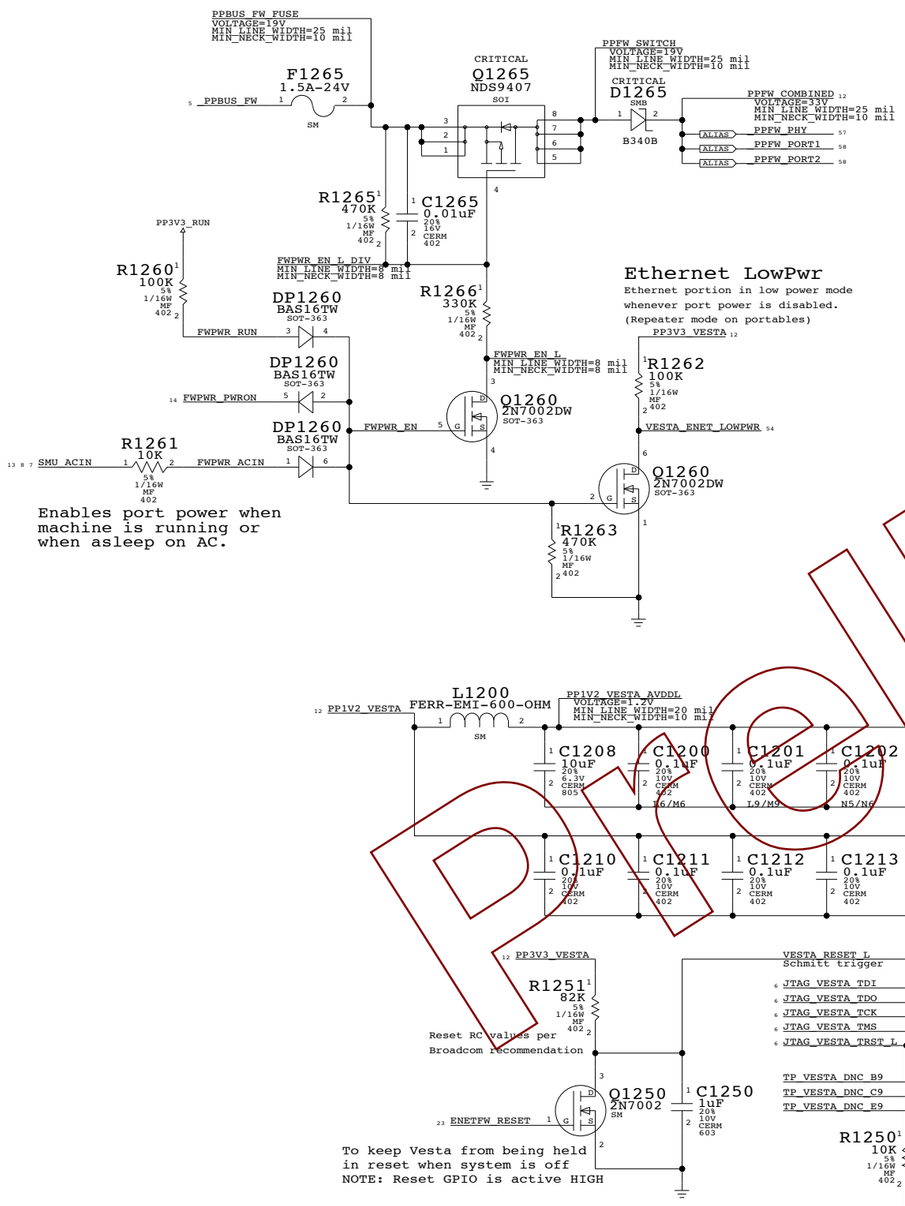
Page Notes

Power aliases required by this page:
- _PPBUS_FW (system supply for bus power)
- _PP12V_RUN_FW (backup PHY power)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- VESTA1V2_BURST / VESTA1V2_PULSE
  Controls operating mode of Vesta 1.2V regulator. If both options are off the regulator will be in continuous mode.

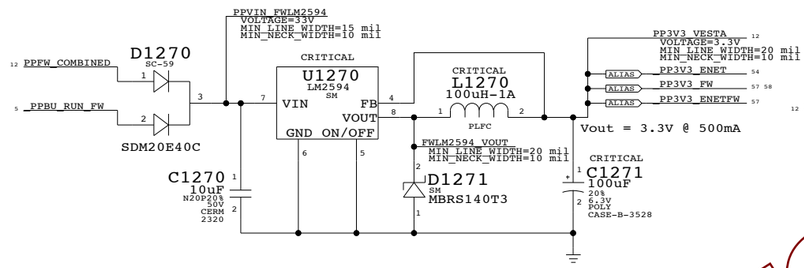
Port Power Switch



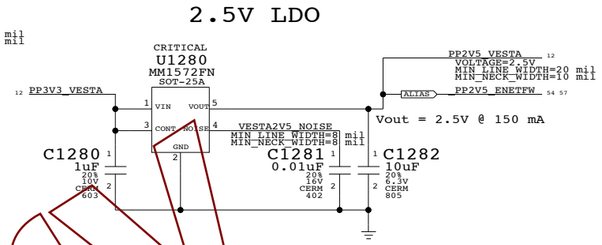
Ethernet LowPwr

Ethernet portion in low power mode whenever port power is disabled.
(Repeater mode on portables)

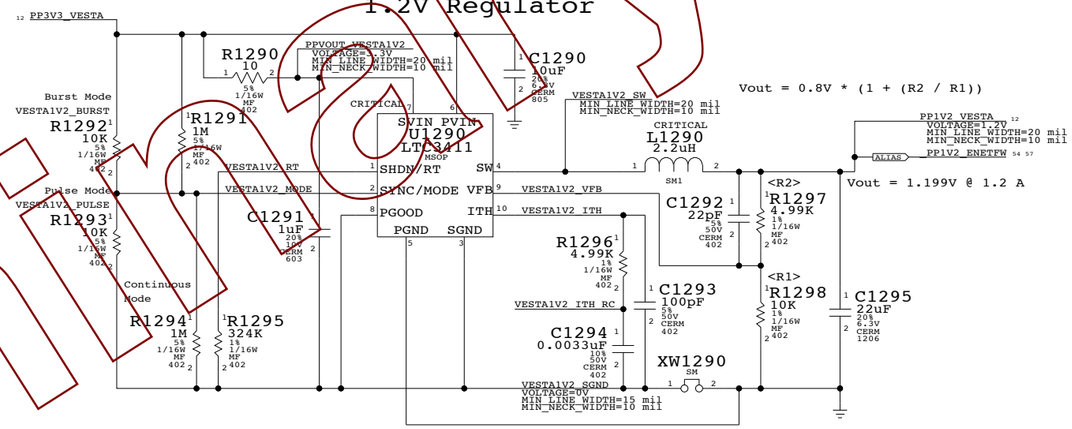
3.3V Regulator



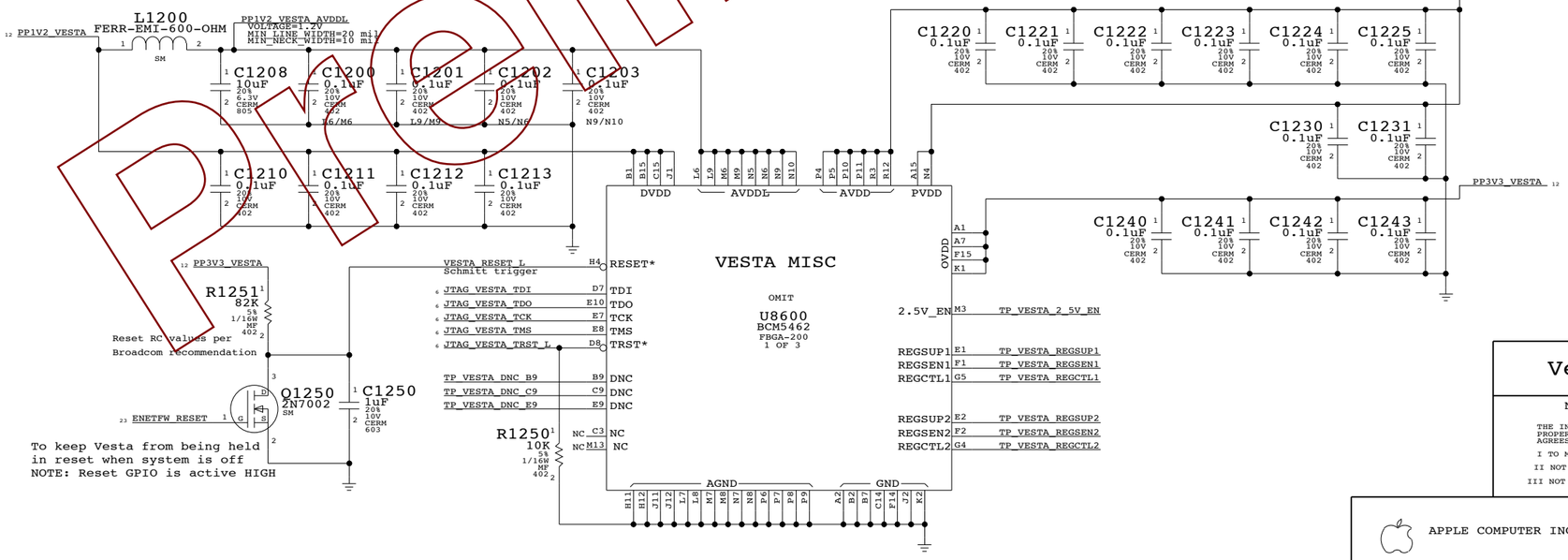
2.5V LDO



1.2V Regulator



VESTA MISC



Master: Link

Vesta Core / Misc

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 12 OF 103	

_DRAWING
TITLE=FIZZY
ABBREV=DRAWING
LAST_MODIFIED=Mon Feb 23 19:03:46 2004

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
SMU_CLK10M_XTAL	15_MIL_SPACING		SMU_CLK10M_XIN 13
	15_MIL_SPACING		SMU_CLK10M_XOUT 13
	15_MIL_SPACING		SMU_CLK10M_XOUT_R 13
RTC_CLK32K_XTAL	15_MIL_SPACING		RTC_CLK32K_X1 13
	15_MIL_SPACING		RTC_CLK32K_X2 13

Page Notes

Power aliases required by this page:
- _PP3V3_ALL_SMU
- _PP3V3_ALL_RTC
- _PP3V3_PWRON_SMU
- _PPVREF_SMU (SMU AVCC or 2.5V reference)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

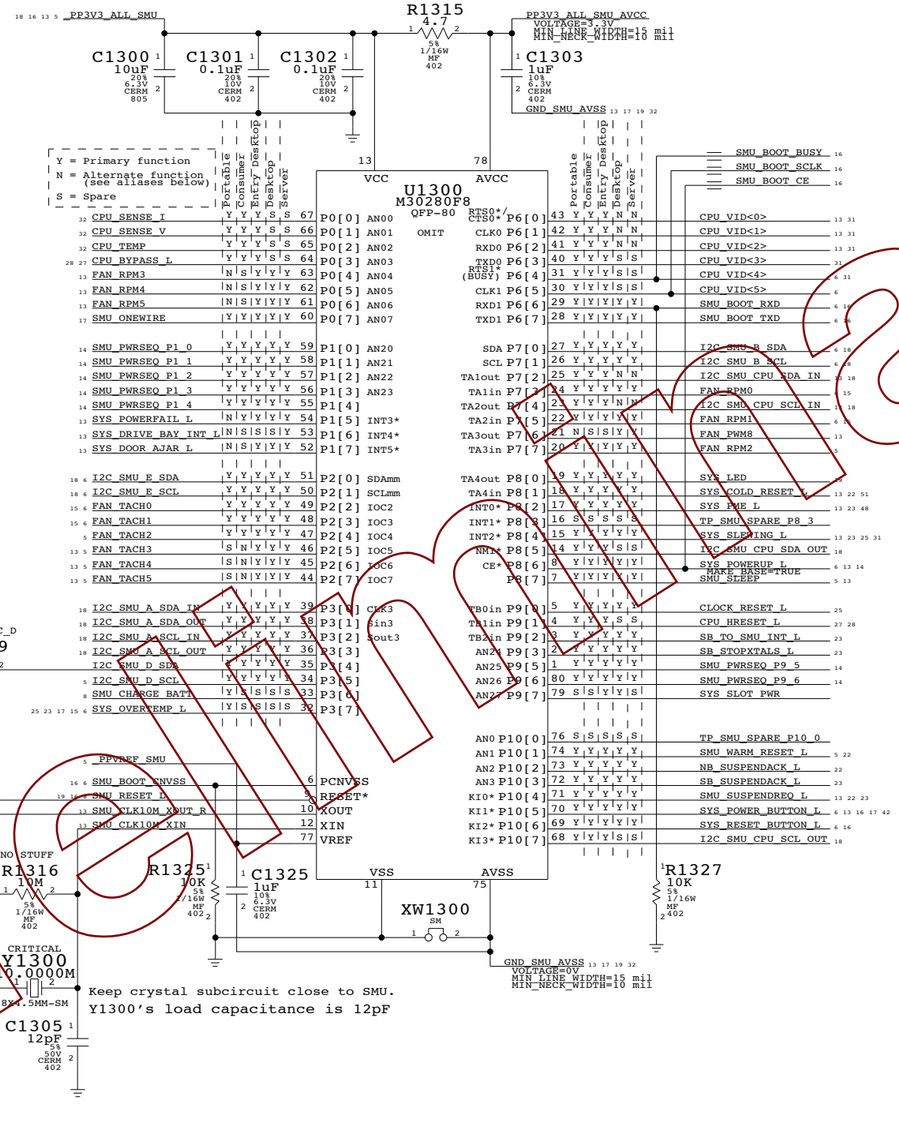
NOTE: CPU current/voltage monitoring (CPU_SENSE_I/CPU_SENSE_V) requires 100K/10uF RC filter at SMU pins. Caps should connect to GND_SMU_AVSS. SMU_VREF should be same signal or reference used by monitoring circuit, but be aware that this will affect other analog inputs such as AC adapter ID.

NOTE: All analog inputs to SMU should have a 100pF capacitor to the SMU AVSS signal (GND_SMU_AVSS). None of those capacitors are provided on this page.

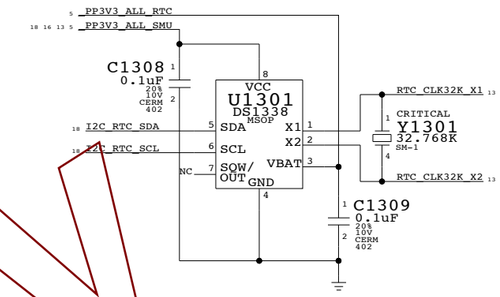
NOTE: Some primary and alternate functions reuire pull-ups that are not. provided on this page. Please. review the latest SMU specification to ensure missing pull-ups are provided on another page.

NOTE: Pinout matches SMU pinout v1.51.

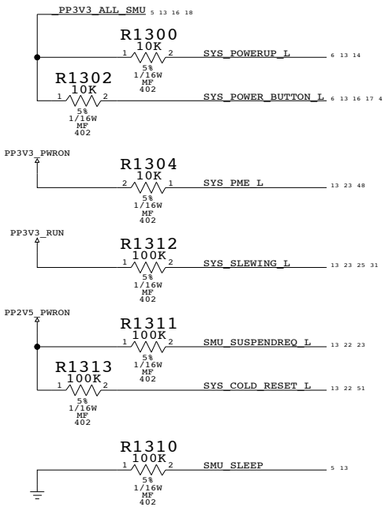
System Management Unit



Real Time Clock



SMU Pull-ups / pull-down



Alternate Functions

Portable

	Port		
FAN_RPM3	0.4	—	ALS0_OUT
FAN_RPM4	0.5	—	ALS1_OUT
FAN_RPM5	0.6	—	ALS_GAIN_BOOST
SYS_POWERFAIL_L	1.5	—	SMU_ACIN
SYS_DRIVE_BAY_INT_L	1.6	—	SMU_BATT_DET_L
SYS_DOOR_AJAR_L	1.7	—	SYS_LID_OPEN
FAN_PWM8	7.6	—	SYS_KBDLED

Consumer

	Port		
FAN_TACH3	2.5	—	SYS_LED_RED
FAN_TACH4	2.6	—	SYS_LED_GREEN
FAN_TACH5	2.7	—	SYS_LED_BLUE

Tower & Server

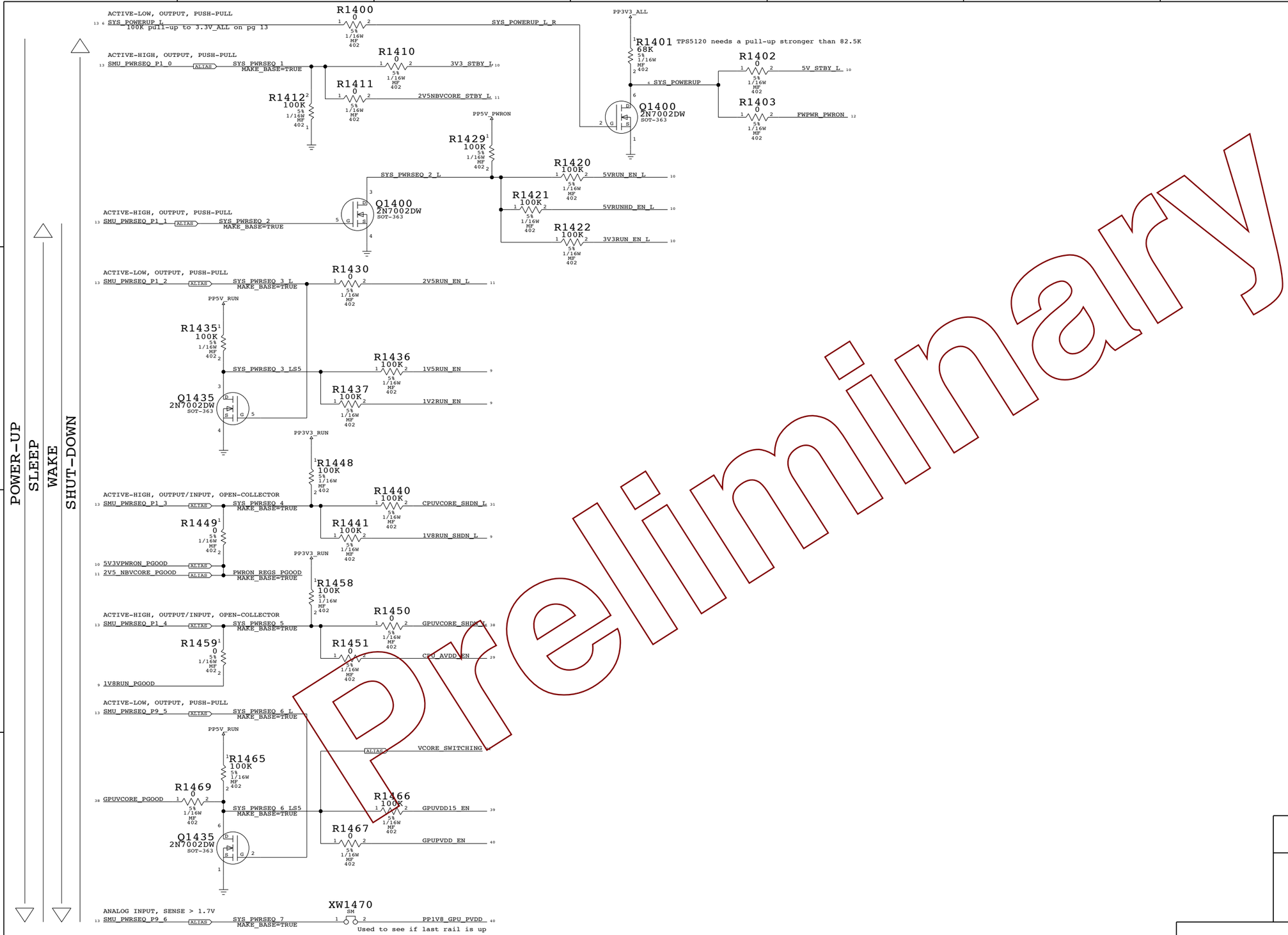
	Port		
CPU_VID<0>	6.0	—	FAN_TACH6
CPU_VID<1>	6.1	—	FAN_TACH7
CPU_VID<2>	6.2	—	FAN_TACH8
I2C_SMU_CPU_SDA_IN	7.2	—	FAN_PWM6
I2C_SMU_CPU_SCL_IN	7.4	—	FAN_PWM7

Master: Link

System Management Unit

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 13 OF 103	



Power Sequencing

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SIZE	DRAWING NUMBER	REV.
D	051-6532	03

SCALE: NONE

SHT 14 OF 103

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
	THERM	MAX1989_D1	MAX1989_D1_P
	THERM	MAX1989_D1	MAX1989_D1_N
	THERM	MAX1989_D2	MAX1989_D2_P
	THERM	MAX1989_D2	MAX1989_D2_N
	THERM	MAX1989_D3	MAX1989_D3_P
	THERM	MAX1989_D3	MAX1989_D3_N
	THERM	MAX1989_D4	MAX1989_D4_P
	THERM	MAX1989_D4	MAX1989_D4_N
	THERM	THERM_1	THERM_1_P
	THERM	THERM_1	THERM_1_N
	THERM	THERM_2	THERM_2_P
	THERM	THERM_2	THERM_2_N
	THERM	THERM_3	THERM_3_P
	THERM	THERM_3	THERM_3_N
	THERM	THERM_1B	THERM_1B_P
	THERM	THERM_1B	THERM_1B_N
	THERM	THERM_2B	THERM_2B_P
	THERM	THERM_2B	THERM_2B_N
	THERM	THERM_3B	THERM_3B_P
	THERM	THERM_3B	THERM_3B_N

Page Notes

Power aliases required by this page:
- _PP3V3_PWRON_THERM
- _PP5V_PWRON_FAN

Signal aliases required by this page:
(NONE)

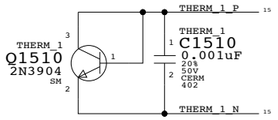
BOM options provided by this page:
- THERM_x / THERM_xB
  Selects between primary and backup thermal sensors for each of the available remote sensor locations.

Remote Temperature Sensors

Place each cap close to associated transistor

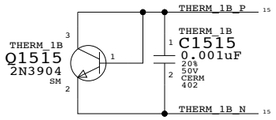
Remote 1

Place close to CPU_VCORE



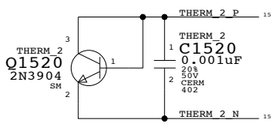
Remote 1 (Backup)

Place close to 5V/3.3V



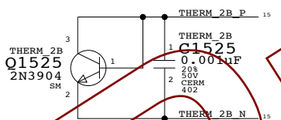
Remote 2

Place close to CPU



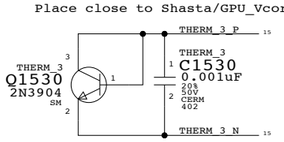
Remote 2 (Backup)

Place close to U3Lite



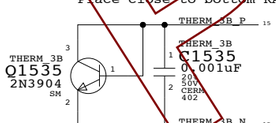
Remote 3

Place close to Shasta/GPU_Vcore



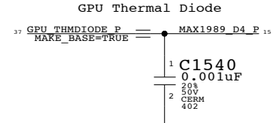
Remote 3 (Backup)

Place close to bottom RAM

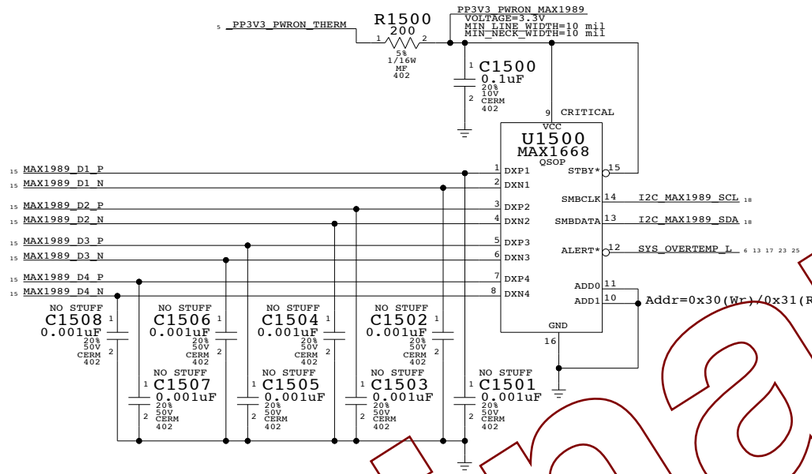


Remote 4

GPU Thermal Diode

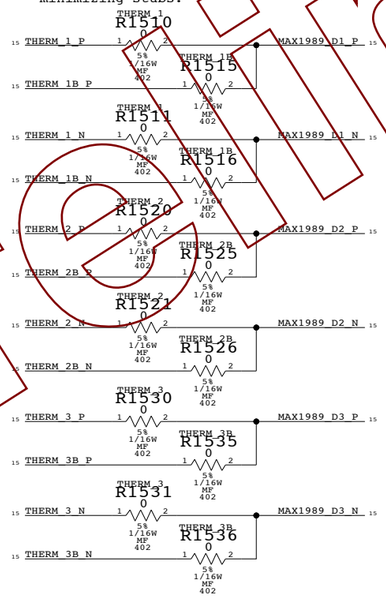


MAX1989 Thermal Sensor

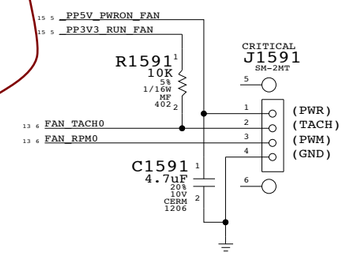


Sensor Selection

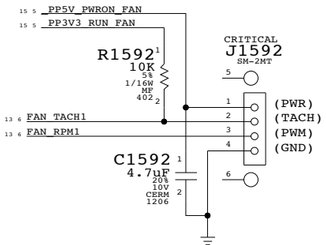
First 3 MAX1668 inputs can connect to two different sensors. These resistors should be close to MAX1668, minimizing stubs.



Fan 1



Fan 2



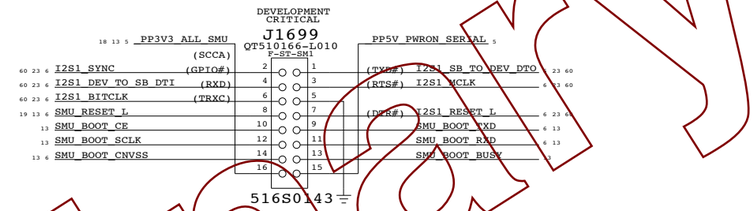
Thermal Sensor / Fans

APPLE COMPUTER INC.

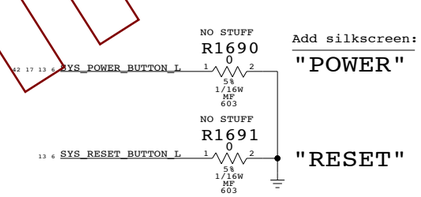
SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 15 OF 103	

SMU Download / Serial Debug Connector

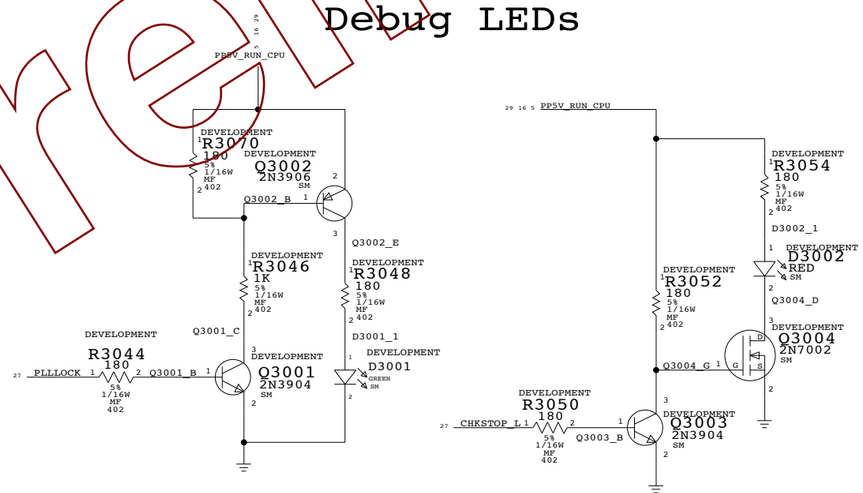
SCC same pins have pinout as modem connector to
allow serial debug flex to use either connector



Debug "Buttons"



Debug LEDs



INTERNAL I/O CONNECTORS

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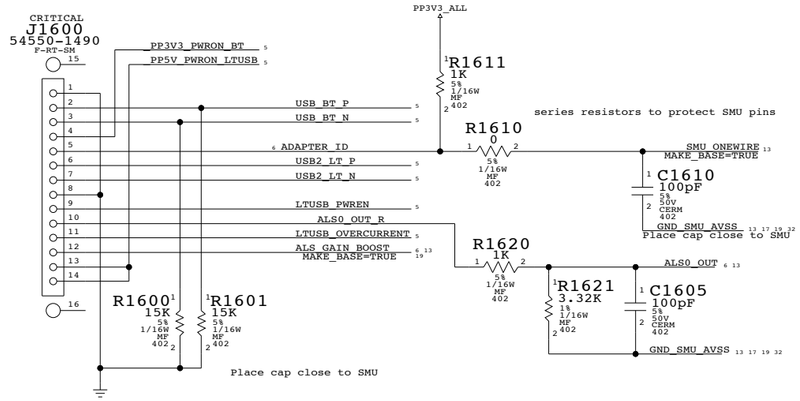
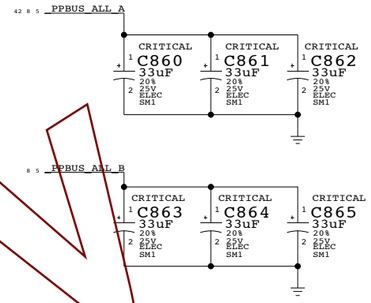
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 16 OF 103	

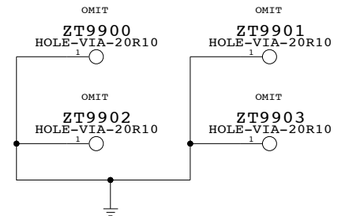
BlueTooth / Left USB Flex Connector



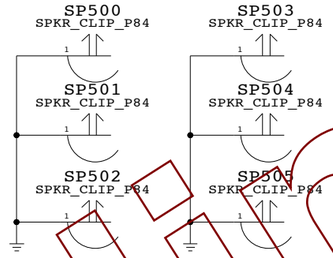
PPBUS Hold-Up Caps



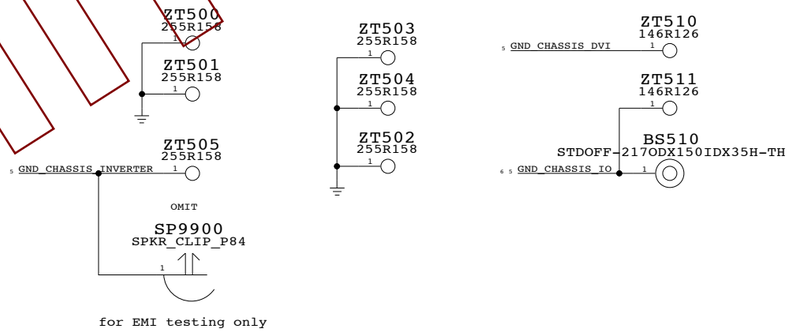
For EMI around ENET magnetic



Speaker Clips

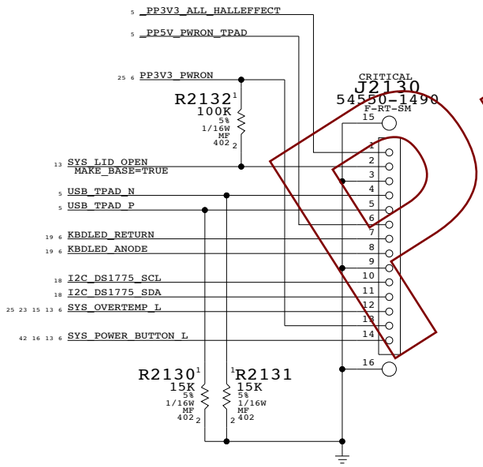


CPU Heat Sink Graphic Heat Sink Right I/O area



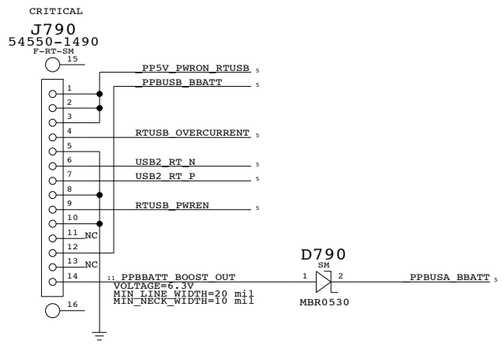
for EMI testing only

USB Trackpad Connector



overtemp may need pull-up resistor

Backup Battery / Right USB Flex Connector



_PPBUSB_BBATT is both an input and an output for backup battery circuit. _PPBUSA_BBATT is an output only.

Q51 Specific connectors

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03

SCALE	SHT	OF
NONE	18	103

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
I2C_SMU_A_OUT	I2C	I2C_SMU_A_OUT	I2C_SMU_A_SCL_OUT
I2C_SMU_A_OUT	I2C	I2C_SMU_A_OUT	I2C_SMU_A_SDA_OUT
I2C_SMU_A_IN	I2C	I2C_SMU_A_IN	I2C_SMU_A_SCL_IN
I2C_SMU_A_IN	I2C	I2C_SMU_A_IN	I2C_SMU_A_SDA_IN
I2C_SMU_CPU_OUT	I2C	I2C_SMU_CPU_OUT	I2C_SMU_CPU_SCL_OUT
I2C_SMU_CPU_OUT	I2C	I2C_SMU_CPU_OUT	I2C_SMU_CPU_SDA_OUT
I2C_SMU_CPU_IN	I2C	I2C_SMU_CPU_IN	I2C_SMU_CPU_SCL_IN
I2C_SMU_CPU_IN	I2C	I2C_SMU_CPU_IN	I2C_SMU_CPU_SDA_IN
	I2C		I2C_CPU_A_SCL
	I2C		I2C_CPU_A_SDA
	I2C		SMU_CPU_JTAG_OR_I2C
	I2C		I2C_CPU_A_SDA_TO_SMU
I2C_SMU_B	I2C	I2C_SMU_B	I2C_SMU_B_SCL
I2C_SMU_B	I2C	I2C_SMU_B	I2C_SMU_B_SDA
I2C_NB_B	I2C	I2C_NB_B	I2C_NB_B_SCL
I2C_NB_B	I2C	I2C_NB_B	I2C_NB_B_SDA
I2C_NB_C	I2C	I2C_NB_C	I2C_NB_C_SCL
I2C_NB_C	I2C	I2C_NB_C	I2C_NB_C_SDA
I2C_SB	I2C	I2C_SB	I2C_SB_SCL
I2C_SB	I2C	I2C_SB	I2C_SB_SDA

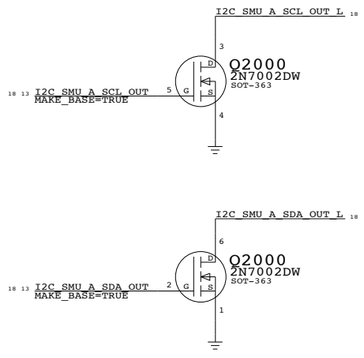
Page Notes

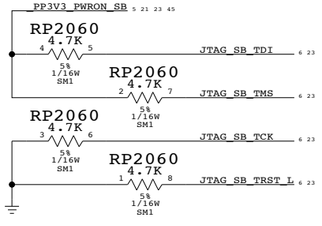
Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

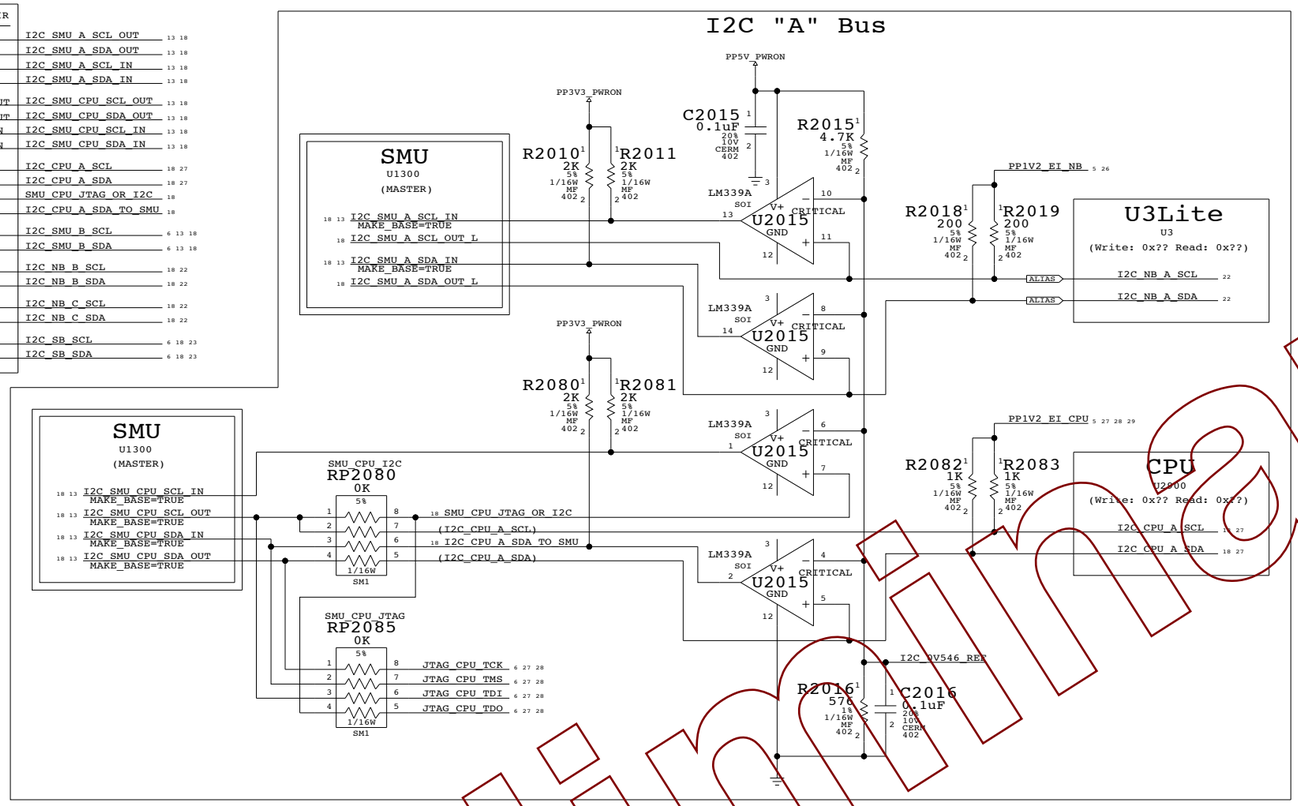
BOM options provided by this page:
(NONE)

U3 Lite I2C inversion

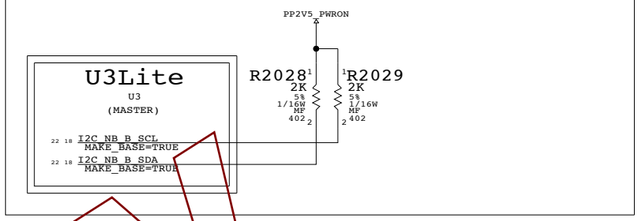




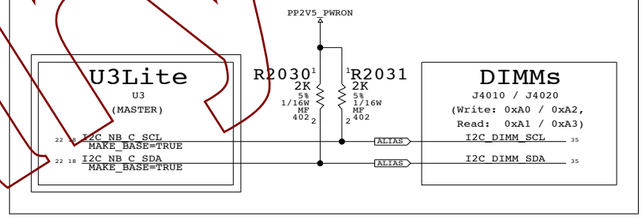
I2C "A" Bus



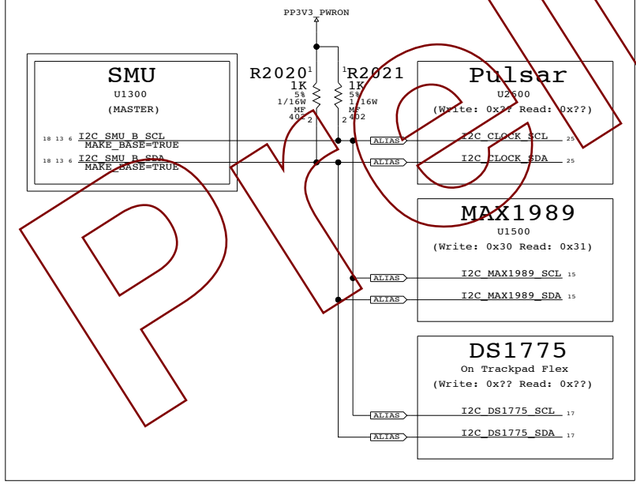
NorthBridge I2C "B" Bus



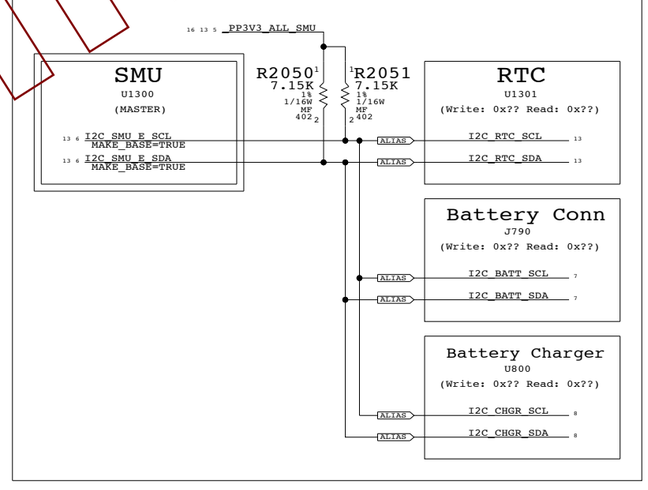
NorthBridge I2C "C" Bus



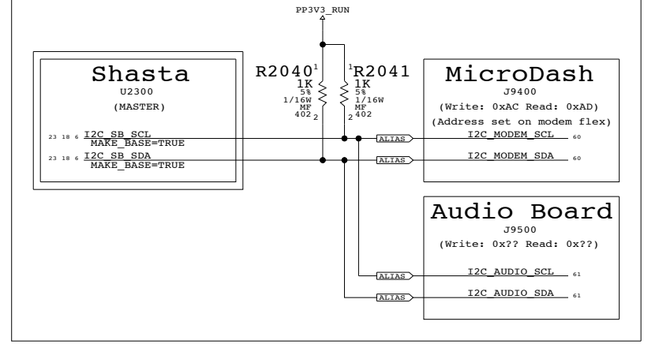
I2C "B" Bus



I2C "E" Bus



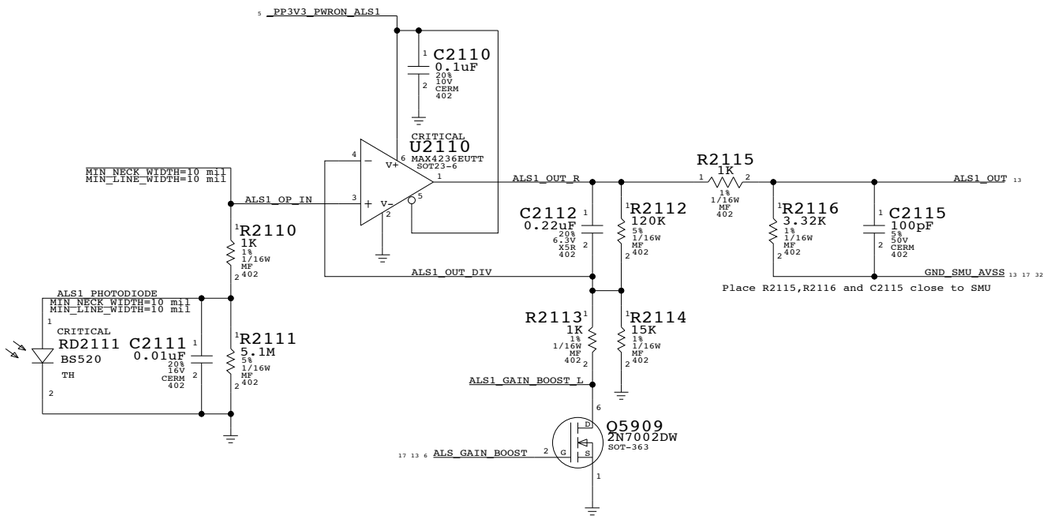
SouthBridge I2C Bus



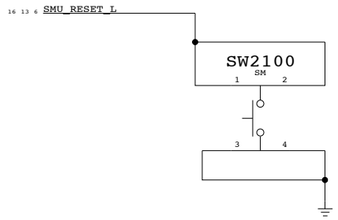
I2C CONNECTIONS

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6532	03
	SCALE: NONE	SHT 20 OF 103	

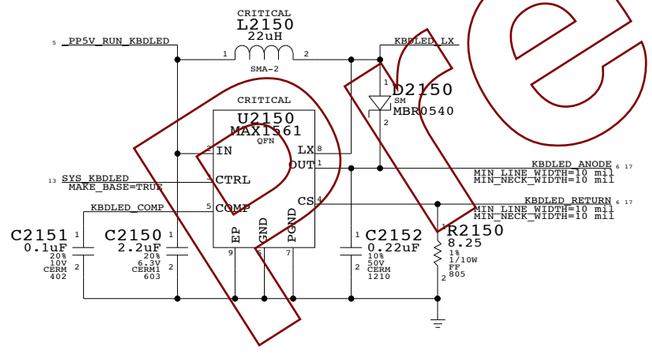
Ambient Light Sensor #1



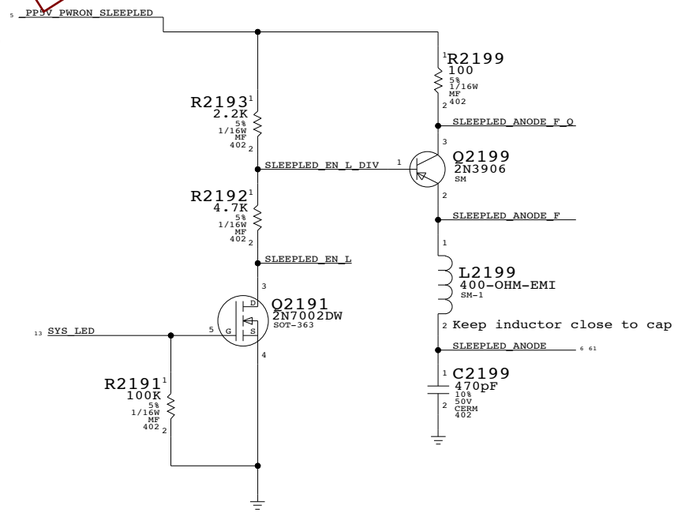
SMU / System Reset Button



Keyboard LED Driver



Sleep LED Circuit



SMU ALS/LEDs

APPLE COMPUTER INC.

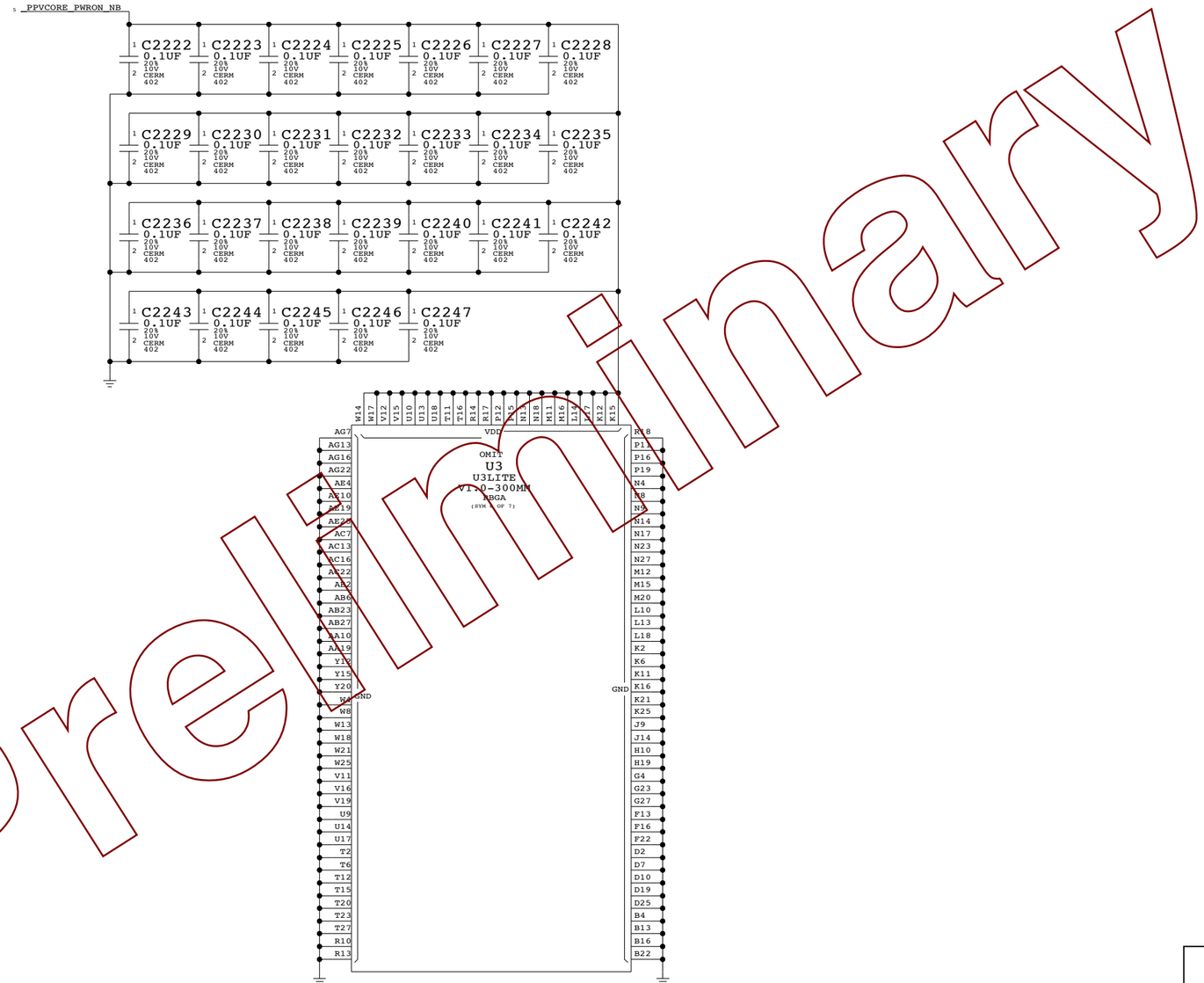
SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 21 OF 103	

Page Notes

Power aliases required by this page:
- _PPVCORE_PWRON_NB

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



Master: Link

U3Lite Core Power

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 22 OF 103	

DRAWING
TITLE=FIZZY
ABBREV=DRAWING
LAST_MODIFIED=Mon Feb 23 19:04:04 2004

Page Notes

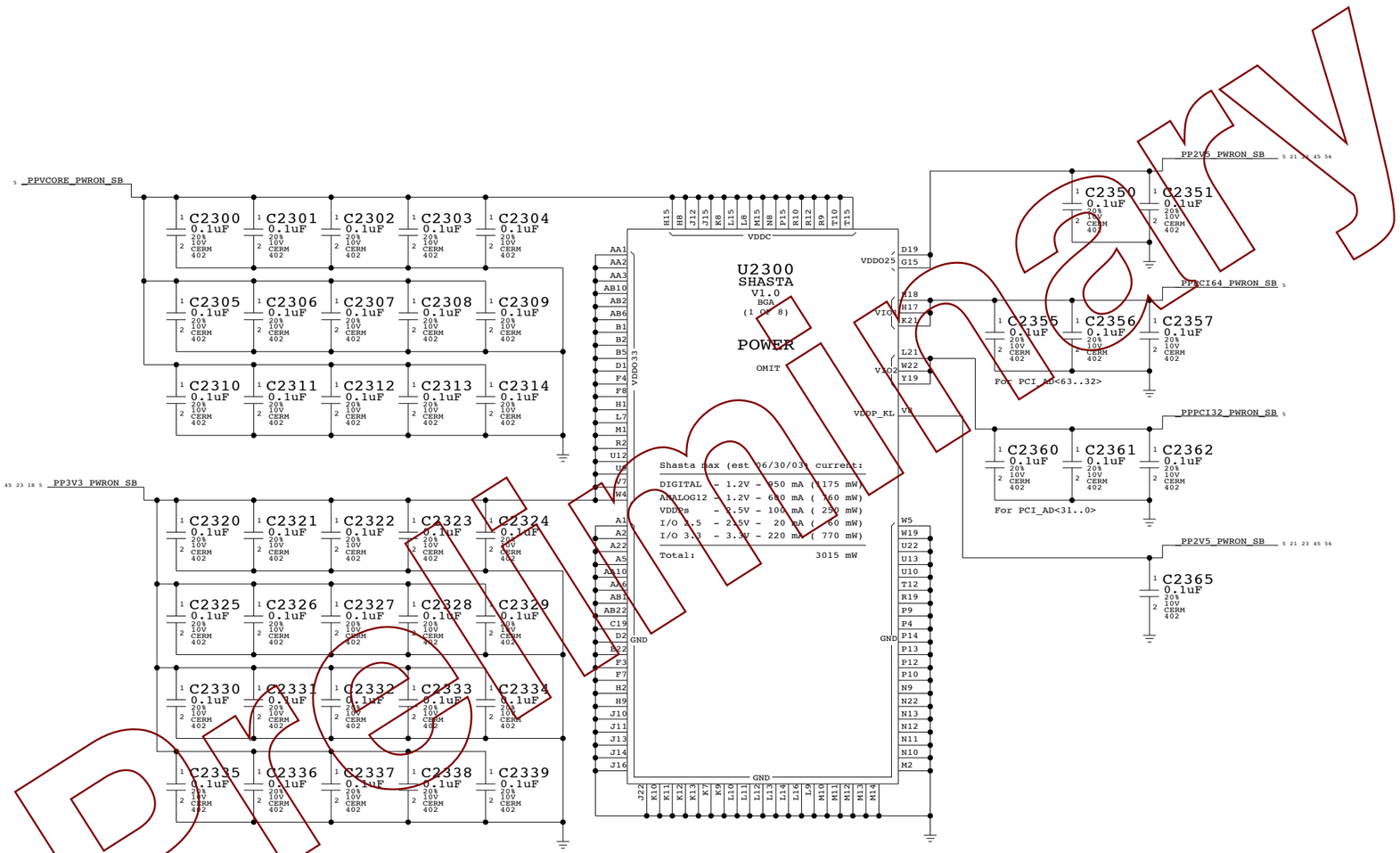
Power aliases required by this page:
- _PPPCI64_PWRON_SB (to 5V or 3.3V)
- _PPPCI32_PWRON_SB (to 5V or 3.3V)
- _PP3V3_PWRON_SB
- _PP2V5_PWRON_SB
- _PPVCORE_PWRON_SB (1.2V)

NOTE: PCI pads use the VIO supply to meet different drive timing characteristics required by the PCI spec for 5V vs. 3.3V operation. Connect _PPPCI32_PWRON_SB to appropriate PCI bus voltage and _PPPCI64_PWRON_SB to same if 64-bit PCI, otherwise 3.3V.

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Power Sequencing:
Must power Shasta VCore rail before any other Shasta supplies.



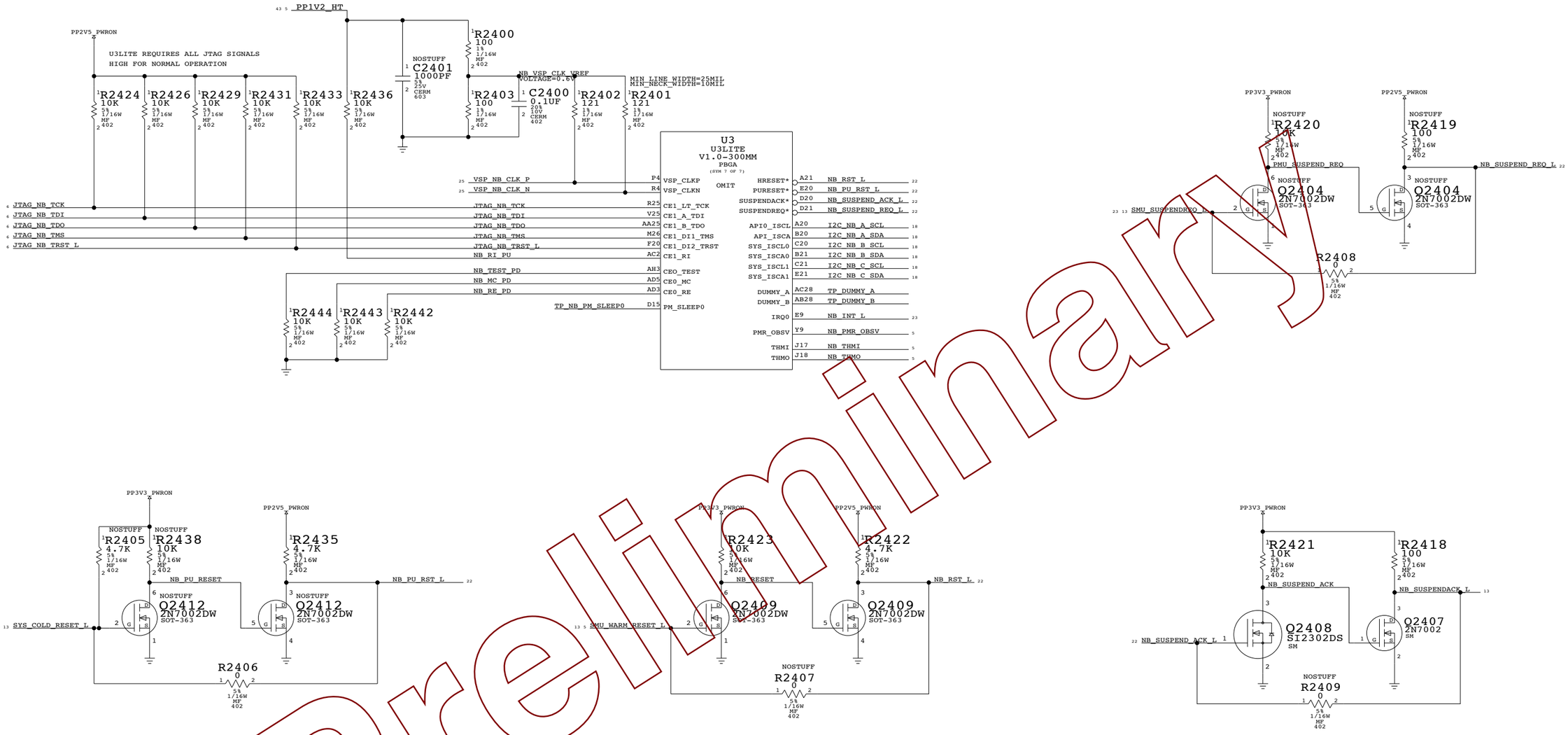
DRAWING
TITLE=FIZZY
ABBREV=DRAWING
LAST_MODIFIED=Mon Feb 23 19:04:08 2004

Master: Link

Shasta Core Power

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 23 OF 103	



ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
R100 SMU_RESET	10_MIL_SPACING		SYS_COLD_RESET_L 13 22 51
R100 SMU_RESET	10_MIL_SPACING		SYS_WARM_RESET_L 5 23 45 48

MASTER: GILA

U3LITE MISC

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 24 OF 103	

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
I2S0_TO_SB			I2S0_DEV_TO_SB_DTI 23 61
I2S0_TO_DEV			I2S0_SB_TO_DEV_DTO 23 61
I2S0_TO_DEV	10_MIL_SPACING		I2S0_MCLK 23 61
I2S0_BIDIR			I2S0_BITCLK 23 61
I2S0_BIDIR			I2S0_SYNC 23 61
I2S1_TO_SB			I2S1_DEV_TO_SB_DTI 6 16 23 60
I2S1_TO_DEV			I2S1_SB_TO_DEV_DTO 6 16 23 60
I2S1_TO_DEV	10_MIL_SPACING		I2S1_MCLK 6 16 23 60
I2S1_BIDIR			I2S1_BITCLK 6 16 23 60
I2S1_BIDIR			I2S1_SYNC 6 16 23 60
I2S2_TO_SB			I2S2_DEV_TO_SB_DTI 23 61
I2S2_TO_DEV			I2S2_SB_TO_DEV_DTO 23
I2S2_TO_DEV	10_MIL_SPACING		I2S2_MCLK 23
I2S2_BIDIR			I2S2_BITCLK 23 61
I2S2_BIDIR			I2S2_SYNC 23 61
SB_CLK18M_XTAL	15_MIL_SPACING		SB_CLK18M_XTALI 23
	15_MIL_SPACING		SB_CLK18M_XTALO 23
	15_MIL_SPACING		SB_CLK18M_XTALO_R 23
SB_CLK25M_ATA	15_MIL_SPACING		SB_CLK25M_ATA 23 25

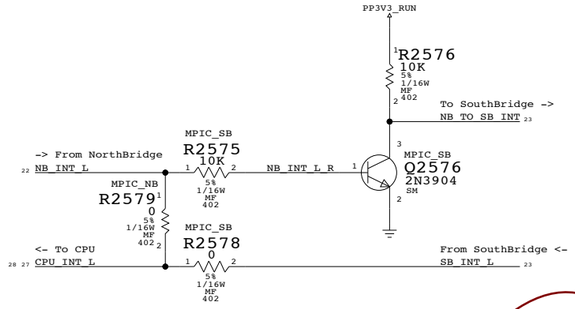
Page Notes

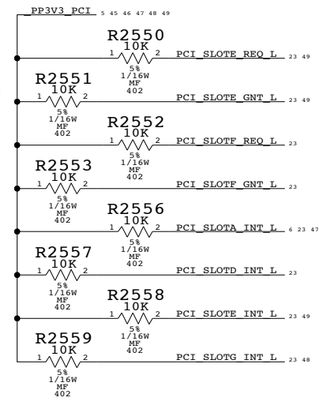
Power aliases required by this page:
- _PP3V3_PCI
- _PP3V3_PWRON_SB
- _PP2V5_PWRON_SB
- _PP1V2_PWRON_SB

Signal aliases required by this page:
(NONE)

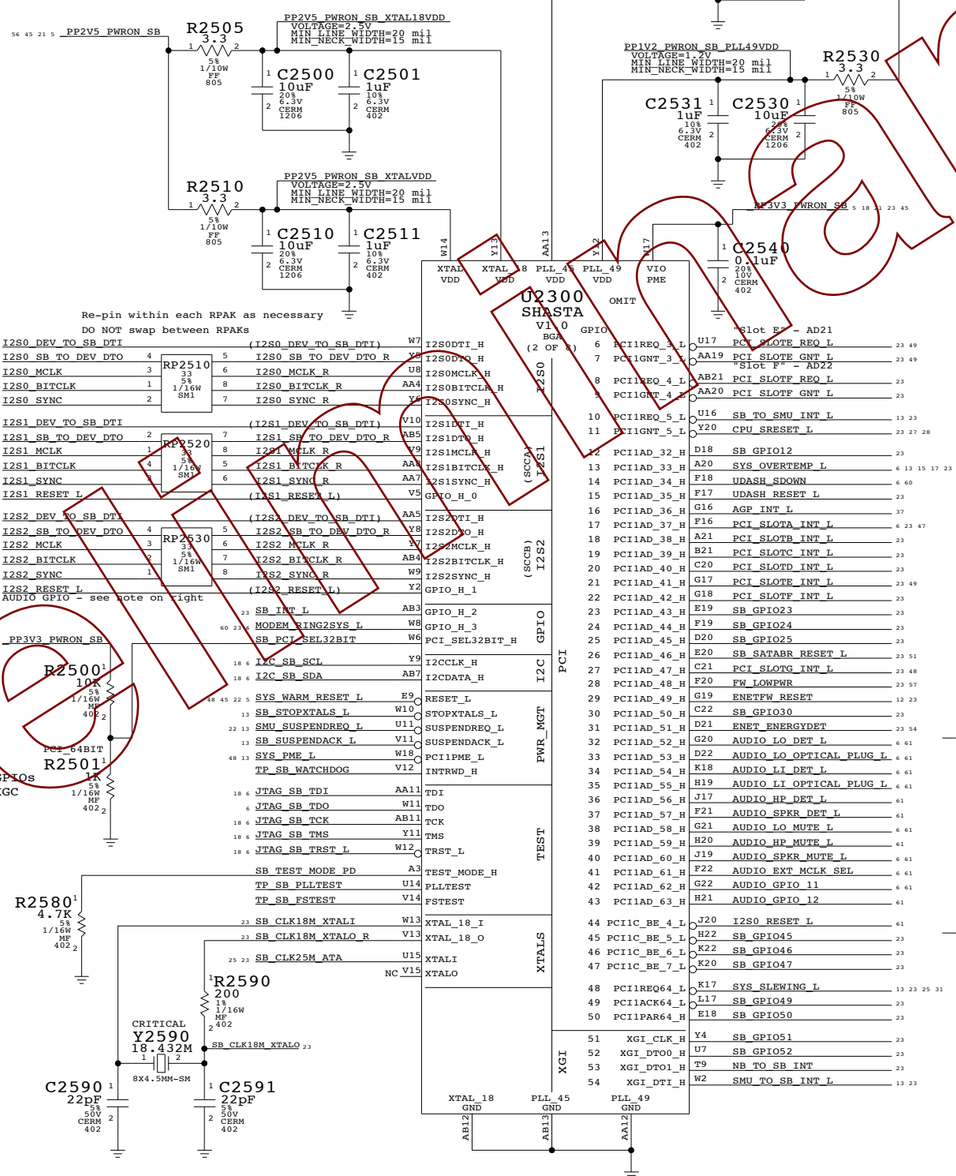
BOM options provided by this page:
- PCI_64BIT
  Configures Shasta for 64-bit PCI
  NOTE: XGC required for Shasta GPIOs
- MPIC_NB/MPIC_SB
  Selects whether NorthBridge or SouthBridge MPIC will be used for interrupt controller.

NorthBridge / SouthBridge MPIC Routing





DRAWING
TITLE=FIZZY
ABBREV=DRAWING
LAST_MODIFIED=Mon Feb 23 19:04:13 2004

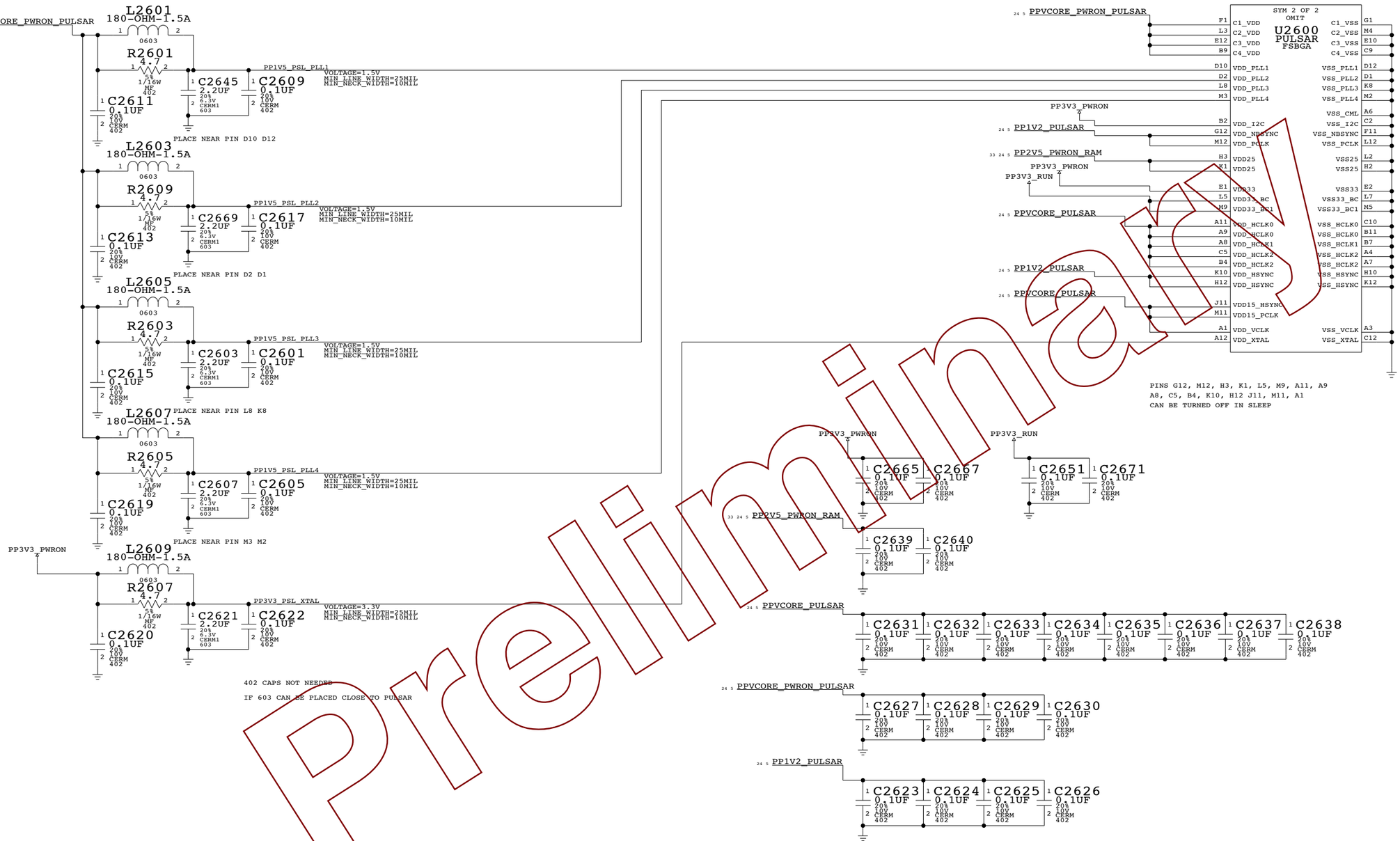


Master: Link

Shasta Serial / Misc

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 25 OF 103	



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
359S0076	1	PULSAR, PBGA	U2600	

MASTER: GILA

PULSAR POWER

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03

SCALE: NONE

SHT 26 OF 103

ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
EI_CPU_CLK_P	EI_CPU_CLK	CLOCKS	EI_CPU_CLK	186
EI_CPU_CLK_N	EI_CPU_CLK	CLOCKS	EI_CPU_CLK	187
EI_CPU1_CLK_P	EI_CPU1_CLK	CLOCKS	EI_CPU1_CLK	116
EI_CPU1_CLK_N	EI_CPU1_CLK	CLOCKS	EI_CPU1_CLK	117
EI_NB_CLK_P	EI_NB_CLK	CLOCKS	EI_NB_CLK	176
EI_NB_CLK_N	EI_NB_CLK	CLOCKS	EI_NB_CLK	177
EI_CPU_SYNC	EI_SYNC	CLOCKS		120
EI_NB_SYNC		CLOCKS		180
EI_CPU1_SYNC	EI_CPU1_SYNC	CLOCKS		118
VSP_NB_CLK_P	VSP_NB_CLK	CLOCKS	VSP_NB_CLK	194
VSP_NB_CLK_N	VSP_NB_CLK	CLOCKS	VSP_NB_CLK	195
AGP_CLK66M_NB	AGP_NB_CLK	CLOCKS		1600
AGP_CLK66M_GPU	AGP_GPU_CLK	CLOCKS		1601
HT_CLK66M_NB	HT_NB_CLK	CLOCKS		1102
HT_CLK66M_SB	HT_SB_CLK	CLOCKS		1101
PCI_CLK66M_SB_INT	CLOCKS_PCI	CLOCKS		1600
PCI_CLK33M_SB_EXT	CLOCKS_PCI	CLOCKS		1021
PLS_EXTCLK	PLS_XTAL	CLOCKS		1110

DIFFERENTIAL SIGNALS SHOULD HAVE 5 MIL SPACING TO EACH OTHER
ALL SPACING GROUPS SHOULD HAVE 15 MIL SPACING TO SIGNALS NOT IN THEIR GROUP

EI_NB_SYNC IS PART OF EI_CPU_SYNC TOPOLOGY

SYM 1 OF 2

OMIT
U2600
PULSAR
FSBGA

			NET SPACING TYPE
GPCLK33_0	L4	PCI_CLK_GP0_R	CLOCKS
GPCLK33_1	K4	PCI_CLK_GP1_R	CLOCKS
VCLKN	A2	VSP_NB_CLK_N_C	CLOCKS
VCLKP	B3	VSP_NB_CLK_P_C	CLOCKS
HCLKN_0	B10	EI_CPU_CLK_N_C	CLOCKS
HCLKN_1	C8	EI_CPU1_CLK_N_R	CLOCKS 5
HCLKN_2	C4	EI_NB_CLK_N_C	CLOCKS
HCLKP_0	A10	EI_CPU_CLK_P_C	CLOCKS
HCLKP_1	B8	EI_CPU1_CLK_P_R	CLOCKS 5
HCLKP_2	B5	EI_NB_CLK_P_C	CLOCKS
GPCLK25_0	J3	PLS_CLK_66M_0_R	CLOCKS
GPCLK25_1	J1	PLS_CLK_66M_1_R	CLOCKS
PCLK25_0	K2	HT_CLK66M_NB_R	CLOCKS
PCLK25_1	L1	RAM_CLK66M_NB_R	CLOCKS
PCLK33_0	K5	PCI_CLK66M_SB_INT_R	CLOCKS
PCLK33_1	L6	PCI_CLK_P1_R	CLOCKS
PCLK33_2	M7	AGP_CLK66M_GPU_R	CLOCKS
PCLK33_3	L9	PCI_CLK_P3_R	CLOCKS
PCLK33_4	M10	PCI_CLK_P4_R	CLOCKS
HTBEN_0	K11	CPU_HTBEN_R	CLOCKS
HTBEN_1	J12	CPU1_HTBEN_R	CLOCKS 5
NBSYNC	F12	EI_NB_SYNC_R	CLOCKS
HSYNC_0	J10	EI_CPU_SYNC_R	CLOCKS
HSYNC_1	H11	EI_CPU1_SYNC_R	CLOCKS 5
REFCLK_0	G2	SB_CLK25M_ATA_R	CLOCKS
REFCLK_1	H1	SATA_CLK25M_R	CLOCKS
SLEWING*	K9	SLEWING_L_R	CLOCKS
ERROR*	M8	CLOCK_ERROR_L	
PCLK12	L11	HT_CLK66M_SB_R	CLOCKS
PCLK15	L10	AGP_CLK66M_NB_R	CLOCKS

SCLK	C1	18 I2C_CLOCK_SCL
SDATA	B1	18 I2C_CLOCK_SDA
RESET*	D3	PLS_RESET_L
XIN	C11	PLS_X_IN
XOUT	B12	PLS_X_OUT
ADDRSEL	E3	PLS_X_ADDRSEL
TEST1	K3	TP_PLS_TEST1
TEST2	E11	TP_PLS_TEST2
TEST3	D11	TP_PLS_TEST3
SCAN_MODE	M1	PLS_SCAN_MODE
REF15	G11	PLS_REF15
REF25	J2	PLS_REF25
REF33	M6	PLS_REF33
REF_CML	A5	TP_PLS_REF_CML
RES_CML	B6	PLS_PRES_CML
FORCESPO*	F2	PLS_FORCE_P0_L_R
PD	C3	PLS_POWER_DOWN

0=IIC ADDR D2/D3
1=IIC ADDR D4/D5

R2701 0 5% 1 2 3.3V 33MHZ PCI_CLK_GP0 5
R2761 0 5% 402 1 2 3.3V 33MHZ PCI_CLK_GP1 5

C2708 0.001UF 50V 10% 1 2CERM 402 VSP_NB_CLK_P 22 25
C2710 0.001UF 50V 10% 1 2CERM 402 VSP_NB_CLK_N 22 25
C2713 0.001UF 50V 10% 1 2CERM 402
C2715 0.001UF 50V 10% 1 2CERM 402 EI_CPU_CLK_P 25 27, EI_CPU_CLK_N 25 27
C2700 0.001UF 50V 10% 1 2CERM 402 EI_NB_CLK_P 25 26
C2702 0.001UF 50V 10% 1 2CERM 402 EI_NB_CLK_N 25 26

R2704 0 5% 402 1 2 — 13 CLOCK_RESET_L
R2738 1K 5% 1/16W MF 402 NOSTUFF 1 2
R2722 1K 5% 1/16W MF 402 1 2 — 17 6 PP3V3_PWRON
R2748 0 5% 1/16W MF 402 NOSTUFF 1 2 — 23 17 15 13 6 SYS_OVERTEMP_L
R2706 249 1% 402 1 2
R2744 681 1% 402 1 2
R2740 1K 1% 402 1 2
R2746 1K 1% 402 1 2
R2742 806 1% 402 1 2
R2750 0 5% 402 1 2 — 11 10 5 SYS_SLEEP (SLEEP)
R2724 1K 5% 402 NOSTUFF 1 2
R2752 0 5% 1/16W MF 402 NO STUFF 1 2 — 15 PLS_EXTCLK
R2754 0 5% 1/16W MF 402 1 2
R2758 330K 5% 1/16W MF 402 NO STUFF 1 2
R2756 0 5% 1/16W MF 402 1 2
R2762 24 5% 1/16W MF 402 NOSTUFF 1 2 — PLS_INTERM
R2764 24 5% 1/16W MF 402 NOSTUFF 1 2
J2700 U.FL-R SMT F-ST-SM NOSTUFF 1 2 3
Y2701 25.0000M CRITICAL 8X4.5MM-SM 1 2 — PLS_X_IN_B, PLS_X_OUT_B
C2707 33PF 5% 50V CERM 402 1 2
C2705 33PF 5% 50V CERM 402 1 2

R2775 0 5% 402 1 2 2.5V 66MHZ TP_PLS_CLK_66M_0
R2776 0 5% 402 1 2 2.5V 66MHZ TP_PLS_CLK_66M_1
R2703 20 5% 402 1 2 2.5V 66MHZ HT_CLK66M_NB 25 43
R2709 20 5% 402 1 2 2.5V 66MHZ RAM_CLK66M_NB 33
R2705 0 5% 402 1 2 3.3V 66MHZ PCI_CLK66M_SB_INT 25 45
R2711 0 5% 402 1 2 3.3V 33MHZ PCI_CLK_P1 5
R2707 0 5% 402 1 2 3.3V 66MHZ AGP_CLK66M_GPU 25 37
R2702 0 5% 402 1 2 3.3V 33MHZ PCI_CLK_P3 5
R2779 0 5% 402 1 2 PCI_CLK_P4 5
R2715 0 5% 402 1 2 1.2V 33MHZ CPU_HTBEN 27 28
R2768 0 5% 402 1 2 1.2V EI_NB_SYNC 25 26
R2772 0 5% 402 1 2 1.2V EI_CPU_SYNC 25 27
R2770 20 5% 402 NOSTUFF 1 2 2.5V 25MHZ SB_CLK25M_ATA 23
R2700 22 5% 402 1 2 2.5V 25MHZ TP_SATA_CLK25M
R2720 0 5% 402 1 2 SYS_SLEWING_L 13 23 31
R2717 0 5% 402 1 2 1.2V 66MHZ HT_CLK66M_SB 25 44
R2719 0 5% 402 1 2 1.5V 66MHZ AGP_CLK66M_NB 25 36

MASTER: GILA

PULSAR CLOCKS

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 27 OF 103	

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
EI_CPU_TO_NB_CLK_P	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_CLK	2812
EI_CPU_TO_NB_CLK_N	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_CLK	2813
EI_NB_TO_CPU_CLK_P	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	2814
EI_NB_TO_CPU_CLK_N	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	2815
EI_CPU_TO_NB_AD<0..43>	EI_CPU_TO_NB_CAD	EI_CPU_TO_NB_AD	2816
EI_NB_TO_CPU_AD<0..43>	EI_NB_TO_CPU_CAD	EI_NB_TO_CPU_AD	2817
EI_CPU_TO_NB_SR_P<0>	EI_CPU_TO_NB_CAD	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_SR0	2818
EI_CPU_TO_NB_SR_N<0>	EI_CPU_TO_NB_CAD	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_SR0	2819
EI_CPU_TO_NB_SR_P<1>	EI_CPU_TO_NB_CAD	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_SR1	2820
EI_CPU_TO_NB_SR_N<1>	EI_CPU_TO_NB_CAD	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_SR1	2821
EI_NB_TO_CPU_SR_P<0>	EI_NB_TO_CPU_CAD	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_SR0	2822
EI_NB_TO_CPU_SR_N<0>	EI_NB_TO_CPU_CAD	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_SR0	2823
EI_NB_TO_CPU_SR_P<1>	EI_NB_TO_CPU_CAD	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_SR1	2824
EI_NB_TO_CPU_SR_N<1>	EI_NB_TO_CPU_CAD	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_SR1	2825

PP1V5_PWRON_NB_AVDD → R2800 2.2 5% 1/16W MF 603 → PP1V5_PWRON_EI_NB_AVDD (VOLTAGE=1.5V; MIN_LINE_WIDTH=25MIL, MIN_NECK_WIDTH=10MIL)

C2818 1UF 10% 6.3V CERM 402

C2819 0.1UF 20% 10V CERM 402

PP1V2_EI_NB

U3 U3LITE V1.0-300MM PBGA (SYM 1 OF 7) OMIT

APPLE PI INTERFACE

EI_NB_TO_CPU_CLK_P	F15	APIO_BCLKIP	APIO_BCLKOP	D6	EI_CPU_TO_NB_CLK_P
EI_NB_TO_CPU_CLK_N	E15	APIO_BCLKIN	APIO_BCLKON	E6	EI_CPU_TO_NB_CLK_N
EI_NB_TO_CPU_AD<0>	F11	APIO_ADI0	APIO_ADO0	J2	EI_CPU_TO_NB_AD<0>
EI_NB_TO_CPU_AD<1>	F12	APIO_ADI1	APIO_ADO1	H1	EI_CPU_TO_NB_AD<1>
EI_NB_TO_CPU_AD<2>	G11	APIO_ADI2	APIO_ADO2	J1	EI_CPU_TO_NB_AD<2>
EI_NB_TO_CPU_AD<3>	H11	APIO_ADI3	APIO_ADO3	K1	EI_CPU_TO_NB_AD<3>
EI_NB_TO_CPU_AD<4>	G12	APIO_ADI4	APIO_ADO4	E1	EI_CPU_TO_NB_AD<4>
EI_NB_TO_CPU_AD<5>	H12	APIO_ADI5	APIO_ADO5	F2	EI_CPU_TO_NB_AD<5>
EI_NB_TO_CPU_AD<6>	H14	APIO_ADI6	APIO_ADO6	J4	EI_CPU_TO_NB_AD<6>
EI_NB_TO_CPU_AD<7>	G14	APIO_ADI7	APIO_ADO7	H4	EI_CPU_TO_NB_AD<7>
EI_NB_TO_CPU_AD<8>	D9	APIO_ADI8	APIO_ADO8	G1	EI_CPU_TO_NB_AD<8>
EI_NB_TO_CPU_AD<9>	C9	APIO_ADI9	APIO_ADO9	H2	EI_CPU_TO_NB_AD<9>
EI_NB_TO_CPU_AD<10>	D11	APIO_ADI10	APIO_ADO10	F1	EI_CPU_TO_NB_AD<10>
EI_NB_TO_CPU_AD<11>	E11	APIO_ADI11	APIO_ADO11	H5	EI_CPU_TO_NB_AD<11>
EI_NB_TO_CPU_AD<12>	A10	APIO_ADI12	APIO_ADO12	H3	EI_CPU_TO_NB_AD<12>
EI_NB_TO_CPU_AD<13>	A9	APIO_ADI13	APIO_ADO13	J3	EI_CPU_TO_NB_AD<13>
EI_NB_TO_CPU_AD<14>	A8	APIO_ADI14	APIO_ADO14	J5	EI_CPU_TO_NB_AD<14>
EI_NB_TO_CPU_AD<15>	B9	APIO_ADI15	APIO_ADO15	J6	EI_CPU_TO_NB_AD<15>
EI_NB_TO_CPU_AD<16>	C11	APIO_ADI16	APIO_ADO16	E3	EI_CPU_TO_NB_AD<16>
EI_NB_TO_CPU_AD<17>	B11	APIO_ADI17	APIO_ADO17	F4	EI_CPU_TO_NB_AD<17>
EI_NB_TO_CPU_AD<18>	A11	APIO_ADI18	APIO_ADO18	E2	EI_CPU_TO_NB_AD<18>
EI_NB_TO_CPU_AD<19>	A12	APIO_ADI19	APIO_ADO19	F5	EI_CPU_TO_NB_AD<19>
EI_NB_TO_CPU_AD<20>	B12	APIO_ADI20	APIO_ADO20	H6	EI_CPU_TO_NB_AD<20>
EI_NB_TO_CPU_AD<21>	C12	APIO_ADI21	APIO_ADO21	J7	EI_CPU_TO_NB_AD<21>
EI_NB_TO_CPU_AD<22>	D12	APIO_ADI22	APIO_ADO22	F3	EI_CPU_TO_NB_AD<22>
EI_NB_TO_CPU_AD<23>	E12	APIO_ADI23	APIO_ADO23	J8	EI_CPU_TO_NB_AD<23>
EI_NB_TO_CPU_AD<24>	A13	APIO_ADI24	APIO_ADO24	F6	EI_CPU_TO_NB_AD<24>
EI_NB_TO_CPU_AD<25>	A14	APIO_ADI25	APIO_ADO25	E5	EI_CPU_TO_NB_AD<25>
EI_NB_TO_CPU_AD<26>	B14	APIO_ADI26	APIO_ADO26	D5	EI_CPU_TO_NB_AD<26>
EI_NB_TO_CPU_AD<27>	C14	APIO_ADI27	APIO_ADO27	E4	EI_CPU_TO_NB_AD<27>
EI_NB_TO_CPU_AD<28>	A16	APIO_ADI28	APIO_ADO28	D8	EI_CPU_TO_NB_AD<28>
EI_NB_TO_CPU_AD<29>	A15	APIO_ADI29	APIO_ADO29	A5	EI_CPU_TO_NB_AD<29>
EI_NB_TO_CPU_AD<30>	B15	APIO_ADI30	APIO_ADO30	C2	EI_CPU_TO_NB_AD<30>
EI_NB_TO_CPU_AD<31>	C15	APIO_ADI31	APIO_ADO31	C3	EI_CPU_TO_NB_AD<31>
EI_NB_TO_CPU_AD<32>	H15	APIO_ADI32	APIO_ADO32	C5	EI_CPU_TO_NB_AD<32>
EI_NB_TO_CPU_AD<33>	G15	APIO_ADI33	APIO_ADO33	C6	EI_CPU_TO_NB_AD<33>
EI_NB_TO_CPU_AD<34>	F17	APIO_ADI34	APIO_ADO34	B2	EI_CPU_TO_NB_AD<34>
EI_NB_TO_CPU_AD<35>	G17	APIO_ADI35	APIO_ADO35	D1	EI_CPU_TO_NB_AD<35>
EI_NB_TO_CPU_AD<36>	G18	APIO_ADI36	APIO_ADO36	B1	EI_CPU_TO_NB_AD<36>
EI_NB_TO_CPU_AD<37>	H18	APIO_ADI37	APIO_ADO37	C1	EI_CPU_TO_NB_AD<37>
EI_NB_TO_CPU_AD<38>	F18	APIO_ADI38	APIO_ADO38	A6	EI_CPU_TO_NB_AD<38>
EI_NB_TO_CPU_AD<39>	E18	APIO_ADI39	APIO_ADO39	C8	EI_CPU_TO_NB_AD<39>
EI_NB_TO_CPU_AD<40>	A17	APIO_ADI40	APIO_ADO40	A2	EI_CPU_TO_NB_AD<40>
EI_NB_TO_CPU_AD<41>	A18	APIO_ADI41	APIO_ADO41	B3	EI_CPU_TO_NB_AD<41>
EI_NB_TO_CPU_AD<42>	B17	APIO_ADI42	APIO_ADO42	A7	EI_CPU_TO_NB_AD<42>
EI_NB_TO_CPU_AD<43>	C17	APIO_ADI43	APIO_ADO43	B5	EI_CPU_TO_NB_AD<43>
EI_NB_TO_CPU_SR_P<0>	D17	APIO_SRIP0	APIO_SROP0	A3	EI_CPU_TO_NB_SR_P<0>
EI_NB_TO_CPU_SR_N<0>	A19	APIO_SRIN0	APIO_SRON0	A4	EI_CPU_TO_NB_SR_N<0>
EI_NB_TO_CPU_SR_P<1>	E17	APIO_SRIP1	APIO_SROP1	B5	EI_CPU_TO_NB_SR_P<1>
EI_NB_TO_CPU_SR_N<1>	B18	APIO_SRIN1	APIO_SRON1	B6	EI_CPU_TO_NB_SR_N<1>
EI_QACK_L	D14	APIO_QACK0	APIO_QREQ0	E14	EI_QREQ_L
	B5	APIO_APSYNC			EI_NB_CLK_P
	H17	APIO_SE	APIO_APCLKP	D18	EI_NB_CLK_N
			APIO_APCLKN	C18	
			APIO_CSTP	F14	CPU_CHKSTOP_L

PLACE R2805 AND R2806 NEAR U3LITE

EI_NB_SYNC → R2805 0 402 → NB_APSYNC

NOSTUFF R2806 0 402 EI_SYNC_FROM_NB

EI_SE

API_APCLK_AVSS

C2821 NOSTUFF 0.001UF 10% 50V CERM 402

PP1V2_EI_NB

R2802 NOSTUFF 100 1% 1/16W MF 402

R2801 NOSTUFF 100 1% 1/16W MF 402

C2820 NOSTUFF 0.1UF 20% 10V CERM 402 (EI_APCLK_VREF VOLTAGE=0.6V)

R2803 NOSTUFF 121 1% 1/16W MF 402

R2804 NOSTUFF 121 1% 1/16W MF 402 (MIN_LINE_WIDTH=25MIL, MIN_NECK_WIDTH=10MIL)

EI_NB_CLK_P, EI_NB_CLK_N

C2820, R2803, R2804 CHANGED TO 603 FOR FMAX

ZT2800 … ZT2817 0.1UF 20% 10V CERM 402

ZT2806, ZT2846, ZT2856, ZT2866 HOLE-VIA-20R10

ZT2807 … ZT2845 HOLE-VIA-20R10

ZT2847 … ZT2855 HOLE-VIA-20R10

OMIT

MASTER: GILA

U3LITE APPLE PI

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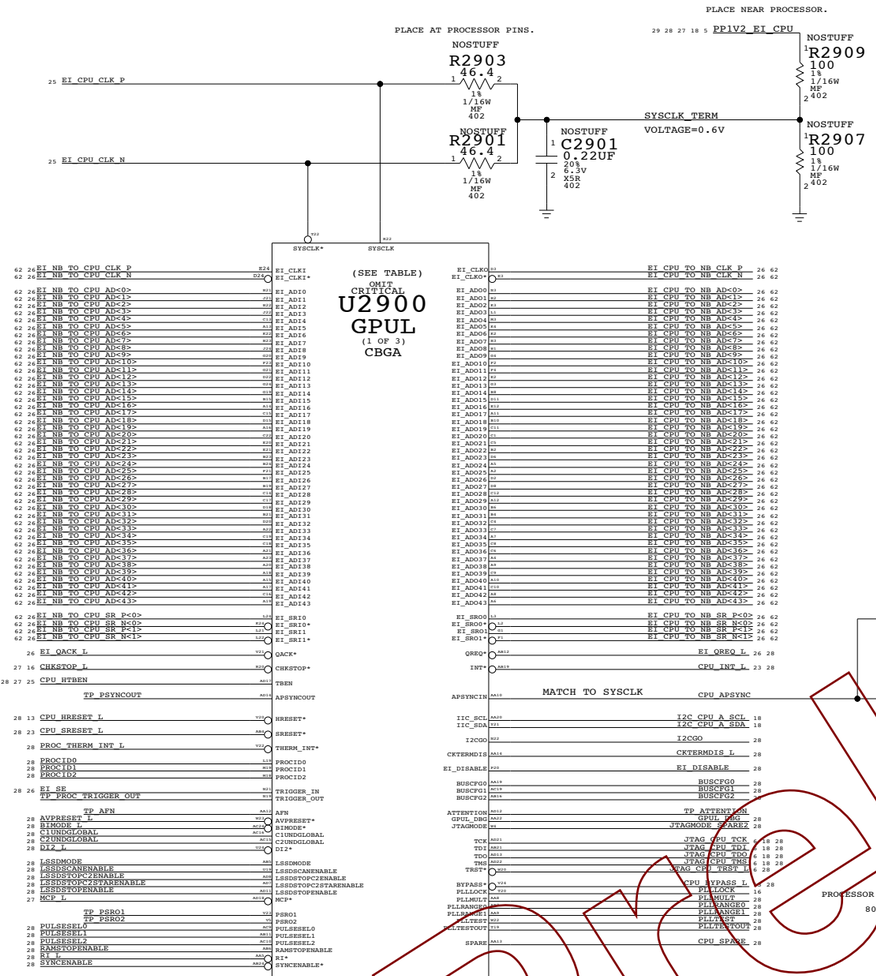
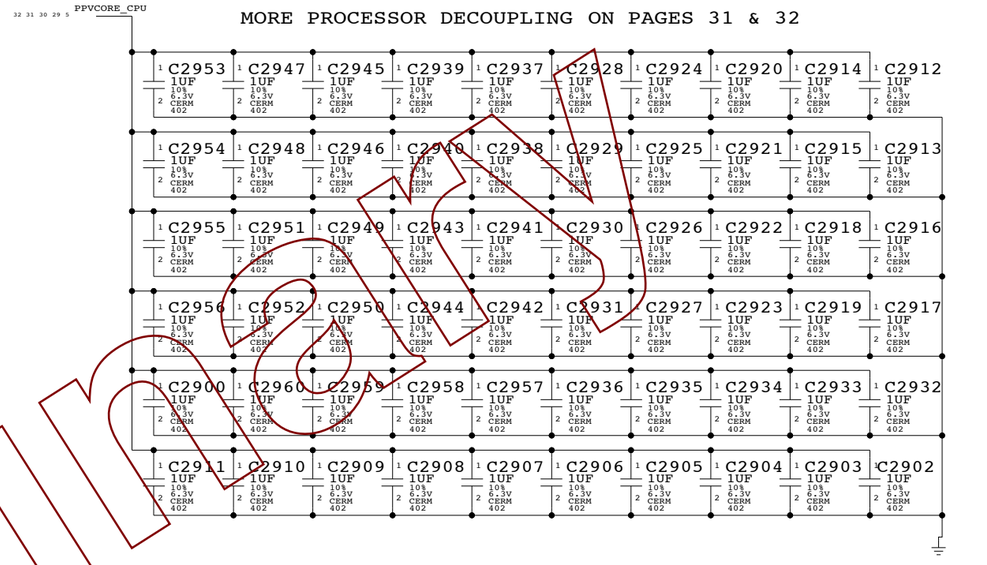
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 28 OF 103	





PROCESSOR LOGIC I/O

MASTER: GILA

NEO APPLE PI

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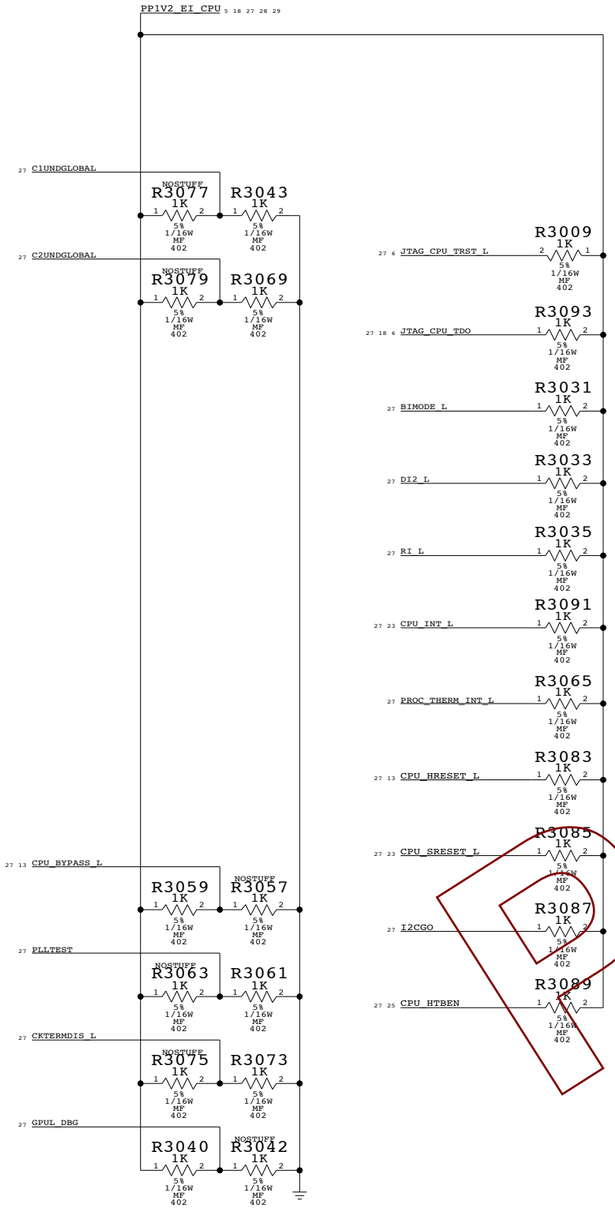
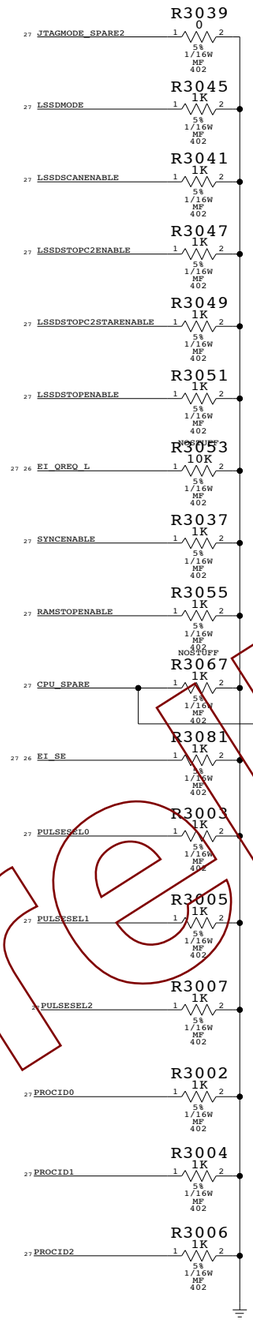
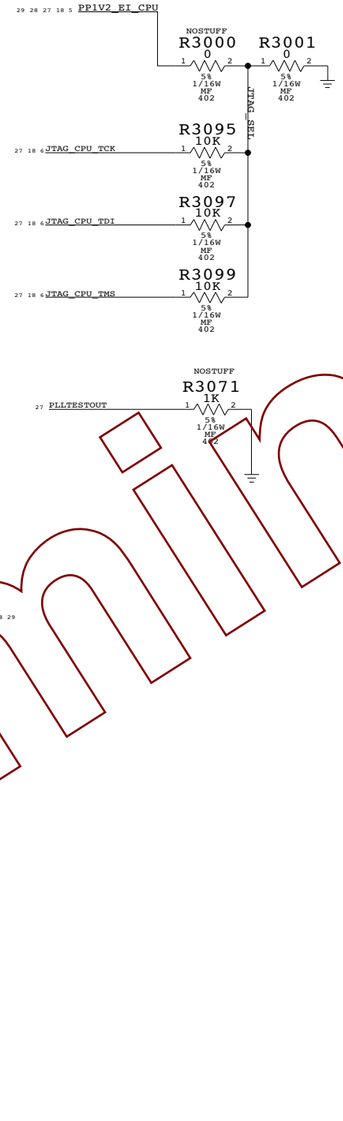
SIZE	DRAWING NUMBER	REV.
D	051-6532	03

SCALE	SHT	OF
NONE	29	103







SELECT PROCESSOR CLOCK MULTIPLIER. PROCESSOR CLOCK(MHZ)= SYSTCLOCK * PLLMULT.

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
*	114S1103	1	RES,1K OHM,1/16W,5%,0402	R3034	EI_3TO1	SYSCLK * 12
	114S1103	1	RES,1K OHM,1/16W,5%,0402	R3018	EI_2TO1	SYSCLK * 8

SELECT EI BUS DIVIDER. BUS DATA RATE(BPS)= (PROCESSOR CLOCK) / BUSCFG.

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
	114S1103	3	RES,1K OHM,1/16W,5%,0402	R3024,R3026,R3028	EI_2TO1	PROC / 2
*	114S1103	3	RES,1K OHM,1/16W,5%,0402	R3024,R3026,R3012	EI_3TO1	PROC / 3
	114S1103	3	RES,1K OHM,1/16W,5%,0402	R3024,R3010,R3028	NOSTUFF	PROC / 4
	114S1103	3	RES,1K OHM,1/16W,5%,0402	R3024,R3010,R3012	NOSTUFF	PROC / 6
	114S1103	3	RES,1K OHM,1/16W,5%,0402	R3008,R3026,R3028	NOSTUFF	PROC / 8
	114S1103	3	RES,1K OHM,1/16W,5%,0402	R3008,R3026,R3012	NOSTUFF	PROC / 12
	114S1103	3	RES,1K OHM,1/16W,5%,0402	R3008,R3010,R3028	NOSTUFF	PROC / 16
	114S1103	3	RES,1K OHM,1/16W,5%,0402	R3008,R3010,R3012	NOSTUFF	

SELECT ELASTIC MODE OR BYPASS.

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
*	114S1103	1	RES,1K OHM,1/16W,5%,0402	R3036		
	114S1103	1	RES,1K OHM,1/16W,5%,0402	R3020	NOSTUFF	BYPASS MODE

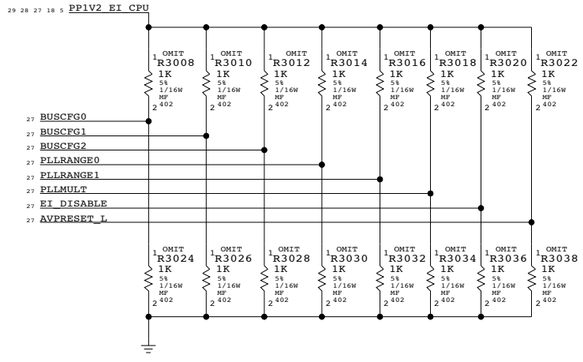
SELECT PLL FREQUENCY RANGE.

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
	114S1103	2	RES,1K OHM,1/16W,5%,0402	R3030,R3032	CPU_PLL_LOW	
*	114S1103	2	RES,1K OHM,1/16W,5%,0402	R3030,R3016	CPU_PLL_HIGH	
	114S1103	2	RES,1K OHM,1/16W,5%,0402	R3014,R3032	CPU_PLL_MEDIUM	
	114S1103	2	RES,1K OHM,1/16W,5%,0402	R3014,R3016	NOSTUFF	RESERVED

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
114S1103	1	RES,1K OHM,1/16W,5%,0402	R3022		AVPRESET OFF
114S1103	1	RES,1K OHM,1/16W,5%,0402	R3038	NOSTUFF	AVPRESET ON

* STUFF THESE ON Q45.

SYSTEM CONFIGURATION



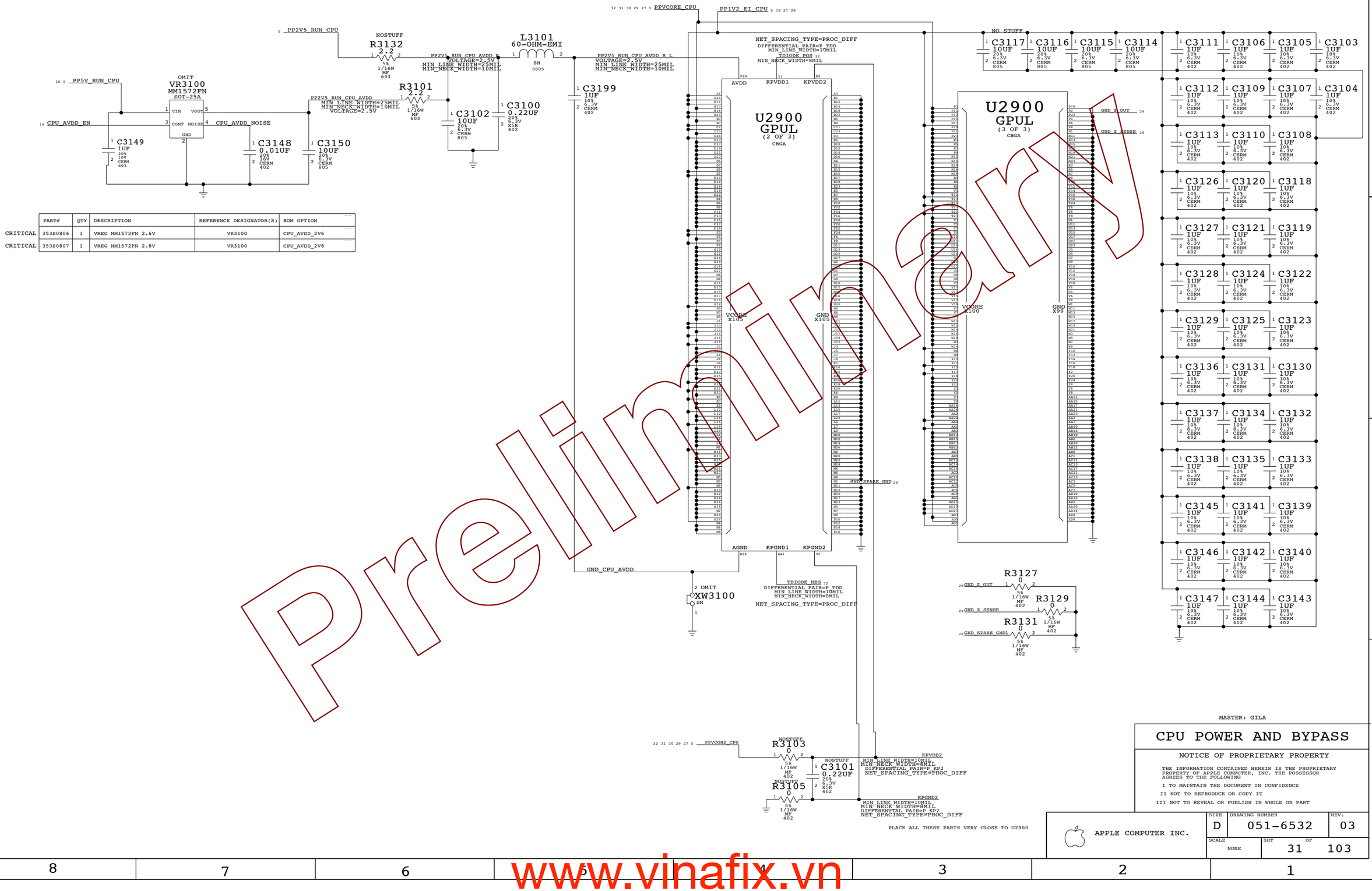
MASTER: GILA

CPU STRAPS

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03

SCALE	SHT	OF
NONE	30	103



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
CRITICAL 353S0806	1	VREG MM1572FN 2.6V	VR3100	CPU_AVDD_2V6
CRITICAL 353S0807	1	VREG MM1572FN 2.8V	VR3100	CPU_AVDD_2V8

MASTER: GILA

CPU POWER AND BYPASS

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 31 OF 103	

32 31 29 27 5 PPVCORE_CPU

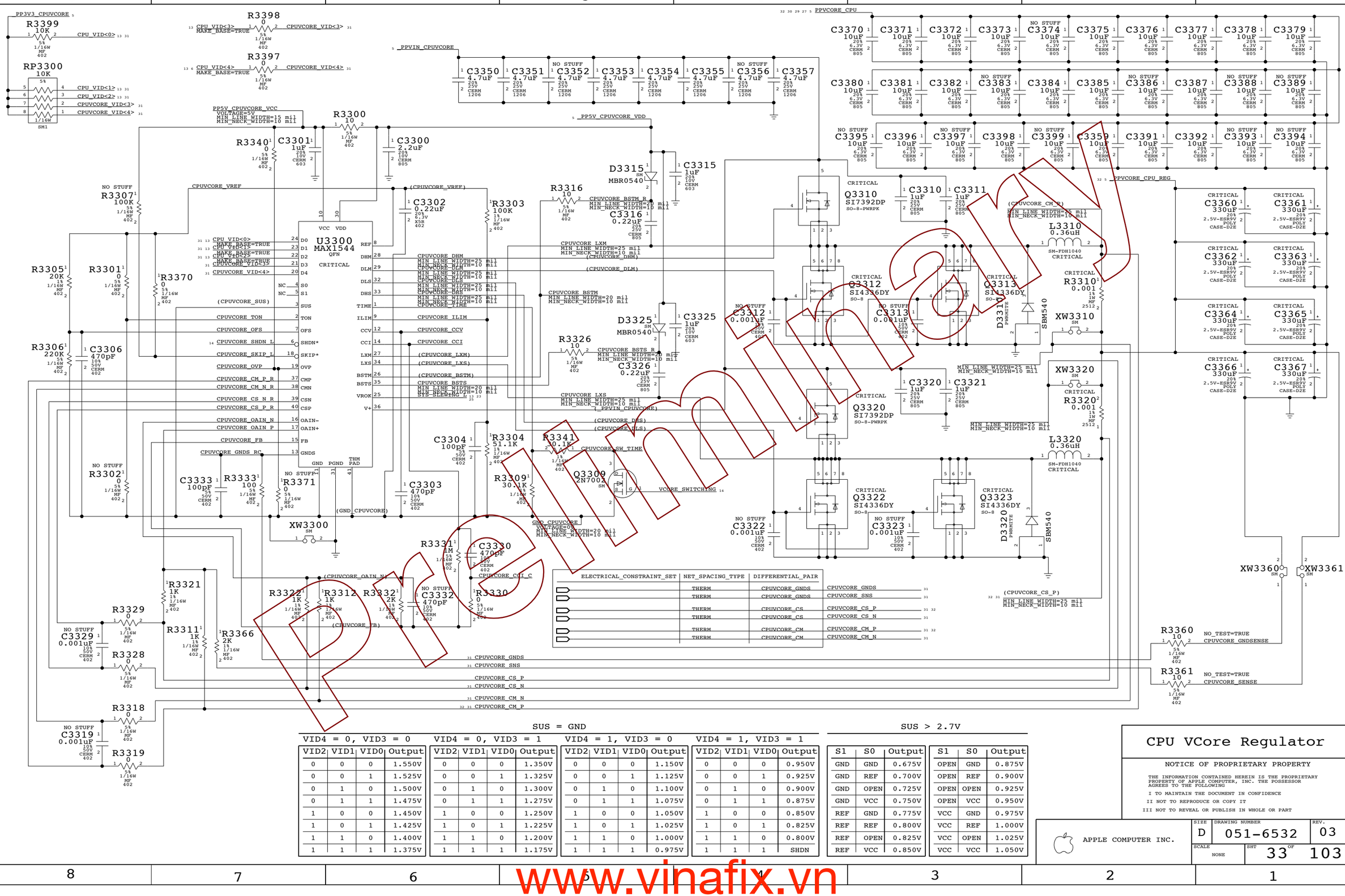
C3222 1UF 10% 6.3V CERM 402	C3221 1UF 10% 6.3V CERM 402	C3220 1UF 10% 6.3V CERM 402	C3219 1UF 10% 6.3V CERM 402	C3218 1UF 10% 6.3V CERM 402	C3217 1UF 10% 6.3V CERM 402	C3216 1UF 10% 6.3V CERM 402	C3215 1UF 10% 6.3V CERM 402	C3212 1UF 10% 6.3V CERM 402	C3200 1UF 10% 6.3V CERM 402
C3293 1UF 10% 6.3V CERM 402	C3268 1UF 10% 6.3V CERM 402	C3261 1UF 10% 6.3V CERM 402	C3259 1UF 10% 6.3V CERM 402	C3235 1UF 10% 6.3V CERM 402	C3232 1UF 10% 6.3V CERM 402	C3226 1UF 10% 6.3V CERM 402	C3224 1UF 10% 6.3V CERM 402	C3245 1UF 10% 6.3V CERM 402	C3223 1UF 10% 6.3V CERM 402
C3294 1UF 10% 6.3V CERM 402	C3269 1UF 10% 6.3V CERM 402	C3264 1UF 10% 6.3V CERM 402	C3260 1UF 10% 6.3V CERM 402	C3236 1UF 10% 6.3V CERM 402	C3233 1UF 10% 6.3V CERM 402	C3227 1UF 10% 6.3V CERM 402	C3225 1UF 10% 6.3V CERM 402	C3256 1UF 10% 6.3V CERM 402	C3234 1UF 10% 6.3V CERM 402
C3295 1UF 10% 6.3V CERM 402	C3271 1UF 10% 6.3V CERM 402	C3265 1UF 10% 6.3V CERM 402	C3262 1UF 10% 6.3V CERM 402	C3239 1UF 10% 6.3V CERM 402	C3237 1UF 10% 6.3V CERM 402	C3230 1UF 10% 6.3V CERM 402	C3228 1UF 10% 6.3V CERM 402	C3289 1UF 10% 6.3V CERM 402	C3267 1UF 10% 6.3V CERM 402
C3296 1UF 10% 6.3V CERM 402	C3270 1UF 10% 6.3V CERM 402	C3266 1UF 10% 6.3V CERM 402	C3263 1UF 10% 6.3V CERM 402	C3240 1UF 10% 6.3V CERM 402	C3238 1UF 10% 6.3V CERM 402	C3231 1UF 10% 6.3V CERM 402	C3229 1UF 10% 6.3V CERM 402	C3201 1UF 10% 6.3V CERM 402	C3278 1UF 10% 6.3V CERM 402
C3297 1UF 10% 6.3V CERM 402	C3282 1UF 10% 6.3V CERM 402	C3276 1UF 10% 6.3V CERM 402	C3272 1UF 10% 6.3V CERM 402	C3252 1UF 10% 6.3V CERM 402	C3250 1UF 10% 6.3V CERM 402	C3243 1UF 10% 6.3V CERM 402	C3241 1UF 10% 6.3V CERM 402	C3206 1UF 10% 6.3V CERM 402	C3204 1UF 10% 6.3V CERM 402
C3298 1UF 10% 6.3V CERM 402	C3281 1UF 10% 6.3V CERM 402	C3277 1UF 10% 6.3V CERM 402	C3273 1UF 10% 6.3V CERM 402	C3253 1UF 10% 6.3V CERM 402	C3251 1UF 10% 6.3V CERM 402	C3244 1UF 10% 6.3V CERM 402	C3242 1UF 10% 6.3V CERM 402	C3207 1UF 10% 6.3V CERM 402	C3205 1UF 10% 6.3V CERM 402
C3299 1UF 10% 6.3V CERM 402	C3284 1UF 10% 6.3V CERM 402	C3279 1UF 10% 6.3V CERM 402	C3274 1UF 10% 6.3V CERM 402	C3257 1UF 10% 6.3V CERM 402	C3254 1UF 10% 6.3V CERM 402	C3248 1UF 10% 6.3V CERM 402	C3246 1UF 10% 6.3V CERM 402	C3210 1UF 10% 6.3V CERM 402	C3208 1UF 10% 6.3V CERM 402
C3202 1UF 10% 6.3V CERM 402	C3283 1UF 10% 6.3V CERM 402	C3280 1UF 10% 6.3V CERM 402	C3275 1UF 10% 6.3V CERM 402	C3258 1UF 10% 6.3V CERM 402	C3255 1UF 10% 6.3V CERM 402	C3249 1UF 10% 6.3V CERM 402	C3247 1UF 10% 6.3V CERM 402	C3211 1UF 10% 6.3V CERM 402	C3209 1UF 10% 6.3V CERM 402
C3203 1UF 10% 6.3V CERM 402	C3292 1UF 10% 6.3V CERM 402	C3291 1UF 10% 6.3V CERM 402	C3290 1UF 10% 6.3V CERM 402	C3288 1UF 10% 6.3V CERM 402	C3287 1UF 10% 6.3V CERM 402	C3286 1UF 10% 6.3V CERM 402	C3285 1UF 10% 6.3V CERM 402	C3214 1UF 10% 6.3V CERM 402	C3213 1UF 10% 6.3V CERM 402

MASTER: GILA

PROC DECOUPLING

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 32 OF 103	


PP3V3_CPUVCORE
R3399 10K CPU_VID<0>
RP3300 10K SM1
CPU_VID<1>
CPU_VID<2>
CPUVCORE_VID<3>
CPUVCORE_VID<4>
R3398 0 MAKE_BASE=TRUE CPUVCORE_VID<3>
R3397 0 MAKE_BASE=TRUE CPUVCORE_VID<4>
PP5V_CPUVCORE_VCC VOLTAGE=5V MIN_LINE_WIDTH=15 mil MIN_NECK_WIDTH=10 mil
R3340 0
R3300 10
C3301 1uF
C3300 2.2uF
PP5V_CPUVCORE_VDD
PPVIN_CPUVCORE
C3350 4.7uF
C3351 4.7uF
C3352 4.7uF NO STUFF
C3353 4.7uF
C3354 4.7uF
C3355 4.7uF
C3356 4.7uF NO STUFF
C3357 4.7uF
PPVCORE_CPU
C3370 10uF
C3371 10uF
C3372 10uF
C3373 10uF
C3374 10uF NO STUFF
C3375 10uF
C3376 10uF
C3377 10uF
C3378 10uF
C3379 10uF
C3380 10uF
C3381 10uF
C3382 10uF
C3383 10uF NO STUFF
C3384 10uF
C3385 10uF
C3386 10uF NO STUFF
C3387 10uF
C3388 10uF NO STUFF
C3389 10uF
C3395 10uF NO STUFF
C3396 10uF
C3397 10uF NO STUFF
C3398 10uF
C3399 10uF NO STUFF
C3359 10uF
C3391 10uF
C3392 10uF
C3393 10uF NO STUFF
C3394 10uF NO STUFF
PPVCORE_CPU_REG
CPUVCORE_VREF
R3307 100K NO STUFF
R3305 20K
R3301 0
R3370 0
R3306 220K
C3306 470pF
U3300 MAX1544 QFN CRITICAL
D0 D1 D2 D3 D4 S0 S1 SUS TON OFS SHDN* SKIP* OVP CMP CMN CSN CSP OAIN- OAIN+ FB GNDS
REF DHM DLM DLS DHS TIME ILIM CCV CCI LXM LXS BSTM BSTS VROK V+ VCC VDD
R3316 10
D3315 MBR0540
C3315 1uF
C3316 0.22uF
R3303 100K
C3302 0.22uF
R3326 10
D3325 MBR0540
C3325 1uF
C3326 0.22uF
R3304 51.1K
C3304 100pF
R3341 30.1K
Q3309 2N7002
R3309 30.1K
C3303 470pF
R3302 0
C3333 100pF
R3333 100
R3371 0 NO STUFF
XW3300 SM
R3321 1K
R3322 1K
R3312 1K
R3332 2K
C3332 470pF NO STUFF
C3330 470pF
R3330 0
R3329 0
C3329 0.001uF NO STUFF
R3328 0
R3311 1K
R3366 2K
R3318 0
C3319 0.001uF NO STUFF
R3319 0
Q3310 SI7392DP CRITICAL
C3310 1uF
C3311 1uF
L3310 0.36uH
R3310 0.001
XW3310 SM
D3310 PWRMITE
SBM540
Q3312 SI4336DY CRITICAL
C3312 0.001uF NO STUFF
C3313 0.001uF NO STUFF
Q3313 SI4336DY CRITICAL
Q3320 SI7392DP CRITICAL
C3320 1uF
C3321 1uF
L3320 0.36uH
R3320 0.001
XW3320 SM
Q3322 SI4336DY CRITICAL
C3322 0.001uF NO STUFF
C3323 0.001uF NO STUFF
Q3323 SI4336DY CRITICAL
D3320 PWRMITE
SBM540
C3360 330uF CRITICAL
C3361 330uF CRITICAL
C3362 330uF CRITICAL
C3363 330uF CRITICAL
C3364 330uF CRITICAL
C3365 330uF CRITICAL
C3366 330uF CRITICAL
C3367 330uF CRITICAL
XW3360 SM
XW3361 SM
R3360 10 NO_TEST=TRUE CPUVCORE_GNDSENSE
R3361 10 NO_TEST=TRUE CPUVCORE_SENSE
ELECTRICAL_CONSTRAINT_SET | NET_SPACING_TYPE | DIFFERENTIAL_PAIR
THERM CPUVCORE_GNDS CPUVCORE_GNDS
THERM CPUVCORE_GNDS CPUVCORE_SNS
THERM CPUVCORE_CS CPUVCORE_CS_P
THERM CPUVCORE_CS CPUVCORE_CS_N
THERM CPUVCORE_CM CPUVCORE_CM_P
THERM CPUVCORE_CM CPUVCORE_CM_N
SUS = GND
VID4 = 0, VID3 = 0
VID2 VID1 VID0 Output
0 0 0 1.550V
0 0 1 1.525V
0 1 0 1.500V
0 1 1 1.475V
1 0 0 1.450V
1 0 1 1.425V
1 1 0 1.400V
1 1 1 1.375V
VID4 = 0, VID3 = 1
VID2 VID1 VID0 Output
0 0 0 1.350V
0 0 1 1.325V
0 1 0 1.300V
0 1 1 1.275V
1 0 0 1.250V
1 0 1 1.225V
1 1 0 1.200V
1 1 1 1.175V
VID4 = 1, VID3 = 0
VID2 VID1 VID0 Output
0 0 0 1.150V
0 0 1 1.125V
0 1 0 1.100V
0 1 1 1.075V
1 0 0 1.050V
1 0 1 1.025V
1 1 0 1.000V
1 1 1 0.975V
VID4 = 1, VID3 = 1
VID2 VID1 VID0 Output
0 0 0 0.950V
0 0 1 0.925V
0 1 0 0.900V
0 1 1 0.875V
1 0 0 0.850V
1 0 1 0.825V
1 1 0 0.800V
1 1 1 SHDN
SUS > 2.7V
S1 S0 Output
GND GND 0.675V
GND REF 0.700V
GND OPEN 0.725V
GND VCC 0.750V
REF GND 0.775V
REF REF 0.800V
REF OPEN 0.825V
REF VCC 0.850V
S1 S0 Output
OPEN GND 0.875V
OPEN REF 0.900V
OPEN OPEN 0.925V
OPEN VCC 0.950V
VCC GND 0.975V
VCC REF 1.000V
VCC OPEN 1.025V
VCC VCC 1.050V
CPU VCore Regulator
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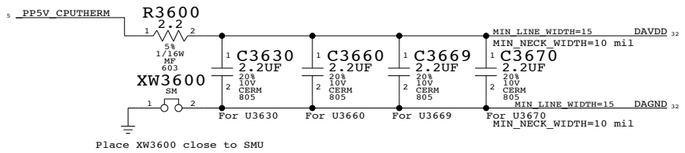
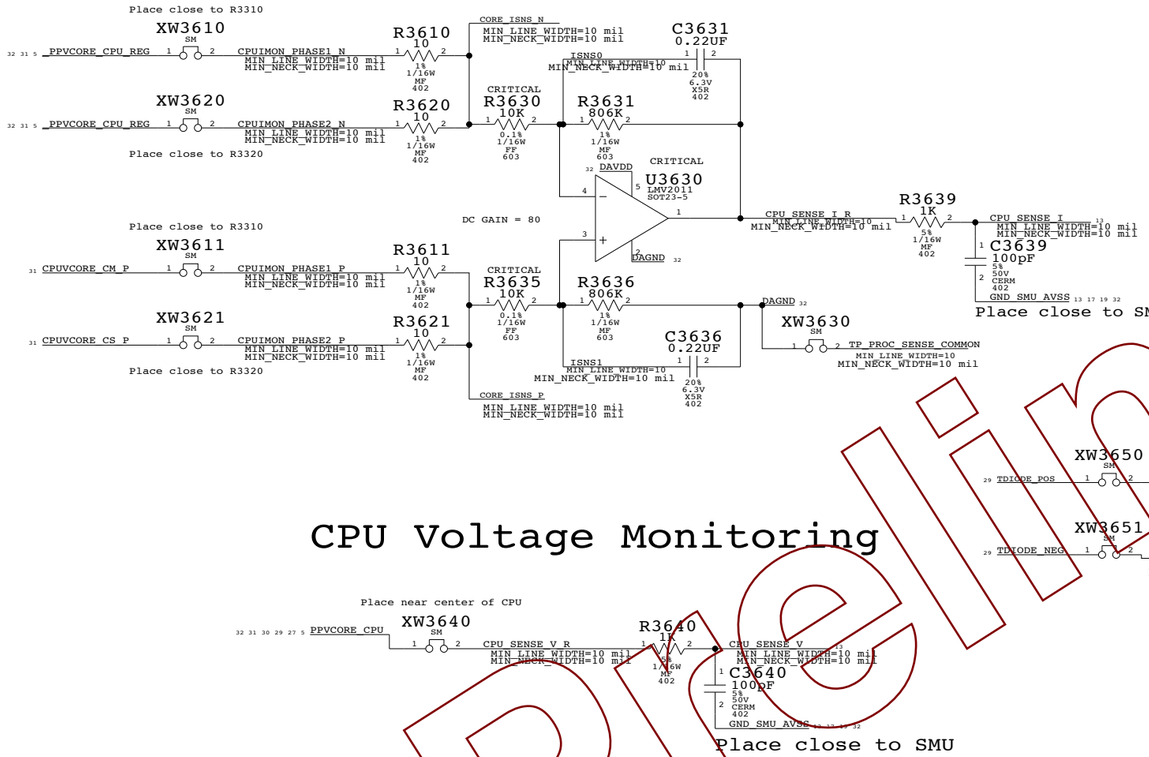


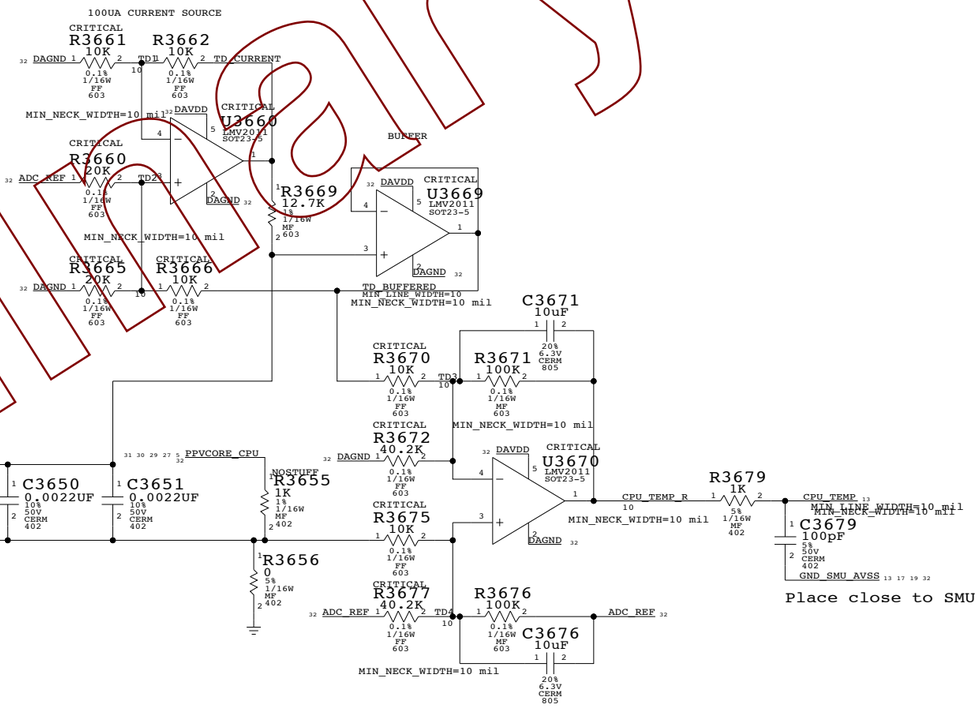
CPU Current Monitoring

Place close to CPU Power Supply



CPU Thermal Diode Circuit

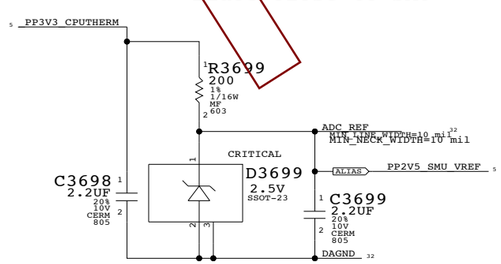
Place close to CPU



CPU Voltage Monitoring

SMU Voltage Reference

Place close to SMU



CPU Temp Monitoring

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 36 OF 103	

U3TWINS DO NOT HAVE MASKS

PP2V5_PWRON_RAM

U3 U3LITE V1.0-300MM PBGA (SYM 2 OF 7) OMIT

MEMORY DATA INTERFACE

PP1V5_PWRON_NB_AVDD

R3702 2.2 5% 1/16W MF 603

PP1V5_PWRON_RAM_NB_AVDD VOLTAGE=1.5V

C3745 1UF 10% 4V CERM 402

C3744 0.1UF 20% 10V CERM 402

MIN_LINE_WIDTH=25MIL MIN_NECK_WIDTH=10MIL

DDR CLK_AVDD

U3 U3LITE V1.0-300MM PBGA (SYM 3 OF 7) OMIT

MEMORY CONTROL INTERFACE

DDR_CLK_AVSS

PP1V25_PWRON_RAM_VREF_NB VOLTAGE=1.25V

R3700 1K 1% 1/16W MF 402

R3701 1K 1% 1/16W MF 402

C3730 0.1UF 20% 10V CERM 402

C3746 0.1UF 20% 10V CERM 402

C3747 0.1UF 20% 10V CERM 402

C3748 0.1UF 20% 10V CERM 402

MIN_LINE_WIDTH=25MIL MIN_NECK_WIDTH=10MIL

C3700 C3701 C3702 C3703 C3704 C3705 C3706 C3707 C3708 C3709 C3710 C3711 C3712 C3713 C3714 C3731 C3732 C3733 C3734 C3735 C3736 C3737 0.1UF 20% 10V CERM 402

C3715 C3716 C3717 C3718 C3719 C3720 C3721 C3722 C3724 C3725 C3726 C3727 C3728 C3729 C3743 C3742 C3740 C3739 C3738 0.1UF 20% 10V CERM 402

MASTER: GILA

U3LITE MEMORY

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SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 37 OF 103	

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

NOTE: SO-DIMMs only use 2 of the 3 clocks provided for each DIMM module. Unused clocks renamed below.

33 RAM_CLK_C_P_R — ALIAS — TP_RAM_CLK_C_P MAKE_BASE=TRUE
33 RAM_CLK_C_N_R — ALIAS — TP_RAM_CLK_C_N MAKE_BASE=TRUE
33 RAM_CLK_F_P_R — ALIAS — TP_RAM_CLK_F_P MAKE_BASE=TRUE
33 RAM_CLK_F_N_R — ALIAS — TP_RAM_CLK_F_N MAKE_BASE=TRUE

Series Termination for Clock/Control Signals

The number in reference designator (RP38x0) is the same.

CLOCKS

RP3800 22 5% 1/16W SM1: 62 33 RAM_CLK_A_P_R — 1 — 8 — RAM_CLK_A_P 35 62
RP3800 22 5% 1/16W SM1: 62 33 RAM_CLK_A_N_R — 2 — 7 — RAM_CLK_A_N 35 62
RP3800 22 5% 1/16W SM1: 62 33 RAM_CLK_B_P_R — 4 — 5 — RAM_CLK_B_P 35 62
RP3800 22 5% 1/16W SM1: 62 33 RAM_CLK_B_N_R — 3 — 6 — RAM_CLK_B_N 35 62
RP3801 22 5% 1/16W SM1: 62 33 RAM_CLK_D_P_R — 3 — 6 — RAM_CLK_D_P 35 62
RP3801 22 5% 1/16W SM1: 62 33 RAM_CLK_D_N_R — 4 — 5 — RAM_CLK_D_N 35 62
RP3801 22 5% 1/16W SM1: 62 33 RAM_CLK_E_P_R — 1 — 8 — RAM_CLK_E_P 35 62
RP3801 22 5% 1/16W SM1: 62 33 RAM_CLK_E_N_R — 2 — 7 — RAM_CLK_E_N 35 62

CKE pulldowns to put RAM into self refresh during sleep

RP3850 10K 5% 1/16W SM1: 62 35 34 RAM_CKE<0>
RP3850 10K 5% 1/16W SM1: 62 35 34 RAM_CKE<1>
RP3850 10K 5% 1/16W SM1: 62 35 34 RAM_CKE<4>
RP3850 10K 5% 1/16W SM1: 62 35 34 RAM_CKE<5>

CS

RP3810 22 5% 1/16W SM1: 62 33 RAM_CS_L_R<0> — 2 — 7 — RAM_CS_L<0> 35 62
RP3810 22 5% 1/16W SM1: 62 33 RAM_CS_L_R<1> — 3 — 6 — RAM_CS_L<1> 35 62
RP3810 22 5% 1/16W SM1: 62 33 RAM_CS_L_R<8> — 1 — 8 — RAM_CS_L<8> 35 62
RP3810 22 5% 1/16W SM1: 62 33 RAM_CS_L_R<9> — 4 — 5 — RAM_CS_L<9> 35 62

CKE

RP3820 22 5% 1/16W SM1: 62 33 RAM_CKE_R<0> — 4 — 5 — RAM_CKE<0> 34 35 62
RP3820 22 5% 1/16W SM1: 62 33 RAM_CKE_R<1> — 3 — 6 — RAM_CKE<1> 34 35 62
RP3820 22 5% 1/16W SM1: 62 33 RAM_CKE_R<4> — 1 — 8 — RAM_CKE<4> 34 35 62
RP3820 22 5% 1/16W SM1: 62 33 RAM_CKE_R<5> — 2 — 7 — RAM_CKE<5> 34 35 62

ADDR

RP3830 22 5% 1/16W SM1: 62 33 RAM_A_R<0> — 2 — 7 — RAM_A<0> 35 62
RP3830 22 5% 1/16W SM1: 62 33 RAM_A_R<1> — 4 — 5 — RAM_A<1> 35 62
RP3830 22 5% 1/16W SM1: 62 33 RAM_A_R<2> — 1 — 8 — RAM_A<2> 35 62
RP3830 22 5% 1/16W SM1: 62 33 RAM_A_R<3> — 3 — 6 — RAM_A<3> 35 62
RP3831 22 5% 1/16W SM1: 62 33 RAM_A_R<4> — 2 — 7 — RAM_A<4> 35 62
RP3831 22 5% 1/16W SM1: 62 33 RAM_A_R<5> — 3 — 6 — RAM_A<5> 35 62
RP3831 22 5% 1/16W SM1: 62 33 RAM_A_R<6> — 1 — 8 — RAM_A<6> 35 62
RP3831 22 5% 1/16W SM1: 62 33 RAM_A_R<7> — 4 — 5 — RAM_A<7> 35 62
RP3832 22 5% 1/16W SM1: 62 33 RAM_A_R<8> — 3 — 6 — RAM_A<8> 35 62
RP3832 22 5% 1/16W SM1: 62 33 RAM_A_R<9> — 1 — 8 — RAM_A<9> 35 62
RP3832 22 5% 1/16W SM1: 62 33 RAM_A_R<10> — 4 — 5 — RAM_A<10> 35 62
RP3832 22 5% 1/16W SM1: 62 33 RAM_A_R<11> — 2 — 7 — RAM_A<11> 35 62
RP3833 22 5% 1/16W SM1: 62 33 RAM_A_R<12> — 4 — 5 — RAM_A<12> 35 62
RP3833 22 5% 1/16W SM1: 62 33 RAM_A_R<13> — 3 — 6 — RAM_A<13> 35 62

BA

RP3833 22 5% 1/16W SM1: 62 33 RAM_BA_R<0> — 1 — 8 — RAM_BA<0> 35
RP3833 22 5% 1/16W SM1: 62 33 RAM_BA_R<1> — 2 — 5 — RAM_BA<1> 35

CNTL

R3840 22 5% 1/16W MF 402: 62 33 RAM_WE_L_R — 1 — 2 — RAM_WE_L 35
R3841 22 5% 1/16W MF 402: 62 33 RAM_CAS_L_R — 1 — 2 — RAM_CAS_L 35
R3842 22 5% 1/16W MF 402: 62 33 RAM_RAS_L_R — 1 — 2 — RAM_RAS_L 35

No series termination on data signals

DIMM "A"

62 33 RAM_DQ_R<0> — ALIAS — RAM_DQ<0> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<1> — ALIAS — RAM_DQ<1> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<2> — ALIAS — RAM_DQ<2> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<3> — ALIAS — RAM_DQ<3> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<4> — ALIAS — RAM_DQ<4> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<5> — ALIAS — RAM_DQ<5> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<6> — ALIAS — RAM_DQ<6> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<7> — ALIAS — RAM_DQ<7> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<8> — ALIAS — RAM_DQ<8> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<9> — ALIAS — RAM_DQ<9> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<10> — ALIAS — RAM_DQ<10> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<11> — ALIAS — RAM_DQ<11> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<12> — ALIAS — RAM_DQ<12> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<13> — ALIAS — RAM_DQ<13> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<14> — ALIAS — RAM_DQ<14> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<15> — ALIAS — RAM_DQ<15> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<16> — ALIAS — RAM_DQ<16> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<17> — ALIAS — RAM_DQ<17> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<18> — ALIAS — RAM_DQ<18> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<19> — ALIAS — RAM_DQ<19> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<20> — ALIAS — RAM_DQ<20> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<21> — ALIAS — RAM_DQ<21> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<22> — ALIAS — RAM_DQ<22> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<23> — ALIAS — RAM_DQ<23> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<24> — ALIAS — RAM_DQ<24> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<25> — ALIAS — RAM_DQ<25> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<26> — ALIAS — RAM_DQ<26> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<27> — ALIAS — RAM_DQ<27> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<28> — ALIAS — RAM_DQ<28> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<29> — ALIAS — RAM_DQ<29> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<30> — ALIAS — RAM_DQ<30> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<31> — ALIAS — RAM_DQ<31> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<32> — ALIAS — RAM_DQ<32> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<33> — ALIAS — RAM_DQ<33> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<34> — ALIAS — RAM_DQ<34> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<35> — ALIAS — RAM_DQ<35> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<36> — ALIAS — RAM_DQ<36> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<37> — ALIAS — RAM_DQ<37> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<38> — ALIAS — RAM_DQ<38> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<39> — ALIAS — RAM_DQ<39> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<40> — ALIAS — RAM_DQ<40> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<41> — ALIAS — RAM_DQ<41> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<42> — ALIAS — RAM_DQ<42> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<43> — ALIAS — RAM_DQ<43> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<44> — ALIAS — RAM_DQ<44> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<45> — ALIAS — RAM_DQ<45> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<46> — ALIAS — RAM_DQ<46> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<47> — ALIAS — RAM_DQ<47> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<48> — ALIAS — RAM_DQ<48> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<49> — ALIAS — RAM_DQ<49> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<50> — ALIAS — RAM_DQ<50> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<51> — ALIAS — RAM_DQ<51> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<52> — ALIAS — RAM_DQ<52> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<53> — ALIAS — RAM_DQ<53> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<54> — ALIAS — RAM_DQ<54> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<55> — ALIAS — RAM_DQ<55> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<56> — ALIAS — RAM_DQ<56> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<57> — ALIAS — RAM_DQ<57> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<58> — ALIAS — RAM_DQ<58> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<59> — ALIAS — RAM_DQ<59> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<60> — ALIAS — RAM_DQ<60> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<61> — ALIAS — RAM_DQ<61> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<62> — ALIAS — RAM_DQ<62> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<63> — ALIAS — RAM_DQ<63> MAKE_BASE=TRUE 35 62

DIMM "B"

62 33 RAM_DQ_R<64> — ALIAS — RAM_DQ<64> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<65> — ALIAS — RAM_DQ<65> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<66> — ALIAS — RAM_DQ<66> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<67> — ALIAS — RAM_DQ<67> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<68> — ALIAS — RAM_DQ<68> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<69> — ALIAS — RAM_DQ<69> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<70> — ALIAS — RAM_DQ<70> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<71> — ALIAS — RAM_DQ<71> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<72> — ALIAS — RAM_DQ<72> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<73> — ALIAS — RAM_DQ<73> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<74> — ALIAS — RAM_DQ<74> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<75> — ALIAS — RAM_DQ<75> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<76> — ALIAS — RAM_DQ<76> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<77> — ALIAS — RAM_DQ<77> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<78> — ALIAS — RAM_DQ<78> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<79> — ALIAS — RAM_DQ<79> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<80> — ALIAS — RAM_DQ<80> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<81> — ALIAS — RAM_DQ<81> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<82> — ALIAS — RAM_DQ<82> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<83> — ALIAS — RAM_DQ<83> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<84> — ALIAS — RAM_DQ<84> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<85> — ALIAS — RAM_DQ<85> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<86> — ALIAS — RAM_DQ<86> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<87> — ALIAS — RAM_DQ<87> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<88> — ALIAS — RAM_DQ<88> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<89> — ALIAS — RAM_DQ<89> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<90> — ALIAS — RAM_DQ<90> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<91> — ALIAS — RAM_DQ<91> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<92> — ALIAS — RAM_DQ<92> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<93> — ALIAS — RAM_DQ<93> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<94> — ALIAS — RAM_DQ<94> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<95> — ALIAS — RAM_DQ<95> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<96> — ALIAS — RAM_DQ<96> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<97> — ALIAS — RAM_DQ<97> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<98> — ALIAS — RAM_DQ<98> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<99> — ALIAS — RAM_DQ<99> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<100> — ALIAS — RAM_DQ<100> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<101> — ALIAS — RAM_DQ<101> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<102> — ALIAS — RAM_DQ<102> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<103> — ALIAS — RAM_DQ<103> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<104> — ALIAS — RAM_DQ<104> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<105> — ALIAS — RAM_DQ<105> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<106> — ALIAS — RAM_DQ<106> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<107> — ALIAS — RAM_DQ<107> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<108> — ALIAS — RAM_DQ<108> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<109> — ALIAS — RAM_DQ<109> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<110> — ALIAS — RAM_DQ<110> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<111> — ALIAS — RAM_DQ<111> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<112> — ALIAS — RAM_DQ<112> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<113> — ALIAS — RAM_DQ<113> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<114> — ALIAS — RAM_DQ<114> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<115> — ALIAS — RAM_DQ<115> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<116> — ALIAS — RAM_DQ<116> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<117> — ALIAS — RAM_DQ<117> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<118> — ALIAS — RAM_DQ<118> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<119> — ALIAS — RAM_DQ<119> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<120> — ALIAS — RAM_DQ<120> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<121> — ALIAS — RAM_DQ<121> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<122> — ALIAS — RAM_DQ<122> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<123> — ALIAS — RAM_DQ<123> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<124> — ALIAS — RAM_DQ<124> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<125> — ALIAS — RAM_DQ<125> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<126> — ALIAS — RAM_DQ<126> MAKE_BASE=TRUE 35 62
62 33 RAM_DQ_R<127> — ALIAS — RAM_DQ<127> MAKE_BASE=TRUE 35 62

No series termination on strobe signals

62 33 RAM_DQS_R<0> — ALIAS — RAM_DQS<0> MAKE_BASE=TRUE 35 62
62 33 RAM_DQS_R<1> — ALIAS — RAM_DQS<1> MAKE_BASE=TRUE 35 62
62 33 RAM_DQS_R<2> — ALIAS — RAM_DQS<2> MAKE_BASE=TRUE 35 62
62 33 RAM_DQS_R<3> — ALIAS — RAM_DQS<3> MAKE_BASE=TRUE 35 62
62 33 RAM_DQS_R<4> — ALIAS — RAM_DQS<4> MAKE_BASE=TRUE 35 62
62 33 RAM_DQS_R<5> — ALIAS — RAM_DQS<5> MAKE_BASE=TRUE 35 62
62 33 RAM_DQS_R<6> — ALIAS — RAM_DQS<6> MAKE_BASE=TRUE 35 62
62 33 RAM_DQS_R<7> — ALIAS — RAM_DQS<7> MAKE_BASE=TRUE 35 62
62 33 RAM_DQS_R<8> — ALIAS — RAM_DQS<8> MAKE_BASE=TRUE 35 62
62 33 RAM_DQS_R<9> — ALIAS — RAM_DQS<9> MAKE_BASE=TRUE 35 62
62 33 RAM_DQS_R<10> — ALIAS — RAM_DQS<10> MAKE_BASE=TRUE 35 62
62 33 RAM_DQS_R<11> — ALIAS — RAM_DQS<11> MAKE_BASE=TRUE 35 62
62 33 RAM_DQS_R<12> — ALIAS — RAM_DQS<12> MAKE_BASE=TRUE 35 62
62 33 RAM_DQS_R<13> — ALIAS — RAM_DQS<13> MAKE_BASE=TRUE 35 62
62 33 RAM_DQS_R<14> — ALIAS — RAM_DQS<14> MAKE_BASE=TRUE 35 62
62 33 RAM_DQS_R<15> — ALIAS — RAM_DQS<15> MAKE_BASE=TRUE 35 62

Memory Series Term

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03

SCALE	SHT	OF
NONE	38	103

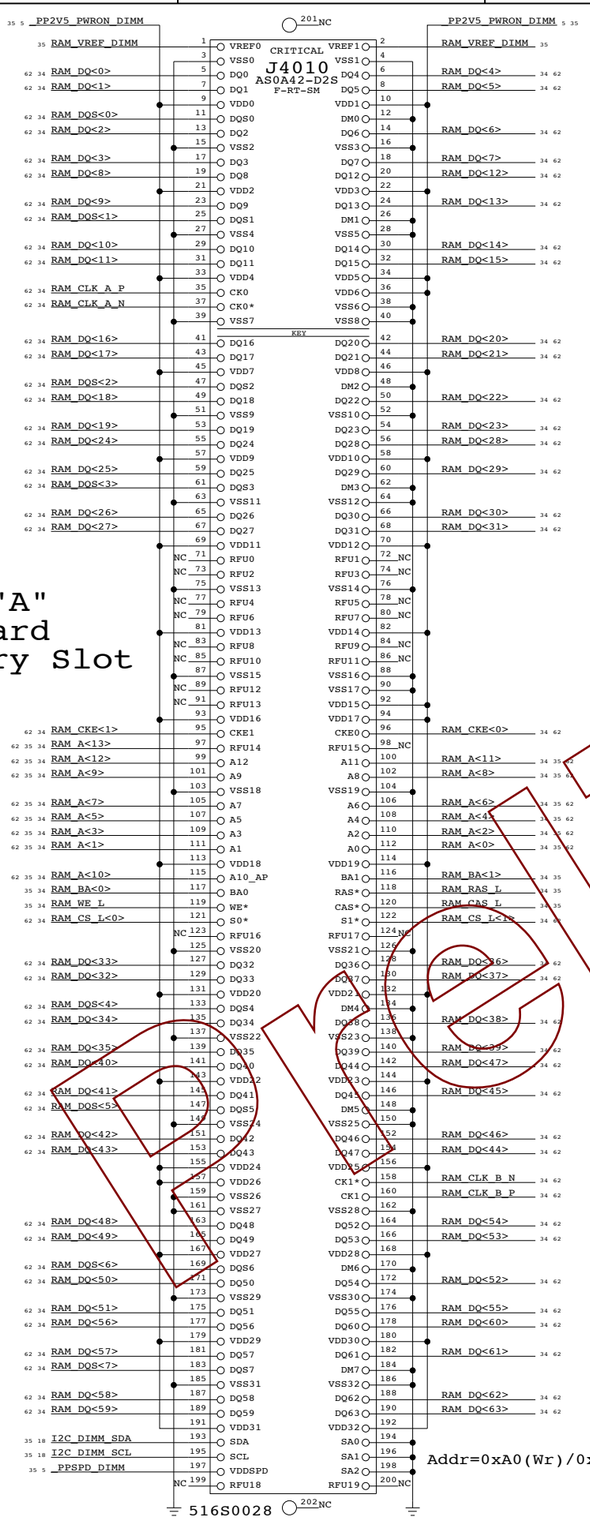
Page Notes

Power aliases required by this page:
- _PP2V5_PWRON_DIMM
- _PPSPD_DIMM (2.5V - 3.3V)

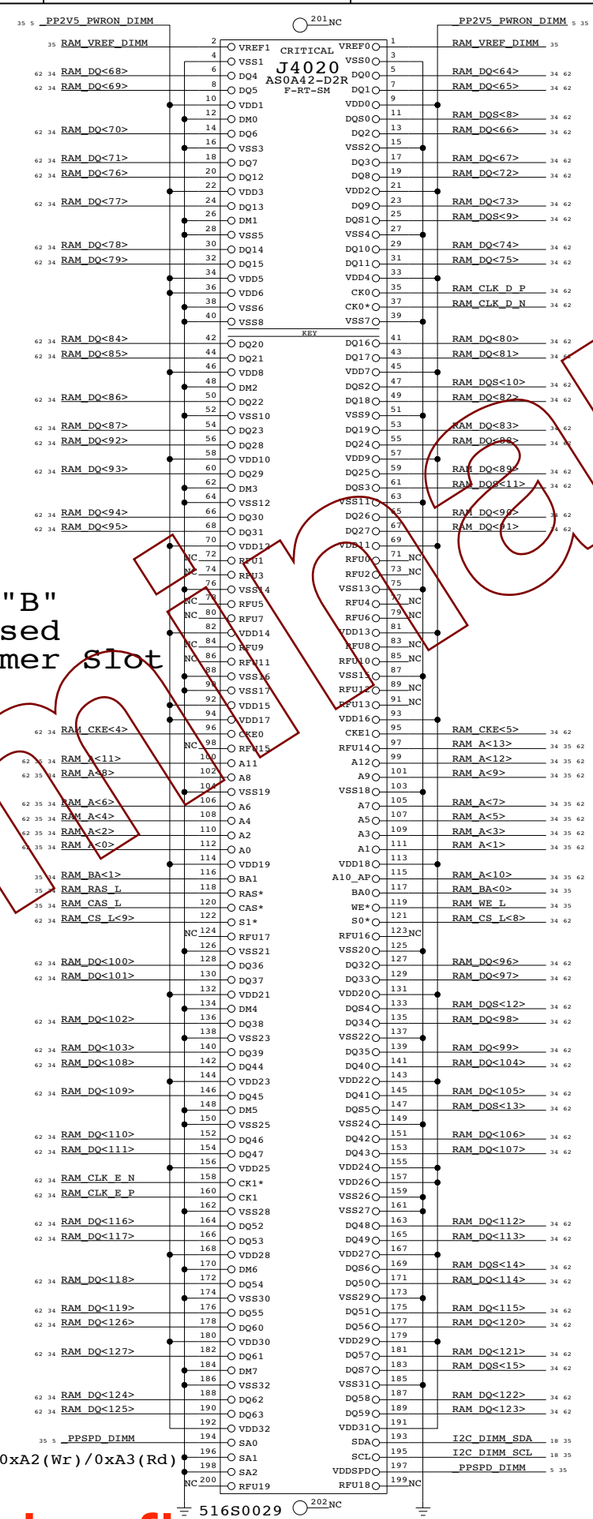
Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Slot "A" Standard Factory Slot

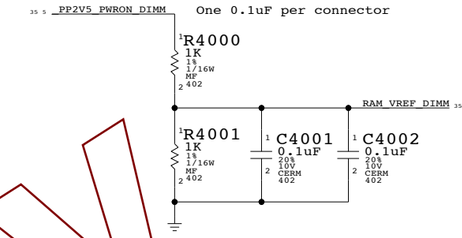


Slot "B" Reversed Customer Slot



DDR VRef

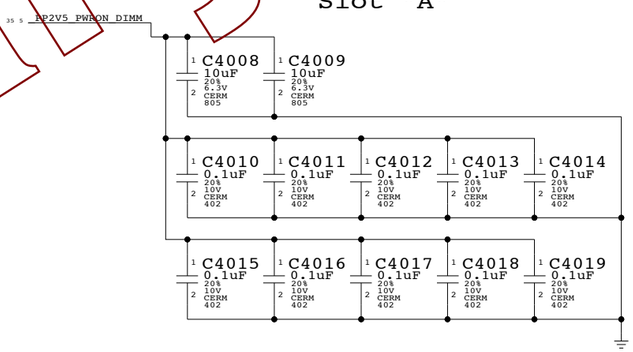
One 0.1uF per connector



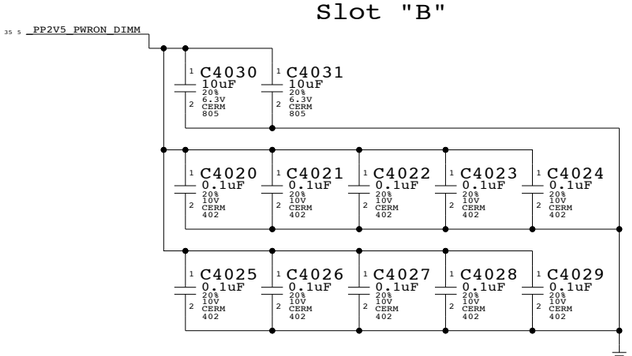
DDR Bypass Caps

(For return current)

Slot "A"



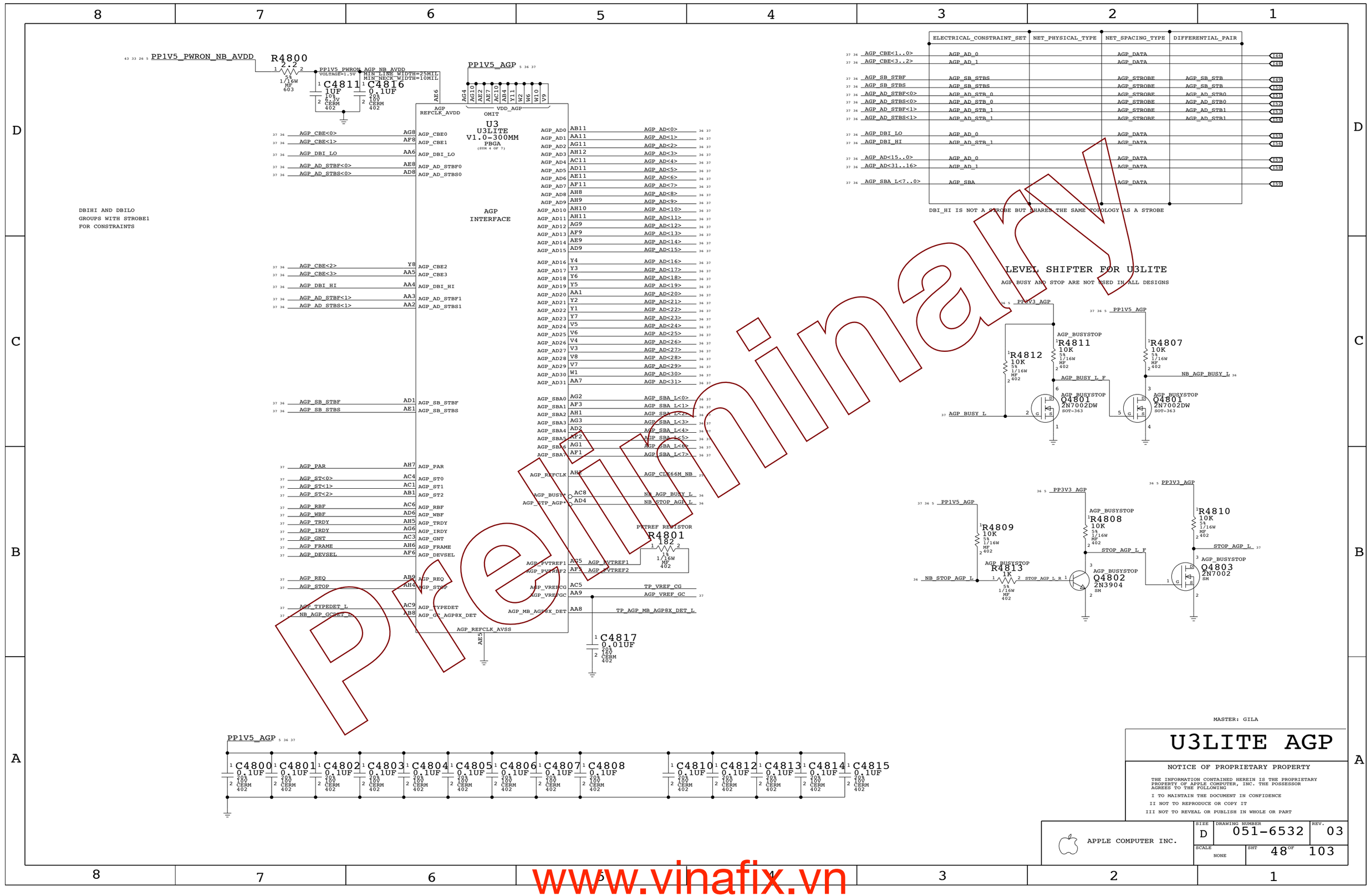
Slot "B"



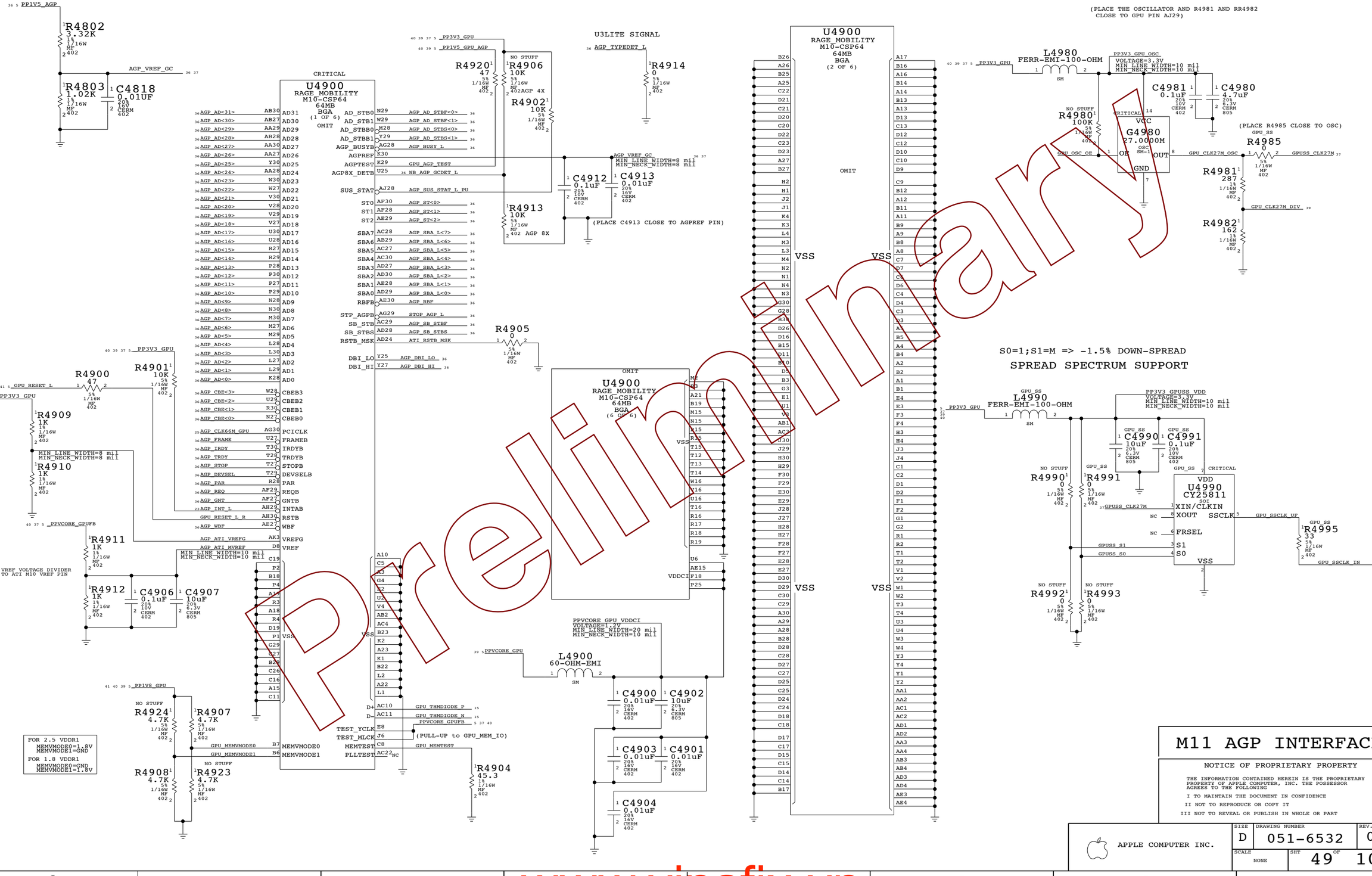
DDR SODIMM CONNS

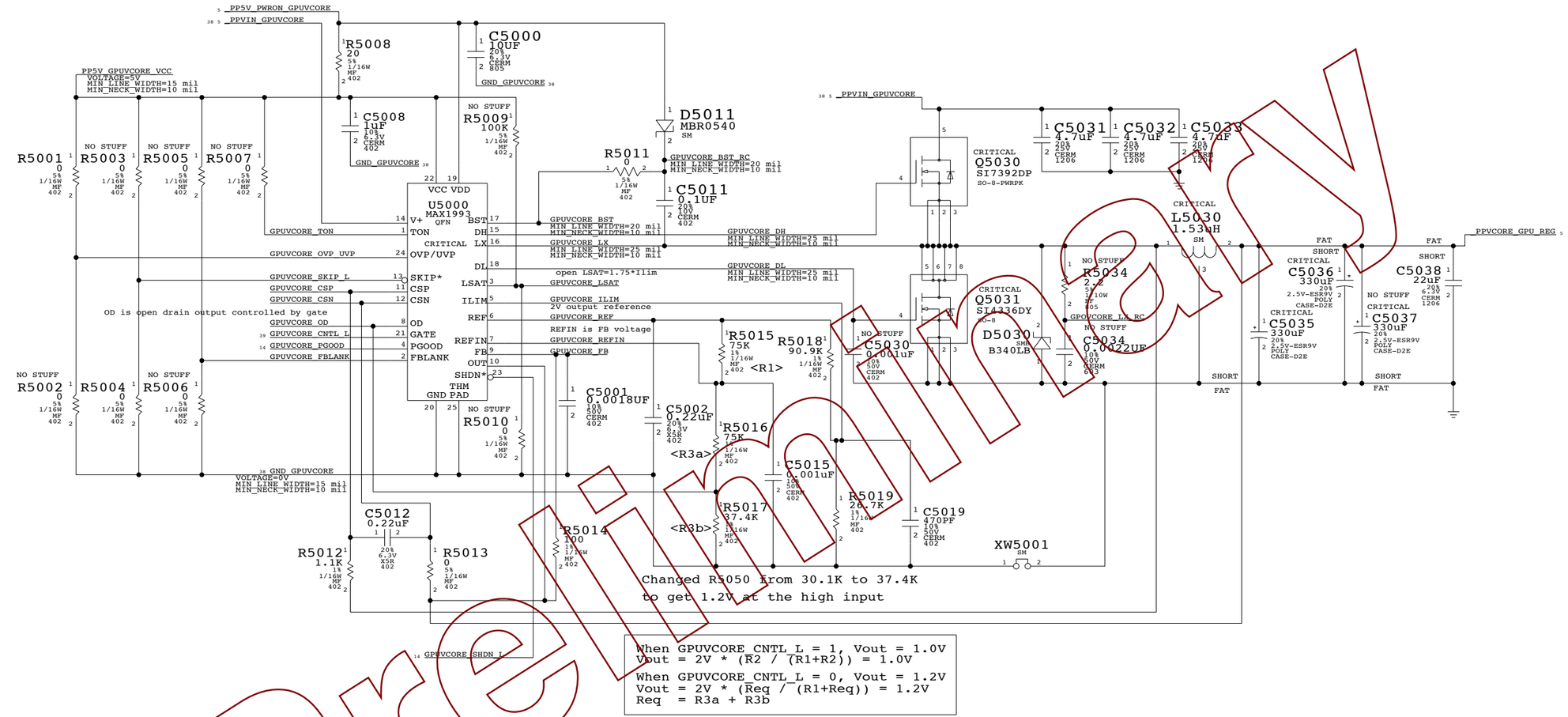
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 40 OF 103	



U3LITE AGP I/O REFERENCE
(PLACE CLOSE TO GPU AGP BALL)





GPU VCore Regulator

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03

SCALE: NONE

SHT 50 OF 103

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR		
	LVDS	LVDS_L0	LVDS_L0P	6 39 42
	LVDS	LVDS_L0	LVDS_L0N	6 39 42
	LVDS	LVDS_L1	LVDS_L1P	6 39 42
	LVDS	LVDS_L1	LVDS_L1N	6 39 42
	LVDS	LVDS_L2	LVDS_L2P	6 39 42
	LVDS	LVDS_L2	LVDS_L2N	6 39 42
	LVDS	LVDS_LCLK	CLKLVDS_LP	6 39 42
	LVDS	LVDS_LCLK	CLKLVDS_LN	6 39 42
	LVDS	LVDS_U0	LVDS_U0P	6 39 42
	LVDS	LVDS_U0	LVDS_U0N	6 39 42
	LVDS	LVDS_U1	LVDS_U1P	6 39 42
	LVDS	LVDS_U1	LVDS_U1N	6 39 42
	LVDS	LVDS_U2	LVDS_U2P	6 39 42
	LVDS	LVDS_U2	LVDS_U2N	6 39 42
	LVDS	LVDS_UCLK	CLKLVDS_UP	6 39 42
	LVDS	LVDS_UCLK	CLKLVDS_UN	6 39 42
GPU_DVO_DATA	8 MIL SPACING		GPU_DVOD<0..19>	39 41
GPU_DVO_DATA20	8 MIL SPACING		GPU_DVOD<20>	39 41
GPU_DVO_DATA	8 MIL SPACING		GPU_DVOD<21..23>	39 41
GPU_DVO_DATA	8 MIL SPACING		GPU_DVO_HSYNC	39 41
GPU_DVO_CTL	8 MIL SPACING		GPU_DVO_VSYNC	39 41
GPU_DVO_CTL	8 MIL SPACING		GPU_DVO_DE	39 41
GPU_DVO_CTL	8 MIL SPACING		GPU_DVO_CLKP	39 41

Page Notes

Power aliases required by this page:
_PP1V5_GPU_AGP, _PP3V3_GPU, PPVCORE_GPU

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Net Spacing Type: LVDS

Line To Line:	15 mils
Length Tolerance:	50 mils
Primary Max Sep:	10 mils
Secondary Max Sep:	100 mils
Secondary Length:	250 mils

NOTE: Target differential impedance for LVDS data pairs is 100 ohms.

40 39 37 5 _PP1V5_GPU_AGP

CRITICAL
Q5100
SI3446DV
TSOP

GPUVDD15_EN 14

PP1V5_GPU_VDD15_UF
VOLTAGE=1.5V
MIN_LINE_WIDTH=25mil
MIN_NECK_WIDTH=10mil

L5126
FERR-220-OHM
0805

39 _PP1V5_GPU_VDD15
VOLTAGE=1.5V
MIN_LINE_WIDTH=25mil
MIN_NECK_WIDTH=10mil

(500mA)

C5133 0.001uF 10% 50V CERM 402

C5127 0.01uF 20% 16V CERM 402
C5126 0.01uF 20% 16V CERM 402
C5132 0.01uF 20% 16V CERM 402
C5124 0.01uF 20% 16V CERM 402
C5125 10uF 20% 6.3V CERM 805

C5131 0.01uF 20% 16V CERM 402
C5130 0.01uF 20% 16V CERM 402
C5129 0.01uF 20% 16V CERM 402
C5128 0.01uF 20% 16V CERM 402

GPU VCORE - 1.2V

(PUT ALL CAPs BELOW ATI ASIC)

39 37 5 PPVCORE_GPU

C5100 10uF 20% 6.3V CERM 805
C5101 10uF 20% 6.3V CERM 805
C5120 0.22uF 20% 6.3V X5R 402
C5102 0.22uF 20% 6.3V X5R 402
C5103 0.22uF 20% 6.3V X5R 402
C5104 0.22uF 20% 6.3V X5R 402
C5105 0.22uF 20% 6.3V X5R 402
C5106 0.22uF 20% 6.3V X5R 402

C5107 0.22uF 20% 6.3V X5R 402
C5108 0.22uF 20% 6.3V X5R 402
C5109 0.22uF 20% 6.3V X5R 402
C5110 0.22uF 20% 6.3V X5R 402
C5111 0.22uF 20% 6.3V X5R 402
C5112 0.22uF 20% 6.3V X5R 402
C5113 0.22uF 20% 6.3V X5R 402
C5114 0.22uF 20% 6.3V X5R 402

C5115 0.22uF 20% 6.3V X5R 402
C5116 0.22uF 20% 6.3V X5R 402
C5117 0.22uF 20% 6.3V X5R 402
C5118 0.22uF 20% 6.3V X5R 402
C5119 0.22uF 20% 6.3V X5R 402
C5123 0.22uF 20% 6.3V X5R 402
C5121 0.22uF 20% 6.3V X5R 402
C5122 0.22uF 20% 6.3V X5R 402

U4900
RAGE_MOBILITY
M10-CSP64
64MB
BGA
(5 OF 6)

F12 L6 T6 AB6 F17 G25 R25 AB25 — VDD15
AJ3 AF25 AG4 AH4 AF5 F6 G6 H6 P6 AD26 V6 W6 AC6 AD6 AE6 F7 F10 AE10 F11 AE11 F13 F14 AE14 AF14 W26 AF15 AE17 AC25 AE18 F23 F24 AE24 P25 M25 N25 W25 V25 — VDDC
G7 G8 G9 G10 G11 G12 G13 G14 G15 G16 G17 G18 G19 G20 G21 G22 G23 G24 H7 H8 H23 H24 J7 J24 K7 K24 L7 L24 M7 M24 N7 N24 P7 P24 R7 R24 T7 T24 U7 U24 V7 V24 W7 W24 Y7 Y24 AA7 AA24 AB7 AB24 AC7 AC8 AC23 AC24 AD7 AD8 AD9 AD10 AD11 AD12 AD13 AD14 AD15 AD16 AD17 AD18 AD19 AD20 AD21 AD22 AD23 — VSS

OMIT

U4900
RAGE_MOBILITY
M10-CSP64
64MB
BGA
(3 OF 6)

41 39 GPU_DVOD<0>	AJ5	ZV_LCDDATA0	ROMCSB AE5 NC
41 39 GPU_DVOD<1>	AK5	ZV_LCDDATA1	R AK28 42 GPU_R
41 39 GPU_DVOD<2>	AG6	ZV_LCDDATA2	G AK27 42 GPU_G
41 39 GPU_DVOD<3>	AH6	ZV_LCDDATA3	B AK26 42 GPU_B
41 39 GPU_DVOD<4>	AJ6	ZV_LCDDATA4 OMIT	
41 39 GPU_DVOD<5>	AK6	ZV_LCDDATA5	VSYNC AG27 GPU_VSYNC 42
41 39 GPU_DVOD<6>	AG7	ZV_LCDDATA6	V2SYNC AG25 NC
41 39 GPU_DVOD<7>	AH7	ZV_LCDDATA7	HSYNC AG26 GPU_HSYNC 42
41 39 GPU_DVOD<8>	AJ7	ZV_LCDDATA8	H2SYNC AG24 NC
41 39 GPU_DVOD<9>	AK7	ZV_LCDDATA9	RSET AK25 GPU_RSET
41 39 GPU_DVOD<10>	AG8	ZV_LCDDATA10	R2SET AJ24 GPU_R2SET
41 39 GPU_DVOD<11>	AH8	ZV_LCDDATA11	
41 39 GPU_DVOD<12>	AJ8	ZV_LCDDATA12	Y_G AK23 42 GPU_Y
41 39 GPU_DVOD<13>	AK8	ZV_LCDDATA13	C_R AK24 42 GPU_C
41 39 GPU_DVOD<14>	AG9	ZV_LCDDATA14	COMP_B AK22 42 GPU_COMP
41 39 GPU_DVOD<15>	AH9	ZV_LCDDATA15	
41 39 GPU_DVOD<16>	AJ9	ZV_LCDDATA16	DIGON AE13 42 FP_PWR_EN
41 39 GPU_DVOD<17>	AK9	ZV_LCDDATA17	BLON AF13 42 INV_ON_PWM
41 39 GPU_DVOD<18>	AG10	ZV_LCDDATA18	HPD1 AF11 GPU_HPD 42
41 39 GPU_DVOD<19>	AH10	ZV_LCDDATA19	PP3V3_GPU 5 37 39 40
41 39 GPU_DVOD<20>	AJ10	ZV_LCDDATA20	
41 39 GPU_DVOD<21>	AK10	ZV_LCDDATA21	AUXWIN AJ27 GPU_AUXWIN
41 39 GPU_DVOD<22>	AG11	ZV_LCDDATA22	
41 39 GPU_DVOD<23>	AH11	ZV_LCDDATA23	DDC1DATA AH28 GPU_DVI_DDC_DATA 42
			DDC1CLK AH27 GPU_DVI_DDC_CLK 42
41 39 GPU_DVO_VSYNC	AJ4	ZV_LCDCNTL0	DDC2DATA AE12 LVDS_DDC_DATA 6 42
41 39 GPU_DVO_HSYNC	AK4	ZV_LCDCNTL1	DDC2CLK AF12 LVDS_DDC_CLK 6 42
41 39 GPU_DVO_DE	AH5	ZV_LCDCNTL2	DDC3DATA AH26 SI_DDC_DATA 41
41 39 GPU_DVO_CLKP	AG5	ZV_LCDCNTL3	DDC3CLK AH25 SI_DDC_CLK 41
39 GPU_AGP_FBSKEW<0>	AJ2	GPIO0	TXOUT_U0N AH18 LVDS_U0N 6 39 42
39 GPU_AGP_FBSKEW<1>	AK2	GPIO1	TXOUT_U0P AG18 LVDS_U0P 6 39 42
39 GPU_X1CLK_SKEW<0>	AK1	GPIO2	TXOUT_U1N AH19 LVDS_U1N 6 39 42
39 GPU_X1CLK_SKEW<1>	AH3	GPIO3	TXOUT_U1P AG19 LVDS_U1P 6 39 42
39 GPU_BUS_CFG<0>	AH2	GPIO4	TXOUT_U2N AH20 LVDS_U2N 6 39 42
39 GPU_BUS_CFG<1>	AJ1	GPIO5	TXOUT_U2P AG20 LVDS_U2P 6 39 42
39 GPU_BUS_CFG<2>	AF4	GPIO6	TXOUT_U3N AH22 TP_LVDS_U3N (NO ICT TEST)
41 SI_RESET_L	AH1	GPIO7	TXOUT_U3P AG22 TP_LVDS_U3P (NO ICT TEST)
GPU_GPIO8_PD	AG3	GPIO8	TXCLK_UN AH21 CLKLVDS_UN 6 39 42
NC	AF3	GPIO9	TXCLK_UP AG21 CLKLVDS_UP 6 39 42
NC	AE4	GPIO10	TXOUT_L0N AK16 LVDS_L0N 6 39 42
NC	AG1	GPIO11	TXOUT_L0P AJ16 LVDS_L0P 6 39 42
NC	AF1	GPIO12	TXOUT_L1N AK17 LVDS_L1N 6 39 42
	AE2	GPIO13	TXOUT_L1P AJ17 LVDS_L1P 6 39 42
42 HPD_PWR_SNS_EN	AE1	GPIO14	TXOUT_L2N AK18 LVDS_L2N 6 39 42
38 GPUVCORE_CNTL_L	AF2	GPIO15	TXOUT_L2P AJ18 LVDS_L2P 6 39 42
37 GPU_SSCLK_IN	AJ3	GPIO16	TXOUT_L3N AK20 TP_LVDS_L3N (NO ICT TEST)
			TXOUT_L3P AJ20 TP_LVDS_L3P (NO ICT TEST)
62 41 GPU_TMDS_DN<0>	AJ13	TX0M	TXCLK_LN AK19 CLKLVDS_LN 6 39 42
62 41 GPU_TMDS_DP<0>	AK13	TX0P	TXCLK_LP AJ19 CLKLVDS_LP 6 39 42
62 41 GPU_TMDS_DN<1>	AJ14	TX1M	
62 41 GPU_TMDS_DP<1>	AK14	TX1P	SSOUT AJ25 NC
62 41 GPU_TMDS_DN<2>	AJ15	TX2M	
62 41 GPU_TMDS_DP<2>	AK15	TX2P	VSS A20
62 41 GPU_TMDS_CLKN	AJ12	TXCM	VSS B21
62 41 GPU_TMDS_CLKP	AK12	TXCP	
37 GPU_CLK27M_DIV	AJ29	XTALIN	
NC	AJ30	XTALOUT	
1 GPU_TESTEN	AH24	TESTEN	
NC	AJ26	SSIN	
	B24	VSS	
	B20	VSS	
	A24	VSS	

R5105 75 1% 1/16W MF 402
R5104 75 1% 1/16W MF 402
R5103 75 1% 1/16W MF 402

R5109 715 1% 1/16W MF 402
R5108 499 1% 1/16W MF 402

R5102 75 1% 1/16W MF 402
R5106 75 1% 1/16W MF 402
R5107 75 1% 1/16W MF 402

R5127 10K 5% 1/16W MF 402
R5100 10K 5% 1/16W MF 402
R5101 10K 5% 1/16W MF 402

40 39 37 5 _PP3V3_GPU

R5119 10K 5% 1/16W MF 402
R5110 10K 5% 1/16W MF 402
R5112 10K 5% 1/16W MF 402 NO STUFF
R5113 10K 5% 1/16W MF 402 NO STUFF
R5115 10K 5% 1/16W MF 402 NO STUFF
R5117 10K 5% 1/16W MF 402 NO STUFF
R5121 10K 5% 1/16W MF 402 NO STUFF

(GPIO0)	GPU_AGP_FBSKEW<0> 39
(GPIO1)	GPU_AGP_FBSKEW<1> 39
(GPIO2)	GPU_X1CLK_SKEW<0> 39
(GPIO3)	GPU_X1CLK_SKEW<1> 39
(GPIO4)	GPU_BUS_CFG<0> 39
(GPIO5)	GPU_BUS_CFG<1> 39
(GPIO6)	GPU_BUS_CFG<2> 39

R5120 10K 5% 1/16W MF 402 NO STUFF
R5111 10K 5% 1/16W MF 402 NO STUFF
R5125 10K 5% 1/16W MF 402 NO STUFF
R5114 10K 5% 1/16W MF 402 NO STUFF
R5116 10K 5% 1/16W MF 402 NO STUFF
R5118 10K 5% 1/16W MF 402 NO STUFF
R5122 10K 5% 1/16W MF 402 NO STUFF

40 39 37 5 _PP3V3_GPU

NO STUFF
R5123 10K 5% 1/16W MF 402
R5126 1K 5% 1/16W MF 402

40 39 37 5 _PP3V3_GPU

EXT_TMDS
R5128 10K 5% 1/16W MF 402

41 40 37 5 _PP1V8_GPU

INT_TMDS
R5129 10K 5% 1/16W MF 402

R5124 1K 5% 1/16W MF 402

M10 Power Shut down Sequencing

PP2V5_RUN

XW5190 SM — DP5190 BAS16TW SOT-363 — XW5193 SM
40 PP1V8_GPU_PVDD_LDO
PP1V8_GPU_PVDD_NECK MIN_LINE_WIDTH=8mil MIN_NECK_WIDTH=8mil
PP2V5_RUN_NECK1 MIN_LINE_WIDTH=8mil MIN_NECK_WIDTH=8mil

XW5191 SM — DP5190 BAS16TW SOT-363
39 37 5 PPVCORE_GPU
PPVCORE_GPU_NECK MIN_LINE_WIDTH=8mil MIN_NECK_WIDTH=8mil
PP1V5_AGP_NECK MIN_LINE_WIDTH=8mil MIN_NECK_WIDTH=8mil

XW5194 SM
PP1V5_GPU_AGP 5 37 39 40

XW5192 SM — DP5190 BAS16TW SOT-363
39 PP1V5_GPU_VDD15
PP1V5_GPU_VDD15_NECK MIN_LINE_WIDTH=8mil MIN_NECK_WIDTH=8mil

M11 CORE PWR/LVDS/TMDS

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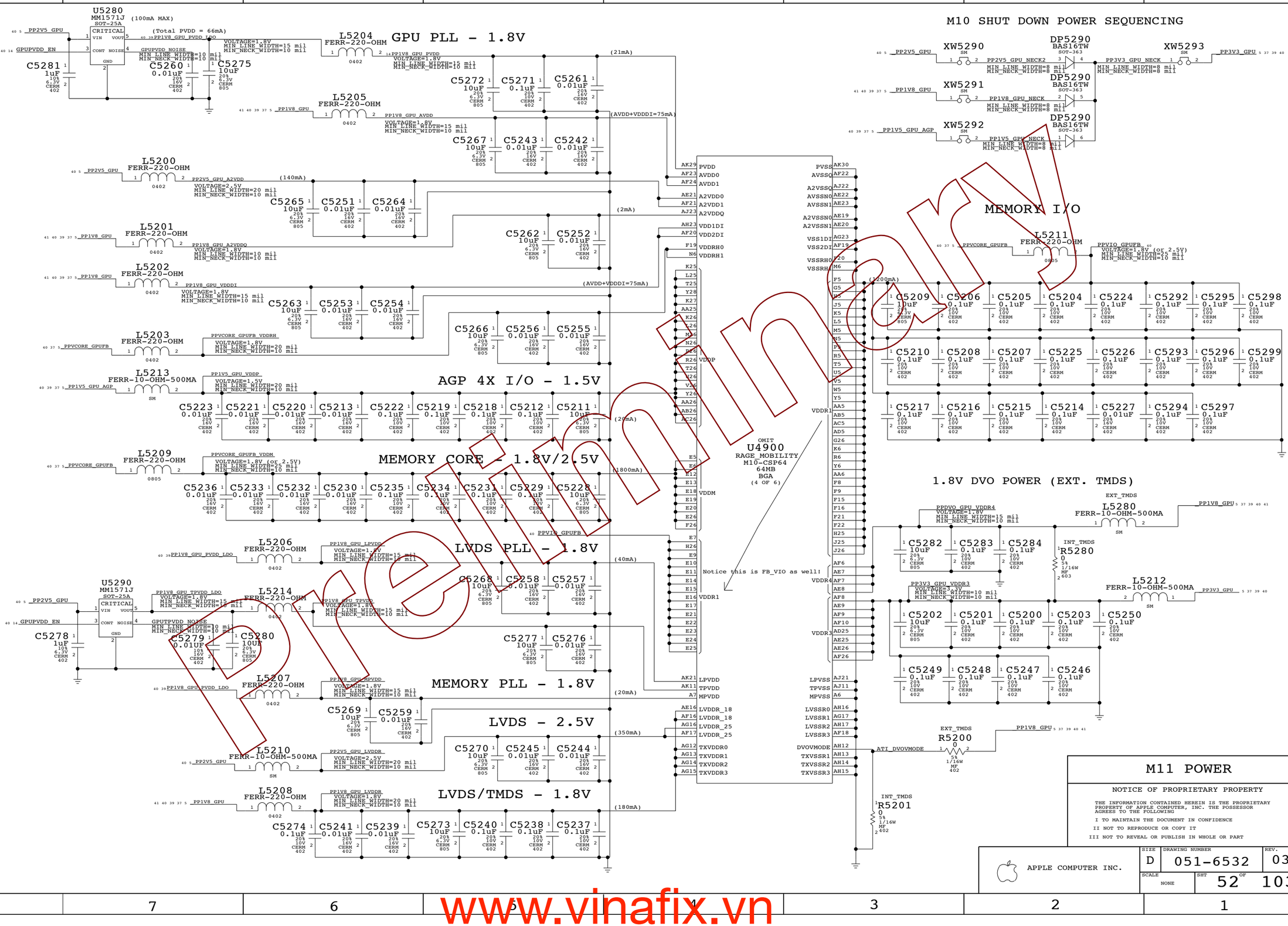
SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 51 OF 103	



Page Notes

Power aliases required by this page:
(None)

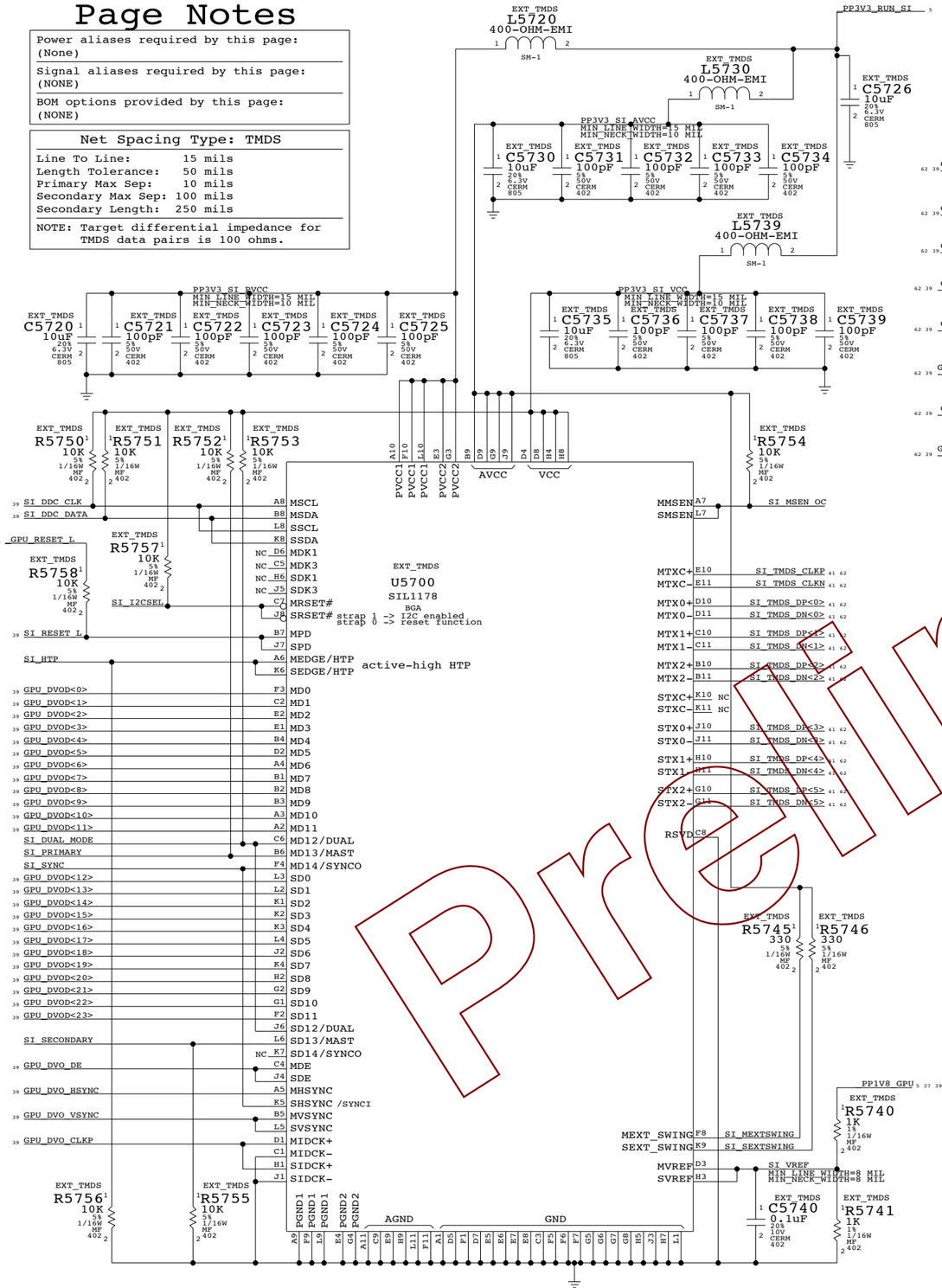
Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

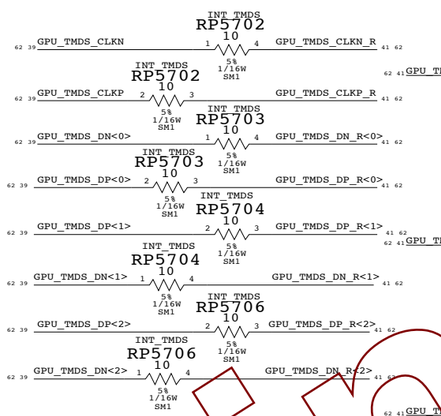
Net Spacing Type: TMDS

Line To Line:	15 mils
Length Tolerance:	50 mils
Primary Max Sep:	10 mils
Secondary Max Sep:	100 mils
Secondary Length:	250 mils

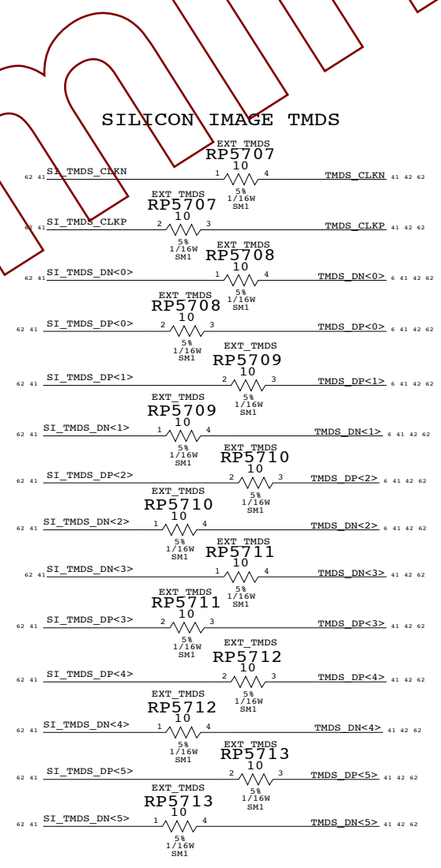
NOTE: Target differential impedance for TMDS data pairs is 100 ohms.



ATI TMDS

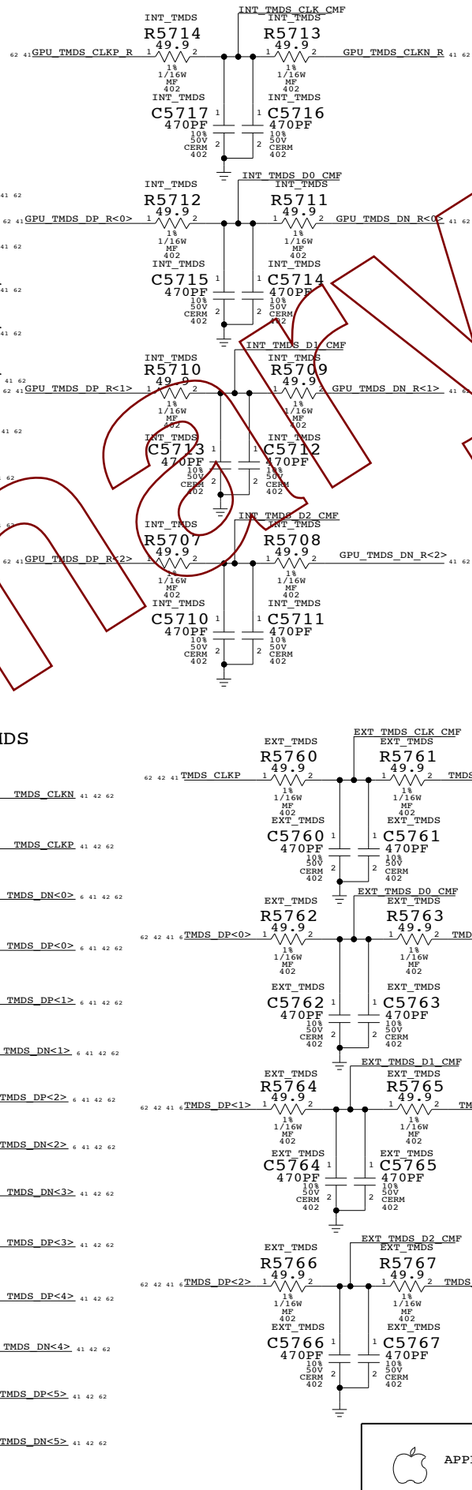


SILICON IMAGE TMDS

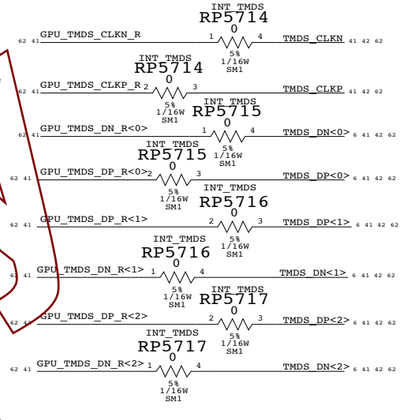


INTERNAL TMDS TERMINATION

TERMINATION NETWORK SHOULD BE CONNECTED AS SHOWN
CMF LINE SHOULD BE ROUTED AS 4MIL SURFACE
TRACE SO THAT IT MAY BE CUT BETWEEN CAPS

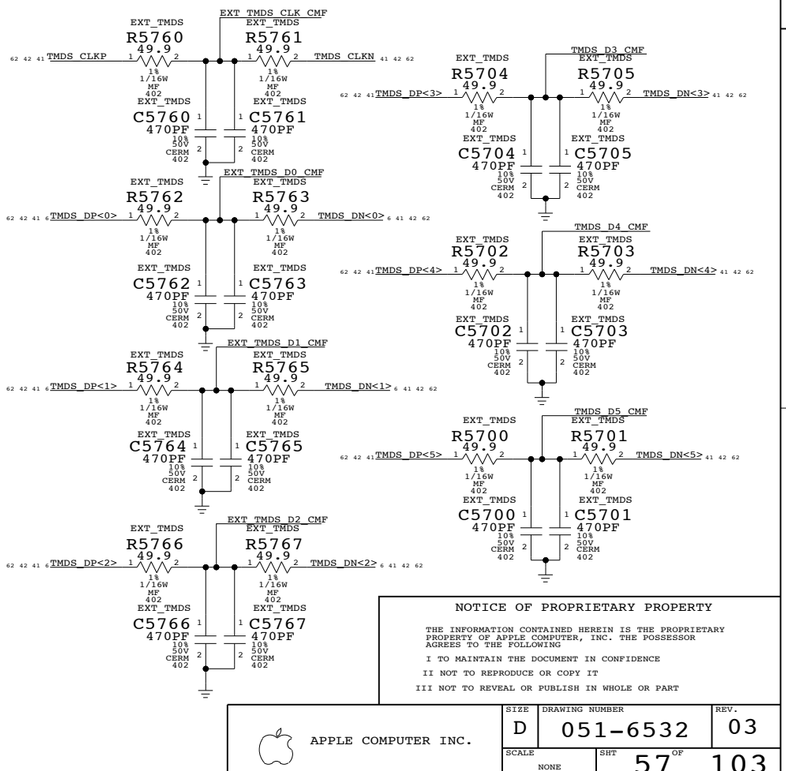


ATI TMDS



EXTERNAL TMDS TERMINATION

TERMINATION NETWORK SHOULD BE CONNECTED AS SHOWN
CMF LINE SHOULD BE ROUTED AS 4MIL SURFACE
TRACE SO THAT IT MAY BE CUT BETWEEN CAPS



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D	051-6532	03
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EXTERNAL VIDEO (DVI) INTERFACE

ANALOG FILTERING PLACE CLOSE TO CONNECTOR

FL5910 CRITICAL LCFILTER SM-220MHZ
FL5911 CRITICAL LCFILTER SM-220MHZ
FL5912 CRITICAL LCFILTER SM-220MHZ
C5910 3.3PF 0.25% 50V CERM 402
C5911 3.3PF 0.25% 50V CERM 402
C5912 3.3PF 0.25% 50V CERM 402

VGA VSYNC BUFFERS

U5913 74AHC1G32 SM
U5914 74AHC1G32 SM
R5913 33 5% 1/16W MF 402
R5914 33 5% 1/16W MF 402

TMDS FILTERING PLACE CLOSE TO CONNECTOR

L5916 90-OHM-300mA 2012H
L5917 90-OHM-300mA 2012H
L5918 90-OHM-300mA 2012H
L5919 90-OHM-300mA 2012H
L5920 90-OHM-300mA 2012H
L5921 90-OHM-300mA 2012H

DVI DDC CURRENT LIMIT

(55mA requirement per DVI spec)

F5900 0.5AMP-13.2V SM
L5900 400-OHM-EMI SM-1
D5900 MBR0530 SM
R5902 4.7K 5% 1/16W MF 402
R5903 4.7K 5% 1/16W MF 402
R5904 100 5% 1/16W MF 402
R5905 100 5% 1/16W MF 402
R5906 100 5% 1/16W MF 402
R5900 0 5% 1/16W MF 402 — PLACE NEAR 3, 11 & 19
R5901 0 5% 1/16W MF 402 — PLACE NEAR C5A & C5B
C5904 100pF 5% 50V CERM 402
C5905 100pF 5% 50V CERM 402
C5906 100pF 5% 50V CERM 402
C5900 0.01UF 20% 50V CERM 603

J5900 CRITICAL QH1112 F-RT-TH

3V LEVEL SHIFTERS

Q5907 2N7002DW SOT-363
Q5907 2N7002DW SOT-363
Q5909 2N7002DW SOT-363
R5907 10K 5% 1/16W MF 402
R5908 10K 5% 1/16W MF 402
R5909 100K 5% 1/16W MF 402

Q5909 shares with ALS sensor to save space

NOTE: Pulldown for DVI_HPD provided by DVI power switch interface

DVI POWER SWITCH

Power key detect path when system is shutdown or asleep.. DDC CLK is isolated from GPU DURING SHUTDOWN. WHEN power key on remote device is pressed, 5V will be driven into DDC CLK. Since host rails will be low, TP0610 will turn on, driving SOFT_PWR_ON_L low. As host rails rise, TP0610 will turn off, as will remote device path into DDC CLK. Insolation will be disabled as well.

Q5933 TP0610 SM
R5933 680 5% 1/16W MF 402
R5935 10K 5% 1/16W MF 402
R5934 330 5% 1/16W MF 402
Q5935 2N3904 SM

Pulldown prevents 3904 from turning on when DVI monitor has active, self-powered DDC clock pullup.

R5920 68.1K 1% 1/16W MF 402
C5920 0.1UF 10% 10V CERM 402
U5920 LMC7211 SM
R5922 10K 1% 1/16W MF 402
R5923 10K 1% 1/16W MF 402
R5921 100K 1% 1/16W MF 402
Q5925 2N7002DW SOT-363
Q5926 TP0610 SM
R5926 100K 5% 1/16W MF 402
R5927 100K 5% 1/16W MF 402
Q5925 2N7002DW SOT-363
R5925 100K 5% 1/16W MF 402
C5929 47UF 20% 6.3V CERM 1210
R5928 330 5% 1/16W MF 402
R5930 20K 5% 1/16W MF 402
R5929 68K 5% 1/16W MF 402
Q5930 2N3904 SM

Power key detect path when system is running. HPD normally driven to 3.3V. When power key on remote device pressed, HPD will be driven to 5V. COMPARATOR ENABLED BY GPU's GPIO.

NEED PULL-DOWN BECAUSE THIS SIGNAL IS TRISTATED INITIALLY

LCD INTERFACE

100K pull-ups are for no-panel case (development) Panel has 2K pull-ups

C5970 0.001uF 20% 50V CERM 402
J5970 CRITICAL G-501973 F-RT-SM
R5972 100K 5% 1/16W MF 402
R5973 100K 5% 1/16W MF 402
C5972 0.001uF 20% 50V CERM 402 — NO STUFF
C5973 0.001uF 20% 50V CERM 402
C5971 0.001uF 20% 50V CERM 402

LCD POWER SWITCH

R5977 100K 5% 1/16W MF 402
C5976 0.0022uF 10% 50V CERM 402
R5976 100K 5% 1/16W MF 402
Q5975 SI3443DV TSOP
L5975 FERR-250-OHM SM
C5975 0.001uF 20% 50V CERM 402
Q5977 2N7002 SM
R5999 0 5% 1/16W MF 402
C5999 0.01uF 20% 50V CERM 603

INVERTER INTERFACE

L5980 FERR-1K-OHM-EMI SM
Q5984 FDG6324L SC70-6
L5981 400-OHM-EMI SM-1
R5984 100K 5% 1/16W MF 402
C5984 10UF 20% 6.3V CERM 805
L5982 400-OHM-EMI SM-1
C5980 0.001UF 20% 50V CERM 402
C5981 0.001UF 20% 50V CERM 402
C5982 0.001UF 20% 50V CERM 402
J5980 CRITICAL SM-2MT
C5983 0.1UF 20% 10V CERM 402
U5983 CRITICAL 74AHC1G32 SM

INVERTER EXPECTS ACTIVE HIGH SIGNAL

S-VIDEO/COMP OUT INTERFACE

XW5960 SM
L5960 FERR-10-OHM-500MA SM
L5962 3.3UH 0603
L5963 3.3UH 0603
L5964 3.3UH 0603
XW5961 SM
L5961 FERR-10-OHM-500MA SM
C5960 0.01UF 20% 50V CERM 603
C5967 560PF 10% 50V CERM 402
C5968 560PF 10% 50V CERM 402
C5969 560PF 10% 50V CERM 402
C5962 560PF 10% 50V CERM 402
C5963 560PF 10% 50V CERM 402
C5964 560PF 10% 50V CERM 402
C5961 0.01UF 20% 50V CERM 603
J5960 CRITICAL MINIDIN RT-TH MH1177

Place GND shorts at graphics controller

Place GND shorts at graphics controller

VIDEO CONNECTORS

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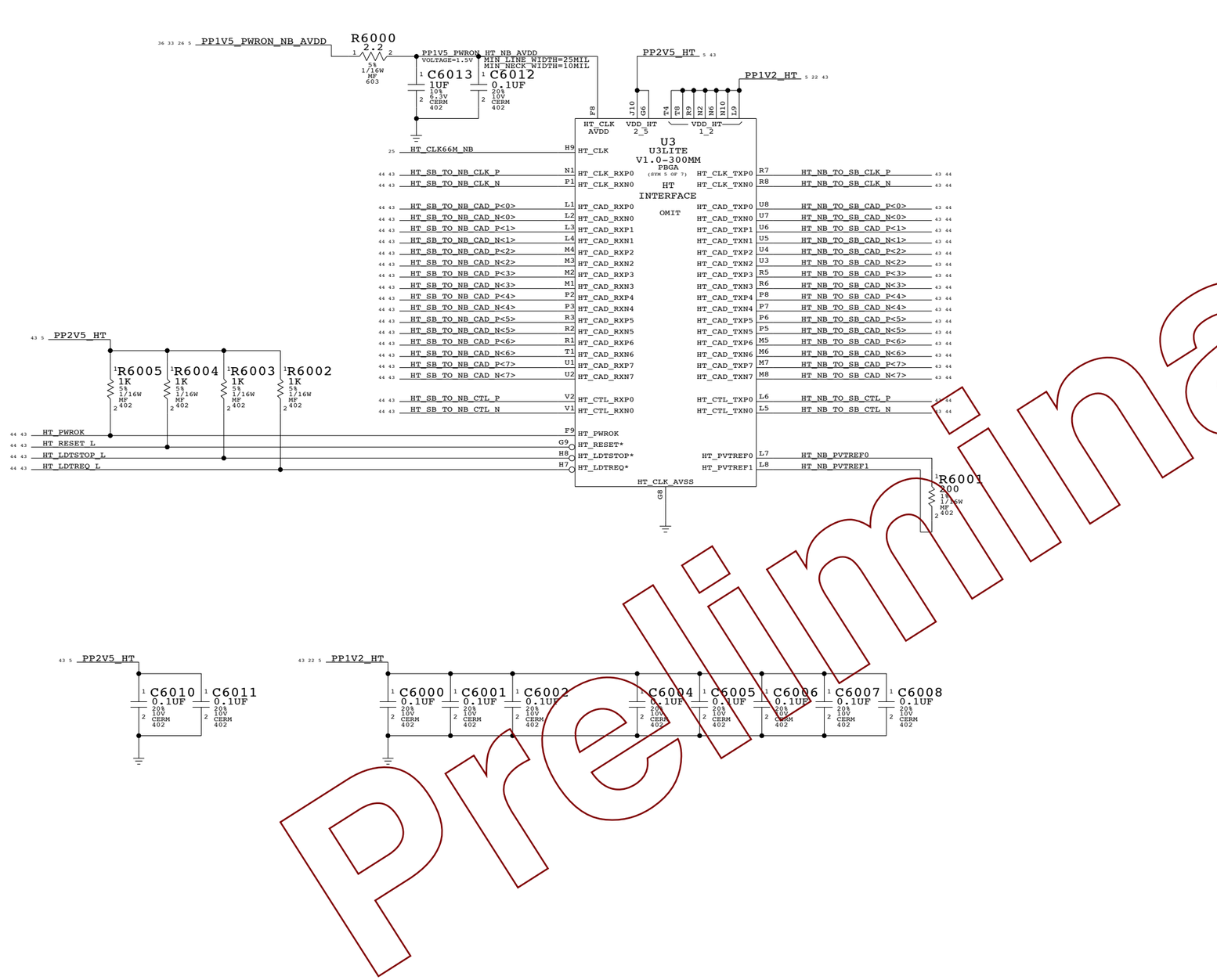


	ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
HT_NB_TO_SB_CLK_P	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CLK	146
HT_NB_TO_SB_CLK_N	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CLK	147
HT_NB_TO_SB_CTL_P	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CTL	183
HT_NB_TO_SB_CTL_N	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CTL	182
HT_NB_TO_SB_CAD_P<0>	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CAD0	151
HT_NB_TO_SB_CAD_N<0>	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CAD0	150
HT_NB_TO_SB_CAD_P<1>	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CAD1	152
HT_NB_TO_SB_CAD_N<1>	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CAD1	153
HT_NB_TO_SB_CAD_P<2>	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CAD2	154
HT_NB_TO_SB_CAD_N<2>	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CAD2	155
HT_NB_TO_SB_CAD_P<3>	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CAD3	156
HT_NB_TO_SB_CAD_N<3>	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CAD3	157
HT_NB_TO_SB_CAD_P<4>	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CAD4	158
HT_NB_TO_SB_CAD_N<4>	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CAD4	159
HT_NB_TO_SB_CAD_P<5>	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CAD5	160
HT_NB_TO_SB_CAD_N<5>	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CAD5	161
HT_NB_TO_SB_CAD_P<6>	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CAD6	162
HT_NB_TO_SB_CAD_N<6>	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CAD6	163
HT_NB_TO_SB_CAD_P<7>	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CAD7	164
HT_NB_TO_SB_CAD_N<7>	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CAD7	165
HT_SB_TO_NB_CLK_P	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CLK	148
HT_SB_TO_NB_CLK_N	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CLK	149
HT_SB_TO_NB_CTL_P	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CTL	184
HT_SB_TO_NB_CTL_N	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CTL	185
HT_SB_TO_NB_CAD_P<0>	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CAD0	166
HT_SB_TO_NB_CAD_N<0>	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CAD0	167
HT_SB_TO_NB_CAD_P<1>	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CAD1	168
HT_SB_TO_NB_CAD_N<1>	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CAD1	169
HT_SB_TO_NB_CAD_P<2>	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CAD2	170
HT_SB_TO_NB_CAD_N<2>	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CAD2	171
HT_SB_TO_NB_CAD_P<3>	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CAD3	172
HT_SB_TO_NB_CAD_N<3>	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CAD3	173
HT_SB_TO_NB_CAD_P<4>	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CAD4	174
HT_SB_TO_NB_CAD_N<4>	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CAD4	175
HT_SB_TO_NB_CAD_P<5>	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CAD5	176
HT_SB_TO_NB_CAD_N<5>	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CAD5	177
HT_SB_TO_NB_CAD_P<6>	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CAD6	178
HT_SB_TO_NB_CAD_N<6>	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CAD6	179
HT_SB_TO_NB_CAD_P<7>	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CAD7	180
HT_SB_TO_NB_CAD_N<7>	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CAD7	181
HT_PWROK	HT_PWROK	HT_2V5		186
HT_RESET_L	HT_CTL	HT_2V5		187
HT_LDTSTOP_L	HT_CTL	HT_2V5		188
HT_LDTREQ_L	HT_CTL	HT_2V5		189

HT_1V2

5 MIL SPACING FOR DIFF PAIR
10 MIL SPACING TO ANYTHING ELSE

HT_2V5

4 MIL SPACING IN GROUP
8 MIL SPACING TO ANYTHING ELSE

LENGTH TOLERENCE DOES NOT NEED TO BE SPECIFIED
MATCHED GROUP CONSTRAINT IS TIGHT ENOUGH

MASTER: GILA

U3LITE HT

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 60 OF 103	

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
	15 MIL SPACING	

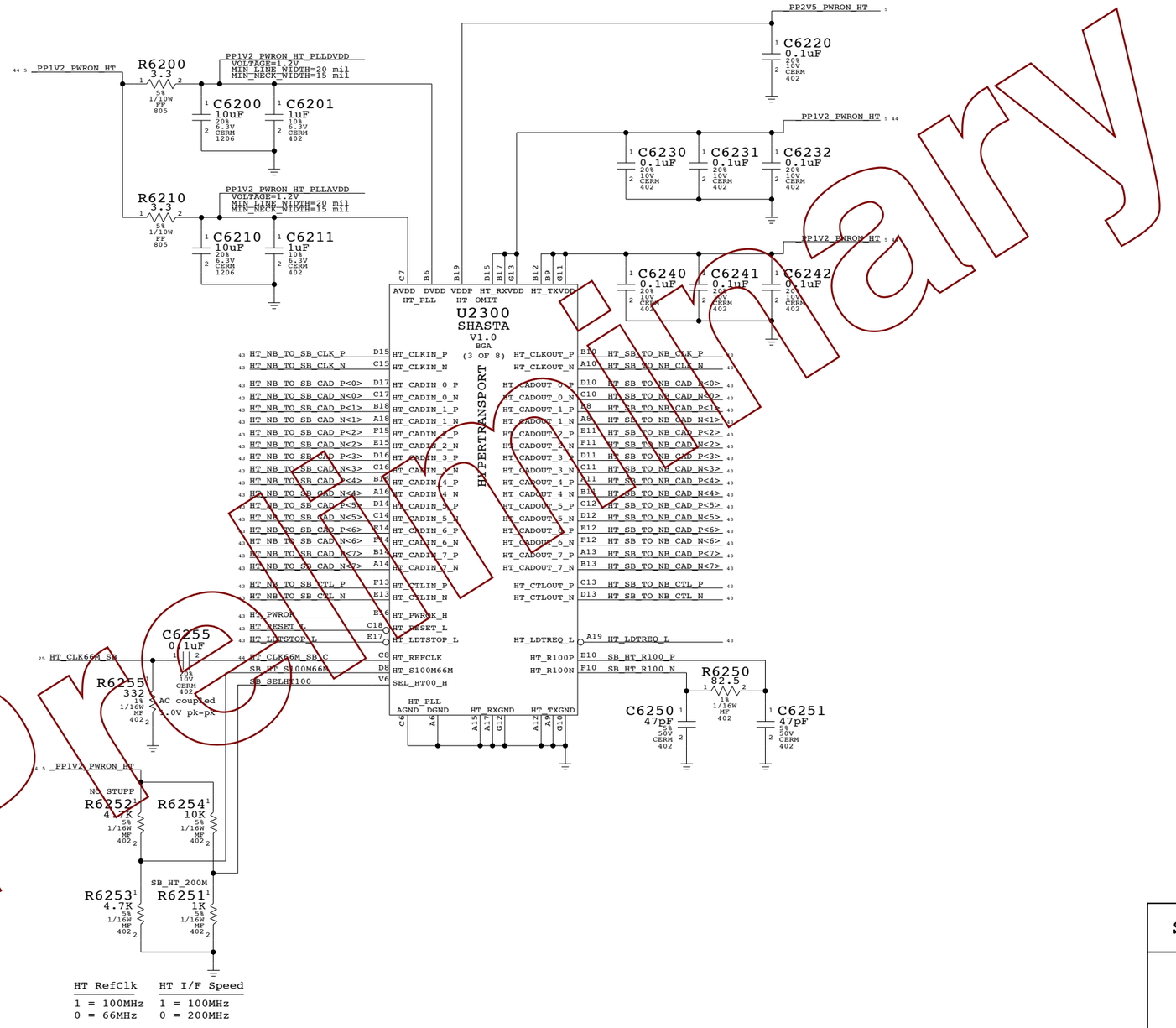
HT CLK66M SB C 44

Page Notes

Power aliases required by this page:
- _PP2V5_PWRON_HT
- _PP1V2_PWRON_HT

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- SB_HT_200M
  Stuffs resistor to select 200MHz HT I/F.



DRAWING
TITLE=FIZZY
ABBREV=DRAWING
LAST_MODIFIED=Mon Feb 23 19:06:27 2004

Master: Fizzy

Shasta HyperTransport

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 62 OF 103	

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
PCI_AD			PCI_AD<31..28> 6 46 47 48 49 62
PCI_AD27			PCI_AD<27> 6 46 47 48 49 62
PCI_AD			PCI_AD<26..24> 6 46 47 48 49 62
PCI_AD23			PCI_AD<23> 6 47 48 49 62
PCI_AD22			PCI_AD<22> 6 47 48 49 62
PCI_AD21			PCI_AD<21> 6 47 48 49 62
PCI_AD20			PCI_AD<20> 6 46 47 48 49 62
PCI_AD			PCI_AD<19..18> 6 46 47 48 49 62
PCI_AD17			PCI_AD<17> 6 46 47 48 49 62
PCI_AD			PCI_AD<16..0> 6 46 47 48 49 62
PCI			PCI_CBE_L<3..0> 6 47 48 49 62
PCI			PCI_PAR 6 47 48 49 62
PCI_CTL			PCI_DEVSEL_L 6 45 47 48 49 62
PCI_CTL			PCI_FRAME_L 6 45 47 48 49 62
PCI_CTL			PCI_IRDY_L 6 45 47 48 49 62
PCI_CTL			PCI_TRDY_L 6 45 47 48 49 62
PCI_CTL			PCI_STOP_L 6 45 47 48 49 62

Page Notes

Power aliases required by this page:
- _PP3V3_PCI
- _PP3V3_SB_PCI (can be _PP3V3_PCI)
- _PP3V3_PWRON_SB
- _PP2V5_PWRON_SB

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

PCI Devices implemented on this page:
AD11 - PCI0 (0x106B/0x0053)
AD11 - PCI1 (0x106B/0x0054)
AD11 - PCI2 (0x106B/0x0055)

AD23 - KeyLargo (0x106B/0x004F, PCI1)
AD28 - SATA 150 (0x1166/0x0240, PCI0 or 2)
AD29 - UATA 133 (0x106B/0x0050, PCI0 or 2)
AD30 - FireWire (0x106B/0x0052, PCI0 or 2)
AD31 - Ethernet (0x106B/0x0051, PCI0)

5 _PP3V3_SB_PCI

NO STUFF C7410 10uF 20% 6.3V CERM 805
C7400 0.1uF 20% 10V CERM 402
C7401 0.1uF 20% 10V CERM 402
C7402 0.1uF 20% 10V CERM 402
C7403 0.1uF 20% 10V CERM 402
C7404 0.1uF 20% 10V CERM 402

NO STUFF C7411 10uF 20% 6.3V CERM 805
C7405 0.1uF 20% 10V CERM 402
C7406 0.1uF 20% 10V CERM 402
C7407 0.1uF 20% 10V CERM 402
C7408 0.1uF 20% 10V CERM 402
C7409 0.1uF 20% 10V CERM 402

PP2V5_PWRON_SB 5 21 23 56

C7420 0.1uF 20% 10V CERM 402
C7421 0.1uF 20% 10V CERM 402
C7422 0.1uF 20% 10V CERM 402
C7423 0.1uF 20% 10V CERM 402

U2300 SHASTA V1.0 BGA (4 OF 8)

VDDOPC: AA22 B22 E21 H16 J21 M16 N21 R20 U21 V19
PCIVDDP: B20 J18 N20 U20
OMIT

PCI

25 PCI_CLK66M_SB_INT	AB9	PCIBR_CLK_H	
25 5 PCI_CLK33M_SB_EXT	U19	PCI1CLK_H	
"Slot A" - AD17			
47 46 6 PCI_SLOTA_REQ_L	AB18	PCI1REQ_0_L	
47 48 PCI_SLOTA_GNT_L	AA18	PCI1GNT_0_L	
"Slot G" - AD27			
47 45 PCI_SLOTG_REQ_L	AB20	PCI1REQ_1_L	
48 45 PCI_SLOTG_GNT_L	AB19	PCI1GNT_1_L	
"Slot D" - AD20			
45 PCI_SLOTD_REQ_L	V17	PCI1REQ_2_L	
45 PCI_SLOTD_GNT_L	V18	PCI1GNT_2_L	
47 46 6 ROM_CS_L	AB8	ROMCS_L	
47 46 6 ROM_OE_L	AA9	ROMOE_L	
47 46 6 ROM_WE_L	Y10	ROMRW_L	

PCI1AD_0_H	L18	PCI_SB_AD<0>	62
PCI1AD_1_H	K19	PCI_SB_AD<1>	62
PCI1AD_2_H	L22	PCI_SB_AD<2>	62
PCI1AD_3_H	M22	PCI_SB_AD<3>	62
PCI1AD_4_H	M18	PCI_SB_AD<4>	62
PCI1AD_5_H	L20	PCI_SB_AD<5>	62
PCI1AD_6_H	M21	PCI_SB_AD<6>	62
PCI1AD_7_H	N16	PCI_SB_AD<7>	62
PCI1AD_8_H	M20	PCI_SB_AD<8>	62
PCI1AD_9_H	P22	PCI_SB_AD<9>	62
PCI1AD_10_H	M17	PCI_SB_AD<10>	62
PCI1AD_11_H	N18	PCI_SB_AD<11>	62
PCI1AD_12_H	M19	PCI_SB_AD<12>	62
PCI1AD_13_H	N19	PCI_SB_AD<13>	62
PCI1AD_14_H	P21	PCI_SB_AD<14>	62
PCI1AD_15_H	R22	PCI_SB_AD<15>	62
PCI1AD_16_H	P20	PCI_SB_AD<16>	62
PCI1AD_17_H	V21	PCI_SB_AD<17>	62
PCI1AD_18_H	P18	PCI_SB_AD<18>	62
PCI1AD_19_H	T20	PCI_SB_AD<19>	62
PCI1AD_20_H	R16	PCI_SB_AD<20>	62
PCI1AD_21_H	R17	PCI_SB_AD<21>	62
PCI1AD_22_H	W21	PCI_SB_AD<22>	62
PCI1AD_23_H	Y22	PCI_SB_AD<23>	62
PCI1AD_24_H	R18	PCI_SB_AD<24>	62
PCI1AD_25_H	T19	PCI_SB_AD<25>	62
PCI1AD_26_H	T18	PCI_SB_AD<26>	62
PCI1AD_27_H	Y21	PCI_SB_AD<27>	48 62
PCI1AD_28_H	W20	PCI_SB_AD<28>	62
PCI1AD_29_H	T16	PCI_SB_AD<29>	62
PCI1AD_30_H	AA21	PCI_SB_AD<30>	62
PCI1AD_31_H	T17	PCI_SB_AD<31>	62
PCI1C_BE_0_L	L19	PCI_SB_CBE_L<0>	62
PCI1C_BE_1_L	P16	PCI_SB_CBE_L<1>	62
PCI1C_BE_2_L	V22	PCI_SB_CBE_L<2>	62
PCI1C_BE_3_L	V20	PCI_SB_CBE_L<3>	62
PCI1DEVSEL_L	T22	PCI_SB_DEVSEL_L	62
PCI1FRAME_L	T21	PCI_SB_FRAME_L	62
PCI1IRDY_L	R21	PCI_SB_IRDY_L	62
PCI1TRDY_L	P19	PCI_SB_TRDY_L	62
PCI1STOP_L	P17	PCI_SB_STOP_L	62
PCI1PAR_H	N17	PCI_SB_PAR	62
PCI1RST_L	U18	SB_PCI_RESET_L	

PP3V3_PCI 5 23 45 46 47 48 49

RP7400 4.7K 5% 1/16W SM1 — PCI_SLOTA_REQ_L 6 45 47
RP7400 4.7K 5% 1/16W SM1 — PCI_SLOTA_GNT_L 6 45 47
RP7400 4.7K 5% 1/16W SM1 — PCI_SLOTG_REQ_L 45 48
RP7400 4.7K 5% 1/16W SM1 — PCI_SLOTG_GNT_L 45 48
RP7401 4.7K 5% 1/16W SM1 — PCI_SLOTD_REQ_L 45
RP7401 4.7K 5% 1/16W SM1 — PCI_SLOTD_GNT_L 45

PP3V3_PWRON_SB 5 18 21 23

R7455 4.7K 5% 1/16W MF 402
C7450 0.1uF 20% 10V CERM 402
R7450 4.7K 5% 1/16W MF 402

U7450 MC74VHC1G08 SOT23-5

48 23 22 5 SYS_WARM_RESET_L

Shasta drives PCI RESET, but its output may not be valid during power-up, so it is ANDed with a reset from the SMU.

PCI_RESET_L 5 46 47 48

49 48 47 46 45 23 5 PP3V3_PCI

RP7402 4.7K 5% 1/16W SM1 — PCI_DEVSEL_L 62 49 48 47 45 6
RP7402 4.7K 5% 1/16W SM1 — PCI_FRAME_L 62 49 48 47 45 6
RP7402 4.7K 5% 1/16W SM1 — PCI_IRDY_L 62 49 48 47 45 6
RP7402 4.7K 5% 1/16W SM1 — PCI_TRDY_L 62 49 48 47 45 6
RP7401 4.7K 5% 1/16W SM1 — PCI_STOP_L 62 49 48 47 45 6

Master: Link

Shasta PCI Interface

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II NOT TO REPRODUCE OR COPY IT

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 74 OF 103	

DRAWING
TITTLE=LINK
ABBREV=DRAWING
LAST_MODIFIED=Mon Feb 23 19:06:40 2004

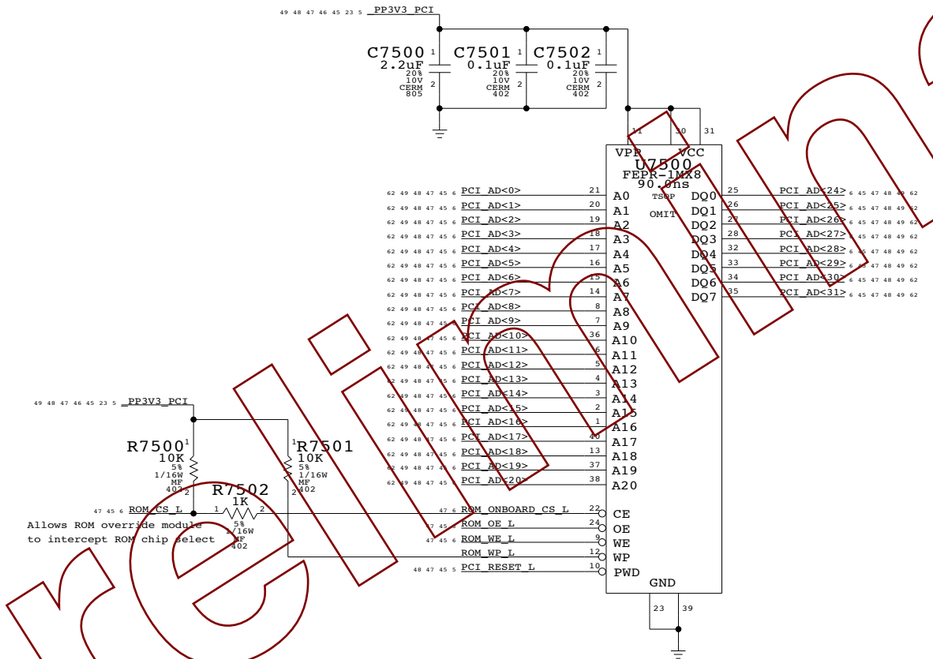
Page Notes

Power aliases required by this page:
- _PP3V3_PCI

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

NOTE: This page does not specify a BootROM part number. Must use a TABLE_x_ITEM symbol to declare U7500 part number.



Master: Fizzy

BootROM

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03

SCALE	SHT	OF
NONE	75	103

DRAWING
TITLE=FIZZY
ABBREV=DRAWING
LAST_MODIFIED=Mon Feb 23 19:06:47 2004

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
PCI_CLK_AIRPORT	CLOCKS	

PCI_CLK33M_AIRPORT 5 47

Page Notes

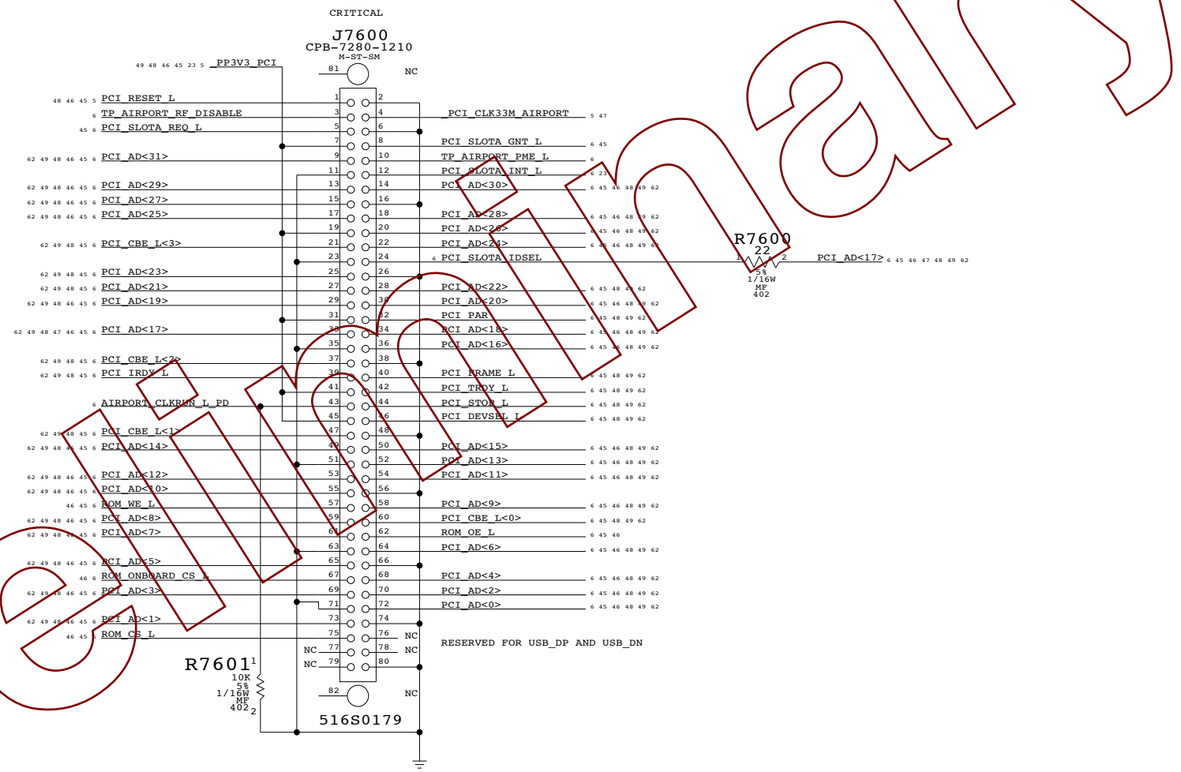
Power aliases required by this page:
- _PP3V3_PCI

Signal aliases required by this page:
- _PCI_CLK33M_AIRPORT (33MHz PCI clock)

BOM options provided by this page:
(NONE)

PCI Devices implemented on this page:
AD17 (Slot "A") - AirPort (0x????/0x????)

NOTE: This AirPort implementation does not support PME#.



DRAWING
TITLE=FIZZY
ABBREV=DRAWING
LAST_MODIFIED=Mon Feb 23 19:06:53 2004

AirPort Extreme

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 76 OF 103	

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
PCI_CLK_USB2	CLOCKS	

PCI_CLK33M_USB2 5 48

Page Notes

Power aliases required by this page:
- _PPVIO_PCI (to 3.3V or 5V)

Signal aliases required by this page:
- _PCI_CLK33M_USB2 (33MHz PCI clock)

BOM options provided by this page:
(NONE)

PCI Devices implemented on this page:
AD27 (Slot "G") - USB2 (0x1033/0x0035)

NOTE: This USB2 implementation supports D3cold.

5 _PPVIO_PCI_USB2

C7703 0.1uF 20% 10V CERM 402

VDD_PCI

CRITICAL
U7700
NEC_uPD720101_USB2
FBGA

PCI_AD<0>	M5	AD0	
PCI_AD<1>	P5	AD1	
PCI_AD<2>	N5	AD2	
PCI_AD<3>	P4	AD3	
PCI_AD<4>	N4	AD4	
PCI_AD<5>	M3	AD5	
PCI_AD<6>	N3	AD6	
PCI_AD<7>	M1	AD7	
PCI_AD<8>	L2	AD8	
PCI_AD<9>	L1	AD9	
PCI_AD<10>	K2	AD10	
PCI_AD<11>	L3	AD11	
PCI_AD<12>	K1	AD12	
PCI_AD<13>	K3	AD13	
PCI_AD<14>	J2	AD14	
PCI_AD<15>	J1	AD15	
PCI_AD<16>	F2	AD16	
PCI_AD<17>	E3	AD17	
PCI_AD<18>	E1	AD18	
PCI_AD<19>	D3	AD19	
PCI_AD<20>	D1	AD20	
PCI_AD<21>	D2	AD21	
PCI_AD<22>	C2	AD22	
PCI_AD<23>	C1	AD23	
PCI_AD<24>	B6	AD24	
PCI_AD<25>	A4	AD25	
PCI_AD<26>	B5	AD26	
PCI_AD<27>	C4	AD27	
PCI_AD<28>	A5	AD28	
PCI_AD<29>	C5	AD29	
PCI_AD<30>	B6	AD30	
PCI_AD<31>	A6	AD31	
PCI_CBE_L<0>	M2	CBE0	
PCI_CBE_L<1>	J3	CBE1	
PCI_CBE_L<2>	F1	CBE2	
PCI_CBE_L<3>	C3	CBE3	
PCI_PAR	J4	PAR	
PCI_FRAME_L	F3	FRAME	
PCI_IRDY_L	F4	IRDY	
PCI_TRDY_L	G1	TRDY	
PCI_STOP_L	G3	STOP	
PCI_SLOTG_IDSEL	B3	IDSEL	
PCI_DEVSEL_L	G5	DEVSEL	
PCI_SLOTG_REQ_L	C6	REQ	
PCI_SLOTG_GNT_L	D6	GNT	
NEC_PERR_L_PU	H2	PERR	
NEC_SERR_L_PU	H1	SERR OD	
NEC_INTA_L	C7	INTA OD	
NEC_INTB_L	B7	INTB OD	
NEC_INTC_L	A7	INTC OD	
48 5 _PCI_CLK33M_USB2	A8	PCLK	
NEC_VBBRST_L	B8	VBBRST(CHIP RESET)	
NEC_CRUN_L_PD	N6	CRUN	
NEC_PME_L	D5	PME OD	
NEC_VCCRST_L	C9	VCCRST(PCI RESET)	
TP_NEC_SMI_L	L6	SMI OD	
NEC_LEGC_PD	L7	LEGC	

IPD NTEST1	M8	TP_NEC_NTEST1	
IPD SMC	M7	TP_NEC_SMC	
IPD TEB	N7	TP_NEC_TEB	
IPD AMC	P7	TP_NEC_AMC	
IPD TEST	L8	TP_NEC_TEST	
NANDTEST	M10	TP_NEC_NANDTEST	
SRCLK	M9	TP_NEC_SRCLK	
SRDTA	N9	TP_NEC_SRDATA	
IPD SRMOD	P9	TP_NEC_SRMOD	

62 45 PCI_SB_AD<27>

R7714 22 5% 1/16W MF 402

49 47 46 45 23 5 _PP3V3_PCI

R7716 10K 5% 1/16W MF 402

R7713 10K 5% 1/16W MF 402

RP7703 47 5% 1/16W SM1

RP7703 47 5% 1/16W SM1

RP7703 47 5% 1/16W SM1

RP7702 47 5% 1/16W SM1

RP7702 47 5% 1/16W SM1

RP7702 47 5% 1/16W SM1

23 PCI_SLOTG_INT_L

45 23 22 5 SYS_WARM_RESET_L

23 13 SYS_PME_L

47 46 45 5 PCI_RESET_L

RP7702 & RP7703 required to facilitate NAND-tree testing

R7715 4.7K 5% 1/16W MF 402

RP7703 47 5% 1/16W SM1

Master: Fizzy

USB 2.0 PCI Interface

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03

SCALE	SHT	OF
NONE	77	103

DRAWING
TITLE=FIZZY
ABBREV=DRAWING
LAST_MODIFIED=Mon Feb 23 19:07:00 2004

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
PCI_CLK_CBUS	CLOCKS	

PCI_CLK33M_CBUS 5 49

Page Notes

Power aliases required by this page:
- _PP5V_CBUS
- _PP3V3_CBUS
- _PP3V3_PCI
- _PP2V5_PCI
- _PPVIO_PCI (to _PP5V_PCI or _PP3V3_PCI)

NOTE: All 4 rails MUST implement the same power state (PWRON or RUN). For PWRON must alias _PCI_CBUS_RESET_L to SYS_WARM_RESET_L. For RUN must alias to PCI_RESET_L instead.

Signal aliases required by this page:
- _PCI_CBUS_RESET_L (see note above)
- _PCI_CLK33M_CBUS (33MHz PCI clock)

BOM options provided by this page:
(NONE)

PCI Devices implemented on this page:
AD21 (Slot "E") - CardBus (0x104C/0xAC56)

Power Sequencing:

Power Up	Power Down
1. Assert RESET	1. Assert RESET
2. _PP3V3_PCI	2. _PPVIO_PCI
3. _PPVIO_PCI	3. _PP3V3_PCI

(_PPVIO_PCI can be same as _PP3V3_PCI)

NOTE: This CardBus implementation does not provide PME# or 12V Vpp support.

PC Card Power Switch

Make sure Vcc and Vpp are wide plane/traces to minimize inductance!

CRITICAL
U7801
TPS2211
V_12 SSOI AVPP
V_5_1
V_5_2 AVCC0
V_3_1 AVCC1
V_3_2 AVCC2
VCCD0
VCCD1
VPPD0
VPPD1
SHTDWN
GND
OC

5 _PP5V_CBUS
5 _PP3V3_CBUS
49 PCI_CBUS_RESET_L_R
Disable card power during reset

PPVPP_CBUS 49 VOLTAGE=5V (or 3.3V) MIN_LINE_WIDTH=25 mil MIN_NECK_WIDTH=10 mil
PPVCC_CBUS 49 VOLTAGE=5V (or 3.3V) MIN_LINE_WIDTH=25 mil MIN_NECK_WIDTH=10 mil

C7808 0.1UF 20% 10V CERM 402
C7809 0.1UF 20% 10V CERM 402
0.1uF are used to increase ESD of up to 10kV

XW7800 SM
This is an internal board short
Allows thinner trace to PGA

TI reference schematic does not have bulk on PPVCC_CBUS

C7810 2.2uF 20% 10V CERM 805
C7811 2.2uF 20% 10V CERM 805

PC Card/CardBus Connector

CRITICAL
J7800
QT500806-L111
M-ST-SM

49 CBUS_DET_1_L	4	3	CBUS_DATA<4> 49
49 CBUS_DATA<11>	6	5	CBUS_DATA<5> 49
49 CBUS_DATA<12>	8	7	CBUS_DATA<6> 49
49 CBUS_DATA<13>	10	9	
	12	11	CBUS_DATA<7> 49
49 CBUS_DATA<14>	14	13	CBUS_CE1_L 49
49 CBUS_DATA<15>	16	15	CBUS_ADDR<10> 49
49 CBUS_CE2_L	18	17	CBUS_OE_L 49
49 CBUS_VS1	20	19	
	22	21	CBUS_ADDR<11> 49
49 CBUS_IORD_L	24	23	CBUS_ADDR<9> 49
49 CBUS_IOWR_L	26	25	CBUS_ADDR<8> 49
49 CBUS_ADDR<17>	28	27	CBUS_ADDR<13> 49
49 CBUS_ADDR<18>	30	29	
	32	31	CBUS_ADDR<14> 49
49 CBUS_ADDR<19>	34	33	CBUS_WE_L 49
49 CBUS_ADDR<20>	36	35	CBUS_READY 49
49 CBUS_ADDR<21>	38	37	PPVCC_CBUS 49
49 PPVCC_CBUS	40	39	
	42	41	PPVPP_CBUS 49
49 PPVPP_CBUS	44	43	CBUS_ADDR<16> 49
49 CBUS_ADDR<22>	46	45	CBUS_ADDR<15> 49
49 CBUS_ADDR<23>	48	47	CBUS_ADDR<12> 49
49 CBUS_ADDR<24>	50	49	
	52	51	CBUS_ADDR<7> 49
49 CBUS_ADDR<25>	54	53	CBUS_ADDR<6> 49
49 CBUS_VS2	56	55	CBUS_ADDR<5> 49
49 CBUS_RESET_L	58	57	CBUS_ADDR<4> 49
49 CBUS_WAIT_L	60	59	
	62	61	CBUS_ADDR<3> 49
49 CBUS_INPACK_L	64	63	CBUS_ADDR<2> 49
49 CBUS_REG_L	66	65	CBUS_ADDR<1> 49
49 CBUS_BVD2_L	68	67	CBUS_ADDR<0> 49
49 CBUS_BVD1_L	70	69	
	72	71	CBUS_DATA<0> 49
49 CBUS_DATA<8>	74	73	CBUS_DATA<1> 49
49 CBUS_DATA<9>	76	75	CBUS_DATA<2> 49
49 CBUS_DATA<10>	78	77	CBUS_WP_L 49
49 CBUS_DET_2_L	80	79	
	84	81	
	83	82	

516S0089

Master: Fizzy

CardBus Interface

NOTICE OF PROPRIETARY PROPERTY

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 78 OF 103	

DRAWING
TITLE=FIZZY
ABBREV=DRAWING
LAST_MODIFIED=Mon Feb 23 19:07:07 2004

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR		
SATA_RXD1	SATA	SATA_RXD1_C	SATA_RXD_P1_C	50 51
SATA_RXD1	SATA	SATA_RXD1_C	SATA_RXD_N1_C	50 51
SATA_TXD1	SATA	SATA_TXD1	SATA_TXD_P1	50 51
SATA_TXD1	SATA	SATA_TXD1	SATA_TXD_N1	50 51
SATA_RXD2	SATA	SATA_RXD2_C	SATA_RXD_P2_C	5 50
SATA_RXD2	SATA	SATA_RXD2_C	SATA_RXD_N2_C	5 50
SATA_TXD2	SATA	SATA_TXD2	SATA_TXD_P2	5 50
SATA_TXD2	SATA	SATA_TXD2	SATA_TXD_N2	5 50
UATA_DD			UATA_DD<15..8>	6 50 52
UATA_DD7			UATA_DD<7>	6 50 52
UATA_DD			UATA_DD<6..0>	6 50 52
UATA_HOST			UATA_DA<2..0>	6 50 52
UATA_HOST			UATA_CS0_L	6 50 52
UATA_HOST			UATA_CS1_L	6 50 52
UATA_HOST			UATA_HSTROBE	6 50 52
UATA_HOST			UATA_STOP	6 50 52
UATA_HOST_R			UATA_DMACK_L	6 50 52
UATA_HOST_R			UATA_RESET_L	6 50 52
UATA_DEV_R_C			UATA_DSTROBE	50 52
UATA_DEV_R			UATA_DMARQ	50 52
UATA_DEV_R			UATA_INTRQ	50 52

Page Notes

Power aliases required by this page:
- _PP1V2_PWRON_DISK

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Net Spacing Type: SATA

Line To Line:	15 mils
Length Tolerance:	50 mils
Primary Max Sep:	10 mils outer
Primary Max Sep:	9 mils inner
Secondary Max Sep:	100 mils
Secondary Length:	500 mils

NOTE: Target differential impedance for SATA data pairs is 100 ohms.

5 PP1V2_PWRON_DISK_SB

SATA_VDD x 5

C8000 0.1uF 20% 10V CERM 402
C8001 0.1uF 20% 10V CERM 402
C8002 0.1uF 20% 10V CERM 402
C8003 0.1uF 20% 10V CERM 402
C8004 0.1uF 20% 10V CERM 402

AB14 AB17 T14 W15 Y18 SATA_VDD

U2300 OMIT
SHASTA
V1.0
BGA
(5 OF 8)

UD_IDEDD_0_H	J6	UATA_DD_R<0>	50
UD_IDEDD_1_H	H7	UATA_DD_R<1>	50
UD_IDEDD_2_H	H6	UATA_DD_R<2>	50
UD_IDEDD_3_H	E2	UATA_DD_R<3>	50
UD_IDEDD_4_H	C1	UATA_DD_R<4>	50
UD_IDEDD_5_H	C2	UATA_DD_R<5>	50
UD_IDEDD_6_H	E3	UATA_DD_R<6>	50
UD_IDEDD_7_H	G6	UATA_DD_R<7>	50
UD_IDEDD_8_H	G5	UATA_DD_R<8>	50
UD_IDEDD_9_H	D4	UATA_DD_R<9>	50
UD_IDEDD_10_H	G7	UATA_DD_R<10>	50
UD_IDEDD_11_H	F6	UATA_DD_R<11>	50
UD_IDEDD_12_H	C3	UATA_DD_R<12>	50
UD_IDEDD_13_H	F5	UATA_DD_R<13>	50
UD_IDEDD_14_H	E5	UATA_DD_R<14>	50
UD_IDEDD_15_H	D5	UATA_DD_R<15>	50
UD_IDEDA0_H	E6	UATA_DA_R<0>	50
UD_IDEDA1_H	C4	UATA_DA_R<1>	50
UD_IDEDA2_H	D6	UATA_DA_R<2>	50
UD_IDECS1FX_L	B3	UATA_CS0_L_R	50
UD_IDECS3FX_L	B4	UATA_CS1_L_R	50
UD_IDEDMACK_L	E8	UATA_DMACK_L_R	50
UD_IDERD_L	E4	UATA_HSTROBE_R	50
UD_IDEWR_L	D3	UATA_STOP_R	50
UD_IDERST_L	E7	UATA_RESET_L_R	50

UATA

DSTROBE aka:
IORDY/HDMARDY*

HSTROBE aka:
DIOR*

STOP aka:
DIOW*

52 50 UATA_DSTROBE	F9	UD_IDECHRDY_H	
52 50 UATA_DMARQ	D7	UD_IDEDMARQ_H	
52 50 UATA_INTRQ	C5	UD_IDEINTRQ_H	

51 50 SATA_RXD_P1_C	Y17	RXDP1	TXDP1	AA16 SATA_TXD_P1 50 51
51 50 SATA_RXD_N1_C	Y16	RXDN1	TXDN1	AB16 SATA_TXD_N1 50 51
		SATA 0		
50 5 SATA_RXD_P2_C	AB15	RXDP2	TXDP2	Y15 SATA_TXD_P2 5 50
50 5 SATA_RXD_N2_C	AA15	RXDN2	TXDN2	Y14 SATA_TXD_N2 5 50
		SATA 1		

SATA_GND
AA14 AA17 T13 W16

AC coupling required for any SATA pair used.
Recommend 0.1uF cap placed close to Shasta.
(Caps provided by device page)

UATA Termination

R8005 10K 5% 1/16W MF 402

RP8000	33	5% 1/16W SM1	
50 UATA_DD_R<0>	4 5		UATA_DD<0> 6 50 52
RP8000	33	5% 1/16W SM1	
50 UATA_DD_R<1>	3 6		UATA_DD<1> 6 50 52
RP8000	33	5% 1/16W SM1	
50 UATA_DD_R<2>	2 7		UATA_DD<2> 6 50 52
RP8003	33	5% 1/16W SM1	
50 UATA_DD_R<3>	4 5		UATA_DD<3> 6 50 52
RP8001	33	5% 1/16W SM1	
50 UATA_DD_R<4>	1 8		UATA_DD<4> 6 50 52
RP8001	33	5% 1/16W SM1	
50 UATA_DD_R<5>	2 7		UATA_DD<5> 6 50 52
RP8003	33	5% 1/16W SM1	
50 UATA_DD_R<6>	3 6		UATA_DD<6> 6 50 52
RP8002	33	5% 1/16W SM1	
50 UATA_DD_R<7>	1 8		UATA_DD<7> 6 50 52
RP8002	33	5% 1/16W SM1	
50 UATA_DD_R<8>	2 7		UATA_DD<8> 6 50 52
RP8003	33	5% 1/16W SM1	
50 UATA_DD_R<9>	2 7		UATA_DD<9> 6 50 52
RP8000	33	5% 1/16W SM1	
50 UATA_DD_R<10>	1 8		UATA_DD<10> 6 50 52
RP8002	33	5% 1/16W SM1	
50 UATA_DD_R<11>	4 5		UATA_DD<11> 6 50 52
RP8001	33	5% 1/16W SM1	
50 UATA_DD_R<12>	3 6		UATA_DD<12> 6 50 52
RP8002	33	5% 1/16W SM1	
50 UATA_DD_R<13>	3 6		UATA_DD<13> 6 50 52
RP8004	33	5% 1/16W SM1	
50 UATA_DD_R<14>	1 8		UATA_DD<14> 6 50 52
RP8003	33	5% 1/16W SM1	
50 UATA_DD_R<15>	1 8		UATA_DD<15> 6 50 52
RP8004	33	5% 1/16W SM1	
50 UATA_DA_R<0>	2 7		UATA_DA<0> 6 50 52
RP8001	33	5% 1/16W SM1	
50 UATA_DA_R<1>	4 5		UATA_DA<1> 6 50 52
RP8004	33	5% 1/16W SM1	
50 UATA_DA_R<2>	4 5		UATA_DA<2> 6 50 52
RP8004	33	5% 1/16W SM1	
50 UATA_RESET_L_R	3 6		UATA_RESET_L 6 50 52
R8000	33	5% 1/16W MF 402	
50 UATA_CS0_L_R	1 2		UATA_CS0_L 6 50 52
R8001	33	5% 1/16W MF 402	
50 UATA_CS1_L_R	1 2		UATA_CS1_L 6 50 52
R8002	22	5% 1/16W MF 402	
50 UATA_HSTROBE_R	1 2		UATA_HSTROBE 6 50 52
R8003	22	5% 1/16W MF 402	
50 UATA_STOP_R	1 2		UATA_STOP 6 50 52
R8004	22	5% 1/16W MF 402	
50 UATA_DMACK_L_R	1 2		UATA_DMACK_L 6 50 52

Master: Link

Shasta Disk

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 80 OF 103	

DRAWING
TITLE=FIZZY
ABBREV=DRAWING
LAST_MODIFIED=Mon Feb 23 19:07:21 2004

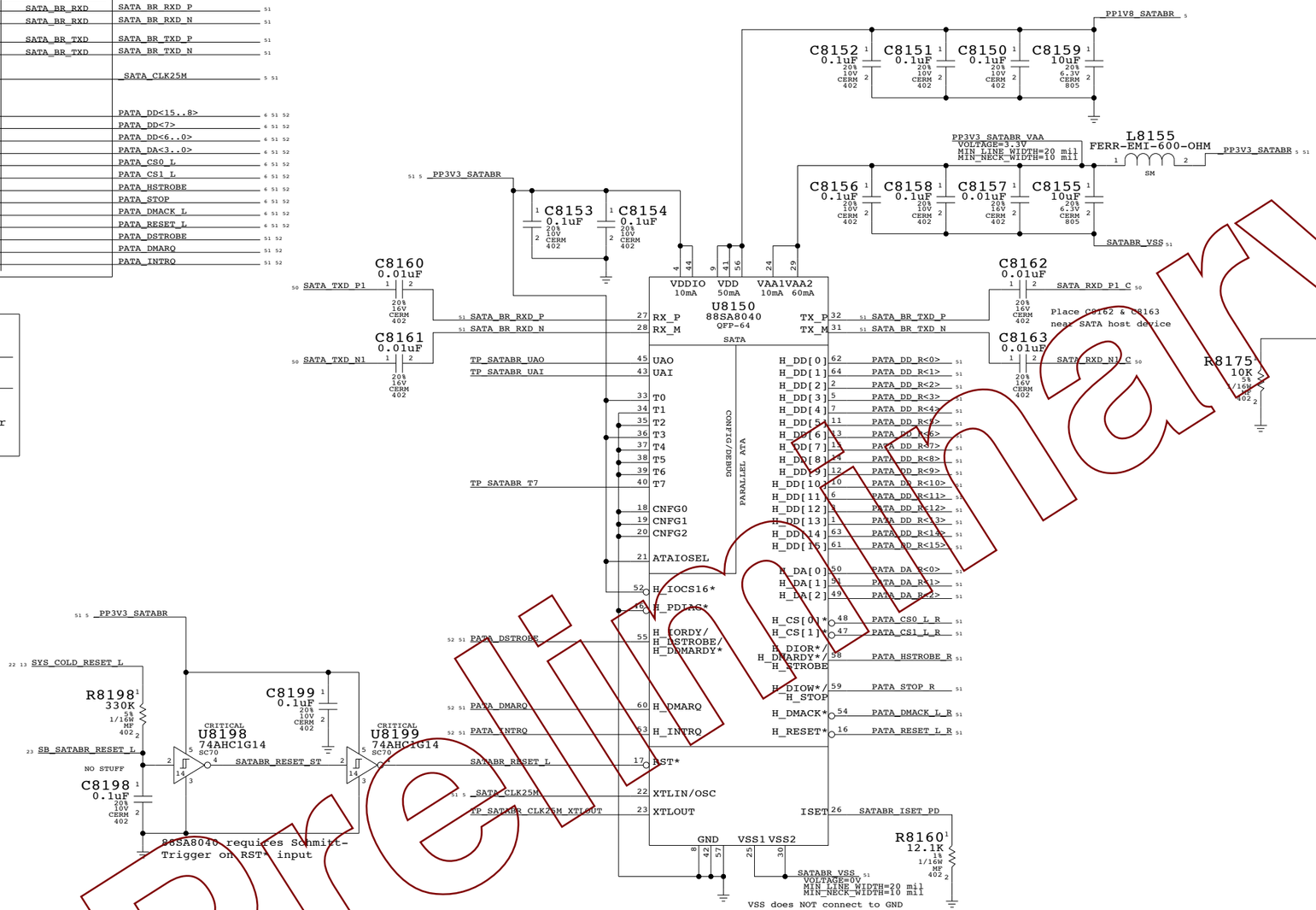
ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
PROVIDED BY SATA CONTROLLER	SATA	SATA_BR_RXD	SATA_BR_RXD_P
	SATA	SATA_BR_RXD	SATA_BR_RXD_N
	SATA	SATA_BR_TXD	SATA_BR_TXD_P
	SATA	SATA_BR_TXD	SATA_BR_TXD_N
	CLOCKS		_SATA_CLK25M
PATA_HOST			PATA_DD<15..8>
PATA_DD7			PATA_DD<7>
PATA_HOST			PATA_DD<6..0>
PATA_HOST			PATA_DA<3..0>
PATA_HOST			PATA_CS0_L
PATA_HOST			PATA_CS1_L
PATA_HOST			PATA_HSTROBE
PATA_HOST			PATA_STOP
PATA_HOST_R			PATA_DMACK_L
PATA_HOST_R			PATA_RESET_L
PATA_DEV_R_C			PATA_DSTROBE
PATA_DEV_R			PATA_DMARQ
PATA_DEV_R			PATA_INTRQ

Page Notes

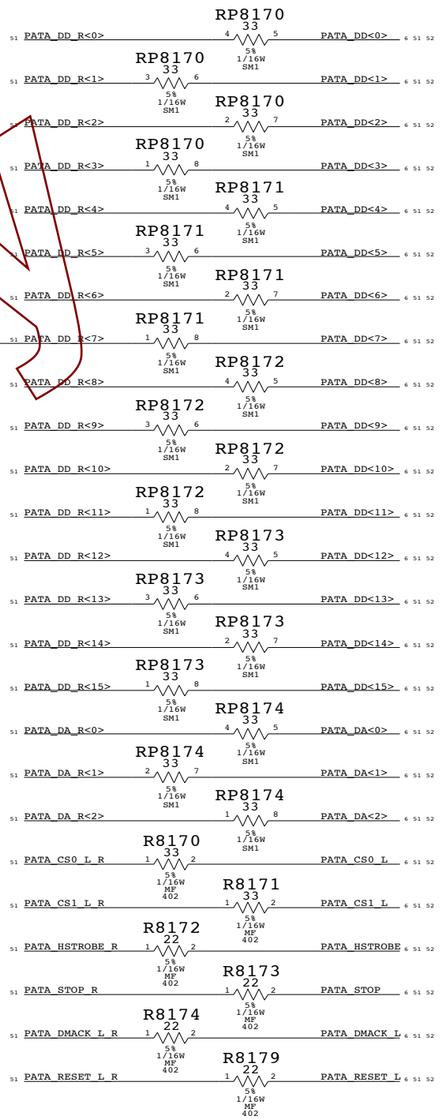
Power aliases required by this page:
- _PP3V3_SATABR
- _PP1V8_SATABR

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- SATA_1_BRIDGE (/ SATA_1_CONN)
  Selects whether 88SA8040 SATA Bridge or SATA connector is connected to Shasta SATA port 1.



PATA Termination



Sourced by host or bi-directional
Terminate near bridge

88SA8040 Config Straps (Device Mode):

T<1..0> - Vendor Unique (VU) and Read/Write Long

T<1..0>	VU Type	R/W Long Type
00	1	1
01	1	2
10	1	1 (default)
11	2	2

T2 - SSC Enable
1 - Enable SATA Spread Spectrum Clocking
0 - Disable SATA Spread Spectrum Clocking
(Internal Pull-down)

T<4..3> - Reference Clock Configuration

T<4..3>	Clock Frequency
00	20 MHz
01	25 MHz
10	30 MHz
11	40 MHz

(Internal Pull-downs)

T5 - Fixed UDMA
1 - UDMA mode fixed by CNFG<2..0> pins
0 - UDMA mode adjustable with Set Features
(Internal Pull-up)

T6 - Power Mode Enable
1 - Enable translation of ATA power management commands into SATA Partial or Slumber mode
0 - Disable translation
(Internal Pull-down)

T7 - Plug-in (output)
1 - SATA cable plugged in
0 - SATA cable unplugged
(Internal Pull-down)

CNFG<2..0> - Mode Configuration

CNFG<2..0>	Mode
000	Device Mode - 100MB/s
001	Device Mode - 133MB/s
010	Device Mode - 150MB/s (default)
100	Host Mode - 100MB/s
101	Host Mode - 133MB/s
110	Host Mode - 150MB/s
011	Reserved
111	Reserved

H_IOCS16_N - DMA_EN
1 - Good status on Set Features to set DMA
0 - Error status on Set Features to set DMA
(Internal Pull-up)

H_PDIAG_N - PATA_ORDER
1 - Reverse Order mode for Parallel ATA pins
0 - Normal Order mode

ATAIOSEL - ATA I/O Enable
1 - Enable output to ATA bus
0 - Disable output to ATA bus
(Internal Pull-up)

DRAWING
TITLE=FIZZY
ABBREV=DRAWING
LAST_MODIFIED=Mon Feb 23 19:07:28 2004

Master: Link

Serial ATA Bridge

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 81 OF 103	

Page Notes

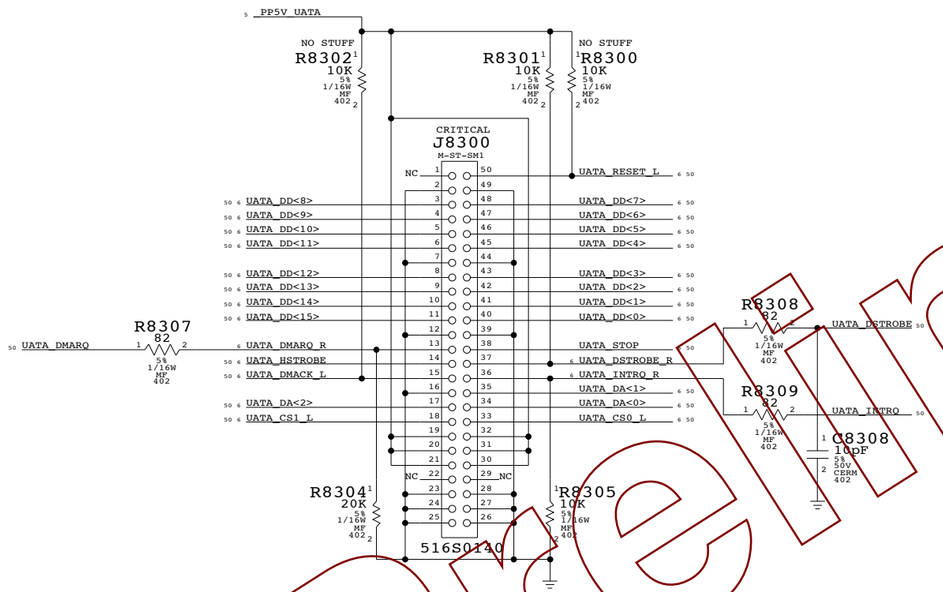
Power aliases required by this page:
- _PP5V_PATA
- _PP5V_UATA
- _PP3V3_PATA
- _PP3V3_UATA

Signal aliases required by this page:
(NONE)

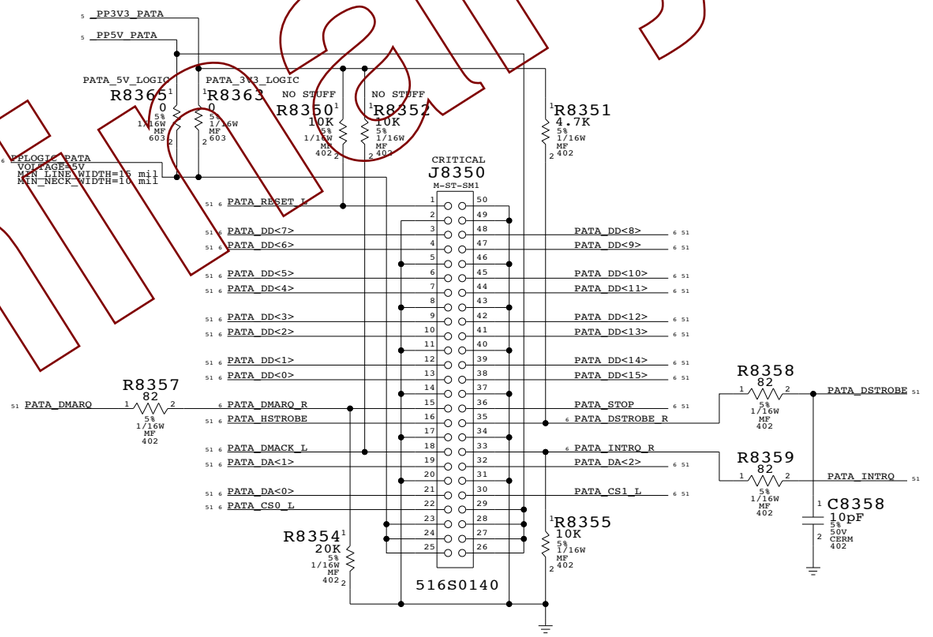
BOM options provided by this page:
(NONE)

NOTE: ATA constraints are expected to be defined on another page (ATA host) and apply to this page via XNets.

UATA (SouthBridge) Connector



PATA (SATA Bridge) Connector



DRAWING
TITLE=FIZZY
ABBREV=DRAWING
LAST_MODIFIED=Mon Feb 23 19:07:36 2004

IDE Connectors

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 83 OF 103	

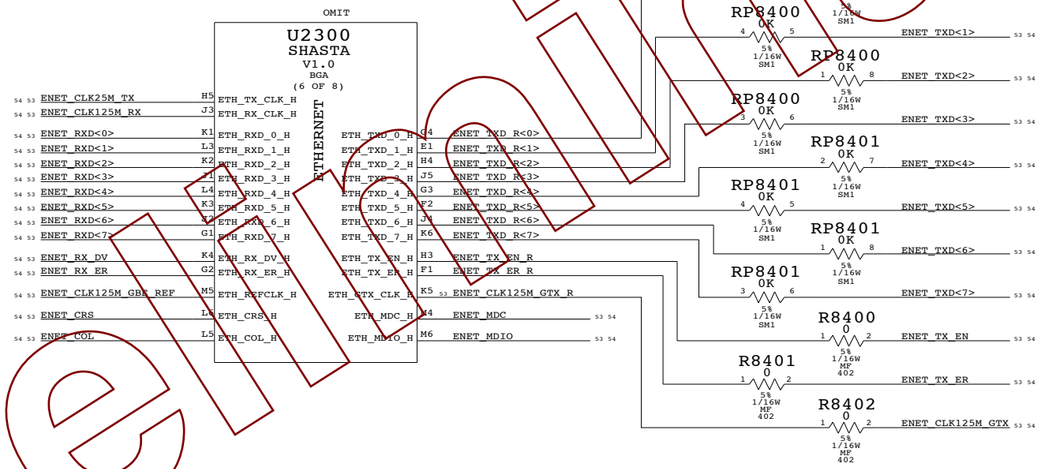
ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
ENET_RX_CLK	ENET	15_MIL_SPACING		ENET_CLK25M_TX 53 54
ENET_RX_CLK	ENET	15_MIL_SPACING		ENET_CLK125M_RX 53 54
ENET_GBE_REF	ENET	15_MIL_SPACING		ENET_CLK125M_GBE_REF 53 54
ENET_TX_CLK	ENET	15_MIL_SPACING		ENET_CLK125M_GTX 53 54
	ENET	15_MIL_SPACING		ENET_CLK125M_GTX_R 53
ENET_RX	ENET			ENET_RXD<7..0> 53 54
ENET_RX_CTL	ENET			ENET_RX_DV 53 54
ENET_RX_CTL	ENET			ENET_RX_ER 53 54
ENET_TX	ENET			ENET_TXD<7..0> 53 54
ENET_TX_CTL	ENET			ENET_TX_EN 53 54
ENET_TX_CTL	ENET			ENET_TX_ER 53 54
ENET_RX_CTL	ENET			ENET_CRS 53 54
ENET_RX_CTL	ENET			ENET_COL 53 54
ENET_MDC	ENET			ENET_MDC 53 54
ENET_MDIO	ENET			ENET_MDIO 53 54

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



DRAWING
TITLE=FIZZY
ABBREV=DRAWING
LAST_MODIFIED=Mon Feb 23 18:36:38 2004

Master: Link

Shasta Ethernet

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 84 OF 103	

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
	15 MIL SPACING		ENET_CLK125M_GBE_REF_R
	15 MIL SPACING		ENET_CLK125M_RX_R
	15 MIL SPACING		ENET_CLK25M_TX_R
ENET_MDI	ENET	ENET_MDI0	ENET_MDI_P<0>
ENET_MDI	ENET	ENET_MDI0	ENET_MDI_N<0>
ENET_MDI	ENET	ENET_MDI1	ENET_MDI_P<1>
ENET_MDI	ENET	ENET_MDI1	ENET_MDI_N<1>
ENET_MDI	ENET	ENET_MDI2	ENET_MDI_P<2>
ENET_MDI	ENET	ENET_MDI2	ENET_MDI_N<2>
ENET_MDI	ENET	ENET_MDI3	ENET_MDI_P<3>
ENET_MDI	ENET	ENET_MDI3	ENET_MDI_N<3>
VESTA_CLK25M_XTAL	15 MIL SPACING		VESTA_CLK25M_XTALI
	15 MIL SPACING		VESTA_CLK25M_XTALO
	15 MIL SPACING		VESTA_CLK25M_XTALO_R

Page Notes

Power aliases required by this page:
- _PP3V3_ENET
- _PP2V5_ENETFW
- _PP1V2_ENETFW

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Net Spacing Type: ENET

Line To Line: 15 mils
Length Tolerance: 50 mils
Primary Max Sep: 5 mils
Secondary Max Sep: 100 mils
Secondary Length: 500 mils

NOTE: Target differential impedance for ENET data pairs is 100 ohms.

Vesta Config Straps:

PHYA<4..0> - PHY Address Select
(Internal Pull-downs)

EN_10B - TBI Interface Select
1 - TBI/RTBI Mode
0 - GMII/RGMII Mode
(Internal Pull-down)

RGMIIEN - RGMII Enable
1 - RGMII/RTBI Mode
0 - GMII/TBI Mode
(Internal Pull-down)

FDX - Full-Duplex Select
Sets manual duplex mode bit
(Internal Pull-up)

F1000 - Speed Select
See table below
(Internal Pull-up)

SPD0 - Speed Select
See table below
(Internal Pull-down)

MANMS - Manual Master/Slave Configuration Select
Sets manual master/slave configuration enable bit
(Internal Pull-down)

HUB - Repeater Select
Sets Hub/DTE bit and master/slave configuration value bit
(Internal Pull-down)

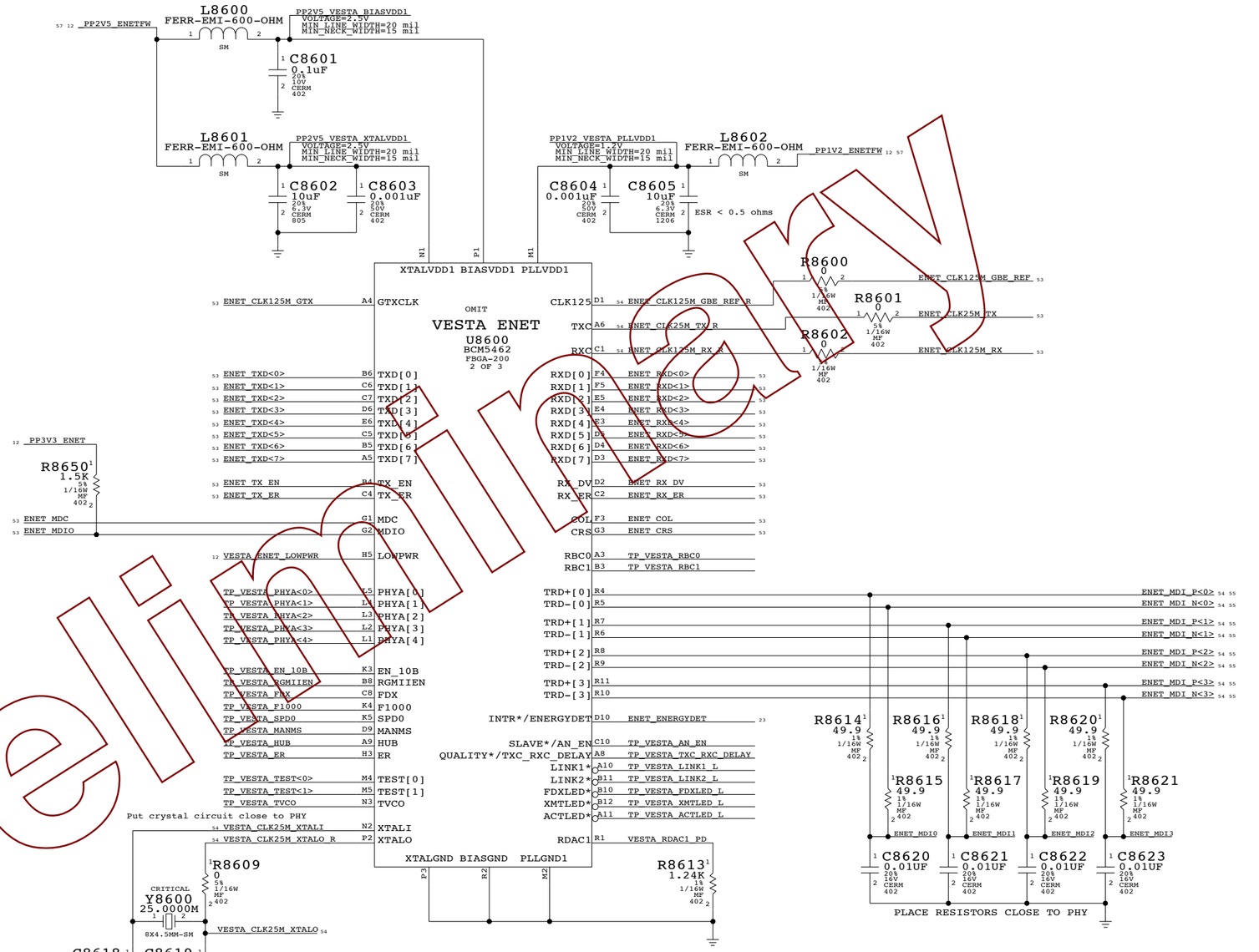
ER - Edge Rate Select
1 - Rise time approx. 5 ns
0 - Rise time approx. 4 ns
(Internal Pull-down)

AN_EN - Auto-Negotiation Select
1 - Auto-negotiation enabled
0 - Auto-negotiation disabled
(Internal Pull-up)

TXC_RXC_DELAY
1 - If RGMII Mode enabled, RXC clock and GTXCLK are delayed by 1.9 ns
0 - No clock delay
(Internal Pull-down)

AN_EN	F1000	SPD0	Description
0	0	0	Force 10BASE-T
0	0	1	Force 100BASE-TX
0	1	X	Force 1000BASE-T (test use only)
1	0	0	Auto-negotiate advertise 10BASE-T
1	0	1	Auto-negotiate advertise 10/100BASE-TX
1	1	0	Auto-negotiate advertise 10/100/1000BASE-T
1	1	1	Auto-negotiate advertise 1000BASE-T

DRAWING
TITLE=FIZZY
ABBREV=DRAWING
LAST_MODIFIED=Mon Feb 23 19:07:51 2004



Master: Link

Vesta Ethernet PHY

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 86 OF 103	

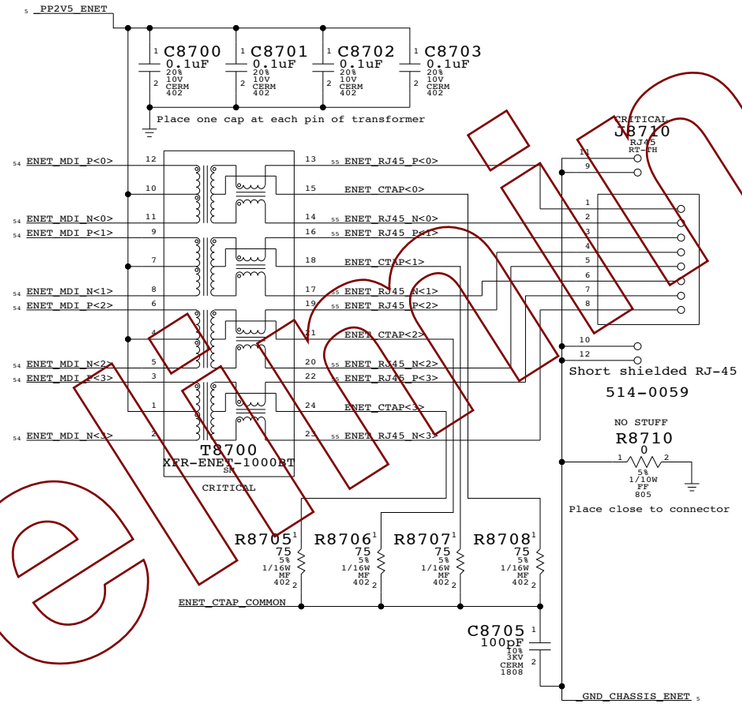
ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
PROVIDED BY ETHERNET PHY	ENET	ENET_RJ45_0	ENET_RJ45_P<0> 55
	ENET	ENET_RJ45_0	ENET_RJ45_N<0> 55
	ENET	ENET_RJ45_1	ENET_RJ45_P<1> 55
	ENET	ENET_RJ45_1	ENET_RJ45_N<1> 55
	ENET	ENET_RJ45_2	ENET_RJ45_P<2> 55
	ENET	ENET_RJ45_2	ENET_RJ45_N<2> 55
	ENET	ENET_RJ45_3	ENET_RJ45_P<3> 55
	ENET	ENET_RJ45_3	ENET_RJ45_N<3> 55

Page Notes

Power aliases required by this page:
- _PP2V5_ENET
- _GND_CHASSIS_ENET

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



DRAWING
TITLE=FIZZY
ABBREV=DRAWING
LAST_MODIFIED=Mon Feb 23 19:07:58 2004

Ethernet Connector

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 87 OF 103	

ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
FW	FW			FW_DATA<7..0> 56 57
FW	FW			FW_CTL<1..0> 56 57
FW_LPS	FW			FW_LPS 56 57
FW_LREQ	FW			FW_LREQ 56 57
FW_PINT	FW			FW_PINT 56 57
FW_LCLK	FW	15_MIL_SPACING		FW_CLK98M_LCLK 56 57
FW_PCLK	FW	15_MIL_SPACING		FW_CLK98M_PCLK 56 57
		15_MIL_SPACING		FW_CLK98M_LCLK_R 56

Page Notes

Power aliases required by this page:
- _PP2V5_PWRON_SB

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

45 23 21 5 _PP2V5_PWRON_SB

C8800 0.1uF 20% 10V CERM 402
C8801 0.1uF 20% 10V CERM 402
C8802 0.1uF 20% 10V CERM 402

U2300 OMIT
SHASTA
V1.0
BGA
(7 OF 8)
FWVDDP: N5, J7, A4

FIREWIRE

PHY_DATA_0_H	N4	FW_DATA<0>	56 57
PHY_DATA_1_H	P5	FW_DATA<1>	56 57
PHY_DATA_2_H	R1	FW_DATA<2>	56 57
PHY_DATA_3_H	M7	FW_DATA<3>	56 57
PHY_DATA_4_H	N6	FW_DATA<4>	56 57
PHY_DATA_5_H	L1	FW_DATA<5>	56 57
PHY_DATA_6_H	M3	FW_DATA<6>	56 57
PHY_DATA_7_H	L2	FW_DATA<7>	56 57
PHY_CTL_0_H	P2	FW_CTL<0>	56 57
PHY_CTL_1_H	N1	FW_CTL<1>	56 57
PHY_LPS_H	P6	FW_LPS	56 57
PHY_LREQ_H	P1	FW_LREQ	56 57
PHY_LCLK_H	R1	FW_CLK98M_LCLK_R	56
PHY_LINKON_L	N7	FW_LINKON	57

57 56 FW_CLK98M_PCLK → PHY_SCLK_H (P2)
57 56 FW_PINT → PHY_PINT_L (P3)

R8800 22 5% 1/16W MF 402
FW_CLK98M_LCLK_R → FW_CLK98M_LCLK 56 57

Master: Link

Shasta FireWire

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 88 OF 103	

DRAWING
TITLE=FIZZY
ABBREV=DRAWING
LAST_MODIFIED=Mon Feb 23 19:08:06 2004

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
(PROVIDED BY LINK PAGE)	15 MIL SPACING		FW_CLK98M_PCLK_R
FW_TPA1	FW	FW_TPA0	FW_TPA_P<0>
FW_TPA1	FW	FW_TPA0	FW_TPA_N<0>
FW_TPB1	FW	FW_TPB0	FW_TPB_P<0>
FW_TPB1	FW	FW_TPB0	FW_TPB_N<0>
FW_TPA2	FW	FW_TPA1	FW_TPA_P<1>
FW_TPA2	FW	FW_TPA1	FW_TPA_N<1>
FW_TPB2	FW	FW_TPB1	FW_TPB_P<1>
FW_TPB2	FW	FW_TPB1	FW_TPB_N<1>
FW_TPA3	FW	FW_TPA2	FW_TPA_P<2>
FW_TPA3	FW	FW_TPA2	FW_TPA_N<2>
FW_TPB3	FW	FW_TPB2	FW_TPB_P<2>
FW_TPB3	FW	FW_TPB2	FW_TPB_N<2>
VESTA_CLK24M_XTAL	15 MIL SPACING		VESTA_CLK24M_XTALI
	15 MIL SPACING		VESTA_CLK24M_XTALO
	15 MIL SPACING		VESTA_CLK24M_XTALO_R

Page Notes

Power aliases required by this page:
- _PPFW_PHY
- _PP3V3_FW
- _PP3V3_ENETFW
- _PP2V5_ENETFW
- _PP1V2_ENETFW

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- VESTA_DS_ONLY_EN0
  If stuffed, adds external pull-up to counter internal pull-down in Vesta. See straps table for more information.
- VESTA_PWR_CLASS_0
  If stuffed, adds external pull-down to counter internal pull-up in Vesta. See straps table for more information.

Net Spacing Type: FW

Line To Line:	15 mils
Length Tolerance:	100 mils
Primary Max Sep:	7.5 mils
Secondary Max Sep:	100 mils
Secondary Length:	500 mils

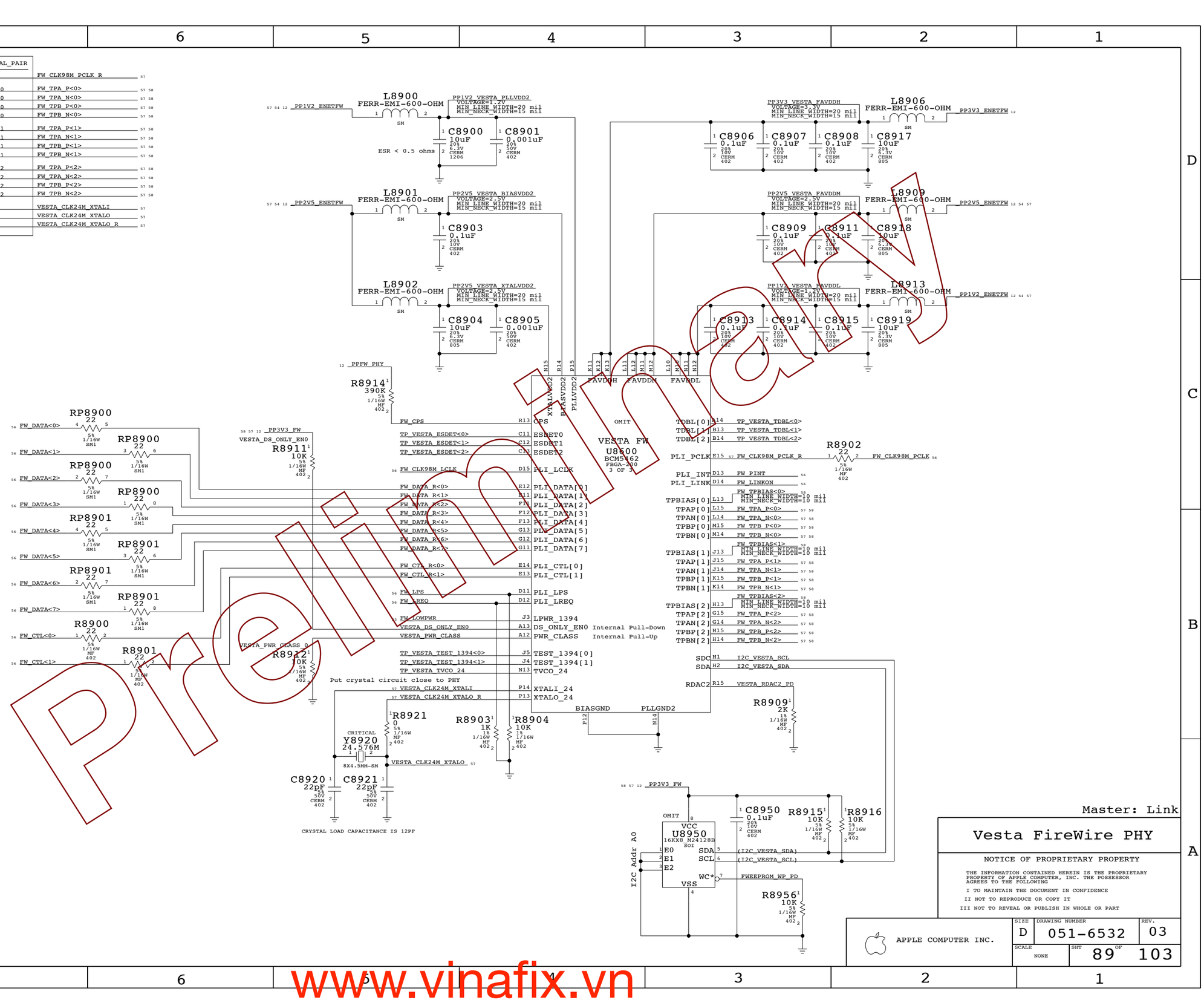
NOTE: Target differential impedance for FW data pairs is 110 ohms.

Vesta Config Straps:

PWR_CLASS - FireWire Power Class
1 - Sets Power Class to 0x4
0 - Sets Power Class to 0x0
(Internal Pull-up)

DS_ONLY_EN0 - Port 0 Data/Strobe
1 - Port 0 Data/Strobe mode only
0 - Port 0 Bilingual mode
(Internal Pull-down)

DRAWING
TITLE=FIZZY
ABBREV=DRAWING
LAST_MODIFIED=Mon Feb 23 19:08:14 2004



Master: Link

Vesta FireWire PHY

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 89 OF 103	

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
PROVIDED BY PHY PAGE	FW	FW_PORT1_TPA_FL	FW_PORT1_TPA_P_FL
	FW	FW_PORT1_TPA_FL	FW_PORT1_TPA_N_FL
	FW	FW_PORT1_TPB_FL	FW_PORT1_TPB_P_FL
	FW	FW_PORT1_TPB_FL	FW_PORT1_TPB_N_FL
	FW	FW_PORT2_TPA_FL	FW_PORT2_TPA_P_FL
	FW	FW_PORT2_TPA_FL	FW_PORT2_TPA_N_FL
	FW	FW_PORT2_TPB_FL	FW_PORT2_TPB_P_FL
	FW	FW_PORT2_TPB_FL	FW_PORT2_TPB_N_FL

Page Notes

Power aliases required by this page:
- _PPFW_PORT1
- _PPFW_PORT2
- _PPFW_PORT3
- _PP3V3_FW
- _GND_CHASSIS_FW_PORT1
- _GND_CHASSIS_FW_PORT2
- _GND_CHASSIS_FW_PORT3

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

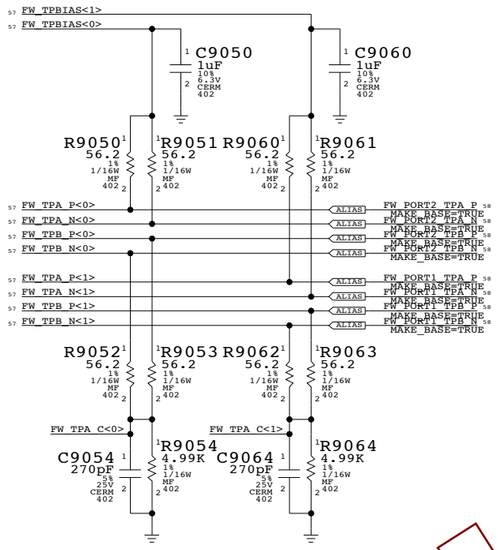
BOM options provided by this page:
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

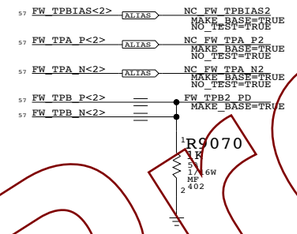
1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

Termination

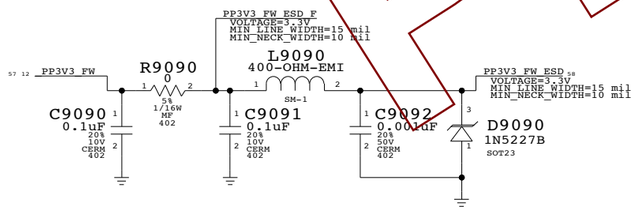
Place close to FireWire PHY



3rd TPA/TPB pair unused
(Is this correct for Vesta?)

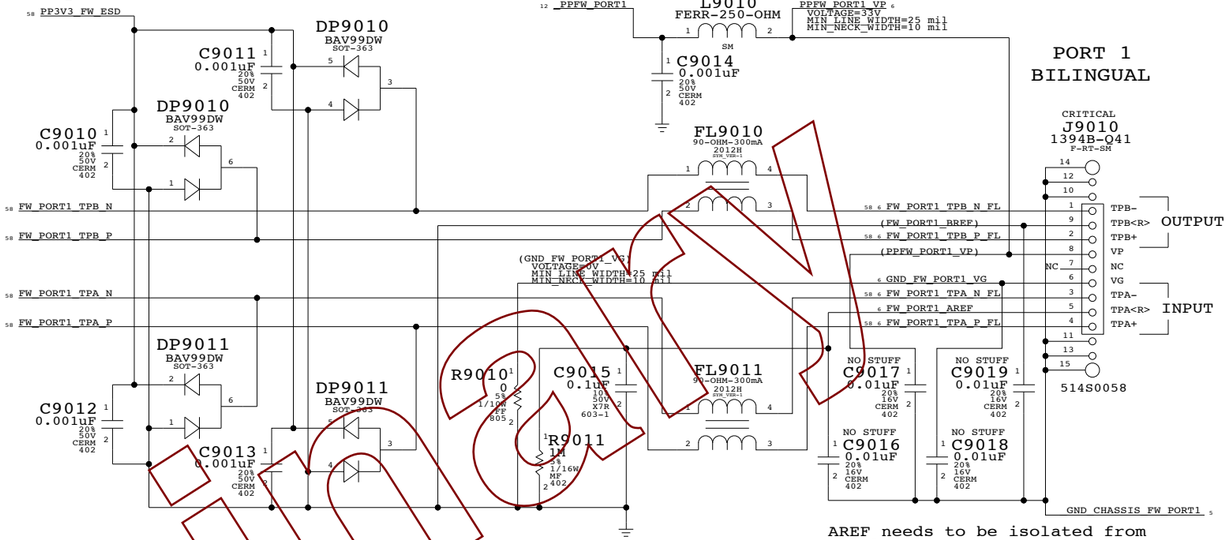


ESD Rail



Cable Power

"Snapback" & "Late VG" Protection

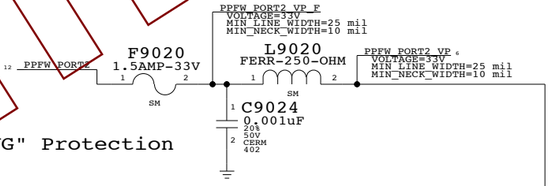


AREF needs to be isolated from all local grounds per 1394b spec

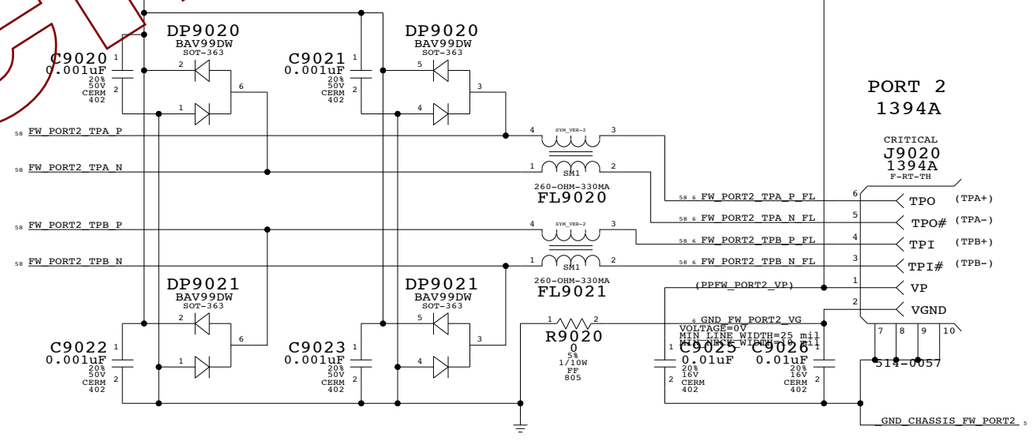
When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

BREF should be hard-connected to logic ground for speed signaling and connection detection currents per 1394b V1.33

Cable Power



"Snapback" & "Late VG" Protection



FireWire Ports

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 90 OF 103	

DRAWING
TITLE=FIZZY
ABBREV=DRAWING
LAST_MODIFIED=Mon Feb 23 19:08:30 2004

ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
USB2_0	USB2	USB2	USB2_0	USB2_P<0> 5 6 59
USB2_0	USB2	USB2	USB2_0	USB2_N<0> 5 6 59
USB2_1	USB2	USB2	USB2_1	USB2_P<1> 5 6 59
USB2_1	USB2	USB2	USB2_1	USB2_N<1> 5 6 59
USB2_2	USB2	USB2	USB2_2	USB2_P<2> 5 6 59
USB2_2	USB2	USB2	USB2_2	USB2_N<2> 5 6 59
USB2_3	USB2	USB2	USB2_3	USB2_P<3> 5 6 59
USB2_3	USB2	USB2	USB2_3	USB2_N<3> 5 6 59
USB2_4	USB2	USB2	USB2_4	USB2_P<4> 5 6 59
USB2_4	USB2	USB2	USB2_4	USB2_N<4> 5 6 59
USB2_NEC_XTAL		15_MIL_SPACING	NEC_CLK30M_XT1	59
		15_MIL_SPACING	NEC_CLK30M_XT2	59
		15_MIL_SPACING	NEC_CLK30M_XT2_R	59

Page Notes

Power aliases required by this page:
- _PP3V3_PWRON_USB

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Net Spacing Type: USB2

Line To Line: 19.5 mils
Length Tolerance: 50 mils
Primary Max Sep: 7.5 mils
Secondary Max Sep: 100 mils
Secondary Length: 500 mils

NOTE: Target differential impedance for USB2 data pairs is 90 ohms.

U2300 SHASTA V1.0 BGA (8 OF 8) OMIT

NC0	P7	TP_SB_NC_P7
NC1	P8	TP_SB_NC_P8
NC2	R3	TP_SB_NC_R3
NC3	R4	TP_SB_NC_R4
NC4	R5	TP_SB_NC_R5
NC5	R6	TP_SB_NC_R6
NC6	R7	TP_SB_NC_R7
NC7	R8	TP_SB_NC_R8
NC8	T1	TP_SB_NC_T1
NC9	T2	TP_SB_NC_T2
NC10	T3	TP_SB_NC_T3
NC11	T4	TP_SB_NC_T4
NC12	T5	TP_SB_NC_T5
NC13	T6	TP_SB_NC_T6
NC14	T7	TP_SB_NC_T7
NC15	T8	TP_SB_NC_T8
NC16	U1	TP_SB_NC_U1
NC17	U2	TP_SB_NC_U2
NC18	U3	TP_SB_NC_U3
NC19	U4	TP_SB_NC_U4
NC20	U5	TP_SB_NC_U5
NC21	U6	TP_SB_NC_U6
NC22	V1	TP_SB_NC_V1
NC23	V2	TP_SB_NC_V2
NC24	V3	TP_SB_NC_V3
NC25	V4	TP_SB_NC_V4
NC26	W1	TP_SB_NC_W1
NC27	W3	TP_SB_NC_W3
NC28	Y1	TP_SB_NC_Y1
NC29	Y3	TP_SB_NC_Y3

59 5 _PP3V3_PWRON_USB
L9135 FERR-EMI-100-OHM SM
PP3V3_PWRON_NEC_AVDD VOLTAGE=3.3V MIN_LINE_WIDTH=20 mil MIN_NECK_WIDTH=10 mil
R9135 4.7 5% 1/16W MF 603
C9135 10uF 20% 6.3V CERM 805
C9136 0.1uF 20% 10V CERM 402
C9137 0.1uF 20% 10V CERM 402
C9120 10uF 20% 6.3V CERM 805
C9121 0.1uF 20% 10V CERM 402
C9122 0.1uF 20% 10V CERM 402
C9123 0.1uF 20% 10V CERM 402
C9124 0.1uF 20% 10V CERM 402
C9125 0.1uF 20% 10V CERM 402
C9126 0.1uF 20% 10V CERM 402
C9127 0.1uF 20% 10V CERM 402
C9128 0.1uF 20% 10V CERM 402
C9129 0.1uF 20% 10V CERM 402
C9130 0.1uF 20% 10V CERM 402
P2 P3 P12 A13 A12 A3 B2 B8 L13 J13 H13 F13 D13 G12 H4 D7 VDD
N10 N12 AVDD

CRITICAL
U7700 NEC_uPD720101_USB2 FBGA

59 5 _PP3V3_PWRON_USB
R9110 10K 5% 1/16W MF 402
RP9110 10K 5% 1/16W SM1

6 5 USB2_OC<0>	(USB2_OC<0>)	B12	OCI1
6 5 USB2_OC<1>	(USB2_OC<1>)	B11	OCI2
5 USB2_OC<2>	(USB2_OC<2>)	B10	OCI3
5 USB2_OC<3>	(USB2_OC<3>)	A10	OCI4
5 USB2_OC<4>	(USB2_OC<4>)	E9	OCI5
6 5 USB2_PWREN<0>		C12	PPON1
6 5 USB2_PWREN<1>		A11	PPON2
5 USB2_PWREN<2>		C11	PPON3
5 USB2_PWREN<3>		E10	PPON4
5 USB2_PWREN<4>		A9	PPON5

59 5 _PP3V3_PWRON_USB
R9140 1.5K 5% 1/16W MF 402
R9141 1.5K 5% 1/16W MF 402
NEC_NC1_PU P6 NC1
NEC_NC2_PU M6 NC2

59 NEC_CLK30M_XT1 L9 XT1/SCLK
59 NEC_CLK30M_XT2_R P8 XT2
R9145 100 5% 1/16W MF 402
CRITICAL
Y9145 30.0000M 8X4.5MM-SM
NEC_CLK30M_XT2 59
C9145 22pF 5% 50V CERM 402
C9146 22pF 5% 50V CERM 402
Y9145 LOAD CAPACITANCE IS 16pF

VSS B1 N1 P13 N13 H1 B3 A2 D2 M2 K1 B13 M1 L12 H12 D12 G4 J1 F1 D8
R9139 0 5% 1/16W MF 603
AVSS AVSS(R) P1 R1 N11
Tie to GND at ball N11
GND_NEC_AVSS_R VOLTAGE=0V MIN_LINE_WIDTH=20 mil MIN_NECK_WIDTH=10 mil

RREF P11 NEC_RREF_PD
R9138 9.09K 1% 1/16W MF 402

RSDM1	M14	USB_NEC_N<0>	R9100 36 1% 1/16W MF 402	
DM1	M13	(USB2_N<0>)		USB2_N<0> 5 6 59
DP1	L14	(USB2_P<0>)		USB2_P<0> 5 6 59
RSDP1	K13	USB_NEC_P<0>	R9101 36 1% 1/16W MF 402	
RSDM2	K14	USB_NEC_N<1>	R9102 36 1% 1/16W MF 402	
DM2	K12	(USB2_N<1>)		USB2_N<1> 5 6 59
DP2	J14	(USB2_P<1>)		USB2_P<1> 5 6 59
RSDP2	J12	USB_NEC_P<1>	R9103 36 1% 1/16W MF 402	
RSDM3	H11	USB_NEC_N<2>	R9104 36 1% 1/16W MF 402	
DM3	G11	(USB2_N<2>)		USB2_N<2> 5 6 59
DP3	G13	(USB2_P<2>)		USB2_P<2> 5 6 59
RSDP3	G14	USB_NEC_P<2>	R9105 36 1% 1/16W MF 402	
RSDM4	F12	USB_NEC_N<3>	R9106 36 1% 1/16W MF 402	
DM4	F14	(USB2_N<3>)		USB2_N<3> 5 6 59
DP4	E12	(USB2_P<3>)		USB2_P<3> 5 6 59
RSDP4	E14	USB_NEC_P<3>	R9107 36 1% 1/16W MF 402	
RSDM5	E13	USB_NEC_N<4>	R9108 36 1% 1/16W MF 402	
DM5	D14	(USB2_N<4>)		USB2_N<4> 5 6 59
DP5	C13	(USB2_P<4>)		USB2_P<4> 5 6 59
RSDP5	C14	USB_NEC_P<4>	R9109 36 1% 1/16W MF 402	

DRAWING
TITLE=FIZZY
ABBREV=DRAWING
LAST_MODIFIED=Mon Feb 23 19:08:38 2004

Master: Fizzy

USB Host Interfaces

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 91 OF 103	

Page Notes

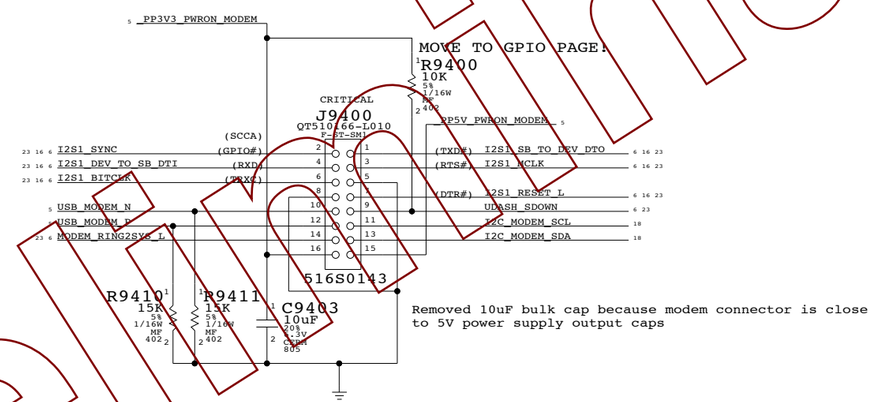
Power aliases required by this page:
- _PP3V3_PWRON_MODEM
  Spec Load: 0.5 A active, 3 mA auxiliary

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Modem Connector

Supports both The Last Dash and Q52 Modems



Removed 10uF bulk cap because modem connector is close to 5V power supply output caps

Modem Interface

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 94 OF 103	

_DRAWING
TITLE=FIZZY
ABBREV=DRAWING
LAST_MODIFIED=Mon Feb 23 19:08:46 2004

Page Notes

Power aliases required by this page:
- _PP5V_PWRON_AUDIO
- _PP3V3_PWRON_AUDIO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

NOTE: It is considered the responsibility of the audio section to provide the appropriate pull-ups and pull-downs for ALL audio GPIOs.

EMI Filtering

L9530 FERR-220-OHM 0402
23 I2S0_SYNC — I2S0_SYNC_F 6 61

L9531 FERR-220-OHM 0402
23 I2S0_MCLK — I2S0_MCLK_F 6 61

L9532 FERR-220-OHM 0402
23 I2S0_DEV_TO_SB_DTI — I2S0_DEV_TO_SB_DTI_F 6 61

L9533 FERR-220-OHM 0402
23 I2S0_SB_TO_DEV_DTO — I2S0_SB_TO_DEV_DTO_F 6 61

L9534 FERR-220-OHM 0402
23 6 AUDIO_SPKR_MUTE_L — AUDIO_SPKR_MUTE_L_F 61

L9535 FERR-220-OHM 0402
23 I2S0_RESET_L — I2S0_RESET_L_F 6 61

L9536 FERR-220-OHM 0402
23 I2S0_BITCLK — I2S0_BITCLK_F 6 61

L9537 FERR-220-OHM 0402
23 I2S2_SYNC — I2S2_SYNC_F 6 61

L9538 FERR-220-OHM 0402
23 I2S2_BITCLK — I2S2_BITCLK_F 6 61

L9539 FERR-220-OHM 0402
23 I2S2_DEV_TO_SB_DTI — I2S2_DEV_TO_SB_DTI_F 6 61

L9540 FERR-220-OHM 0402
23 I2S2_RESET_L — I2S2_RESET_L_F 6 61

Sound Board Connector

Place shorts at 3.3V and 5V regulators

XW9505 SM
5 _PP5V_PWRON_AUDIO — 6 PP5V_PWRON_AUDIO
VOLTAGE=5V
MIN_LINE_WIDTH=20 mil
MIN_NECK_WIDTH=10 mil
This is an internal board short

CRITICAL
J9500 QT500406-L111 M-ST-SM1

5 _PP5V_RUN_AUDIO

23 6	AUDIO_GPIO_11	AUDIO_LO_DET_L	6 23
23 6	AUDIO_EXT_MCLK_SEL	AUDIO_LO_OPTICAL_PLUG_L	6 23
23 6	AUDIO_LO_MUTE_L	AUDIO_LI_DET_L	6 23
		AUDIO_LI_OPTICAL_PLUG_L	6 23
		AUDIO_SPKR_MUTE_L_F	61
61 6	I2S0_MCLK_F		
61 6	I2S0_BITCLK_F	I2S0_RESET_L_F	6 61
61 6	I2S0_SYNC_F	I2S2_RESET_L_F	61
61 6	I2S0_SB_TO_DEV_DTO_F		
61 6	I2S0_DEV_TO_SB_DTI_F	I2C_AUDIO_SDA	18
		I2C_AUDIO_SCL	18
61 6	I2S2_BITCLK_F		
61 6	I2S2_SYNC_F	SLEEPLED_ANODE	6 19
61 6	I2S2_DEV_TO_SB_DTI_F	(SLEEP_LED_GND)	

516S0154

Place shorts at 3.3V and 5V regulators

XW9503 SM
6 PP3V3_PWRON_AUDIO — _PP3V3_PWRON_AUDIO 41
VOLTAGE=3.3V
MIN_LINE_WIDTH=20 mil
MIN_NECK_WIDTH=10 mil
This is an internal board short

Place ground short near 3.3V and 5V regulators

XW9500 SM
6 GND_AUDIO — 2 1
VOLTAGE=0V
MIN_LINE_WIDTH=20 mil
MIN_NECK_WIDTH=10 mil
This is an internal board short

Audio GPIO Pull-ups & Pull-downs

61 5 _PP3V3_PWRON_AUDIO

AUDIO_LO_DET_L - 100k PU on Kazoo (pg 6)
AUDIO_LO_OPTICAL_PLUG_L - 100k PU on Kazoo (pg 6)
AUDIO_LI_DET_L - 100k PU on Kazoo (pg 7)
AUDIO_LI_OPTICAL_PLUG_L - 100k PU on Kazoo (pg 8)

23 AUDIO_HP_DET_L — R9504 10K 5% 1/16W MF 402 — NO STUFF
23 AUDIO_SPKR_DET_L — R9515 10K 5% 1/16W MF 402 — R9505 10K 5% 1/16W MF 402

AUDIO_LO_MUTE_L - 100k PD on Kazoo (pg 6)

23 AUDIO_HP_MUTE_L — R9507 10K 5% 1/16W MF 402

AUDIO_SPKR_MUTE_L - 100k PD on Kazoo (pg 5)
AUDIO_EXT_MCLK_SEL - 100k PD on Kazoo (pg 8)
AUDIO_GPIO_11 - 100k PD on Kazoo (pg 8)

23 AUDIO_GPIO_12 — R9511 10K 5% 1/16W MF 402

I2S0_RESET_L - 100k PD on Kazoo (pg 4)
I2S2_RESET_L - 100k PD on Kazoo (pg 8)

DRAWING
TITLE=LINK
ABBREV=DRAWING
LAST_MODIFIED=Mon Feb 23 19:08:54 2004

Audio Interface

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 95 OF 103	

Electrical Constraints

No series termination on PCI signals

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
	RAM_CAD		RAM_DQS_R<15..0> 33 34
	RAM_CAD		RAM_DQ_R<127..0> 33 34
RAM_DQS0	RAM_CAD		RAM_DQS<0> 34 35
RAM_DQS0	RAM_CAD		RAM_DQ<7..0> 34 35
RAM_DQS1	RAM_CAD		RAM_DQS<1> 34 35
RAM_DQS1	RAM_CAD		RAM_DQ<15..8> 34 35
RAM_DQS2	RAM_CAD		RAM_DQS<2> 34 35
RAM_DQS2	RAM_CAD		RAM_DQ<23..16> 34 35
RAM_DQS3	RAM_CAD		RAM_DQS<3> 34 35
RAM_DQS3	RAM_CAD		RAM_DQ<31..24> 34 35
RAM_DQS4	RAM_CAD		RAM_DQS<4> 34 35
RAM_DQS4	RAM_CAD		RAM_DQ<39..32> 34 35
RAM_DQS5	RAM_CAD		RAM_DQS<5> 34 35
RAM_DQS5	RAM_CAD		RAM_DQ<47..40> 34 35
RAM_DQS6	RAM_CAD		RAM_DQS<6> 34 35
RAM_DQS6	RAM_CAD		RAM_DQ<55..48> 34 35
RAM_DQS7	RAM_CAD		RAM_DQS<7> 34 35
RAM_DQS7	RAM_CAD		RAM_DQ<63..56> 34 35
RAM_DQS8	RAM_CAD		RAM_DQS<8> 34 35
RAM_DQS8	RAM_CAD		RAM_DQ<71..64> 34 35
RAM_DQS9	RAM_CAD		RAM_DQS<9> 34 35
RAM_DQS9	RAM_CAD		RAM_DQ<79..72> 34 35
RAM_DQS10	RAM_CAD		RAM_DQS<10> 34 35
RAM_DQS10	RAM_CAD		RAM_DQ<87..80> 34 35
RAM_DQS11	RAM_CAD		RAM_DQS<11> 34 35
RAM_DQS11	RAM_CAD		RAM_DQ<95..88> 34 35
RAM_DQS12	RAM_CAD		RAM_DQS<12> 34 35
RAM_DQS12	RAM_CAD		RAM_DQ<103..96> 34 35
RAM_DQS13	RAM_CAD		RAM_DQS<13> 34 35
RAM_DQS13	RAM_CAD		RAM_DQ<111..104> 34 35
RAM_DQS14	RAM_CAD		RAM_DQS<14> 34 35
RAM_DQS14	RAM_CAD		RAM_DQ<119..112> 34 35
RAM_DQS15	RAM_CAD		RAM_DQS<15> 34 35
RAM_DQS15	RAM_CAD		RAM_DQ<127..120> 34 35

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
	RAM_CLK	RAM_CLK_A_R	RAM_CLK_A_P_R 33 34
	RAM_CLK	RAM_CLK_A_R	RAM_CLK_A_N_R 33 34
	RAM_CLK	RAM_CLK_B_R	RAM_CLK_B_P_R 33 34
	RAM_CLK	RAM_CLK_B_R	RAM_CLK_B_N_R 33 34
	RAM_CLK	RAM_CLK_D_R	RAM_CLK_D_P_R 33 34
	RAM_CLK	RAM_CLK_D_R	RAM_CLK_D_N_R 33 34
	RAM_CLK	RAM_CLK_E_R	RAM_CLK_E_P_R 33 34
	RAM_CLK	RAM_CLK_E_R	RAM_CLK_E_N_R 33 34
RAM_CLK0	RAM_CLK	RAM_CLK_A	RAM_CLK_A_P 34 35
RAM_CLK0	RAM_CLK	RAM_CLK_A	RAM_CLK_A_N 34 35
RAM_CLK0	RAM_CLK	RAM_CLK_B	RAM_CLK_B_P 34 35
RAM_CLK0	RAM_CLK	RAM_CLK_B	RAM_CLK_B_N 34 35
RAM_CLK1	RAM_CLK	RAM_CLK_D	RAM_CLK_D_P 34 35
RAM_CLK1	RAM_CLK	RAM_CLK_D	RAM_CLK_D_N 34 35
RAM_CLK1	RAM_CLK	RAM_CLK_E	RAM_CLK_E_P 34 35
RAM_CLK1	RAM_CLK	RAM_CLK_E	RAM_CLK_E_N 34 35
	RAM_CAD		RAM_CKE_R<1..0> 33 34
	RAM_CAD		RAM_CKE_R<5..4> 33 34
RAM_CKE0	RAM_CAD		RAM_CKE<0> 34 35
RAM_CKE0	RAM_CAD		RAM_CKE<1> 34 35
RAM_CKE1	RAM_CAD		RAM_CKE<4> 34 35
RAM_CKE1	RAM_CAD		RAM_CKE<5> 34 35
	RAM_CAD		RAM_CS_L_R<1..0> 33 34
	RAM_CAD		RAM_CS_L_R<9..8> 33 34
RAM_CS0	RAM_CAD		RAM_CS_L<0> 34 35
RAM_CS0	RAM_CAD		RAM_CS_L<1> 34 35
RAM_CS1	RAM_CAD		RAM_CS_L<8> 34 35
RAM_CS1	RAM_CAD		RAM_CS_L<9> 34 35
	RAM_CAD		RAM_A_R<13..0> 33 34
	RAM_CAD		RAM_BA_R<1..0> 33 34 62
	RAM_CAD		RAM_RAS_L_R 33 34 62
	RAM_CAD		RAM_CAS_L_R 33 34 62
	RAM_CAD		RAM_WE_L_R 33 34 62
RAM_A_CTL	RAM_CAD		RAM_A<13..0> 34 35
RAM_A_CTL	RAM_CAD		RAM_BA_R<1..0> 33 34 62
RAM_A_CTL	RAM_CAD		RAM_RAS_L_R 33 34 62
RAM_A_CTL	RAM_CAD		RAM_CAS_L_R 33 34 62
RAM_A_CTL	RAM_CAD		RAM_WE_L_R 33 34 62

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
	TMDS	TMDS_D0	TMDS_DP<0> 6 41 42
	TMDS	TMDS_D0	TMDS_DN<0> 6 41 42
	TMDS	TMDS_D1	TMDS_DP<1> 6 41 42
	TMDS	TMDS_D1	TMDS_DN<1> 6 41 42
	TMDS	TMDS_D2	TMDS_DP<2> 6 41 42
	TMDS	TMDS_D2	TMDS_DN<2> 6 41 42
	TMDS	TMDS_CLK	TMDS_CLKP 41 42
	TMDS	TMDS_CLK	TMDS_CLKN 41 42
	TMDS	TMDS_D3	TMDS_DP<3> 41 42
	TMDS	TMDS_D3	TMDS_DN<3> 41 42
	TMDS	TMDS_D4	TMDS_DP<4> 41 42
	TMDS	TMDS_D4	TMDS_DN<4> 41 42
	TMDS	TMDS_D5	TMDS_DP<5> 41 42
	TMDS	TMDS_D5	TMDS_DN<5> 41 42
	TMDS	CONN_TMDS_D0	TMDS_CONN_DP<0> 42
	TMDS	CONN_TMDS_D0	TMDS_CONN_DN<0> 42
	TMDS	CONN_TMDS_D1	TMDS_CONN_DP<1> 42
	TMDS	CONN_TMDS_D1	TMDS_CONN_DN<1> 42
	TMDS	CONN_TMDS_D2	TMDS_CONN_DP<2> 42
	TMDS	CONN_TMDS_D2	TMDS_CONN_DN<2> 42
	TMDS	CONN_TMDS_CLK	TMDS_CONN_CLKP 6 42
	TMDS	CONN_TMDS_CLK	TMDS_CONN_CLKN 6 42
	TMDS	CONN_TMDS_D3	TMDS_CONN_DP<3> 42
	TMDS	CONN_TMDS_D3	TMDS_CONN_DN<3> 42
	TMDS	CONN_TMDS_D4	TMDS_CONN_DP<4> 42
	TMDS	CONN_TMDS_D4	TMDS_CONN_DN<4> 42
	TMDS	CONN_TMDS_D5	TMDS_CONN_DP<5> 42
	TMDS	CONN_TMDS_D5	TMDS_CONN_DN<5> 42
	TMDS	SI_TMDS_D0	SI_TMDS_DP<0> 41
	TMDS	SI_TMDS_D0	SI_TMDS_DN<0> 41
	TMDS	SI_TMDS_D1	SI_TMDS_DP<1> 41
	TMDS	SI_TMDS_D1	SI_TMDS_DN<1> 41
	TMDS	SI_TMDS_D2	SI_TMDS_DP<2> 41
	TMDS	SI_TMDS_D2	SI_TMDS_DN<2> 41
	TMDS	SI_TMDS_CLK	SI_TMDS_CLKP 41
	TMDS	SI_TMDS_CLK	SI_TMDS_CLKN 41
	TMDS	SI_TMDS_D3	SI_TMDS_DP<3> 41
	TMDS	SI_TMDS_D3	SI_TMDS_DN<3> 41
	TMDS	SI_TMDS_D4	SI_TMDS_DP<4> 41
	TMDS	SI_TMDS_D4	SI_TMDS_DN<4> 41
	TMDS	SI_TMDS_D5	SI_TMDS_DP<5> 41
	TMDS	SI_TMDS_D5	SI_TMDS_DN<5> 41
	TMDS	GPU_TMDS_D0	GPU_TMDS_DP<0> 39 41
	TMDS	GPU_TMDS_D0	GPU_TMDS_DN<0> 39 41
	TMDS	GPU_TMDS_D1	GPU_TMDS_DP<1> 39 41
	TMDS	GPU_TMDS_D1	GPU_TMDS_DN<1> 39 41
	TMDS	GPU_TMDS_D2	GPU_TMDS_DP<2> 39 41
	TMDS	GPU_TMDS_D2	GPU_TMDS_DN<2> 39 41
	TMDS	GPU_TMDS_CLK	GPU_TMDS_CLKP 39 41
	TMDS	GPU_TMDS_CLK	GPU_TMDS_CLKN 39 41
	TMDS	GPU_TMDS_D0_R	GPU_TMDS_DP_R<0> 41
	TMDS	GPU_TMDS_D0_R	GPU_TMDS_DN_R<0> 41
	TMDS	GPU_TMDS_D1_R	GPU_TMDS_DP_R<1> 41
	TMDS	GPU_TMDS_D1_R	GPU_TMDS_DN_R<1> 41
	TMDS	GPU_TMDS_D2_R	GPU_TMDS_DP_R<2> 41
	TMDS	GPU_TMDS_D2_R	GPU_TMDS_DN_R<2> 41
	TMDS	GPU_TMDS_CLK_R	GPU_TMDS_CLKP_R 41
	TMDS	GPU_TMDS_CLK_R	GPU_TMDS_CLKN_R 41

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
EI_CPU_TO_NB_CLK			EI_CPU_TO_NB_CLK_P 26 27
EI_CPU_TO_NB_CLK			EI_CPU_TO_NB_CLK_N 26 27
EI_NB_TO_CPU_CLK			EI_NB_TO_CPU_CLK_P 26 27
EI_NB_TO_CPU_CLK			EI_NB_TO_CPU_CLK_N 26 27
EI_CPU_NB_DATA			EI_CPU_TO_NB_AD<43..0> 26 27
EI_NB_CPU_DATA			EI_NB_TO_CPU_AD<43..0> 26 27
EI_CPU_TO_NB_CAD			EI_CPU_TO_NB_SR_P<0> 26 27
EI_CPU_TO_NB_CAD			EI_CPU_TO_NB_SR_N<0> 26 27
EI_CPU_TO_NB_CAD			EI_CPU_TO_NB_SR_P<1> 26 27
EI_CPU_TO_NB_CAD			EI_CPU_TO_NB_SR_N<1> 26 27
EI_NB_TO_CPU_CAD			EI_NB_TO_CPU_SR_P<0> 26 27
EI_NB_TO_CPU_CAD			EI_NB_TO_CPU_SR_N<0> 26 27
EI_NB_TO_CPU_CAD			EI_NB_TO_CPU_SR_P<1> 26 27
EI_NB_TO_CPU_CAD			EI_NB_TO_CPU_SR_N<1> 26 27

45	PCI_SB_AD<0>	PCI_AD<0> 6 45 46 47 48 49
45	PCI_SB_AD<1>	PCI_AD<1> 6 45 46 47 48 49
45	PCI_SB_AD<2>	PCI_AD<2> 6 45 46 47 48 49
45	PCI_SB_AD<3>	PCI_AD<3> 6 45 46 47 48 49
45	PCI_SB_AD<4>	PCI_AD<4> 6 45 46 47 48 49
45	PCI_SB_AD<5>	PCI_AD<5> 6 45 46 47 48 49
45	PCI_SB_AD<6>	PCI_AD<6> 6 45 46 47 48 49
45	PCI_SB_AD<7>	PCI_AD<7> 6 45 46 47 48 49
45	PCI_SB_AD<8>	PCI_AD<8> 6 45 46 47 48 49
45	PCI_SB_AD<9>	PCI_AD<9> 6 45 46 47 48 49
45	PCI_SB_AD<10>	PCI_AD<10> 6 45 46 47 48 49
45	PCI_SB_AD<11>	PCI_AD<11> 6 45 46 47 48 49
45	PCI_SB_AD<12>	PCI_AD<12> 6 45 46 47 48 49
45	PCI_SB_AD<13>	PCI_AD<13> 6 45 46 47 48 49
45	PCI_SB_AD<14>	PCI_AD<14> 6 45 46 47 48 49
45	PCI_SB_AD<15>	PCI_AD<15> 6 45 46 47 48 49
45	PCI_SB_AD<16>	PCI_AD<16> 6 45 46 47 48 49
45	PCI_SB_AD<17>	PCI_AD<17> 6 45 46 47 48 49
45	PCI_SB_AD<18>	PCI_AD<18> 6 45 46 47 48 49
45	PCI_SB_AD<19>	PCI_AD<19> 6 45 46 47 48 49
45	PCI_SB_AD<20>	PCI_AD<20> 6 45 46 47 48 49
45	PCI_SB_AD<21>	PCI_AD<21> 6 45 47 48 49
45	PCI_SB_AD<22>	PCI_AD<22> 6 45 47 48 49
45	PCI_SB_AD<23>	PCI_AD<23> 6 45 47 48 49
45	PCI_SB_AD<24>	PCI_AD<24> 6 45 46 47 48 49
45	PCI_SB_AD<25>	PCI_AD<25> 6 45 46 47 48 49
45	PCI_SB_AD<26>	PCI_AD<26> 6 45 46 47 48 49
48 45	PCI_SB_AD<27>	PCI_AD<27> 6 45 46 47 48 49
45	PCI_SB_AD<28>	PCI_AD<28> 6 45 46 47 48 49
45	PCI_SB_AD<29>	PCI_AD<29> 6 45 46 47 48 49
45	PCI_SB_AD<30>	PCI_AD<30> 6 45 46 47 48 49
45	PCI_SB_AD<31>	PCI_AD<31> 6 45 46 47 48 49
45	PCI_SB_CBE_L<0>	PCI_CBE_L<0> 6 45 47 48 49
45	PCI_SB_CBE_L<1>	PCI_CBE_L<1> 6 45 47 48 49
45	PCI_SB_CBE_L<2>	PCI_CBE_L<2> 6 45 47 48 49
45	PCI_SB_CBE_L<3>	PCI_CBE_L<3> 6 45 47 48 49
45	PCI_SB_DEVSEL_L	PCI_DEVSEL_L 6 45 47 48 49
45	PCI_SB_FRAME_L	PCI_FRAME_L 6 45 47 48 49
45	PCI_SB_IRDY_L	PCI_IRDY_L 6 45 47 48 49
45	PCI_SB_TRDY_L	PCI_TRDY_L 6 45 47 48 49
45	PCI_SB_STOP_L	PCI_STOP_L 6 45 47 48 49
45	PCI_SB_PAR	PCI_PAR 6 45 47 48 49

ALIAS

MAKE_BASE=TRUE

DRAWING
TITLE=LINK
ABBREV=DRAWING
LAST_MODIFIED=Mon Feb 23 18:36:43 2004

Electrical Constraints

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE: NONE	SHT 99 OF 103	

*** Signal Cross-Reference for the entire design ***

```
1V2PWRON_ITH        9B6<>
1V2PWRON_ITH_RC     9A7<
1V2PWRON_MODE       9A6<>
1V2PWRON_PGOOD      9B4<>
1V2PWRON_RT         9B6<
1V2PWRON_RUNSS      9B6<>
1V2PWRON_SGND       9A6<>
1V2PWRON_SW         9B4<>
1V2PWRON_VFB        9A5<>
1V2PWRON_VFB_DIV    9A5<
1V2RUN_EN           9A2<> 14C6<
1V5PWRON_SW         9C5<>
1V5PWRON_VFB_DIV    9B5<
1V5RUN_EN           9C2<> 14C6<
1V8RUN_CC           9D5<>
1V8RUN_PGOOD        9D5<> 14B8<
1V8RUN_SHDN_L       9D6<> 14B6<
2V5NBVCORE_STBY_L   11C3< 14D6<
2V5PWRON_SW         11C3<>
2V5RUN_EN_L         11D2<> 14C6<
2V5_BOOST_ESR       11C3<>
2V5_BST_HI          11C4<>
2V5_BST_LO          11C4<>
2V5_FB              11C4<>
2V5_FB_RC           11B2<
2V5_HI_GATE         11C4<>
2V5_INV             11C4<
```

```
PCI_SLOTB_INT_L     23B3<> 23C2<
PCI_SLOTC_INT_L     23B2< 23B3<>
PCI_SLOTD_GNT_L     45A7< 45B5<>
PCI_SLOTD_INT_L     23A7< 23B3<>
PCI_SLOTD_REQ_L     45B5<> 45B7<
PCI_SLOTE_GNT_L     23A7< 23C3<> 49A6<
PCI_SLOTE_IDSEL     49B6<
PCI_SLOTE_INT_L     23A7< 23B3<> 49A6<>
PCI_SLOTE_REQ_L     23A7< 23C3<> 49A6>
PCI_SLOTF_GNT_L     23A7< 23C3<>
PCI_SLOTF_INT_L     23B2< 23B3<>
PCI_SLOTF_REQ_L     23A7< 23C3<>
PCI_SLOTG_GNT_L     45B5<> 45B7< 48B5<
PCI_SLOTG_IDSEL     48B5<
PCI_SLOTG_INT_L     23A7< 23B3<> 48B7<
PCI_SLOTG_REQ_L     45B5<> 45B7< 48B5>
PCI_STOP_L          6B8> 45A2< 45D6> 47B4<> 48B5<>
                    49A6<> 62B1>
PCI_TRDY_L          6B8> 45A2< 45D6> 47B4<> 48B5<>
                    49A6<> 62B1>
PLLLOCK             16A6< 27B6<>
PLLMULT             27B6<> 28B3<
PLLRANGE0           27B6<> 28B3<
PLLRANGE1           27B6<> 28B3<
PLLTEST             27B6<> 28A8<
PLLTESTOUT          27B6<> 28C4<
PLS_CLK_66M_0_R     25C4<>
PLS_CLK_66M_1_R     25C4<>
```

```
PPBATT_ALL_F          6A5> 7A7<
PPBATT_ALL_FUSEA      8C2<> 11A8<>
PPBATT_ALL_FUSEA_ZENER  11A7<>
PPBATT_ALL_FUSEB      8C1<>
PPBATT_ALL_VSNS       7A5< 8A5<
PPBATT_CHGR_OUT       8A3< 8C3<>
PPBATT_CHGR_RSNS      8B3<
PPBATT_CHGR_SW        8A4<>
PPBBATT_BOOST_OUT     11A8<> 17A4<>
PPBUS_ALL_A           5D7< 6A3> 6A7>
PPBUS_ALL_B           5D7< 6A3> 6B1>
PPDVO_GPU_VDDR4       40B2<
PPFW_COMBINED         12D5<> 12D5<>
PPFW_PORT2_VP_F       58B3<
PPLOGIC_PATA          6A5> 52C4<>
PPVCC_CBUS            49B1<> 49B2<> 49D1<>
PPVCORE_CPU           5C5> 27D4< 29A4< 29D5<> 30D7<
PPVCORE_GPU           5C5> 37A6< 39A3<> 39D4<
PPVCORE_GPUFB         5B6>
PPVCORE_GPUFB_VDDM    40B6<
PPVCORE_GPUFB_VDDRH   40C6<
```


APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE NONE	SHT 100	OF 103

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03

SCALE	SHT	OF
NONE	101	103

*** Part Cross-Reference for the entire design ***

BS510	PCB_STANDOFF	17
C700	CAP	7
C710	CAP	7
C720	CAP	7
C800	CAP	8
C801	CAP	8
C802	CAP	8
C805	CAP	8
C806	CAP	8
C807	CAP	8
C808	CAP	8
C811	CAP	8
C812	CAP	8
C813	CAP	8
C814	CAP	8
C815	CAP	8
C816	CAP	8
C817	CAP	8
C818	CAP_P	8
C820	CAP	8
C822	CAP	8
C823	CAP	8
C824	CAP	8
C825	CAP	8
C826	CAP	8
C827	CAP	8
C828	CAP	8
C829	CAP	8
C830	CAP	8
C831	CAP	8
C851	CAP	8
C860	CAP_P	17
C861	CAP_P	17
C862	CAP_P	17
C863	CAP_P	17
C864	CAP_P	17
C865	CAP_P	17
C882	CAP	8
C897	CAP	8
C940	CAP	9
C941	CAP	9
C942	CAP	9
C950	CAP	9
C951	CAP	9
C952	CAP	9
C953	CAP	9
C954	CAP	9
C955	CAP	9
C956	CAP	9
C957	CAP	9
C960	CAP	9
C961	CAP	9
C970	CAP	9
C971	CAP	9
C972	CAP	9
C980	CAP	9
C981	CAP	9
C1001	CAP_P	10
C1003	CAP	10
C1004	CAP_P	10
C1005	CAP	10
C1006	CAP	10
C1009	CAP	10
C1011	CAP	10
C1012	CAP	10
C1013	CAP_P	10
C1031	CAP	10
C1035	CAP	10
C1050	CAP	10
C1051	CAP	10
C1052	CAP	10
C1053	CAP	10
C1054	CAP	10
C1055	CAP	10
C1056	CAP	10
C1057	CAP	10
C1058	CAP	10
C1059	CAP	10
C1060	CAP	10
C1061	CAP	10
C1062	CAP	10
C1063	CAP	10
C1065	CAP	10
C1066	CAP	10
C1067	CAP	10
C1068	CAP	10
C1070	CAP	10
C1071	CAP	10
C1072	CAP	10
C1074	CAP_P	10
C1075	CAP_P	10
C1076	CAP	10
C1077	CAP	10
C1080	CAP	10
C1081	CAP	10
C1082	CAP	10
C1085	CAP	10
C1086	CAP	10
C1087	CAP_P	10
C1100	CAP	11
C1101	CAP	11
C1102	CAP	11
C1103	CAP	11
C1104	CAP	11
C1105	CAP	11
C1106	CAP	11
C1107	CAP	11
C1108	CAP	11
C1109	CAP	11
C1110	CAP	11
C1111	CAP	11
C1112	CAP	11
C1113	CAP	11
C1115	CAP	11
C1116	CAP	11
C1117	CAP	11
C1118	CAP	11
C1120	CAP	11
C1121	CAP	11
C1122	CAP	11
C1125	CAP_P	11
C1126	CAP	11
C1127	CAP	11
C1131	CAP	11
C1135	CAP	11
C1140	CAP	11
C1141	CAP	11
C1142	CAP	11
C1145	CAP	11
C1146	CAP	11
C1147	CAP_P	11
C1148	CAP_P	11
C1160	CAP	11
C1161	CAP	11
C1162	CAP	11
C1164	CAP	11
C1170	CAP	11
C1171	CAP	11
C1190	CAP	11
C1192	CAP	11
C1193	CAP_P	11
C1200	CAP	12
C1201	CAP	12
C1202	CAP	12
C1203	CAP	12
C1208	CAP	12
C1210	CAP	12
C1211	CAP	12
C1212	CAP	12
C1213	CAP	12
C1220	CAP	12
C1221	CAP	12
C1222	CAP	12
C1223	CAP	12
C1224	CAP	12
C1225	CAP	12
C1230	CAP	12
C1231	CAP	12
C1240	CAP	12
C1241	CAP	12
C1242	CAP	12
C1243	CAP	12
C1250	CAP	12
C1265	CAP	12
C1270	CAP	12
C1271	CAP_P	12
C1280	CAP	12
C1281	CAP	12
C1282	CAP	12
C1290	CAP	12
C1291	CAP	12
C1292	CAP	12
C1293	CAP	12
C1294	CAP	12
C1295	CAP	12
C1300	CAP	13
C1301	CAP	13
C1302	CAP	13
C1303	CAP	13
C1304	CAP	13
C1305	CAP	13
C1308	CAP	13
C1309	CAP	13
C1310	CAP	13
C1325	CAP	13
C1500	CAP	15
C1501	CAP	15
C1502	CAP	15
C1503	CAP	15
C1504	CAP	15
C1505	CAP	15
C1506	CAP	15
C1507	CAP	15
C1508	CAP	15
C1510	CAP	15
C1515	CAP	15
C1520	CAP	15
C1525	CAP	15
C1530	CAP	15
C1535	CAP	15
C1540	CAP	15
C1591	CAP	15
C1592	CAP	15
C1605	CAP	17
C1610	CAP	17
C2015	CAP	18
C2016	CAP	18
C2110	CAP	19
C2111	CAP	19
C2112	CAP	19
C2115	CAP	19
C2150	CAP	19
C2151	CAP	19
C2152	CAP	19
C2199	CAP	19
C2222	CAP	20
C2223	CAP	20
C2224	CAP	20
C2225	CAP	20
C2226	CAP	20
C2227	CAP	20
C2228	CAP	20
C2229	CAP	20
C2230	CAP	20
C2231	CAP	20
C2232	CAP	20
C2233	CAP	20
C2234	CAP	20
C2235	CAP	20
C2236	CAP	20
C2237	CAP	20
C2238	CAP	20
C2239	CAP	20
C2240	CAP	20
C2241	CAP	20
C2242	CAP	20
C2243	CAP	20
C2244	CAP	20
C2245	CAP	20
C2246	CAP	20
C2247	CAP	20
C2300	CAP	21
C2301	CAP	21
C2302	CAP	21
C2303	CAP	21
C2304	CAP	21
C2305	CAP	21
C2306	CAP	21
C2307	CAP	21
C2308	CAP	21
C2309	CAP	21
C2310	CAP	21
C2311	CAP	21
C2312	CAP	21
C2313	CAP	21
C2314	CAP	21
C2320	CAP	21
C2321	CAP	21
C2322	CAP	21
C2323	CAP	21
C2324	CAP	21
C2325	CAP	21
C2326	CAP	21
C2327	CAP	21
C2328	CAP	21
C2329	CAP	21
C2330	CAP	21
C2331	CAP	21
C2332	CAP	21
C2333	CAP	21
C2334	CAP	21
C2335	CAP	21
C2336	CAP	21
C2337	CAP	21
C2338	CAP	21
C2339	CAP	21
C2350	CAP	21
C2351	CAP	21
C2355	CAP	21
C2356	CAP	21
C2357	CAP	21
C2360	CAP	21
C2361	CAP	21
C2362	CAP	21
C2365	CAP	21
C2400	CAP	22
C2401	CAP	22
C2500	CAP	23
C2501	CAP	23
C2510	CAP	23
C2511	CAP	23
C2520	CAP	23
C2521	CAP	23
C2530	CAP	23
C2531	CAP	23
C2540	CAP	23
C2590	CAP	23
C2591	CAP	23
C2601	CAP	24
C2603	CAP	24
C2605	CAP	24
C2607	CAP	24
C2609	CAP	24
C2611	CAP	24
C2613	CAP	24
C2615	CAP	24
C2617	CAP	24
C2619	CAP	24
C2620	CAP	24
C2621	CAP	24
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C2625	CAP	24
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C2627	CAP	24
C2628	CAP	24
C2629	CAP	24
C2630	CAP	24
C2631	CAP	24
C2632	CAP	24
C2633	CAP	24
C2634	CAP	24
C2635	CAP	24
C2636	CAP	24
C2637	CAP	24
C2638	CAP	24
C2639	CAP	24
C2640	CAP	24
C2645	CAP	24
C2651	CAP	24
C2665	CAP	24
C2667	CAP	24
C2669	CAP	24
C2671	CAP	24
C2700	CAP	25
C2702	CAP	25
C2705	CAP	25
C2707	CAP	25
C2708	CAP	25
C2710	CAP	25
C2713	CAP	25
C2715	CAP	25
C2800	CAP	26
C2801	CAP	26
C2802	CAP	26
C2803	CAP	26
C2804	CAP	26
C2805	CAP	26
C2806	CAP	26
C2807	CAP	26
C2808	CAP	26
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C2810	CAP	26
C2811	CAP	26
C2812	CAP	26
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C2816	CAP	26
C2817	CAP	26
C2818	CAP	26
C2819	CAP	26
C2820	CAP	26
C2821	CAP	26
C2900	CAP	27
C2901	CAP	27
C2902	CAP	27
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C2956	CAP	27
C2957	CAP	27
C2958	CAP	27
C2959	CAP	27
C2960	CAP	27
C3100	CAP	29
C3101	CAP	29
C3102	CAP	29
C3103	CAP	29
C3104	CAP	29
C3105	CAP	29
C3106	CAP	29
C3107	CAP	29
C3108	CAP	29
C3109	CAP	29
C3110	CAP	29
C3111	CAP	29
C3112	CAP	29
C3113	CAP	29
C3114	CAP	29
C3115	CAP	29
C3116	CAP	29
C3117	CAP	29
C3118	CAP	29
C3119	CAP	29
C3120	CAP	29
C3121	CAP	29
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C3123	CAP	29
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C3131	CAP	29
C3132	CAP	29
C3133	CAP	29
C3134	CAP	29
C3135	CAP	29
C3136	CAP	29
C3137	CAP	29
C3138	CAP	29
C3139	CAP	29
C3140	CAP	29
C3141	CAP	29
C3142	CAP	29
C3143	CAP	29
C3144	CAP	29
C3145	CAP	29
C3146	CAP	29
C3147	CAP	29
C3148	CAP	29
C3149	CAP	29
C3150	CAP	29
C3199	CAP	29
C3200	CAP	30
C3201	CAP	30
C3202	CAP	30
C3203	CAP	30
C3204	CAP	30
C3205	CAP	30
C3206	CAP	30
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C3209	CAP	30
C3210	CAP	30
C3211	CAP	30
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C3248	CAP	30
C3249	CAP	30
C3250	CAP	30
C3251	CAP	30
C3252	CAP	30
C3253	CAP	30
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C3256	CAP	30
C3257	CAP	30
C3258	CAP	30
C3259	CAP	30
C3260	CAP	30
C3261	CAP	30
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C3264	CAP	30
C3265	CAP	30
C3266	CAP	30
C3267	CAP	30
C3268	CAP	30
C3269	CAP	30
C3270	CAP	30
C3271	CAP	30
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C3273	CAP	30
C3274	CAP	30
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C3279	CAP	30
C3280	CAP	30
C3281	CAP	30
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C3286	CAP	30
C3287	CAP	30
C3288	CAP	30
C3289	CAP	30
C3290	CAP	30
C3291	CAP	30
C3292	CAP	30
C3293	CAP	30
C3294	CAP	30
C3295	CAP	30
C3296	CAP	30
C3297	CAP	30
C3298	CAP	30
C3299	CAP	30
C3300	CAP	31
C3301	CAP	31
C3302	CAP	31
C3303	CAP	31
C3304	CAP	31
C3306	CAP	31
C3310	CAP	31
C3311	CAP	31
C3312	CAP	31
C3313	CAP	31
C3315	CAP	31
C3316	CAP	31
C3319	CAP	31
C3320	CAP	31
C3321	CAP	31
C3322	CAP	31
C3323	CAP	31
C3325	CAP	31
C3326	CAP	31
C3329	CAP	31
C3330	CAP	31
C3332	CAP	31
C3333	CAP	31
C3350	CAP	31
C3351	CAP	31
C3352	CAP	31
C3353	CAP	31
C3354	CAP	31
C3355	CAP	31
C3356	CAP	31
C3357	CAP	31
C3359	CAP	31
C3360	CAP_P	31
C3361	CAP_P	31
C3362	CAP_P	31
C3363	CAP_P	31
C3364	CAP_P	31
C3365	CAP_P	31
C3366	CAP_P	31
C3367	CAP_P	31
C3370	CAP	31
C3371	CAP	31
C3372	CAP	31
C3373	CAP	31
C3374	CAP	31
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C3376	CAP	31
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C3380	CAP	31
C3381	CAP	31
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C3383	CAP	31
C3384	CAP	31
C3385	CAP	31
C3386	CAP	31
C3387	CAP	31
C3388	CAP	31
C3389	CAP	31
C3391	CAP	31
C3392	CAP	31
C3393	CAP	31
C3394	CAP	31
C3395	CAP	31
C3396	CAP	31
C3397	CAP	31
C3398	CAP	31
C3399	CAP	31
C3630	CAP	32
C3631	CAP	32
C3636	CAP	32
C3639	CAP	32
C3640	CAP	32
C3650	CAP	32
C3651	CAP	32
C3660	CAP	32
C3669	CAP	32
C3670	CAP	32
C3671	CAP	32
C3676	CAP	32
C3679	CAP	32
C3698	CAP	32
C3699	CAP	32
C3700	CAP	33
C3701	CAP	33
C3702	CAP	33
C3703	CAP	33
C3704	CAP	33
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C3711	CAP	33
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C3716	CAP	33
C3717	CAP	33
C3718	CAP	33
C3719	CAP	33
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C3721	CAP	33
C3722	CAP	33
C3724	CAP	33
C3725	CAP	33
C3726	CAP	33
C3727	CAP	33
C3728	CAP	33
C3729	CAP	33
C3730	CAP	33
C3731	CAP	33
C3732	CAP	33
C3733	CAP	33
C3734	CAP	33
C3735	CAP	33
C3736	CAP	33
C3737	CAP	33
C3738	CAP	33
C3739	CAP	33
C3740	CAP	33
C3742	CAP	33
C3743	CAP	33
C3744	CAP	33
C3745	CAP	33
C3746	CAP	33
C3747	CAP	33
C3748	CAP	33
C4001	CAP	35
C4002	CAP	35
C4008	CAP	35
C4009	CAP	35
C4010	CAP	35
C4011	CAP	35
C4012	CAP	35
C4013	CAP	35
C4014	CAP	35
C4015	CAP	35
C4016	CAP	35
C4017	CAP	35
C4018	CAP	35
C4019	CAP	35
C4020	CAP	35
C4021	CAP	35
C4022	CAP	35
C4023	CAP	35
C4024	CAP	35
C4025	CAP	35
C4026	CAP	35
C4027	CAP	35
C4028	CAP	35
C4029	CAP	35
C4030	CAP	35
C4031	CAP	35
C4800	CAP	36
C4801	CAP	36
C4802	CAP	36
C4803	CAP	36
C4804	CAP	36
C4805	CAP	36
C4806	CAP	36
C4807	CAP	36
C4808	CAP	36
C4810	CAP	36
C4811	CAP	36
C4812	CAP	36
C4813	CAP	36
C4814	CAP	36
C4815	CAP	36
C4816	CAP	36
C4817	CAP	36
C4818	CAP	37
C4900	CAP	37
C4901	CAP	37
C4902	CAP	37
C4903	CAP	37
C4904	CAP	37
C4906	CAP	37
C4907	CAP	37
C4912	CAP	37
C4913	CAP	37
C4980	CAP	37
C4981	CAP	37
C4990	CAP	37
C4991	CAP	37
C5000	CAP	38
C5001	CAP	38
C5002	CAP	38
C5008	CAP	38
C5011	CAP	38
C5012	CAP	38
C5015	CAP	38
C5019	CAP	38
C5030	CAP	38
C5031	CAP	38
C5032	CAP	38
C5033	CAP	38
C5034	CAP	38
C5035	CAP_P	38
C5036	CAP_P	38
C5037	CAP_P	38
C5038	CAP	38
C5100	CAP	39
C5101	CAP	39
C5102	CAP	39
C5103	CAP	39
C5104	CAP	39
C5105	CAP	39
C5106	CAP	39
C5107	CAP	39
C5108	CAP	39
C5109	CAP	39
C5110	CAP	39
C5111	CAP	39
C5112	CAP	39
C5113	CAP	39
C5114	CAP	39
C5115	CAP	39
C5116	CAP	39
C5117	CAP	39
C5118	CAP	39
C5119	CAP	39
C5120	CAP	39
C5121	CAP	39
C5122	CAP	39
C5123	CAP	39
C5124	CAP	39
C5125	CAP	39
C5126	CAP	39
C5127	CAP	39
C5128	CAP	39
C5129	CAP	39
C5130	CAP	39
C5131	CAP	39
C5132	CAP	39
C5133	CAP	39
C5200	CAP	40
C5201	CAP	40
C5202	CAP	40
C5203	CAP	40
C5204	CAP	40
C5205	CAP	40
C5206	CAP	40
C5207	CAP	40
C5208	CAP	40
C5209	CAP	40
C5210	CAP	40
C5211	CAP	40
C5212	CAP	40
C5213	CAP	40
C5214	CAP	40
C5215	CAP	40
C5216	CAP	40
C5217	CAP	40
C5218	CAP	40
C5219	CAP	40
C5220	CAP	40
C5221	CAP	40
C5222	CAP	40
C5223	CAP	40
C5224	CAP	40
C5225	CAP	40
C5226	CAP	40
C5227	CAP	40
C5228	CAP	40
C5229	CAP	40
C5230	CAP	40
C5231	CAP	40
C5232	CAP	40
C5233	CAP	40
C5234	CAP	40
C5235	CAP	40
C5236	CAP	40
C5237	CAP	40
C5238	CAP	40
C5239	CAP	40
C5240	CAP	40
C5241	CAP	40
C5242	CAP	40
C5243	CAP	40
C5244	CAP	40
C5245	CAP	40
C5246	CAP	40
C5247	CAP	40
C5248	CAP	40
C5249	CAP	40
C5250	CAP	40
C5251	CAP	40
C5252	CAP	40
C5253	CAP	40
C5254	CAP	40
C5255	CAP	40
C5256	CAP	40
C5257	CAP	40
C5258	CAP	40
C5259	CAP	40
C5260	CAP	40
C5261	CAP	40
C5262	CAP	40
C5263	CAP	40
C5264	CAP	40
C5265	CAP	40
C5266	CAP	40
C5267	CAP	40
C5268	CAP	40
C5269	CAP	40
C5270	CAP	40
C5271	CAP	40
C5272	CAP	40
C5273	CAP	40
C5274	CAP	40
C5275	CAP	40
C5276	CAP	40
C5277	CAP	40
C5278	CAP	40
C5279	CAP	40
C5280	CAP	40
C5281	CAP	40
C5282	CAP	40
C5283	CAP	40
C5284	CAP	40
C5292	CAP	40
C5293	CAP	40
C5294	CAP	40
C5295	CAP	40
C5296	CAP	40
C5297	CAP	40
C5298	CAP	40
C5299	CAP	40
C5700	CAP	41
C5701	CAP	41
C5702	CAP	41
C5703	CAP	41
C5704	CAP	41
C5705	CAP	41
C5710	CAP	41
C5711	CAP	41
C5712	CAP	41
C5713	CAP	41
C5714	CAP	41
C5715	CAP	41
C5716	CAP	41
C5717	CAP	41
C5720	CAP	41
C5721	CAP	41
C5722	CAP	41
C5723	CAP	41
C5724	CAP	41
C5725	CAP	41
C5726	CAP	41
C5730	CAP	41
C5731	CAP	41
C5732	CAP	41
C5733	CAP	41
C5734	CAP	41
C5735	CAP	41
C5736	CAP	41
C5737	CAP	41
C5738	CAP	41
C5739	CAP	41
C5740	CAP	41
C5760	CAP	41
C5761	CAP	41
C5762	CAP	41
C5763	CAP	41
C5764	CAP	41
C5765	CAP	41
C5766	CAP	41
C5767	CAP	41
C5900	CAP	42
C5904	CAP	42
C5905	CAP	42
C5906	CAP	42
C5910	CAP	42
C5911	CAP	42
C5912	CAP	42
C5920	CAP	42
C5929	CAP	42
C5960	CAP	42
C5961	CAP	42
C5962	CAP	42
C5963	CAP	42
C5964	CAP	42
C5967	CAP	42
C5968	CAP	42
C5969	CAP	42
C5970	CAP	42
C5971	CAP	42
C5972	CAP	42
C5973	CAP	42
C5975	CAP	42
C5976	CAP	42
C5980	CAP	42
C5981	CAP	42
C5982	CAP	42
C5983	CAP	42
C5984	CAP	42
C5999	CAP	42
C6000	CAP	43
C6001	CAP	43
C6002	CAP	43
C6004	CAP	43
C6005	CAP	43
C6006	CAP	43
C6007	CAP	43
C6008	CAP	43
C6010	CAP	43
C6011	CAP	43
C6012	CAP	43
C6013	CAP	43
C6200	CAP	44
C6201	CAP	44
C6210	CAP	44
C6211	CAP	44
C6220	CAP	44
C6230	CAP	44
C6231	CAP	44
C6232	CAP	44
C6240	CAP	44
C6241	CAP	44
C6242	CAP	44
C6250	CAP	44
C6251	CAP	44
C6255	CAP	44
C7400	CAP	45
C7401	CAP	45
C7402	CAP	45
C7403	CAP	45
C7404	CAP	45
C7405	CAP	45
C7406	CAP	45
C7407	CAP	45
C7408	CAP	45
C7409	CAP	45
C7410	CAP	45
C7411	CAP	45
C7420	CAP	45
C7421	CAP	45
C7422	CAP	45
C7423	CAP	45
C7450	CAP	45
C7500	CAP	46
C7501	CAP	46
C7502	CAP	46
C7703	CAP	48
C7800	CAP	49
C7801	CAP	49
C7802	CAP	49
C7803	CAP	49
C7804	CAP	49
C7805	CAP	49
C7806	CAP	49
C7807	CAP	49
C7808	CAP	49
C7809	CAP	49
C7810	CAP	49
C7811	CAP	49
C8000	CAP	50
C8001	CAP	50
C8002	CAP	50
C8003	CAP	50
C8004	CAP	50
C8150	CAP	51
C8151	CAP	51
C8152	CAP	51
C8153	CAP	51
C8154	CAP	51
C8155	CAP	51
C8156	CAP	51
C8157	CAP	51
C8158	CAP	51
C8159	CAP	51
C8160	CAP	51
C8161	CAP	51
C8162	CAP	51
C8163	CAP	51
C8198	CAP	51
C8199	CAP	51
C8308	CAP	52
C8358	CAP	52
C8601	CAP	54
C8602	CAP	54
C8603	CAP	54
C8604	CAP	54
C8605	CAP	54
C8618	CAP	54
C8619	CAP	54
C8620	CAP	54
C8621	CAP	54
C8622	CAP	54
C8623	CAP	54
C8700	CAP	55
C8701	CAP	55
C8702	CAP	55
C8703	CAP	55
C8705	CAP	55
C8800	CAP	56
C8801	CAP	56
C8802	CAP	56
C8900	CAP	57
C8901	CAP	57
C8903	CAP	57
C8904	CAP	57
C8905	CAP	57
C8906	CAP	57
C8907	CAP	57
C8908	CAP	57
C8909	CAP	57
C8911	CAP	57
C8913	CAP	57
C8914	CAP	57
C8915	CAP	57
C8917	CAP	57
C8918	CAP	57
C8919	CAP	57
C8920	CAP	57
C8921	CAP	57
C8950	CAP	57
C9010	CAP	58
C9011	CAP	58
C9012	CAP	58
C9013	CAP	58
C9014	CAP	58
C9015	CAP	58
C9016	CAP	58
C9017	CAP	58
C9018	CAP	58
C9019	CAP	58
C9020	CAP	58
C9021	CAP	58
C9022	CAP	58
C9023	CAP	58
C9024	CAP	58
C9025	CAP	58
C9026	CAP	58
C9050	CAP	58
C9054	CAP	58
C9060	CAP	58
C9064	CAP	58
C9090	CAP	58
C9091	CAP	58
C9092	CAP	58
C9120	CAP	59
C9121	CAP	59
C9122	CAP	59
C9123	CAP	59
C9124	CAP	59
C9125	CAP	59
C9126	CAP	59
C9127	CAP	59
C9128	CAP	59
C9129	CAP	59
C9130	CAP	59
C9135	CAP	59
C9136	CAP	59
C9137	CAP	59
C9145	CAP	59
C9146	CAP	59
C9403	CAP	60
D790	DIODE_SCHOT	17
D800	DIODE	8
D810	DIODE_SCHOT	8
D1030	DIODE_SCHOT	10
D1031	DIODE_SCHOT	10
D1035	DIODE_SCHOT	10
D1036	DIODE_SCHOT	10
D1060	DIODE_SCHOT	10
D1110	DIODE_SCHOT	11
D1115	DIODE_SCHOT	11
D1130	DIODE_SCHOT	11
D1131	DIODE_SCHOT	11
D1135	DIODE_SCHOT	11
D1136	DIODE_SCHOT	11
D1160	DIODE_SCHOT	11
D1161	DIODE	11
D1162	DIODE_SCHOT	11
D1163	DIODE_SCHOT	11
D1164	DIODE_SCHOT	11
D1165	ZENER	11
D1265	DIODE_SCHOT	12
D1270	DIODE_SCHOT_3P2	12
D1271	DIODE_SCHOT	12
D1310	DIODE	13
D2150	DIODE_SCHOT	19
D3001	LED	16
D3002	LED	16
D3310	DIODE_3P_C	31
D3315	DIODE_SCHOT	31
D3320	DIODE_3P_C	31
D3325	DIODE_SCHOT	31
D3699	VREF_LM4050	32
D5011	DIODE_SCHOT	38
D5030	DIODE_SCHOT	38
D5900	DIODE_SCHOT	42
D9090	ZENER	58
DP800	DPAK3P	8
DP1260	DPAK3P	12
DP5190	DPAK3P	39
DP5290	DPAK3P	40
DP9010	DIODE_DUAL_6P	58
DP9011	DIODE_DUAL_6P	58
DP9020	DIODE_DUAL_6P	58
DP9021	DIODE_DUAL_6P	58
F895	FUSE	8
F899	FUSE	8
F1265	FUSE	12
F5900	FUSE	42
F9020	FUSE	58
FL5910	FILTER_LC	42
FL5911	FILTER_LC	42
FL5912	FILTER_LC	42
FL9010	FILTER_4P	58
FL9011	FILTER_4P	58
FL9020	FILTER_4P	58
FL9021	FILTER_4P	58
G4980	OSC	37
J700	CON_M4RT_S_SM	7
J750	CON_M10RT_S_SM	7
J790	CON_F14RT_S2MT_SM	17
J1591	CON_4RT_WRIB	15
J1592	CON_4RT_WRIB	15
J1600	CON_F14RT_S2MT_SM	17
J1699	CON_F16ST_D_SMA	16
J2130	CON_F14RT_S2MT_SM	17
J2700	CON_F1ST_S2MT_SM	25
J4010	CON_F200RT_DDRDIMM_SM1	35
J4020	CON_F200RT_DDRDIMM_SM2	35
J5900	CON_F30RT_T6MT_TH1	42
J5960	CON_F5RT_MINIDIN_TH	42
J5970	CON_F30RT_S2MT_SM	42
J5980	CON_4RT_WRIB	42
J7600	CON_M80ST_D2MT_SM	47
J7800	CON_M80ST_D4MT_SM	49
J8300	CON_M50SM_5MM	52
J8350	CON_M50SM_5MM	52
J8710	CON_RJ45_SHORT_4MT_TH	55
J9010	CON_F9RT_1394B_S6MT_SMA	58
J9020	CON_F6RT_S4MT_TH	58
J9400	CON_F16ST_D_SMA	60
J9500	CON_M40ST_D4MT_SM	61
L750	IND	7
L751	IND	7
L755	IND	7
L756	IND	7
L759	IND	7
L810	IND	8
L950	IND	9
L970	IND	9
L1060	IND	10
L1065	IND	10
L1110	IND	11
L1115	IND	11
L1200	IND	12
L1270	IND	12
L1290	IND	12
L2150	IND	19
L2199	IND	19
L2601	IND	24
L2603	IND	24
L2605	IND	24
L2607	IND	24
L2609	IND	24
L3101	IND	29
L3310	IND	31
L3320	IND	31
L4900	IND	37
L4980	IND	37
L4990	IND	37
L5030	IND_3P	38
L5126	IND	39
L5200	IND	40
L5201	IND	40
L5202	IND	40
L5203	IND	40
L5204	IND	40
L5205	IND	40
L5206	IND	40
L5207	IND	40
L5208	IND	40
L5209	IND	40
L5210	IND	40
L5211	IND	40
L5212	IND	40
L5213	IND	40
L5214	IND	40
L5280	IND	40
L5720	IND	41
L5730	IND	41
L5739	IND	41
L5900	IND	42
L5915	FILTER_4P	42
L5916	FILTER_4P	42
L5917	FILTER_4P	42
L5918	FILTER_4P	42
L5919	FILTER_4P	42
L5920	FILTER_4P	42
L5921	FILTER_4P	42
L5960	IND	42
L5961	IND	42
L5962	IND	42
L5963	IND	42
L5964	IND	42
L5975	IND	42
L5980	IND	42
L5981	IND	42
L5982	IND	42
L8155	IND	51
L8600	IND	54
L8601	IND	54
L8602	IND	54
L8900	IND	57
L8901	IND	57
L8902	IND	57
L8906	IND	57
L8909	IND	57
L8913	IND	57
L9010	IND	58
L9020	IND	58
L9090	IND	58
L9135	IND	59
L9530	IND	61
L9531	IND	61
L9532	IND	61
L9533	IND	61
L9534	IND	61
L9535	IND	61
L9536	IND	61
L9537	IND	61
L9538	IND	61
L9539	IND	61
L9540	IND	61
Q715	TRA_2N7002DW	7
Q720	TRA_SI4405DY	7
Q800	TRA_2N7002DW	8
Q810	TRA_SI4835BDY	8
Q811	TRA_MOSFET_NCHN_8P	8
Q850	TRA_SI4405DY	8
Q877	TRA_2N7002DW	8
Q880	TRA_SI4435DY	8
Q882	TRA_2N7002DW	8
Q890	TRA_SI4435DY	8
Q895	TRA_SUD45P03	8
Q899	TRA_SUD45P03	8
Q960	TRA_SI3446DV	9
Q980	TRA_SI3446DV	9
Q1003	TRA_SI3443DV	10
Q1004	TRA_SI3443DV	10
Q1007	TRA_SI3443DV	10
Q1060	TRA_IRF7821	10
Q1061	TRA_MOSFET_NCHN_8P	10
Q1065	TRA_SI4816DY	10
Q1110	TRA_IRF7821	11
Q1111	TRA_MOSFET_NCHN_8P	11
Q1115	TRA_SI7392DP	11
Q1116	TRA_MOSFET_NCHN_8P	11
Q1190	TRA_SI6467BDQ	11
Q1250	TRA_2N7002	12
Q1260	TRA_2N7002DW	12
Q1265	TRA_NDS9407	12
Q1400	TRA_2N7002DW	14
Q1435	TRA_2N7002DW	14
Q1510	TRA_2N3904	15
Q1515	TRA_2N3904	15
Q1520	TRA_2N3904	15
Q1525	TRA_2N3904	15
Q1530	TRA_2N3904	15
Q1535	TRA_2N3904	15
Q2000	TRA_2N7002DW	18
Q2191	TRA_2N7002DW	19
Q2199	TRA_2N3906	19
Q2404	TRA_2N7002DW	22
Q2407	TRA_2N7002	22
Q2408	TRA_SI2302DS	22
Q2409	TRA_2N7002DW	22
Q2412	TRA_2N7002DW	22
Q2576	TRA_2N3904	23
Q3001	TRA_2N3904	16
Q3002	TRA_2N3906	16
Q3003	TRA_2N3904	16
Q3004	TRA_2N7002	16
Q3309	TRA_2N7002	31
Q3310	TRA_SI7392DP	31
Q3312	TRA_MOSFET_NCHN_8P	31
Q3313	TRA_MOSFET_NCHN_8P	31
Q3320	TRA_SI7392DP	31
Q3322	TRA_MOSFET_NCHN_8P	31
Q3323	TRA_MOSFET_NCHN_8P	31
Q4801	TRA_2N7002DW	36
Q4802	TRA_2N3904	36
Q4803	TRA_2N7002	36
Q5030	TRA_SI7392DP	38
Q5031	TRA_MOSFET_NCHN_8P	38
Q5100	TRA_SI3446DV	39
Q5907	TRA_2N7002DW	42
Q5909	TRA_2N7002DW	19 42
Q5925	TRA_2N7002DW	42
Q5926	TRA_TP0610	42
Q5930	TRA_2N3904	42
Q5933	TRA_TP0610	42
Q5935	TRA_2N3904	42
Q5975	TRA_SI3443DV	42
Q5977	TRA_2N7002	42
Q5984	TRA_FDG6324L	42
R500	RES	5
R501	RES	5
R502	RES	5
R503	RES	5
R504	RES	5
R505	RES	5
R599	RES	5
R705	RES	7
R706	RES	7
R708	RES	7
R709	RES	7
R710	RES	7
R711	RES	7
R712	RES	7
R713	RES	7
R715	RES	7
R719	RES	7
R720	RES	7
R754	RES	7
R755	RES	7
R800	RES	8
R801	RES	8
R802	RES	8
R805	RES	8
R806	RES	8
R810	RES	8
R811	RES	8
R812	RES	8
R820	RES	8
R821	RES	8
R822	RES	8
R823	RES	8
R824	RES	8
R825	RES	8
R826	RES	8
R827	RES	8
R828	RES	8
R829	RES	8
R830	RES	8
R850	RES	8
R851	RES	8
R880	RES	8
R881	RES	8
R882	RES	8
R890	RES	8
R891	RES	8
R892	RES	8
R895	RES	8
R896	RES	8
R897	RES	8
R898	RES	8
R899	RES	8
R940	RES	9
R941	RES	9
R950	RES	9
R951	RES	9
R952	RES	9
R953	RES	9
R954	RES	9
R955	RES	9
R956	RES	9
R957	RES	9
R958	RES	9
R970	RES	9
R971	RES	9
R1031	RES	10
R1032	RES	10
R1033	RES	10
R1035	RES	10
R1036	RES	10
R1050	RES	10
R1052	RES	10
R1053	RES	10
R1070	RES	10
R1071	RES	10
R1072	RES	10
R1073	RES	10
R1080	RES	10
R1081	RES	10
R1082	RES	10
R1083	RES	10
R1100	RES	11
R1102	RES	11
R1103	RES	11
R1120	RES	11
R1121	RES	11
R1122	RES	11
R1123	RES	11
R1131	RES	11
R1132	RES	11
R1133	RES	11
R1135	RES	11
R1136	RES	11
R1140	RES	11
R1141	RES	11
R1142	RES	11
R1143	RES	11
R1161	RES	11
R1162	RES	11
R1163	RES	11
R1164	RES	11
R1166	RES	11
R1171	RES	11
R1250	RES	12
R1251	RES	12
R1260	RES	12
R1261	RES	12
R1262	RES	12
R1263	RES	12
R1265	RES	12
R1266	RES	12
R1290	RES	12
R1291	RES	12
R1293	RES	12
R1294	RES	[illegible]
R1295	RES	12
R1296	RES	12
R1297	RES	12
R1298	RES	[illegible]
R1300	RES	13
R1304	RES	13
R1310	RES	13
R1311	RES	13
R1312	RES	13

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE NONE	SHT 102	OF 103

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03

SCALE	SHT	OF
NONE	103	103