1. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.
2. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
3. ALL CAPACITANCE VALUES ARE IN MICROFARADS.

SANTANA - M51 MLB
DVT -- 06/29/06

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3 Power Block Diagram M51_PAUL 06/29/2006
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5 FUNC TEST 1 OF 2 M51_HENRY 06/29/2006
6 POWER CONN / MISC M51_PAUL 06/29/2006
7 CPU 1 OF 2-FSB M50_HENRY 06/29/2006
8 CPU 2 OF 2-PWR/GND M50_HENRY 06/29/2006
9 CPU DECAPS & VICT< M51_HENRY 06/29/2006
10 ASIC TEMP SENSORS M51_DAVE (MASTER)
11 CPU ITP700FX DEBG M50_HENRY 06/29/2006
12 NB CPU Interface M50_HENRY 06/29/2006
13 NB Misc / Video Interface M50_HENRY 06/29/2006
14 NB Misc Interfaces M50_HENRY 06/29/2006
15 NB DDR2 Interfaces M50_HENRY 06/29/2006
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17 NB Power 2 M50_HENRY 06/29/2006
18 NB Grounds M50_HENRY 06/29/2006
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20 NB Config Straps M50_HENRY 06/29/2006
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22 SB: 2 OF 4 M50_Doug 06/29/2006
23 SB: 3 OF 4 M50_Doug 06/29/2006
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50 TPM M51_HENRY 06/29/2006
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53 AUDIO: COMBO OUT AMP AUDIO 06/29/2006
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66 XM PCI-E & PWR M51_DAVE (MASTER)
67 XM I/O M51_DAVE (MASTER)
68 Internal Display Conn M51_DAVE (MASTER)
69 External Display Conn M51_DAVE (MASTER)
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TO MAINTAIN THE DOCUMENT IN CONFIDENCE
### Production BOM

<table>
<thead>
<tr>
<th>PART NUMBER</th>
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<th>QTY</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
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### Development BOM

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<tr>
<td>M51_COMMON</td>
<td>M51_BEST, M51_DEV, ALTERNATE</td>
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### BarCode Label / EEE #'s

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### Module Parts

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### SENSOR STUFFING OPTIONS

When Development Sensors are on board, pull-up/ull-downs for unused pins.

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###小微部分

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</tbody>
</table>
ON L8 (NORTH SIDE SECONDARY) PLACE INSIDE SOCKET CAVITY

SOUTH SIDE SECONDARY CAVITY ON L1 (SOUTH SIDE PRIMARY)

We had a 330UF elec cap here for 1.05V rail - check we can remove

VCCP CORE DECOUPLING
PLACE IN SIDE SOCKET (ON SOUTH SIDE SECONDARY)

NEED LARGE RAIL FOR 1.05V

VCC CORE DECOUPLING
PLACE IN SIDE SOCKET (ON SOUTH SIDE SECONDARY)

NEED LARGE RAIL FOR 1.05V

CPU DECAPS & VID<>
CPU ITP700FLEX DEBUG SUPPORT

ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S TCK PIN AND THEN PULL BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX CONNECTOR'S PROD PIN.

SYNC_DATE=06/29/2006
SYNC_MASTER=M50_HENRY
=PP1V05_S0_CPU
=PP3V3_S5_SB_PM

XDP_TCK
XDP_TDI
XDP_TDO
XDP_BPM_L<0>
XDP_BPM_L<1>
XDP_BPM_L<2>
XDP_BPM_L<3>
XDP_BPM_L<4>
XDP_BPM_L<5>

(AND WITH RESET BUTTON)
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NB_CFG<11>

Internal pull-ups

RESERVED

NB_CFG<12>

High = Mobile CPU

Low = Normal

NB_CFG<13:12>

Lane Reversal

NB_CFG<15>

Reserved

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NOTE: ENABLE INTERNAL 1.05V SUSPEND REG

- LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR
- BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED

INTERNAL 20K PD ENABLED WHEN AC '07

BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED

NONE

INTERNAL 20K PD ONLY ENABLED IN S3COLD

NOTE: EE_CS HAS INTERNAL PD, ONLY ENABLED WHEN LAN_RST#=L
One cap for each side of every RPAK, one cap for every two discrete resistors. 

ERROR! shown at the top of each group applies to every part below it.
 DDR2 Vtt Regulator

MemVTT_EN can be used to disable MemVTT in sleep.

If power inputs are not 5V, MemVTT_EN can be used to disable MemVTT in sleep.

Can 5V be 3.3V if 1V8 is 3.3V?

- =PP0V9_S0_MEMVTT
- =PP1V8_S0_MEMVTT
- =PP5V_S0_MEMVTT

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- =PP0V9_S0_MEMVTT_LDO

Using 1% FR BOM CONSOLIDATION

BOM options provided by this page:
- =PP0V9_S0_MEMVTT
- =PP1V8_S0_MEMVTT
- =PP5V_S0_MEMVTT

Memory Vtt Supply

Sync_master=M50_Henry
Sync_date=06/29/2006

www.vinafix.vn
IT IS 2.2V INSTEAD OF 2.7V BECAUSE THE SNAPBACK ESD DIODES HAVE A .5V DROP.

44
3
=PP3V3_S5_FW
44
8
15 WATTS MAX
24 VOLTS

FW_B_TPB_P
FW_A_TPB_N
FW_A_TPA_N
VOLTAGE=1.86V
FW_A_TPBIAS
FW_B_TPBIAS
18nH-15mA
VOLTAGE=0V
NO_TEST=TRUE
NO_TEST=TRUE
VOLTAGE=3.3V
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=33V
MIN_LINE_WIDTH=1.7MM
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=33V
MIN_LINE_WIDTH=1.7MM
CRITICAL
CRITICAL
CRITICAL

NOTE: TI RECOMMENDS THIS FOR UNCONNECTED PORTS

MIN_NECK_WIDTH=0.25 mm
VOLTAGE=6.3V
10%
R4660
R4662
R4661
CRITICAL
CRITICAL
CRITICAL

NOTE: TI PHY REQUIRES 1uF EVEN THOUGH SPEC CALLS OUT .33uF

FERR-250-OHM
SM-1

ORIGNAL TOKO CHOKE

www.vinafix.vn
PCI-E X1 PORT "A" = ETHERNET (YUKON)
- PCI-E X1 PORT "A" = ETHERNET (YUKON)
- PCI-E X1 PORT "A" = ETHERNET (YUKON)
- PCI-E X1 PORT "A" = ETHERNET (YUKON)
- PCI-E X1 PORT "A" = ETHERNET (YUKON)
- PCI-E X1 PORT "A" = ETHERNET (YUKON)
- PCI-E X1 PORT "A" = ETHERNET (YUKON)
- PCI-E X1 PORT "A" = ETHERNET (YUKON)

PCI-E X1 PORT "B" = MINI CARD (AIRPORT)
- PCI-E X1 PORT "B" = MINI CARD (AIRPORT)
- PCI-E X1 PORT "B" = MINI CARD (AIRPORT)
- PCI-E X1 PORT "B" = MINI CARD (AIRPORT)
- PCI-E X1 PORT "B" = MINI CARD (AIRPORT)
- PCI-E X1 PORT "B" = MINI CARD (AIRPORT)

PCI-E X1 PORTS C, D, E, F = UNUSED
- PCI-E X1 PORTS C, D, E, F = UNUSED
- PCI-E X1 PORTS C, D, E, F = UNUSED
- PCI-E X1 PORTS C, D, E, F = UNUSED
- PCI-E X1 PORTS C, D, E, F = UNUSED
- PCI-E X1 PORTS C, D, E, F = UNUSED
- PCI-E X1 PORTS C, D, E, F = UNUSED
- PCI-E X1 PORTS C, D, E, F = UNUSED
R6306-07 SHOULD BE PLACED LESS THAN 2.54MM FROM U2100
R6303 SHOULD BE PLACED LESS THAN 2.54MM FROM U6301
4.5V POWER SUPPLY FOR CODEC AND LINE IN AMP

MIC INPUT TO BOTH L&R
GAIN SETTINGS: +16dB
MODULATION SETTING: LOW EMI
GAIN AND SWITCHING FREQUENCY STUFF OPTIONS
--- PPV3 &G AUDIO
--- PPV3 &G AUDIO
CPU CURRENT SENSE CALIBRATION CIRCUIT

Switches in fixed load on power supplies to calibrate current sense circuits

SYSTEM CURRENT SENSE

SYSTEM VOLTAGE SENSE

CPU & SYSTEM SENSE

APP CATION INC.

www.vinafix.vn
DVI DDC CURRENT LIMIT

DVI INTERFACE

PLC CLOSE TO MINI-DVI CONNECTOR

3V LEVEL SHIFTERS

ANALOG FILTERING

PLACE CLOSE TO CONNECTOR

External Display Conns

APPLE COMPUTER INC.

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