

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SANTANA - M51 MLB

EVT -- 05/19/06

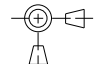
REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
17		440406	ENGINEERING RELEASED	05/19/06	06/22/04

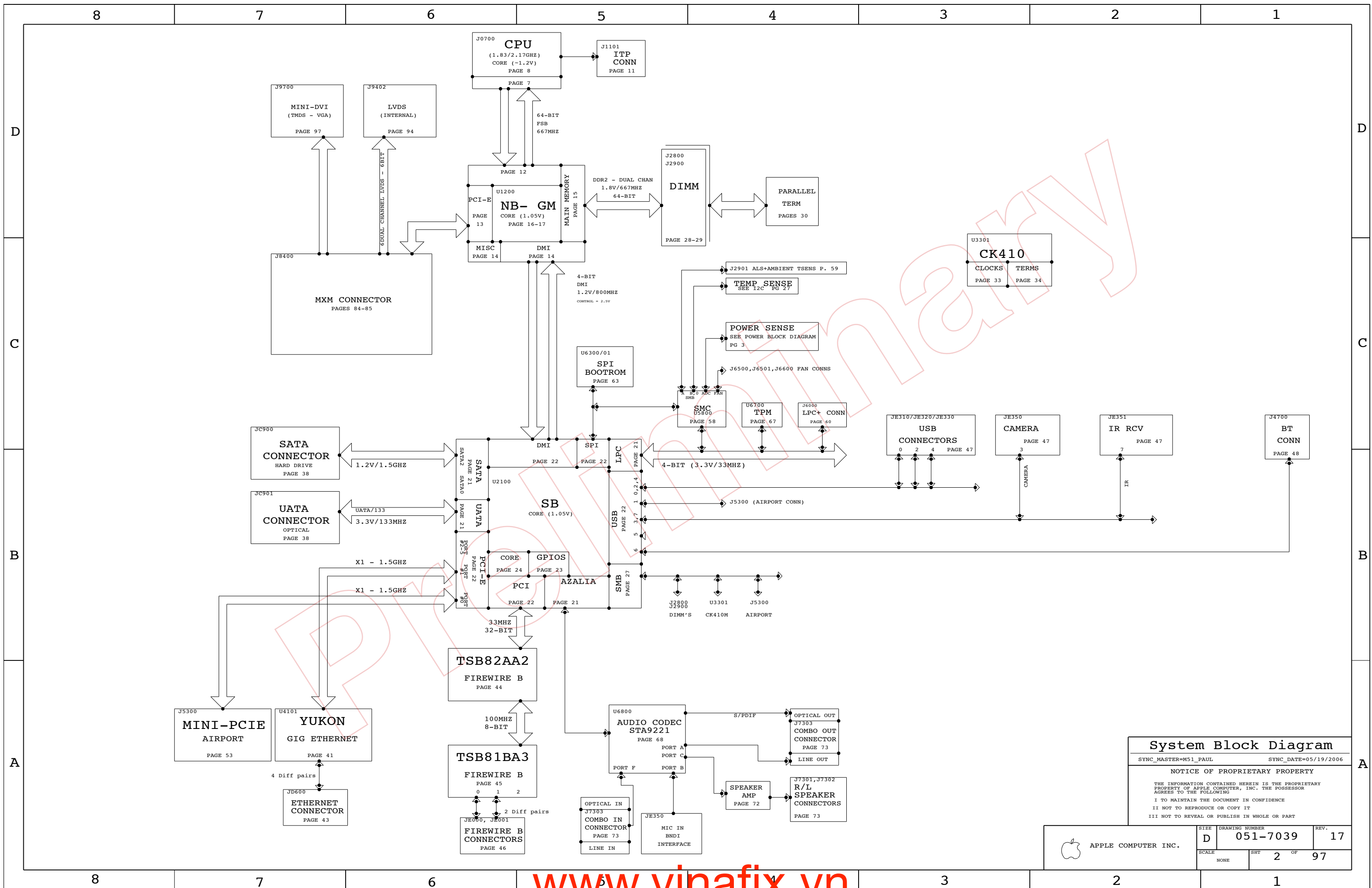
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47	63	SPI BOOTROM	M50_DOUG	05/19/2006
48	65	HD AND OD FAN	M51_HENRY	05/19/2006
49	66	CPU FAN, HD & OD TEMP	M51_HENRY	05/19/2006
50	67	TPM	M50_HENRY	05/19/2006
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52	69	AUDIO: LINE INPUT AMP	AUDIO	05/19/2006
53	70	AUDIO: COMBO OUT AMP	AUDIO	05/19/2006
54	71	AUDIO: SPEAKER AMP_1	AUDIO	05/19/2006
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62	79	1.8V & 1.2V VREG	M51_PAUL	05/19/2006
63	80	1.5V_S0 & 1.05V_S0 VREG	M51_PAUL	05/19/2006
64	82	5V DC/DC	M50_PAUL	05/19/2006
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66	84	MXM PCI-E & PWR	M51_DAVE (MASTER)	
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68	94	Internal Display Conns	M51_DAVE (MASTER)	
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Schematic / PCB #'s

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-7039	1	PCB, SCHEM, MLB, M51	SCH1		
820-1984	1	PCB, FAB, MLB, M51	MLB1		

DIMENSIONS ARE IN MILLIMETERS		METRIC		Apple Computer Inc.	
xx : _____		DRAPFER	DESIGN CK	NOTICE OF PROPRIETARY PROPERTY THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THE DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART	
x.xx : _____		ENG APPD	MFG APPD		
x.xxx : _____		QA APPD	DESIGNER		
ANGLES : _____		RELEASE	SCALE		
DO NOT SCALE DRAWING		SCALE NONE		TITLE	
 THIRD ANGLE PROJECTION		MATERIAL/FINISH NOTED AS APPLICABLE		SIZE D	DRAWING NUMBER 051-7039
				REV. 17	SHT 1 OF 97



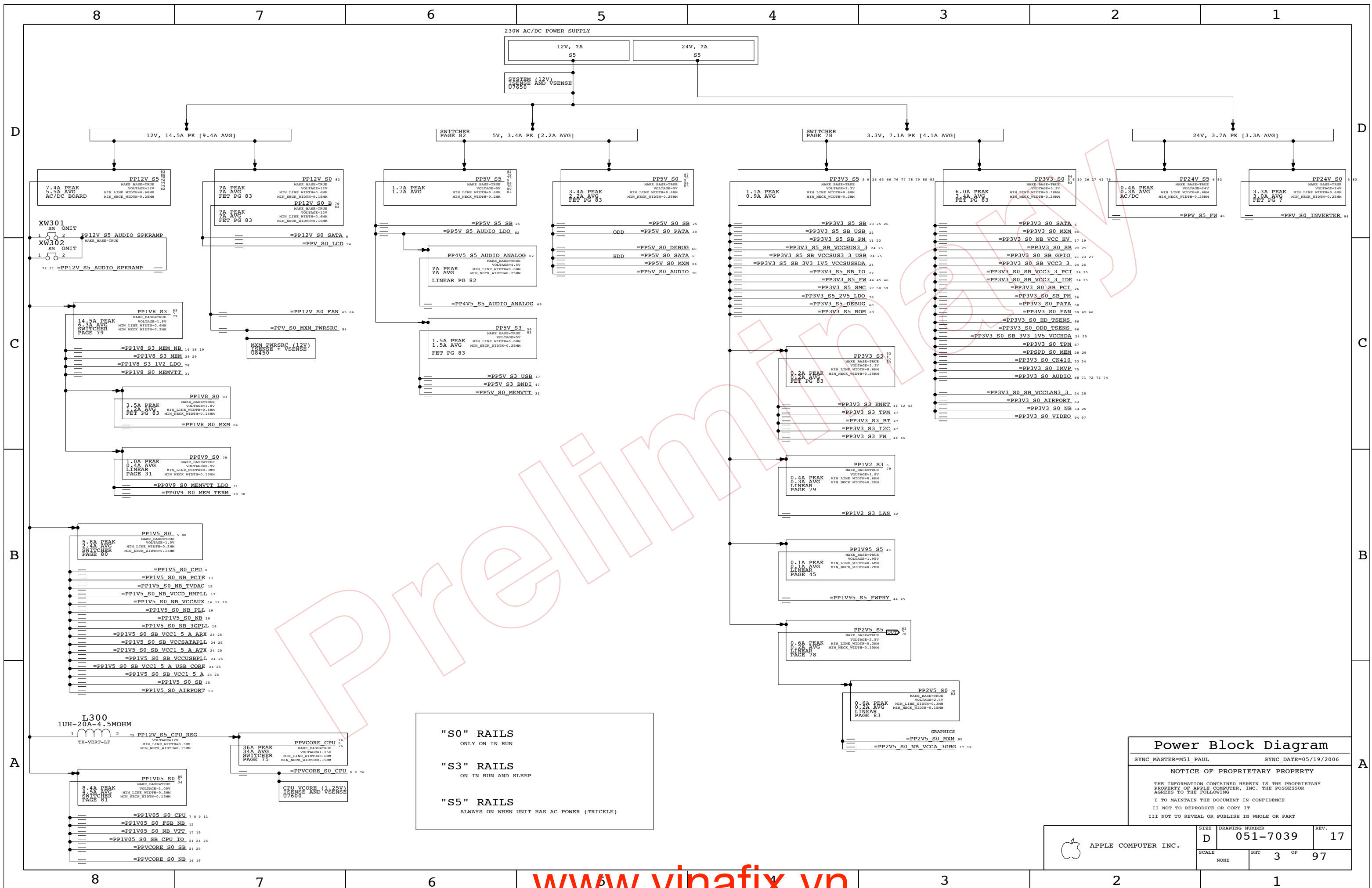
System Block Diagram

SYNC_MASTER=M51_PAUL SYNC_DATE=05/19/2006

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7039	17
SCALE	SHT	OF	
NONE	2	97	



"S0" RAILS
ONLY ON IN RUN

"S3" RAILS
ON IN RUN AND SLEEP

"S5" RAILS
ALWAYS ON WHEN UNIT HAS AC POWER (TRICKLE)

Power Block Diagram

SYNC_MASTER=M51_PAUL SYNC_DATE=05/19/2006

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	D	051-7039	17
SCALE	SHT	OF	
NONE	3	97	

Production BOM

BOM NUMBER	BOM NAME	BOM OPTIONS
630-7512	PCBA,MLB,2.33GHz,M51	M51_COMMON,M51_BEST,EEE_V4K
630-7595	PCBA,MLB,2.16GHz,M51	M51_COMMON,M51_BETTER,EEE_VMD

Development BOM

BOM NUMBER	BOM NAME	BOM OPTIONS
603-8960	PCBA,DEVBOM,M51	M51_DEVELOPMENT

BOMOPTION Groups

BOM GROUP	BOM OPTIONS
M51_COMMON	COMMON,M51_COMMON1,M51_COMMON2,ALTERNATE
M51_COMMON1	NB_TSENS_EXT,CPU_TSENS_EXT,GPU_TSENS_INT,GPU_TSENS_EXT,MXM_ROM,NBCFG_PEG_REVERSE
M51_COMMON2	SB_SYSRST_4_PVT,ITP,MEROM
M51_DEVELOPMENT	DEVELOPMENT,M51_DEV1
M51_DEV1	CPU_PWR_SENSE,CPU_TSENS_INT,MXM_PWR_SENSE,SYS_PWR_SENSE,AMB_TSENS

MEROM BOM OPTION DUE TO PAGE 76 SHARING W/ M50

BarCode Label / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
825-6447	1	BAR CODE LABEL, MLB, M51	[EEE:VMD]	CRITICAL	EEE_VMD
825-6447	1	BAR CODE LABEL, MLB, M51	[EEE:V4K]	CRITICAL	EEE_V4K

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
511S0025	1	IC,CPU-SKT,479BGA	J0700	CRITICAL	
338S0328	1	IC,945PM,NORTHBRIDGE	U1200	CRITICAL	
343S0385	1	IC,SB,652BGA	U2100	CRITICAL	
359S0101	1	IC,CY28445-5,CLK GEN,68PIN QFN	U3301	CRITICAL	
338S0270	1	IC,88E8053,GIGABIT ENET XCVR,64P QFN,NO	U4101	CRITICAL	
341S1797	1	IC,ENET LAN ROM	U4102	CRITICAL	
341S1789	1	IC,TPM,TSSOP,28P	U6700	CRITICAL	
353S1465	1	IC,CPU VREG,IMVP,TWO PHASE,SCREENED	U7500	CRITICAL	
341S1892	1	IC,2K I2C EEPROM,MXM,M51	U8570	CRITICAL	MXM_ROM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
341T0019	1	IC,EFI BOOT ROM,M51	U6301	CRITICAL	
341T0020	1	IC,SMC,M51	U5800	CRITICAL	
337S3292	1	MEROM 2.3GHZ, M51	CPU	CRITICAL	M51_BEST
337S3293	1	MEROM 2.16GHZ, M51	CPU	CRITICAL	M51_BETTER

Misc. Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
742-0048	1	BAT,COIN,3V,220MAH,CR2032	BT2600	CRITICAL	NOSTUFF
820-2038	1	IO ALIGNMENT BOARD, M51	PCB2	CRITICAL	
946-0743	1	IO ALIGNMENT BOARD ADHESIVE	ADH1	CRITICAL	

BATTERY IS INSTALLED AT FATP

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
126S0086	126S0078		ALL	Sanyo alt for Nich.
126S0099	126S0073		ALL	Sanyo alt for Nich.
126S0068	126S0088		ALL	Sanyo alt for Nich.

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
378S0141	378S0140		ALL	GREEN LED ALT.
359S0117	359S0101		U3301	SILEGO CK410 CLOCK
353S1461	353S1465		U7500	CPU VREG_NEW REV

BOM Config

SYNC_MASTER=M51_DAVE SYNC_DATE=(MASTER)

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	D	051-7039	17
SCALE	SHT	OF	
NONE	4	97	

LAYOUT: PLACE CLOSE TO DESTINATION
* OPPOSITE END FROM CLOCK BUFFER

FSB SIGNALS

34 21 SB_CLK100M_SATA_P PP6C4 OMIT P4MM
34 21 SB_CLK100M_SATA_N PP6C5 OMIT P4MM

12 11 7 FSB_CPURST_L PP621 OMIT P4MM

1473 NC_NB_CFG<17> MAKE_BASE=TRUE
1474 NC_NB_CFG<15> MAKE_BASE=TRUE
1475 NC_NB_CFG<14> MAKE_BASE=TRUE
1476 NC_NB_CFG<13> MAKE_BASE=TRUE
1477 NC_NB_CFG<12> MAKE_BASE=TRUE
1478 NC_NB_CFG<11> MAKE_BASE=TRUE
1479 NC_NB_CFG<10> MAKE_BASE=TRUE
1480 NC_NB_CFG<8> MAKE_BASE=TRUE
1481 NC_NB_CFG<6> MAKE_BASE=TRUE
1482 NC_NB_CFG<4> MAKE_BASE=TRUE
1483 NC_NB_CFG<3> MAKE_BASE=TRUE

PPVCORE_CPU FUNC_TEST=TRUE
PP3V3_S5 FUNC_TEST=TRUE
PP2V5_S5 FUNC_TEST=TRUE
PP1V8_S3 FUNC_TEST=TRUE
PP1V2_S3 FUNC_TEST=TRUE
PP1V5_S0 FUNC_TEST=TRUE
PP1V05_S0 FUNC_TEST=TRUE
PP5V_S5 FUNC_TEST=TRUE
PP5V_S0 FUNC_TEST=TRUE
PP5V_S5 FUNC_TEST=TRUE
PP3V3_S5 FUNC_TEST=TRUE
PP3V3_S0 FUNC_TEST=TRUE
PP24V_S0 FUNC_TEST=TRUE

XDP_BPM_L<3> FUNC_TEST=TRUE
XDP_BPM_L<2> FUNC_TEST=TRUE
XDP_BPM_L<1> FUNC_TEST=TRUE
XDP_BPM_L<0> FUNC_TEST=TRUE
XDP_DBRESET_L FUNC_TEST=TRUE
SW_RST_BTN_L FUNC_TEST=TRUE
POWER_BUTTON_L FUNC_TEST=TRUE
LPC_AD<0> FUNC_TEST=TRUE
LPC_AD<1> FUNC_TEST=TRUE
LPC_AD<2> FUNC_TEST=TRUE
LPC_AD<3> FUNC_TEST=TRUE
LPC_FRAME_L FUNC_TEST=TRUE
PM_CLKRUN_L FUNC_TEST=TRUE
BOOT_LPC_SPI_L FUNC_TEST=TRUE
DEBUG_RST_L FUNC_TEST=TRUE
FWH_INIT_L FUNC_TEST=TRUE
PCI_CLK_PORT80 FUNC_TEST=TRUE
INT_SERIRQ FUNC_TEST=TRUE
PM_SUS_STAT_L FUNC_TEST=TRUE
SMC_MD1 FUNC_TEST=TRUE
SMC_RST_L FUNC_TEST=TRUE
SMC_NMI FUNC_TEST=TRUE
SV_SET_UP FUNC_TEST=TRUE
ISENSF_CAL_EN FUNC_TEST=TRUE
INV_ENABLE_BL FUNC_TEST=TRUE
LCD_PWM FUNC_TEST=TRUE
CPU_VID<0> FUNC_TEST=TRUE
CPU_VID<1> FUNC_TEST=TRUE
CPU_VID<2> FUNC_TEST=TRUE
CPU_VID<3> FUNC_TEST=TRUE
CPU_VID<4> FUNC_TEST=TRUE
CPU_VID<5> FUNC_TEST=TRUE
CPU_VID<6> FUNC_TEST=TRUE
PM_DPRST_PVR FUNC_TEST=TRUE
CPU_DPRST_L FUNC_TEST=TRUE
VR_PWRGOOD_DELAY FUNC_TEST=TRUE
VR_PWRGD_CK410 FUNC_TEST=TRUE
ALL_SYS_PWRGD FUNC_TEST=TRUE
PM_SLP_S4_L FUNC_TEST=TRUE
PM_SLP_S3_L FUNC_TEST=TRUE

SMC_TCK FUNC_TEST=TRUE
SMC_TDI FUNC_TEST=TRUE
SMC_TDO FUNC_TEST=TRUE
SMC_TMS FUNC_TEST=TRUE
SMC_TRST_L FUNC_TEST=TRUE
SMC_TX_L FUNC_TEST=TRUE
SMC_RX_L FUNC_TEST=TRUE
SMC_MANUAL_RST_L FUNC_TEST=TRUE

XDP_TCK FUNC_TEST=TRUE
XDP_TDI FUNC_TEST=TRUE
XDP_TDO FUNC_TEST=TRUE
XDP_TMS FUNC_TEST=TRUE
XDP_TRST_L FUNC_TEST=TRUE
POWER_BUTTON_L FUNC_TEST=TRUE
SW_RST_BTN_L FUNC_TEST=TRUE
NB_TSENS_HS_DXP FUNC_TEST=TRUE
NB_TSENS_HS_DYN FUNC_TEST=TRUE
CPU_XDP_CLK_N FUNC_TEST=TRUE
CPU_XDP_CLK_P FUNC_TEST=TRUE
ITPRESET_L FUNC_TEST=TRUE
XDP_BPM_L<5> FUNC_TEST=TRUE
XDP_BPM_L<4> FUNC_TEST=TRUE

D

D

34 23 SB_CLK14P3M_TIMER PP6D9 OMIT P4MM
34 23 SB_CLK48M_USBC1LR PP6E0 OMIT P4MM

LAYOUT NOTE: PLACE NEAR NORTHBRIDGE

I513 TP_PCI_GNT3_L MAKE_BASE=TRUE

SPARE USB PORT

USB_F_N TP_USB_F_N MAKE_BASE=TRUE
USB_F_P TP_USB_F_P MAKE_BASE=TRUE

INVERTER DOES NOT USE THIS SIGNAL
LVDS_BKLTEN TP_LVDS_BKLTEN MAKE_BASE=TRUE

PCI_CLK_SB PP6D0 OMIT P4MM
PCI_CLK_FW PP626 OMIT P4MM
PCI_CLK_SMC PP627 OMIT P4MM

LAYOUT NOTE: PLACE NEAR SOUTHBRIDGE

VR_PWRGOOD_DELAY PP665 OMIT P4MM
NB_RST_IN_LR PP666 OMIT P4MM

DMI_S2N_N<0> PP673 OMIT P4MM
DMI_S2N_P<0> PP674 OMIT P4MM
MEM_VREF_NB_0 PP6E1 OMIT P4MM
MEM_VREF_NB_1 PP675 OMIT P4MM

NC_AUD_BI_PORT_G_L NO_TEST=TRUE
NC_ALS_GAIN NO_TEST=TRUE
NC_AUD_VREF_PORT_C NO_TEST=TRUE
NC_AUD_VREF_PORT_D NO_TEST=TRUE
NC_SMC_BATT_CHG_EN NO_TEST=TRUE
NC_SMC_BATT_ISET NO_TEST=TRUE
NC_SMC_BATT_TRICKLE_PU_L NO_TEST=TRUE
NC_SMC_BATT_VSET NO_TEST=TRUE
NC_SMC_P20 NO_TEST=TRUE
NC_SMC_P21 NO_TEST=TRUE
NC_SMC_P22 NO_TEST=TRUE
NC_SMC_P23 NO_TEST=TRUE
NC_SMC_P26 NO_TEST=TRUE
NC_SMC_P27 NO_TEST=TRUE
NC_SMC_SYS_ISET NO_TEST=TRUE
NC_SMC_SYS_VSET NO_TEST=TRUE
NC_SMS_X_AXIS NO_TEST=TRUE
NC_SMS_Y_AXIS NO_TEST=TRUE
NC_SMS_Z_AXIS NO_TEST=TRUE

NC_J7302_3 NO_TEST=TRUE
NC_J7302_6 NO_TEST=TRUE
NC_AUD_BI_PORT_E_L NO_TEST=TRUE
NC_AUD_BI_PORT_E_R NO_TEST=TRUE
NC_SMC_MEM_ISENSE NO_TEST=TRUE
NC_AUD_BI_PORT_H_L NO_TEST=TRUE
NC_AUD_BI_PORT_H_R NO_TEST=TRUE
NC_AUD_VREF_PORT_B NO_TEST=TRUE

TP_MEM_B_A<15> NO_TEST=TRUE
TP_MEM_B_A<14> NO_TEST=TRUE

PCIE_B_D2R_P PP600 OMIT P4MM
PCIE_B_D2R_N PP601 OMIT P4MM
DMI_N2S_P<0> PP6D3 OMIT P4MM
DMI_N2S_N<0> PP6D4 OMIT P4MM

LPC_FRAME_L PP6D8 OMIT P4MM
SPI_SO PP612 OMIT P4MM
SPI_SI PP613 OMIT P4MM

B

B

ALL I2C BUSES (PLACE IN ACCESSIBLE LOCATION TOP SIDE)

SMBUS_SB_SCL PP604 OMIT P4MM
SMBUS_SB_SDA PP605 OMIT P4MM

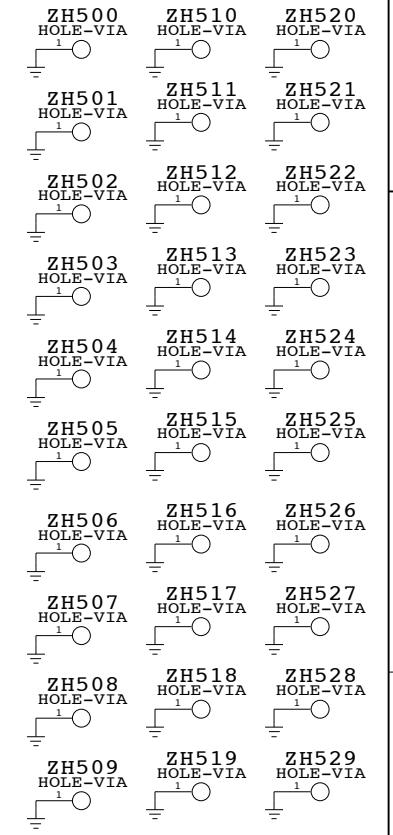
SMBUS_SMC_A_S3_SCL PP610 OMIT P4MM
SMBUS_SMC_A_S3_SDA PP611 OMIT P4MM

PEG_R2D_C_N<0> NO_TEST=TRUE
PEG_R2D_C_P<0> NO_TEST=TRUE
PEG_R2D_C_N<1> NO_TEST=TRUE
PEG_R2D_C_P<1> NO_TEST=TRUE
PEG_R2D_C_N<2> NO_TEST=TRUE
PEG_R2D_C_P<2> NO_TEST=TRUE
PEG_R2D_C_N<3> NO_TEST=TRUE
PEG_R2D_C_P<3> NO_TEST=TRUE
PEG_R2D_C_N<4> NO_TEST=TRUE
PEG_R2D_C_P<4> NO_TEST=TRUE
PEG_R2D_C_N<5> NO_TEST=TRUE
PEG_R2D_C_P<5> NO_TEST=TRUE
PEG_R2D_C_N<6> NO_TEST=TRUE
PEG_R2D_C_P<6> NO_TEST=TRUE
PEG_R2D_C_N<7> NO_TEST=TRUE
PEG_R2D_C_P<7> NO_TEST=TRUE
PEG_R2D_C_N<8> NO_TEST=TRUE
PEG_R2D_C_P<8> NO_TEST=TRUE
PEG_R2D_C_N<9> NO_TEST=TRUE
PEG_R2D_C_P<9> NO_TEST=TRUE
PEG_R2D_C_N<10> NO_TEST=TRUE
PEG_R2D_C_P<10> NO_TEST=TRUE
PEG_R2D_C_N<11> NO_TEST=TRUE
PEG_R2D_C_P<11> NO_TEST=TRUE
PEG_R2D_C_N<12> NO_TEST=TRUE
PEG_R2D_C_P<12> NO_TEST=TRUE
PEG_R2D_C_N<13> NO_TEST=TRUE
PEG_R2D_C_P<13> NO_TEST=TRUE
PEG_R2D_C_N<14> NO_TEST=TRUE
PEG_R2D_C_P<14> NO_TEST=TRUE
PEG_R2D_C_N<15> NO_TEST=TRUE
PEG_R2D_C_P<15> NO_TEST=TRUE

PEG_R2D_N<0> NO_TEST=TRUE
PEG_R2D_P<0> NO_TEST=TRUE
PEG_R2D_N<1> NO_TEST=TRUE
PEG_R2D_P<1> NO_TEST=TRUE
PEG_R2D_N<2> NO_TEST=TRUE
PEG_R2D_P<2> NO_TEST=TRUE
PEG_R2D_N<3> NO_TEST=TRUE
PEG_R2D_P<3> NO_TEST=TRUE
PEG_R2D_N<4> NO_TEST=TRUE
PEG_R2D_P<4> NO_TEST=TRUE
PEG_R2D_N<5> NO_TEST=TRUE
PEG_R2D_P<5> NO_TEST=TRUE
PEG_R2D_N<6> NO_TEST=TRUE
PEG_R2D_P<6> NO_TEST=TRUE
PEG_R2D_N<7> NO_TEST=TRUE
PEG_R2D_P<7> NO_TEST=TRUE
PEG_R2D_N<8> NO_TEST=TRUE
PEG_R2D_P<8> NO_TEST=TRUE
PEG_R2D_N<9> NO_TEST=TRUE
PEG_R2D_P<9> NO_TEST=TRUE
PEG_R2D_N<10> NO_TEST=TRUE
PEG_R2D_P<10> NO_TEST=TRUE
PEG_R2D_N<11> NO_TEST=TRUE
PEG_R2D_P<11> NO_TEST=TRUE
PEG_R2D_N<12> NO_TEST=TRUE
PEG_R2D_P<12> NO_TEST=TRUE
PEG_R2D_N<13> NO_TEST=TRUE
PEG_R2D_P<13> NO_TEST=TRUE
PEG_R2D_N<14> NO_TEST=TRUE
PEG_R2D_P<14> NO_TEST=TRUE
PEG_R2D_N<15> NO_TEST=TRUE
PEG_R2D_P<15> NO_TEST=TRUE

PEG_D2R_N<0> NO_TEST=TRUE
PEG_D2R_P<0> NO_TEST=TRUE
PEG_D2R_N<1> NO_TEST=TRUE
PEG_D2R_P<1> NO_TEST=TRUE
PEG_D2R_N<2> NO_TEST=TRUE
PEG_D2R_P<2> NO_TEST=TRUE
PEG_D2R_N<3> NO_TEST=TRUE
PEG_D2R_P<3> NO_TEST=TRUE
PEG_D2R_N<4> NO_TEST=TRUE
PEG_D2R_P<4> NO_TEST=TRUE
PEG_D2R_N<5> NO_TEST=TRUE
PEG_D2R_P<5> NO_TEST=TRUE
PEG_D2R_N<6> NO_TEST=TRUE
PEG_D2R_P<6> NO_TEST=TRUE
PEG_D2R_N<7> NO_TEST=TRUE
PEG_D2R_P<7> NO_TEST=TRUE
PEG_D2R_N<8> NO_TEST=TRUE
PEG_D2R_P<8> NO_TEST=TRUE
PEG_D2R_N<9> NO_TEST=TRUE
PEG_D2R_P<9> NO_TEST=TRUE
PEG_D2R_N<10> NO_TEST=TRUE
PEG_D2R_P<10> NO_TEST=TRUE
PEG_D2R_N<11> NO_TEST=TRUE
PEG_D2R_P<11> NO_TEST=TRUE
PEG_D2R_N<12> NO_TEST=TRUE
PEG_D2R_P<12> NO_TEST=TRUE
PEG_D2R_N<13> NO_TEST=TRUE
PEG_D2R_P<13> NO_TEST=TRUE
PEG_D2R_N<14> NO_TEST=TRUE
PEG_D2R_P<14> NO_TEST=TRUE
PEG_D2R_N<15> NO_TEST=TRUE
PEG_D2R_P<15> NO_TEST=TRUE

MISC GROUND VIAS



FUNC TEST 1 OF 2

SYNC_MASTER=M51_HENRY SYNC_DATE=05/19/2006

NOTICE OF PROPRIETARY PROPERTY

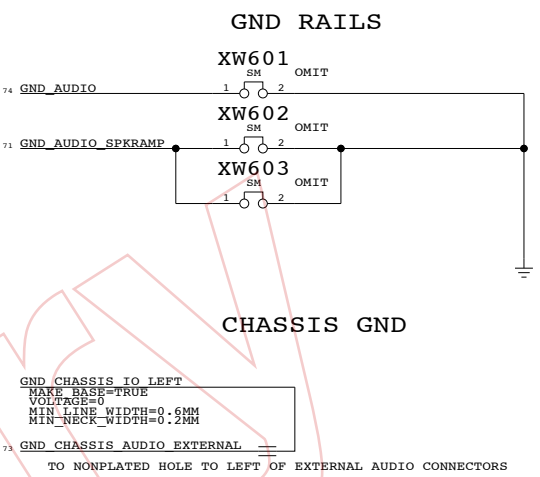
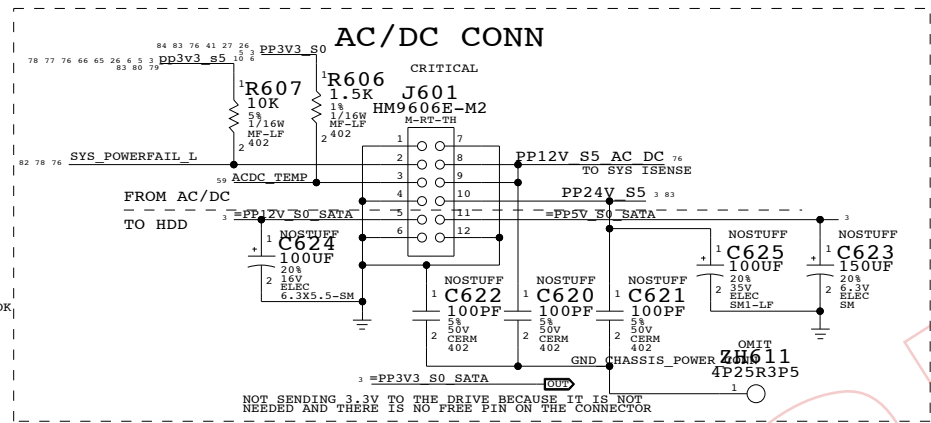
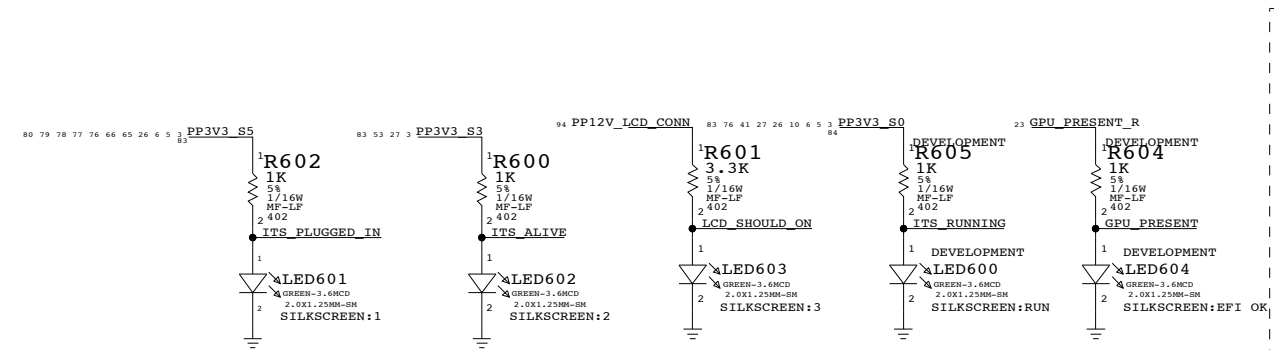
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	D	051-7039	17
SCALE	SHT	OF	
NONE	5	97	

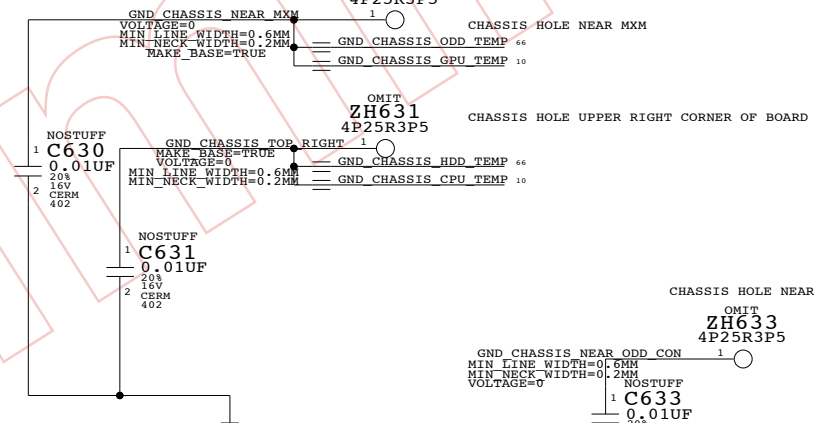
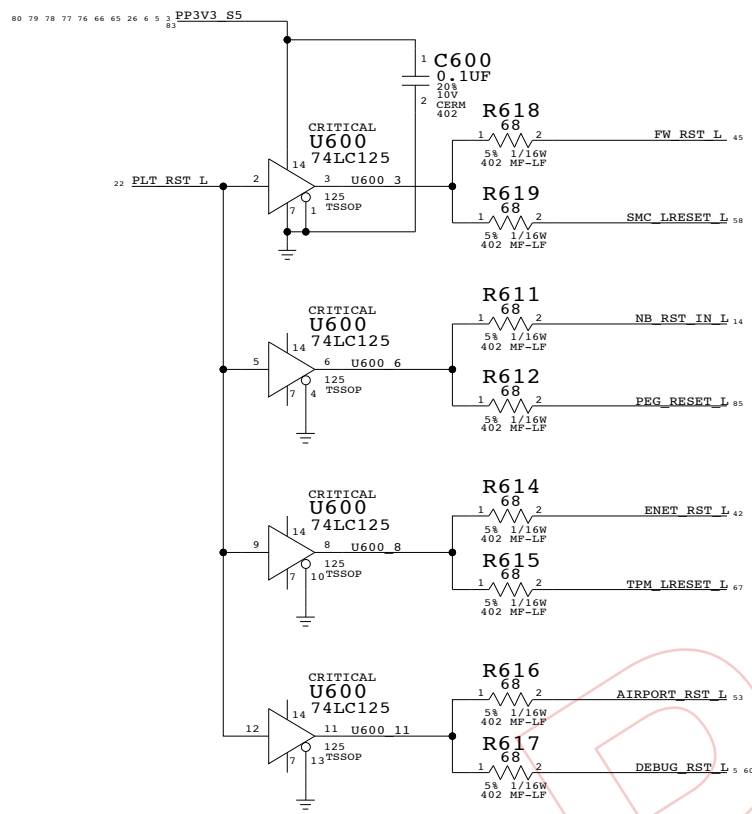
A

A

SYSTEM STATUS

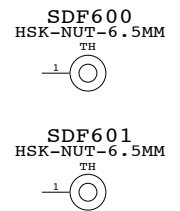


C



HEATSINK BACKER PLATE STANDOFFS

LOCATED NORTH OF CPU



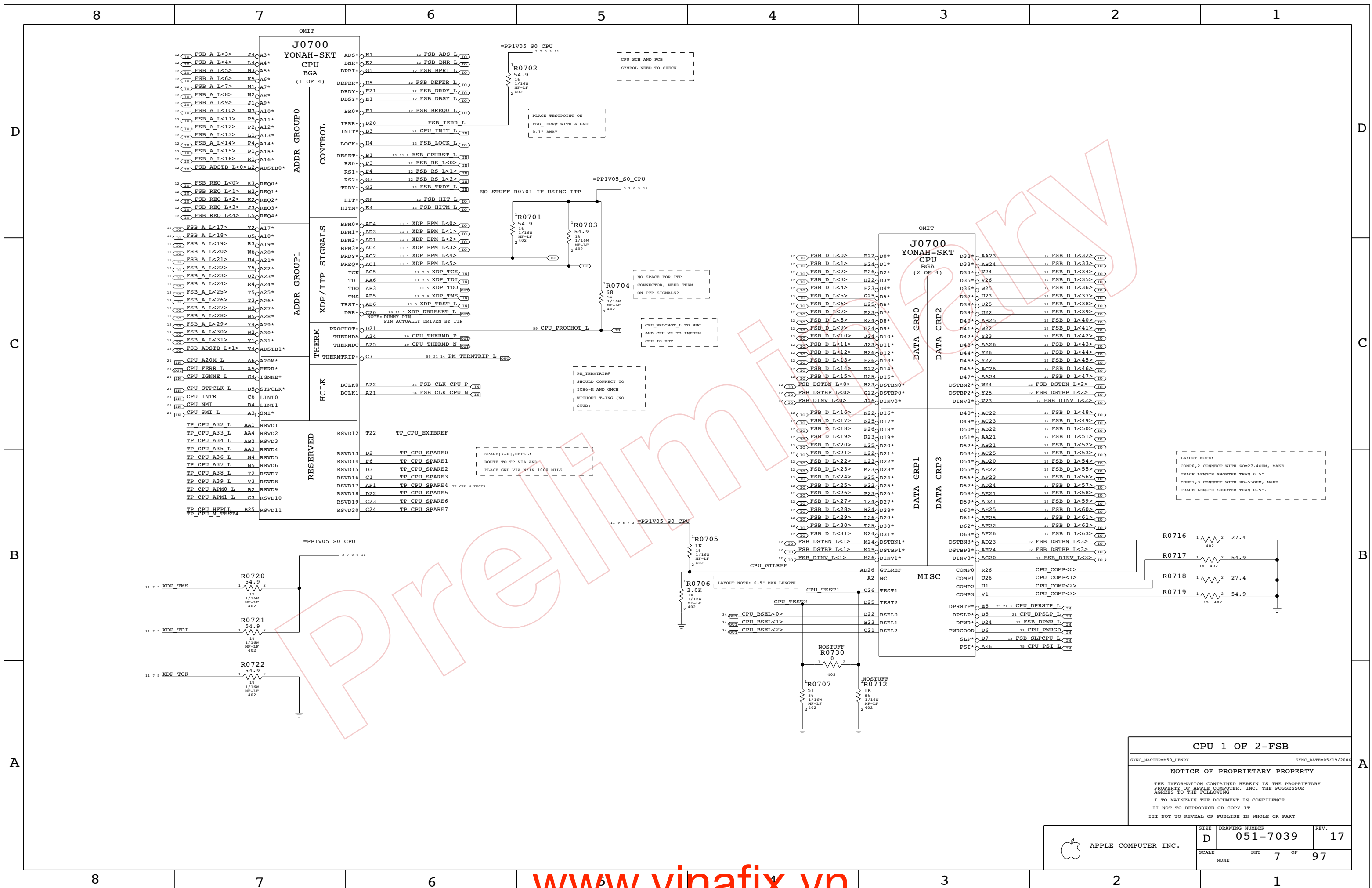
POWER CONN / MISC

SYNC_MASTER=M51_PAUL SYNC_DATE=05/19/2006

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SCALE	SHT	OF	
NONE	6	97	



CPU 1 OF 2-FSB

SYNC_MASTER=M50_HENRY SYNC_DATE=05/19/2006

NOTICE OF PROPRIETARY PROPERTY

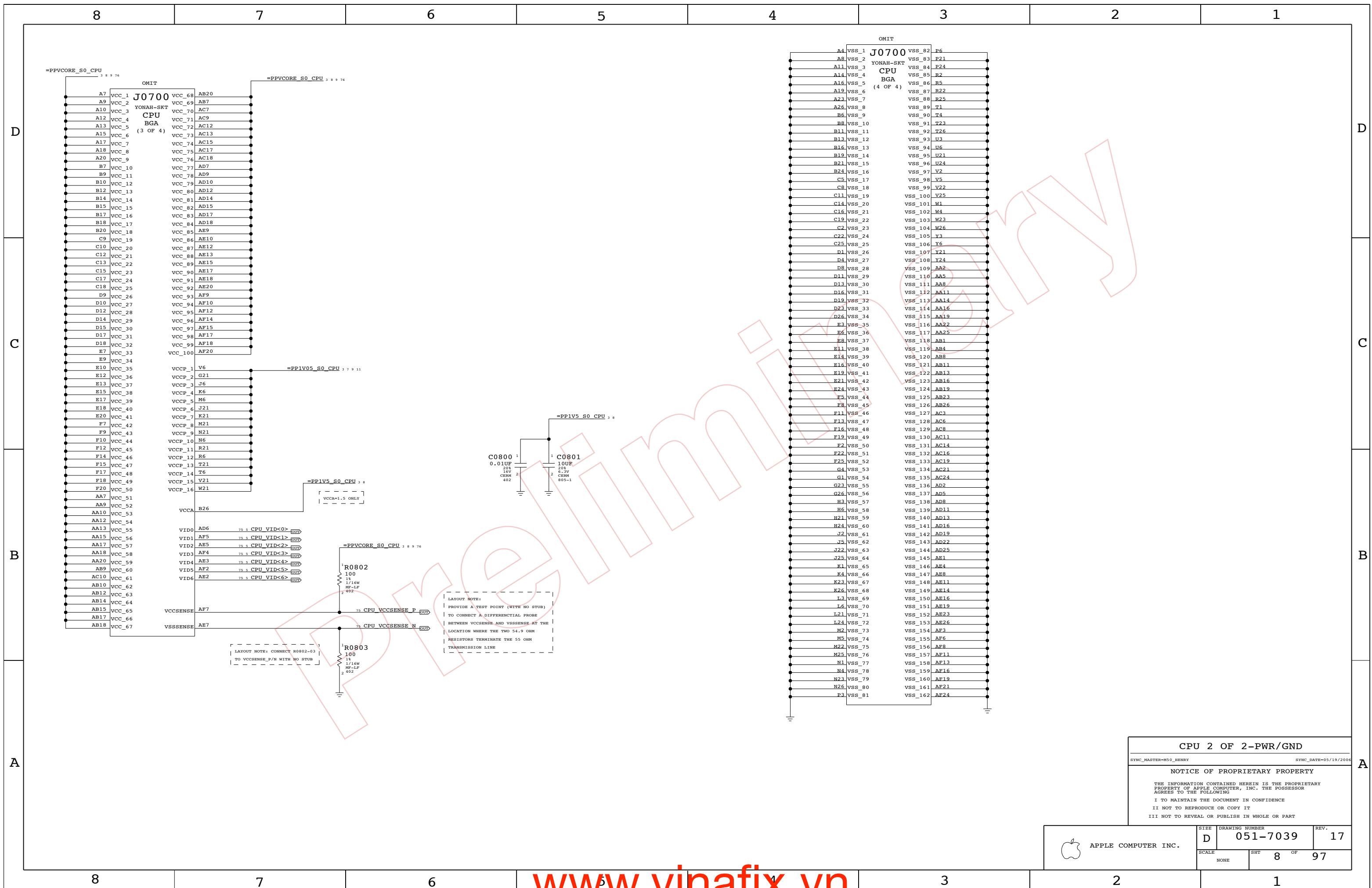
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	D	051-7039	17
SCALE	SHT 7 OF 97		
NONE			



CPU 2 OF 2-PWR/GND

SYNC_MASTER=M50_HENRY SYNC_DATE=05/19/2006

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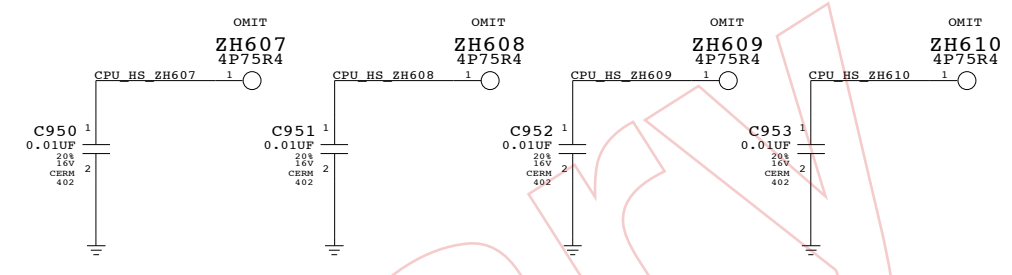
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

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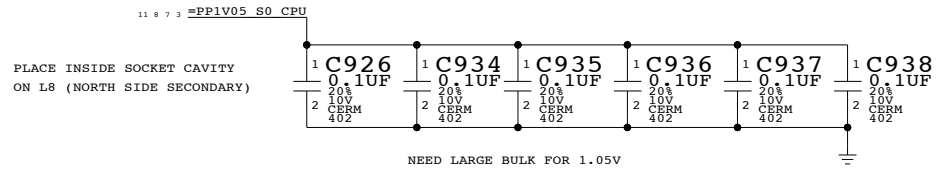
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7039	17
SCALE	SHT 8 OF 97		
NONE			

CPU HEATSINK MOUNTING HOLES



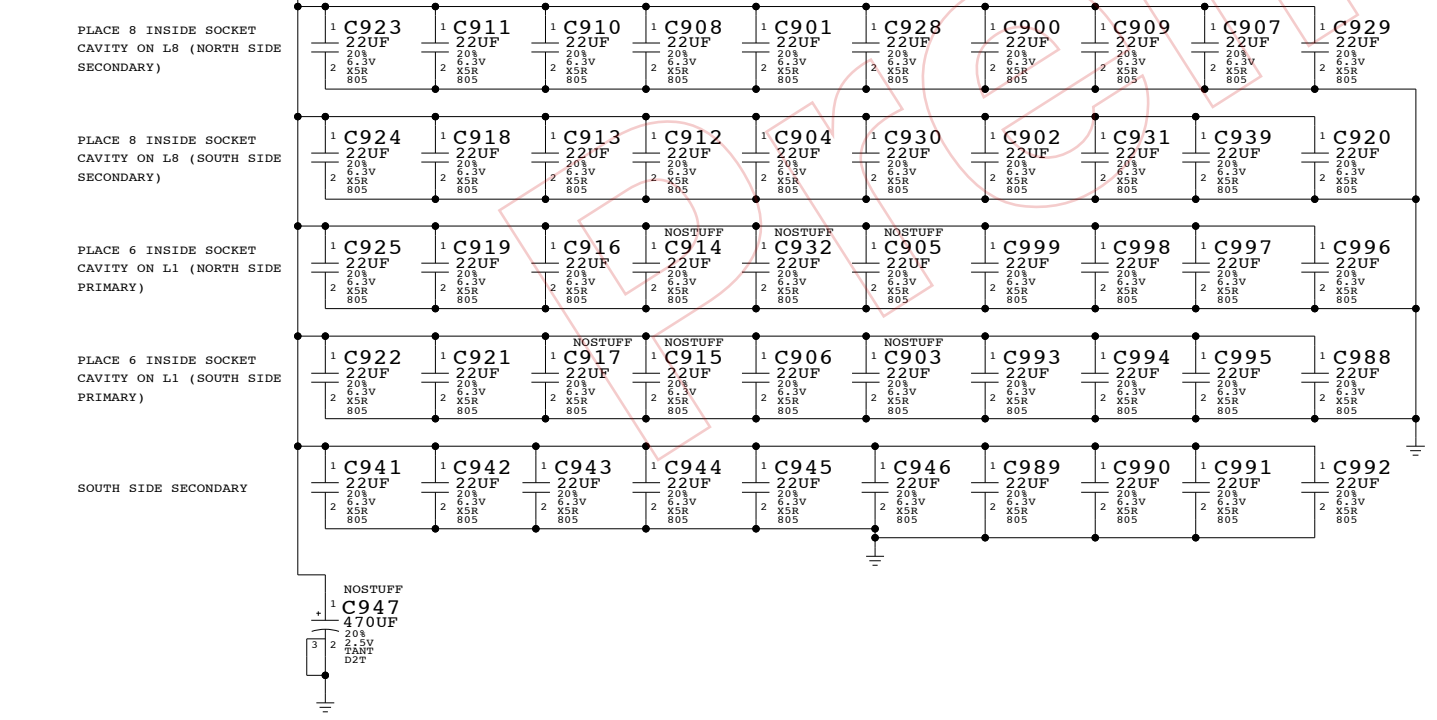
WE HAD A 330UF ELEC CAP HERE FOR 1.05V RAIL - CHECK WE CAN REMOVE

VCCP CORE DECOUPLING



VCC CORE DECOUPLING

DESIGN FOR 44 CERAMIC AND 3 ELECT BULK 1800UF



CPU DECAPS & VID<>
 SYNC_MASTER=M51_HENRY SYNC_DATE=05/19/2006
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7039	17
SCALE	SHT 9 OF 97		
NONE			

D

C

B

A

D

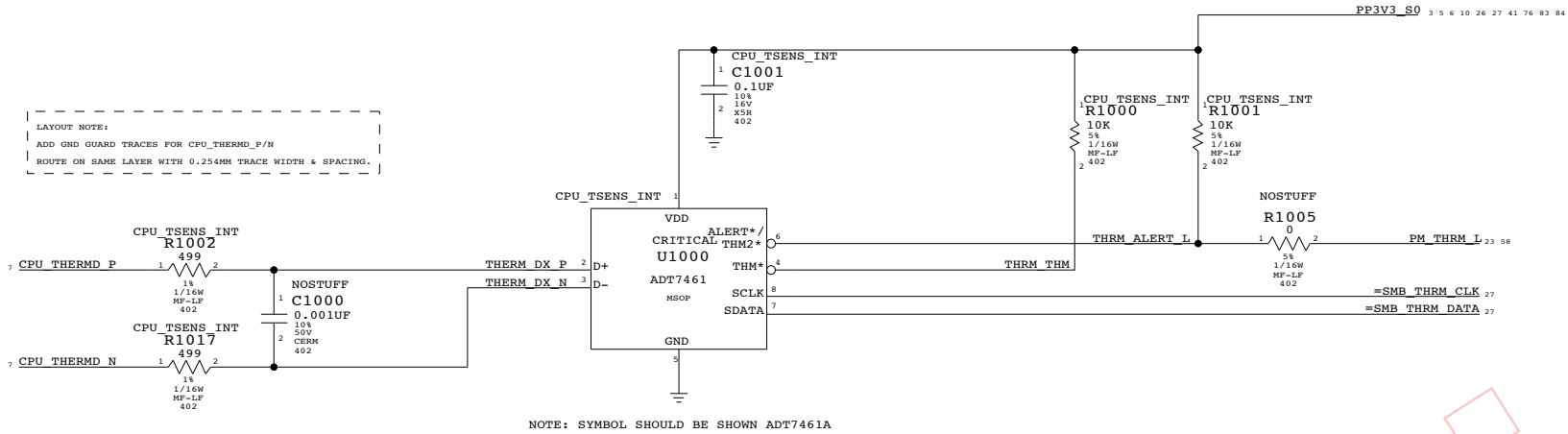
C

B

A

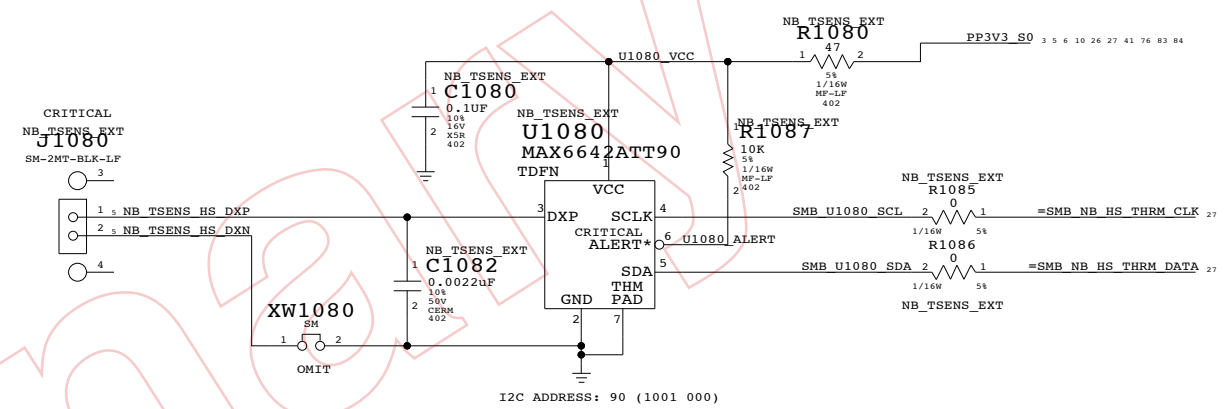
CPU INTERNAL DIODE THERMAL SENSOR

NOTE:
IF CPU T DIODE TO BE READ IN OFF STATE,
THEN THIS SHOULD BE S5



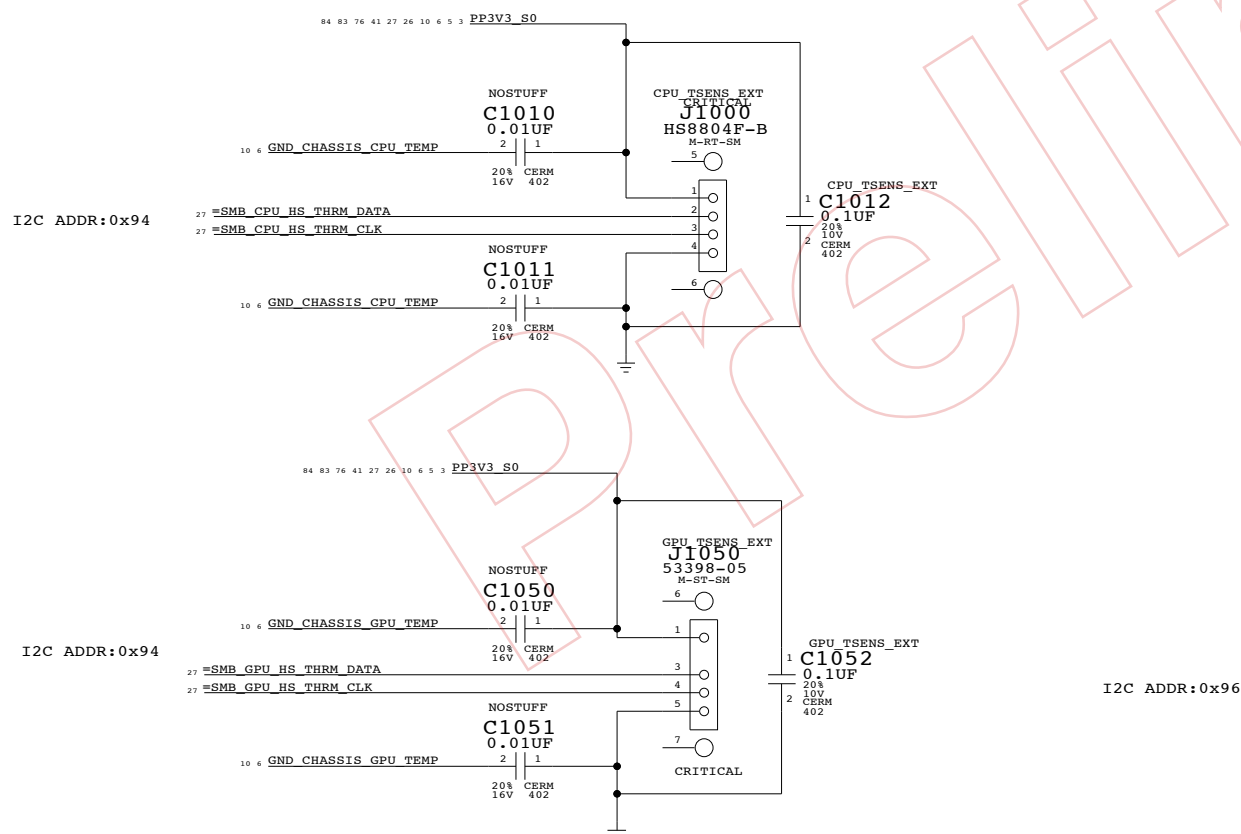
NOTE: SYMBOL SHOULD BE SHOWN ADT7461A

NB HEATSINK TEMPERATURE SENSE

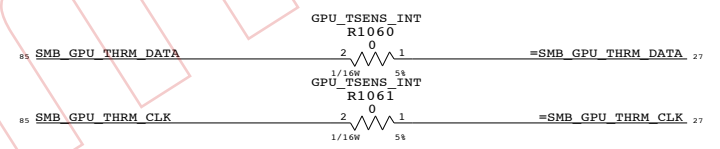


I2C ADDRESS: 90 (1001 000)

CPU AND GPU REMOTE HEATSINK THERMAL SENSORS

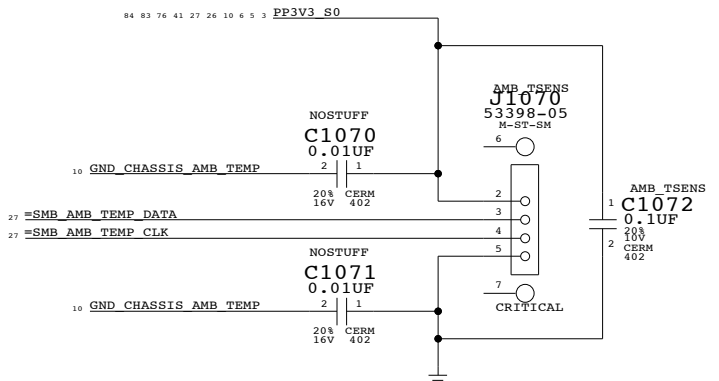


MXM CARD TEMPERATURE SENSOR (GPU INTERNAL DIODE)



NOTE: I2C ADDR:98(1001 100) ON NVIDIA CARD
MAY NOT BE CONSISTENT WITH OTHER CARDS

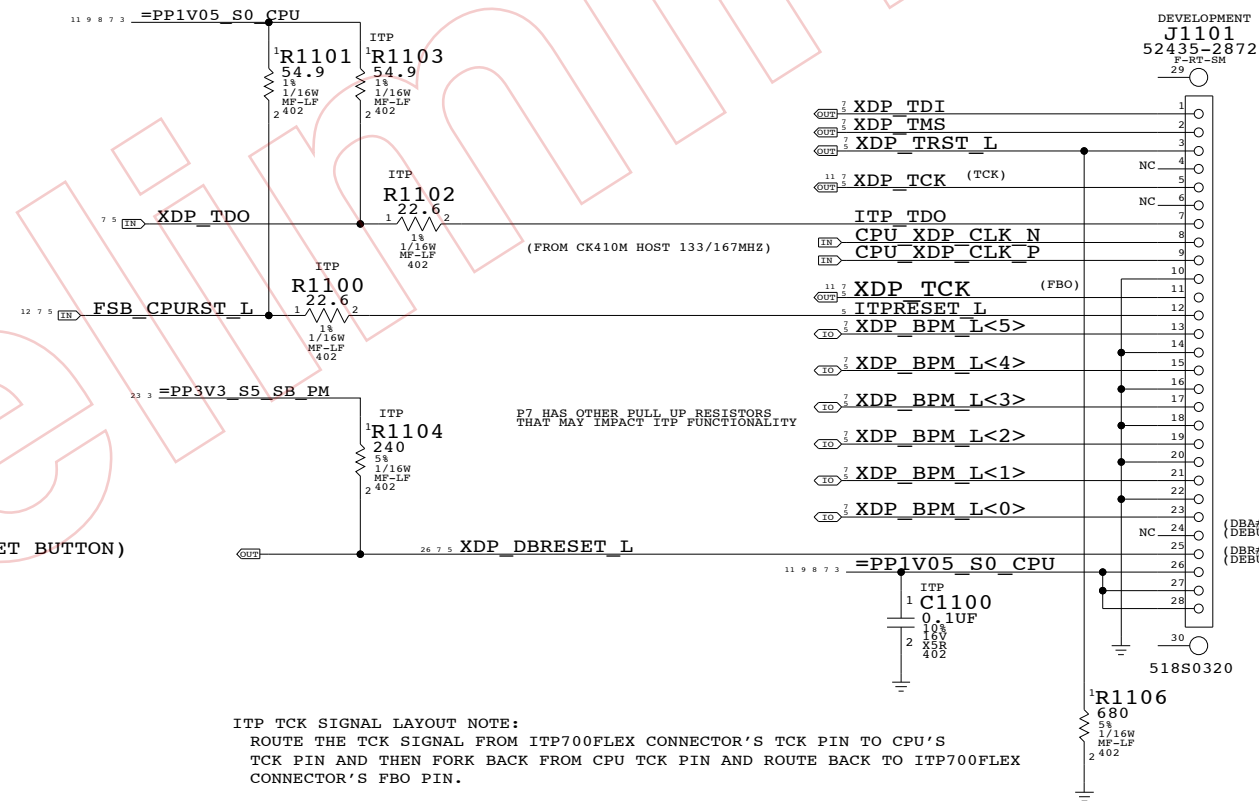
AMBIENT TEMPERATURE (CPU FAN INTAKE) SENSOR



ASIC TEMP SENSORS
 SYNC_MASTER=M51_DAVE SYNC_DATE=(MASTER)
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SCALE	SHT	10 OF	97
NONE			

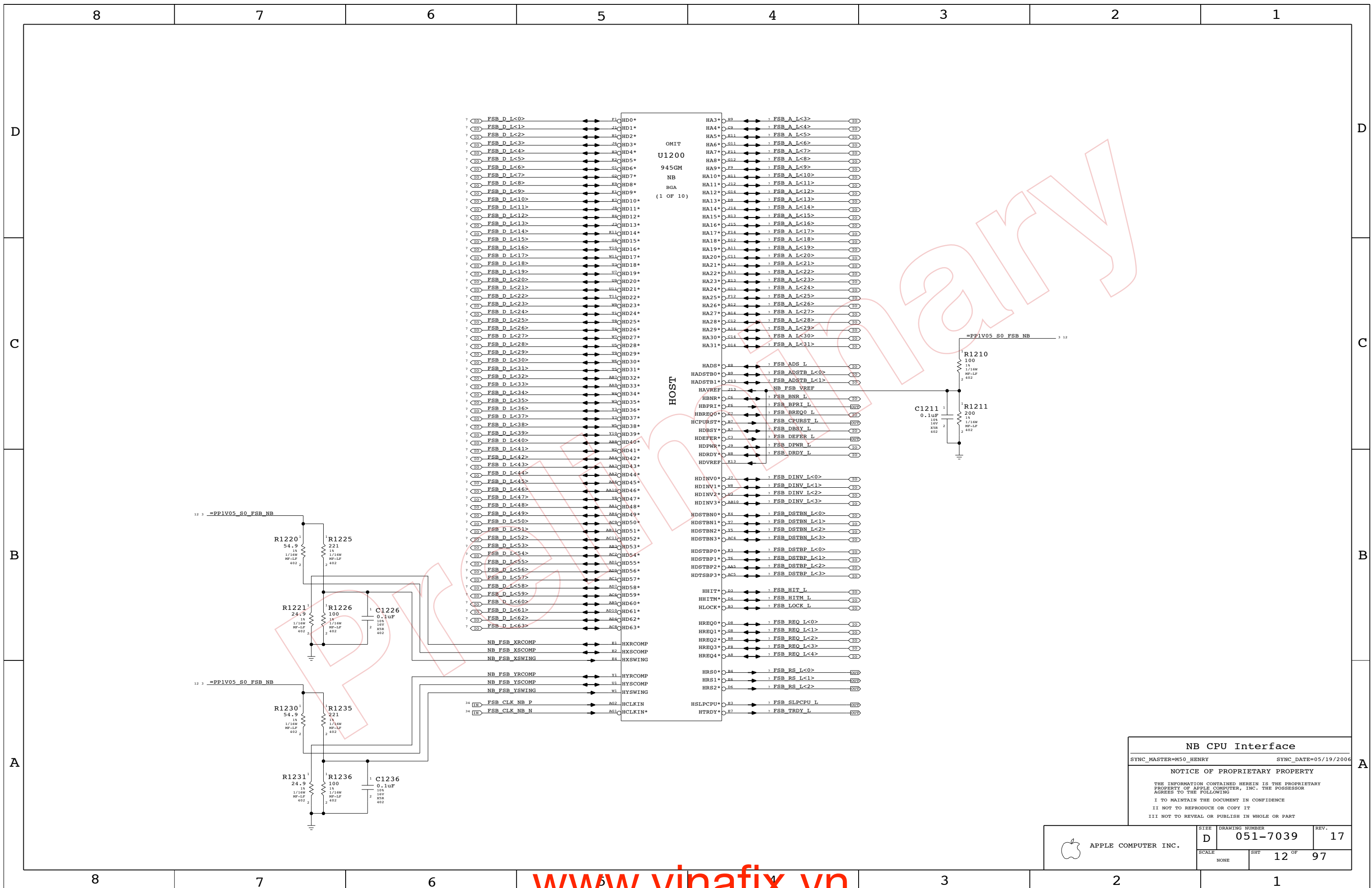
CPU ITP700FLEX DEBUG SUPPORT



CPU ITP700FLEX DEBUG
 SYNC_MASTER=M50_HENRY SYNC_DATE=05/19/2006

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	D	051-7039	17
SCALE	SHT	11 OF	97
NONE			



NB CPU Interface

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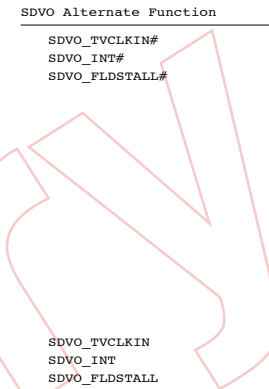
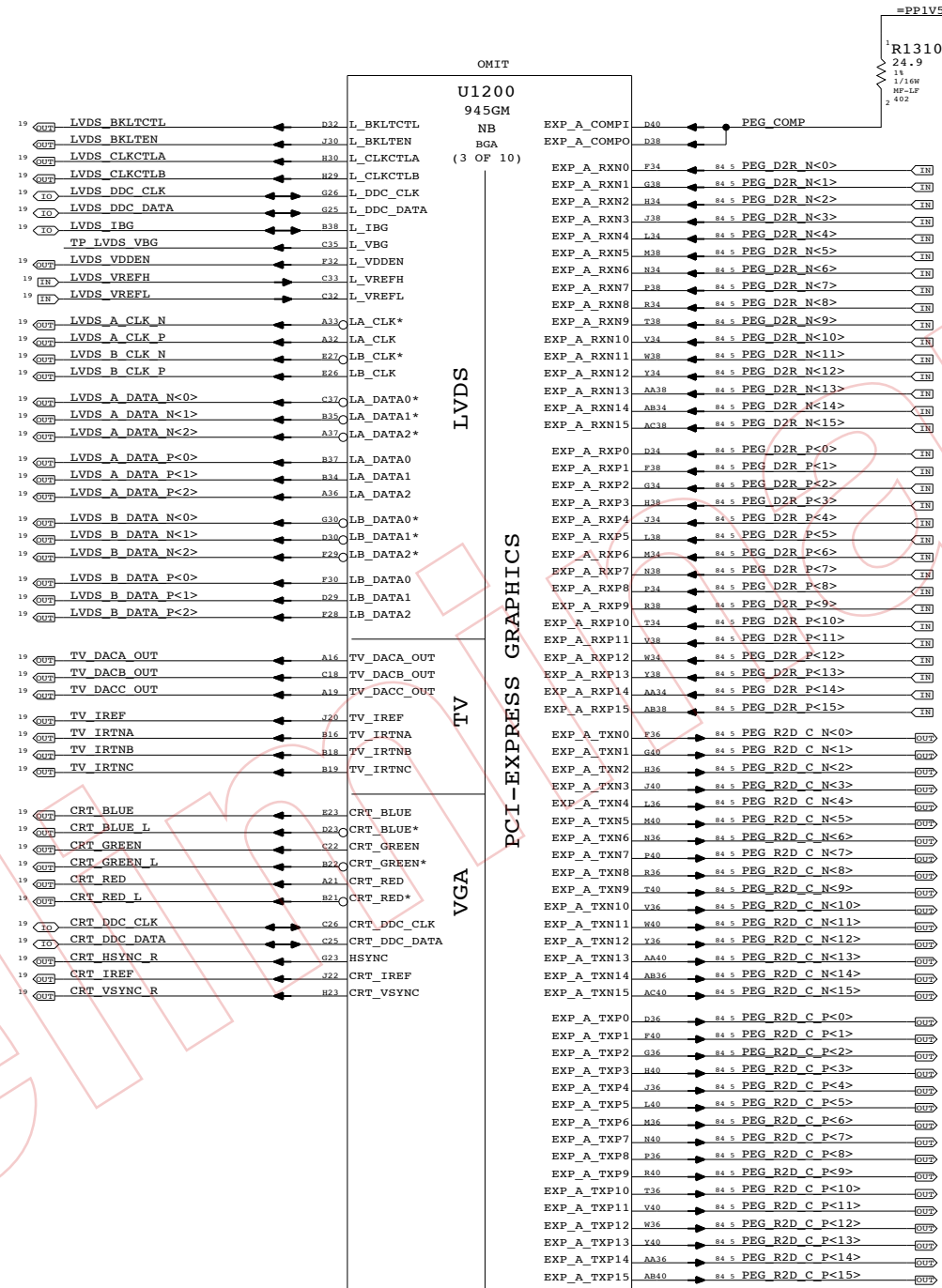
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7039	17
SCALE	SHT	12 OF	97
NONE			

LVDS Disable
 Can leave all signals NC if LVDS is not implemented
 Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
 VCCD_LVDS must remain powered with proper decoupling.
 Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:
 Composite: DACA only
 S-Video: DACB & DACC only
 Component: DACA, DACB & DACC
 Unused DAC outputs must remain powered, but can omit
 filtering components. Unused DAC outputs should
 connect to GND through 75-ohm resistors.

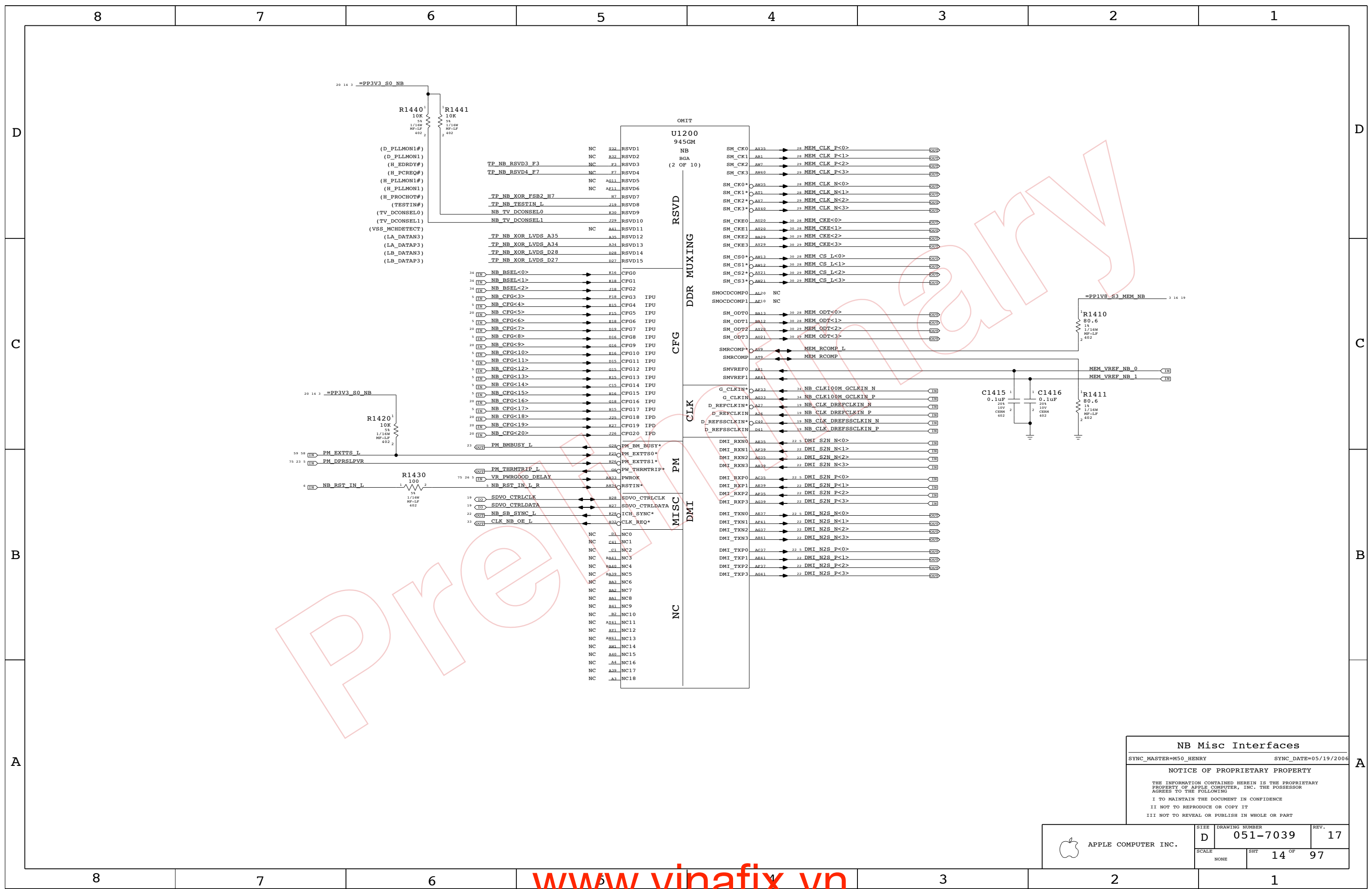
TV-Out Disable
 Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail.
 Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and
 VCCA_TVVBG to 1.5V power rail. Tie VSSA_TVVBG to GND.

CRT Disable
 Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie
 HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core
 rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.



NB PEG / Video Interfaces
 SYNC_MASTER=M50_HENRY SYNC_DATE=05/19/2006
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7039	17
SCALE	SHT	13 OF 97	
NONE			



NB Misc Interfaces

SYNC_MASTER=M50_HENRY SYNC_DATE=05/19/2006

NOTICE OF PROPRIETARY PROPERTY

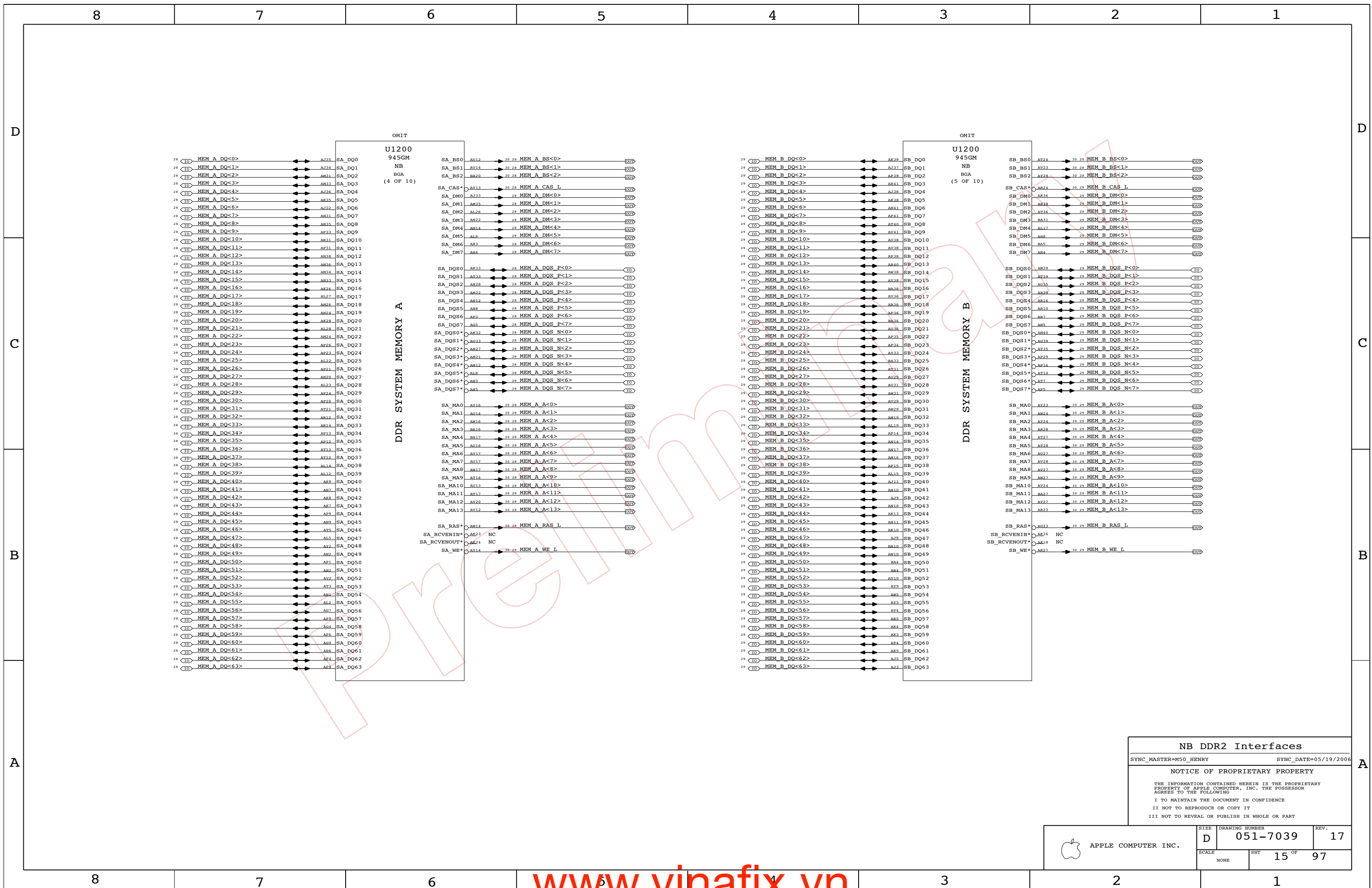
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	D	051-7039	17
SCALE	SHT	OF	REV.
NONE	14	97	



NB DDR2 Interfaces

SYNC_MASTER=M50_HENRY SYNC_DATE=05/19/2006

NOTICE OF PROPRIETARY PROPERTY

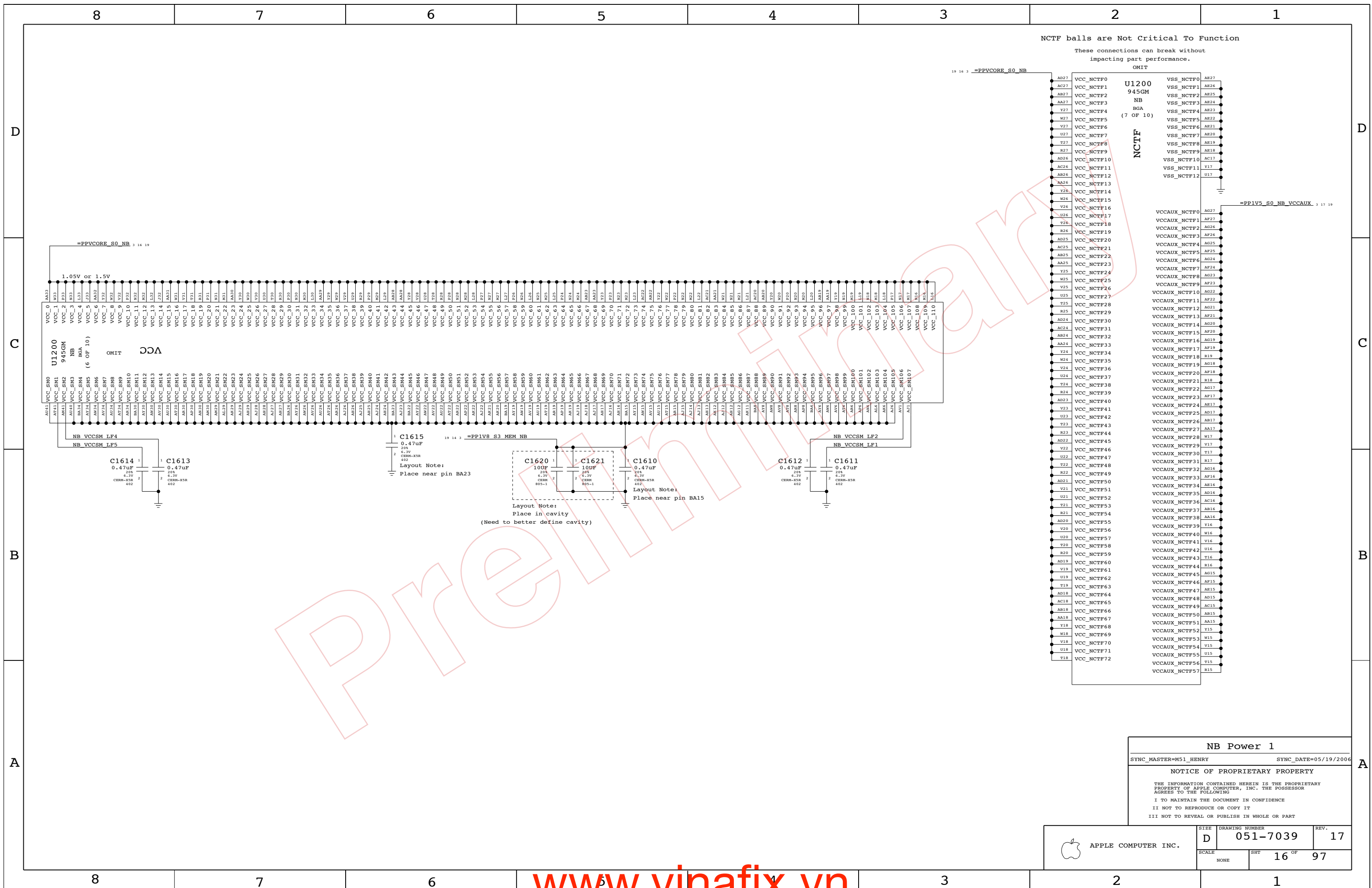
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7039	REV. 17
	SCALE NONE	SHEET 15 OF 97	



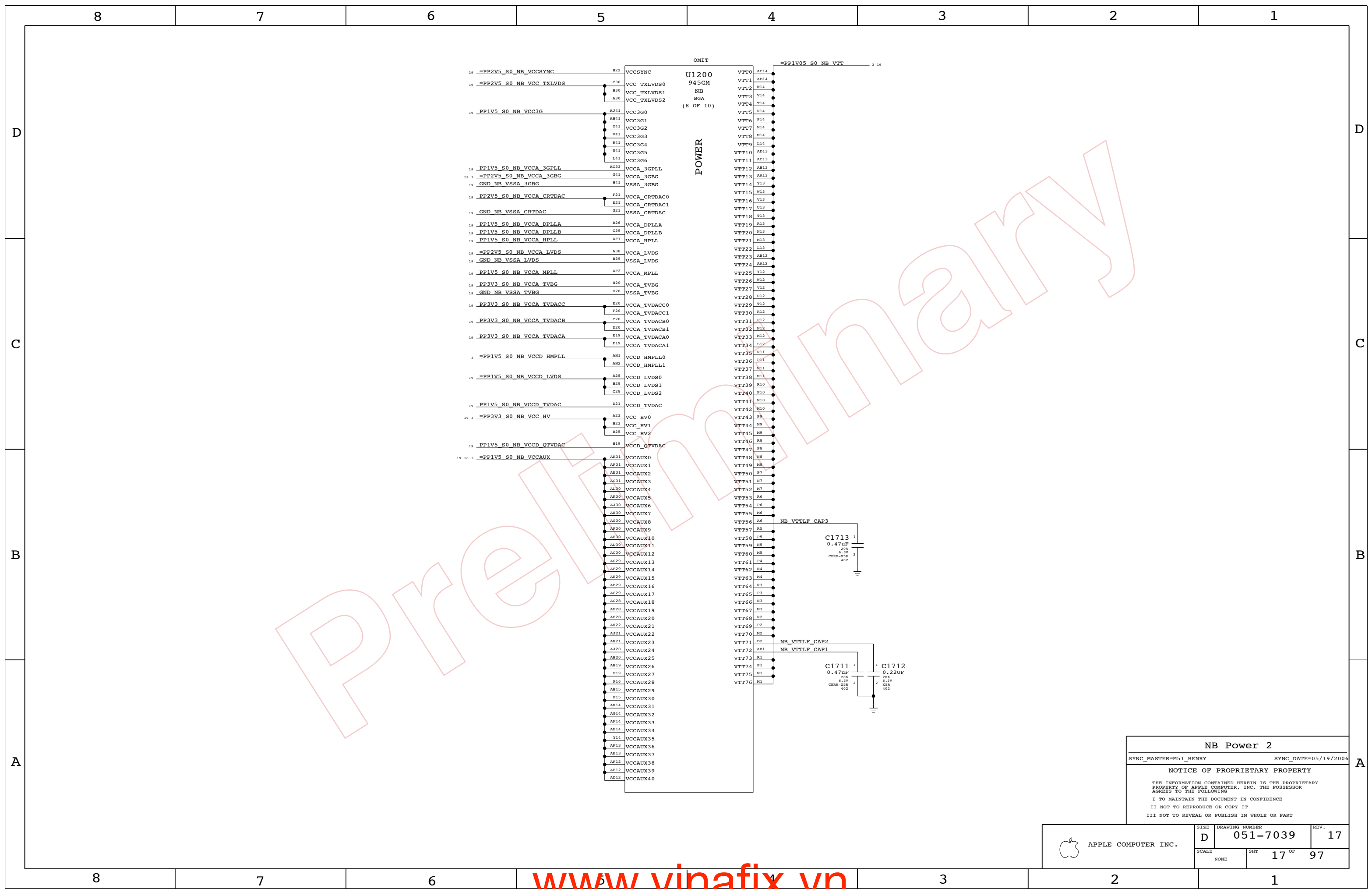
NCTF balls are Not Critical To Function
 These connections can break without impacting part performance.
 OMIT

U1200
 945GM
 NB
 BGA
 (7 OF 10)
 NCTF

VCCAUX_NCTF0
 VCCAUX_NCTF1
 VCCAUX_NCTF2
 VCCAUX_NCTF3
 VCCAUX_NCTF4
 VCCAUX_NCTF5
 VCCAUX_NCTF6
 VCCAUX_NCTF7
 VCCAUX_NCTF8
 VCCAUX_NCTF9
 VCCAUX_NCTF10
 VCCAUX_NCTF11
 VCCAUX_NCTF12
 VCCAUX_NCTF13
 VCCAUX_NCTF14
 VCCAUX_NCTF15
 VCCAUX_NCTF16
 VCCAUX_NCTF17
 VCCAUX_NCTF18
 VCCAUX_NCTF19
 VCCAUX_NCTF20
 VCCAUX_NCTF21
 VCCAUX_NCTF22
 VCCAUX_NCTF23
 VCCAUX_NCTF24
 VCCAUX_NCTF25
 VCCAUX_NCTF26
 VCCAUX_NCTF27
 VCCAUX_NCTF28
 VCCAUX_NCTF29
 VCCAUX_NCTF30
 VCCAUX_NCTF31
 VCCAUX_NCTF32
 VCCAUX_NCTF33
 VCCAUX_NCTF34
 VCCAUX_NCTF35
 VCCAUX_NCTF36
 VCCAUX_NCTF37
 VCCAUX_NCTF38
 VCCAUX_NCTF39
 VCCAUX_NCTF40
 VCCAUX_NCTF41
 VCCAUX_NCTF42
 VCCAUX_NCTF43
 VCCAUX_NCTF44
 VCCAUX_NCTF45
 VCCAUX_NCTF46
 VCCAUX_NCTF47
 VCCAUX_NCTF48
 VCCAUX_NCTF49
 VCCAUX_NCTF50
 VCCAUX_NCTF51
 VCCAUX_NCTF52
 VCCAUX_NCTF53
 VCCAUX_NCTF54
 VCCAUX_NCTF55
 VCCAUX_NCTF56
 VCCAUX_NCTF57

NB Power 1
 SYNC_MASTER=M51_HENRY SYNC_DATE=05/19/2006
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SCALE	SHT	16 OF 97	
NONE			



Pre-release

NB Power 2

SYNC_MASTER=M51_HENRY SYNC_DATE=05/19/2006

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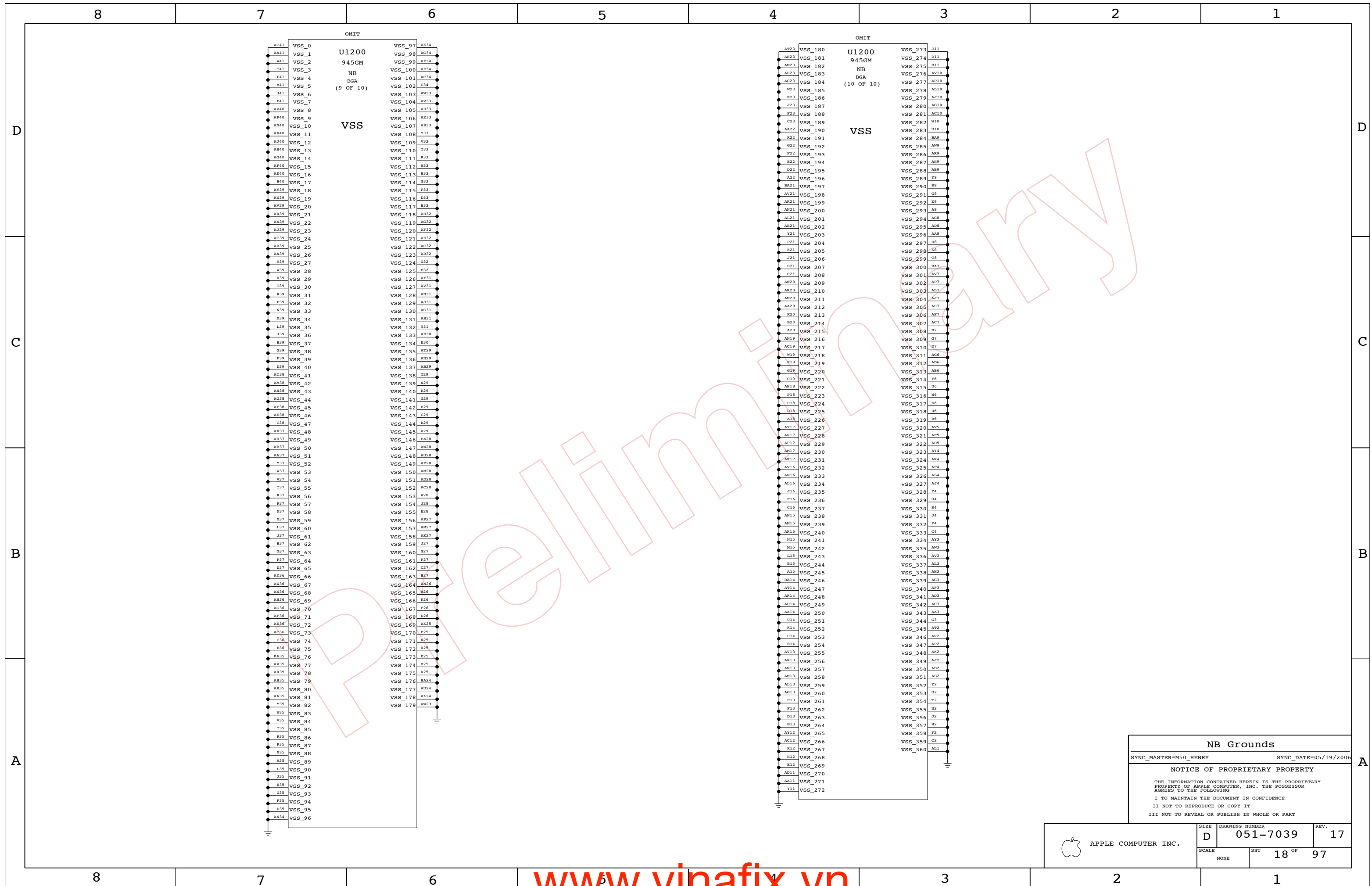
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SCALE		SHT	OF
NONE		17	97



NB Grounds

SYNC_MASTER=M50_HENRY SYNC_DATE=05/19/2006

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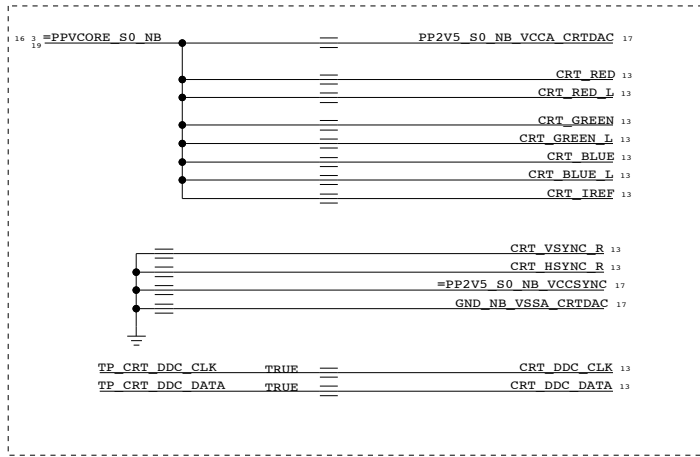
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7039	17
SCALE	SHT	18 OF 97	
NONE			

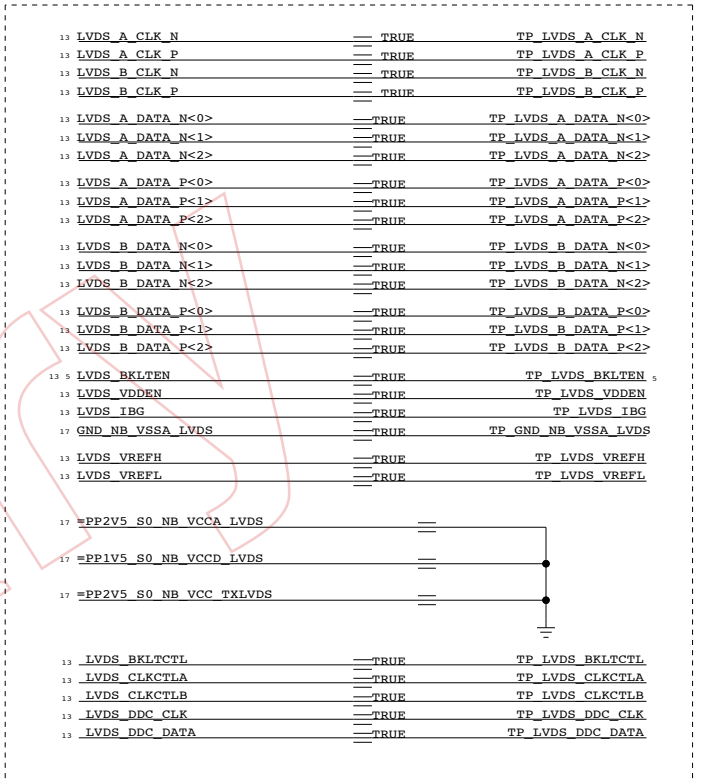
D

D

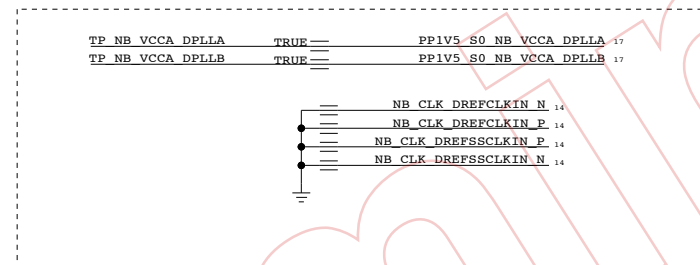
TVOUT DISABLE



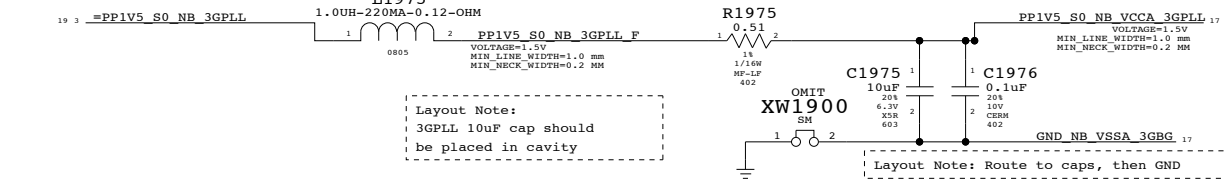
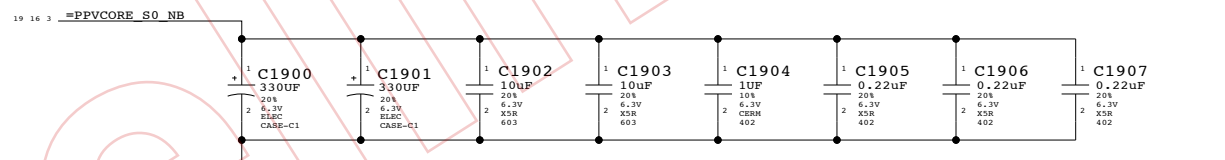
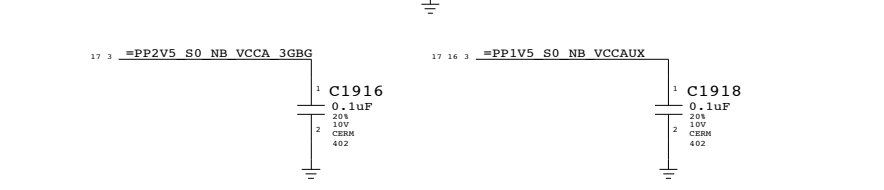
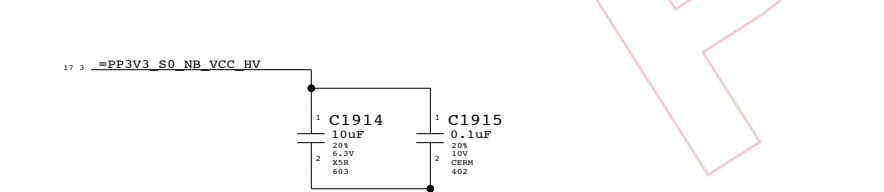
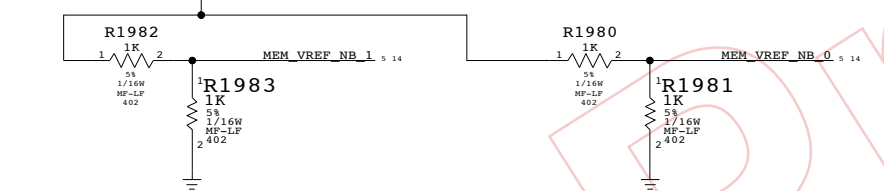
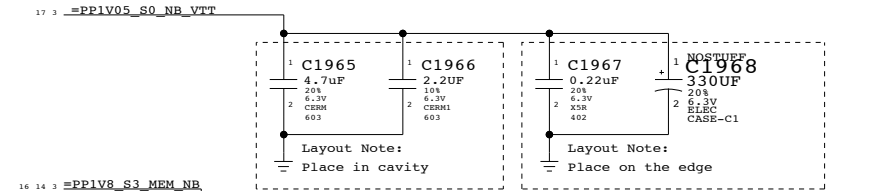
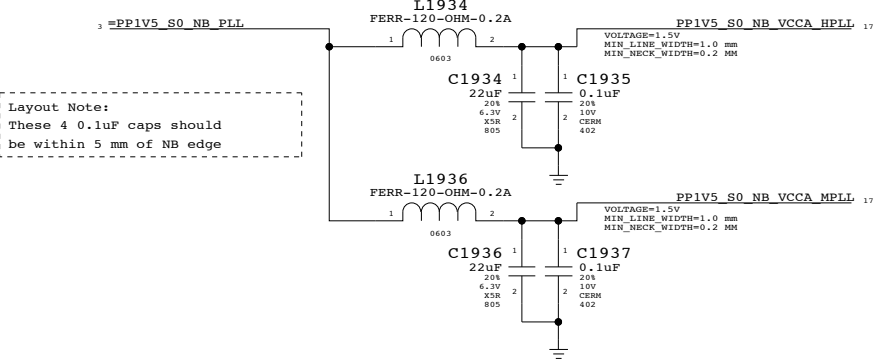
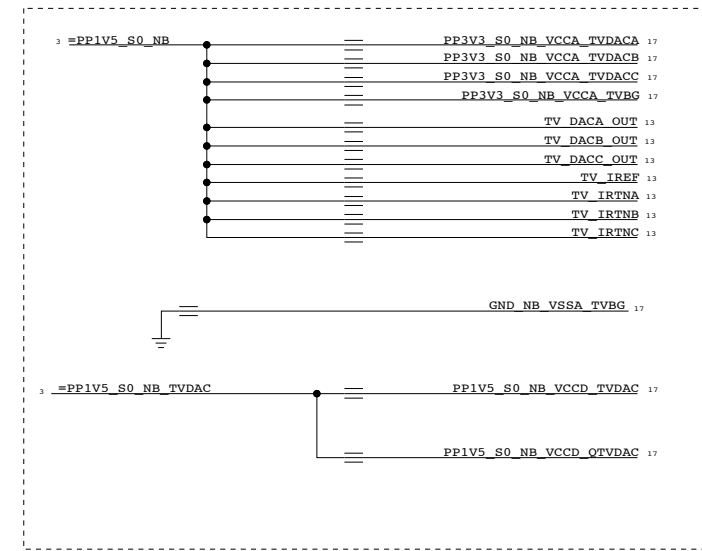
LVDS DISABLE



DISPLAY DISABLE



TVOUT DISABLE



Layout Note:
 These 4 0.1uF caps should be within 5 mm of NB edge

Layout Note:
 Place in cavity

Layout Note:
 Place on the edge

Layout Note:
 Place L and C close to MCH

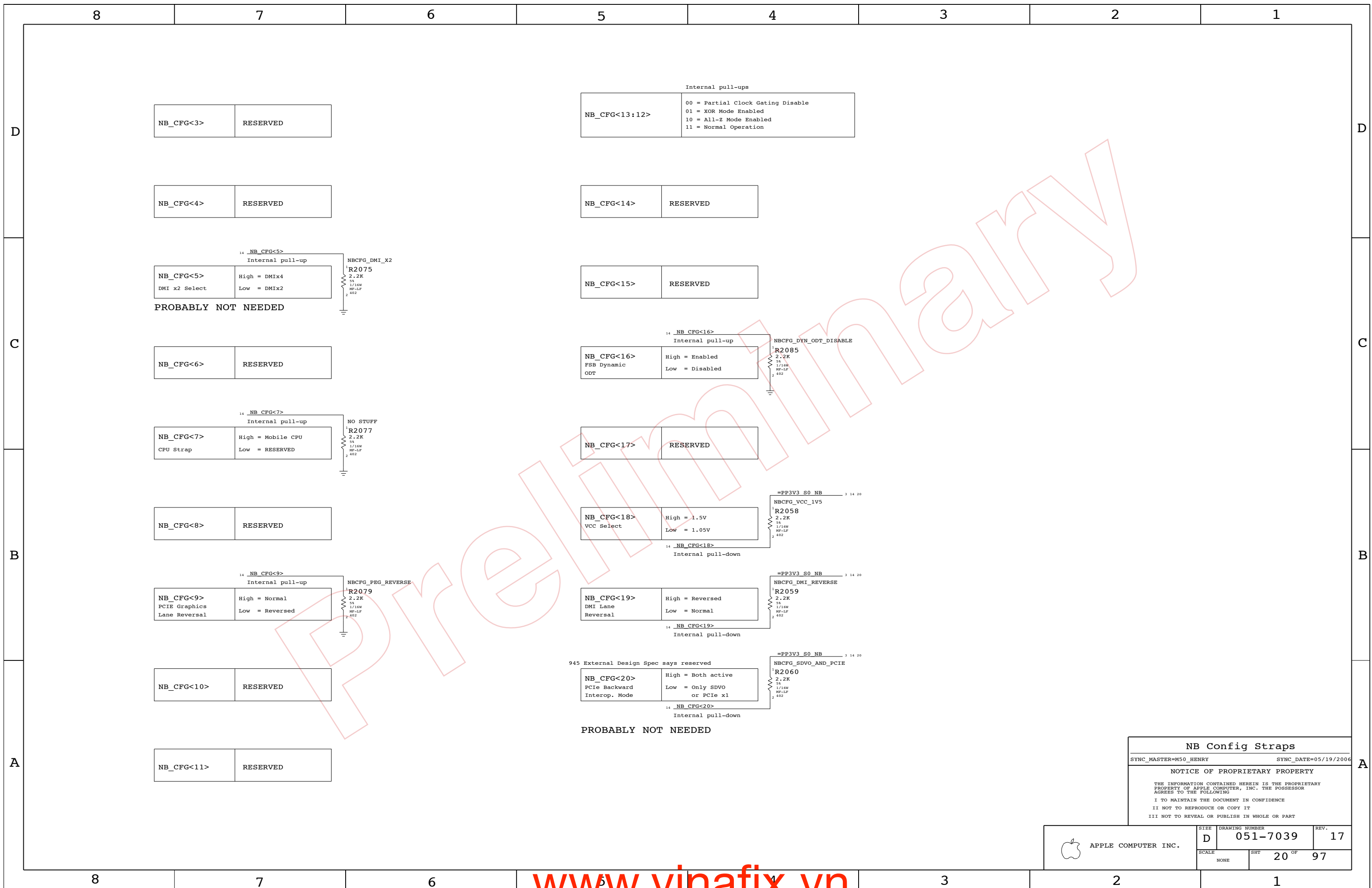
Layout Note:
 10uF caps should be close to MCH on opposite side.

Layout Note:
 3GPLL 10uF cap should be placed in cavity

Layout Note: Route to caps, then GND

NB (GM) Decoupling
 SYNC_MASTER=M51_DAVE SYNC_DATE=(MASTER)
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	D	051-7039	17
SCALE	SHT	19 OF 97	
NONE			



Internal pull-ups

NB_CFG<13:12>	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal Operation
---------------	--

NB_CFG<3>	RESERVED
-----------	----------

NB_CFG<14>	RESERVED
------------	----------

NB_CFG<4>	RESERVED
-----------	----------

14_NB_CFG<5>
Internal pull-up

NB_CFG<5>	High = DMIX4 DMI x2 Select Low = DMIX2
-----------	--

PROBABLY NOT NEEDED

NB_CFG<15>	RESERVED
------------	----------

NB_CFG<6>	RESERVED
-----------	----------

14_NB_CFG<16>
Internal pull-up

NB_CFG<16>	High = Enabled FSB Dynamic ODT Low = Disabled
------------	--

14_NB_CFG<7>
Internal pull-up

NB_CFG<7>	High = Mobile CPU CPU Strap Low = RESERVED
-----------	--

NB_CFG<17>	RESERVED
------------	----------

NB_CFG<8>	RESERVED
-----------	----------

14_NB_CFG<18>
Internal pull-down

NB_CFG<18>	High = 1.5V VCC Select Low = 1.05V
------------	--

14_NB_CFG<9>
Internal pull-up

NB_CFG<9>	High = Normal PCIe Graphics Lane Reversal Low = Reversed
-----------	---

14_NB_CFG<19>
Internal pull-down

NB_CFG<19>	High = Reversed DMI Lane Reversal Low = Normal
------------	---

NB_CFG<10>	RESERVED
------------	----------

945 External Design Spec says reserved

14_NB_CFG<20>
Internal pull-down

NB_CFG<20>	High = Both active PCIe Backward Interop. Mode Low = Only SDVO or PCIe x1
------------	---

PROBABLY NOT NEEDED

NB_CFG<11>	RESERVED
------------	----------

NB Config Straps

SYNC_MASTER=M50_HENRY SYNC_DATE=05/19/2006

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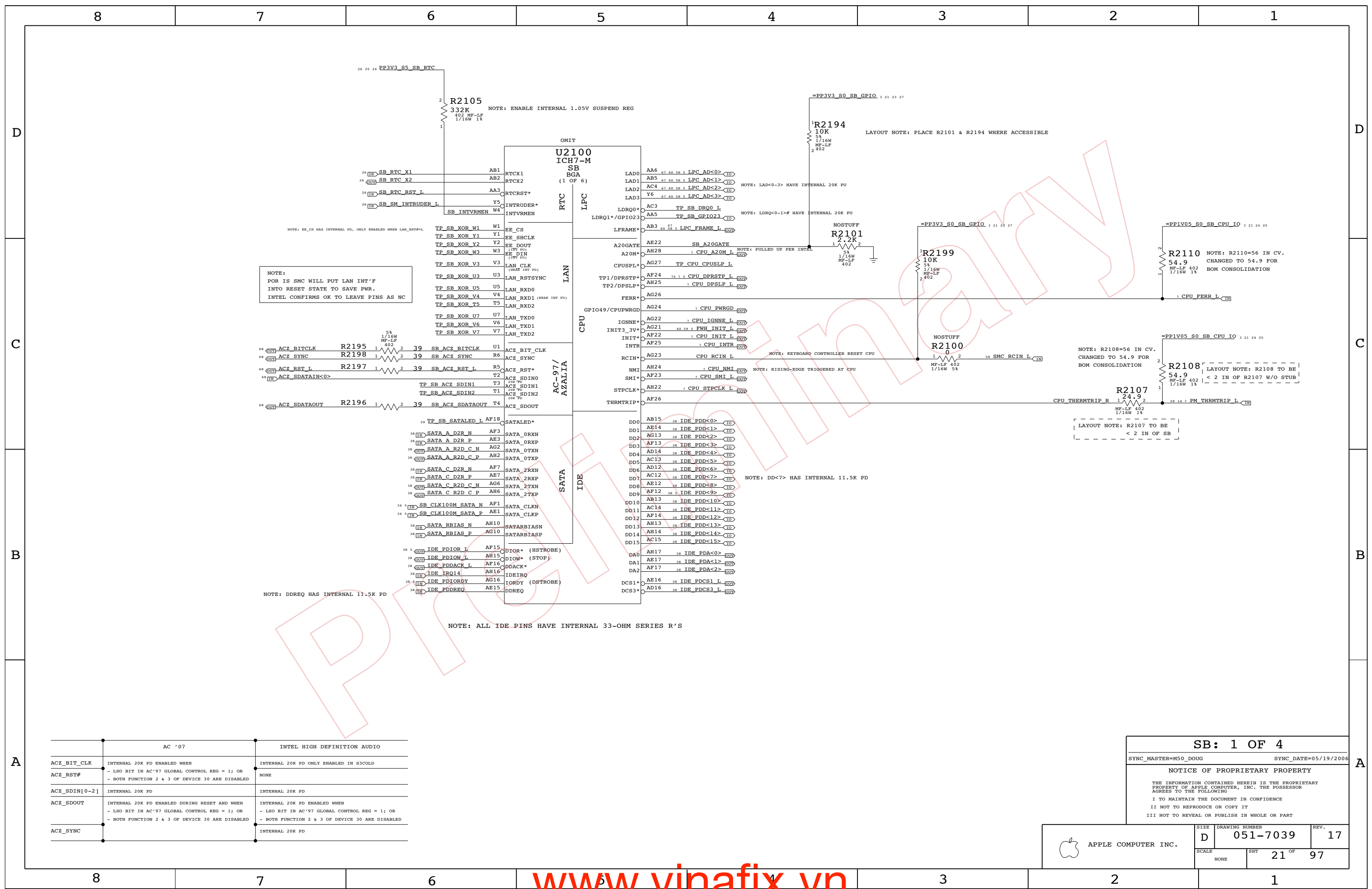
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7039	17
SCALE	SHT	20 OF	97
NONE			



NOTE:
POR IS SMC WILL PUT LAN INT'F
INTO RESET STATE TO SAVE PWR.
INTEL CONFIRMS OK TO LEAVE PINS AS NC

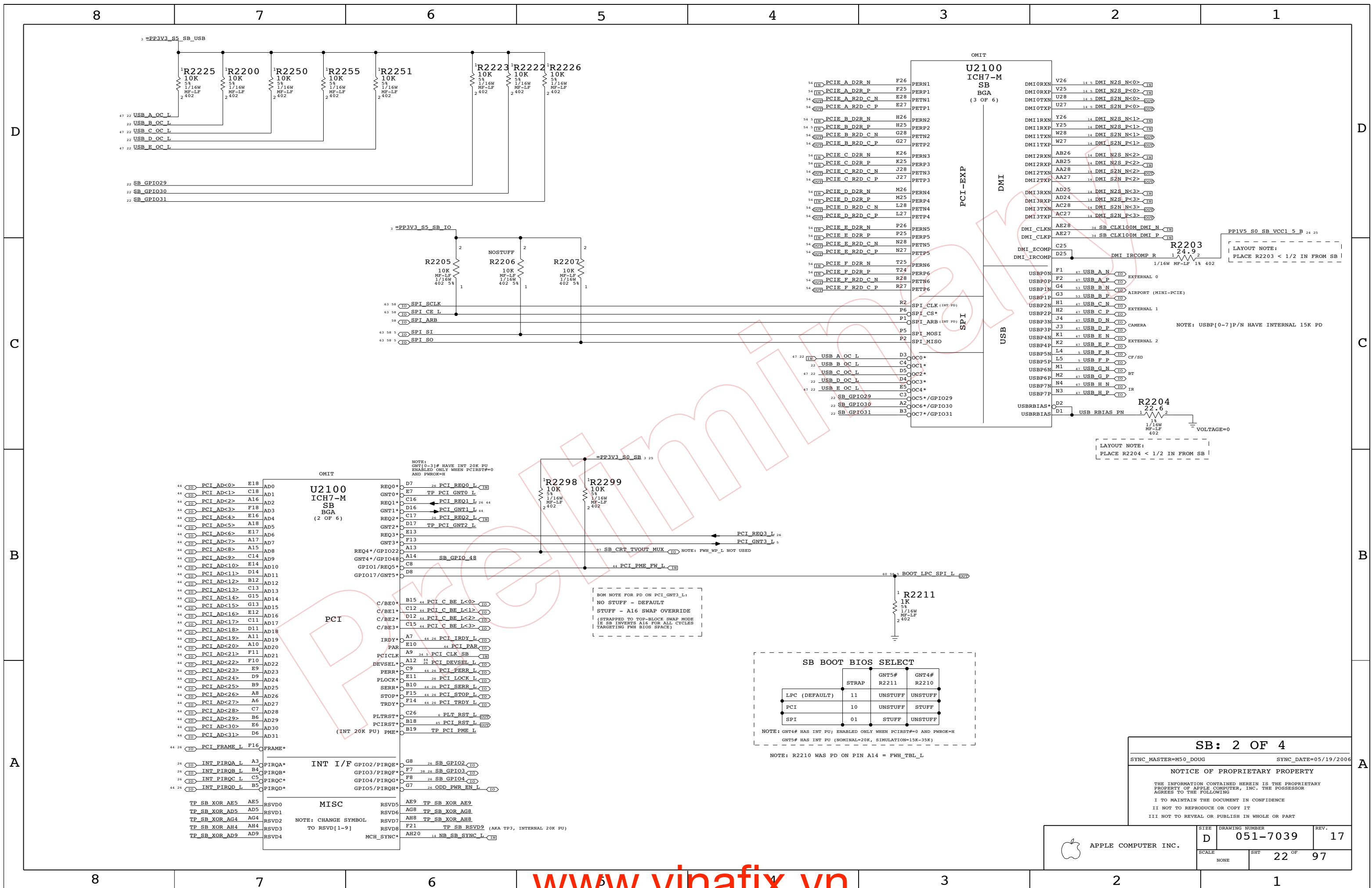
NOTE: DDREQ HAS INTERNAL 11.5K PD

NOTE: ALL IDE PINS HAVE INTERNAL 33-OHM SERIES R'S

AC '07	INTEL HIGH DEFINITION AUDIO
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR INTERNAL 20K PD ONLY ENABLED IN S3COLD
ACZ_RST#	NONE
ACZ_SDIN[0-2]	INTERNAL 20K PD
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
ACZ_SYNC	INTERNAL 20K PD

SB: 1 OF 4	
SYNC_MASTER=M50_DOUG	SYNC_DATE=05/19/2006
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	D	051-7039	17
SCALE	SHT	21 OF 97	
NONE			



SB BOOT BIOS SELECT

	STRAP	GNT5# R2211	GNT4# R2210
LPC (DEFAULT)	11	UNSTUFF	UNSTUFF
PCI	10	UNSTUFF	STUFF
SPI	01	STUFF	UNSTUFF

NOTE: GNT4# HAS INT PU; ENABLED ONLY WHEN PCIRST#0 AND PWR0R-H
GNT5# HAS INT PU (NOMINAL=20K, SIMULATION=15K-35K)
NOTE: R2210 WAS PD ON PIN A14 = FWH_TBL_L

SB: 2 OF 4

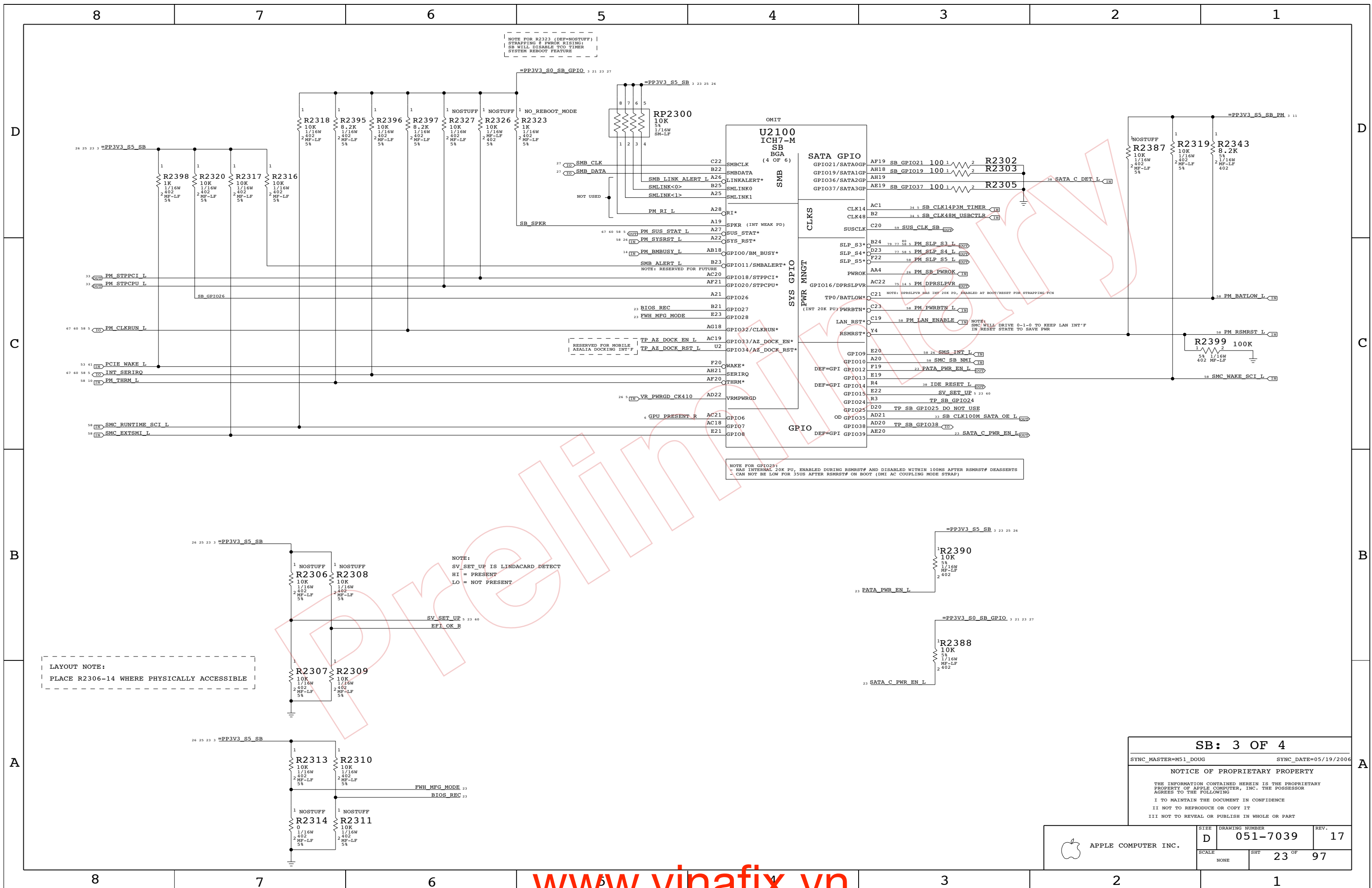
SYNC_MASTER=M50_D0UG SYNC_DATE=05/19/2006

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SCALE	SHT	22 OF 97	
NONE			



NOTE FOR R2323 (DEF=NOSTUFF) | STRAPPING & PWROK RISING: SB WILL DISABLE TOO TIMER SYSTEM REBOOT FEATURE

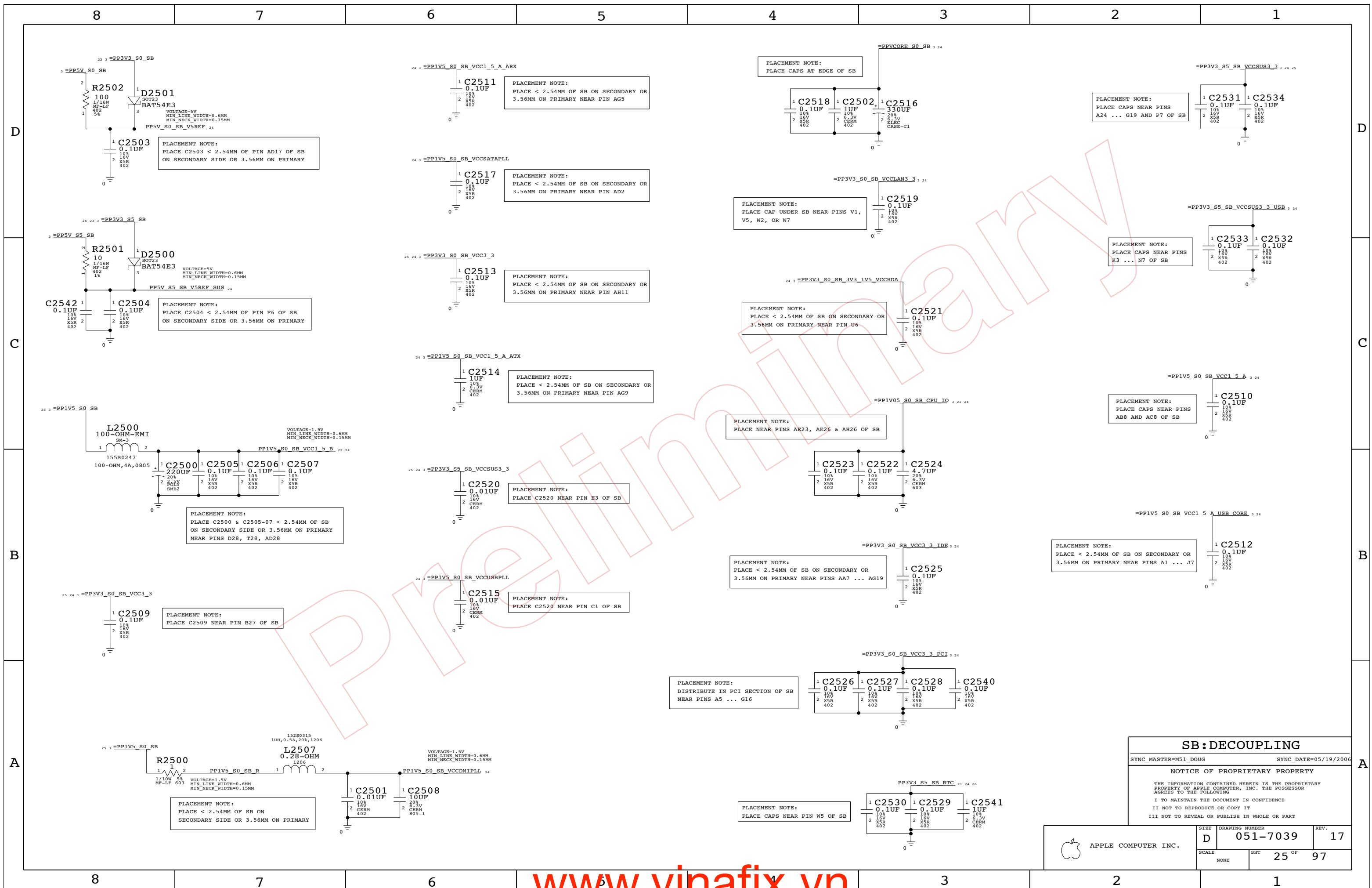
NOTE FOR GPIO25:
 * HAS INTERNAL 20K PU, ENABLED DURING RSMRST# AND DISABLED WITHIN 100MS AFTER RSMRST# DEASSERTS
 * CAN NOT BE LOW FOR 35US AFTER RSMRST# ON BOOT (DMI AC COUPLING MODE STRAP)

LAYOUT NOTE:
 PLACE R2306-14 WHERE PHYSICALLY ACCESSIBLE

NOTE:
 SV_SET_UP IS LINDACARD DETECT
 HI = PRESENT
 LO = NOT PRESENT

SB: 3 OF 4
 SYNC_MASTER=M51_D0UG SYNC_DATE=05/19/2006
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	D	051-7039	17
SCALE	SHT		23 OF 97
NONE			



SB: DECOUPLING

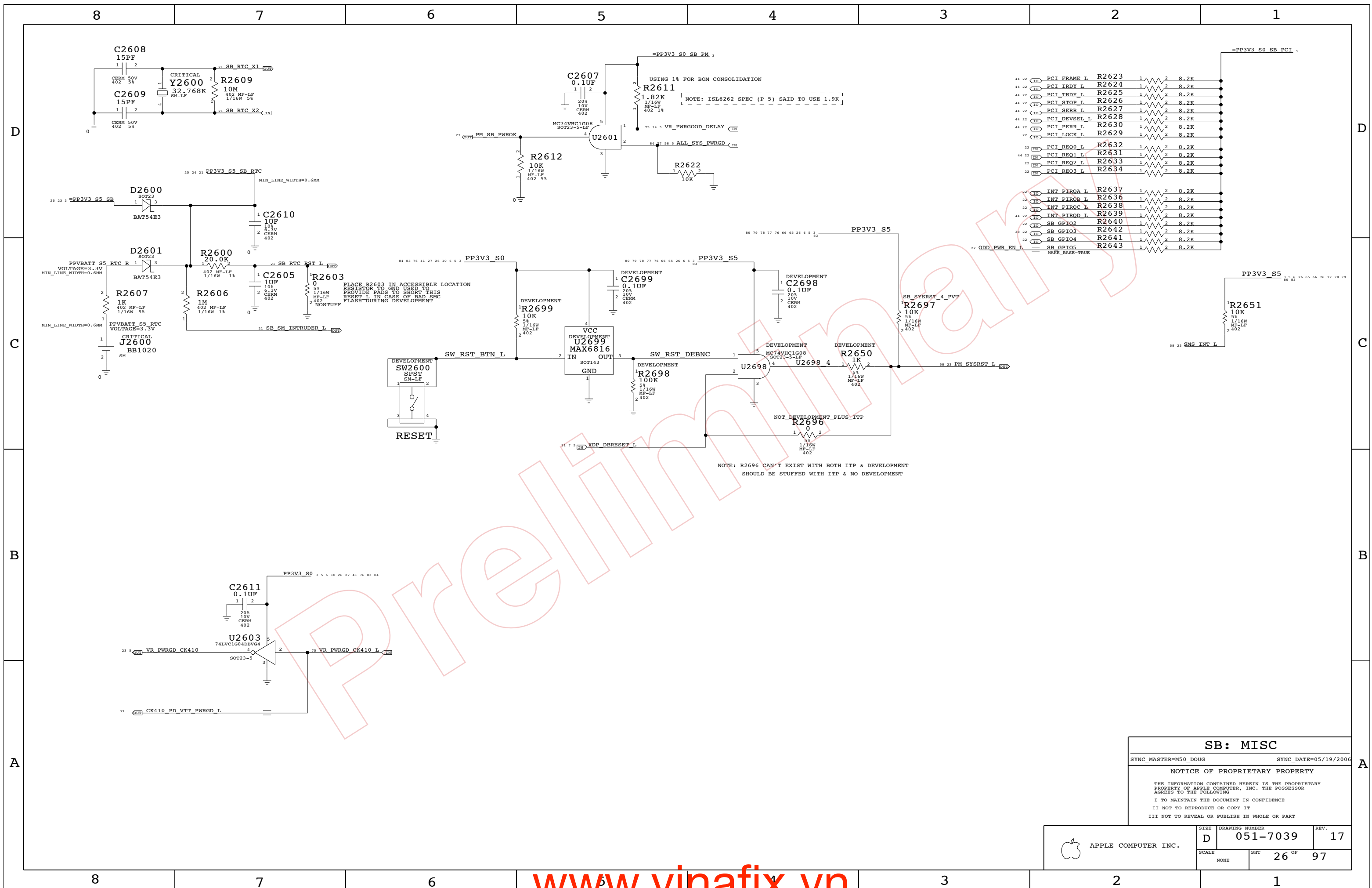
SYNC_MASTER=M51_D0UG SYNC_DATE=05/19/2006

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APPLE COMPUTER INC.	SCALE	SHT	REV.
	NONE	25 OF 97	17



SB: MISC

SYNC_MASTER=M50_DOUG SYNC_DATE=05/19/2006

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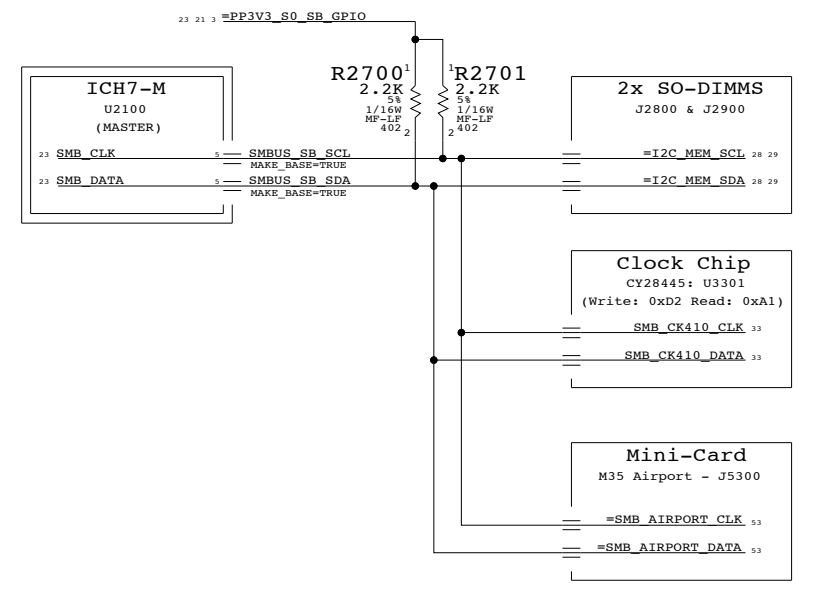
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

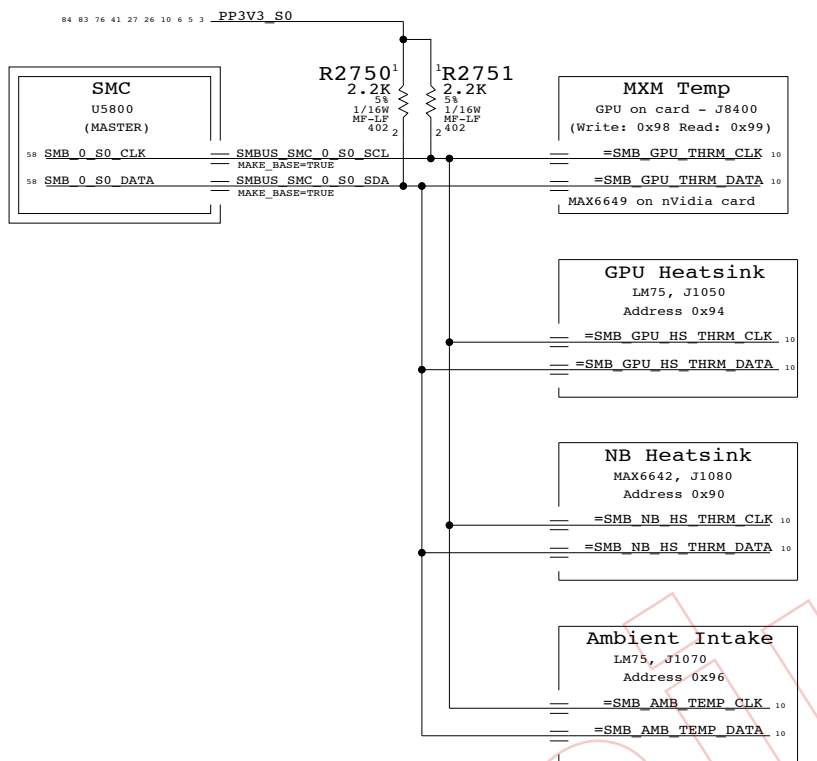
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7039	17
SCALE	SHT		OF
NONE	26		97

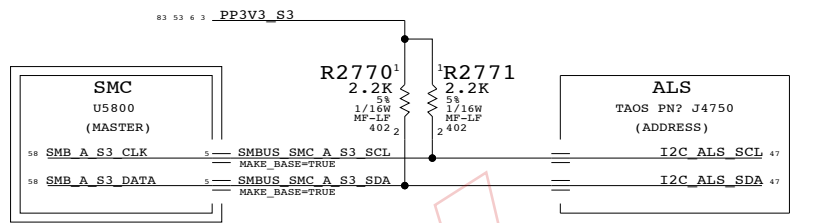
ICH7-M SMBus Connections



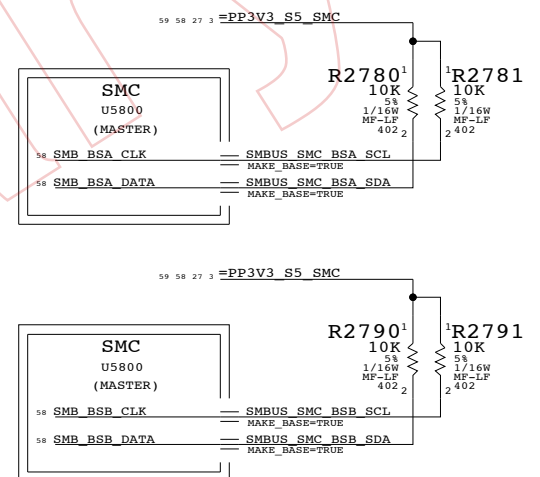
SMC "0" SMBus Connections



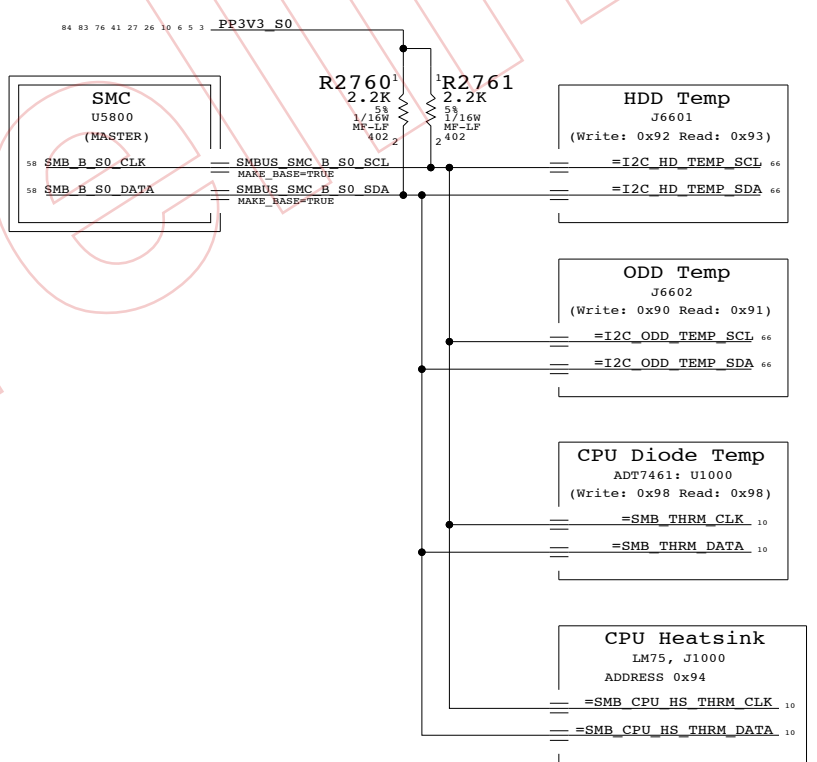
SMC "A" SMBus Connections



Unused SMC "Battery A/B" SMBus



SMC "B" SMBus Connections



M51 SMBus Connections

SYNC_MASTER=M51_DAVE SYNC_DATE=(MASTER)

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	D	051-7039	17
SCALE	SHT	27 OF	97
NONE			

Page Notes

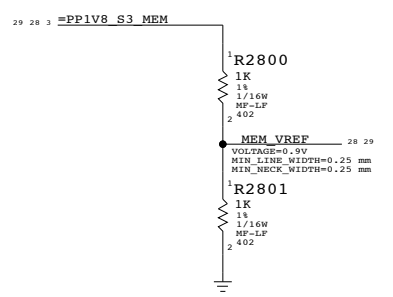
Power aliases required by this page:
 - =PP1V8_S3_MEM
 - =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
 - =I2C_MEM_SCL
 - =I2C_MEM_SDA

BOM options provided by this page:
 (NONE)

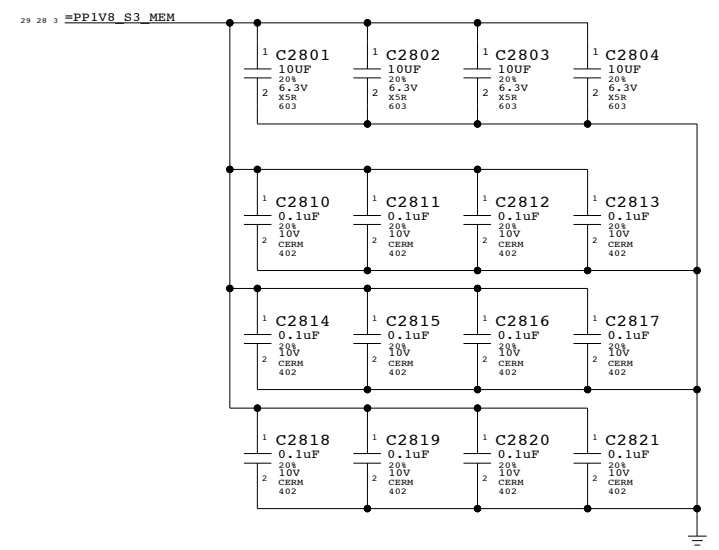
DDR2 VRef

One 0.1uF per connector



DDR2 Bypass Caps

(For return current)



DDR2 SO-DIMM Connector A

SYNC_MASTER=M50_HENRY SYNC_DATE=05/19/2006

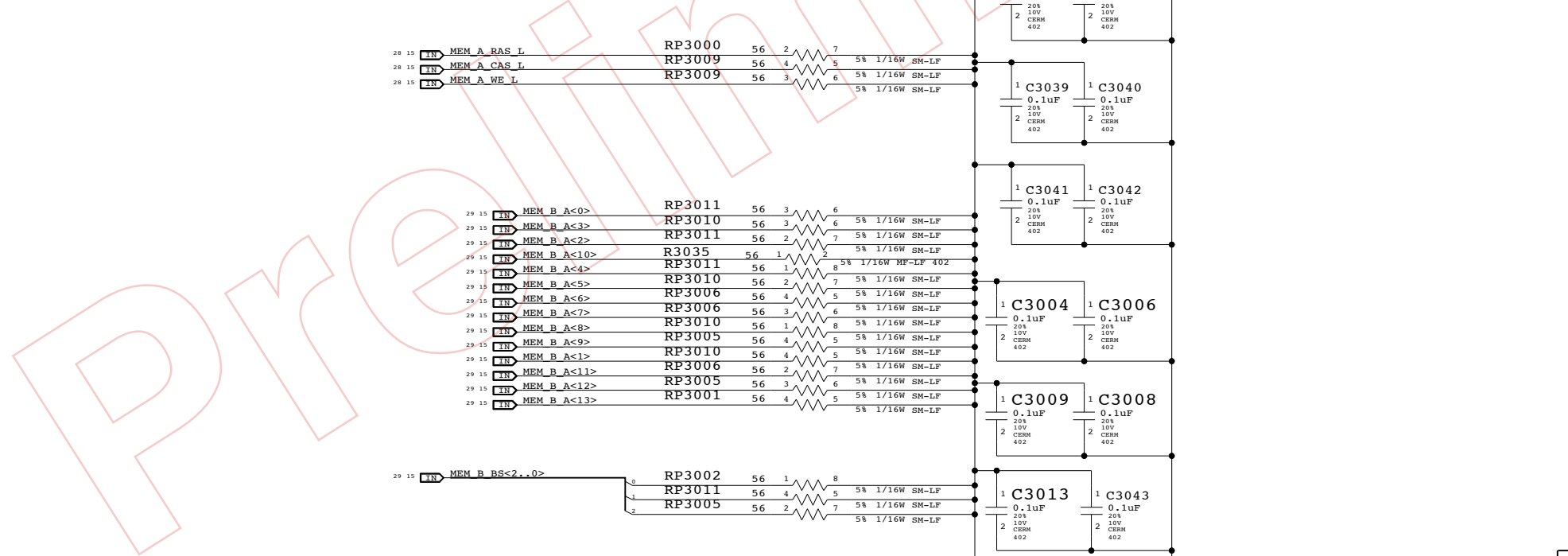
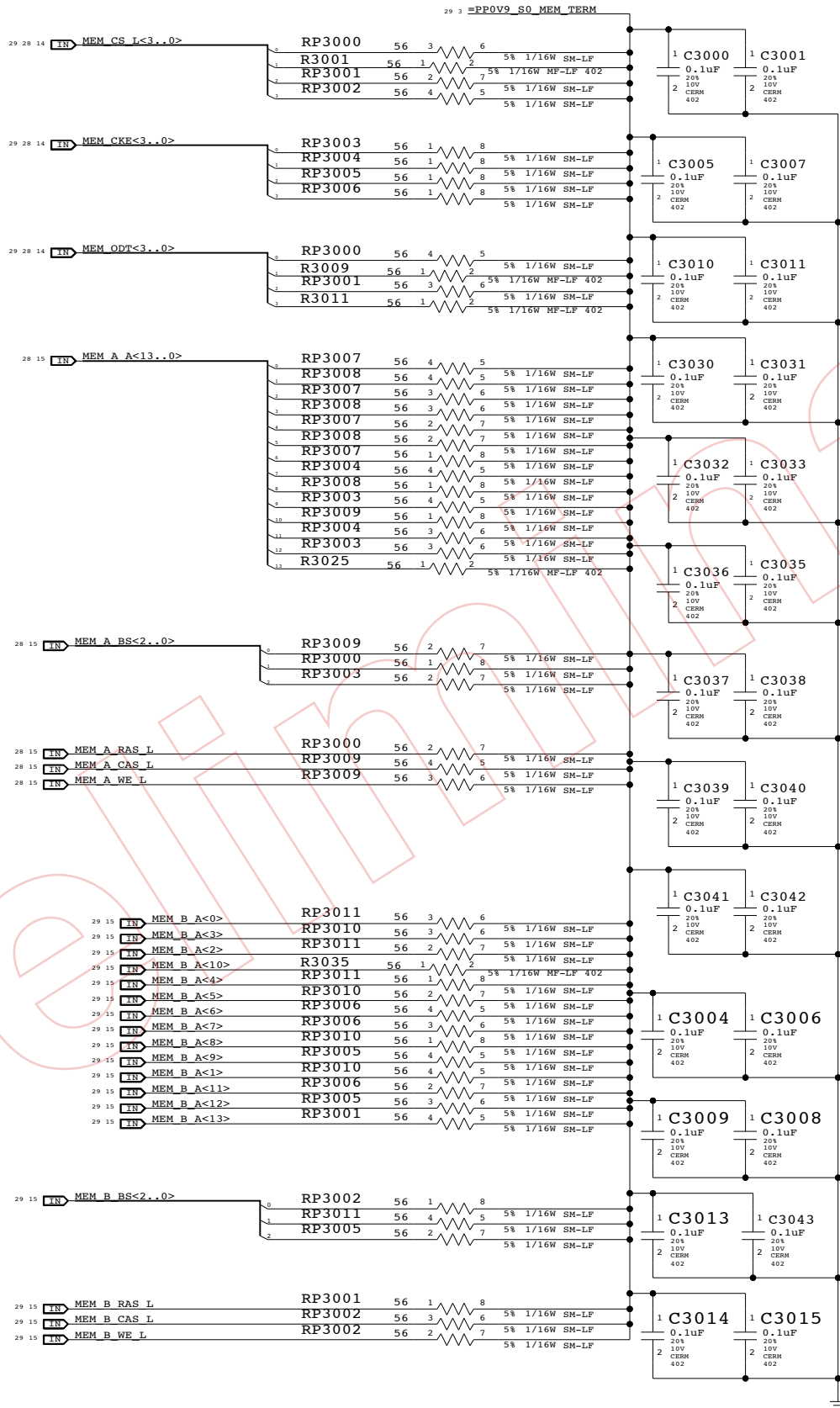
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SCALE	SHT	28 OF	97
NONE			

One cap for each side of every RPAK, one cap for every two discrete resistors
BOMOPTION shown at the top of each group applies to every part below it



Memory Active Termination

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	D	051-7039	17
SCALE	SHT	OF	
NONE	30	97	

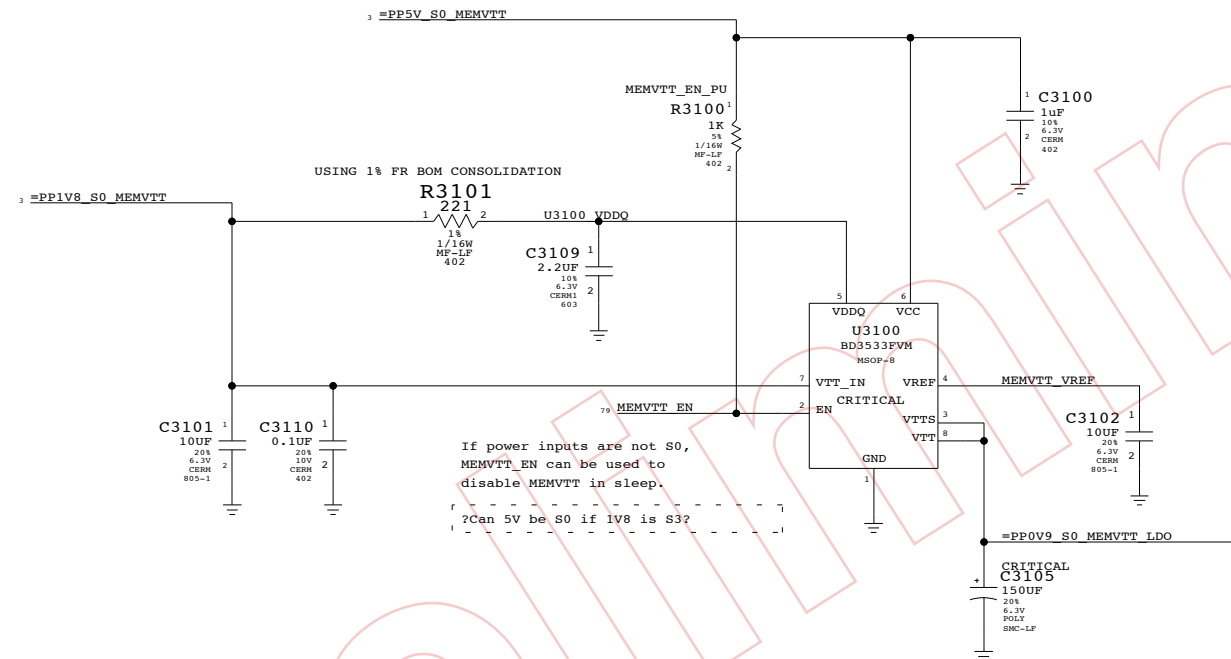
Page Notes

Power aliases required by this page:
 - =PP5V_S0_MEMVTT
 - =PP1V8_S0_MEMVTT
 - =PP0V9_S0_MEMVTT_LDO

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

DDR2 Vtt Regulator



Memory Vtt Supply
 SYNC_MASTER=M50_HENRY SYNC_DATE=05/19/2006
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7039	17
SCALE	SHT	31 OF 97	
NONE			

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C

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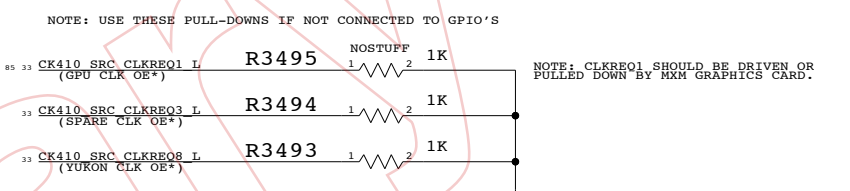
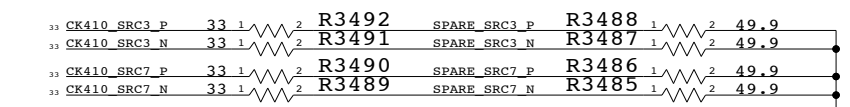
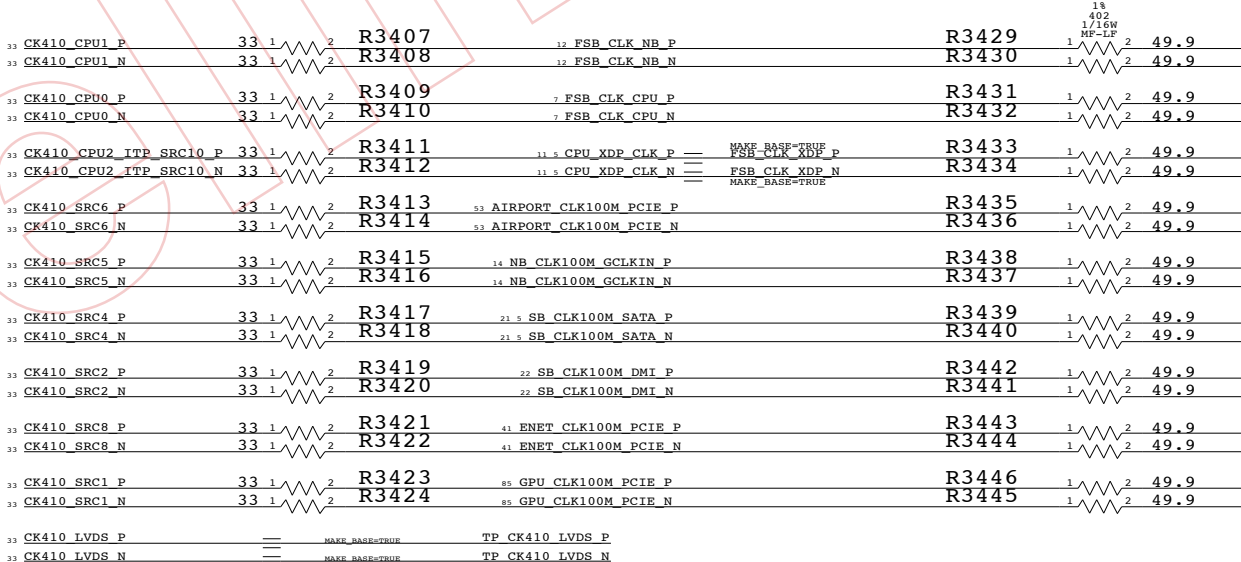
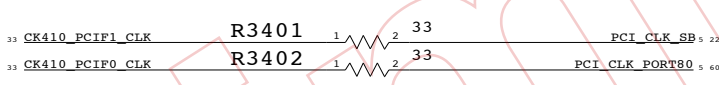
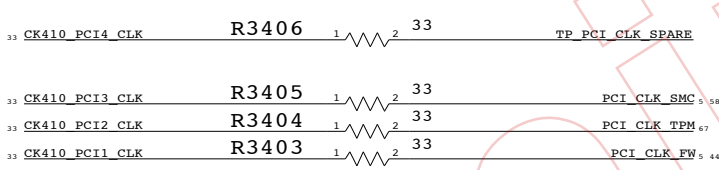
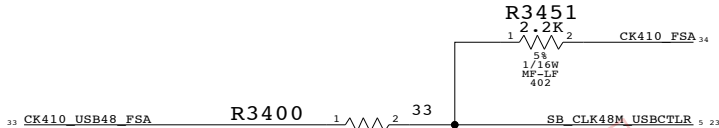
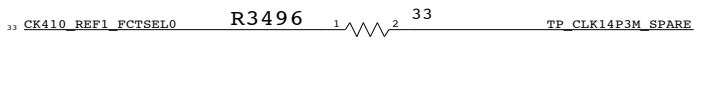
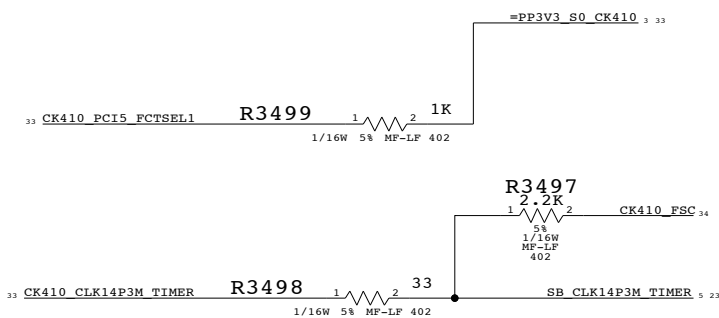
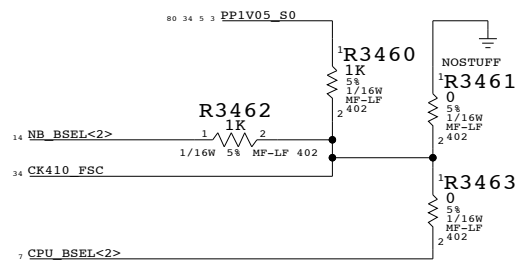
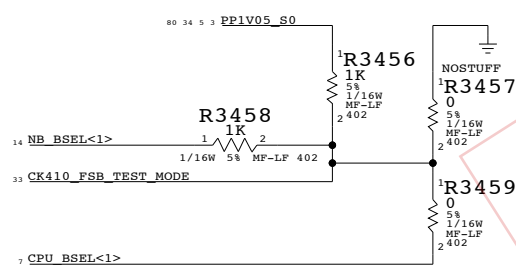
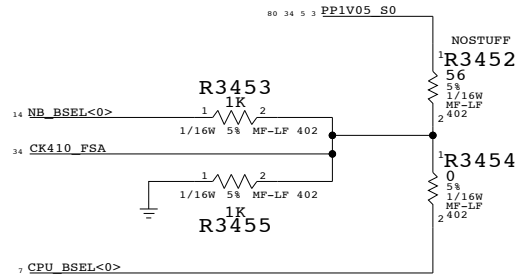
B

A

A

FSB FREQUENCY SELECT:

	STUFF	NO STUFF
CPU DRIVEN	R3454 R3455 R3461	R3452 R3453 R3463
533MHZ (133MHZ CPU CLK)	R3459 R3460 R3461	R3454 R3455 R3463
667MHZ (166MHZ CPU CLK)	R3452 R3453 R3461	R3459 R3460 R3463



NOTE: USE THESE PULL-DOWNS IF NOT CONNECTED TO GPIO'S

NOTE: CLKREQ1 SHOULD BE DRIVEN OR PULLED DOWN BY HXM GRAPHICS CARD.

CLOCKS: TERMINATIONS

SYNC_MASTER=M51_HENRY SYNC_DATE=05/19/2006

NOTICE OF PROPRIETARY PROPERTY

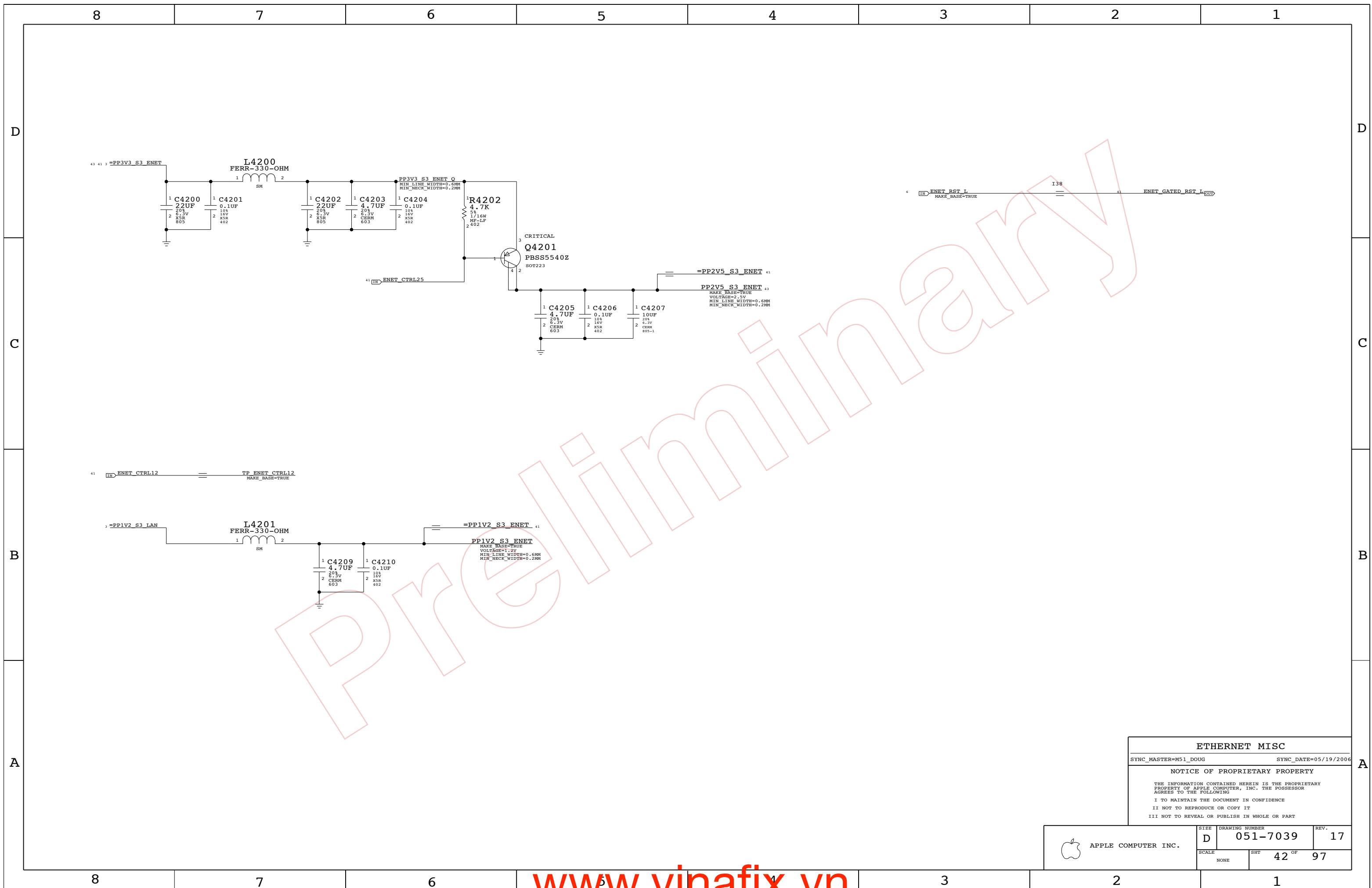
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SCALE	SHT		OF
NONE	34		97



ETHERNET MISC

SYNC_MASTER=M51_DOUG SYNC_DATE=05/19/2006

NOTICE OF PROPRIETARY PROPERTY

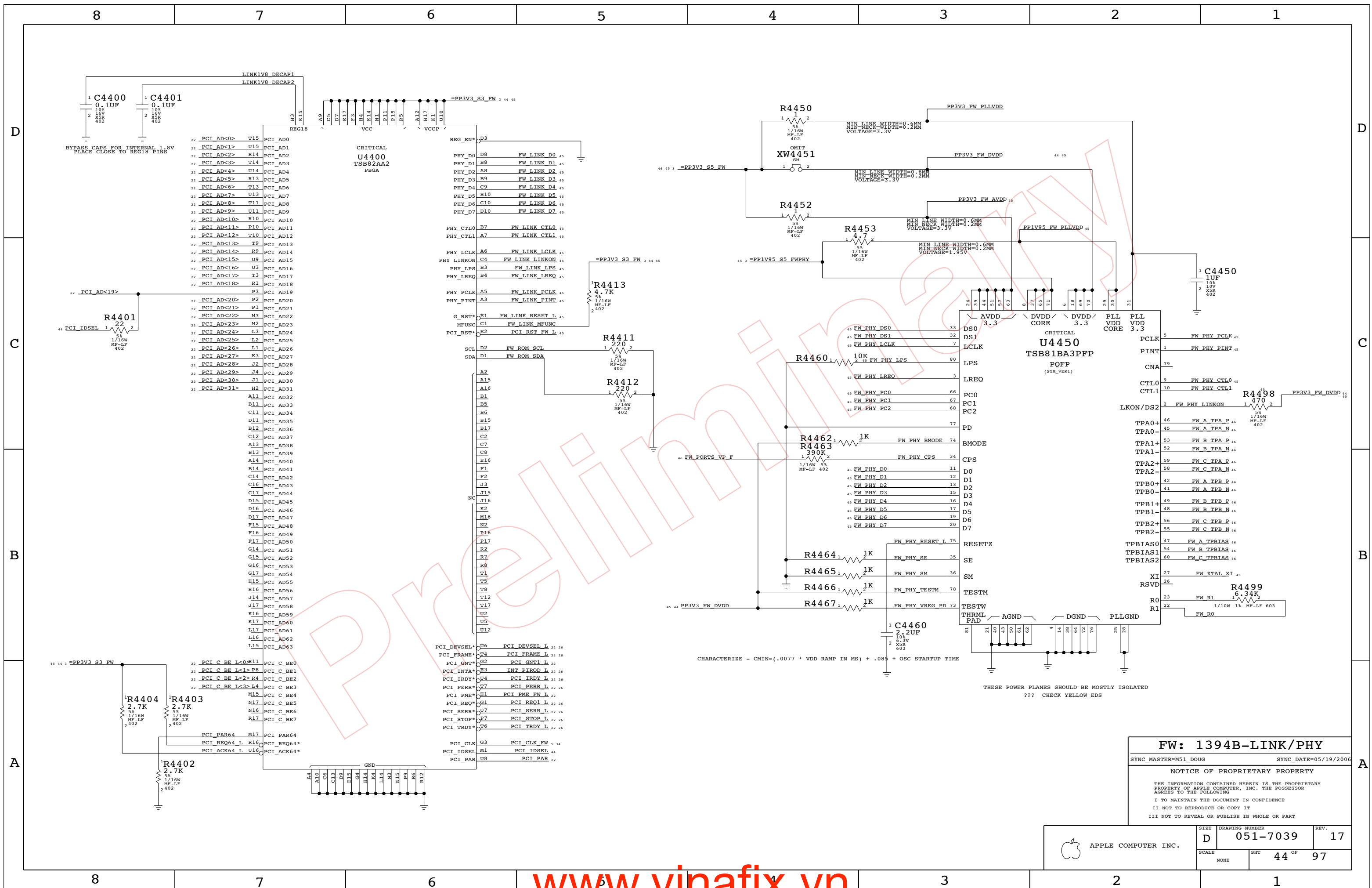
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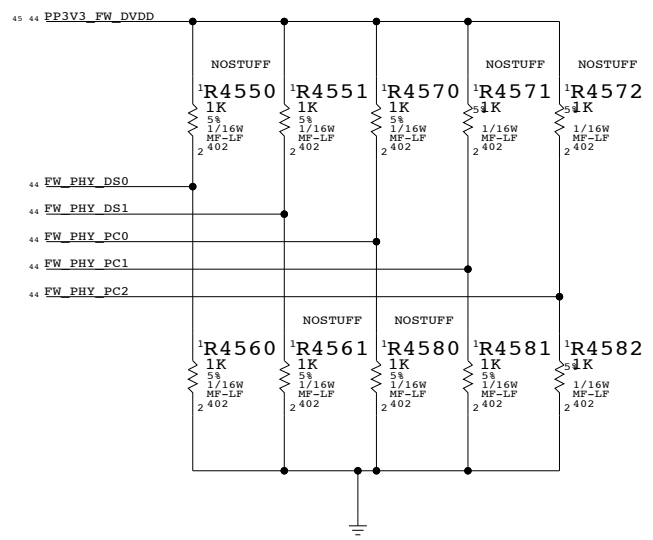
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7039	REV. 17
	SCALE NONE	SHT 42 OF	97



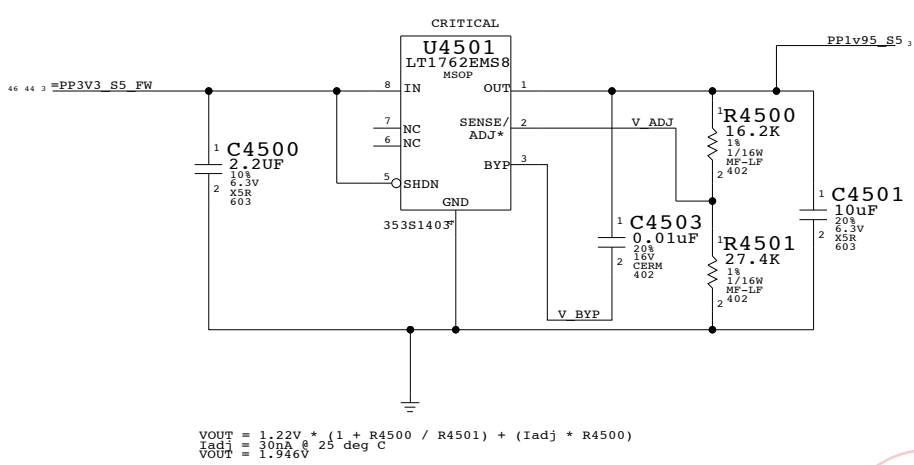
FW: 1394B-LINK/PHY	
SYNC_MASTER=M51 DOUG	SYNC_DATE=05/19/2006
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	D	051-7039	17
SCALE	SHT	44 OF	97
NONE			

1394 PHY DATA/STROBE AND POWER CLASS OPTIONS

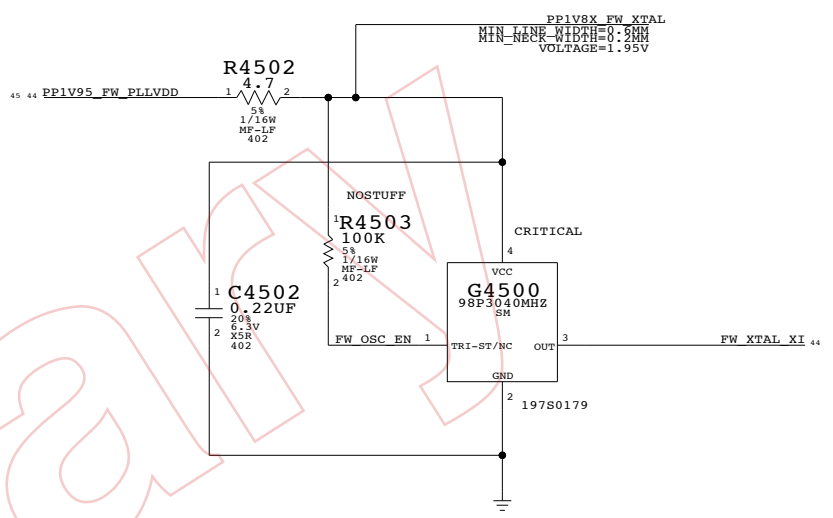


1394 PHY 1.95V REGULATOR



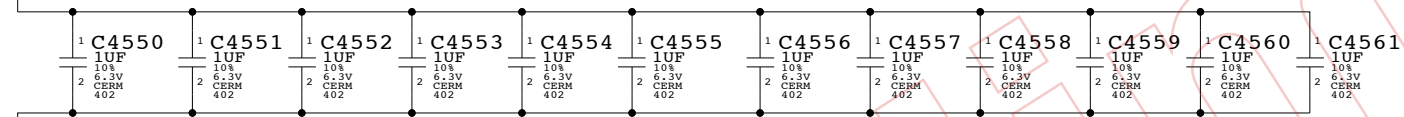
1394 PHY CRYSTAL OSCILLATOR

FIXME!!! CHARACTERIZE TO SEE IF THIS BRINGS US CLOSE ENOUGH TO 1.8V - 4.7 CHOSEN FOR BOM CONSOLIDATION



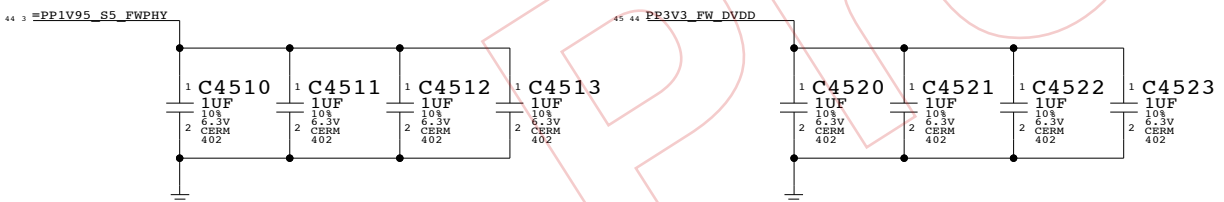
- FW LINK D0 MAKE_BASE=TRUE == FW_PHY_D0
 - FW LINK D1 MAKE_BASE=TRUE == FW_PHY_D1
 - FW LINK D2 MAKE_BASE=TRUE == FW_PHY_D2
 - FW LINK D3 MAKE_BASE=TRUE == FW_PHY_D3
 - FW LINK D4 MAKE_BASE=TRUE == FW_PHY_D4
 - FW LINK D5 MAKE_BASE=TRUE == FW_PHY_D5
 - FW LINK D6 MAKE_BASE=TRUE == FW_PHY_D6
 - FW LINK D7 MAKE_BASE=TRUE == FW_PHY_D7
 - FW LINK CTL0 MAKE_BASE=TRUE == FW_PHY_CTL0
 - FW LINK CTL1 MAKE_BASE=TRUE == FW_PHY_CTL1
 - FW LINK LCLK MAKE_BASE=TRUE == FW_PHY_LCLK
 - FW LINK LPS MAKE_BASE=TRUE == FW_PHY_LPS
 - FW LINK LREQ MAKE_BASE=TRUE == FW_PHY_LREQ
 - FW LINK PCLK MAKE_BASE=TRUE == FW_PHY_PCLK
 - FW LINK LINKON MAKE_BASE=TRUE == FW_PHY_LINKON
 - FW LINK PINT MAKE_BASE=TRUE == FW_PHY_PINT
- NOTE: 1K IS PER TI SPEC TO BALANCE OUT THE 470 PULLUP ON DS2
- NORMALLY TERMINATIONS WOULD GO HERE...
- SIMULATIONS SHOW THAT THERMINATIONS WERE NOT NEEDED FOR M51
- CONSTRAIN NETS TO 200-250PS IF NO TERM-Rs...

LINK DECOUPLING

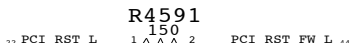
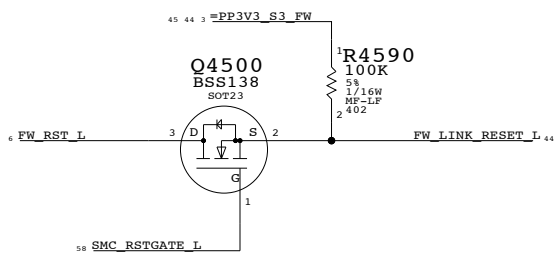


NOTE: PLACE 1 CAP CLOSE TO EACH POWER PIN ON U4400

PHY DECOUPLING



1394 LINK POWER ON RESET AND PCI RESET



NOTE: 1% FOR BOM CONSOLIDATION(APPLIED TO M50)

NOTE: R SHOULD BE CHOSEN TO PREVENT OVERSHOOT

NOTE: PLACE 1 CAP CLOSE TO EACH POWER PIN ON U4450

FW: 1394B MISC

SYNC_MASTER=M51 DOUG SYNC_DATE=05/19/2006

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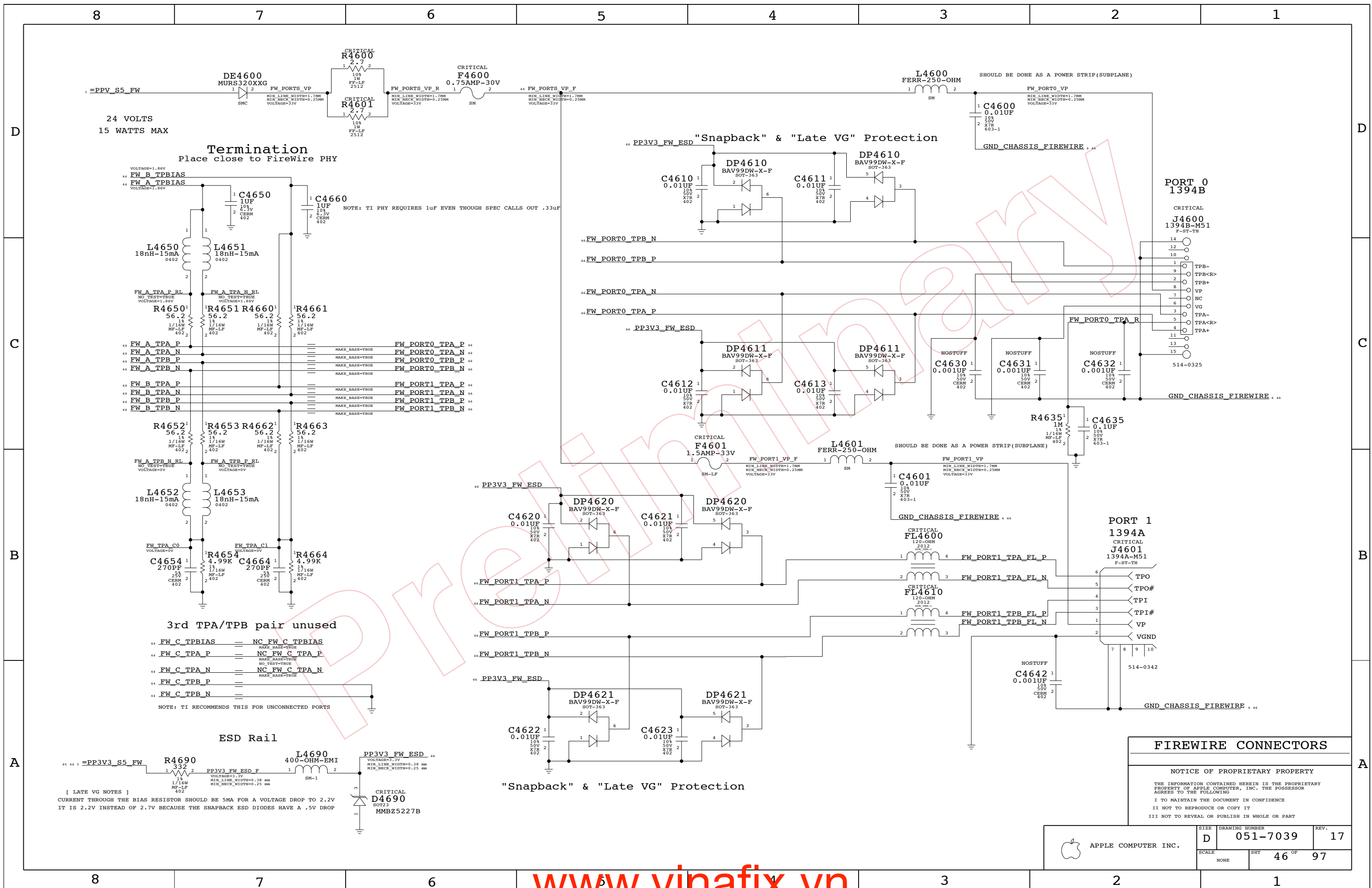
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	D	051-7039	17
SCALE	SHT	45 OF	97
NONE			



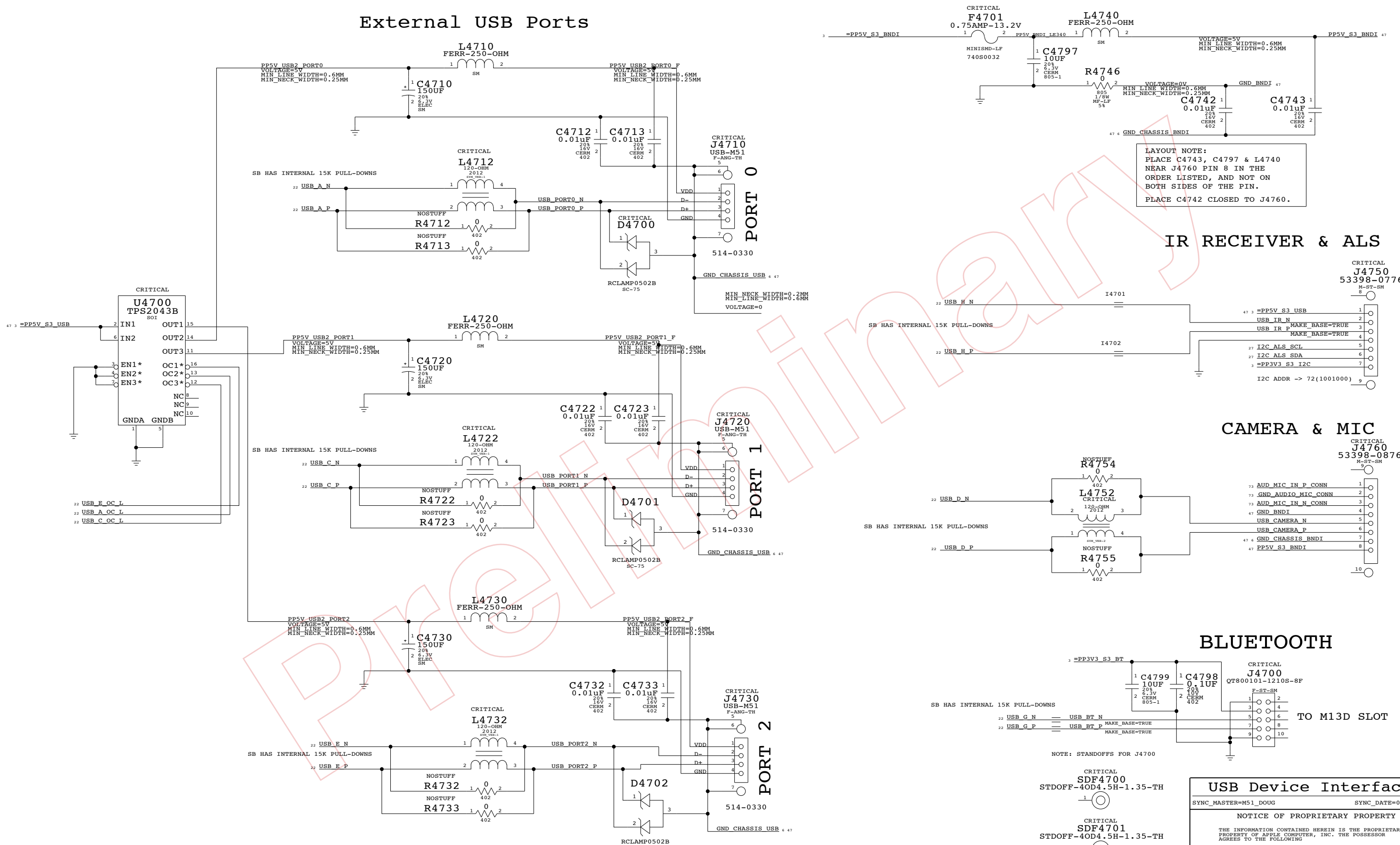
FIREWIRE CONNECTORS

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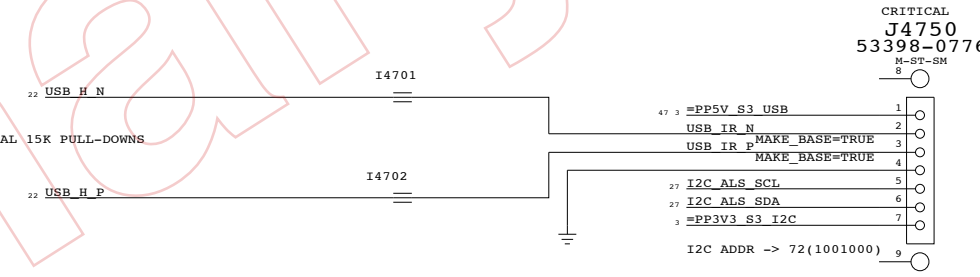
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7039	17
SCALE	SHT	46 OF	97
NONE			

External USB Ports

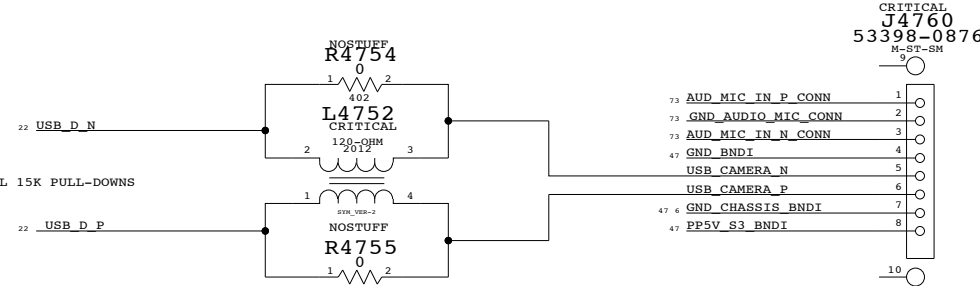


LAYOUT NOTE:
PLACE C4743, C4797 & L4740
NEAR J4760 PIN 8 IN THE
ORDER LISTED, AND NOT ON
BOTH SIDES OF THE PIN.
PLACE C4742 CLOSED TO J4760.

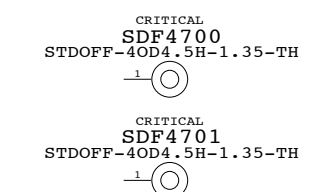
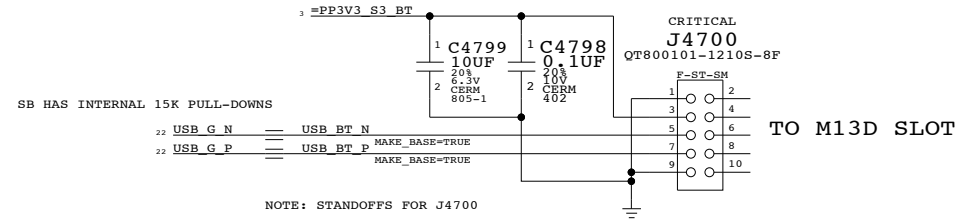
IR RECEIVER & ALS



CAMERA & MIC



BLUETOOTH



USB Device Interfaces

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	D	051-7039	17
SCALE	SHT	47 OF	97
NONE			

8

7

6

5

4

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D

C

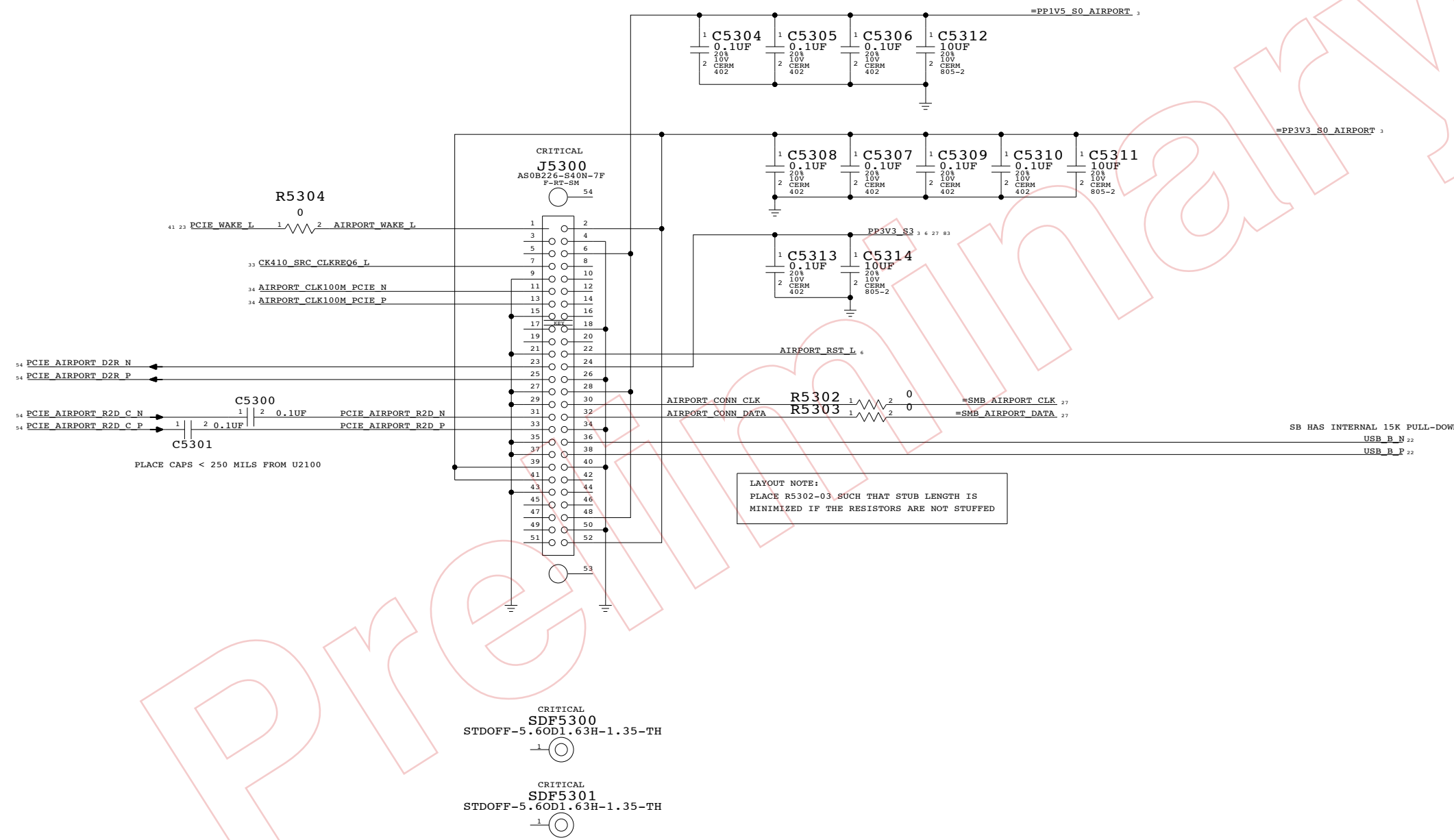
C

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A

A



AIRPORT CONN

SYNC_MASTER=M51_DOUG SYNC_DATE=05/19/2006

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	D	051-7039	17
SCALE	SHT	REV.	
NONE	53 OF	97	

8

7

6

5

4

3

2

1

D

D

C

C

B

B

A

A

PCI-E X1 PORT "A" = ETHERNET (YUKON)

22 PCIE_A_R2D_C_N == PCIE_ENET_R2D_C_N 41
MAKE_BASE=TRUE

22 PCIE_A_R2D_C_P == PCIE_ENET_R2D_C_P 41
MAKE_BASE=TRUE

22 PCIE_A_D2R_N == PCIE_ENET_D2R_N 41
MAKE_BASE=TRUE

22 PCIE_A_D2R_P == PCIE_ENET_D2R_P 41
MAKE_BASE=TRUE

PCI-E X1 PORT "B" = MINI CARD (AIRPORT)

22 PCIE_B_R2D_C_N == PCIE_AIRPORT_R2D_C_N 53
MAKE_BASE=TRUE

22 PCIE_B_R2D_C_P == PCIE_AIRPORT_R2D_C_P 53
MAKE_BASE=TRUE

22 PCIE_B_D2R_N == PCIE_AIRPORT_D2R_N 53
MAKE_BASE=TRUE

22 PCIE_B_D2R_P == PCIE_AIRPORT_D2R_P 53
MAKE_BASE=TRUE

PCI-E X1 PORTS C, D, E, F = UNUSED

22 PCIE_C_R2D_C_N == TP_PCIE_C_R2D_C_N
MAKE_BASE=TRUE

22 PCIE_C_R2D_C_P == TP_PCIE_C_R2D_C_P
MAKE_BASE=TRUE

22 PCIE_C_D2R_N == TP_PCIE_C_D2R_N
MAKE_BASE=TRUE

22 PCIE_C_D2R_P == TP_PCIE_C_D2R_P
MAKE_BASE=TRUE

22 PCIE_D_R2D_C_N == TP_PCIE_D_R2D_C_N
MAKE_BASE=TRUE

22 PCIE_D_R2D_C_P == TP_PCIE_D_R2D_C_P
MAKE_BASE=TRUE

22 PCIE_D_D2R_N == TP_PCIE_D_D2R_N
MAKE_BASE=TRUE

22 PCIE_D_D2R_P == TP_PCIE_D_D2R_P
MAKE_BASE=TRUE

22 PCIE_E_R2D_C_N == TP_PCIE_E_R2D_C_N
MAKE_BASE=TRUE

22 PCIE_E_R2D_C_P == TP_PCIE_E_R2D_C_P
MAKE_BASE=TRUE

22 PCIE_E_D2R_N == TP_PCIE_E_D2R_N
MAKE_BASE=TRUE

22 PCIE_E_D2R_P == TP_PCIE_E_D2R_P
MAKE_BASE=TRUE

22 PCIE_F_R2D_C_N == TP_PCIE_F_R2D_C_N
MAKE_BASE=TRUE

22 PCIE_F_R2D_C_P == TP_PCIE_F_R2D_C_P
MAKE_BASE=TRUE

22 PCIE_F_D2R_N == TP_PCIE_F_D2R_N
MAKE_BASE=TRUE

22 PCIE_F_D2R_P == TP_PCIE_F_D2R_P
MAKE_BASE=TRUE

Preliminary

PCI-E CONNECTIONS

SYNC_MASTER=M51_DOUG SYNC_DATE=05/19/2006

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NONE	54	97	

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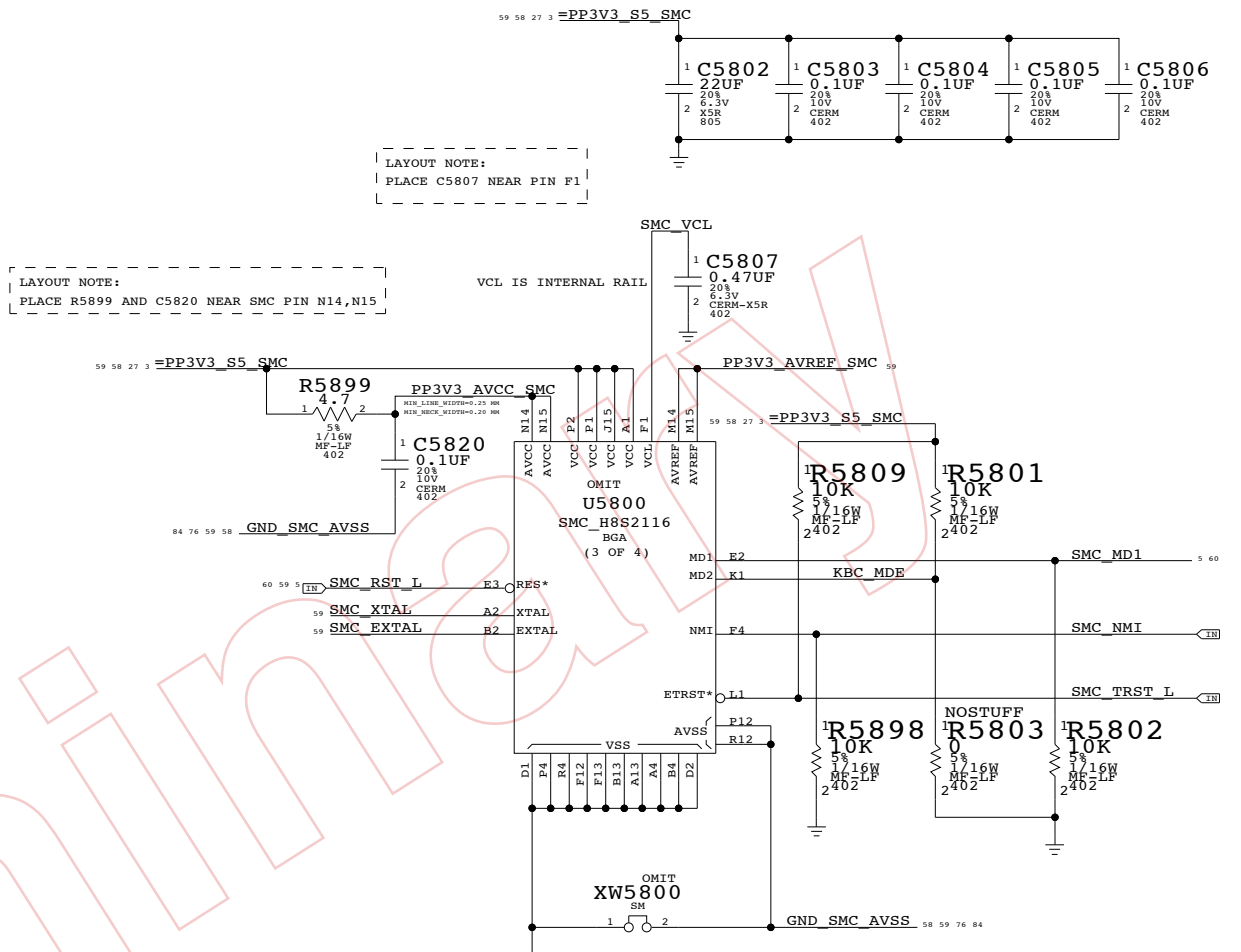
1

UNUSED PINS HAVE THE FORMAT SMC_XXX WHERE XXX IS THE PORT NUMBER. THEY ARE SET BY SOFTWARE TO BE DRIVEN OUTPUTS ALWAYS SO THEY CAN BE LEFT NO-CONNECTED.

Pin	Signal	Port	Pin	Signal	Port
23	PM_LAN_ENABLE	B12	P10	SMC_PM_G2_EN	OUT
23	SMC_RSTGATE_L	C13	P11	SMC_ADAPTER_EN	OUT
84 77 26	ALL_SYS_PWRGD	A15	P12	SPI_ARB	IN
74	RSMRST_PWRGD	B14	P13	SPI_SCLK	IN
23	SMC_SB_NMI	B15	P14	SPI_SI	OUT
23	PM_RSMRST_L	C14	P15	SPI_SO	IN
75	IMVP_VR_ON	D12	P16	SMC_PROCHOT_3_3_L	IN
23	PM_PWRBTN_L	C15	P17	SMC_CPU_INIT_3_3_L	IN
59	SMC_P20	D13	P20	SMC_CPU_ISENSE	IN
59	SMC_P21	D14	P21	SMC_CPU_VSENSE	IN
59	SMC_P22	D15	P22	SMC_GPU_ISENSE	IN
59	SMC_P23	E12	P23	SMC_GPU_VSENSE	IN
59	SMC_BATT_TRICKLE_EN_L	E14	P24	SMC_DCIN_ISENSE	IN
59	SMC_BATT_CHG_EN	E15	P25	SMC_PBUS_VSENSE	IN
59	SMC_P26	E13	P26	SMC_BATT_ISENSE	IN
59	SMC_P27	F14	P27	SMC_FWIRE_ISENSE	IN
67 60 21 5	LPC_AD<0>	D9	P30/LAD0	SMC_WAKE_SCI_L	IN
67 60 21 5	LPC_AD<1>	C9	P31/LAD1	SMC_TPM_GPIO	OUT
67 60 21 5	LPC_AD<2>	A9	P32/LAD2	PM_CLKRUN_L	IO
67 60 21 5	LPC_AD<3>	B9	P33/LAD3	PM_SUS_STAT_L	IN
67 60 21 5	LPC_FRAME_L	D8	P34/LFRAME*	SMC_TX_L	OUT
67 60 21 5	SMC_LRESET_L	C8	P35/LRESET*	SMC_RX_L	OUT
34	PCI_CLK_SMC	A8	P36/LCLK	SMB_BSB_CLK	IO
67 60 21 5	INT_SERIRQ	D7	P37/SERIRQ	SMC_ONOFF_L	IN
59	SMC_XDP_TMS	A5	P40/TMIO	SMC_BC_ACOG	IN
59	SMC_SYS_LED_16B	B5	P41/TMO0	SMC_BS_ALRT_L	IN
27	SMB_BSB_DATA	D5	P42/SDA1	PM_SLP_S3_L	IN
59	SMC_TPM_PP	C3	P43/TM11/EXSCK1	PM_SLP_S4_L	IN
59	SMC_XDP_TRST_L	B1	P44/TM01	PM_SLP_S5_L	IN
59	SMC_XDP_TCK	C2	P45	SMC_SUS_CLK	IN
59	SMC_SYS_LED	D3	P46/PWX0/PWM0	SMB_0_S0_DATA	IO
59	SMC_SYS_KBDLED	C1	P47/PWX1/PWM1		
60 59 5	SMC_TX_L	G1	P50		
60 59 5	SMC_RX_L	G4	P51		
27	SMB_0_S0_CLK	F2	P52/SCL0		

Pin	Signal	Port	Pin	Signal	Port
21	SMC_RCIN_L	R3	PA0/KIN8*/PA2DC	SMC_CASE_OPEN	IN
60 22 5	BOOT_LPC_SPI_L	P3	PA1/KIN9*/PA2DD	SMC_TCK	IN
23	PM_SYSRST_L	R2	PA2/KIN10*/PS2AC	SMC_TDI	IN
67 60 21 5	SMC_TPM_RESET_L	N3	PA3/KIN11*/PS2AD	SMC_TDO	OUT
59	PM_EXTTLS_L	R1	PA4/KIN12*/PS2BC	SMC_TMS	IN
23 10	PM_THRM_L	N2	PA5/KIN13*/PS2BD		
59	SYS_ONEWIRE	M4	PA6/KIN14*/PS2CC	SMC_PPF0	59
23	PM_BATLOW_L	N1	PA7/KIN15*/PS2CD	SMC_PPF1	59
23	SMC_EXTSMI_L	B10	PB0/LSMI*	SMC_LID	IN
23	SMC_RUNTIME_SCI_L	A10	PB1/LSCI	SMC_CPU_RESET_3_3_L	IN
59	SMC_ODD_DETECT	D10	PB2	SMC_BATT_ISET	OUT
59	ISENSE_CAL_EN	A11	PB3	SMC_BATT_VSET	OUT
59	SMC_EXCARD_CP	B11	PB4	SMC_SYS_ISET	OUT
59	SMC_EXCARD_PWR_EN	C11	PB5	SMC_SYS_VSET	OUT
59	SMC_EXCARD_OC_L	A12	PB6		
59	SMC_XDP_TDO_3_3	D11	PB7	SPI_CE_L	IO
65	SMC_FAN_0_CTL	G14	PC0/TIOCA0/WUE8*	SMC_XDP_TCK_3_3	IN
65	SMC_FAN_1_CTL	G15	PC1/TIOCBO/WUE9*	SMB_BSA_DATA	IO
65	SMC_FAN_2_CTL	G13	PC2/TIOCC0/TCLKA/WUE10*	SMB_A_S3_DATA	IO
65	SMC_FAN_3_CTL	G12	PC3/TIOCDO/TCLKB/WUE11*	SMB_A_S3_CLK	IO
65	SMC_FAN_0_TACH	H14	PC4/TIOCA1/WUE12*	SMB_B_S0_DATA	IO
65	SMC_FAN_1_TACH	H15	PC5/TIOCB1/TCLKC/WUE13*	SMB_B_S0_CLK	IO
65	SMC_FAN_2_TACH	H13	PC6/TIOCA2/WUE14*		
65	SMC_FAN_3_TACH	H12	PC7/TIOCB2/TCLKD/WUE15*	SMC_PROCHOT	OUT
59	SMS_X_AXIS	M11	PD0/AN8	SMC_THRMTRIP	OUT
59	SMS_Y_AXIS	P11	PD1/AN9	SMC_FWE	IN
59	SMS_Z_AXIS	R11	PD2/AN10	ALS_GAIN	OUT
59	SMC_ANALOG_ID	N11	PD3/AN11	SMS_INT_L	OUT
59	SMC_NB_ISENSE	P10	PD4/AN12	SMC_ONOFF_L	OUT
59	SMC_MEM_ISENSE	R10	PD5/AN13		
59	ALS_LEFT	N10	PD6/AN14		
59	ALS_RIGHT	M10	PD7/AN15		

Pin	Signal	Port	Pin	Signal	Port
G3	NC0		NC12	E15	
H3	NC1		NC13	A14	
K3	NC2		NC14	C12	
L3	NC3		NC15	C10	
M4	NC4		NC16	C5	
N5	NC5		NC17	A3	
N7	NC6		NC18	B8	
M12	NC7		NC19	E4	
M13	NC8		NC20	H4	
L12	NC9		NC21	M9	
K15	NC10		NC22	N8	
J14	NC11				



SMC

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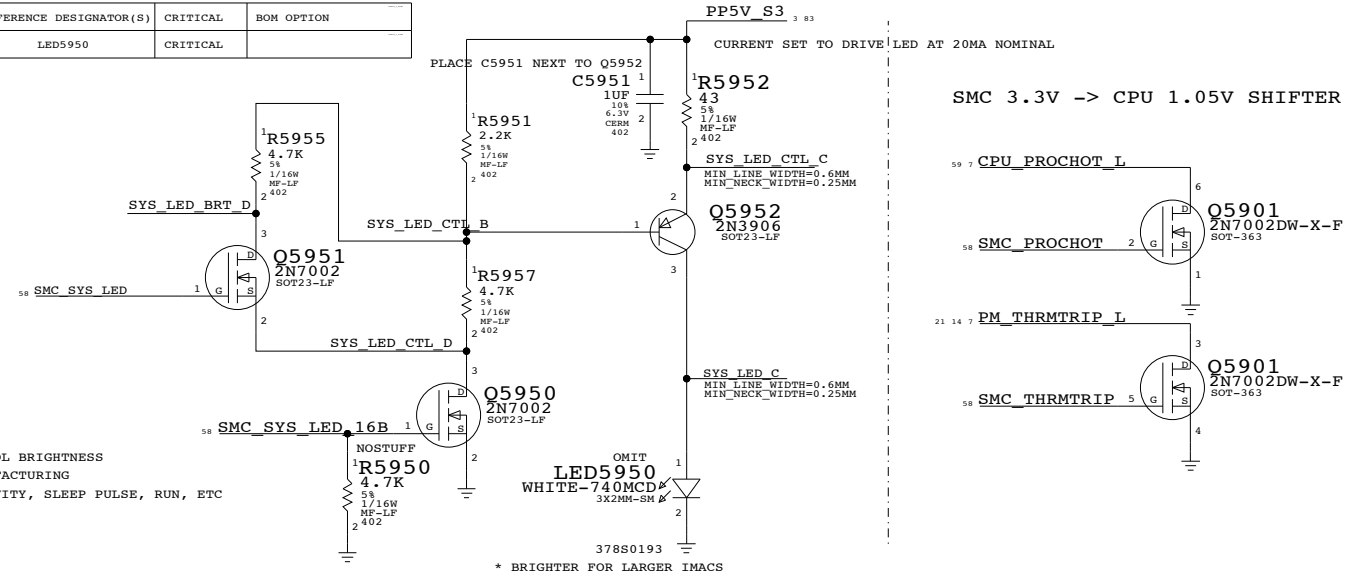
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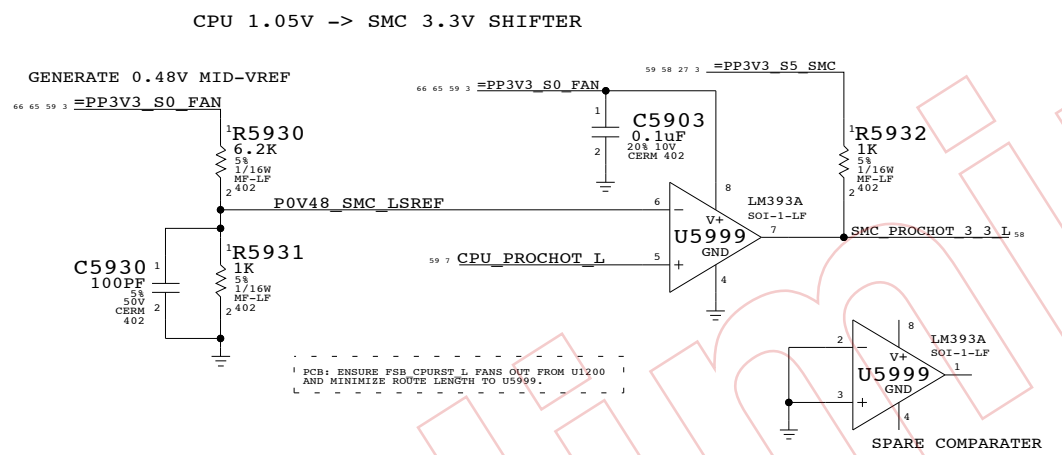
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
37880193	1	LED, WHITE, 740MCD, LF, 3X2MM	LED5950	CRITICAL	

D



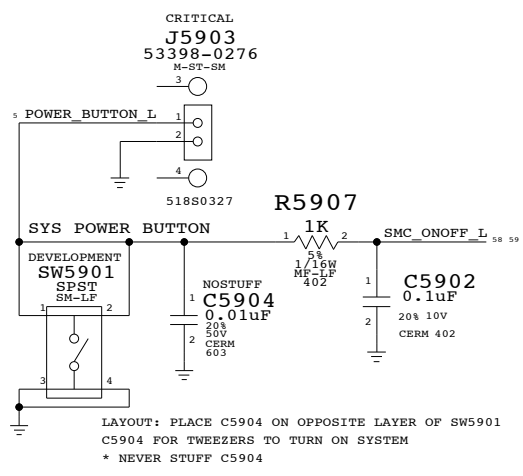
WHITE SYSLED
SMC_SYS_LED - PWM, S/W VARIED TO CONTROL BRIGHTNESS ACROSS LARGE VOLUME MANUFACTURING
SMC_SYS_LED_16B - PWM, NORMAL LED ACTIVITY, SLEEP PULSE, RUN, ETC

C



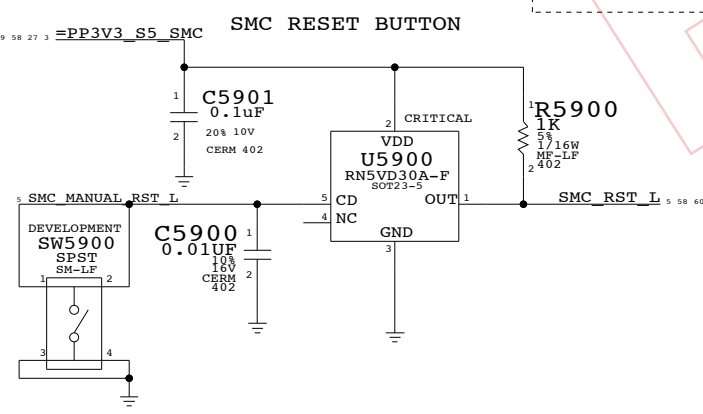
PCB: ENSURE FSB CPURST L FANS OUT FROM U1200 AND MINIMIZE ROUTE LENGTH TO U5999.

POWER BUTTON HEADER

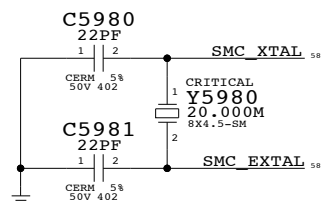


LAYOUT: PLACE C5904 ON OPPOSITE LAYER OF SW5901 C5904 FOR TWEEZERS TO TURN ON SYSTEM
* NEVER STUFF C5904

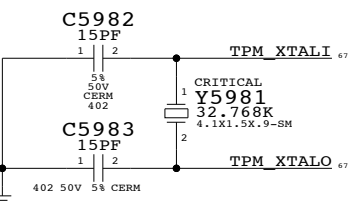
A



SMC CRYSTAL



TPM CRYSTAL



LAYOUT NOTE: PLACE CAPACITORS BETWEEN CRYSTAL AND SMC/TPM

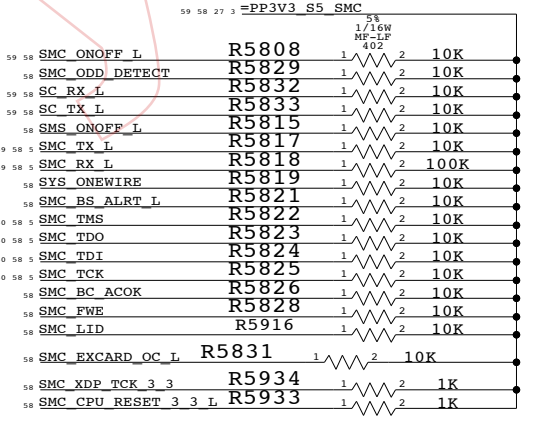
SMC ALIASES, PULLUPS, AND TESTPOINTS

NO-CONNECT UNUSED PINS		DEBUG TESTPOINTS ON SELECTED INPUTS/OUTPUTS	
SMC_P20	NC SMC_P20	SMC_SYS_KBDLED	TP_SMC_SYS_KBDLED
SMC_P21	NC SMC_P21	SMC_FF0	TP_SMC_FF0
SMC_P22	NC SMC_P22	SMC_PM_G2_EN	TP_SMC_PM_G2_EN
SMC_P23	NC SMC_P23	SMC_ADAPTER_EN	TP_SMC_ADAPTER_EN
SMC_P26	NC SMC_P26	ALS_LEFT	TP_ALS_LEFT
SMC_P27	NC SMC_P27	ALS_RIGHT	TP_ALS_RIGHT
SMC_BATT_ISET	NC SMC_BATT_ISET	SMC_FF1	TP_SMC_FF1
SMC_BATT_VSET	NC SMC_BATT_VSET	SMC_XDP_TCK	TP_SMC_XDP_TCK
SMC_SYS_ISET	NC SMC_SYS_ISET	SMC_XDP_TRST_L	TP_SMC_XDP_TRST_L
SMC_SYS_VSET	NC SMC_SYS_VSET	SMC_PB7	TP_SMC_PB7
SMC_BATT_TRICKLE_EN_L	NC SMC_BATT_TRICKLE_EN_L		
SMC_BATT_CHG_EN	NC SMC_BATT_CHG_EN		
ALS_GAIN	NC ALS_GAIN		

NC OR PULLDOWN UNUSED ANALOG SENSE PINS

SMS_X_AXIS	NC SMS_X_AXIS
SMS_Y_AXIS	NC SMS_Y_AXIS
SMS_Z_AXIS	NC SMS_Z_AXIS
SMC_NB_ISENSE	NC SMC_NB_ISENSE
SMC_MEM_ISENSE	NC SMC_MEM_ISENSE

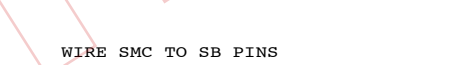
SMC PULL-UPS & PULL-DOWNS



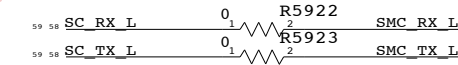
TPM RESET PULLUP



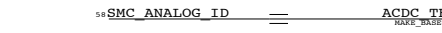
WIRE-OR DIMM OVERTEMP TO SMC



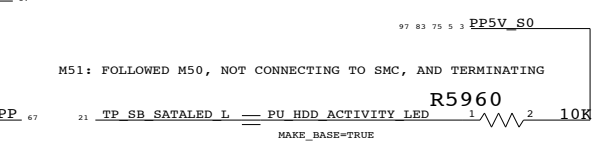
WIRE SMC TO SB PINS



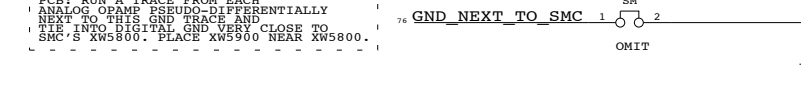
POWER SUPPLY TEMP SENSE



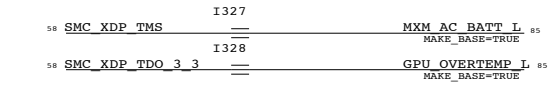
HDD ACTIVITY MONITOR



TIE ANALOG SENSOR OPAMP GROUNDS TO SMC GROUND



M51 SPECIFIC: GPU MONITORING SIGNALS

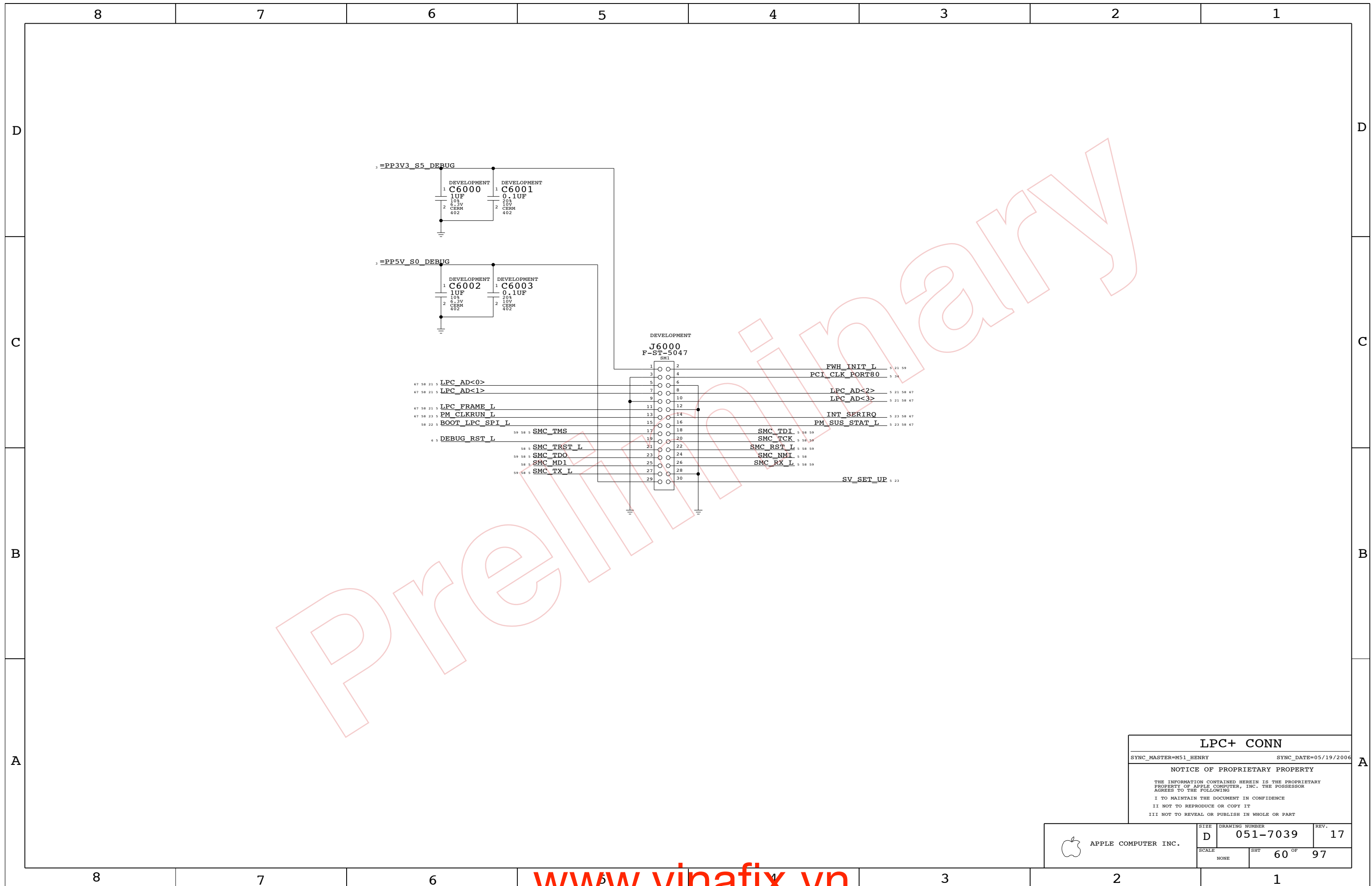


SMC & TPM SUPPORT

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Pre-release

LPC+ CONN

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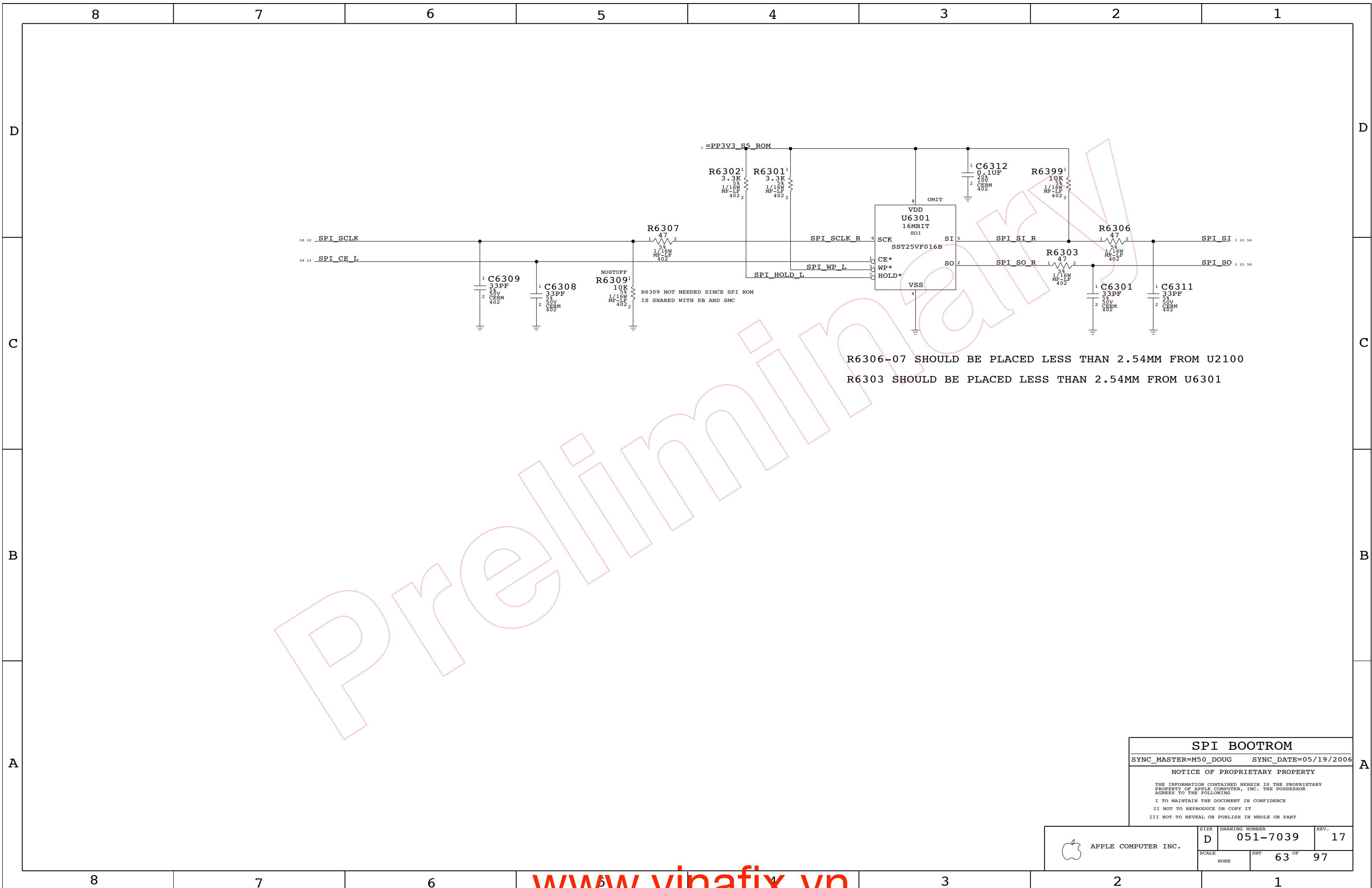
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	SCALE NONE	SHT 60 OF	97



R6306-07 SHOULD BE PLACED LESS THAN 2.54MM FROM U2100
 R6303 SHOULD BE PLACED LESS THAN 2.54MM FROM U6301

SPI BOOTROM

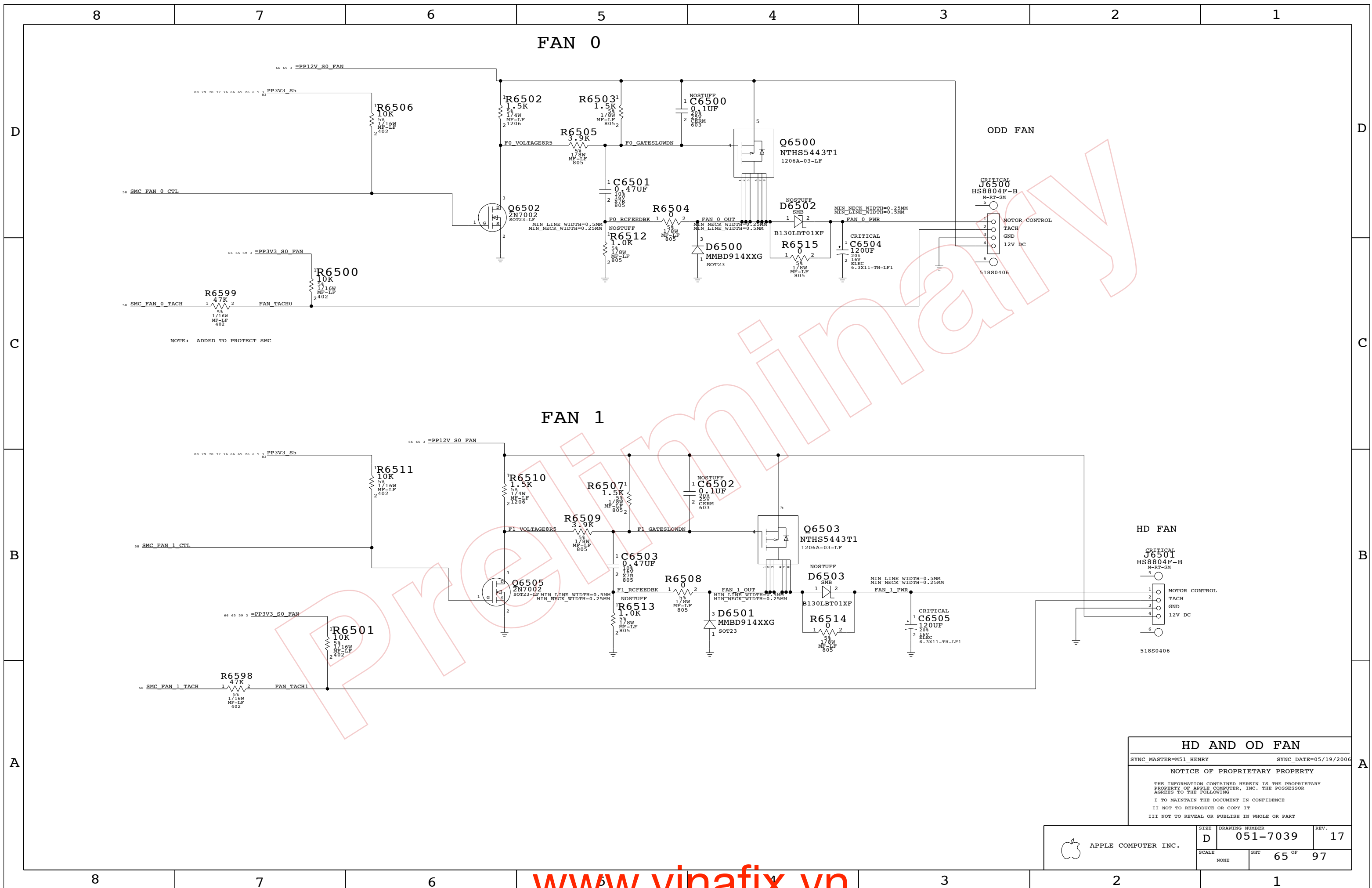
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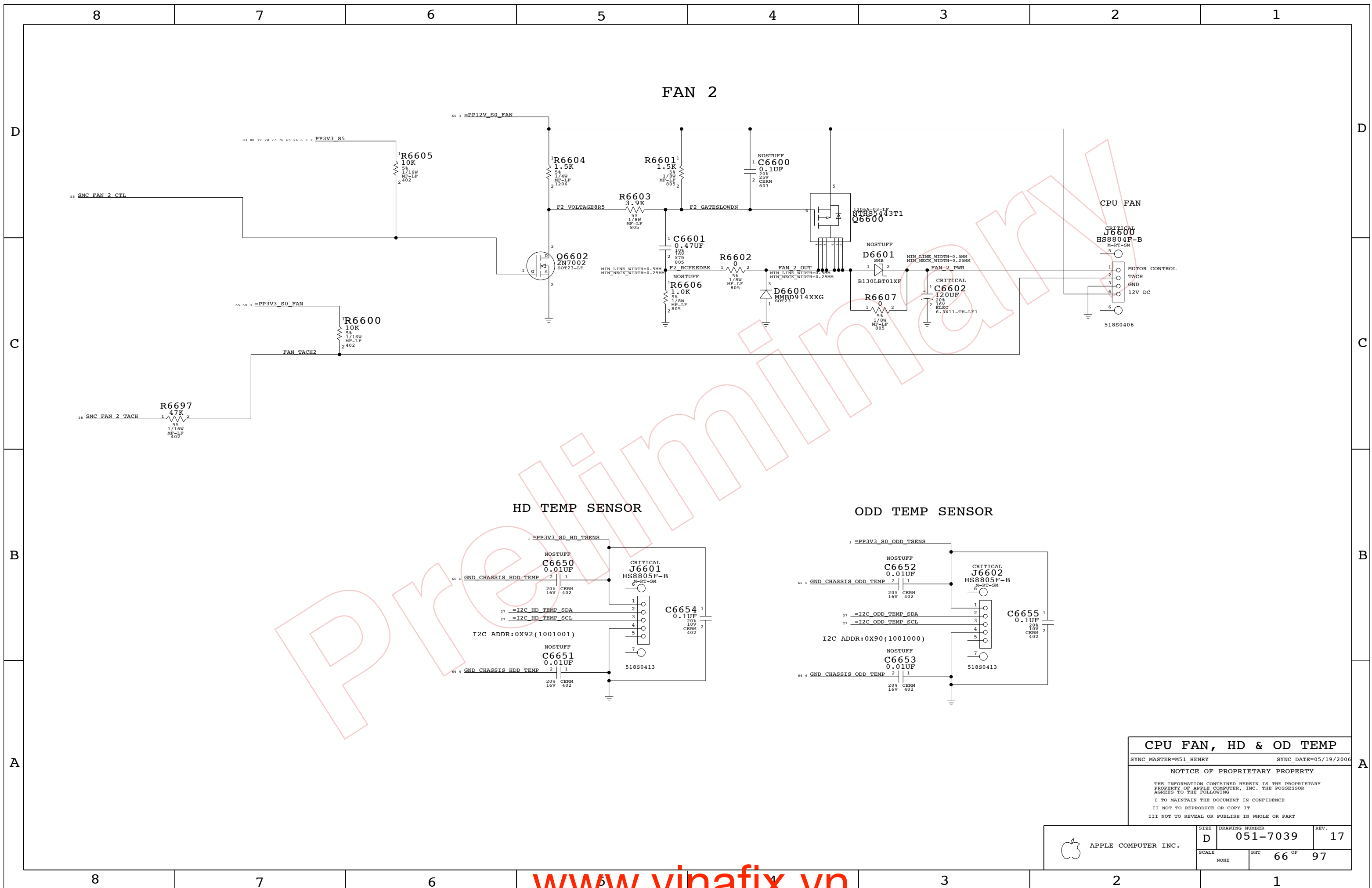
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NONE	63 OF		97



NOTE: ADDED TO PROTECT SMC

HD AND OD FAN
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NONE			



FAN 2

HD TEMP SENSOR

ODD TEMP SENSOR

CPU FAN, HD & OD TEMP

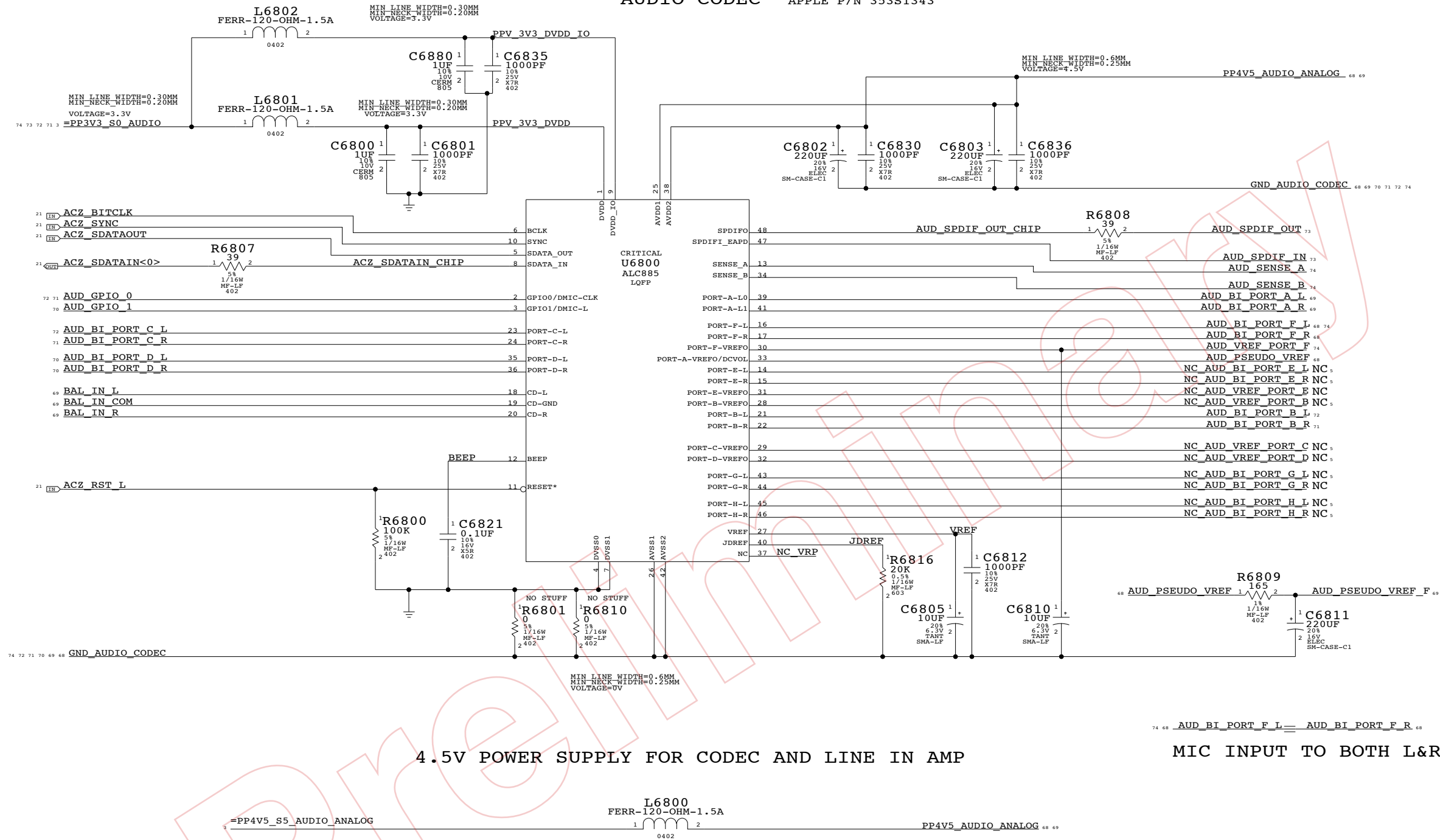
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NONE			

AUDIO CODEC APPLE P/N 353S1343



4.5V POWER SUPPLY FOR CODEC AND LINE IN AMP

MIC INPUT TO BOTH L&R

AUDIO: CODEC
 SYNC_MASTER=AUDIO SYNC_DATE=05/19/2006
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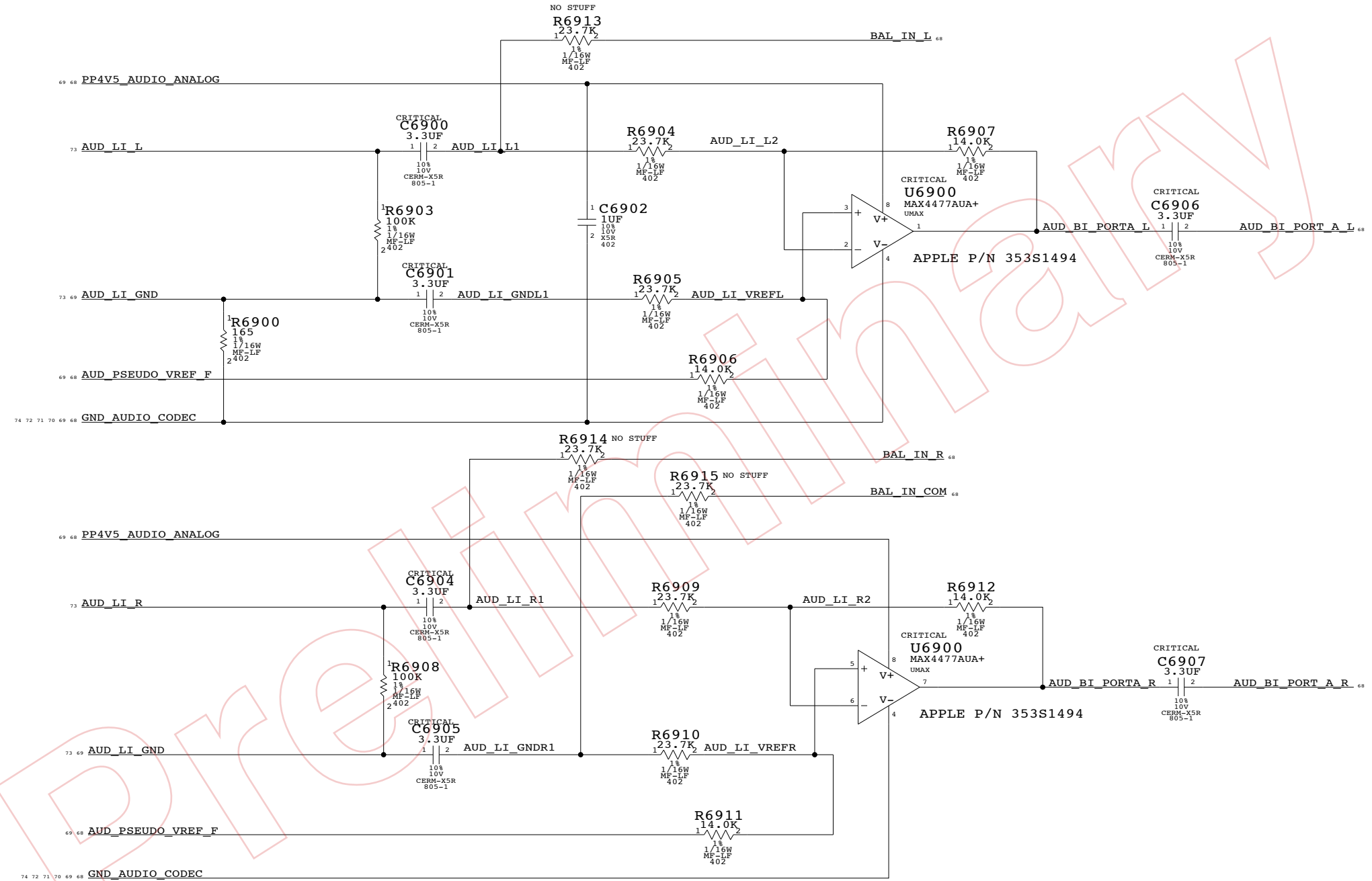
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LINE IN PSEUDO-DIFFERENTIAL AMP
AV= 0.59



AUDIO: LINE INPUT AMP

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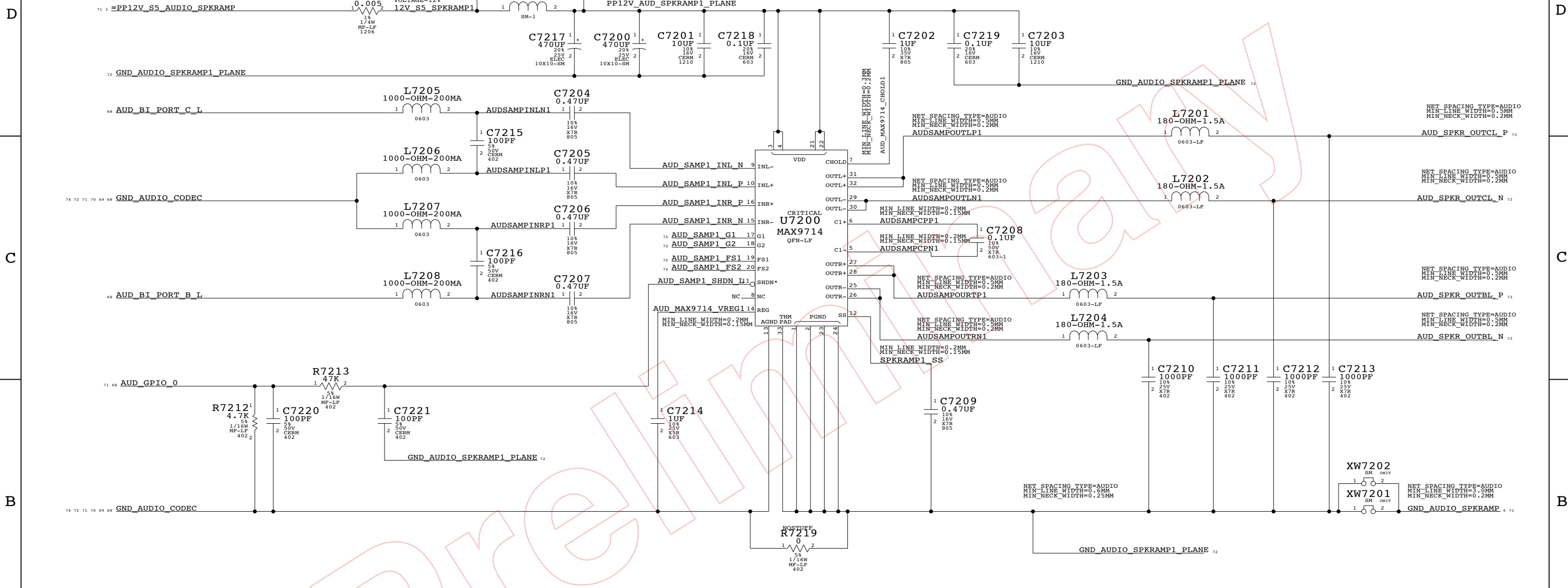
2

1

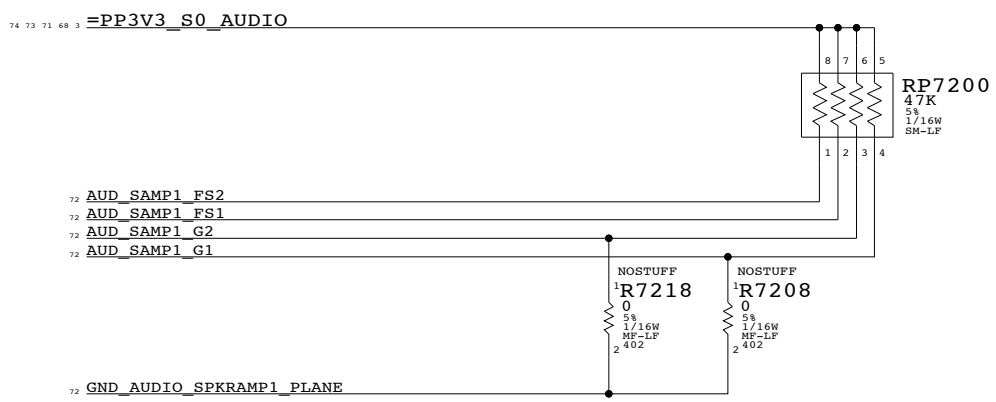
NET SPACING TYPE=AUDIO
 MIN_LINE_WIDTH=3.0MM
 MIN_NECK_WIDTH=0.2MM
 VOLTAGE=12V

NET SPACING TYPE=AUDIO
 MIN_LINE_WIDTH=0.6MM
 MIN_NECK_WIDTH=0.25MM
 VOLTAGE=12V

SPEAKER AMP
 APPLE P/N 353S1156

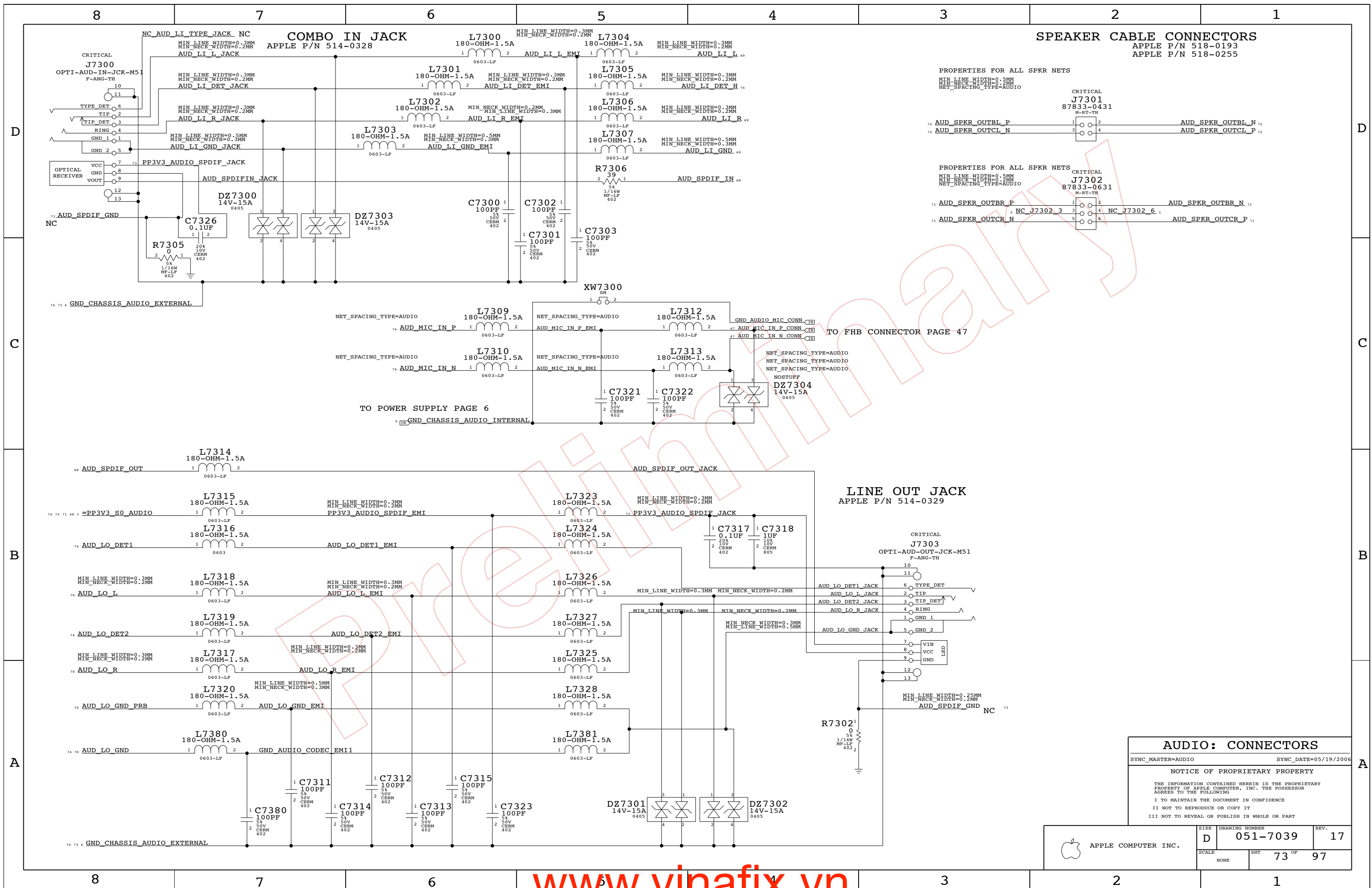


GAIN SETTINGS: +16DB
 MODULATION SETTING: LOW EMI
 GAIN AND SWITCHING FREQUENCY STUFF OPTIONS



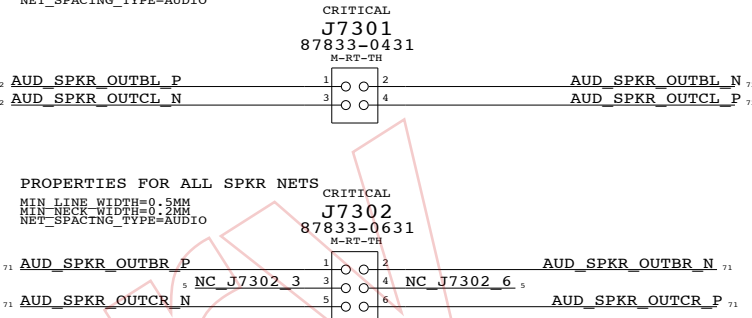
AUDIO: SPEAKER AMP
 SYNC_MASTER=AUDIO SYNC_DATE=05/19/2006
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SCALE	SHT	72 OF	97
NONE			

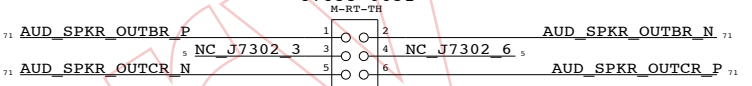


SPEAKER CABLE CONNECTORS
 APPLE P/N 518-0193
 APPLE P/N 518-0255

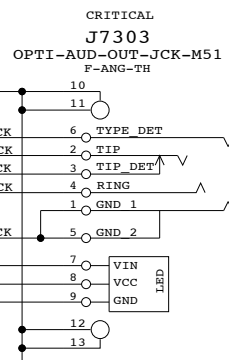
PROPERTIES FOR ALL SPKR NETS
 MIN_LINE_WIDTH=0.5MM
 MIN_NECK_WIDTH=0.2MM
 NET_SPACING_TYPE=AUDIO



PROPERTIES FOR ALL SPKR NETS
 MIN_LINE_WIDTH=0.5MM
 MIN_NECK_WIDTH=0.2MM
 NET_SPACING_TYPE=AUDIO



LINE OUT JACK
 APPLE P/N 514-0329



AUDIO: CONNECTORS

SYNC_MASTER=AUDIO SYNC_DATE=05/19/2006

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7039	17
SCALE	SHT	73 OF	97
NONE			

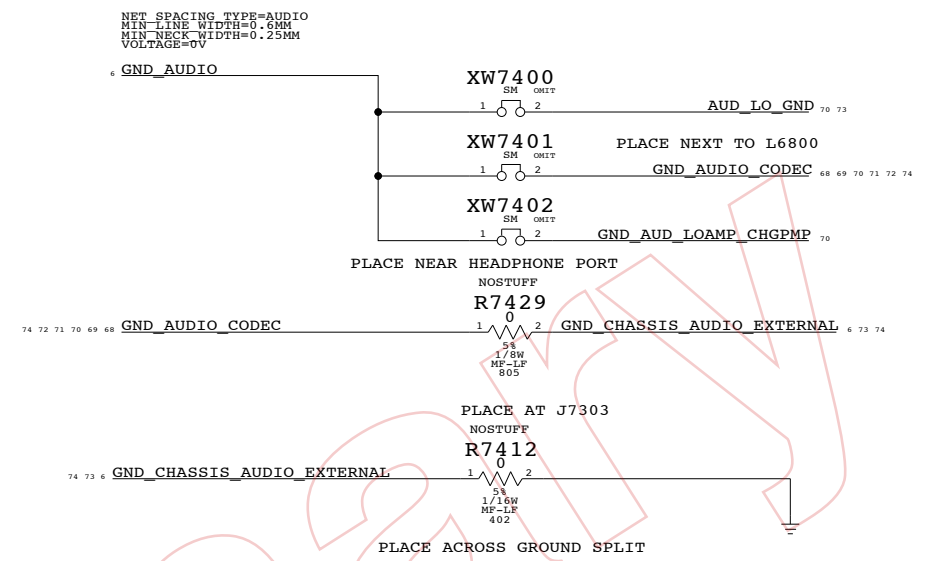
CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	DAC	PIN COMPLEX	MUTE CONTROL
LINE OUT	0X0C	0X02	0X14 (D)	GPIO 1
SPKR AMP	0X0D	0X03	0X18 (B)	GPIO 0
SPKR AMP1	0X0F	0X05	0X1A (C)	GPIO 0
SPDIFOUT		CONVERTER=0X06	PIN=0X1E	
		DETECT DELEGATE PIN	0X16H	

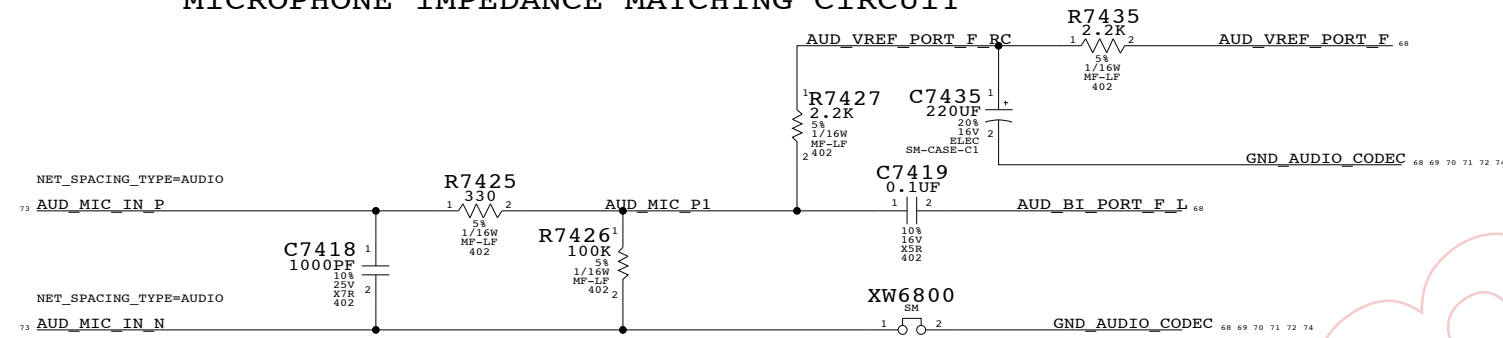
CODEC INPUT SIGNAL PATHS

FUNCTION	ADC	MIXER	PORT	VREF
MIC INPUT	0X07	0X24	0X19 (F)	80%
LINE INPUT	0X08	0X23	0X15 (A)	50%
SPDIFIN	CONVERTER=0X0A		PIN=0X1F	

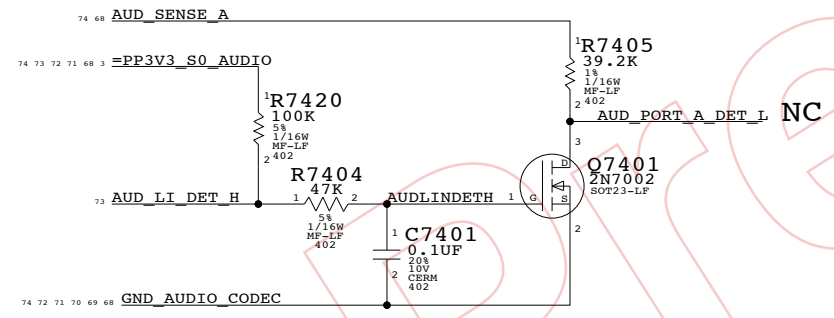
AUDIO GROUND RETURNS



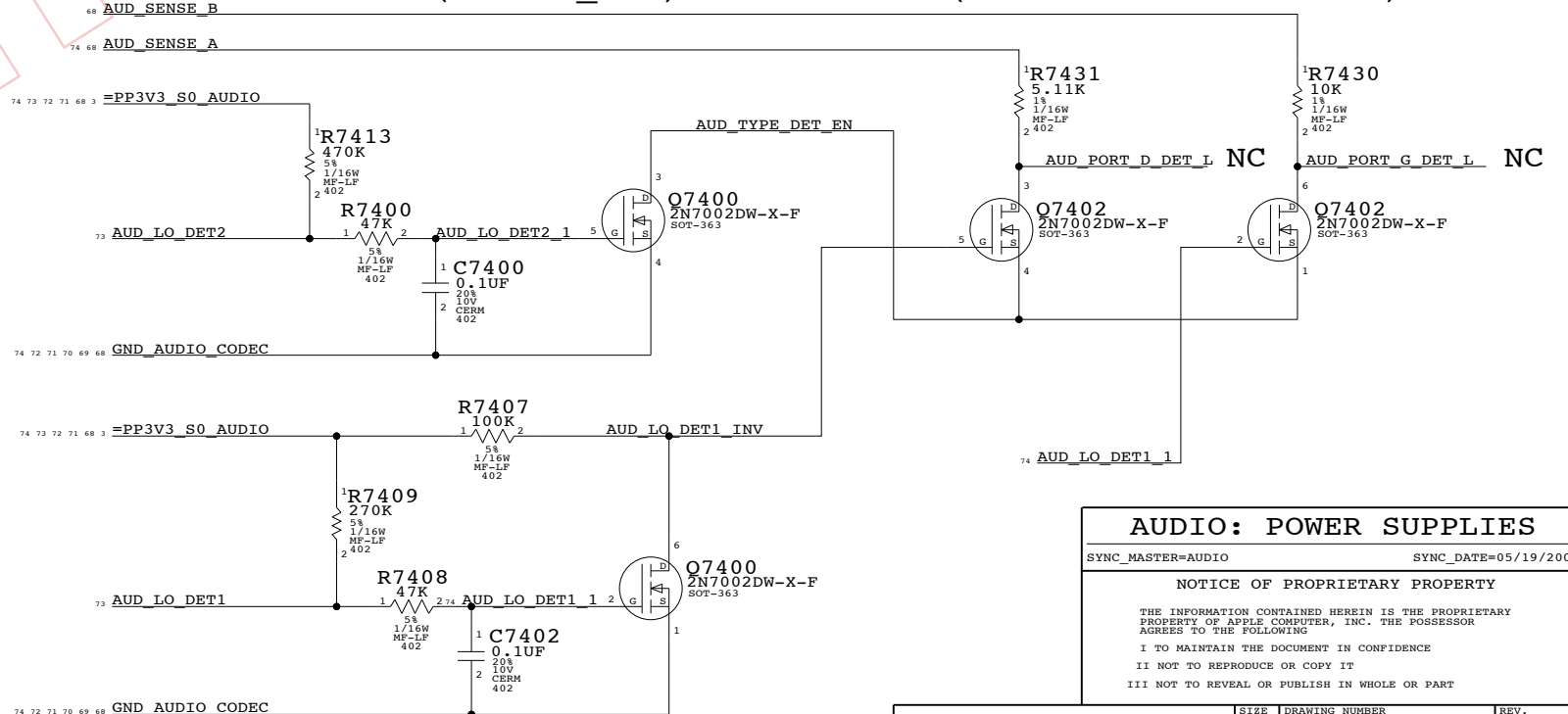
MICROPHONE IMPEDANCE MATCHING CIRCUIT



PORT A (LI) PLUG DETECT



PORT D/G (LO/DIG_OUT) PLUG DETECT (G TELLS H TO COME ON)



AUDIO: POWER SUPPLIES

SYNC_MASTER=AUDIO SYNC_DATE=05/19/2006

NOTICE OF PROPRIETARY PROPERTY

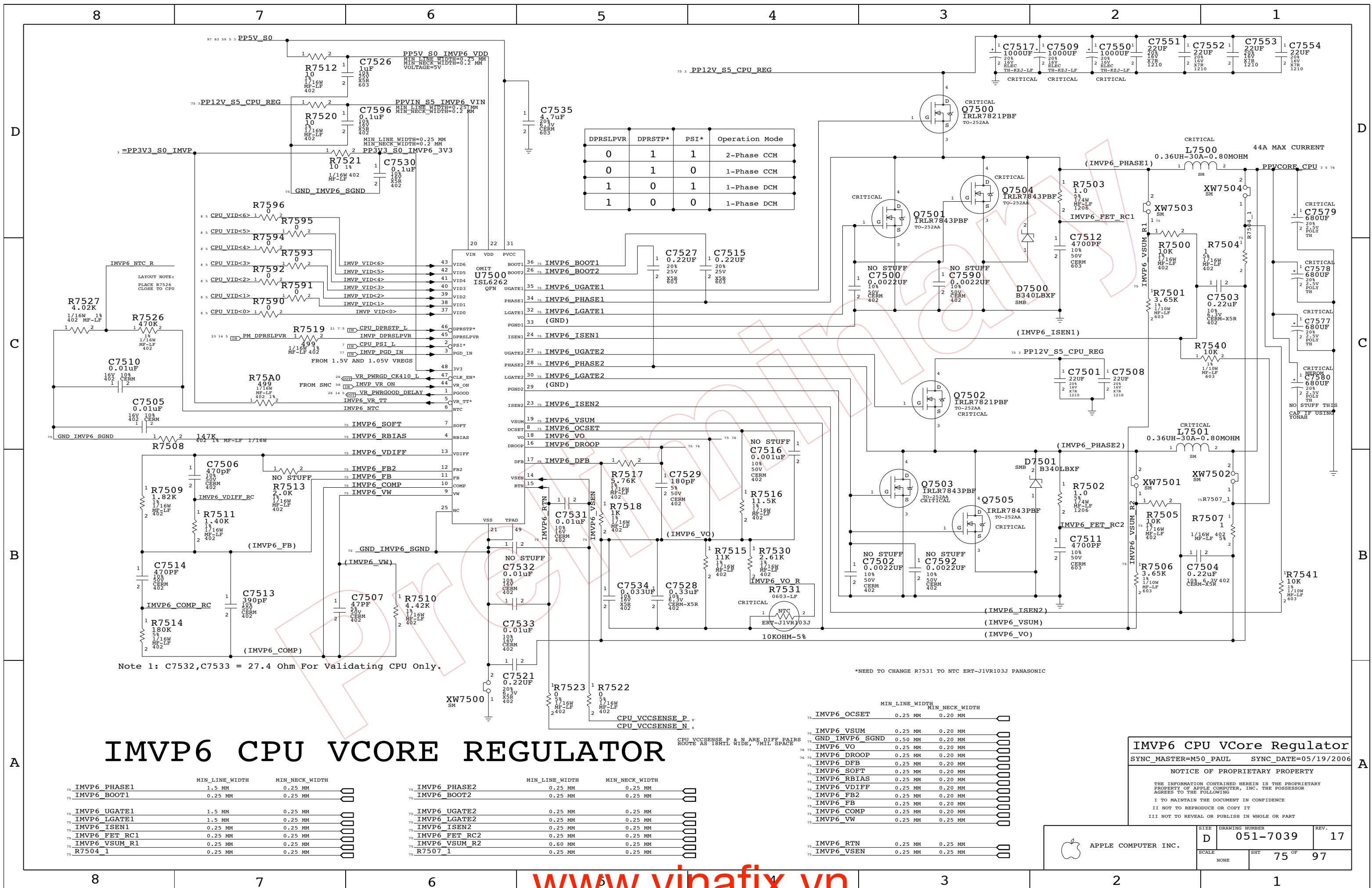
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	D	051-7039	17
SCALE	SHT	74 OF 97	
NONE			



DPRSLPVR	DPRSTP*	PSI*	Operation Mode
0	1	1	2-Phase CCM
0	1	0	1-Phase CCM
1	0	1	1-Phase DCM
1	0	0	1-Phase DCM

Note 1: C7532,C7533 = 27.4 Ohm For Validating CPU Only.

*NEED TO CHANGE R7531 TO NTC ERT-J1VR103J PANASONIC

IMVP6 CPU VCore Regulator

CPU_VCCSENSE_P & N ARE DIFF PAIRS ROUTE AS 18MIL WIDE, 7MIL SPACE

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
75 IMVP6 PHASE1	1.5 MM	0.25 MM
75 IMVP6 BOOT1	0.25 MM	0.25 MM
75 IMVP6 UGATE1	1.5 MM	0.25 MM
75 IMVP6 LGATE1	1.5 MM	0.25 MM
75 IMVP6 ISEN1	0.25 MM	0.25 MM
75 IMVP6 FET RC1	0.25 MM	0.25 MM
75 IMVP6 VSUM R1	0.25 MM	0.25 MM
75 R7504_1	0.25 MM	0.25 MM

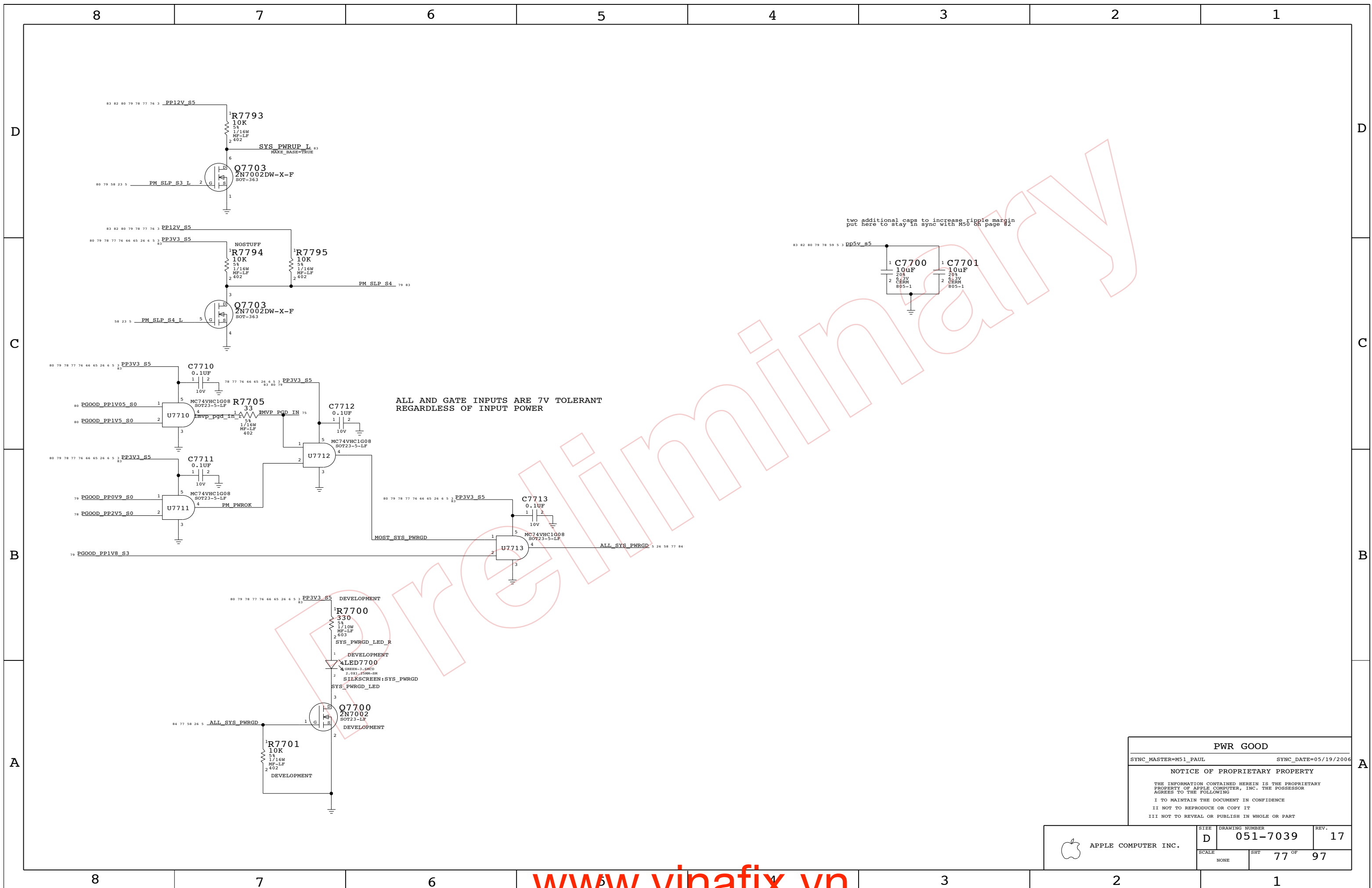
	MIN_LINE_WIDTH	MIN_NECK_WIDTH
75 IMVP6 PHASE2	0.25 MM	0.25 MM
75 IMVP6 BOOT2	0.25 MM	0.25 MM
75 IMVP6 UGATE2	0.25 MM	0.25 MM
75 IMVP6 LGATE2	0.25 MM	0.25 MM
75 IMVP6 ISEN2	0.25 MM	0.25 MM
75 IMVP6 FET RC2	0.25 MM	0.25 MM
75 IMVP6 VSUM R2	0.60 MM	0.25 MM
75 R7507_1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
75 IMVP6_OCSET	0.25 MM	0.20 MM
75 IMVP6_VSUM	0.25 MM	0.20 MM
75 GND_IMVP6_SGND	0.50 MM	0.20 MM
75 IMVP6_VO	0.25 MM	0.20 MM
75 IMVP6_DROOP	0.25 MM	0.20 MM
75 IMVP6_DFB	0.25 MM	0.20 MM
75 IMVP6_SOFT	0.25 MM	0.20 MM
75 IMVP6_RBIAS	0.25 MM	0.20 MM
75 IMVP6_VDIFF	0.25 MM	0.20 MM
75 IMVP6_FB2	0.25 MM	0.20 MM
75 IMVP6_FB	0.25 MM	0.20 MM
75 IMVP6_COMP	0.25 MM	0.20 MM
75 IMVP6_VW	0.25 MM	0.25 MM
75 IMVP6_RTN	0.25 MM	0.25 MM
75 IMVP6_VSEN	0.25 MM	0.25 MM

IMVP6 CPU VCore Regulator
 SYNC_MASTER=M50_PAUL SYNC_DATE=05/19/2006

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7039	17
SCALE	SHT	75 OF	97
NONE			



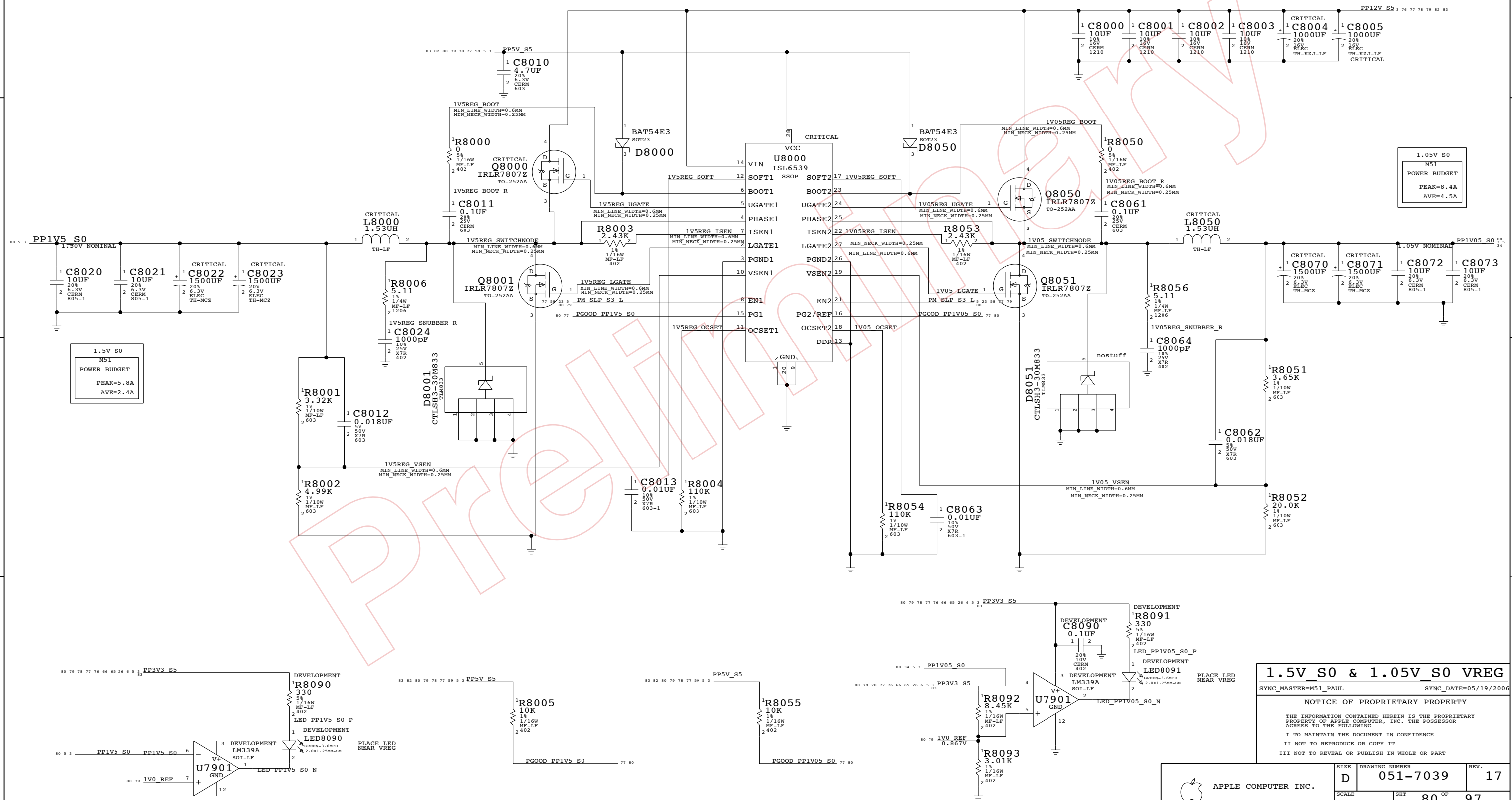
ALL AND GATE INPUTS ARE 7V TOLERANT
REGARDLESS OF INPUT POWER

two additional caps to increase ripple margin
put here to stay in sync with M50 on page 82

PWR GOOD	
SYNC_MASTER=M51_PAUL	SYNC_DATE=05/19/2006
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 APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7039	REV. 17
	SCALE NONE	SHT 77 OF 97	

1.5V S0 AND 1.05V S0 RAILS



1.5V_S0 & 1.05V_S0 VREG

SYNC_MASTER=M51_PAUL SYNC_DATE=05/19/2006

NOTICE OF PROPRIETARY PROPERTY

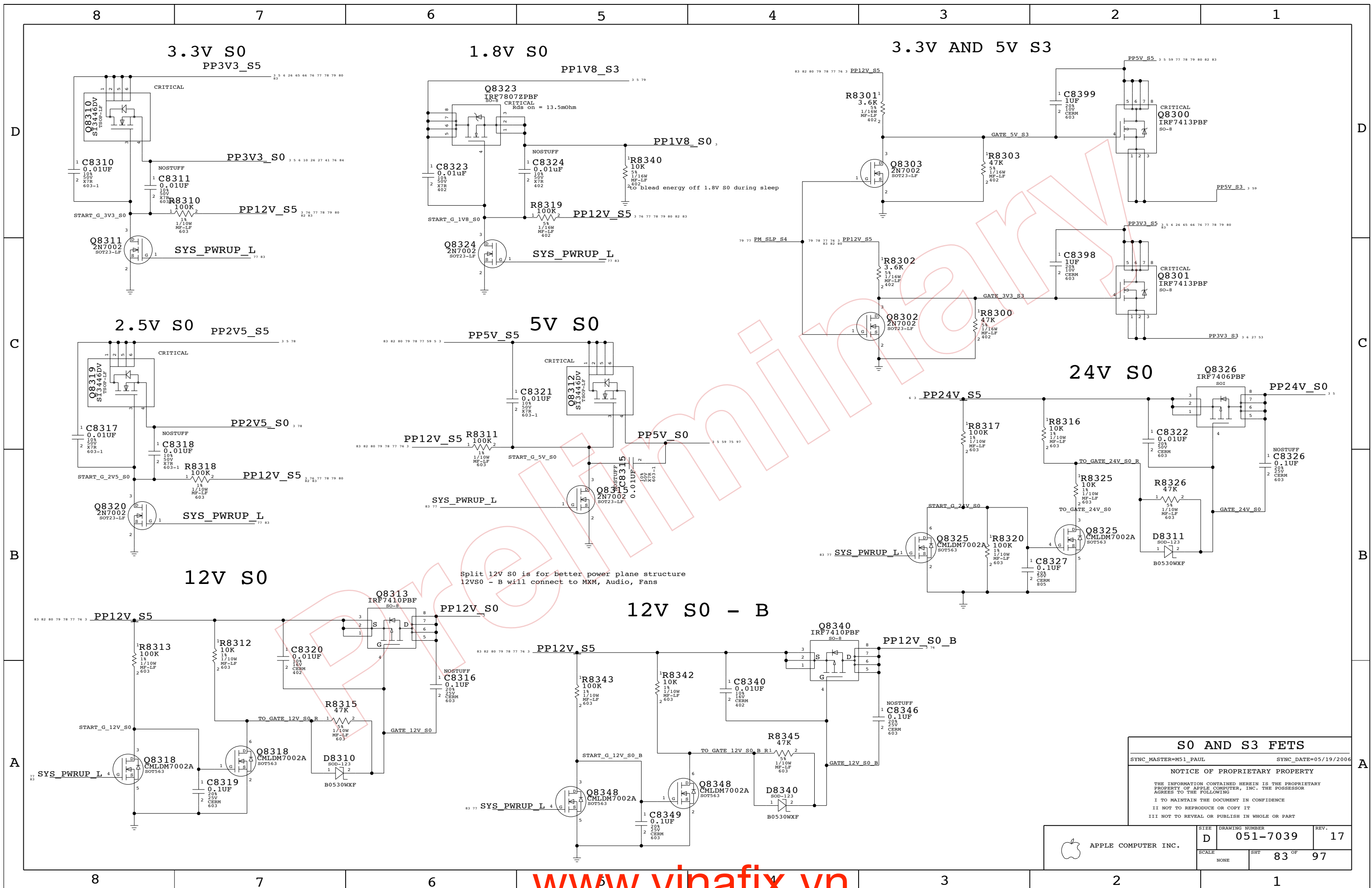
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7039	17
SCALE	SHT	80 OF	97
NONE			



S0 AND S3 FETS

SYNC_MASTER=M51_PAUL SYNC_DATE=05/19/2006

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7039	17
SCALE	SHT	83 OF	97
NONE			

Page Notes

Power aliases required by this page:

- =PP12V_S0_MXM
- =PP5V_S0_MXM
- =PP1V8_S0_MXM

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Note: PCI-E Lanes are reversed to untangle routes
Need to stuff config strap using BOM option NBCFG_PEG_REVERSE
Polarity is also inverted (Tx+ goes to Rx-) to untangle routes

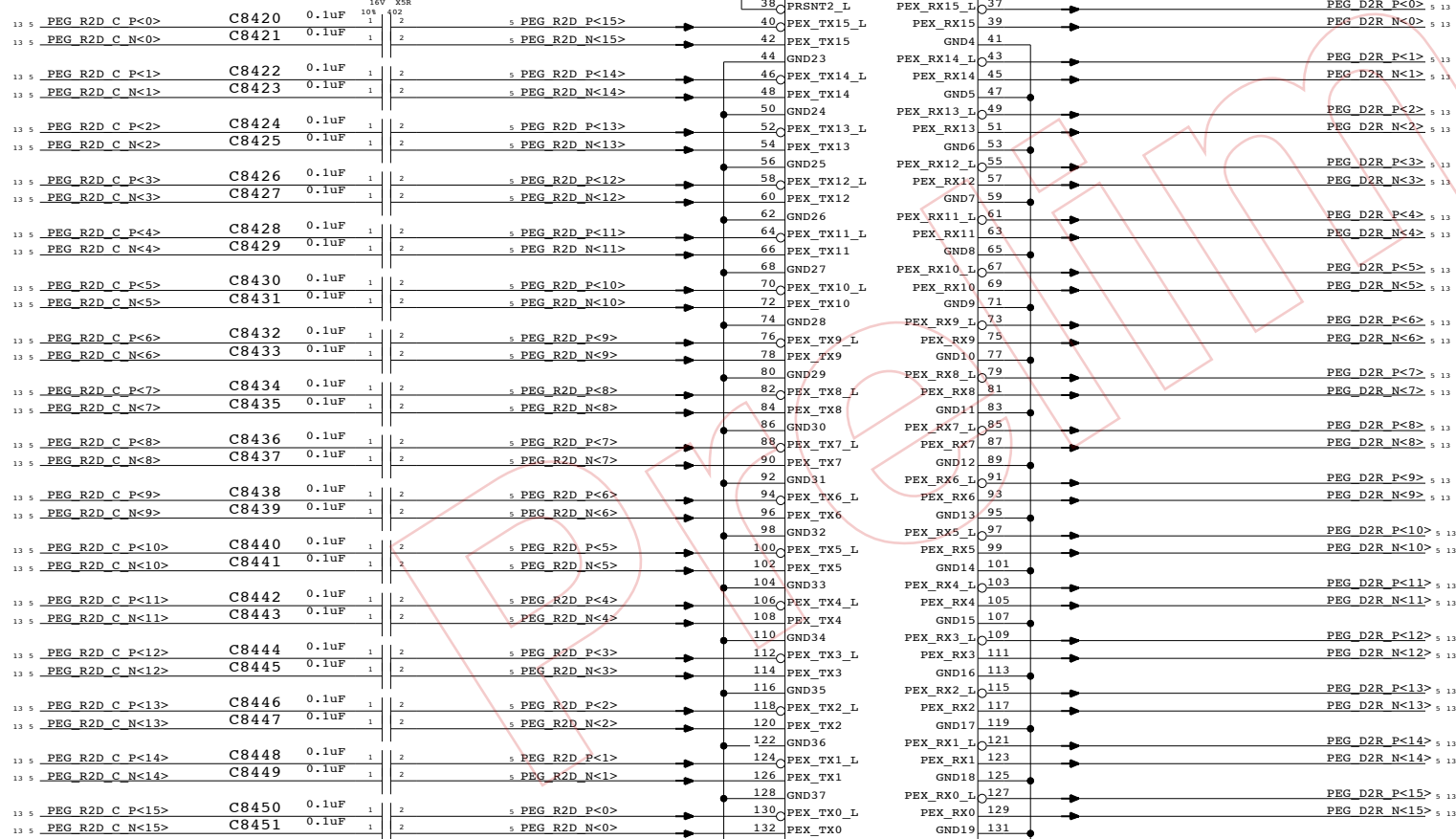
MXM SPEC POWER REQUIREMENTS

(NOT NECESSARILY THE SAME FOR EVERY MODULE)

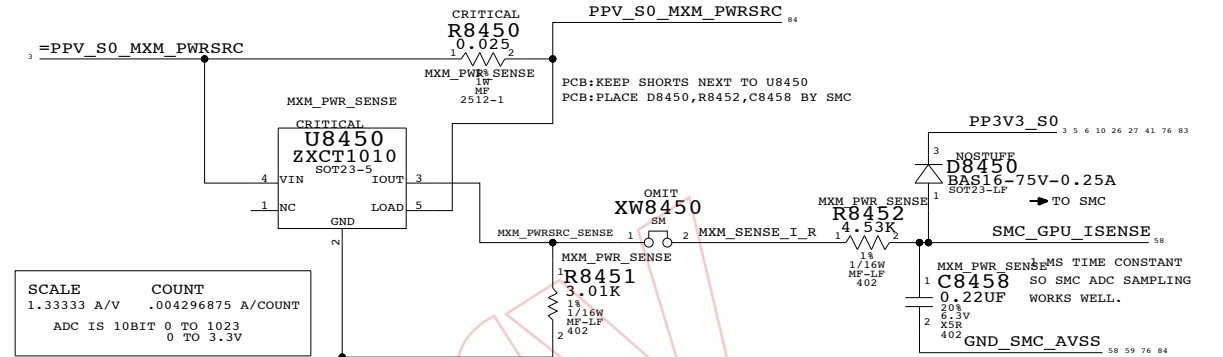
VOLTAGE	CURRENT	POWER
3V3	1.5 A	4.95 W
5V	0.5 A	2.5 W
2V5	0.5 A	1.25 W
1V8	3.5 A	6.3 W
PWR (12V)	UP TO 4 A	PLATFORM DEPENDENT

M51: FIX ON CARD ALLOWS US TO NOT STUFF MOST OF THE 1.8V DECOUPLING, WITH NO DROOP OR NOISE

PLACE CAPS NEAR NB

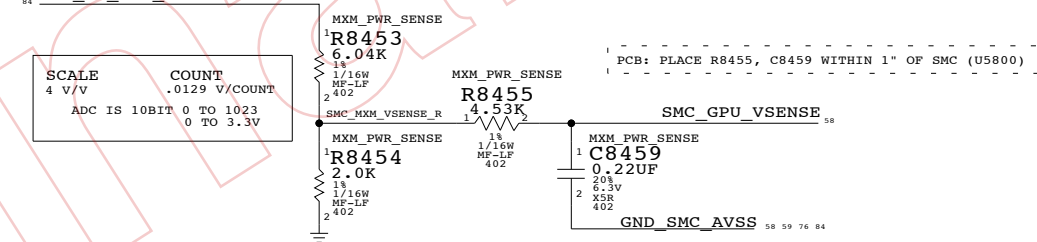


MXM PWRSRC (GPU CORE) CURRENT SENSE



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
10780070	1	RES, 0-OHM, 2512	R8450	PRODUCTION

MXM PWRSRC VOLTAGE SENSE (SCALING 12V INPUT VOLTAGE TO SMC)



MXM PCI-E & PWR

SYNC_MASTER=M51_DAVE SYNC_DATE=(MASTER)

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7039	17
SCALE	SHT	84 OF	97
NONE			

Page Notes

Power aliases required by this page:
 - =PP3V3_S0_MXM
 - =PP2V5_S0_MXM

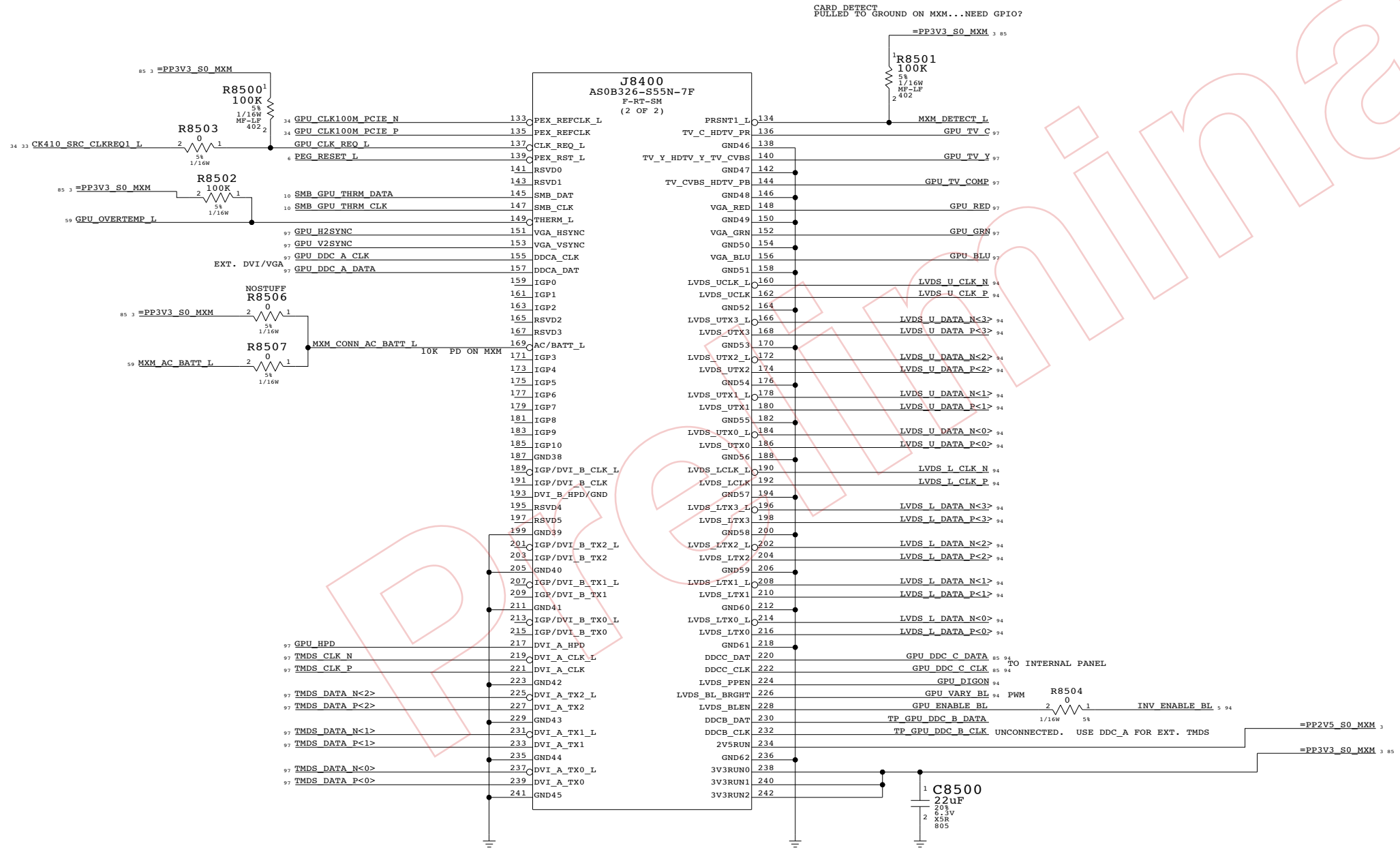
Signal aliases required by this page:
 - =SMB_GPU_THRM_DATA
 - =SMB_GPU_THRM_CLK

BOM options provided by this page:
 (NONE)

MXM SPEC POWER REQUIREMENTS

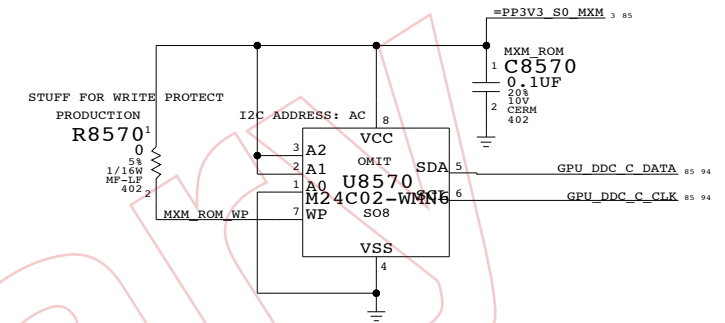
(NOT NECESSARILY THE SAME FOR EVERY MODULE)

VOLTAGE	CURRENT	POWER
3V3	1.5 A	4.95 W
5V	0.5 A	2.5 W
2V5	0.5 A	1.25 W
1V8	3.5 A	6.3 W
PWR (12V)	UP TO 4 A	PLATFORM DEPENDENT



MXM SYSTEM INFORMATION ROM

PLACE CLOSE TO J8400



MXM I/O	
SYNC_MASTER=M51_DAVE	SYNC_DATE=(MASTER)
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7039	17
SCALE	SHT	85 OF	97
NONE			

Page Notes

Power aliases required by this page:
 - =PP12V_LCD
 - =PP24V_INVERTER
 - =PP3V3_S0_VIDEO

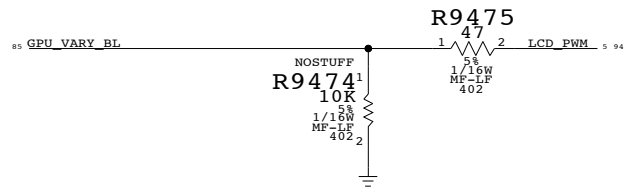
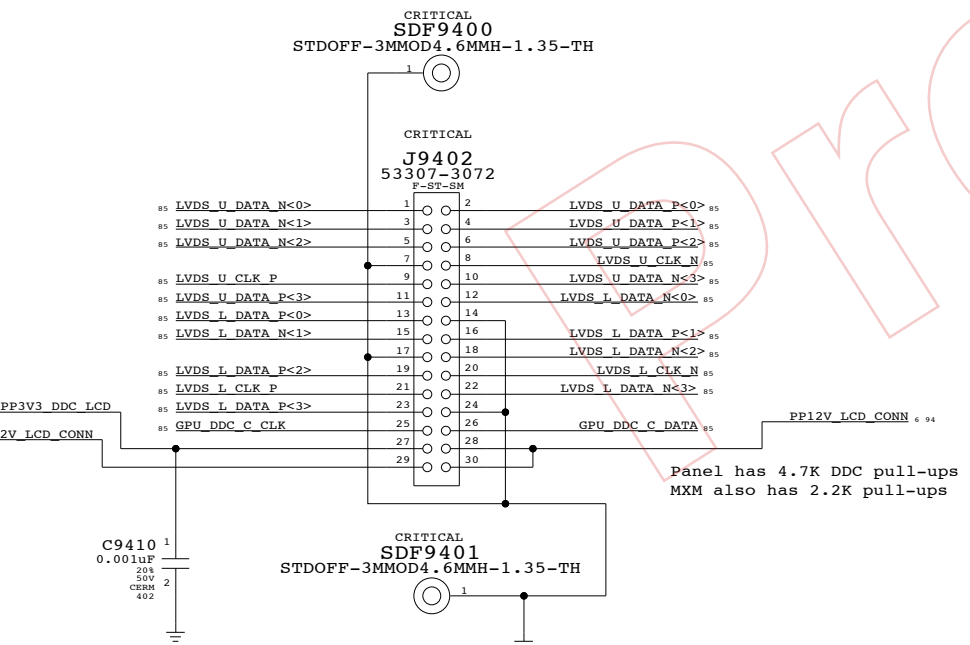
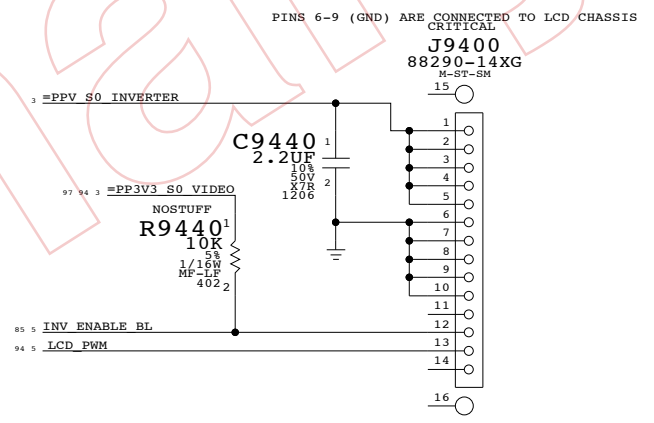
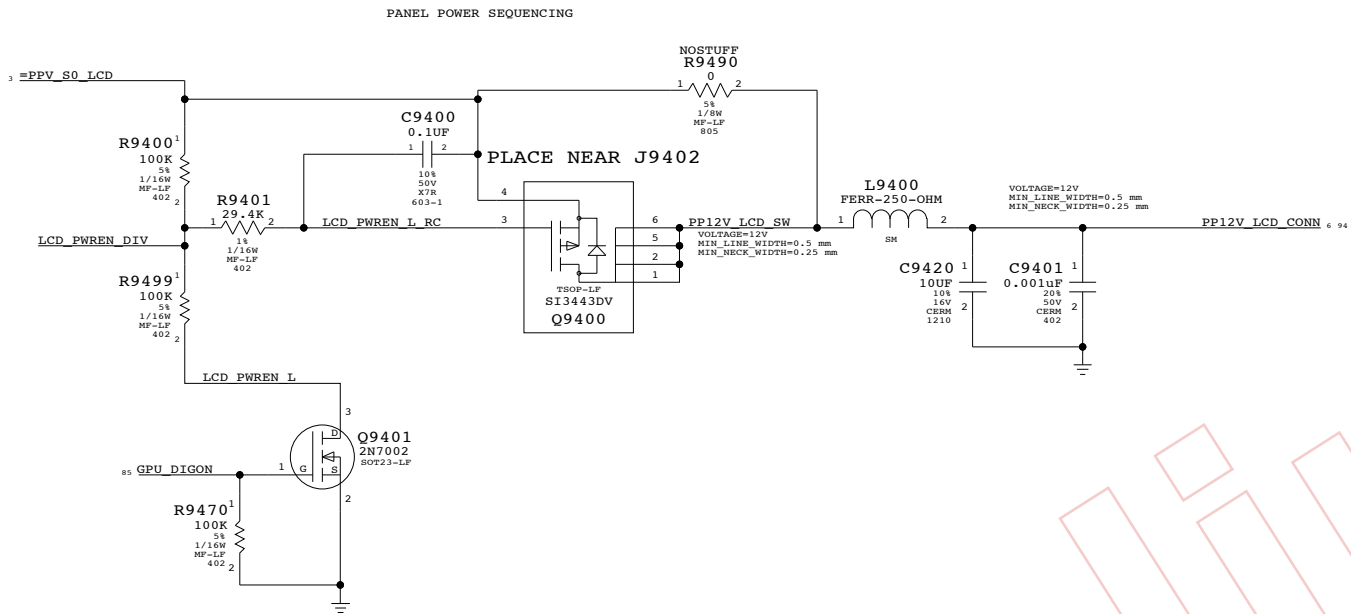
Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

97 94 3 =PP3V3_S0_VIDEO =PP3V3_DDC_LCD 94

LCD (LVDS) INTERFACE

INVERTER INTERFACE



Internal Display Conns

SYNC_MASTER=M51_DAVE SYNC_DATE=(MASTER)

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	D	051-7039	17
SCALE	SHT		94 OF 97
NONE			

