### Capacitance Values

- All capacitance values are in microfarads.

### Resistance Values

- All resistance values are in ohms, 0.1 watt ± 5%.

### Table of Contents

<table>
<thead>
<tr>
<th>PART#</th>
<th>PCBF, BOZEMAN, Q41C</th>
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### Reference Designators

- SCH1

### Date

- 06/03/2005

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- 3
- 2
- 1

### Engineering Release

- 06/03/2005

### Other Information

- Apple Computer Inc.
- A00001
- SCHEM, BOZEMAN, Q41C
- 051-6839
- 02
- www.vinafix.vn
Design-Specific Rules

Layer-specific rules for 90-ohm differential impedance
Layer-specific rules for 60-ohm single-ended impedance
Layer-specific rules for 50-ohm single-ended impedance
Portable-specific override rules

BOM OPTIONS

Module Components

Board Information
Enhanced MAC-1 Test Coverage

Functional test points use a P4 pad placed on bottom side.

**Functional Test Points**

<table>
<thead>
<tr>
<th>Location</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>Place 2-3 mm of audio connector.</td>
</tr>
<tr>
<td>B</td>
<td>Place 2-3 mm of debug connector.</td>
</tr>
<tr>
<td>C</td>
<td>Place 2-3 mm of ALS connector.</td>
</tr>
<tr>
<td>D</td>
<td>Place 2-3 mm of ODD/HDD connector.</td>
</tr>
</tbody>
</table>

**Enhanced MAC-1 Test Coverage**

- Place 5-10 GND TPs.
- Place within 25 mm of power supply.
- Place within 50 mm of debug connector.
- Place within 25 mm of ODD/HDD connector.
- Place within 25 mm of ALS connector.
- Place within 25 mm of battery connector.
- Place within 25 mm of left USB connector.
- Place within 25 mm of right USB connector.
The MMM_MCU_PMU BOM option is selected. Note: Neither option is necessary when it can be monitored by in shutdown. ALL moves the MCU to the PMU I2C bus so the time or only when the system is on. Selects whether MMM MCU is powered all - MMM_PWR_ALL / MMM_PWR_PWRON. I2C bus 1 to resolve address conflict. PMU unstead. One ADT7467 connects to NB. Most devices are connected directly to. Allows bypassing Governator I2C bus. - GOV_I2C / GOV_I2C_BYPASS. BOM options provided by this page: (NONE) Signal aliases required by this page: (NONE) Power aliases required by this page: (NONE)
Nets not requiring TPs due to JTAG
ADAPTER INPUT/INRUSH LIMITER

GREATER THAN 13.1V DETECT

BATTERY INPUT/CURRENT SENSE

ADAPTER DETECTION

A29 ADAPTER DETECTION

POWER INPUTS

SYSTEM ADAPTER ANALOG AC DET
3.3V I/O DECOUPLING
(48 rails on E1)

3.3V I/O DECOUPLING
(48 rails on E1)

3.3V I/O DECOUPLING
(48 rails on E1)

3.3V I/O DECOUPLING
(48 rails on E1)

3.3V I/O DECOUPLING
(48 rails on E1)

3.3V I/O DECOUPLING
(48 rails on E1)
indicated LTC3412 output voltage.
Selects appropriate resistor for the 
-I2VCORE_xVx 
burst mode for LTC3412 regulator.
Selects between forced continuous and
-I2VCORE_CONT / I2VCORE_BURST 
BOM options provided by this page:
-I2VCORE_PGOOD
Signal aliases required by this page:
-I2PLLVDD_LDO
-I2PLLVDD
-I2VCORE
-I2VCORE_ITH
-PWRON_I2PLLVDD
-PW VIN
-PV CORE
-PW ON_I2VCORE
-PW ON_I2VCORE
-PW ON_I2VCORE
Power aliases required by this page:

C2207
470pF
4.7M
CERM
MF-LF
1/16W
402
50V
10%
R2207
4.7M
1%
R2206
4.7M
1%
R2205
4.7M
1%
R2209
4.7M
1%
R2208
4.7M
1%
R2204
4.7M
1%

Vburst = 0.8V * (Rb2 / (Rb1 + Rb2))
Iburst = (Vburst - 0.2V) * (3.75A / 0.8V)
If I2VCORE_BURST is selected:
MIN_NECK_WIDTH=0.15 mm
MIN_LINE_WIDTH=0.20 mm
MIN_NECK_WIDTH=0.15 mm
MIN_LINE_WIDTH=0.20 mm
MIN_NECK_WIDTH=0.15 mm
MIN_LINE_WIDTH=0.20 mm
MIN_LINE_WIDTH=0.20 mm
SERIAL DEBUG INTERFACE

debugging aids

place the small black square near the SLEEP LED

place "POWER BTN" in silk near resistor

place "PMU RESET" in silk near resistor

place "SYS RESET" in silk near resistor

PMU_RESET CIRCUIT

SERIAL_DEBUG_INTERFACE

DCDC

SLEEP LED

CHARGE LED

LEDS/Reset/Debug

APPLE COMPUTER INC.
**Power Management Unit**

**Additional PMU05 "Modules"**

<table>
<thead>
<tr>
<th>Module</th>
<th>ALS</th>
<th>SPI Dual Battery Charger</th>
<th>Battery Current Mon</th>
</tr>
</thead>
<tbody>
<tr>
<td>MEM</td>
<td>CPU T-diodes</td>
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</table>

**Page Notes**

- PMU Pull-ups / pull-downs

- TP_PMU_AN_P0_0
- TP_PMU_AN_P0_1
- TP_PMU_AN_P0_2
- TP_PMU_AN_P0_3
- TP_PMU_AN_P0_4
- TP_PMU_AN_P0_5
- TP_PMU_AN_P0_6
- TP_PMU_AN_P0_7

- TP_PMU_P7_0
- TP_PMU_P7_1
- TP_PMU_P7_2
- TP_PMU_P7_3
- TP_PMU_P7_4
- TP_PMU_P7_5
- TP_PMU_P7_6
- TP_PMU_P7_7

**Electrical Constraints**

-nett=PP3V3_PWRON_PMU
-nett=PP3V3_ALL_PMU
-nett=SYS_LID_OPEN
-nett=SYNOVERTEMP_L
-nett=SYS_SLEEP
-nett=SYS_WARM_RESET_L
-nett=SYS_COLD_RESET_L

**Signal Aliases Required by This Page:**

- =JTAG_BBANGER_TRST_L
- =JTAG_BBANGER_TCK
- =JTAG_BBANGER_TDI
- =JTAG_BBANGER_TMS
- =I2C_PMU_SDA
- =I2C_PMU_SCL

**BOM Options Provided by This Page:**

- 100pF capacitor to the PMU AVSS
- None of the spares can be used for spares (Analog capable)
- Signal (GND_PMU_AVSS)

**Page Notes:**

- None of the spares can be used for spares (Analog capable)
- Power Management Unit (PMU05)
- Keep crystal subcircuit close to PMU.
- Power Management Unit

**Notes:**

- The components provided by this page:

- TP_PMU_AN_P0_0
- TP_PMU_AN_P0_1
- TP_PMU_AN_P0_2
- TP_PMU_AN_P0_3
- TP_PMU_AN_P0_4
- TP_PMU_AN_P0_5
- TP_PMU_AN_P0_6
- TP_PMU_AN_P0_7

- TP_PMU_P7_0
- TP_PMU_P7_1
- TP_PMU_P7_2
- TP_PMU_P7_3
- TP_PMU_P7_4
- TP_PMU_P7_5
- TP_PMU_P7_6
- TP_PMU_P7_7

**Notes:**

- All analog inputs to PMU should have a 100pF capacitor to the PMU AVSS
- None of the spares can be used for spares (Analog capable)
- Signal (GND_PMU_AVSS)

**Notes:**

- The components provided by this page:

- TP_PMU_AN_P0_0
- TP_PMU_AN_P0_1
- TP_PMU_AN_P0_2
- TP_PMU_AN_P0_3
- TP_PMU_AN_P0_4
- TP_PMU_AN_P0_5
- TP_PMU_AN_P0_6
- TP_PMU_AN_P0_7

- TP_PMU_P7_0
- TP_PMU_P7_1
- TP_PMU_P7_2
- TP_PMU_P7_3
- TP_PMU_P7_4
- TP_PMU_P7_5
- TP_PMU_P7_6
- TP_PMU_P7_7

**Notes:**

- All analog inputs to PMU should have a 100pF capacitor to the PMU AVSS
- None of the spares can be used for spares (Analog capable)
- Signal (GND_PMU_AVSS)

**Notes:**

- The components provided by this page:

- TP_PMU_AN_P0_0
- TP_PMU_AN_P0_1
- TP_PMU_AN_P0_2
- TP_PMU_AN_P0_3
- TP_PMU_AN_P0_4
- TP_PMU_AN_P0_5
- TP_PMU_AN_P0_6
- TP_PMU_AN_P0_7

- TP_PM_PMU_P7_0
- TP_PMU_P7_1
- TP_PMU_P7_2
- TP_PMU_P7_3
- TP_PMU_P7_4
- TP_PMU_P7_5
- TP_PMU_P7_6
- TP_PMU_P7_7

**Notes:**

- All analog inputs to PMU should have a 100pF capacitor to the PMU AVSS
- None of the spares can be used for spares (Analog capable)
- Signal (GND_PMU_AVSS)
RT ALS SENSOR

Keyboard LED Driver

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<td>0.1uF</td>
<td>OMIT</td>
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<td>0.1uF</td>
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<td>1/16W</td>
<td>MF-LF</td>
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<td>20%</td>
</tr>
<tr>
<td>C3206</td>
<td>0.1uF</td>
<td>20%</td>
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<tr>
<td>C3205</td>
<td>0.1uF</td>
<td>20%</td>
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<tr>
<td>C3204</td>
<td>0.1uF</td>
<td>20%</td>
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I57, I58, I59, I51-6839, 000, 02, 32° 115
**ADAPTER CONNECTOR**

CRITICAL
Q41C Internal I/O II

---

**LEFT USB/LEFT ALS**

---

**BACKUP BATTERY / RT USB CONNECTOR**

---

**PBUS HOLD-UP CAPS**

---

**CPU FAN**

---

**GPU FAN**

---
### Page Notes

Power aliases required by this page:
- MAXBUS_GBL_L
- MAXBUS_NB_TO_CPUS_R
- MAXBUS_CPUS_BIDIR_R
- MAXBUS_DATA54
- MAXBUS_DATA42
- MAXBUS_DATA41
- MAXBUS_CPUS_BIDIR

OMIT

**BGA**

VDD18_40
VDD18_31
VDD18_23
VDD18_20
VDD18_19
VDD18_5
VDD18_1

P22
L14
J23
J20
J12
C3
C29
C14

(41 Balls on I2)

MaxBus Pull-ups / Pull-downs

**MaxBus Pull-ups / Pull-downs**

- **RP3510**
- **RP3511**
- **RP3512**
- **RP3513**
- **RP3514**

**MaxBus Pull-ups / Pull-downs**

Clock input. Length should match that of clock(s) from I2 to CPU(s).

CERM

6.3V

1uF

402

10%

402

10%

402

10%

402

10%

402

10%

402

10%

402

10%

402

10%
Main Memory Series Termination

SERIES RESISTORS FOR CONTROL SIGNALS
PINs ARE SWAPPABLE FOR RPAKS RP4600-RP4804

SERIES RESISTORS FOR CLOCKS

SERIES RESISTORS FOR CS / CKE
Do not swap with other RPAks

Scale: OF REV.
Size: D SHT

www.vinafix.vn
SLOT "B"
LOWER/REV SLOT
CUSTOMER SLOT
NOTE: AGP 8x signals are not provided

BOM options provided by this page:
- =AGP_VREF - VRef divider output for
- =PP1V5_AGP
- =PP3V3_AGP
NOTE: Implements "Power Miser" feature
- GPU_PWRPLAY signal for power sequencing
- =GPUVCORE_PGOOD - Active high Power Good Signal aliases required by this page:
- =PPVIN_LTC1778_GPU

WHEN VCORE_CNTL LOW => 1.054V
1.054V = 0.8V * (1 + Ra / Rb)

WHEN VCORE_CNTL HIGH => 1.307V
1.307V = 0.8V * (1 + Ra*(Rc+Rb) / (Rc*Rb))
The DVO bus can be run with 3.3V or 1.5V/1.8V.
NOTE: This AirPort implementation does not support PME.

PCI Devices implemented on this page:
- NONE

BOM options provided by this page:
- =USB_BT_N (Bluetooth USB D-)
- =USB_BT_P (Bluetooth USB D+)
- =PCI_AIRPORT_RESET_L (PCI Reset)
- =PCI_CLK33M_AIRPORT (33MHz PCI clock)

Signal aliases required by this page:
- =PP3V3_PWRON_BT (Bluetooth Power)
- =PP3V3_PCI (802.11g Power)

Power aliases required by this page:
I315
NOTE: This USB2 implementation supports:
- PCI_USB2_INT_L
- PCI_USB2_GNT_L
- PCI_USB2_REQ_L
- PCI_CLK33M_USB2

Signal aliases required by this page:
- PPVIO_PCI (to 3.3V or 5V)
lengthen net by ~250ps. Net has a violation on I2. May want to
NOTE: ENET_RX_DV has a hold spec
non-shared schematic page.
This page does not provide any
schematic page.
NOTE: All I2 GPIOs should have a
series termination. Any
signals, should be provided by
The PHY page or a non-shared
resistor for GPIO 16. It must be
The PHY page or a non-shared
bom options provided by this page:
NONE
Signal aliases required by this page:
- =PP2V5R3V3_PWRON_I2_ENET
Power aliases required by this page:
- =PP2V5R3V3_PWRON_I2_ENET

These GPIOs are referenced
to the Ethernet I/O rail

ENET_RESET_L
ENET_RESET_H
ENET_MDC
ENET_MDC_H
ENET_MDIO
ENET_MDIO_H
ENET_TXD_R<6>
ENET_TXD_R<4>
ENET_TXD_R<3>
ENET_TXD_R<0>
ENET_MDIO
ENET_MDC
ENET_RESET_L
ENET_RESET_H
ENET_MDC
ENET_MDC_H
ENET_MDIO
ENET_MDIO_H
ENET_TXD_R<6>
ENET_TXD_R<4>
ENET_TXD_R<3>
ENET_TXD_R<0>

I2 Ethernet Interface
NOTE: UNLESS OTHERWISE INDICATED IN THE SCHEMATIC, ANY Schematic PAGE IS INTENDED TO PROVIDE A TERMINATION RESISTOR FOR I2 ENET_DV (25K Ohm)
TO PREFabricATE THE SCH CIRCUIT IN COMPlEMENT WITH THE TABLE OF COMPONENTS TO BE INCLUDED AS PART OF THE PRESENTATION
Sandwich each RJ54 pair between chassis grounds
MDI pairs and all RJ45 pairs

Must maintain 50-ohms trace impedance on all via count, and short if possible
All differential signals should be close, parallel, matched lengths, with minimum via count, and short if possible

1. Decoupling caps
2. TX SERIES TERMINATION - LOCATE NEAR LINK
3. RX SERIES TERMINATION - LOCATE NEAR PHY

- Power aliases required by this page:
- Signal aliases required by this page:
- BOM options provided by this page:

Transformers should be mirrored on opposite sides of the board

- Place one cap at each pin of transformer
- mirrored on opposite sides of the board

Transformers should be

Ethernet routing priority:
1000BT-824-00275

XFR-SM

Ethernet Connector

SYNC_MASTER=N/A
SYNC_DATE=N/A
Place series terminators approximately halfway between Vesta and NB.
(They should probably be slightly closer to Vesta than the NB.)

---

FireWire Series Term

---

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---

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USB2 data pairs is 90 ohms.

NOTE:
- Target differential impedance for Secondary Length: 500 mils
- Secondary Max Sep: 100 mils
- Primary Max Sep: 7.5 mils
- Length Tolerance: 50 mils
- Line To Line: 19.5 mils

- RP92xxPy (pinswappable USB pulldowns)

Signal aliases required by this page:

- PP3V3_PWRON_USB

Power aliases required by this page:

- =PP1V5_PWRON_I2_USBPLL

Crystal load capacitance is 16pF

Put crystal circuit close to I2

- =RP9210
- =RP9220
- =RP9230
- =RP9211
- =RP9212
- =RP9213

One pair for each port USB2_*<0..5>

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USB2 data pairs is 90 ohms.

Signal aliases required by this page:
- =PP3V3_PWRON_USB2

Power aliases required by this page:
I42
I41
I40
I37
I35
I33

USB2_NEC_XTAL

PROVIDED BY I2 PAGES

Page Notes

Net spacing type: USB2
Note: target differential impedance for USB2 data pairs is 90 ohms.
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<table>
<thead>
<tr>
<th>Table</th>
<th>Description</th>
<th>Type</th>
<th>Value</th>
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