Enhanced MAC-1 Test Coverage

Functional test points use a P6 pad placed on bottom side.

- Place within 25 mm of power supply.
- Place within 25 mm of inverter connector.
- Place within 25 mm of battery connector.
- Place 5-10 GND TPs.
- Place within 50 mm of debug connector.
- Place within 25 mm of fan connector.
- Place within 25 mm of left USB connector.
- Place within 25 mm of right USB connector.
- Place within 25 mm of audio connector.
BOM_MCU_PMU BOM option is selected.

NOTE: Neither option is necessary when it can be monitored by in shutdown.

ALL moves the MCU to the PMU I2C bus so the time or only when the system is on.

Selects whether MMM MCU is powered all
- MMM_PWR_ALL / MMM_PWR_PWRON

I2C bus 1 to resolve address conflict.

PMU unstead. One ADT7467 connects to NB

Most devices are connected directly to

Allows bypassing Governator I2C bus.
- GOV_I2C / GOV_I2C_BYPASS

BOM options provided by this page:

(SNONE)

Signal aliases required by this page:

(SNONE)

Power aliases required by this page:

(SNONE)
Nets not requiring TPs due to JTAG

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Rev. 02 051-6839
Apple Computer Inc.

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For 4.15V cells, \( V_{CTL} = 0.123 \) REFIN

**Switcher Voltage Control**

<table>
<thead>
<tr>
<th>Component</th>
<th>Value</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>R1321</td>
<td>10K</td>
<td></td>
</tr>
<tr>
<td>R1322</td>
<td>4.7K</td>
<td></td>
</tr>
<tr>
<td>R1323</td>
<td>4.7K</td>
<td></td>
</tr>
<tr>
<td>R1325</td>
<td>2.2UF</td>
<td></td>
</tr>
<tr>
<td>C1301</td>
<td>10UF</td>
<td></td>
</tr>
<tr>
<td>C1302</td>
<td>10UF</td>
<td></td>
</tr>
<tr>
<td>Q1340</td>
<td>2N7002DW-X-F</td>
<td>SO-8-LF</td>
</tr>
</tbody>
</table>

**Switcher Current Control**

<table>
<thead>
<tr>
<th>Component</th>
<th>Value</th>
<th>Note</th>
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</thead>
<tbody>
<tr>
<td>R1341</td>
<td>4.7K</td>
<td></td>
</tr>
<tr>
<td>R1342</td>
<td>4.7K</td>
<td></td>
</tr>
<tr>
<td>R1345</td>
<td>4.7K</td>
<td></td>
</tr>
<tr>
<td>C1347</td>
<td>10UF</td>
<td></td>
</tr>
<tr>
<td>Q1346</td>
<td>2N7002DW-X-F</td>
<td>SOT23</td>
</tr>
</tbody>
</table>

**Battery Switch-Over Circuit**

**Battery Charger**

- **Input:** 100K
- **Output:** 100K
- **Input Current:** 100K
- **Output Current:** 100K

\[ V_{IN} = \frac{V_{OUT}}{R_{LOAD}} \]

\[ I_{LOAD} = \frac{V_{OUT}}{R_{LOAD}} \]

**Note:** The diagram includes components such as resistors, capacitors, and transistors, with specific values and placements indicated in the text. The diagram also highlights the battery charger circuit, with components like diodes, switches, and voltage regulators. The text is not explicitly transcribed, as it is a schematic with no textual labels for each component.
Page Notes

The 3.3V rails are meant to be aliased together. They may be split out separately for test purposes. Note that these four rails are aliased together and are therefore routed in at least one place as one pair only.

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indicated LTC3412 output voltage. Selects appropriate resistor for the burst mode for LTC3412 regulator. Selects between forced continuous and I2VCORE_CONT / I2VCORE_BURST BOM options provided by this page:

- =PP1V5_PWRON_I2PLL_LDO
- =PPVIN_PWRON_I2PLLVDD
- =PPVCORE_PWRON_I2_REG
- =PP2V7R5V5_PWRON_I2VCORE

Power aliases required by this page:

- I2VCORE_ITH_RC
- I2VCORE_MODE_VDIV
- I2VCORE_MODE
- I2VCORE_ITH
- I2VCORE_RUNSS
- I2VCORE_SW

Vburst = 0.8V * (Rb2 / (Rb1 + Rb2))
Iburst = (Vburst - 0.2V) * (3.75A / 0.8V)

If I2VCORE_BURST is selected:

- MIN_NECK_WIDTH=0.15 mm
- MIN_LINE_WIDTH=0.20 mm

One for each PVIN pin

I2 VCore Regulator

I2 PLL LDO

I2 Power Supplies
PLACE IN BETWEEN 3/5/1.5/2.5V PWR SUPPLY

PLACE UNDERNEATH UPPER RAM

PLACE CLOSE TO CPU

KEEP STUFFING RESISTORS CLOSE TO ADT7467 CONTROLLER
These must be selected to set the CPU core to Maxbus:
- CPU0_PLL0_0/1
- CPU0_PLL1_0/1
- CPU0_PLL2_0/1
- CPU0_PLL3_0/1
- CPU0_PLL4_0/1
- CPU0_PLL5_0/1

These must be selected to set the Maxbus voltage:
- CPU0_JTAG_TMS
- CPU0_JTAG_TDO
- CPU0_JTAG_TDI

Signal aliases required by this page:
- =PP3V3_PWRON_PLLSEL
- =PP1V5R1V8_MAXBUS

One of these must be selected to ensure the above condition is met:
- CPU0_BMODE0_L
- CPU0_BMODE1_L
- CPU_BVSEL<0>

One of these must be selected to set the desired spec frequency ratio to attain the desired spec:
- CPU0_BUSRATIO_24.0X
- CPU0_BUSRATIO_20.0X
- CPU0_BUSRATIO_19.0X
- CPU0_BUSRATIO_18.0X
- CPU0_BUSRATIO_17.0X
- CPU0_BUSRATIO_16.0X
- CPU0_BUSRATIO_15.0X
- CPU0_BUSRATIO_14.0X
- CPU0_BUSRATIO_13.0X
- CPU0_BUSRATIO_12.0X
- CPU0_BUSRATIO_11.0X
- CPU0_BUSRATIO_10.0X
- CPU0_BUSRATIO_9.0X
- CPU0_BUSRATIO_8.5X
- CPU0_BUSRATIO_8.0X
- CPU0_BUSRATIO_7.0X
- CPU0_BUSRATIO_6.5X
- CPU0_BUSRATIO_6.0X
- CPU0_BUSRATIO_5.5X
- CPU0_BUSRATIO_5.0X
- CPU0_BUSRATIO_4.5X
- CPU0_BUSRATIO_4.0X
- CPU0_BUSRATIO_3.5X
- CPU0_BUSRATIO_3.0X
- CPU0_BUSRATIO_2.5X
- CPU0_BUSRATIO_2.0X

CPU拉高

CPU拉低
AVDD = 0.59 * (1 + R4620/4621)
<table>
<thead>
<tr>
<th>RAM_ADDR_R&lt;12&gt;</th>
<th>RAM_ADDR_R&lt;9&gt;</th>
<th>RAM_ADDR_R&lt;8&gt;</th>
<th>RAM_ADDR_R&lt;6&gt;</th>
<th>RAM_ADDR_R&lt;4&gt;</th>
<th>RAM_ADDR_R&lt;1&gt;</th>
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<tbody>
<tr>
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**NET_TYPE**

- 2
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**PHYSICAL**

- 1/16W
- 1/16W
- 1/16W
- 1/16W
- 1/16W

**SM-LF**

- 22
- 2
- 1
- 3
- 3
- 1/16W

**MF-LF**

- 22
- 2
- 1
- 3
- 3
- 1/16W

**RAM DQS_P_R<7..0>**

- 39
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**RAM CKE<3..0>**

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**RAM_CLKDDR_2_N**

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**RAM_CLKDDR_2_P**

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**RAM_CLKDDR_3_N_R**

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**RAM_CLKDDR_0_P**

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**IN**

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**OUT**

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**RAM DQS_B_N<7..0>**

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**RAM DQS_B_P<7..0>**

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**RAM DQS_A_N<1>**

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**RAM_CKE<0>**

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**RAM_CLKDDR_1_N**

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**RAM_CLKDDR_0_P**

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**Series Resistance for Control Signals**

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**Series Resistance for Clocks**

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**Series Resistance for CS/BHE**

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**Series Termination**

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### Diagram Description

#### DDR2 VREF
- ADD ONE 0.1UF PER SLOT

#### DDR2 BYPASS
- SLOT "A"
- UPPER/STD SLOT
- FACTORY SLOT

---

**Component Details**

- **C5001**: CERM 10V 20%
- **C5002**: CERM 0.1uF 20%
- **C5003**: CERM 10V 20%
- **C5004**: CERM 0.1uF 20%

---

**Notation**

- **ADDR=0x0A(WR)/0x0A1(RD)**
- **SYNC_MASTER=MARIAS-MDIFF**
- **I TO MAINTAIN THE DOCUMENT IN CONFIDENCE AGREES TO THE FOLLOWING**
- **NOTICE OF PROPRIETARY PROPERTY**
- **NOT SIZE NONE**
SLOT "B"
LOWER/REV SLOT
CUSTOMER SLOT

DDR2 VREF
ONE 0.1uF PER SLOT

DDR2 BYPASS
SLOT "B"
### Mill Frame Buffer Constraints

**SYNC_DATE=06/03/2005**

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**SCOPE**

**SCALE**

**SIZE**

**DRAWING NUMBER**

**051-6839**

**REV.**

**02**

**D 55° 115**

**D D D D**

**C C C C**

**B B B B**

**A A A A**
NOTE: AGP 8x signals are not provided

BOM options provided by this page:

- =AGP_VREF - VRef divider output for

Signal aliases required by this page:

- =PP1V5_AGP

**Page Notes**

Place resistors midway between

Place C5732 at NB

If chips are co-located

Can also connect to NB

Connect to GPU AGP ref

Sync master = Maria's

Sync date: 06/03/2005

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051-6839 02

57° 115
NOTE: Implements "Power Miser" feature
- GPU_PWRPLAY

BOM options provided by this page:
- =GPUVCORE_PGOOD - Active high Power Good

Signal aliases required by this page:
- =PPVCORE_GPU_REG
- =PPVIN_LTC1778_GPU

Power aliases required by this page:

WHEN VCORE_CNTL LOW => 1.054V
WHEN VCORE_CNTL HIGH => 1.307V

C5830 220pF 402 1% 1/16W 5%
CERM

CERM

R5829 0 402 5%

NO STUFF

R5827 R5826 0 402 MF-LF 1/16W 5% 1/16W 5%

1.054V = 0.8V * (1 + Ra / Rb)
WHEN VCORE_CNTL LOW => 1.054V
WHEN VCORE_CNTL HIGH => 1.307V

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M11 Power Shutdown Sequencing

SPREAD SPECTRUM SUPPORT
SO=1; S1=M => -1.5% DOWN-SPREAD

LVDDR 2.8V LDO

27M OSC

PLACE THE OSCILLATOR AND R6501/R6502 CLOSE TO M18 IC

PLL

VDD

GND

GPU_SS

VOLTAGE=3.3V
MIN_NECK_WIDTH=0.2 mm
MIN_LINE_WIDTH=0.2 mm

PP3V3_GPU_SS

R6510

C6510

6.3V

20%

CERM

X7R

10V

20%

CERM

SYNC_DATE=06/03/2005

SYNC_MASTER=MARIAS

MMALMSCS

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NOTE: This USB2 implementation supports PCI Devices implemented on this page:
- USB2_NEC
- PCI_USB2_INT_L
- PCI_USB2_REQ_L
- PCI_CLK33M_USB2
- PP3V3_PCI_USB2 (D3cold rail)
- PPVIO_PCI (to 3.3V or 5V)

Power aliases required by this page:

- PCI_USB2_RESET_L
- PCI_USB2_IDSEL

SPACING
CLOCK
NET_TYPE
PHYSICAL
CLOCK

facilitate NAND-tree testing
RP7510 & R7510-12 required to

USB2_NEC
SM-LF
MF-LF
1/16W
47
5%

RP7510
SM-LF
1/16W

R7501
USB2_NEC
6
MF-LF
1/16W
10K
402
5%

R7502
MF-LF
1/16W

R7503
USB2_NEC
MF-LF
1/16W
61
402
5%

R7504
MF-LF
1/16W

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 Page Notes

Power supply required by this page:
- (PPFW_PORT2)

Signal aliases required by this page:

NOTE: This page is expected to contain the necessary aliases to map the appropriate connections and/or to properly terminate unused signals.

Notes of provided by this page:

- FireWire PHY pairs are NOT connected on this page. It is assumed that FireWire PHY page will properly terminate unused signals.

112th implementation based on Apple Firewire Design Guide (F005 3.4, 5/15/03)

Termination

Place close to FireWire PHY

“Snapback” & “Late VG” Protection

Cable Power

3rd TPA/TPB pair unused

Port 1

Port 2

FireWire Ports

051-6839 02

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Please cross terminators approximately halfway between Vesta and NB.
(They should probably be slightly closer to Vesta than the NB.)

RP9100

RP9101

RP9103

RP9102

RP9108

FW_CTL<1>

FW_CTL<0>

FW_LPS

FW_LREQ

RP9100P1

RP9100P2

RP9100P3

RP9100P4

RP9100P5

RP9100P6

RP9100P7

RP9100P8

RP9101P1

RP9101P2

RP9101P3

RP9101P4

RP9101P5

RP9101P6

RP9101P7

RP9101P8

Sync Date = 06/03/2005
Sync Master = MARIAS
051-6839 02
91° 115
USB2 data pairs is 90 ohms.

NOTE: Target differential impedance for Secondary Length:  500 mils
Secondary Max Sep:  100 mils
Primary Max Sep:   7.5 mils
Length Tolerance:   50 mils
Line To Line:     19.5 mils

BOM options provided by this page:
- =RP92xxPy (pinswappable USB pulldowns)

Signal aliases required by this page:
- =PP3V3_PWRON_USB

Power aliases required by this page:

ELECTRICAL_CONSTRAINT_SET
Net Spacing Type: USB2
Page Notes

(USB2_I2_XTAL)

(USB2_I2_XTAL)
USB2 data pairs is 90 ohms.

Signal aliases required by this page:

- NEC_CLK30M_XT2
- NEC_USB2

Page Notes

Net Spacing Type: USB2

Note: Target differential impedance for USB2 data pairs is 90 ohms.
Audio Board Connector

Place shorts at output of 3.3V and 5V regulator

XWA051
LAYOUT POWER AUDIO PWD  PWD

XWA050
LAYOUT POWER AUDIO PWD  PWD

XWA033
LAYOUT POWER AUDIO PWD  PWD

CA033
0.1uF

XWA001
LAYOUT POWER AUDIO PWD  PWD

XWA000
LAYOUT POWER AUDIO PWD  PWD

CA050
0.1uF

CA051
0.1uF

XWA001
LAYOUT POWER AUDIO PWD  PWD

XWA000
LAYOUT POWER AUDIO PWD  PWD

CA051
0.1uF

CA050
0.1uF

Place shorts at power supply

Audio Board Connector

Audio Board Connector.png

Audio Board Connector

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