1. All resistance values are in ohms, 0.1 watt +/- 5%.

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<th>CSA</th>
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<th>MASTER</th>
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### Design-Specific Rules

#### Layer-specific rules for 90-ohm differential impedance

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#### Layer-specific rules for 60-ohm single-ended impedance

<table>
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<th>Parameter</th>
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#### Layer-specific rules for 50-ohm single-ended impedance

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<td>TOP, BOTTOM</td>
<td>0.118 mm</td>
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### Board Stack-Up and Construction

#### Board Construction with Prepreg and Copper Plating

1. **Signal (1/2 oz)**
2. **Ground (1/2 oz)**
3. **Ground (1/2 oz)**
4. **Ground (1/2 oz)**
5. **Signal (1/2 oz)**
6. **Ground (1/2 oz)**
7. **Signal (1/2 oz)**
8. **Signal (1/2 oz)**
9. **CUT POWER PLANE (1 OZ)**
10. **Ground (1/2 oz)**
11. **Signal (1/2 oz)**
12. **Signal (1/2 oz)**

#### Board Design

- **MECH. HOLES**
- **GND CHASSIS INVERTER**
- **GND CHASSIS DVI2**
- **GND CHASSIS DVI3**
- **GND CHASSIS FW EMI**
- **GND CHASSIS FW_HOLE**
- **GND CHASSIS LCD3**
- **GND CHASSIS INV_GND_CLIP**
- **GND CHASSIS UPPER_DVI**

### BOM Options

#### Module Components

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Description</th>
<th>Reference</th>
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</table>

### Board Information

**Part Number:**

- **A7PM-1P67_LGA**
- **IC, CPU0, 1.5GHZ, 1.28V, 23W, 85C**
- **IC, GDDR SDRAM, 2MX32X4, 300MHZ, LF FBGA144**
- **IC, PMU05, V1, QFP**
- **IC, VOLTAGE=0V, MAKE_BASE=TRUE**
- **IC, GDDR SDRAM, 2MX32X4, 300MHZ, LF FBGA144**

**Product Information:**

- **Apple Computer Inc.**
- **051-6929**

---

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Enhanced MAC-1 Test Coverage

Functional test points use a P4 pad placed on bottom side.

| Place within 25 mm of LVDS connector. | Place within 25 mm of power supply. | Place within 25 mm of audio connector. |
| Place within 5-10 GND TPs. | Place within 25 mm of battery connector. | Place within 25 mm of ODD/HDD connector. |

- Place within 25 mm of left USB connector.
- Place within 25 mm of right USB connector.
- Place within 25 mm of fan connector.
- Place within 25 mm of TPAD connector.
- Place within 25 mm of battery connector.
- Place within 25 mm of fan connector.
- Place within 25 mm of left USB connector.
1.5V/1.8V SWITCHER

\[ Vout = 1.0V \times (1 + Ra/Rb) \]
Selects between forced continuous and BOM options provided by this page:

Power aliases required by this page:

- PP2V7R5V5_PWRON_I2VCORE

C2207
4.7M
CERM
MF-LF
1/16W

R2205
2200pF
MF-LF
1/16W
1%

MIN_NECK_WIDTH=0.15 mm
MIN_LINE_WIDTH=0.20 mm

Vburst = 0.8V * (Rb2 / (Rb1 + Rb2))
Iburst = (Vburst - 0.2V) * (3.75A / 0.8V)

MIN_NECK_WIDTH=0.15 mm
MIN_LINE_WIDTH=0.20 mm

Vburst = 0.8V * (Rb2 / (Rb1 + Rb2))
Iburst = (Vburst - 0.2V) * (3.75A / 0.8V)
GPIO Pull-ups / Pull-downs

- =PP3V3_PCI if slot E
- =PP3V3_I2_PCISLOTEGPIOS (PWRON or PCI)

GPIO_09
GPIO_15
GPIO_06
GPIO_05
EXT_13
EXT_11
EXT_15
EXT_04
EXT_02

Page Notes

- Pull-up/down to be provided by audio page. (*) - See above
- Internal pull-up to 3.3V PWRON
- 10K Pull-up to 3.3V on I2 PCI page.

Alternate GPIO Functions
(see REV.16 to form set name)

Audio Mute Sequencing
Prevents mute glitch from reaching audio circuit

Audio Mute Sequencing
Prevents mute glitch from reaching audio circuit
RT ALS SENSOR

Keyboard LED Driver

ALS Support
ADAPTER CONNECTOR

RIGHT USB BOARD

BACKUP BATTERY CONNECTOR

PBUS HOLD-UP CAPS

LEFT ALS CONNECTOR

CPU FAN

GPU FAN

Q16C Internal I/O II
BOM options provided by this page:
- =CPU0_JTAG_TCK
- =CPU0_JTAG_TDI
- =CPU0_JTAG_TDO
- =PP3V3_PWRON_PLLS

Power aliases required by this page:
- **MAXBUS_1V5** option does not exist for A7PM

### CPU0 PLL Config Circuitry

### CPU0 Frequency Configuration

- Includes CPU enabling supported by A8 only.

---

**NOTICE OF PROPRIETARY PROPERTY**

**NOT TO REVEAL OR PUBLISH IN WHOLE OR PART**

**NOT TO REPRODUCE OR COPY IT**

---

**APPLE COMPUTER INC.**

**SYNC_MASTER=MULLET SYN**

**SYNC_DATE=08/02/2005**

---

**SCALE**

**SIZE**

---

**DRAWING NUMBER**

---

**TABLE_BOMGROUP_ITEM**

---

**D 051-6929 C**

---

**37° 115**

---

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NOTE: AGP 8x signals are not provided (NONE)

BOM options provided by this page:
- AGP_GPU_RESET_L - Active low reset for GPU
- AGP_VREF - VRef divider output for Signal aliases required by this page:
- PP1V5_AGP
- PP3V3_AGP

Power aliases required by this page:
- I798

SPACING PHYSICAL DIFFERENTIAL_PAIR

AGP_CLK66M_GPUCLOCKCLOCK

R5720
MF-LF1/16W 5%
47K 402
2

R5725
MF-LF 1/16W
402 1%
2

R5721
MF-LF
1/16W
1

R5726
MF-LF
402 2

R5722
MF-LF
1%
1

R5700
AGP8X_DET_PU

ATI_DBI_HI_PU

AGP8X_DET*

DEVSEL*

FRAME*

IRDY*

STOP*

INTA*

PAR

AGP AD<30>

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AGP AD<4>

AGP AD<1>

AGP AD<5>

AGP AD<3>

AGP AD<2>

AGP AD<0>

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NOTE: Implements a low-swing DVO bus only

BOM options provided by this page:
- =PP1V8_GPU_DVO

Signal aliases required by this page:
- =PP1V5R3V3_GPU_VREF
- =PP3V3_GPU_VDDR3

Power aliases required by this page:
- GPU_LVDDR_2V8

MEMORY I/O - 1.8V/2.5V

DVO I/O (EXT.TMDS) - 1.5V/1.8V

AGP 4X I/O - 1.5V

LVDS PLL - 1.8V

LVDS I/O - 1.8V

LVDS I/O - 2.5V/2.8V

GPU (M11) I/O Power
M11 Power Shutdown Sequencing

LVDDDR 2.8V LDO

SPREAD SPECTRUM SUPPORT
$O=1$; $S1=M \Rightarrow -1.5\%$ DOWN-SPREAD

27M OSC

PLACE THE OSCILLATOR AND R6501/R6502 DIFFERENTIAL_PAIR CLOSE TO M18 IC

FERR-EMI-100-OHM

(PLACE R6500 CLOSE TO OSC)
TMDS data pairs is 100 ohms.

Signal aliases required by this page:

- PP3V3_RUN_SI
- SI_I2C_DATA
- SI_I2C_CLK
- RP68xxPy (pinswappable series R)

Upper DVO series termination

Place close to GPU

Upper Channel series termination

Upper Channel Common-mode Termination

Upper TMDS Transmitter
Page Notes

Power aliases required by this page:
- =USB_BT_N            (Bluetooth USB D-)
- =USB_BT_P            (Bluetooth USB D+)
- =PCI_AIRPORT_RESET_L (PCI Reset)
- =PCI_CLK33M_AIRPORT  (33MHz PCI clock)

Signal aliases required by this page:
- =PP3V3_PWRON_BT (Bluetooth Power)
- =PP3V3_PCI      (802.11g Power)

Power aliases required by this page:
- =PP3V3_PWRON_BT

NOTE: This AirPort implementation does not support PME.

PCI Devices implemented on this page:
AD17 (Slot "A") - AirPort (0x????/0x????)

BOM options provided by this page:

Page Notes

Reference implementation on this page:
AD17 (Slot "A") - AirPort (0x????/0x????).

NOTE: This AirPort implementation does not support PME.
PCI Devices implemented on this page:
- USB2_NEC

BOM options provided by this page:
- =PPVIO_PCI (to 3.3V or 5V)

Signal aliases required by this page:
- =PCI_USB2_GNT_L
- =PCI_USB2_IDSEL
- =PCI_USB2_RESET_L

Net Type

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ELECTRICAL_CONSTRAINT_SET

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</table>

Note: This VDD implementation supports 3.3V.

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### Page Notes

- Signal aliases required by this page:
  - UATA_DEV_R
  - UATA_DSTROBE
  - UATA_HOST_R
  - UATA_HOST
  - UATA_HSTROBE
  - UATA_DD
  - UATA_DD_R<6..0>
  - UATA_DA_R<2..0>
  - UATA_DD_R<15..8>
  - UATA_DMACK_L_R
  - UATA_STOP_R
  - UATA_HSTROBE_R

- Power aliases required by this page:
  - IDE_IORDY
  - IDE_CIORDY
  - IDE_CIORDY
  - IDE_CS1FX_L
  - IDE_CS0FX_L
  - IDE_CS3FX_L

### UATA100 SERIES TERMINATION

Place close to I2

- RP8150P5
- RP8150P6
- RP8150P8
- RP8150P7
- RP8151P5
- RP8151P7
- RP8151P8
- RP8152P5
- RP8152P7
- RP8152P8
- RP8153P5
- RP8153P6
- RP8153P7
- RP8153P8
- RP8154P5
- RP8154P7
- RP8154P8

### 12 UATA Interface

- DATA_AOUT
- DATA_AIN
- DATA_AOUT_B
- DATA_AIN_B
- DATA_BOUT
- DATA_BIN
- DATA_BOUT_B
- DATA_BIN_B
- DATA_COUT
- DATA_CIN
- DATA_COUT_B
- DATA_CIN_B
- DATA_DOUT
- DATA_DIN
- DATA_DOUT_B
- DATA_DIN_B
- DATA_EOUT
- DATA_EIN
- DATA_EOUT_B
- DATA_EIN_B
- DATA_FOUT
- DATA_FIN
- DATA_FOUT_B
- DATA_FIN_B
- DATA_GOUT
- DATA_GIN
- DATA_GOUT_B
- DATA_GIN_B
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- DATA_HIN
- DATA_HOUT_B
- DATA_HIN_B
- DATA_AIN_2
- DATA_AOUT_2
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- DATA_CIN_2
- DATA_COUT_2
- DATA_DIN_2
- DATA_DOUT_2
- DATA_EIN_2
- DATA_EOUT_2
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- DATA_GOUT_2
- DATA_HIN_2
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- DATA_FOUT_3
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- DATA_GOUT_3
- DATA_HIN_3
- DATA_HOUT_3
- DATA_AIN_4
- DATA_AOUT_4
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- DATA_DIN_4
- DATA_DOUT_4
- DATA_EIN_4
- DATA_EOUT_4
- DATA_FIN_4
- DATA_FOUT_4
- DATA_GIN_4
- DATA_GOUT_4
- DATA_HIN_4
- DATA_HOUT_4

---

OFSHT  OUT
IN
BI

---

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Violation on I^2. May want to non-shared schematic page.

Resistor for GPIO 16. It must be pull-up or pull-down resistor.

NOTE: All I^2 GPIOs should have a termination, including clock signals, should be provided by the PHY page or a non-shared series termination. Any termination, including clock signals, should be provided by the PHY page or a non-shared series termination.

NOTE: This page does not provide any BOM options provided by this page:
Place series terminators approximately halfway between Vesta and NB. (They should probably be slightly closer to Vesta than the NB.)

<table>
<thead>
<tr>
<th>Component</th>
<th>Value</th>
<th>Tolerance</th>
<th>Quantity</th>
</tr>
</thead>
<tbody>
<tr>
<td>R9100</td>
<td>0</td>
<td>5%</td>
<td>1/16W</td>
</tr>
<tr>
<td>R9101</td>
<td>21</td>
<td>5%</td>
<td>1/16W</td>
</tr>
<tr>
<td>R9102</td>
<td>63</td>
<td>5%</td>
<td>1/16W</td>
</tr>
<tr>
<td>R9103</td>
<td>72</td>
<td>5%</td>
<td>1/16W</td>
</tr>
</tbody>
</table>

FireWire Series Term

- FW_LREQ_R FW_LREQ_R
- FW_LPS_R FW_LPS_R
- FW_CTL_R<0> FW_CTL_R<0>
- FW_CTL_R<1> FW_CTL_R<1>
- FW_CTL_R<2> FW_CTL_R<2>
- FW_CTL_R<3> FW_CTL_R<3>
- FW_CTL_R<4> FW_CTL_R<4>
- FW_CTL_R<5> FW_CTL_R<5>
- FW_CTL_R<6> FW_CTL_R<6>
- FW_CTL_R<7> FW_CTL_R<7>
- FW_CTL_R<8> FW_CTL_R<8>

www.vinafix.vn
Secondary Length: 500 mils
Secondary Max Sep: 100 mils
Primary Max Sep: 7.5 mils
USB2 data pairs is 90 ohms.
NOTE: Target differential impedance for Length Tolerance: 50 mils
Line To Line: 19.5 mils

BOM options provided by this page:
- =RP92xxPy (pinswappable USB pulldowns)

Signal aliases required by this page:
- =PP3V3_PWRON_USB

Power aliases required by this page:
- =PP1V5_PWRON_I2_USBPLL

Crystal load capacitance is 16pF

Put crystal circuit close to I2

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SYNC_MASTER=N/A  SYNC_DATE=N/A

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NOTICE OF PROPRIETARY PROPERTY

www.vinafix.vn
NOTE: Target differential impedance for USB2_NEC (NONE)

Signal aliases required by this page:

Power aliases required by this page:

Page Notes

Page Noted

Net spacing type: USB2

Target differential impedance for USB2 data pairs is 90 ohms
### Spacing & Physical Constraints

**Spacing Rule**
- Spaces between elements are as specified except where noted.

**Physical Assignment**
- Physical placement is as specified except where noted.

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**Information**
- Drawing Number: 12345678
- Scale: None
- Notice: To be filled out by Apple Computer, Inc.

### Schematics

#### FW (FireWire Digital)
- FW_SELFFW: 0.2 MM
- FW_SELF: 0.2 MM
- FW: 0.2 MM

#### ENET (Ethernet Digital)
- ENET_SELFFW: 0.2 MM
- ENET_SELF: 0.2 MM
- ENET: 0.2 MM

#### PCI
- PCI_SELFFW: 0.2 MM
- PCI_SELF: 0.2 MM
- PCI: 0.2 MM

#### RAM
- RAM_SELFFW: 0.2 MM
- RAM_SELF: 0.2 MM
- RAM: 0.2 MM

#### UATA
- UATA_SELFFW: 0.2 MM
- UATA_SELF: 0.2 MM
- UATA: 0.2 MM

#### USB2
- USB2_SELFFW: 0.2 MM
- USB2_SELF: 0.2 MM
- USB2: 0.2 MM

#### Audio AGP
- AGP_SELFFW: 0.4 MM
- AGP_SELF: 0.4 MM
- AGP: 0.4 MM

#### I2S
- I2S_SELFFW: 0.2 MM
- I2S_SELF: 0.2 MM
- I2S: 0.2 MM

#### I2C
- I2C_SELFFW: 0.2 MM
- I2C_SELF: 0.2 MM
- I2C: 0.2 MM

#### MaxBus
- MaxBus_SELFFW: 0.2 MM
- MaxBus_SELF: 0.2 MM
- MaxBus: 0.2 MM

#### ENETCONN
- ENETCONN_SELFFW: 0.2 MM
- ENETCONN_SELF: 0.2 MM
- ENETCONN: 0.2 MM

#### FW_TP
- FW_TP_SELFFW: 0.2 MM
- FW_TP_SELF: 0.2 MM
- FW_TP: 0.2 MM

#### I2_FBCLK / XTAL
- I2_FBCLK_SELFFW: 0.2 MM
- I2_FBCLK_SELF: 0.2 MM
- I2_FBCLK: 0.2 MM
- XTAL_SELFFW: 0.2 MM
- XTAL_SELF: 0.2 MM
- XTAL: 0.2 MM

### Notes
- ENET_SELFFW is CONNECTED TO ENET SELF.
- I2C_SELFFW is CONNECTED TO I2C SELF.
- UATA_SELFFW is CONNECTED TO UATA SELF.
- USB2_SELFFW is CONNECTED TO USB2 SELF.
- AGP_SELFFW is CONNECTED TO AGP SELF.
- I2S_SELFFW is CONNECTED TO I2S SELF.
- I2C_SELFFW is CONNECTED TO I2C SELF.

**Spacing & Physical Constraints**
- Spaces between elements are as specified except where noted.
- Physical assignment is as specified except where noted.

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### Schematics

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- PCI_SELF: 0.2 MM
- PCI: 0.2 MM

#### RAM
- RAM_SELFFW: 0.2 MM
- RAM_SELF: 0.2 MM
- RAM: 0.2 MM

#### UATA
- UATA_SELFFW: 0.2 MM
- UATA_SELF: 0.2 MM
- UATA: 0.2 MM

#### USB2
- USB2_SELFFW: 0.2 MM
- USB2_SELF: 0.2 MM
- USB2: 0.2 MM

#### Audio AGP
- AGP_SELFFW: 0.4 MM
- AGP_SELF: 0.4 MM
- AGP: 0.4 MM

#### I2S
- I2S_SELFFW: 0.2 MM
- I2S_SELF: 0.2 MM
- I2S: 0.2 MM

#### I2C
- I2C_SELFFW: 0.2 MM
- I2C_SELF: 0.2 MM
- I2C: 0.2 MM

#### MaxBus
- MaxBus_SELFFW: 0.2 MM
- MaxBus_SELF: 0.2 MM
- MaxBus: 0.2 MM

#### ENETCONN
- ENETCONN_SELFFW: 0.2 MM
- ENETCONN_SELF: 0.2 MM
- ENETCONN: 0.2 MM

#### FW_TP
- FW_TP_SELFFW: 0.2 MM
- FW_TP_SELF: 0.2 MM
- FW_TP: 0.2 MM

#### I2_FBCLK / XTAL
- I2_FBCLK_SELFFW: 0.2 MM
- I2_FBCLK_SELF: 0.2 MM
- I2_FBCLK: 0.2 MM
- XTAL_SELFFW: 0.2 MM
- XTAL_SELF: 0.2 MM
- XTAL: 0.2 MM

**Notes**
- ENET_SELFFW is CONNECTED TO ENET SELF.
- I2C_SELFFW is CONNECTED TO I2C SELF.
- UATA_SELFFW is CONNECTED TO UATA SELF.
- USB2_SELFFW is CONNECTED TO USB2 SELF.
- AGP_SELFFW is CONNECTED TO AGP SELF.
- I2S_SELFFW is CONNECTED TO I2S SELF.
- I2C_SELFFW is CONNECTED TO I2C SELF.