3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.
### BOM Configuration

#### BOM OPTION Groups

<table>
<thead>
<tr>
<th>BOM GROUP</th>
<th>BOM OPTIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1 COMMON</td>
<td>ALTERNATE,CPU_2_16GHZ,VRAM_SAM256</td>
</tr>
<tr>
<td>&quot;EEE:VHV&quot;</td>
<td>M1_COMMON,CPU_1_83GHZ,VRAM_SAM128</td>
</tr>
<tr>
<td>&quot;EEE:VHT&quot;</td>
<td>M1_COMMON,CPU_2_0GHZ,VRAM_SAM256</td>
</tr>
<tr>
<td>&quot;EEE:VHU&quot;</td>
<td>M1_COMMON,CPU_2_16GHZ,VRAM_SAM256</td>
</tr>
</tbody>
</table>

#### Bar Code Label / EEE #'s

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>630-7570</td>
<td>1</td>
<td>630-7570,256VRAM_RAM_STA</td>
</tr>
<tr>
<td>630-7571</td>
<td>1</td>
<td>630-7571,128VRAM_RAM_STA</td>
</tr>
<tr>
<td>630-7569</td>
<td>1</td>
<td>630-7569,SAM256_RAM_STA</td>
</tr>
</tbody>
</table>

#### Module Parts

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>128S0100</td>
<td>1</td>
<td>128S0100,256VRAM_RAM_STA</td>
</tr>
<tr>
<td>128S0091</td>
<td>1</td>
<td>128S0091,128VRAM_RAM_STA</td>
</tr>
<tr>
<td>128S0089</td>
<td>1</td>
<td>128S0089,SAM256_RAM_STA</td>
</tr>
</tbody>
</table>

#### Alternate Parts

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
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<tbody>
<tr>
<td>826-4393</td>
<td>1</td>
<td>826-4393,ATP,INVERTER_BUF_KBDLED</td>
</tr>
<tr>
<td>826-4393</td>
<td>1</td>
<td>826-4393,ATP,INVERTER_BUF_KBDLED</td>
</tr>
</tbody>
</table>

---

www.vinafix.vn
Power Supply NO_TESTS

- NO_TEST
- EXPOSED_VIA

CPU FSB NO_TESTS

- NO_TEST
- EXPOSED_VIA

Misc EXPOSED_VIA Nets

- EXPOSED_VIA

Functional Test Points

- Fan Connectors
  - FUNC_TEST
    - CPU FSB NO_TESTs
  - Battery Digital Connector
  - Left I/O Data Connector
  - Left ALS Connector
  - Camera Connector
  - Thermal Diode Connectors
  - Other Func Test Points
  - Current Sense Calibration

Battery Digital Connector

- FUNC_TEST

Left I/O Power Connector

- FUNC_TEST

Sync Date = N/A

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

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www.vinafix.vn
Chassis connection to be made at the mounting hole northwest of the DVI connector

Chassis connection to be made at the mounting hole east of the LVDS connector

Chassis connection to be made at the mounting hole east of the DVI connector

Chassis connection to be made at the mounting hole west of the LVDS connector

**Ethernet Power Management Support**

**USB Port "A"** (Debug Port) = Right USB 2.0 Port

**USB Port "B"** = Trackpad (Geyser)

**USB Port "C"** = Left USB 2.0 Port

**USB Port "D"** = Camera

**USB Port "E"** = ExpressCard

**USB Port "F"** = IR Receiver

**USB Port "G"** = Bluetooth (NI3P)

**USB Port "H"** = Reserved (PCI-E Mini Card)

Trace deleted to make room for other diffpairs over RAM connector.

**Signal Aliases**
CPU ZONE THERMAL SENSOR

PLACEHOLDER ADT7461A

LAYOUT NOTE:
(TO CPU INTERNAL THERMAL DIODE)

CPU THERMD_N

LAYOUT NOTE:
CPU ZONE THERMAL SENSOR
ROUTE CPU_THERMD_P AND
10 MIL TRACE
LAYER.
10 MIL SPACING
FOR CPU_THERMD_P AND CPU_THERMD_N ON SAME
ADD GND GUARD TRACE

PLACE U1001 NEAR THE U1200

PARTS LIST:

PLACEHOLDER ADT7461A

C1001
1/16W 1% 499
C1002
1/16W 5% 402
R1001
12K 1/16W 499
R1002
10K 1/16W 402
R1005
10K 1/16W 402
R1006
10K 1/16W 402

www.vinafix.vn
CPU ITP700FLEX DEBUG SUPPORT

ITP TCK SIGNAL LAYOUT NOTE:
ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX CONNECTOR'S FBO PIN.

(XAND WITH RESET BUTTON) XDP DBRESET L

ITP IS USING TAP I/F, NC IN 945GM CHIPSET SYSTEM. DEBUG PORT ACTIVE, AND WITH SYSTEM RESET LOGIC

REV. 1
APPLE COMPUTER INC.
SCALE NONE
ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX CONNECTOR'S FBO PIN.

ITP TCO
CRITICAL

SYNC_DATE=10/12/2005
SYNC_MASTER=M42

=PP1V05 S0_CPU

=PPIV3 SS_SB

ITPCM

11 104

63

CPU ITP700FLEX DEBUG

www.vinafix.vn
Tie VCCA_CRTDAC to VCC Core rail, and tie VSSA_CRTDAC and VCC.Sync to GND. Tie HSYNC and VSYNC to GND. Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie CRT Disable TV-Out Disable filtering components. Unused DAC outputs should remain powered, but can omit unused DAC outputs must. Component: DACA, DACB & DACC S-Video: DACB & DACC only.

Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used...
NB Misc Interfaces

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APPLE COMPUTER INC.

DRAWING NUMBER OF 104

SCALE NONE

WEB VINAFIX.VN
1.05V or 1.5V

Place in cavity

Layout Note:
Place near pin K31

Layout Note:
Place near pin K33

NB Power 1

SYNC_MASTER=(MASTER)

SYNC_DATE=(MASTER)
RTC Battery Connector

SB RTC Crystal Circuit

Platform Reset Connections

Buffered

Initial resistor values are based on CMY, but may change after characterization.

SB Misc

Linda Card represents 3 loads
TPM_LRESET_L
SMC_LRESET_L
DEBUG_RST_L
PEG_RESET_L
LIO_PLT_RESET_L

SYNC_DATE=(MASTER)

SYNC_MASTER=(MASTER)

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www.vinafix.vn
"Lower" (surface-mount) slot
The reference voltage must be provided.
One cap for each side of every RPAK, one cap for every two discrete resistors. Ensure CS_L and ODT resistors are close to SO-DIMM connector.
**Page Notes**

Power aliases required by this page:
- =PP5V_S0_MEMVTT
- =PP1V8_S0_MEMVTT
- =PP0V9_S0_MEMVTT_LDO

Signal aliases required by this page:
- MEMVTT

BOM options provided by this page:
- =PP5V_S0_MEMVTT
- =PP1V8_S0_MEMVTT
- =PP0V9_S0_MEMVTT_LDO

---

**DDR2 Vtt Regulator**

- FF = =PP5V_S0_MEMVTT
- FF = =PP1V8_S0_MEMVTT
- FF = =PP0V9_S0_MEMVTT_LDO

If power inputs are not S0, MEMVTT EN can be used to
do a soft reset of the system. It is okay to turn off 5V and
leave 1.8V powered in S3.

---

**Memory Vtt Supply**

- =PP5V_S0_MEMVTT
- =PP1V8_S0_MEMVTT
- =PP0V9_S0_MEMVTT_LDO

---

**Dimension Notes**

- MIN_NECK_WIDTH = 0.2 mm
- MIN_LINE_WIDTH = 0.2 mm
- PP1V8_S0_MEMVTT_VDDQ

---

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---

**Memory Vtt Supply**

- PP0V9_S0_MEMVTT_LDO
- PP1V8_S0_MEMVTT
- PP5V_S0_MEMVTT

---

**www.vinafix.vn**
Yukon Power Control

Allows powering Yukon down during battery sleep to save power

<table>
<thead>
<tr>
<th>State</th>
<th>PM_SLP_S4_L</th>
<th>PM_SLP_S3BATT</th>
<th>PM_SLP_S3BATT_L</th>
<th>P2V5S3_EN_L</th>
<th>P1V2S3_RUNSS</th>
</tr>
</thead>
<tbody>
<tr>
<td>S0 Batt</td>
<td>0V</td>
<td>3.3V</td>
<td>0V (3.3V ON)</td>
<td>3.3V</td>
<td>0V (2.5V ON)</td>
</tr>
<tr>
<td>S3 AC</td>
<td>0V</td>
<td>3.3V</td>
<td>0V (3.3V ON)</td>
<td>3.3V</td>
<td>0V (2.5V ON)</td>
</tr>
<tr>
<td>S3 Batt</td>
<td>PBUS</td>
<td>3.3V</td>
<td>PBUS (3.3V OFF)</td>
<td>0V</td>
<td>Hi-Z (2.5V OFF)</td>
</tr>
<tr>
<td>S5 AC</td>
<td>0V</td>
<td>PBUS (3.3V OFF)</td>
<td>0V (2.5V OFF)</td>
<td>0V</td>
<td>Hi-Z (2.5V OFF)</td>
</tr>
<tr>
<td>G3H Batt</td>
<td>PBUS</td>
<td>0V</td>
<td>Hi-Z (2.5V OFF)</td>
<td>0V</td>
<td>Hi-Z (2.5V OFF)</td>
</tr>
<tr>
<td>S0</td>
<td>3.3V</td>
<td>0V (3.3V ON)</td>
<td>3.3V (1.2V ON)</td>
<td>3.3V (1.2V ON)</td>
<td></td>
</tr>
<tr>
<td>S3</td>
<td>3.3V</td>
<td>0V (3.3V ON)</td>
<td>3.3V (1.2V ON)</td>
<td>3.3V (1.2V ON)</td>
<td></td>
</tr>
<tr>
<td>S5</td>
<td>0V</td>
<td>PBUS (3.3V OFF)</td>
<td>0V (2.5V OFF)</td>
<td>0V</td>
<td>Hi-Z (2.5V OFF)</td>
</tr>
<tr>
<td>G3H</td>
<td>0V</td>
<td>PBUS (3.3V OFF)</td>
<td>0V (2.5V OFF)</td>
<td>0V</td>
<td>Hi-Z (2.5V OFF)</td>
</tr>
</tbody>
</table>

**SYNC_DATE=(MASTER)**
**SYNC_MASTER=(MASTER)**

Yukon Power Control

051-7099

APPLE COMPUTER INC.
Port Power Switch

Right USB Port

Place L5200, L5205 and L5206 across moat
Left I/O Board Connector

Place XW500 at 5V switcher

Place XW5105 at 5V switcher

Place XW510 at 5V switcher

Place XW5500 at 5V switcher

Place XW5505 at 5V switcher

Place XW5510 at 5V switcher

Place XW5515 at 5V switcher

---

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---

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PCI-E x1 Port "A" = Ethernet (Yukon)
PCI-E x1 Port "B" = PCI-E Mini Card

C5710
PCI-E x1 Port "C" = ExpressCard

C5720
PCI-E x1 Port "D" = Unused

C5721
PCI-E x1 Port "E" = Unused

C5722
PCI-E x1 Port "F" = Unused

TP_PCIE_F_R2DP
TP_PCIE_F_D2RN
TP_PCIE_F_D2RP
TP_PCIE_F_R2DN

TP_PCIE_D_R2RN
TP_PCIE_D_R2DP
TP_PCIE_D_D2RP
TP_PCIE_D_D2RN

TP_PCIE_E_R2DN
TP_PCIE_E_D2RN
TP_PCIE_E_D2RP
TP_PCIE_E_R2DP

TP_PCIE_E_R2DP
TP_PCIE_E_D2RN
TP_PCIE_E_D2RP
TP_PCIE_E_R2DN

TP_PCIE_C_D2RN
TP_PCIE_C_D2RP
TP_PCIE_C_R2DN
TP_PCIE_C_R2RP

TP_PCIE_B_D2RN
TP_PCIE_B_D2RP
TP_PCIE_B_R2DN
TP_PCIE_B_R2DP

TP_PCIE_B_D2RN
TP_PCIE_B_D2RP
TP_PCIE_B_R2DN
TP_PCIE_B_R2DP

TP_PCIE_B_R2D_C_P
TP_PCIE_B_R2D_C_N
TP_PCIE_B_D2R_P
TP_PCIE_B_D2R_N

TP_PCIE_C_R2D_C_P
TP_PCIE_C_R2D_C_N
TP_PCIE_C_D2R_P
TP_PCIE_C_D2R_N

TP_PCIE_E_R2D_C_P
TP_PCIE_E_R2D_C_N
TP_PCIE_E_D2R_P
TP_PCIE_E_D2R_N

TP_PCIE_F_R2D_C_N
TP_PCIE_F_D2R_N
TP_PCIE_F_D2R_P
TP_PCIE_F_R2D_P

TP_PCIE_D_R2D_C_P
TP_PCIE_D_R2D_C_N
TP_PCIE_D_D2R_P
TP_PCIE_D_D2R_N
CAN BE LEFT NO-CONNECTED.

SMC_XXX WHERE XXX IS THE PORT NUMBER.
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R6309 IS NOT NEEDED WHEN SHARING SPI FLASH WITH ICH7M AND TEKOA (LAN CHIP)

R6307 AND R6306 SHOULD BE PLACED LESS THAN 100 MILS FROM ICH7M
R6303 SHOULD BE PLACED LESS THAN 100 MILS FROM FLASH ROM
NOTE: Be aware of pull-up on this signal. If unconnected, powers up with PVIN.

Connect RUNSS off-page to control

\[
\text{Vout} = 0.8V \times \left(1 + \frac{\text{Ra}}{\text{Rb}}\right)
\]

\[
\text{Vout} = 0.8V \times \left(1 + \frac{\text{Ra}}{\text{Rb} + \text{Rc}}\right)
\]

---

**2.5V S0 FET**

- \( \text{PP2V5_S0_P2V5S0} \)
- \( \text{PP2V5_S0_FET} \)
- \( \text{PV2V5S3_EN_L} \)
- \( \text{PP2V5_S0_P2V5S0} \)

**1.2V S0 FET**

- \( \text{PP1V2_S0_P1V2S0} \)
- \( \text{PP1V2_S0_P1V2S0} \)
- \( \text{P1V2S0_EN_RC} \)

**2.5V & 1.2V Regulators**

- \( \text{SYNC_MASTER} = \text{MASTER} \)
- \( \text{SYNC_DATE} = \text{MASTER} \)

---

**2.5V S3 Regulator**

- \( \text{PPVIN_S3_P1V2S3} \)
- \( \text{PPVIN_S3_P2V5S3} \)
- \( \text{P2V5S3_EN_L} \)
- \( \text{PPVIN_S3_PSVIN} \)

**1.2V S3 Regulator**

- \( \text{PV1V2S3_VFB} \)
- \( \text{PV1V2S3_SW} \)
- \( \text{PV1V2S3_ITH} \)
Left I/O Power Connector

Battery Connector (Digital Signals)

PBus-In & Battery Connectors
GDDR3 Frame Buffer A

This master version contains the following information:

- Pins and connections of GDDR3 frame buffer A
- Schematic diagram of GDDR3 frame buffer A

Page Notes

- Page notes are required by this page: (NONE)
- Page notes provided by this page: (NONE)

1. GDDR3 vendor/device identification scheme.
2. MIN_LINE_WIDTH = 0.25 mm
3. MIN_NECK_WIDTH = 0.25 mm
4. VOLTAGE = 1.8V
5. MIN_LINE_WIDTH = 0.25 mm

Page Dimensions: 1224.0x792.0
Sum of peak currents on this page: 605mA

Signal aliases required by this page:

Power aliases required by this page:

R9350
499
402
1%

VOLTAGE=2.5V
MIN_LINE_WIDTH=0.2 mm

PP2V5_S0_GPU_VDD2DI

8
8
22UF

CERM
805
805
402
MF-LF

ATI_R2SET

2
2
1

2
1

1uF

CERM
402
CERM

73
12
12
0402
SM
SM
SM
SM

VOLTAGE=2.5V
MIN_NECK_WIDTH=0.25 mm

VOLTAGE=2.5V
MIN_LINE_WIDTH=0.2 mm

VOLTAGE=0V
MIN_LINE_WIDTH=0.3 mm

VOLTAGE=0V
MIN_NECK_WIDTH=0.25 mm

ATI M56 Video Interfaces

Composite/S-Video VOA Component

www.vinafix.vn
Place series R's and common-mode filtering close to GPU, common mode chokes near connector.
Left ALS Connector

Bluetooth (M13P), IR & SATA HDD Flex Connector

NOTE: _UF_ nets cross DDR2 signals and pick up significant noise. Common-mode chokes are to remove this noise from DATA signals.
LVDS Interface Pull-downs

NOTE: These parts are to counter an invalid state caused by the pull-up. Pull-up in the panel though some voltage will still be seen on LVDS signals when they should be 0V.

<table>
<thead>
<tr>
<th>Layer</th>
<th>LVDS Interface Pull-downs</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1</td>
<td>LVDS_PD</td>
</tr>
<tr>
<td></td>
<td>5%</td>
</tr>
<tr>
<td></td>
<td>1/16W</td>
</tr>
<tr>
<td></td>
<td>8.2K</td>
</tr>
<tr>
<td>RP9900</td>
<td></td>
</tr>
<tr>
<td>RP9901</td>
<td></td>
</tr>
<tr>
<td>RP9902</td>
<td></td>
</tr>
</tbody>
</table>

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<td></td>
<td>1/16W</td>
</tr>
<tr>
<td></td>
<td>8.2K</td>
</tr>
<tr>
<td>RP9903</td>
<td></td>
</tr>
</tbody>
</table>

LVDS Interface Pull-downs

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</tr>
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<td></td>
<td>1/16W</td>
</tr>
<tr>
<td></td>
<td>8.2K</td>
</tr>
<tr>
<td>RP9904</td>
<td></td>
</tr>
<tr>
<td>RP9905</td>
<td></td>
</tr>
<tr>
<td>RP9906</td>
<td></td>
</tr>
</tbody>
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LVDS Interface Pull-downs

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<td>5%</td>
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<tr>
<td></td>
<td>1/16W</td>
</tr>
<tr>
<td></td>
<td>8.2K</td>
</tr>
<tr>
<td>RP9907</td>
<td></td>
</tr>
<tr>
<td>RP9908</td>
<td></td>
</tr>
<tr>
<td>RP9909</td>
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</tr>
</tbody>
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LVDS Interface Pull-downs

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<tr>
<td></td>
<td>1/16W</td>
</tr>
<tr>
<td></td>
<td>8.2K</td>
</tr>
<tr>
<td>RP9910</td>
<td></td>
</tr>
<tr>
<td>RP9911</td>
<td></td>
</tr>
<tr>
<td>RP9912</td>
<td></td>
</tr>
</tbody>
</table>

LVDS Interface Pull-downs

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<table>
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<td></td>
<td>1/16W</td>
</tr>
<tr>
<td></td>
<td>8.2K</td>
</tr>
<tr>
<td>RP9913</td>
<td></td>
</tr>
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