### BOMs

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>CRITICAL</th>
<th>BOM COMMENT</th>
</tr>
</thead>
<tbody>
<tr>
<td>826-4393</td>
<td>8</td>
<td>LBL, P/N LABEL, PCB, 28MM X 6MM</td>
<td>CRITICAL</td>
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### Module Parts

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<tr>
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<th>QTY</th>
<th>DESCRIPTION</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1170052</td>
<td>1</td>
<td>IC, SANTAYNEZ, MEROM, 1.6GHz, ES, 20W, 956BGA</td>
<td>CRITICAL</td>
<td>CPU_1_HYDRO</td>
</tr>
<tr>
<td>1170052</td>
<td>1</td>
<td>LOW POWER CLOCK SYNTHESIZER, SLG2AP101, 68PIN</td>
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<tr>
<td>1170052</td>
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<td>IC, PRGM, SST SST89V54RD, UCNTRLR, M82</td>
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<tr>
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<td>IC, ISL6258, REV2, BAT CHGR, 28P QFN</td>
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### Alternate Parts

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### Configuration Options

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<tr>
<td>FWC: Master = No/1/1</td>
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<tr>
<td>FWC: ZADDO/1/1</td>
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### 1UF 0402 Capacitor Vendor Tables for Acoustics

#### SAMSUNG

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<tr>
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<th>REFERENCE DES</th>
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<tbody>
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<td>1008009</td>
<td>5</td>
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<tr>
<td>1008010</td>
<td>6</td>
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#### MURATA

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### 2.2UF 0402 Capacitor Vendor Tables for Acoustics

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### 10UF 0603 Capacitor Vendor Tables for Acoustics

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ICT Test Points

These nets have a ICT_TEST property. This indicates a MUSTHAVE requirement for ICT.
Mini-XDP Connector

NOTES: This is not the standard XDP pinout.
Use with 920-0451 adapter board to support CPU, NB & SB debugging.

Direction of XDP module to edge of board

Please avoid any obstructions

XDP_PWRGD
NB_CFG[4]
NB_CFG[7]
NB_CFG[6]
NB_CFG[1]
NB_CFG[0]
R1399
XDP
1/20W
1K
201
MF
23
26
53 52 51 46
21
25

1
R1315
1/20W
54.9
201
XDP
MF
1%
2
1

www.vinafix.vn

Use with 920-0451 adapter board to support CPU, NB & SB debugging.

NOTE: This is not the standard XDP pinout.
Tie VCC_AXG and VCC_AXG_NCTF to GND.
Tie DPLL_REF_CLK* and DPLL_REF_SSCLK* to VCC (VCore).
Tie DPLL_REF_CLK and DPLL_REF_SSCLK to GND.
TV_DCONSELx to GND.
Can also tie CRT_DDC_*, L_CTRL_*, L_DDC_*, SDVO_CTRL_* and Internal Graphics Disable
and filtered at all times!
VCCD_CRT, VCCD_QDAC and VCC_SYNC.
VSYNC and CRT_TVO_IREF to GND.
Tie TVx_DAC, TVx_RTN, R/R#/G/G#/B/B#, HSYNC, CRT & TV-Out Disable
rails must be filtered except for VCCA_CRT.
All CRT/TVDAC rails must be powered.  All
Tie R/R#/G/G#/B/B#, HSYNC and VSYNC to GND.
CRT Disable / TV-Out Enable
TVDAC rails.  VCCA_TVx_DAC and VCCA_DAC_BG can
Tie TVx_DAC and TVx_RTN to GND.  Must power all
Can leave all signals NC if LVDS is not implemented.
LVDS Disable

---

www.vinafix.vn
Current numbers from Crestline EDS, doc #21749.

76 28 28 250 mA
27 27

60 mA
40 mA
40 mA
40 mA
10 mA
5 mA
64 72

57 26

51 24

52 23

60 27

53 22

61 21

51 21

8 19

7 18

6 17

46 44 44

30 29

19 16

8 7

6 5

0.4 mA

64 26

53 26

63 26

PP1V8_S0 NB VCCTXLVDS
PP1V25_S0M NB VCCA_HPLL
PP1V25_S0 NB_VCCA_DPLLB
PP1V25_S0 NB_PEGPLL
PP1V8_S0_NB_VCCTXLVDS
www.vinafix.vn
NOTE: This filter is required even if using only external graphics.

Filtering changed per EN 50601-2-2

CRITICAL

Layout Notes:

- B.0.0
- A
- D
- C
- 051-7230

NB Graphics Decoupling

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Platform Reset Connections

Unbuffered

Buffered

SB RTC Crystal Circuit

This part is never stuffed, it provides a set of pads on the board to short or to solder a reset button.

Place R2808 pads on bottom side near board edge

Silk: "SYS RST"

SB Misc
CPU speed is currently set to 200MHz.
MEM CLOCK TERMINATION
Place one resistor at each end of Y split

---
R3390  R3391
0.05  2.2

---
R3392  R3393
200  200

---
R3394  R3395
200  200

---
R3396  R3397
200  200

---

One cap for each side of every RPAK, one cap for every two discrete resistors
BOM OPTION shown at the top of each group applies to every part below it

---

LAYOUT NOTE: PLACE ONE CAP CLOSE TO EVERY TWO PULLUP RESISTORS TERMINATED TO PREV_XU_MEM_TERM
Micro DVI, USB, to RIO Hatch Assembly

Audio Connector

Hatch and Audio Connectors

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APPLE INC.

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USB 2.0 CONNECTOR

Connect to 5V S5 or S3 per layout

Current limit to 1.5A continuous

USB/SMC MUX

USB external connectors

Notice of proprietary property
IPD Connector

Inverted to drive SMC_RESET logic

Power Button Inverter

Inverted to drive SMC_RESET logic
those designated as inputs require pull-ups. Pins designed as outputs can be left floating; those designated as inputs require pull-ups.
Debug Power Button

SMC 1.05V to 3.3V Level Shifting

- Reset Power Button
- Place R5001 on bottom side near board edge
- Silk: "SMC_RST"

2

1/16W

Place on bottom side

57

40

Silk: "PWR BTN"

LSOC_PRESS_H
SMC_ONOFF_H
SMC_ONOFF_L
SMC_MANUAL_RST_L

SSM6N15FE
Q5030
OUT

1/16W

5%

1/20W

3.3V TO PBUS LEVEL SHIFTING

- R5010 will pull down SMC MANUAL_RST_L in the event of a keyboard SMC reset generated when left shift, option, and control and the power button is depressed.

- Q5030 will pull down SMC MANUAL_RST_L in the event of a keyboard SMC reset generated when left shift, option, and control and the power button is depressed.

SMC 3.3V to 1.05V Level Shifting

- CPU_PROCHOT_L
- PM_THRMTRIP_L

Battery Pack Status

SMC AVREF Supply

3.3V TO PBUS LEVEL SHIFTING

- CPU_PROCHOT
- PM_THRMTRIP

SMC 1.05V to 3.3V Level Shifting

- Reset Power Button
- Place R5001 on bottom side near board edge
- Silk: "SMC_RST"

2

1/16W

Place on bottom side

57

40

Silk: "PWR BTN"

LSOC_PRESS_H
SMC_ONOFF_H
SMC_ONOFF_L
SMC_MANUAL_RST_L

SSM6N15FE
Q5030
OUT

1/16W

5%

1/20W

3.3V TO PBUS LEVEL SHIFTING

- R5010 will pull down SMC MANUAL_RST_L in the event of a keyboard SMC reset generated when left shift, option, and control and the power button is depressed.

- Q5030 will pull down SMC MANUAL_RST_L in the event of a keyboard SMC reset generated when left shift, option, and control and the power button is depressed.

SMC 3.3V to 1.05V Level Shifting

- CPU_PROCHOT_L
- PM_THRMTRIP_L

Battery Pack Status

SMC AVREF Supply

3.3V TO PBUS LEVEL SHIFTING

- CPU_PROCHOT
- PM_THRMTRIP
LPC+SPI Connector

Place R5101 close to J5100

Place halfway between SPIROM and J5100

Place R5102 close to J5100

Place within 0.5" of SB

Pullup to internal ROM on S5

LPC+SPI Connector

SPI_CS MUX

Place halfway between SPIROM and J5100

Place within 0.5" of SB

Place R5102 close to J5100

Place within 0.5" of SB

Pullup to internal ROM on S5
**ACIN VOLTAGE SENSE**

Max 14.5V + 10% ACIN = 3.0V SMC_PBUS_VSENSE

R5300 and R5301 values chosen for RC filter @ 4.53KOhm Thevenin resistance

**GPU VOLTAGE SENSE**

**PBUS VOLTAGE SENSE**

Nominal 8.4V PBUS = 3.0V SMC_PBUS_VSENSE

R5350 and R5351 values chosen for RC filter @ 4.53KOhm Thevenin resistance

---

**Voltage Sensors**

APPLE INC.

051-7230  A-A-D

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REMOTE TEMP AT HEAT SPREADER

APN: 518S0354

CPU THERMAL DIODE

LOCAL TEMP NEAR POWER SUPPLIES

(TO CPU INTERNAL THERMAL DIODE)

1. ROUTE DXP AND DXN DIFFERENTIALLY
2. ROUTE GROUNDED GUARD TRACES AROUND THE DXP/DXN DIFF PAIR
3. PLACE C5522 NEAR U5520 VDD

WRITE: 0x9E READ: 0x9F

WRITE: 0x90 READ: 0x91

TEMPERATURE SENSORS
FAN CONNECTOR

---

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---

**Diagram Details**

- **Motor Control GND**
- **5V DC**
- **TACH**
- **NC NC**
- **Fan Connector**
- **R5665 47K**
- **R5660 47K**
- **R5661 100K**
- **Q5660 SSM3K15FV**
- **51800354**
- **PP3V3_B_S0**
- **SMC_FAN_0_TACH**
- **SMC_FAN_0_CTL**
- **PP5V_S0**
- **FAN_RT_TACH**
- **FAN_RT_PWM**

---

**Technical Specifications**

- **SYNC_MASTER=M70**
- **SYNC_DATE=01/09/2007**

---

**Website:** www.vinafix.vn
SUDDEN MOTION SENSOR

APN: 338S0354

I2C addresses:
Address low => 0x30, 0x31
Address high => 0x32, 0x33
Alias SCL/SDA to GND if using analog outputs only

Desired orientation when placed on board top-side:

Desired orientation when placed on board bottom-side:

www.vinafix.vn
SPI ROM

---

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---

PLACEMENT_NOTE=Place R6114 within 12.7mm of U6100

PLACEMENT_NOTE=Place R6190 within 12.7mm of U2300

PLACEMENT_NOTE=Place R6191 within 12.7mm of U2300

PLACEMENT_NOTE=Place R6193 within 12.7mm of U2300

---

**SPI ROM**

- SPI_INT_CE_L<0>
- SPI_A_INT_HOLD_L
- SPI_A_INT_CLK
- SPI_A_SI_R
- SPI_A_SCLK_R
- SPI_CE_R_L<0>
- SPI_SI_R
- SPI_A_INT_WP_L
- SPI_SO
- SPI_CE_L<0>
- SPI_A_INT_SI
- SPI_SCLK_R
- SPI_A_SO_R

**SPI ROMs**

SYNC_MASTER=WFERRY

SYNC_DATE=04/26/2006

---

www.vinafix.vn
1.5V/1.05V POWER SUPPLY

State | PM_SLP_S3_L | PP1V5_S0 | PP1V05_S0  
S0    | HIGH        | 1.5V      | 1.05V      
S3/S5/G3Hot | LOW | 0.0V      | 0.00V      

Vout = 0.758V * (1 + Ra / Rb)
Vout = 0.758V * (1 + Rc / Rb)

Routing Note:
The discharge path (VO1) should have a sensing trace, separate from the output voltage.

Placement Note:
R7361, C7305 close to U7300 pin 15.

Note: pu on PGOOD page
1.8V/0.9V POWER SUPPLY

State | PM_S4_STATE_L | PM_SLP_S3 | PP1V8_S3 | PP0V9_S0
-----|---------------|-----------|----------|----------
S0   | HIGH         | HIGH      | 1.8V     | 0.9V     
S3   | HIGH         | LOW       | 1.8V     | 0.9V     
5V/3V_LOW | LOW       | LOW       | 0.0V     | 0.0V     

\[ \text{Vout} = 0.75V \times (1 + \frac{\text{Ra}}{\text{Rb}}) \]

Placement Note:
- PLACE C7507, C7508 GND NEAR PIN 1
- PLACE XW7500, NEAR C7542 PIN 2
- PLACE C7543 NEAR NB

Routing Note:
- using Kelvin connection.
- Connect CS_GND to 6 vias under the thermal pad
- MIN_LINE_WIDTH=0.3 mm
- MIN_NECK_WIDTH=0.2 mm
- MIN_LINE_WIDTH=0.6 mm
- MIN_NECK_WIDTH=0.2 mm

CRITICAL Q7520 SI7110DN PWRPK-1212-8
CRITICAL Q7521 SI7108DNS PWRPK-1212-8

MAX CURRENT = 11A
PWM FREQ. = 400 kHz
5V/3.3V POWER SUPPLY

State | SN6_PM_G2_EN | PP3V3_G3H | PP5V_S5 | PP3V3_S5
G3H  | LOW          | 3.3V      | 0.0V    | 0.0V
S0/S3/S5 | HIGH        | 3.3V      | 5.0V    | 3.3V

Routing Note:
- A dedicated trace to the output cap
- The discharge path (VO1) should have a dedicated trace to the output cap
- Put 6 vias under the thermal pad

Vout = 1V \times (1 + Ra / Rb)
5.106V = 1V \times (1 + 20K / 4.87K)

PWM FREQ. = 280 kHz
MAX CURRENT = 6.0A
(inductor limited) PP5V_S5

PWM FREQ. = 430 kHz
MAX CURRENT = 7.8A
(OCP setting limited) PP3V3_S5

5V/3.3V Supplies

C7600:
- 10UF
- X5R
- 6.3V
- OMIT

C7604:
- 10UF
- X5R
- 6.3V
- OMIT

C7602:
- close to U7600 pin 22.

C7603:
- close to U7600 pin 21.

C7605:
- close to U7600 pin 20.

R7601,
- 5.90K
- 201
- MF
- 1%

R7603:
- 7.15K
- 201
- MF
- 1%

R7605:
- 241

WARNING:
- The discharge path (VO1) should have a dedicated trace to the output cap
- Put 6 vias under the thermal pad

Other components,
- C7640
- C7641
- C7667
- C7660
- R7668
- R7669
- R7670
- C7680
- C7681
- C7682
- SI7110DN
- X5R
- 6.3V
- 20%
- A1
- B1
- C1
- D1
- E1
- F1
- G1
- H1
- I1
- J1
- K1
- L1
- M1
- N1
- O1
- P1
- Q1
- R1
- S1
- T1
- U1
- V1
- W1
- X1
- Y1
- Z1

Dedicated trace
- A
- B
- C
- D

www.vinafix.vn
3.425V G3H SUPPLY

Supply needs to guarantee 3.31V delivered to SMC VRef generator

Q7730 will pull down
P3V42G3H_OUTPUT in the event of a keyboard SMC reset
generated when left shift, option, and control
and the power button is depressed.

Vout = 1.25V * (1 + Ra / Rb)

1.25V S0 REGULATOR

Vout = 0.8V * (1 + Ra / (Rb + Rc))

www.vinafix.vn
S3 FETS & S3/S5 CONTROL

5V/3.3V S5 RUN/SS CONTROL  1.8V S3 RUN/SS CONTROL

--- Diagram ---

--- Diagram ---
LVDS, Camera Conn. and ALS Conn.

APN: 518S0356

www.vinafix.vn
SST8051 microcontroller for HDCP support
A 1.3K OHM 1% RESISTOR IS REQUIRED BETWEEN CRT_IREF AND CRT_TVO_IREF.

Place components near J4200 unless otherwise noted.

CRITICAL
Some signals require 27.4-ohm single-ended impedance. Most CPU signals with impedance requirements are 55-ohm single-ended.

**NOTE:** Design Guide allows closer spacing if signal lengths can be shortened.

Design Guide recommends FSB signals be routed only on internal layers. Worst-case spacing is 2:1 within Data bus, with 3:1 spacing to the DSTBs. Worst-case spacing is 2:1 within Addr bus, with 3:1 spacing to the ADSTBs.

### CPU Signal Constraints

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**NOTE:** 7 mil gap is for VCCSense pair, which

### CPU/FSB Constraints

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**NOTE:** 7 mil gap is for VCCSense pair, which
CRT_HSYNC/CRT_VSYNC signals are 55-ohm +/- 15% single-ended impedance.

- 55-ohm +/- 15% from second termination resistor to connector.
- 50-ohm +/- 15% from first to second termination resistor.
## DDR2 Memory Bus Constraints

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## Memory Net Properties

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### PCI Bus Constraints

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**PHYSICAL_RULE_SET**

- ENET_MDI
- PCIE_D2R
- PCIE_R2D
- LAN_55S
- PCI_55S

**TABLE_SPACING_RULE_ITEM**

- **TABLE_SPACING_ASSIGNMENT_ITEM**
  - =100_OHM_DIFF

**DIFFPAIR NECK GAP**

- **TABLE_PHYSICAL_RULE_ITEM**
  - **TABLE_PHYSICAL_RULE_HEAD**

### Electrical Constraint Set

- **SB_CLINK_VREF1**
- **SB_CLINK_VREF0**
- **CLINK_NB_RESET_L**
- **ENET_MDI0**
- **ENET_100D**
- **ENET_LAN**
- **LAN_55S**
- **GLAN_COMP**
- **PCIE_B_D2R**
- **PCIE_B_R2D**
- **PCIE_A_R2D**
- **INT_PIRQD_L**
- **PCI_REQ2_L**
- **PCI_CNTL**
- **PCI_CNTL**
- **PCI_C_BE_L**
- **PCI_AD**
- **PCI_AD20**
- **PCI_AD19**

**PHYSICAL**

- **CLINK_VREF**
- **CLINK_VREF**
- **CLINK**
- **CLINK**

- **ENET_MDI**
- **ENET_MDI**
- **ENET_MDI**

- **ENET_LAN**
- **ENET_LAN**

- **GLAN_100D**
- **ENET_GLAN**

- **PCIE_100D**

- **PCI_55S**
- **PCI_55S**
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**SB Constraints (2 of 2)**

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**PHYSICAL_RULE_SET**

- ENET_MDI
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- LAN_55S
- PCI_55S

**TABLE_SPACING_RULE_ITEM**

- **TABLE_SPACING_ASSIGNMENT_ITEM**
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  - **TABLE_PHYSICAL_RULE_HEAD**

**III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART**

**II NOT TO REPRODUCE OR COPY IT**

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![Image of a page from a document]
### M82 Board-Specific Spacing & Physical Constraints

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<td>0.100 mm</td>
<td>0.1 mm</td>
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<td>0.100 mm</td>
<td>0.1 mm</td>
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<tr>
<td>70_OHM_DIFF</td>
<td>27P4_OHM_SE</td>
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<td>55_OHM_SE</td>
<td>50_OHM_SE</td>
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<td>45_OHM_SE</td>
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### DIFFPAIR PRIMARY GAP

<table>
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</tr>
</thead>
<tbody>
<tr>
<td>0.280 mm</td>
<td>0.250 mm</td>
<td>0.180 mm</td>
<td>0.200 mm</td>
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### DIFFPAIR NECK GAP

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</tr>
</thead>
<tbody>
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<td>0.280 mm</td>
<td>0.205 mm</td>
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### LINE-TO-LINE SPACING

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<tbody>
<tr>
<td>0.25 mm</td>
<td>0.2 mm</td>
<td>0.2 mm</td>
<td>0.3 mm</td>
<td>0.1 mm</td>
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### WEIGHT

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