### Schematic / PCB #’s

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### ALIASES RESOLVED

- **SCHEM, MLB, MBP17**
- **05/07/2007**
- **深入推进和应用**
- **MEANING**
- **METRIC**

Apple Computer Inc.
### BOM Variants

<table>
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<tr>
<th>Part Number</th>
<th>QTY</th>
<th>Description</th>
<th>Reference EKE</th>
<th>Critical</th>
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</tr>
</thead>
<tbody>
<tr>
<td>630-764521</td>
<td>1</td>
<td>CPU, 2.4GHZ, BST, VRAM-SAMSUNG</td>
<td>M76_COMMON,CPU_2_4GHZ,FB_256_SAMSUNG</td>
<td>CRITICAL</td>
<td>630-764521</td>
</tr>
<tr>
<td>630-686513</td>
<td>1</td>
<td>CPU, 2.4GHZ, BST, VRAM-SAMSUNG</td>
<td>M76_COMMON,CPU_2_4GHZ,FB_256_HYNIX</td>
<td>CRITICAL</td>
<td>630-686513</td>
</tr>
<tr>
<td>630-777717</td>
<td>1</td>
<td>CPU, 2.4GHZ, BST, VRAM-SAMSUNG</td>
<td>M76_COMMON,CPU_2_4GHZ,FB_256_HYNIX</td>
<td>CRITICAL</td>
<td>630-777717</td>
</tr>
<tr>
<td>630-472121</td>
<td>1</td>
<td>CPU, 2.4GHZ, BST, VRAM-SAMSUNG</td>
<td>M76_COMMON,CPU_2_4GHZ,FB_256_HYNIX</td>
<td>CRITICAL</td>
<td>630-472121</td>
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### M76 BOM Groups

<table>
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<th>BOM Group</th>
<th>BOM Number</th>
<th>Reference EKE</th>
<th>Critical</th>
<th>ROM Option</th>
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<tr>
<td>M76_COMMON</td>
<td>M76_COMMON</td>
<td>M76_COMMON</td>
<td>M76_COMMON,CPU_2_4GHZ,FB_256_SAMSUNG</td>
<td>CRITICAL</td>
<td>M76_COMMON</td>
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<tr>
<td>M76_COMMON</td>
<td>M76_COMMON</td>
<td>M76_COMMON</td>
<td>M76_COMMON,CPU_2_4GHZ,FB_256_HYNIX</td>
<td>CRITICAL</td>
<td>M76_COMMON</td>
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<th>Description</th>
<th>Reference EKE</th>
<th>Critical</th>
<th>ROM Option</th>
</tr>
</thead>
<tbody>
<tr>
<td>626-519231</td>
<td>1</td>
<td>U8400, U8400, U8400, U8400</td>
<td>M76_COMMON,CPU_2_4GHZ,FB_256_SAMSUNG</td>
<td>CRITICAL</td>
<td>626-519231</td>
</tr>
<tr>
<td>626-585333</td>
<td>1</td>
<td>U2300, U2300, U2300</td>
<td>M76_COMMON,CPU_2_4GHZ,FB_256_SAMSUNG</td>
<td>CRITICAL</td>
<td>626-585333</td>
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<tr>
<td>626-581933</td>
<td>1</td>
<td>U2900, U2900, U2900</td>
<td>M76_COMMON,CPU_2_4GHZ,FB_256_SAMSUNG</td>
<td>CRITICAL</td>
<td>626-581933</td>
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<th>Critical</th>
<th>ROM Option</th>
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<td>228011361</td>
<td>1</td>
<td>U4900, U4900, U4900</td>
<td>M76_COMMON,CPU_2_4GHZ,FB_256_SAMSUNG</td>
<td>CRITICAL</td>
<td>228011361</td>
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<tr>
<td>228015361</td>
<td>1</td>
<td>U80001, U80001, U80001</td>
<td>M76_COMMON,CPU_2_4GHZ,FB_256_SAMSUNG</td>
<td>CRITICAL</td>
<td>228015361</td>
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<tr>
<td>228018361</td>
<td>1</td>
<td>U2300, U2300, U2300</td>
<td>M76_COMMON,CPU_2_4GHZ,FB_256_SAMSUNG</td>
<td>CRITICAL</td>
<td>228018361</td>
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<tr>
<td>228019361</td>
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<td>U3700, U3700, U3700</td>
<td>M76_COMMON,CPU_2_4GHZ,FB_256_SAMSUNG</td>
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### Alternate Parts

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<th>Reference EKE</th>
<th>Critical</th>
<th>ROM Option</th>
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</thead>
<tbody>
<tr>
<td>630-764521</td>
<td>1</td>
<td>CPU, 2.4GHZ, BST, VRAM-SAMSUNG</td>
<td>M76_COMMON,CPU_2_4GHZ,FB_256_SAMSUNG</td>
<td>CRITICAL</td>
<td>630-764521</td>
</tr>
<tr>
<td>630-686513</td>
<td>1</td>
<td>CPU, 2.4GHZ, BST, VRAM-SAMSUNG</td>
<td>M76_COMMON,CPU_2_4GHZ,FB_256_HYNIX</td>
<td>CRITICAL</td>
<td>630-686513</td>
</tr>
<tr>
<td>630-777717</td>
<td>1</td>
<td>CPU, 2.4GHZ, BST, VRAM-SAMSUNG</td>
<td>M76_COMMON,CPU_2_4GHZ,FB_256_HYNIX</td>
<td>CRITICAL</td>
<td>630-777717</td>
</tr>
<tr>
<td>630-472121</td>
<td>1</td>
<td>CPU, 2.4GHZ, BST, VRAM-SAMSUNG</td>
<td>M76_COMMON,CPU_2_4GHZ,FB_256_HYNIX</td>
<td>CRITICAL</td>
<td>630-472121</td>
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13.2.0
3/07/07 -- Removed RX3920-RX3927.

13.3.0 15.4.0
3/07/07 -- Q7080 PP1V8_GPU FET changed for lower Rds on from FDM6296 to RJK0301DPB
- SB GPIOs: Changed R2514 from pulldown to pulldown to correct auto power-on issue (Linda card detect GPIO)
- FireWire Ports: Changed D4260 to PDS540 for higher current capacity

15.4.0
15.2.0
3/28/07 -- Change BOM option for 1.8V regulator feedback to 1.8V GPU FET input.
- SB GPIOs: Added PCI_DEVID<3..0> pullup straps

3/21/07 -- Integrated m75/mlb CSA pgs. 84,85 & 89 through:
- Power Control: Tied all 4 5V/3.3V enables (EN1, EN2, EN3 and EN5) together as part of PM_G2_EN

3/20/07 -- Change R9811 from 15.0K to 14.0K. This is so that M57 inverter and split inverter can use same backlight table.

3/19/07 -- Added OMIT BOM option to L4731 and L4741.

3/19/07 -- SMBus: moved Remote Temps from SMC B to SMC A in order to use EMC1043-5.

3/19/07 -- Power Control: Corrected alias connections for 5V/3V3 S5 enable signals

3/19/07 -- Changed Resistors for M76 Vcore setpoints (i.e. 1.05V, 1.05V, 1.125V, 1.25V)

3/19/07 -- <rdar://problem/5073301> M76: Change GPU Vmin

3/19/07 -- <rdar://problem/4838347> EMC - M76 MLB changes

3/19/07 -- Change table test notes.

3/22/07 -- Added P9762 for voltage zinggle on ISL5275 BOOT and PHASE pins.

3/20/07 -- Added P9760 for potential battery inrush current.

3/19/07 -- Removed CH930 to R7802 for space reasons.

3/16/07 -- Change BOM option for 1.8V regulator feedback to 1.8V GPU FET input.

3/12/07 -- Added OMIT BOM option P1V8S3_1V825 to M76_COMMON2 BOM group.

3/08/07 -- Changed Resistors for M76 Vcore setpoints (i.e. 1.05V, 1.05V, 1.125V, 1.25V)

3/08/07 -- Changed R9960 511K from NOSTUFF to INV_SPLIT to improve current and voltage asymmetry ratio.

3/08/07 -- Added OMIT BOM option L4731 and L4741.

3/06/07 -- Changed Charger PWM limit resistor according to MARC K.'S M70 values

3/05/07 -- Integrated m75/mlb pages 22,25,28,30-32,50,53-55,72,74,76,78,80-82,84-90,94,95 through:
- Thermal Sensors: Moved remote sensor U5500 to SMC SMBus A and S3 power rail to clear I2C addr clash

3/05/07 -- Removed BOM option for HDCP as feature is removed.

3/03/07 -- Moved F7090 to F7400 to F7405 for higher current capacity

3/03/07 -- Changed 1.8V supply feedback resistors R7520 to 21.5K 0.1% and R7521 15.0K 0.1%.

3/03/07 -- Changed 1.8V supply feedback resistors R7520 to 21.5K 0.1% and R7521 15.0K 0.1%.
- GPU FB: Changed unterminated-mode reference voltage to 4% (R8297 -> 1.02k, R8432/82, R8532/82 -> 2.2K).
- GPU FB: Changed unterminated-mode reference voltage to 4% (R8297 -> 1.02k, R8432/82, R8532/82 -> 2.2K).

3/02/07 -- Change 46833 by cerickso@m75_mlb_051-7225_12.5.0_tmp.Ecad on 2007/03/02 09:49:13

3/01/07 -- <rdar://problem/50632> Task: Current Surge When Insert Battery Without AC Plugged-In

3/01/07 -- Change BOM option for 1.8V regulator feedback to 1.8V GPU FET input.

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3/01/07 -- Changed 1.8V supply feedback resistors R7520 to 21.5K 0.1% and R7521 15.0K 0.1%.

3/01/07 -- Change BOM option for 1.8V regulator feedback to 1.8V GPU FET input.

3/01/07 -- <rdar://problem/50632> Task: Current Surge When Insert Battery Without AC Plugged-In

3/01/07 -- Change BOM option for 1.8V regulator feedback to 1.8V GPU FET input.

3/01/07 -- Added OMIT BOM option L4731 and L4741.

3/01/07 -- Change BOM option for 1.8V regulator feedback to 1.8V GPU FET input.

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3/01/07 -- Change BOM option for 1.8V regulator feedback to 1.8V GPU FET input.
Chassis connection to be made at the mounting hole east of the LVDS connector.

Thermal Module Holes

All holes are plated through holes with two exceptions:

Chassis GNDs

Frame holes

Digital Ground

RAM door (Torx) holes

Add 8 blind vias per side to GND

Stuff either B7020 or B980.
Mini-XDP Connector

NOTE: This is not the standard XDP pinout.
Use with 920-0451 adapter board to support CPU, NB & SB debugging.

Direction of XDP module
Please avoid any instructions on un-numbered side of R1300
Tie VCC_AXG and VCC_AXG_NCTF to GND.

If video is used, VCC_AXG must remain powered with proper
decoupling. Otherwise, tie VCC_AXG to GND also.

Note: NR DC says to tie LVSU_VPEEL/L to GND. This causes
a glitch during wake-up on LVDS DATA/SCLK pair. One
recommendation is to float both signals, see Radar #5267636.

CRT Disable / TV-Out Enable

ART-OUT signal usage:

Composite: VGA only
Component: RGB, S-VGA & S-VGA

Unused DAC outputs must remain powered, but can
out filtering components. Unused DAC outputs
must be properly filtered with 7-ohm resistors.

TV-Out Disable / TV-Out Enable

Tie LVDS_R and LVDS_B to GND. Must power all
LVDS rails. LVDS_RATE and LVDS_RATE_B must
share filtering with VCC_CRT, CRT.

CRT Disable / CRT Enable

Tie X/R/0/V0/R0/0 to HSYNC and VSYNC to GND.
All CRT/VGA rails must be powered. All
rails must be filtered except for VCC_CRT.

CRT & TV-Out Disable

TV-Out Disable, CRT=0/0/0/0/0/0/0, S-VGA, VSYNC,
VSYNC and CRT_VD, SVP to GND.
Can tie the following rails to GND:
CRT_VD, CRT_VD, CRT_VD, CRT_VD, CRT_VD,
CRT_CRT, CRT_CRT, CRT_CRT, CRT_CRT.

NOTE: Must keep VCC_TVOUT powered
and filtered at all times.

Internal Graphics Disable

Enable instructions for TV-Out and CRT & TV-Out Disable above.
Can also tie CRT_VD_V, CRT_VD_V, CRT_VD_V, CRT_VD_V,
CRT_VD_V, CRT_VD_V, CRT_VD_V, CRT_VD_V, CRT_VD_V,
CRT_VD_V, CRT_VD_V, CRT_VD_V, CRT_VD_V, CRT_VD_V,
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CRT_VD_V, CRT_VD_V, CRT_VD_V, CRT_VD_V, CRT_VD_V,
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CRT_VD_V, CRT_VD_V, CRT_VD_V, CRT_VD_V, CRT_VD_V,
CRT_VD_V, CRT_VD_V, CRT_VD_V, CRT_VD_V, CRT_VD_V,
CRT_VD_V, CRT_VD_V, CRT_VD_V, CRT_VD_V, CRT_VD_V,
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CRT_VD_V, CRT_VD_V, CRT_VD_V, CRT_VD_V, CRT_VD_V,
CRT_VD_V, CRT_VD_V, CRT_VD_V, CRT_VD_V, CRT_VD_V,
CRT_VD_V, CRT_VD_V, CRT_VD_V, CRT_VD_V, CRT_VD_V,
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CRT_VD_V, CRT_VD_V, CRT_VD_V, CRT_VD_V, CRT_VD_V,
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CRT_VD_V, CRT_VD_V, CRT_VD_V, CRT_VD_V, CRT_VD_V,
CRT_VD_V, CRT_VD_V, CRT_VD_V, CRT_VD_V, CRT_VD_V,
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CRT_VD_V, CRT_VD_V, CRT_VD_V, CRT_VD_V, CRT_VD_V,
CRT_VD_V, CRT_VD_V, CRT_VD_V, CRT_VD_V, CRT_VD_V,
CRT_VD_V, CRT_VD_V, CRT_VD_V, CRT_VD_V, CRT_VD_V,
CRT_VD_V, CRT_VD_V, CRT_VD_V, CRT_VD_V, CRT_VD_V,
CRT_VD_V, CRT_VD_V, CRT_VD_V, CRT_VD_V, CRT_VD_V,
CRT_VD_V, CRT_VD_V, CRT_VD_V, CRT_VD_V, CRT_VD_V,
CRT_VD_V, CRT_VD_V, CRT_VD_V, CRT_VD_V, CRT_VD_V,
CRT_VD_V, CRT_VD_V, CRT_VD_V, CRT_VD_V, CRT_VD_V,
CRT_VD_V, CRT_VD_V, CRT_VD_V, CRT_VD_V, CRT_VD_V,
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CRT_VD_V, CRT_VD_V, CRT_VD_V, CRT_VD_V, CRT_VD_V,
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CRT_VD_V, CRT_VD_V, CRT_VD_V, CRT_VD_V, CRT_VD_V,
CRT_VD_V, CRT_VD_V, CRT_VD_V, CRT_VD_V, CRT_VD_V,
CRT_VD_V, CRT_VD_V, CRT_VD_V, CRT_VD_V, CRT_VD_V,
CRT_VD_V, CRT_VD_V, CRT_VD_V, CRT_VD_V, CRT_VD_V,
CRT_VD_V, CRT_VD_V, CRT_VD_V, CRT_VD_V, CRT_VD_V,
CRT_VD_V, CRT_VD_V, CRT_VD_V, CRT_VD_V, CRT_VD_V,
Crestline Thermal Diode Pins

Mainly for investigation. If not used, alias these nets directly to GND.
Current numbers from Crestline EDS Addendum, doc #20127.

VCCD_TVDAC also powers internal thermal sensors.

These 2 caps should be within 4.56 mm of NB edge.

Layout Note:

MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.3 MM

 PP1V25_S0_NB_VCCD_TVDAC

PP1V8_S0_NB_DPLL

PPVCORE_S0_NB_GFX

CMCH Graphics Core Power

Crestline LVDS Support

NB Graphics Decoupling

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NOTES

Drawing Number

22 92

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Current numbers from ICH8M Max Power Estimates Rev 2.0, doc #610194.
**CK505 Configuration Straps**

**FCT_SEL** (GFX clock select)

**FS_A, FS_B, FS_C** (Host clock freq select)

**FS_CPS>B, FS_A CPU MHz**

(Only 100-200MHz supported by SLM001P534 and CY28656-5)

---

**CLK Termination**

(Note: HOST/DK/TX clock termination requires SLM001P534 or equiv. support only)

---

**CLKREQ Controls**

---

**Unused Clocks**

---

**Clock Termination**
One cap for each side of every SS4K, one cap for every two discrete resistors

Ensure CS_L and ODT resistors are close to SO-DIMM connector.
### ENET Enable Generation

"ENET = "OUT" || ["AC" as "ACT" as "WOL_EN"]

*Note:* S3 term is guaranteed by source of R3800 & Q3810, MUST BE S3 RAIL.

### 3.3V ENET FET

**NOTE:** S3 term is guaranteed by FET & pull-up source, MUST BE S3 RAIL.

### WLAN Enable Generation

"WLAN = "OUT" || ["AC" as "ACT" as "WOL_EN"]

**NOTE:** S3 term is guaranteed by source of R3800 & Q3810, MUST BE S3 RAIL.

### Yukon AVDDL LDO

1.9V for Yukon Ultra, 2.5V for Yukon EC

Yukon Ultra requires 1.9V on its magnetics to pass compliance tests.

**NOTE:** S3 term is guaranteed by source of R3800 & Q3810, MUST BE S3 RAIL.

### Yukon Power Control

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Yukon Power Control

12345678

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Yukon Crystal

Yukon Power Control

1.9V for Yukon Ultra, 2.5V for Yukon EC

Yukon Ultra requires 1.9V on its magnetics to pass compliance tests.

**NOTE:** S3 term is guaranteed by source of R3800 & Q3810, MUST BE S3 RAIL.
Transformers should be mirrored on opposite sides of the board.

Place one cap at each pin of transformers.
Strap via alias on port page.

Lo: Beta Mode enable (1394b).
Hi: Data-Strobe only (1394a).

DSx Straps:
Implement 1K pull-up or pull-down on port page.
FireWire Port Power Switch

Current Limit/Active Late-VG Protection

Late-VG Event Detection

R4220 & R4225 PADS SHOULD BE ROUTED DIRECTLY TO MAX5944 SENSEA & SENSEB RESPECTIVELY. SENSEA & SENSEB SHOULD NOT BE PART OF THE MAIN CURRENT PATH.

Current Limits
0.020 ohm => 2.4A
0.025 ohm => 2A
0.050 ohm => 1.6A (Ideal)

MAX5944 current limit trips if integrator (counter) reaches 16. A new sample (taken every 125 us) is weighted as 1 if over the limit (at any point during the period) and 1/2 if under the limit. At a result, the decision tends to trim easily on decisions that produce periodic current spikes. Current limit has been set higher to compensate.
FireWire PHY Config Straps

Configured PHY for:
- 2-port Portable Power Class (18) - Port "A" Data-Store only (1394A)
- Port "A" Bilingual (1394B)

Termination
Place close to FireWire PHY
LTS requires even though
eps calls out 2.33mW

Late-VG Protection Power

CABLE POWER

FireWire Ports

SYNC_MASTER=M75_MLB SYNC_DATE=12/04/2006
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Left Clutch Barrel Interconnect

SIM Interconnect

Connector Shield
Camera Power
Camera Ground
Camera USB D-
Camera TwinAx Shield 2
Camera USB D+
Camera Ground
Camera Power
Connector shield

MIN_LINE_WIDTH=0.25 mm
VOLTAGE=5V
MIN_NECK_WIDTH=0.2 mm

PP5V_S3
USB_WWAN_P
USB_WWAN_N
USB_CAMERA_P
USB_CAMERA_N
USB camera_F_P
USB camera_F_N
PPVCC_WWAN_SIM
MIN_LINE_WIDTH=0.25 mm
VOLTAGE=3.3V
MIN_NECK_WIDTH=0.2 mm

R4740
R4741
51450171
51450172

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NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.
LPC+ Connector  
FWH_INIT_L Generation

---

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LPC+ Debug Connector

---

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Switches in fixed load on power supplies to calibrate current sense circuits
Battery Current Sense

DCIn Current Sense

Battery Charger Thermal Sensor

(Tm0P) R:0x93, W:0x92
Left ALS Filter

Left ALS circuit has 1K series-R

Keyboard LED Driver

WP: This circuit does not use return, can tie cathode to GND on topcase flex

Right ALS Circuit

RTALS_OP_IN and RTALS_OP_COMP need to be matched
I2C addresses:

- ADDR low => 0x30, 0x31
- ADDR high => 0x32, 0x33

Alias SCL/SDA to GND if using analog outputs only

Desired orientation when placed on board top-side:

- Package Top
- +X
- +Y (up)
- +Z (dn)

Desired orientation when placed on board bottom-side:

- Top-through View
- +X (dn)
- +Y (up)
- +Z (dn)

### Sudden Motion Sensor (SMS)

- SMBUS_SMC_MGMT_SCL
- SMBUS_SMC_MGMT_SDA
- SMS_X_AXIS
- SMS_Y_AXIS
- SMS_Z_AXIS
- SMS_MOT_DIS
- SMS_MOT_EN
- SMS_X_AXIS
- SMS_ONOFF_L
- SMS_SMS_INT
- PP3V3_S3

---

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APN: 338S0354

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### DC-In Connector

- **Vref** = 3.42V * (R2a / (R1a + R2a))
- **Vth** = (Vref / (R2b / (R1b + R2b))

Assuming 1% variance for R6910-R6915 and 3.42V:

- **Worst case Vth**: min: 12.47V, max: 13.54V

**Note:** R6910 is on LID.

System must provide 10K-70K impedance to A52 adapter for system load detection.

REQ of R6910 (on LID), R6912, & R6913 is 36.9K.
100K pull-down on VR_EN per Crestline Issue #306022.
When both are low TPS51120 VIN current drops from 100-150uA to 10-20uA. EN3 can float or tie to VREG5 for automatic 3.3V LDO enable.

NOTE: EN5 can float or tie to VIN for automatic 5V LDO enable.
Vout = 0.75V * (1 + Ra / Rb)

Vout = 1.50V

8A max output

L7620 limit

NO STUFF

100PF

50V

402

5%

CERM

C7610

1

2

0.1UF

X7R603-1

10%

50V

C7615

1

2

22UF

25V

20%

POLY

C7620

1

2

2.5V

330UF

CASE-D2E-LF

20%

POLY

C7632

1

2

1/16W

MF-LF

402

1%

R7601

1 2

16V

2.2UF

10%

603X5R

C7601

1

2

200K

R7619

1

2

603X5R

C7600

1

2

1/16W

MF-LF

402

1%

200K

R7611

1

2

PWRPK-1212-8

SI7114DN

CRITICAL

Q7620

5

4

1 2 3

SI7108DNS

PWRPK-1212-8

CRITICAL

Q7625

5

4

1 2 3

SM

PLACEMENT_NOTE=Place XW7620 close to L7620.

XW7600

1 2

6.04K

MF-LF

1%

402

1/16W

R7605

1

2

603X5R

C7630

1

2

1/16W

1% 10K

402MF-LF

R7610

1

2

1/16W

MF-LF

402

10K

1%

R7611

1

2

603X5R

C7621

1

2

1.0UH-22A

IHLP2525CZ-SM

CRITICAL

L7620

1 2

SM

P530-1241

A-0-0

www.vinafix.vn
3.3V FW PHY Supply

1.95V FW PHY Supply

Vout = 1.25V * (1 + Ra / Rb)

Vout = 3.316V
200mA max output (Switcher limit)

Backup power in case of FW bus VP short to keep PHY powered.
3.425V "G3Hot" Supply

Supply needs to guarantee 3.3V delivered to PMC VCC generator

1.5V / 1.05V PWRGD Circuit

Reports when 1.5V S0 and 1.05V S0 are in regulation

Other S0 Rails PWRGD Circuit

Does not include SPM rails

NOTE: 0.9V/2.5V is not checked!

Other S0 Rails PWRGD Circuit

Does not include SPM rails
Page Notes

Signal aliases required by this page:
- =PP1V8_S0_FB_VDDQ

Power aliases required by this page:
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GDDR3 Frame Buffer A

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**PGOOD Monitor for GPU Rails**

LTC2900 provides a programmable reset delay which is required to play nice with ICHx PGOOD circuit.

Fast wake condition is worst case. ICHx can create an 82 duration of 1 sec clock (62 us). If mux select is on core well and NB-gate is implemented, glitch filter or 3.3V PGOOD assertion time is required for PGOODs to be valid at end of 95 us HBM timer. If mux select on resume well, then observed PGOOD will not change during 82 us. This allows monitor whatever PGOOD delays are provided.

NOTE: New H/W and S/W challenge since NB gfx might be powered off if using external GPU. S/W will have to determine that the entire device is in deep sleep before the NB-gate is enabled. If mux select is on core well, this could mean powering up IG supply will be necessary before going to sleep to keep PGOODs valid.

**Panel/Backlight Control Mux**

NOTE: SEL = LOW selects port B

**Mux Select Conditioning**

**GPU LVDS I/F**

**LVDS Data Mux Power Supply**

**LVDS Interface Mux**

---

**APPENDIX:**

- **Definitions:**
  - NM = Negative Monitor
  - PM = Positive Monitor
  - LB = Left Backlight
  - RB = Right Backlight
  - L = Left
  - R = Right
  - U = Upper
  - D = Lower

- **Component Specifications:**
  - **ICs:**
    - LTC2900
  - **Capacitors:**
    - 0.1μF
  - **Resistors:**
    - 220kΩ
  - **Inductors:**
    - 121μH
  - **Diodes:**
    - 1N4148
  - **Transistors:**
    - 2N7002DW-X-F

- **Notes:**
  - Make sure to check the component placement and orientation on the PCB.
  - Verify all connections and soldering are secure.
  - Ensure proper ground connections to prevent noise and interference.

---

**Drawing Number:**

- **DATE:**
  - 03/19/2007

---

**Website:**

- www.vinafix.vn
### CPU Signal Constraints

<table>
<thead>
<tr>
<th>CPU Net</th>
<th>Line-to-Line Spacing</th>
<th>Layer</th>
<th>Min Neck Width</th>
<th>Max Neck Length</th>
<th>Physical Rule Set</th>
</tr>
</thead>
<tbody>
<tr>
<td>FSB_DATA</td>
<td>25 Mil</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FSB_DATA2DSTB</td>
<td>25 Mil</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FSB_DSTB_55S</td>
<td>25 Mil</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FSB_55S</td>
<td>25 Mil</td>
<td></td>
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<td></td>
</tr>
</tbody>
</table>

**NOTES:**
- Design Guide recommends at least 25 mils, >50 mils preferred.
- CPU nets require 25 mils spacing to other nets.
- CPU VCCSENSE requires 25 mils to other nets.

### CPU / FSB Net Properties

<table>
<thead>
<tr>
<th>Net Type</th>
<th>Description</th>
<th>Width</th>
<th>Height</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU_VCCSENSE</td>
<td>Power voltage sense pin</td>
<td>88</td>
<td>46</td>
</tr>
<tr>
<td>FSB_DSTB_55S</td>
<td>Data strobe bus 55-ohm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>FSB_55S</td>
<td>Data bus 55-ohm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CPU_COMP</td>
<td>CPU core output</td>
<td>11</td>
<td></td>
</tr>
<tr>
<td>CPU_FROM_SB</td>
<td>CPU core output</td>
<td>11</td>
<td></td>
</tr>
<tr>
<td>NB_BSEL&lt;1&gt;</td>
<td>Bus select output</td>
<td></td>
<td></td>
</tr>
<tr>
<td>XDP_BPM_L</td>
<td>Clock output</td>
<td>13</td>
<td></td>
</tr>
<tr>
<td>XDP_TRST_L</td>
<td>Reset output</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>XDP_CLK_P</td>
<td>Clock output</td>
<td>14</td>
<td></td>
</tr>
<tr>
<td>CPU_ITP</td>
<td>Input pin</td>
<td>14</td>
<td></td>
</tr>
<tr>
<td>CPU_PWRGD</td>
<td>Power good pin</td>
<td>14</td>
<td></td>
</tr>
<tr>
<td>CPU_PROCHOT_L</td>
<td>Prochot output</td>
<td>14</td>
<td></td>
</tr>
<tr>
<td>CPU_FROM_SB</td>
<td>CPU core output</td>
<td>11</td>
<td></td>
</tr>
<tr>
<td>CPU_DPSLP_L</td>
<td>DPSLP output</td>
<td>11</td>
<td></td>
</tr>
<tr>
<td>CPU_NMI</td>
<td>NMI output</td>
<td>14</td>
<td></td>
</tr>
<tr>
<td>CPU_GTLREF</td>
<td>GTLREF output</td>
<td>14</td>
<td></td>
</tr>
<tr>
<td>CPU_STPCLK_L</td>
<td>STPCLK output</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>CPU_FROM_SB</td>
<td>CPU core output</td>
<td>11</td>
<td></td>
</tr>
<tr>
<td>CPU_DPSLP_L</td>
<td>DPSLP output</td>
<td>11</td>
<td></td>
</tr>
<tr>
<td>CPU_NMI</td>
<td>NMI output</td>
<td>14</td>
<td></td>
</tr>
<tr>
<td>CPU_GTLREF</td>
<td>GTLREF output</td>
<td>14</td>
<td></td>
</tr>
<tr>
<td>CPU_STPCLK_L</td>
<td>STPCLK output</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>CPU_FROM_SB</td>
<td>CPU core output</td>
<td>11</td>
<td></td>
</tr>
<tr>
<td>CPU_DPSLP_L</td>
<td>DPSLP output</td>
<td>11</td>
<td></td>
</tr>
<tr>
<td>CPU_NMI</td>
<td>NMI output</td>
<td>14</td>
<td></td>
</tr>
<tr>
<td>CPU_GTLREF</td>
<td>GTLREF output</td>
<td>14</td>
<td></td>
</tr>
<tr>
<td>CPU_STPCLK_L</td>
<td>STPCLK output</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>CPU_FROM_SB</td>
<td>CPU core output</td>
<td>11</td>
<td></td>
</tr>
<tr>
<td>CPU_DPSLP_L</td>
<td>DPSLP output</td>
<td>11</td>
<td></td>
</tr>
<tr>
<td>CPU_NMI</td>
<td>NMI output</td>
<td>14</td>
<td></td>
</tr>
<tr>
<td>CPU_GTLREF</td>
<td>GTLREF output</td>
<td>14</td>
<td></td>
</tr>
<tr>
<td>CPU_STPCLK_L</td>
<td>STPCLK output</td>
<td>10</td>
<td></td>
</tr>
</tbody>
</table>

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### CPU / FSB Constraints

<table>
<thead>
<tr>
<th>Net Type</th>
<th>Description</th>
<th>Width</th>
<th>Height</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU_VCCSENSE</td>
<td>Power voltage sense pin</td>
<td>88</td>
<td>46</td>
</tr>
<tr>
<td>FSB_DSTB_55S</td>
<td>Data strobe bus 55-ohm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>FSB_55S</td>
<td>Data bus 55-ohm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CPU_COMP</td>
<td>CPU core output</td>
<td>11</td>
<td></td>
</tr>
<tr>
<td>CPU_FROM_SB</td>
<td>CPU core output</td>
<td>11</td>
<td></td>
</tr>
<tr>
<td>NB_BSEL&lt;1&gt;</td>
<td>Bus select output</td>
<td></td>
<td></td>
</tr>
<tr>
<td>XDP_BPM_L</td>
<td>Clock output</td>
<td>13</td>
<td></td>
</tr>
<tr>
<td>XDP_TRST_L</td>
<td>Reset output</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>XDP_CLK_P</td>
<td>Clock output</td>
<td>14</td>
<td></td>
</tr>
<tr>
<td>CPU_ITP</td>
<td>Input pin</td>
<td>14</td>
<td></td>
</tr>
<tr>
<td>CPU_PWRGD</td>
<td>Power good pin</td>
<td>14</td>
<td></td>
</tr>
<tr>
<td>CPU_PROCHOT_L</td>
<td>Prochot output</td>
<td>14</td>
<td></td>
</tr>
<tr>
<td>CPU_FROM_SB</td>
<td>CPU core output</td>
<td>11</td>
<td></td>
</tr>
<tr>
<td>CPU_DPSLP_L</td>
<td>DPSLP output</td>
<td>11</td>
<td></td>
</tr>
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<td>14</td>
<td></td>
</tr>
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<td>14</td>
<td></td>
</tr>
<tr>
<td>CPU_STPCLK_L</td>
<td>STPCLK output</td>
<td>10</td>
<td></td>
</tr>
<tr>
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<td>CPU core output</td>
<td>11</td>
<td></td>
</tr>
<tr>
<td>CPU_DPSLP_L</td>
<td>DPSLP output</td>
<td>11</td>
<td></td>
</tr>
<tr>
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<td>NMI output</td>
<td>14</td>
<td></td>
</tr>
<tr>
<td>CPU_GTLREF</td>
<td>GTLREF output</td>
<td>14</td>
<td></td>
</tr>
<tr>
<td>CPU_STPCLK_L</td>
<td>STPCLK output</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>CPU_FROM_SB</td>
<td>CPU core output</td>
<td>11</td>
<td></td>
</tr>
<tr>
<td>CPU_DPSLP_L</td>
<td>DPSLP output</td>
<td>11</td>
<td></td>
</tr>
<tr>
<td>CPU_NMI</td>
<td>NMI output</td>
<td>14</td>
<td></td>
</tr>
<tr>
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<td>GTLREF output</td>
<td>14</td>
<td></td>
</tr>
<tr>
<td>CPU_STPCLK_L</td>
<td>STPCLK output</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>CPU_FROM_SB</td>
<td>CPU core output</td>
<td>11</td>
<td></td>
</tr>
<tr>
<td>CPU_DPSLP_L</td>
<td>DPSLP output</td>
<td>11</td>
<td></td>
</tr>
<tr>
<td>CPU_NMI</td>
<td>NMI output</td>
<td>14</td>
<td></td>
</tr>
<tr>
<td>CPU_GTLREF</td>
<td>GTLREF output</td>
<td>14</td>
<td></td>
</tr>
<tr>
<td>CPU_STPCLK_L</td>
<td>STPCLK output</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>CPU_FROM_SB</td>
<td>CPU core output</td>
<td>11</td>
<td></td>
</tr>
<tr>
<td>CPU_DPSLP_L</td>
<td>DPSLP output</td>
<td>11</td>
<td></td>
</tr>
<tr>
<td>CPU_NMI</td>
<td>NMI output</td>
<td>14</td>
<td></td>
</tr>
<tr>
<td>CPU_GTLREF</td>
<td>GTLREF output</td>
<td>14</td>
<td></td>
</tr>
<tr>
<td>CPU_STPCLK_L</td>
<td>STPCLK output</td>
<td>10</td>
<td></td>
</tr>
</tbody>
</table>

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### Memory Net Properties

<table>
<thead>
<tr>
<th>Name</th>
<th>Symbol</th>
<th>Reference</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>MEM_A_DQ_BYTE4</td>
<td>MEM_DQ</td>
<td>MEM_DATAMEM_55S</td>
<td></td>
</tr>
<tr>
<td>MEM_B_DQS7</td>
<td>MEM_DQS</td>
<td>MEM_85D</td>
<td></td>
</tr>
<tr>
<td>MEM_B_DQS3</td>
<td>MEM_DQS</td>
<td>MEM_85D</td>
<td></td>
</tr>
<tr>
<td>MEM_B_DQS2</td>
<td>MEM_DQS</td>
<td>MEM_85D</td>
<td></td>
</tr>
<tr>
<td>MEM_B_DQS0</td>
<td>MEM_DQS</td>
<td>MEM_85D</td>
<td></td>
</tr>
<tr>
<td>MEM_B_DM7</td>
<td>MEM_DATA</td>
<td>MEM_DATAMEM_55S</td>
<td></td>
</tr>
<tr>
<td>MEM_B_DM0</td>
<td>MEM_DATA</td>
<td>MEM_55S</td>
<td></td>
</tr>
<tr>
<td>MEM_B_DQ_BYTE7</td>
<td>MEM_DQS</td>
<td>MEM_DATAMEM_55S</td>
<td></td>
</tr>
<tr>
<td>MEM_B_DQ_BYTE1</td>
<td>MEM_DATA</td>
<td>MEM_DATAMEM_55S</td>
<td></td>
</tr>
<tr>
<td>MEM_B_WE_L</td>
<td>MEM_DATA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_B_RAS_L</td>
<td>MEM_DATA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_B_CMD</td>
<td>MEM_DATA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_B_CNTL</td>
<td>MEM_DATA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_A_DQ_BYTE4</td>
<td>MEM_DQ</td>
<td>MEM_DATAMEM_55S</td>
<td></td>
</tr>
<tr>
<td>MEM_A_DQ6</td>
<td>MEM_DQS</td>
<td>MEM_55S</td>
<td></td>
</tr>
<tr>
<td>MEM_A_DQ4</td>
<td>MEM_DQS</td>
<td>MEM_55S</td>
<td></td>
</tr>
<tr>
<td>MEM_A_DQ_P&lt;0&gt;</td>
<td>MEM_A_DQ</td>
<td>MEM_DATAMEM_55S</td>
<td></td>
</tr>
<tr>
<td>MEM_A_DM6</td>
<td>MEM_DATA</td>
<td>MEM_DATAMEM_55S</td>
<td></td>
</tr>
<tr>
<td>MEM_A_DM3</td>
<td>MEM_DATA</td>
<td>MEM_DATAMEM_55S</td>
<td></td>
</tr>
<tr>
<td>MEM_A_DM2</td>
<td>MEM_DATA</td>
<td>MEM_DATAMEM_55S</td>
<td></td>
</tr>
<tr>
<td>MEM_A_DQ_BYTE2</td>
<td>MEM_DATA</td>
<td>MEM_DATAMEM_55S</td>
<td></td>
</tr>
<tr>
<td>MEM_A_DQ_BYTE1</td>
<td>MEM_DATA</td>
<td>MEM_DATAMEM_55S</td>
<td></td>
</tr>
<tr>
<td>MEM_A_CMD</td>
<td>MEM_DATA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_A_CNTL</td>
<td>MEM_DATA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_A_CNTL</td>
<td>MEM_DATA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_CLK_P&lt;2..0&gt;</td>
<td>MEM_CLK</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_A_CAS_L</td>
<td>MEM_DATA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_85D MEM_DQS</td>
<td>MEM_85D</td>
<td>MEM_DQS</td>
<td></td>
</tr>
<tr>
<td>MEM_85D MEM_DQS</td>
<td>MEM_85D</td>
<td>MEM_DQS</td>
<td></td>
</tr>
<tr>
<td>MEM_85D MEM_DQS</td>
<td>MEM_85D</td>
<td>MEM_DQS</td>
<td></td>
</tr>
<tr>
<td>MEM_85D MEM_DQS</td>
<td>MEM_85D</td>
<td>MEM_DQS</td>
<td></td>
</tr>
<tr>
<td>MEM_85D MEM_DQSMEM_A_DQS1</td>
<td>MEM_85D</td>
<td>MEM_DQS</td>
<td></td>
</tr>
<tr>
<td>MEM_A_DQS1</td>
<td>MEM_DATA</td>
<td>MEM_DATAMEM_55S</td>
<td></td>
</tr>
<tr>
<td>MEM_A_DQS0</td>
<td>MEM_DATA</td>
<td>MEM_DATAMEM_55S</td>
<td></td>
</tr>
<tr>
<td>MEM_A_DQS1</td>
<td>MEM_DATA</td>
<td>MEM_DATAMEM_55S</td>
<td></td>
</tr>
<tr>
<td>MEM_A_DQS0</td>
<td>MEM_DATA</td>
<td>MEM_DATAMEM_55S</td>
<td></td>
</tr>
<tr>
<td>MEM_A_DQS_N&lt;5&gt;</td>
<td>MEM_DATA</td>
<td>MEM_DATAMEM_55S</td>
<td></td>
</tr>
<tr>
<td>MEM_A_DQS_P&lt;5&gt;</td>
<td>MEM_DATA</td>
<td>MEM_DATAMEM_55S</td>
<td></td>
</tr>
<tr>
<td>MEM_A_DQS_N&lt;4&gt;</td>
<td>MEM_DATA</td>
<td>MEM_DATAMEM_55S</td>
<td></td>
</tr>
<tr>
<td>MEM_A_DQS_P&lt;4&gt;</td>
<td>MEM_DATA</td>
<td>MEM_DATAMEM_55S</td>
<td></td>
</tr>
<tr>
<td>MEM_A_DQS_N&lt;3&gt;</td>
<td>MEM_DATA</td>
<td>MEM_DATAMEM_55S</td>
<td></td>
</tr>
<tr>
<td>MEM_85D MEM_DQSMEM_A_DQS0</td>
<td>MEM_85D</td>
<td>MEM_DQS</td>
<td></td>
</tr>
<tr>
<td>MEM_A_DQS0</td>
<td>MEM_DATA</td>
<td>MEM_DATAMEM_55S</td>
<td></td>
</tr>
<tr>
<td>MEM_A_CNTL</td>
<td>MEM_DATA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_A_CNTL</td>
<td>MEM_DATA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_CLK_P&lt;2..0&gt;</td>
<td>MEM_CLK</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_A_CNTL</td>
<td>MEM_DATA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_A_CNTL</td>
<td>MEM_DATA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_A_CNTL</td>
<td>MEM_DATA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_CLK_P&lt;2..0&gt;</td>
<td>MEM_CLK</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_A_CNTL</td>
<td>MEM_DATA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_A_CNTL</td>
<td>MEM_DATA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_A_CNTL</td>
<td>MEM_DATA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_CLK_P&lt;2..0&gt;</td>
<td>MEM_CLK</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_A_CNTL</td>
<td>MEM_DATA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_A_CNTL</td>
<td>MEM_DATA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_A_CNTL</td>
<td>MEM_DATA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_CLK_P&lt;2..0&gt;</td>
<td>MEM_CLK</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_A_CNTL</td>
<td>MEM_DATA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_A_CNTL</td>
<td>MEM_DATA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_A_CNTL</td>
<td>MEM_DATA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_CLK_P&lt;2..0&gt;</td>
<td>MEM_CLK</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Source:** Santa Rosa Platform Design Guide 1.0 (December 2006), Section 4.2
### Disk Interface Constraints

<table>
<thead>
<tr>
<th>Source</th>
<th>Constraint</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.7 &amp; 10.9</td>
<td>Disk Interface</td>
<td>Constraints</td>
</tr>
</tbody>
</table>

### HD Audio Interface Constraints

<table>
<thead>
<tr>
<th>Source</th>
<th>Constraint</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>Napa Platform DG, Rev 0.9 (#17978), Section 10.9.1</td>
<td>HD Audio Interface</td>
<td>Constraints</td>
</tr>
</tbody>
</table>

### USB 2.0 Interface Constraints

<table>
<thead>
<tr>
<th>Source</th>
<th>Constraint</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>USB 2.0 Interface Constraints</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
PCI Bus Constraints

Controller Link (AMT) Constraints

Ethernet (Yukon) Constraints

SB Constraints (2 of 2)
Clock Signal Constraints

Clock Net Properties

SMC SMBus Net Properties

Clock & SMC Constraints

SOURCE: Santa Rosa Platform DD, Rev 1.0 ($21112), Sections 14.1 - 14.6
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Port 2 Not Used

FireWire Net Properties

<table>
<thead>
<tr>
<th>Port</th>
<th>Net</th>
<th>Rf</th>
<th>Freq</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Port 0 TPA</td>
<td>FW_PORT0_TPA_N</td>
<td>110_OHM_DIFF</td>
<td>FW_LKON</td>
<td>FW_PHY_CLK98P304M_XI</td>
</tr>
<tr>
<td>Port 1 TPA</td>
<td>FW_PORT1_TPA_P</td>
<td>110_OHM_DIFF</td>
<td>FW_LKON</td>
<td>FW_PHY_CLK98P304M_XI</td>
</tr>
<tr>
<td>Port 0 TPB</td>
<td>FW_PORT0_TPB_P</td>
<td>110_OHM_DIFF</td>
<td>FW_LKON</td>
<td>FW_PHY_CLK98P304M_XI</td>
</tr>
<tr>
<td>Port 1 TPB</td>
<td>FW_PORT1_TPB_N</td>
<td>110_OHM_DIFF</td>
<td>FW_LKON</td>
<td>FW_PHY_CLK98P304M_XI</td>
</tr>
</tbody>
</table>

FireWire Interface Constraints

<table>
<thead>
<tr>
<th>Port</th>
<th>Net</th>
<th>Min Width</th>
<th>Max Length</th>
<th>Gap Width</th>
</tr>
</thead>
<tbody>
<tr>
<td>Port 0 TPA</td>
<td>FW_PORT0_TPA_P</td>
<td>110_OHM_DIFF</td>
<td>110_OHM_DIFF</td>
<td>110_OHM_DIFF</td>
</tr>
<tr>
<td>Port 1 TPA</td>
<td>FW_PORT1_TPA_N</td>
<td>110_OHM_DIFF</td>
<td>110_OHM_DIFF</td>
<td>110_OHM_DIFF</td>
</tr>
</tbody>
</table>

Sync Date: 01/25/2007
Sync Master: T9_NOME

WWW.VINAFIX.VN
### GDDR3 Frame Buffer Signal Constraints

<table>
<thead>
<tr>
<th>Net Type</th>
<th>Min Width</th>
<th>Max Length</th>
<th>Min Gap</th>
<th>Gap Spacing</th>
</tr>
</thead>
<tbody>
<tr>
<td>GDDR3_50SE</td>
<td>*50_OHM_SE</td>
<td>*20_MIL</td>
<td>*2.5:1_SPACING</td>
<td></td>
</tr>
<tr>
<td>GDDR3_CMD</td>
<td>100_OHM_DIFF</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VGA_SYNC</td>
<td>STANDARD</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Video Signal Constraints

<table>
<thead>
<tr>
<th>Net Type</th>
<th>Min Width</th>
<th>Max Length</th>
<th>Min Gap</th>
<th>Gap Spacing</th>
</tr>
</thead>
<tbody>
<tr>
<td>TMDS</td>
<td>12.7 MM</td>
<td>*50_OHM_SE</td>
<td>12.7 MM</td>
<td></td>
</tr>
</tbody>
</table>

### GDDR3 FB A/B Net Properties

<table>
<thead>
<tr>
<th>Net Type</th>
<th>Min Width</th>
<th>Max Length</th>
<th>Min Gap</th>
<th>Gap Spacing</th>
</tr>
</thead>
<tbody>
<tr>
<td>FB_A_DQ&lt;15..8&gt;</td>
<td>12.7 MM</td>
<td>12.7 MM</td>
<td>12.7 MM</td>
<td></td>
</tr>
<tr>
<td>FB_A_DQ&lt;7..0&gt;</td>
<td>12.7 MM</td>
<td>12.7 MM</td>
<td>12.7 MM</td>
<td></td>
</tr>
<tr>
<td>FB_A_RDQS&lt;3&gt;</td>
<td>12.7 MM</td>
<td>12.7 MM</td>
<td>12.7 MM</td>
<td></td>
</tr>
<tr>
<td>FB_A_WDQS&lt;2&gt;</td>
<td>12.7 MM</td>
<td>12.7 MM</td>
<td>12.7 MM</td>
<td></td>
</tr>
<tr>
<td>FB_A_CK</td>
<td>12.7 MM</td>
<td>12.7 MM</td>
<td>12.7 MM</td>
<td></td>
</tr>
<tr>
<td>FB_A_WE_L</td>
<td>12.7 MM</td>
<td>12.7 MM</td>
<td>12.7 MM</td>
<td></td>
</tr>
</tbody>
</table>

### GDDR3 FB C/D Net Properties

<table>
<thead>
<tr>
<th>Net Type</th>
<th>Min Width</th>
<th>Max Length</th>
<th>Min Gap</th>
<th>Gap Spacing</th>
</tr>
</thead>
<tbody>
<tr>
<td>FB_C_DQ&lt;63..56&gt;</td>
<td>12.7 MM</td>
<td>12.7 MM</td>
<td>12.7 MM</td>
<td></td>
</tr>
<tr>
<td>FB_C_DQ&lt;55..48&gt;</td>
<td>12.7 MM</td>
<td>12.7 MM</td>
<td>12.7 MM</td>
<td></td>
</tr>
<tr>
<td>FB_C_DQ&lt;39..32&gt;</td>
<td>12.7 MM</td>
<td>12.7 MM</td>
<td>12.7 MM</td>
<td></td>
</tr>
</tbody>
</table>

### G84M Net Properties

<table>
<thead>
<tr>
<th>Net Type</th>
<th>Min Width</th>
<th>Max Length</th>
<th>Min Gap</th>
<th>Gap Spacing</th>
</tr>
</thead>
<tbody>
<tr>
<td>GDDR3_FB_C/D</td>
<td>12.7 MM</td>
<td>12.7 MM</td>
<td>12.7 MM</td>
<td></td>
</tr>
<tr>
<td>GDDR3_FB_A/B</td>
<td>12.7 MM</td>
<td>12.7 MM</td>
<td>12.7 MM</td>
<td></td>
</tr>
</tbody>
</table>

### GPU (G84M) Constraints

<table>
<thead>
<tr>
<th>Constraint Type</th>
<th>Min Width</th>
<th>Max Length</th>
<th>Min Gap</th>
<th>Gap Spacing</th>
</tr>
</thead>
<tbody>
<tr>
<td>GDDR3_FB_C/D</td>
<td>12.7 MM</td>
<td>12.7 MM</td>
<td>12.7 MM</td>
<td></td>
</tr>
<tr>
<td>GDDR3_FB_A/B</td>
<td>12.7 MM</td>
<td>12.7 MM</td>
<td>12.7 MM</td>
<td></td>
</tr>
</tbody>
</table>

---

**NOT TO REVEAL OR PUBLISH IN WHOLE OR PART**

**TO MAINTAIN THE DOCUMENT IN CONFIDENCE**

**PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR**
**Graphics Constraint Relaxations**

Allow 0.1 mm necks for >0.1 mm lines between thru-hole SO-DIMM pins.

**Memory Constraint Relaxations**

=1:1_DIFFPAIR

THERM_1TO1_55S

SENSE_1TO1_55S

=55_OHM_SE*

=55_OHM_SE

**SIM Card Constraints**

GND_P2MM 0.20 MM

MEM_70D BOTTOM 6.35 MM

MEM_45S 0.100 MM 2.54 MM

| OVERRIDE OVERRIDE OVERRIDE OVERRIDE OVERRIDE OVERRIDE OVERRIDE OVERRIDE |

MEM_CLK

GND

PWR_P2MM

*USB

**ISL4, ISL10**

0.100 MM 2.54 MM

MEM_85D

**LAYER MINIMUM NECK WIDTH MAXIMUM NECK LENGTH DIFFPAIR PRIMARY GAP DIFFPAIR NECK GAP PHYSICAL_RULE_SET**

*WWAN_SIM*

=2:1_SPACING

*SENSE*

=50_OHM_SE

**TABLE PHYSICAL_ASSIGNMENT_ITEM**

**TABLE PHYSICAL_ASSIGNMENT_HEAD**

**TABLE PHYSICAL_RULE_ITEM**

**TABLE PHYSICAL_RULE_HEAD**

**TABLE PHYSICAL_RULE_SET AREA_TYPENET_PHYSICAL_TYPE**

**TABLE PHYSICAL_RULE_SET AREA_TYPENET_PHYSICAL_TYPE**

**ELECTRICAL_CONSTRAINT_SET PHYSICAL SPACING**

I118

(USB_CAMERA)

(VGA_SYNC)

(VGA_R_TV_Y)

(USB_EXTA)

(USB_EXTD)

(PCIE_MINI)

(PCIE_EXCARD)

(VGA_55S)

(TMDS_100D)

(TMDS_CLK_R_N)

(LVDS_100D)

(LVDS_100D)

(LVDS_100D)

(LVDS_100D)

(LVDS_100D)

(RSFSTHMSNS_D_P)

(THERM_1TO1_55S)

(REMTHMSNS_DX_P)

(THERM_1TO1_55S)

(SENSE_1TO1_55S)

(CPU_THERMD_P)

(CPUTHMSNS_D2_P)

(USB_CAMERA_F_P)

(USB_90D)

(USB2_RT_N)

(SATA_A_R2D_UF_P)

(FW_110D)

(FW_PORT0_TPA_FL_P)

(ENET_100D)

(ENET_CONN)

(ENET_MDI_R_N<3..0>)

(PCIE_100D)

(THERM_1TO1_55S)

(SENSE_1TO1_55S)

(P1V25ISNS_P)

(P1V8ISNS_P)

(THERM_DIFFPAIR)

(SENSE_DIFFPAIR)

(USB_90D)

(USB_90D)

(USB_90D)

(USB_90D)

(SATASATA_100D)

(SATASATA_100D)

(SATASATA_100D)

(FW_PORT0_TPA_FL_N)

(FW_TP)

(PCIE)

(PCIE)

(PCIE_EXCARD_R2D_N)

(PCIE_EXCARD_R2D_P)

(ENET_MDI)

(ENET_100D)

(PCIE)

(PCIE_EXCARD_R2D_N)

(PCIE_EXCARD_R2D_P)

(ENET_MDI)

(ENET_100D)

(PCIE)

(ENET)

(ENET_100D)

(ENETCONN)

(ENET_MDI_R_N<3..0>)

(PCIE)

(PCIE)

(PCIE_EXCARD_R2D_N)

(PCIE_EXCARD_R2D_P)

(ENET_MDI)

(ENET_100D)

(PCIE)

(ENET)

(ENET_100D)

(ENETCONN)

(ENET_MDI_R_N<3..0>)

(PCIE)

(PCIE)

(PCIE_EXCARD_R2D_N)

(PCIE_EXCARD_R2D_P)

(ENET_MDI)

(ENET_100D)

(PCIE)

(ENET)

(ENET_100D)

(ENETCONN)

(ENET_MDI_R_N<3..0>)

(PCIE)

(PCIE)

(PCIE_EXCARD_R2D_N)

(PCIE_EXCARD_R2D_P)

(ENET_MDI)

(ENET_100D)

(PCIE)

(ENET)

(ENET_100D)

(ENETCONN)

(ENET_MDI_R_N<3..0>)

(PCIE)

(PCIE)

(PCIE_EXCARD_R2D_N)

(PCIE_EXCARD_R2D_P)

(ENET_MDI)

(ENET_100D)

(PCIE)

(ENET)

(ENET_100D)

(ENETCONN)

(ENET_MDI_R_N<3..0>)

(PCIE)

(PCIE)

(PCIE_EXCARD_R2D_N)

(PCIE_EXCARD_R2D_P)

(ENET_MDI)

(ENET_100D)

(PCIE)

(ENET)

(ENET_100D)

(ENETCONN)

(ENET_MDI_R_N<3..0>)

(PCIE)

(PCIE)

(PCIE_EXCARD_R2D_N)

(PCIE_EXCARD_R2D_P)

(ENET_MDI)

(ENET_100D)

(PCIE)

(ENET)

(ENET_100D)

(ENETCONN)

(ENET_MDI_R_N<3..0>)

(PCIE)

(PCIE)

(PCIE_EXCARD_R2D_N)

(PCIE_EXCARD_R2D_P)

(ENET_MDI)

(ENET_100D)

(PCIE)

(ENET)

(ENET_100D)

(ENETCONN)

(ENET_MDI_R_N<3..0>)

(PCIE)

(PCIE)

(PCIE_EXCARD_R2D_N)

(PCIE_EXCARD_R2D_P)

(ENET_MDI)

(ENET_100D)

(PCIE)

(ENET)

(ENET_100D)

(ENETCONN)

(ENET_MDI_R_N<3..0>)

(PCIE)

(PCIE)

(PCIE_EXCARD_R2D_N)

(PCIE_EXCARD_R2D_P)

(ENET_MDI)

(ENET_100D)

(PCIE)

(ENET)

(ENET_100D)

(ENETCONN)

(ENET_MDI_R_N<3..0>)

(PCIE)

(PCIE)

(PCIE_EXCARD_R2D_N)

(PCIE_EXCARD_R2D_P)

(ENET_MDI)

(ENET_100D)

(PCIE)

(ENET)

(ENET_100D)

(ENETCONN)

(ENET_MDI_R_N<3..0>)

(PCIE)

(PCIE)

(PCIE_EXCARD_R2D_N)

(PCIE_EXCARD_R2D_P)

(ENET_MDI)

(ENET_100D)

(PCIE)

(ENET)

(ENET_100D)

(ENETCONNECT)
### M75/M76 Board-Specific Spacing & Physical Constraints

<table>
<thead>
<tr>
<th>MINIMUM LINE WIDTH</th>
<th>ALLOW ROUTE</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.089 MM</td>
<td>=STANDARD</td>
</tr>
<tr>
<td>0.099 MM</td>
<td>=STANDARD</td>
</tr>
<tr>
<td>0.102 MM</td>
<td>90_OHM_DIFF</td>
</tr>
<tr>
<td>0.125 MM</td>
<td>=STANDARD</td>
</tr>
<tr>
<td>0.125 MM</td>
<td>=STANDARD</td>
</tr>
<tr>
<td>0.140 MM</td>
<td>=STANDARD</td>
</tr>
<tr>
<td>0.140 MM</td>
<td>=STANDARD</td>
</tr>
<tr>
<td>0.330 MM</td>
<td>=STANDARD</td>
</tr>
<tr>
<td>0.330 MM</td>
<td>=STANDARD</td>
</tr>
<tr>
<td>0.220 MM</td>
<td>=STANDARD</td>
</tr>
</tbody>
</table>

**Default width/spacing is 100-ohm differential, but pairs can neck to 95-ohms without DRC.**

**Note:**

- **100_OHM_DIFF** is for select 100-ohm differential pairs with switch difficulties through 40:1 spacing.
- **70_OHM_DIFF** is for select 70-ohm differential pairs with switch difficulties through 40:1 spacing.
- **55_OHM_SE** is for select 55-ohm single-ended pairs with switch difficulties through 40:1 spacing.

---

**Version:**

- **ALLEGRO (MIL or MM)**
- **BOARD UNITS**: BOARD LAYERS BOARD AREAS

**Table:**

<table>
<thead>
<tr>
<th>TABLE_PHYSICAL_RULE_ITEM</th>
<th>TABLE_PHYSICAL_RULE_ITEM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Version</td>
<td>Version</td>
</tr>
<tr>
<td>APPLE COMPUTER INC.</td>
<td>APPLE COMPUTER INC.</td>
</tr>
<tr>
<td>051-7261 A.0.0</td>
<td>051-7261 A.0.0</td>
</tr>
</tbody>
</table>

**Technical Notes:**

- **OFSHT**
- **REV.**

---

**Default width/spacing is 100-ohm differential, but pairs can neck to 95-ohms without DRC.**