PAGE CONTENTS

1 TITLE PAGE AND CONTENTS
2 SYSTEM BLOCK DIAGRAM
3 POWER BLOCK DIAGRAM
4 PCB NOTES AND HOLES
5 MPC7447A MAXBUS INTERFACE
6 MPC7447A DATA / NC PINS / BOOTSTRAP
7 CPU PLL AND CONFIGURATION STRAPS
8 INTREPID MAXBUS AND BOOT STRAPS
9 INTREPID MEMORY INTERFACE / BOOT ROM
10 DDR MEMORY MIXERS
11 400PIN STACKED DDR SODIMM CONNECTOR
12 INTREPID AGP 4X/PCI
13 INTREPID ENET/FW/UEATA/EIDE INTERFACES
14 INTREPID GPIO/SERIAL/USB INTERFACES/SSCG
15 INTREPID POWER RAILS/1.5V LOO
16 INTREPID DECOUPLING
17 USB 2.0 INTERFACE (uPD720101)
18 CARDBUS INTERFACE (PCI11510)
19 M11 AGP INTERFACE & SPREAD SPECTRUM SUPPORT
20 M11 LVDS/TMDS/GPIO & GPU VCORE
21 M11 POWER

PAGE CONTENTS

22 VIDEO CONNECTORS - INVERTER, DVI, S-VIDEO, LVDS
23 KB,TPAD,HALL EFFECT,PWR BUTTON,LM/Sensor
24 INTERNAL CONNECTORS - AIRPORT, HARD DRIVE, OPTICAL DRIVE
25 FAN CONTROLLER, USB MODEM/SOFT MODEM, BOUND/LEFT USB/BLUE TOOTH, SERIAL/org DEBUG
26 GIGABIT ETHERNET INTERFACE
27 FIREWIRE PHY
28 FIREWIRE PORTS
29 PMU
30 BATTERY CHARGER AND CONNECTOR
31 PBUS SUPPLY / PMU SUPPLY / BACKUP BATTERY
32 3.3V / 5V SYSTEM POWER SUPPLY
33 CPU CORE VOLTAGE POWER SUPPLY
34 1.5V/ 1.8V / 2.5V SYSTEM POWER SUPPLIES
35 SIGNAL CONSTRAINTS (1 OF 4) - DDR MEM/CLK
36 SIGNAL CONSTRAINTS (2 OF 4) - CPU
37 SIGNAL CONSTRAINTS (3 OF 4) - DIGITAL/DIFF
38 SIGNAL CONSTRAINTS (4 OF 4) - POWER NETS
39 FUNCTIONAL TESTPOINTS
40 REVISION HISTORY
41 SIGNAL LOCATIONS
42 COMPONENT LOCATIONS (1 OF 2)
43 COMPONENT LOCATIONS (2 OF 2)
PCB SPECS

THICKNESS: 1.2 MM / 0.047 IN
1/2 OZ CU THICKNESS: 0.7 MILS
1.0 OZ CU THICKNESS: 1.4 MILS

IMPEDANCE: 50 OHMS +/- 10%
DIELECTRIC: FR-4
LAYER COUNT: 10

SIGNAL TRACE WIDTH: 4 MILS
SIGNAL TRACE SPACING: 2-3 MILS

SEE PCB CAD FILES FOR MORE SPECIFIC INFO.

BOARD STACK-UP AND CONSTRUCTION

<table>
<thead>
<tr>
<th>Layer</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Prepreg (3 MIL)</td>
</tr>
<tr>
<td>2</td>
<td>Prepreg (3 MIL)</td>
</tr>
<tr>
<td>3</td>
<td>Core (3 MIL)</td>
</tr>
<tr>
<td>4</td>
<td>Prepreg (5 MIL)</td>
</tr>
<tr>
<td>5</td>
<td>Core (5 MIL)</td>
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<tr>
<td>6</td>
<td>Prepreg (5 MIL)</td>
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<tr>
<td>7</td>
<td>Core (3 MIL)</td>
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<tr>
<td>8</td>
<td>Prepreg (3 MIL)</td>
</tr>
<tr>
<td>9</td>
<td>Prepreg (3 MIL)</td>
</tr>
<tr>
<td>10</td>
<td>Prepreg (3 MIL)</td>
</tr>
</tbody>
</table>

SIGNAL (1/2 OZ)
PREPREG (3 MIL)
CORE (3 MIL)
PREPREG (5 MIL)
PREPREG (3 MIL)
PREPREG (5 MIL)

THICKNESS: 1.2 MM / 0.047 IN
1.0 OZ CU THICKNESS: 1.4 MILS
1/2 OZ CU THICKNESS: 0.7 MILS

PREPREG THICKNESS: 2-3 MILS
SIGNAL TRACE SPACING: 4 MILS
SIGNAL TRACE WIDTH: 4 MILS

DIELECTRIC: FR-4
IMPEDANCE: 50 OHMS +/- 10%

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D 051-6570 B
4/44
INTREPID BOOT STRAPS

BIT 32 TO 39

BIT 40 TO 47

BIT 48 TO 55

MAX BUS PULL-UPS

INTREPID BOOT STRAPS

BIT 56 TO 63

Intrepid MaxBus
SEL = LOW; HOST = B PORT; A PORT = 100OHM TO GND
SEL = HIGH; HOST = A PORT; B PORT = 100OHM TO GND
ASLEEP ON BATTERY (SAVES POWER)

PLACE ALL SERIES RES CLOSE TO PHY

PLACE CAPS (IN ORDER) ON PINS 32/35, 36/40, 45 & 78

R2EQV = R2A||R2B

PLACE RESISTORS CLOSE TO PH

MARVELL 88E1111
10/100/1000 ETHERNET
12.8V PBUS SUPPLY

PMU SUPPLY

BACKUP BATTERY

BOOTSTRAP SYSTEM FROM ADAPTER OR BATTERY
### SIGNAL CONSTRAINTS - PAGE 1

**D**

**GROUP 0**

| SIGNAL | PROPAGATION_DELAY | MAX_SPEED | MIN_SPEED | HOLD_ADDRESSES | PRIMARY千克 | SECONDARY千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千克 | DEFERRED千
<table>
<thead>
<tr>
<th>CPU_WT_L</th>
<th>CPU_TT&lt;0..4&gt;</th>
<th>CPU_TS_L</th>
<th>CPU_TEA_L</th>
<th>CPU_TBST_L</th>
<th>CPU_TA_L</th>
<th>CPU_QREQ_L</th>
<th>CPU_QACK_L</th>
<th>CPU_DRDY_L</th>
<th>CPU_DTI&lt;0..2&gt;</th>
<th>CPU_DATA&lt;32..63&gt;</th>
<th>CPU_DATA&lt;0..31&gt;</th>
<th>CPU_CI_L</th>
<th>CPU_BR_L</th>
<th>CPU_BG_L</th>
<th>CPU_AACK_L</th>
</tr>
</thead>
</table>

**Max Vias**
- Layer S: 1500 MIL: 3100 MIL
- Layer S: 1500 MIL: 3500 MIL
- Layer S: 1500 MIL: 2700 MIL
- Layer S: 1500 MIL: 2700 MIL
- Layer S: 1500 MIL: 2800 MIL
- Layer S: 1500 MIL: 2700 MIL
- Layer S: 1500 MIL: 3200 MIL

**Max Exposed Length**
- 250

**Net Spacing Type**
- 6

**No Test**
- True
- True

**Pulse Param**
- 83 MHz
- 83 MHz

**Scale**
- 19

**Temporary Area for TMDS/DVO signal constraints**

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**SHT**

**REV.**

**D**

**C**

**B**

**A**
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I PVT Release (Rev. A)
04/02/04  -  1. USB series termination near NEC PHY change to 43.2 ohm (Pg 17)
03/11/04  -  1. INT. TMDS Termination change to 2* 75 ohm = 150ohm (except CLK pair) (Pg 20)

DVT Release (Rev. A)
2. USB series termination near NEC PHY change to 47 ohm (Pg 17)
2. NO STUFF R236,R1,R271&R194 to remove PCI stub (Pg 9)

02/12/04  -  1. CPU VCore adjustment for V1.1 A7PM CPU (Pg 33)
3. ATI INT.TMDS termination change to 0 ohm, Qty:8 (Pg 20)
2. CPU AVDD adjustment for V1.1 A7PM CPU (Pg 5)

DVT Release (Rev. 03)
2. NO STUFF R236,R1,R271&R194 to remove PCI stub (Pg 9)
3. Modify LDO power sequence
4. AGP I/O VREF voltage divider chagne to both 1K ohm (Pg 12)
2. Add Bom Table for R97 2.21K ohm VCore Offset (Pg 33)

DVT Release (Rev. 04)
2. Add R468 and R601 for
3. Add R755,R756,R758,R759 for power rail
4. Connect OVDDSENSE to MAXBUS_SLEEP

DVT Release (Rev. 02)
1. CPU VCore adjustment for V1.1 A7PM CPU (Pg 33)
3. ATI INT.TMDS termination change to 0 ohm, Qty:8 (Pg 20)
2. NO STUFF R236,R1,R271&R194 to remove PCI stub (Pg 9)

DVT Release
1. Add 10K pull down for INT_TDO on page 13
3. Connect INT_TDO from intrepid to Cypress Chip PD* (U31)
2. Modify CPU_VCORE setting to Motorola new spec

PVT Release (Rev. A)
1. Schematic originated from Q16 MLB
2. Connect INT_TDO from Intrepid to Marvell 88E1111(U43)
3. Add R755,R756,R758,R759 for power rail
4. Connect VDD(Page 6) to CPU_VCORE_SLEEP(PAGE 5)

PVT Release (Rev. A)
1. Schematic originated from Q16 MLB
2. Add R468 and R601 for
3. Add R755,R756,R758,R759 for power rail
4. Connect OVDDSENSE to MAXBUS_SLEEP

PVT Release (Rev. A)
1. Schematic originated from Q16 MLB
2. Add R468 and R601 for
3. Add R755,R756,R758,R759 for power rail