### TABLE 5

**Table 5 Item**

<table>
<thead>
<tr>
<th>REFERENCE DESIGNATOR(S)</th>
<th>BOM OPTION</th>
</tr>
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<tbody>
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**Table 5 Head**

<table>
<thead>
<tr>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>PART#</th>
</tr>
</thead>
<tbody>
<tr>
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</tr>
</tbody>
</table>

**Bom Options (in common parts)**

<table>
<thead>
<tr>
<th>STUFF</th>
<th>NO STUFF</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.5V_MAXBUS</td>
<td>1.5V_MAXBUS</td>
</tr>
<tr>
<td>BSCG</td>
<td>BSCG</td>
</tr>
<tr>
<td>3V_HD_LOGIC</td>
<td>3V_HD_LOGIC</td>
</tr>
<tr>
<td>NO_BBANG</td>
<td>BBANG</td>
</tr>
<tr>
<td>INT_2_5V_COLD</td>
<td>INT_2_5V_HOT</td>
</tr>
<tr>
<td>ATI_MEMIO_HI</td>
<td>ATI_MEMIO_LO</td>
</tr>
<tr>
<td>USB_MODEM</td>
<td>SOFT_MODEM</td>
</tr>
<tr>
<td>GPU_PWRMSR</td>
<td>INT_TMDS</td>
</tr>
<tr>
<td>GPU_SS</td>
<td>VGA_BUFFER_RES</td>
</tr>
<tr>
<td>EXT_TMDS</td>
<td></td>
</tr>
</tbody>
</table>

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- Component Locations (2 of 2)
PCB SPECS

THICKNESS : 1.2 MM / 0.047 IN
1/2 OZ CU THICKNESS: 0.7 MILS
1.0 OZ CU THICKNESS: 1.4 MILS

IMPEDANCE : 50 OHMS +/- 10%
DIELECTRIC: FR-4
LAYER COUNT: 10
SIGNAL TRACE WIDTH: 4 MILS
SIGNAL TRACE SPACING: 4 MILS
PREPREG THICKNESS: 2-3 MILS

SEE PCB CAD FILES FOR MORE SPECIFIC INFO.

BOARD HOLES

GROUND VIAS

ASICS HEATSINK MOUNTS

GROUND VIAS

BOARD STACK-UP AND CONSTRUCTION

THICKNESS : 1.2 MM / 0.047 IN
1/2 OZ CU THICKNESS: 0.7 MILS
1.0 OZ CU THICKNESS: 1.4 MILS

IMPEDANCE : 50 OHMS +/- 10%
DIELECTRIC: FR-4
LAYER COUNT: 10
SIGNAL TRACE WIDTH: 4 MILS
SIGNAL TRACE SPACING: 4 MILS
PREPREG THICKNESS: 2-3 MILS

SEE PCB CAD FILES FOR MORE SPECIFIC INFO.
SEL = LOW; HOST = B PORT; A PORT = 1000HM TO GND
SEL = HIGH; HOST = A PORT; B PORT = 1000HM TO GND
LEFT I/O & AUDIO BOARD (LIO)

PLACE CLOSE TO CPU

PLACE IN BETWEEN 3.5/1.5/2.5V PMN SUPPLY

PLACE UNDERNEATH UPPER RAM ALTERNATE

PLACE CLOSE TO BATTERY CHARGER/VCORE

USB MODEM/SOFT MODEM

FAN INTERFACE

FAN INTERFACE

FAN INTERFACE

FAN INTERFACE

FAN INTERFACE

CPU FAN

GPU FAN

RIGHT USB BOARD

SERIAL DEBUG INTERFACE

TABLE 5 ITEM
SIGNAL CONSTRAINTS - PAGE 1

GOAL: MINIMIZE TH VIAS

SECONDARY LAYERS: 4,7
PRIMARY LAYERS: 9

ALL THE DVOD GROUP SIGNALS ROUTE AT LAYER 4 OR 7 AND ROUTE AS STANDARD 50OHM SIGNALS AT 4 MILS

100 OHM SPACING
### Functional Test Points

**Purpose:**

The functional test points listed below are for reference only. They are not to be considered as part of the final product. The test points are used for troubleshooting and should not be used for the following reasons:

- **P1:** As an input source for any test fixture.
- **P2:** As an input source for any test fixture.
- **P3:** As an input source for any test fixture.
- **P4:** As an input source for any test fixture.
- **P5:** As an input source for any test fixture.
- **P6:** As an input source for any test fixture.
- **P7:** As an input source for any test fixture.
- **P8:** As an input source for any test fixture.

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**Test Points:**

<table>
<thead>
<tr>
<th>Test Point</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>USB</td>
<td></td>
</tr>
<tr>
<td>RT. USB</td>
<td></td>
</tr>
<tr>
<td>WIRELESS</td>
<td></td>
</tr>
<tr>
<td>OPTICAL</td>
<td></td>
</tr>
<tr>
<td>TRACKPAD</td>
<td></td>
</tr>
<tr>
<td>MODEM/SERIAL</td>
<td></td>
</tr>
<tr>
<td>KEYBOARD</td>
<td></td>
</tr>
<tr>
<td>BATTERY</td>
<td></td>
</tr>
<tr>
<td>FANS</td>
<td></td>
</tr>
<tr>
<td>ETHERNET</td>
<td></td>
</tr>
<tr>
<td>FIREWIRE</td>
<td></td>
</tr>
</tbody>
</table>

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REVISION HISTORY

DVT RELEASE
Add ATI Power sequencing Circuit for M10 Power-up and Power-down (p.19-22, p.32-35)
Edit I2C table for LMU (p.13)
Add LMU connector and components (p.23)
Updated S-video filter values to those of P84 (p.22)
Replaced all 132S1061 [1uF,0805,10V,20%] with 132S0046 [1uF,0603,10V,20%] (p.14,15,27,30,33,34)
Updated 1.5V/2.5V switcher BOM to stay in sync with P84 [FET change and current limits] (p.34)
NO STUFFed entire 1.5V LDO circuit (p.15)
Removed XW17, jumper for CPU_VCORE_SLEEP (p.33)
Broke out quad OR-gate to discrete components for better placement (p.22,29)
Removed redundancy in DDR memory constraints (p.35)
Renamed FW low voltage power rails (p.27,37)
Pinned out audio connector (p.25)
Added full support for non-zero CPU_PLL_CFG<4> in run state (p.7)
Changed keyboard ZIF to large SMK connector (p.23)
Added A29 adapter detection circuit (p.29)
Renamed +14V_PBUS to +PBUS (p.all)
Changed JTAG_ENET_TDI to pullup [LA clk not used] (p.13)
Changed INT_TST_PLLEN_PD to pulldown only [LA clk not used] (p.13)
Removed temporary P84 constraints and finished up AGP clock changes (p.12,34)
Removed INT_CPUFB_IN cap per P84 (p.8)
Added 10K pullup to CG_ADDRSEL and 10K pulldown to CG_FSEL on CY28512 (p.14)
Changed Y6 to smaller form-factor crystal (p.26)
Removed LMU connector (p.23)
Changed to Q11 adpater detection scheme (p.28)
Added 5 bypass caps to each SO-DIMM connector (p.11)
Changed LIO board connector to 40 pin Molex connector (p.26)
Changed right USB board connector to 16 pin Hirose connector (p.26)
Changed PBUS holdup caps to P59 electrolytic cans (p.30)
Added P59 SO-DIMM connector as placeholder (p.12)
Corrected PLL_CFG<4> for Apollo 7 [needs to always be zero] (p.5,7)
Removed second fuse from FW ports [single fuse provides adequate power] (p.27)

DVT RELEASE (continue)

Add Sense Resistor to Vcore power rail, remove one 220uF cap <back to EVTA design> (P 33)

08/07/03 - Change CPU VCORE setting for both BEST and BETTER configurations again (p. 33)
07/28/03 - Change BOM option for C51,C52,C77,C78,C91,C92,C111 to 8.2uF Panasonic AL cap only (p. 34)
07/06/03 - Change R97 & R98 to 0402 package (p.33)
06/16/03 - Replace C705,C707,C711,C703 & C685 with part 128S0025 (p.20&32)
06/06/03 - Add four 0ohm jumper, in case there is no sw support for the multi-stage VCore (p.38)
06/03/03 - Add CPU Core Voltage offset option circuit (p.33)
05/27/03 - Change RP31 to 4.7K for I2C timing specification  (p.13)

04/21/03 - Add 12 ICT JTAG TEST PADs (P 39)
04/17/03 - Change 3V/5V inductors (152S0137) L61 & L62 (P 32)

03/13/03 - Change 3-P FAN connectors to 4-P (p.25)

EVT ENCLOSURE RELEASE

02/17/03 - Rename all Reference Designators

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