## REVISION HISTORY

### PROTO
- 04/05/2001: Printed revision history

### EVT
- 04/30/2001: Changed R2464 to correct unused GPIO logic level

### PVT
- 05/03/2001: Released as REV 07 for Pre-PVT
- 05/31/2001: Released as REV A for PVT/Production

### DVT
- 04/28/2001: Stuffed R2466 to correct unused GPIO logic level
- 05/31/2001: Changed R1720 and R2205 to 7.5K.
- 05/04/2001: Released as REV 06 for DVT

### Pre-PVT
- 04/27/2001: Changed R5822 to 100K for power sequencing improvements
- 05/04/2001: Released as REV 05 for DVT

### PVT
- 05/09/2001: Added FETs to control leakage on Vesta rails
- 06/28/2001: Added five ceramic caps to Vcore supply input
- 04/11/2001: Released as REV 01 for PROTO

### PROTO
- 04/15/2001: Various lead-free replacements
- 05/31/2001: Corrected caps on FireWire VP rail to 50V

### EVT
- 04/11/2001: Various Pb-free replacements
- 05/04/2001: Added NEC USB2 controller and PCI clock buffer

### PVT
- 04/07/2001: Various lead-free replacements
- 05/04/2001: Added Hynix VRAM option and PCBA
**I2S Series Rs**

<table>
<thead>
<tr>
<th>MAXBUS Pullups</th>
<th>AGP Pullups</th>
<th>USB Pulldowns</th>
<th>PCI Pullups</th>
<th>FW Series Rs</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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</tbody>
</table>

**Lower DVO Series Rs**

**MAXBUS Pullups**

**AGP Pullups**

**USB Pulldowns**

**PCI Pullups**

**FW Series Rs**

---

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Enhanced MAC-1 Test Coverage

Functional test points use a P6 pad placed on bottom side.
MMM_MCU_PMU BOM option is selected. Note: Neither option is necessary when it can be monitored by in shutdown. ALL moves the MCU to the PMU I2C bus so the time or only when the system is on. Selects whether MMM MCU is powered all – MMM_PWR_ALL / MMM_PWR_PWRON I2C bus 1 to resolve address conflict. PMU unstead. One ADT7467 connects to NB Most devices are connected directly to Allows bypassing Governator I2C bus. – GOV_I2C / GOV_I2C_BYPASS BOM options provided by this page: (NONE) Signal aliases required by this page: (NONE) Power aliases required by this page: (NONE)
Nets not requiring TPs due to JTAG
12.8V PBUS SUPPLY

CONNECT LTC1625 TR PINS TO VPP5V-SW PWR

MAIN BATTERY OR BACKUP BATTERY
BOOTSTRAP SYSTEM FROM ADAPTER,
MAIN BATTERY OR BACKUP BATTERY

PMU SUPPLY

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12.8V PBUS/PMU Supplies

APPLE COMPUTER INC.
1.5V/1.8V SWITCHER

Vout = 1.0V * (1 + Ra/Rb)

1.8V/1.5V Supplies

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Signal aliases required by this page:

- 10uF cap per rail.

NOTE: The four 3.3V rails are meant to be placed together. They are divided separately for test purposes.

Input aliases required by this page:

Output aliases provided by this page:

www.vinafix.vn
RT ALS SENSOR

Keyboard LED Driver

ALSO Support
BOM options provided by this page:
- =MAXBUS_CPU0_CLK

Power aliases required by this page:
- =PP1V5R1V8_MAXBUS

Page Notes
- Page notes printed by this page.
- Comments printed by this page.
- Notes provided by this page.

MAXBUS Straps

VIO DECOUPLING (28 PINS)

MAXBUS_ADDR<30>
MAXBUS_ADDR<29>
MAXBUS_ADDR<26>
MAXBUS_ADDR<24>
MAXBUS_ADDR<23>
MAXBUS_ADDR<21>
MAXBUS_ADDR<18>
MAXBUS_ADDR<16>
MAXBUS_ADDR<12>
MAXBUS_ADDR<10>
MAXBUS_ADDR<9>
MAXBUS_ADDR<8>
MAXBUS_ADDR<7>
MAXBUS_ADDR<2>
MAXBUS_ADDR<1>
MAXBUS_ADDR<0>

A8 MaxBus (CPU0)
AVDD = 0.59 * (1 + R4620 / R4621)
### Mill Frame Buffer Constraints

**REV.** D

**SCALE** 1/4" = 1'

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---

**M11 Frame Buffer Constraints**

**FAB_REFERENCE** 051-6839 F

---

**A**

**B**

**C**

---

**D**

---

<table>
<thead>
<tr>
<th>Component</th>
<th>Electrical Constraint Set</th>
<th>Physical Constraint Set</th>
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</thead>
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<tr>
<td>FB_B_DQ_R&lt;63..56&gt;</td>
<td>(provided above)</td>
<td>(provided above)</td>
</tr>
<tr>
<td>FB_B_DQ_R&lt;55..48&gt;</td>
<td>(provided above)</td>
<td>(provided above)</td>
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<tr>
<td>FB_B_DQ_R&lt;47..40&gt;</td>
<td>(provided above)</td>
<td>(provided above)</td>
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<tr>
<td>FB_B_DQ_R&lt;39..32&gt;</td>
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<td>(provided above)</td>
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<tr>
<td>FB_B_DQ_R&lt;31..24&gt;</td>
<td>(provided above)</td>
<td>(provided above)</td>
</tr>
<tr>
<td>FB_B_DQ_R&lt;23..16&gt;</td>
<td>(provided above)</td>
<td>(provided above)</td>
</tr>
<tr>
<td>FB_B_DQ_R&lt;15..8&gt;</td>
<td>(provided above)</td>
<td>(provided above)</td>
</tr>
<tr>
<td>FB_B_DQ_R&lt;7..0&gt;</td>
<td>(provided above)</td>
<td>(provided above)</td>
</tr>
<tr>
<td>FB_B_DQM_R&lt;6&gt;</td>
<td>(provided above)</td>
<td>(provided above)</td>
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<tr>
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<td>(provided above)</td>
<td>(provided above)</td>
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<td>(provided above)</td>
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<tr>
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<td>(provided above)</td>
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<td>(provided above)</td>
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<tr>
<td>FB_B_DQM_R&lt;0&gt;</td>
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<td>FB_B_DQS_R&lt;5&gt;</td>
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<td>FB_B_DQS_R&lt;4&gt;</td>
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<tr>
<td>FB_B_DQS_R&lt;0&gt;</td>
<td>(provided above)</td>
<td>(provided above)</td>
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<tr>
<td>FB_B_CAS_L_R</td>
<td>(provided above)</td>
<td>(provided above)</td>
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<tr>
<td>FB_B_BA_R&lt;2..0&gt;</td>
<td>(provided above)</td>
<td>(provided above)</td>
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<tr>
<td>FB_B_ADDR_R&lt;12..0&gt;</td>
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<tr>
<td>FB_B_CS_L_R</td>
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<tr>
<td>FB_B_CKE_R</td>
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<tr>
<td>FB_B_CLKDDR_1_N_R</td>
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<td>FB_B_CLKDDR_1_P_R</td>
<td>(provided above)</td>
<td>(provided above)</td>
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<tr>
<td>FB_B_CLKDDR_0_N_R</td>
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<tr>
<td>FB_B_CLKDDR_0_P_R</td>
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<td>(provided above)</td>
</tr>
</tbody>
</table>

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**FB_A_DQ_R<63..56>**

**FB_A_DQ_R<55..48>**

**FB_A_DQ_R<47..40>**

**FB_A_DQ_R<39..32>**

**FB_A_DQ_R<31..24>**

**FB_A_DQ_R<23..16>**

**FB_A_DQ_R<15..8>**

**FB_A_DQ_R<7..0>**

**FB_A_DQM_R<7>**

**FB_A_DQM_R<6>**

**FB_A_DQM_R<4>**

**FB_A_DQM_R<3>**

**FB_A_DQM_R<2>**

**FB_A_DQM_R<1>**

**FB_A_DQM_R<0>**

**FB_A_DQS_R<7>**

**FB_A_DQS_R<6>**

**FB_A_DQS_R<5>**

**FB_A_DQS_R<4>**

**FB_A_DQS_R<3>**

**FB_A_DQS_R<2>**

**FB_A_DQS_R<1>**

**FB_A_DQS_R<0>**

**FB_A_WE_L_R**

**FB_A_CAS_L_R**

**FB_A_BA_R<2..0>**

**FB_A_ADDR_R<12..0>**

**FB_A_CS_L_R**

**FB_A_CKE_R**

**FB_A_CLK_DDR_1_P_R**

**FB_A_CLK_DDR_0_N_R**

---

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NOTE: AGP 8x signals are not provided

BOM options provided by this page:
- =AGP_GPU_RESET_L - Active low reset for GPU
- =AGP_VREF - VRef divider output for

Signal aliases required by this page:
- =PP1V5_AGP
- =PP3V3_AGP

Power aliases required by this page:
- ELECTRICAL_CONSTRAINT_SET
- I798
- SPACING
- CLOCK
- NET_TYPE
- PHYSICAL
- DIFFERENTIAL_PAIR

AGP_CLK66M_GPU = PP1V5_AGP

R5720 47K
44
43
10

R5725 10K
402
5%
2

R5721 MF-LF 1/16W 402 5% 2

R5726 47K
402
MF-LF 5%

R5730

C5732 0.1uF
402
X5R 16V

C5731

R5730 1K
402
MF-LF 1%

R5731

R5722

AGP SUS_STAT_L_PU

STP_AGP_L

STOP_AGP_L

AGP_AD_STB1_N

AGP_AD_STB0_N

AGP_AD_STB0_P

AGP_SB_STB_N

AGP_SB_STB_P

AGP_DEVSEL_L

AGP_TRDY_L

AGP_IRDY_L

AGP_FRAME_L

AGP_GNT_L

AGP_INT_L

AGP_ATI_RESET_L

AGP_CLK66M_GPU
Implement "Power Miser" feature

BOM options provided by this page:
- =GPUVCORE_PGOOD - Active high Power Good
- =PPVIN_LTC1778_GPU
- 81778_ITH_RC
- 20.0K
- 402
- 10%
- 7
- 402
- 1%
- 1
- 2
- 2
- 1
- C5831
- 402
- 25V
- NO STUFF
- 0
- 402
- 5%
- 1
- 2
- 2
- 1
- C5822
- 0.1uF
- 10V
- 20%
- 6
- 402
- 1/16W
- 402
- 1%

\[1.054V = 0.8V \times \left(1 + \frac{R_a}{R_b}\right)\]
\[1.307V = 0.8V \times \left(1 + \frac{R_a \times (R_c+R_b)}{R_c \times R_b}\right)\]

C5810
- 4.7uF
- 1206
- 20%
- 1
- 1
- 1
- 1
- L5800
- 4.7uF
- 3
- 25V
- CERM
- 10V
- 20%
- 2
- 2
- 2
- C5803
- 470uF
- TANT
- 7343-H2.9
- CRITICAL
NOTE: Implements a low-swing DVO bus only - DVO_1V5

BOM options provided by this page:
- =PP1V5_GPU_DVO
- =PP3V3_GPU_VDDR3
- =PP1V8R2V5_GPU_FB_VIO

Signal aliases required by this page:
- =PP1V8_GPU_VDD_MEM_CLK
- =PP1V8_GPU_PANEL_IO
- =PP1V8_GPU_LVDS_PLL
- =PP1V8_GPU_LVDDR_2V8
- =PP2V8_GPU_LVDS_IO
- =PP2V5_GPU_LVDS_IO

Dimensions:
- MIN_LINE_WIDTH=0.5 mm
- VOLTAGE=1.8V

Critical parts:
- BGA

Miscellaneous:
- SYNC_MASTER=MARÍAS
- GPIO - 3.3V
- AGP 4X I/O - 1.5V

Notes:
- www.vinafix.vn
- MIN_NECK_WIDTH=0.25 mm
- SIZE 43
- FERR-220-OHM
- MAKE_BASE=TRUE
- CRITICAL
- OMIT
- CRITICALLY OMIT
- BGA
- FERR-10-OHM-500MA
- FERR-220-OHM
- FERR-10-OHM-250MA
- FERR-10-OHM-125MA
- FERR-10-OHM
- FERR-10-OHM-6.3V
M11 Power Shutdown Sequencing

LVDDR 2.8V LDO

SPREAD SPECTRUM SUPPORT
S0=1; S1=0 => -1.5% DOWN-SPREAD

27M OSC

---
Isolation will be disabled as well.

As host rails rise, TP0610 will turn off, as will remote power key on remote device DDC_CLK is isolated from system is shutdown or asleep.

3.3V. When power key HPD normally driven to HPD_PWR_SNS_EN will turn off, as will remote device path into DDC_CLK.

Isolation required for DVI power switch

NOTE: Pulldown for DVI_HPD provided by DVI power switch interface

MIN_NECK_WIDTH=0.25 mm

SM-LF
<table>
<thead>
<tr>
<th>Signal Alias</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>I2_PCI_FBCLK</td>
<td>Feedback clock from I2 to PCI device</td>
</tr>
<tr>
<td>PCI_CTL</td>
<td>Control signals for PCI device</td>
</tr>
<tr>
<td>PCI_AD31_24</td>
<td>Address lines for PCI device</td>
</tr>
<tr>
<td>PCI_AD23_22</td>
<td>Address lines for PCI device</td>
</tr>
<tr>
<td>PCI_CLK_SLOTD</td>
<td>Clock signals for PCI slot A</td>
</tr>
<tr>
<td>PCI_CLK_SLOTA</td>
<td>Clock signals for PCI slot A</td>
</tr>
<tr>
<td>I2_PCI_FBCLK_OUT_R</td>
<td>Feedback clock output from I2 to PCI device</td>
</tr>
<tr>
<td>TP_PCI_CLK33M_SLOTA_R</td>
<td>Clock signals for PCI slot A</td>
</tr>
</tbody>
</table>

**PCI Interface**

- **PCI Device**
  - PCI_DEVSEL_L
  - PCI_IRDY_L
  - PCI_FRAME_L
  - PCI_PAR_H
  - PCI_REQ_0_L

- **PCI Bus Interface**
  - PCI/ROM INTERFACE
  - PCI_INTERFACE
  - PCI DEVICE 1

**Page Notes**

Page Notes - Page 8 of 14

- **I2 PCI Interface**
- **PCI FULL-UPS**
- **ROM CS_L**
- **ROM OES_L**

**SPACING**

- **I2_FBCLK**
- **CLOCK**

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NOTE: This AirPort implementation does not support PME.

PCI AD17 (Slot "A") - AirPort (0x????/0x????)

PCI Devices implemented on this page:
- =USB_BT_N (Bluetooth USB D-)
- =USB_BT_P (Bluetooth USB D+)
- =PCI_AIRPORT_RESET_L (PCI Reset)
- =PCI_CLK33M_AIRPORT (33MHz PCI clock)

Signal aliases required by this page:
- =PP3V3_PWRON_BT (Bluetooth Power)

Power aliases required by this page:
- =PP3V3_PCI_AIRPORT
- =PP3V3_PWRON_BT

Q85 Connector
Q16C/516S0361/F-ST-SM
Q41C/516S0352/M-ST-SM-LF

Q85 AIRPORT/BT CONN
Q16C/516S0361/F-ST-SM
Q41C/516S0352/M-ST-SM-LF

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NOTE: This USB2 implementation supports PCI Devices implemented on this page:
- USB2_NEC
- PCI_USB2_INT_L
- PP3V3_PCI_USB2 (D3cold rail)
- PPVIO_PCI (to 3.3V or 5V)

ELECTRICAL_CONSTRAINT_SET

Page Notes
lengthen net by ~250ps. Net has a non-shared schematic page.

resistor for GPIO 16. It must be pull-up or pull-down resistor.

series termination. Any

NOTE: This page does not provide any BOM options provided by this page:
Page Notes

Signal aliases required by this page:
- _PP2V5_ENET

Power aliases required by this page:
- ELECTRICAL_CONSTRAINT_SET

Page Notes

Transformers should be mirrored on opposite sides of the board.

Place close to connector.

Ethernet routing priority:
- 1. Decoupling caps
- 2. TX SERIES TERMINATION - LOCATE NEAR LINK
- 3. EA SERIES TERMINATION - LOCATE NEAR PAY

All differential signals should be close, parallel, matched lengths, with minimum via count, and short if possible.

Sandwich each RJ54 pair between chassis grounds.

MIN_NECK_WIDTH=0.25 mm
MIN_LINE_WIDTH=0.5 mm
VOLTAGE=2.5V

Ethernet Connector

www.vinafix.vn
"Snapback" & "Late VG" Protection

Cable Power

Port 1 Bilingual

Port 2 1394A

FireWire Ports

---

**Termination**

Place close to FireWire PHY

3rd TPA/TPB pair unused

ESD Rail

---

"Snapback" & "Late VG" Protection

---

**Cable Power**

---

**Port 1 Bilingual**

---

**Port 2 1394A**

---

**FireWire Ports**

---
Place series terminators approximately halfway between Lesta and Nb. (They should probably be slightly closer to Lesta than the Nb.).

FireWire Series Term

WWW.VINAFIX.VN
USB2 data pairs is 90 ohms.

NOTE: Target differential impedance for Secondary Length:  500 mils
Primary Max Sep:   7.5 mils
Length Tolerance:   50 mils
Line To Line:     19.5 mils

BOM options provided by this page:
- =RP92xxPy (pinswappable USB pulldowns)

Signal aliases required by this page:
- =PP3V3_PWRON_USB

Power aliases required by this page:

Net Spacing Type: USB2

Page Notes

One pair for each port USB2_*<0..5>

Crystal load capacitance is 16pF

Put crystal circuit close to I2

Crystal load capacitance is 0.1uF

Crystal load capacitance is 22pF
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Audio Board Connector

Place shorts at output of 3.3V and 5V regulator.

Audio Board Connector

Audio Board Connector

Audio Board Connector

Audio Board Connector
<table>
<thead>
<tr>
<th>Constraint</th>
<th>Value 1</th>
<th>Value 2</th>
<th>Value 3</th>
<th>Value 4</th>
<th>Value 5</th>
</tr>
</thead>
<tbody>
<tr>
<td>DVO</td>
<td>0.25 MM</td>
<td>75_OHM_SE</td>
<td>100_OHM_DIFF</td>
<td>100_OHM_DIFF</td>
<td>100_OHM_DIFF</td>
</tr>
<tr>
<td>S-VIDEO</td>
<td>0.15 MM</td>
<td>75_OHM_SE</td>
<td>100_OHM_DIFF</td>
<td>100_OHM_DIFF</td>
<td>100_OHM_DIFF</td>
</tr>
<tr>
<td>VGA</td>
<td>0.25 MM</td>
<td>75_OHM_SE</td>
<td>100_OHM_DIFF</td>
<td>100_OHM_DIFF</td>
<td>100_OHM_DIFF</td>
</tr>
<tr>
<td>LVDS</td>
<td>0.25 MM</td>
<td>75_OHM_SE</td>
<td>100_OHM_DIFF</td>
<td>100_OHM_DIFF</td>
<td>100_OHM_DIFF</td>
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<td>100_OHM_DIFF</td>
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</tr>
<tr>
<td>THERM</td>
<td>0.25 MM</td>
<td>75_OHM_SE</td>
<td>100_OHM_DIFF</td>
<td>100_OHM_DIFF</td>
<td>100_OHM_DIFF</td>
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