PCB SPECS

THICKNESS: 1.2 MM / 0.047 IN
1/2 OZ CU THICKNESS: 0.7 MILS
1.0 OZ CU THICKNESS: 1.4 MILS

IMPEDANCE: 50 OHMS +/- 10%
DIELECTRIC: FR-4
LAYER COUNT: 12
SIGNAL TRACE WIDTH: 4 MILS
SIGNAL TRACE SPACING: 4 MILS
PREPREG THICKNESS: 2-3 MILS

SEE PCB CAD FILES FOR MORE SPECIFIC INFO.
CPU PLL CONFIG CIRCUITRY

STATE ENCODING | CPU_PLL_STOP_OC | CPU_VCORE_HI_OC
---|---|---
LOW SPEED | 0 | 0
HIGH SPEED | 0 | 0
PLL DISABLE | 1 | 2

CPU CONFIGURATION

MAXBUS VSEL

BUSTYPE SELECT

CPU PLL CONFIGURATION

APOLLO 7

MULTIPLIER | CORE FREQUENCY (AT BUS FREQUENCY) | CPU_PLL_CFG
---|---|---
| 4 | 0 | 0123
| 1 | 0 | 0011
| 1 | 0 | 0010
| 1 | 0 | 0001
| 1 | 0 | 0010
| 1 | 0 | 0011
| 1 | 0 | 0000
| 1 | 0 | 0001

CPU CONFIGURATION

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www.vinhafix.vn
SEL = LOW; HOST = B PORT; A PORT = 100OHM TO GND
SEL = HIGH; HOST = A PORT; B PORT = 100OHM TO GND
MEM_MUXSEL_H<0> AND MEM_MUXSEL_L<0> ARE ACTIVE LOW
MEM_MUXSEL_H<1> AND MEM_MUXSEL_L<1> ARE ACTIVE HIGH

ADDED 0 OHM RESISTORS IN CASE POLARITY IS WRONG
PCI1510 PULL-UPS

PC CARD/CARDBUS CONNECTOR

CARDBUS

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**OUTPUT VOLTAGE**

![Diagram of output voltage](image)

**FOR V-STEP:**

- When A/R is high (fast): D4-GO read as is.
- When A/R is low (slow): <=1K-ohm = 0
  >=100K-ohm = 1

If all pull-ups are >=10K and all pull-downs are <=1K, V_A = V_S.
<table>
<thead>
<tr>
<th>SIGNAL NAME</th>
<th>DIFFERENTIAL_PAIR</th>
<th>MAX_EXPOSED_LENGTH</th>
<th>NET_SPACING_TYPE</th>
<th>MAX_VIAS</th>
</tr>
</thead>
<tbody>
<tr>
<td>RJ45_DN&lt;2&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EIDE_DMACK_L</td>
<td>EIDE_OPTICAL_WR_L</td>
<td></td>
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<tr>
<td>EIDE_OPTICAL_RD_L</td>
<td>EIDE_CS1_L</td>
<td></td>
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<tr>
<td>HD_DMARQ</td>
<td>EIDE_CS0_L</td>
<td>UIDE_DATA&lt;6..0&gt;</td>
<td>100 MHZ</td>
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<td>ENET_PHY_TX_EN</td>
<td>UIDE_INTRQ</td>
<td>UIDE_IOCHRDY</td>
<td>200.0000</td>
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<tr>
<td>FW_LINK_CNTL&lt;1..0&gt;</td>
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<tr>
<td>DPOE_D</td>
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<tr>
<td>DPHD_D</td>
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<tr>
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<tr>
<td>DPHD_L</td>
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<tr>
<td>DPOE контакт</td>
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<tr>
<td>DPHD контакт</td>
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</tr>
</tbody>
</table>

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**EXTERNAL LAYER (GBL)” (J SERIES 2.0)***

**DIFFERENTIAL TRACES**

- E = 4.3 (dielectric constant)
- W = 3.4 MIL (trace width)
- S = 10 MIL (separation of diff traces)
- ER = 4.3 (dielectric constant)
- ZDIFF = 107.17 OHM

**INTERNAL LAYER (GBL)” (J SERIES 2.0)**

- T = 4.3 (dielectric constant)
- W = 4 MIL (trace width)
- S = 5 MIL (separation of diff traces)
- ER = 4.3 (dielectric constant)
- ZDIFF = 107.17 OHM

**SIGMA FIX VALUE**

- Er = 4.3 (dielectric constant)
- W = 3.4 MIL (trace width)
- S = 10 MIL (separation of diff traces)

**Cu Thickness (1.0 Mil)**

- 500.0000

**Cu Thickness (2.0 Mil)**

- 100.0000

**Cu Thickness (5.0 Mil)**

- 200.0000

**Cu Thickness (10.0 Mil)**

- 500.0000

**Ground Plane (GBL)” (J SERIES 2.0)**

- GROUND PLANE

**Arduino Fix Value**

- 500.0000

**TRACES**

- H0 = 25.0 Microinch (trace height)
- G0 = 7.0 Microinch (trace width)
- D0 = 10.0 Microinch (trace separation)
- M0 = 10.0 Microinch (trace location)

**LINES**

- L0 = 4.0 Microinch (line height)
- L1 = 4.0 Microinch (line width)
- L2 = 4.0 Microinch (line separation)
- L3 = 4.0 Microinch (line location)

**DIAGRAM**

- Diagram showing various signals and traces with their respective properties.
<table>
<thead>
<tr>
<th>Section</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>ISSUE 1</td>
</tr>
<tr>
<td>B</td>
<td>ISSUE 2</td>
</tr>
<tr>
<td>C</td>
<td>ISSUE 3</td>
</tr>
<tr>
<td>D</td>
<td>ISSUE 4</td>
</tr>
</tbody>
</table>

**FUNCTIONAL TEST POINTS**

- JTAG_ASIC_TCK
- JTAG_ASIC_TMS
- FUNC_TEST=YES
- JTAG_ASIC_TDI
- INT_I2C_CLK1
- INT_I2C_DATA2
- DVI_DDC_DATA_UF
- LVDS_L0N
- LVDS_L2P
- LVDS_U0N
- LVDS_U1N
- CLKLVDS_LN
- VGA_B
- VGA_HSYNC
- MODEM_USB_DP
- PCI_FRAME_L
- EIDE_OPTICAL_DATA<9>
- EIDE_OPTICAL_DATA<7>
- EIDE_OPTICAL_DATA<6>
- AIRPORT_PCI_INT_L
- AIRPORT_PCI_REQ_L
- SVC_PAR
- I290
- I289
- I288
- TEB_TP
- FANR_PWM
- PMU_BATT_DET_L
- VCORE_VID0
- VCORE_MUX_EN
- KBD_COMMAND_L
- KBD_CONTROL_L
- KBD_X<0>
- KBD_X<1>
- KBD_X<7>
- FW_TPO0R
- FW_TPI1P
- FW_TPO1N
- GPU_VCORE
- VCORE_FB
- ADAPTER_DET
- CHARGE_LED_L
- KBD_LED1_OUT
- VCORE_FB
- SUTRO_ALS_GAIN_SW
- CPU_VCORE_SLEEP
- CPU_HRESET_L
- RJ45_DP<0>
- RJ45_DP<3>
- NEC_LEFT_USB_OVERCURRENT
- NONE
- REV.
- B051-6459

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