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### Schematic

- **Date**: 08/24/2005
- **Description**: Reference Designated
- **Rev.**: 1
- **Zone**: LB, P/N LABEL, PCB, 28MM X 6MM
- **Sync Master**: 08/24/2005

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**Cross Reference Page**

- 61: I2 DAV Interface
- 62: NEC USB
- 63: 12 SATA Interface
- 64: I2 DOM/ODM Connectors
- 65: Vesta Ethernet PHY
- 66: Ethernet Connector
- 67: I2 Firewire Interface
- 68: Vesta Firewire PHY
- 69: Firewire Ports
- 70: Firewire Series Term
- 71: I2 DBH Interface
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- 73: NEC USB/PHY Interface
- 74: 100 Audio Board Connector
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**PDF CSB CONTENTS**

- 52 DOMS SD-MDIM Slot A
- 53 HDMI 2 SD-MDIM Slot A

**SYNC MASTER DATE**

- 08/24/2005

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**METRIC**

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**CE**

- 08/24/2005

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**Product Release**

- 08/24/2005
**Enhanced MAC-1 Test Coverage**

Functional test points use a P6 pad placed on bottom side.

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**Functional Test Points**

- Place within 25 mm of inverter connector.
- Place within 25 mm of power supply.
- Place 2 TPs @ connector.
- Place within 25 mm of ODD/HDD connector.
- Place within 25 mm of battery connector.
- Place within 25 mm of right USB connector.
- Place within 25 mm of left USB connector.
BOM_MCU_PMU BOM option is selected.

NOTE: Neither option is necessary when
it can be monitored by in shutdown.

ALL moves the MCU to the PMU I2C bus so
the time or only when the system is on.
Selects whether MMM MCU is powered all
- MMM_PWR_ALL / MMM_PWR_PWRON

I2C bus 1 to resolve address conflict.
PMU unstead. One ADT7467 connects to NB
Most devices are connected directly to
Allows bypassing Governator I2C bus.
- GOV_I2C / GOV_I2C_BYPASS

BOM options provided by this page:
(NONE)
Signal aliases required by this page:
(NONE)
Power aliases required by this page:
(NONE)
Nets not requiring TPs due to JTAG
PMU Reset Circuit

Sleep LED

Charge LED

Serial Debug Interface

Debugging Aids

LEDs/Reset/Debug

Apple Computer Inc.

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Scale: None

Revision: Apple Computer Inc.
PLACE CLOSE TO CPU

PLACE IN BETWEEN 3/5/1.5/2.5V PWR SUPPLY

PLACE UNDERNEATH UPPER RAM ALTERNATE 1

PLACE CLOSE TO BATTERY CHARGER/VCORE ALTERNATE 2

KEEP STUFFING RESISTORS CLOSE TO ADT7467 CONTROLLER
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USB Trackpad Conn

SOFT MODEM CONN

APPLE COMPUTER INC.
SERIES RESISTORS FOR CONTROL SIGNALS
PINS ARE SNAPPABLE FOR RPAKS RP4800-RP4804

SERIES RESISTORS FOR CLOCKS

SERIES RESISTORS FOR CS / CKE
Do not swap with other RPAKs
SLOT "A"
UPPER/STD SLOT
FACTORY SLOT

DDR2 VREF
ADD ONE 0.1uF PER SLOT

RAM_VREF
MIN_NECK_WIDTH=0.25 mm
MIN_LINE_WIDTH=0.38 mm
MAKE_BASE=TRUE
ADD ONE 0.1UF PER SLOT

SDA
VSS57
DM7
VSS43
DQ43
DQ42
VSS40
DQ40
VSS36
DQS4
VSS33
NC/ODT1
CAS*
WE*
BA0
A10/AP
VDD6
A9
A12
NC2
VDD0
DQ27
VSS27
DM3
DQ19
DQ18
DQS2*
VSS14
DQ11
DQ10
DQS1*
DQ8
DQ3
VSS6
VSS1
VSS2
VSS7
VSS5
VSS2
DM6
CK1
S0*
RAS*
VDD5
DQS3
DQ29
DQ23
DQ22
DQ20
DQ15
CK0*
DQ13
DQ12
VSS7
VSS5
VSS2
DM1
DQ6
DQ4
VSS6
VSS1
VSS2
DQ62
DQS7
DQ60
DQ53
DQ52
DQ46
DQ44
RAS*
VDD11
DQ20
DQ15
CK0*
DQ13
DQ12
VSS7
VSS5
VSS2
DM1
DQ6
DQ4
VSS6
VSS1
VSS2

SLOT "B"
LOWER/REV SLOT
CUSTOMER SLOT

RAM_DATA_B<59>
RAM_DQM_B<7>
RAM_DATA_B<60>
RAM_DATA_B<54>
RAM_DATA_B<52>
RAM_DQS_B_N<6>
RAM_DATA_B<51>
RAM_DQS_B_P<4>
RAM_DQS_B_N<4>
RAM_DATA_B<39>
RAM_WE_L
RAM_ADDR<1>
RAM_ADDR<8>
RAM_ADDR<12>
RAM_BA<2>
RAM_CKE<2>
RAM_DATA_B<27>
RAM_DATA_B<21>
RAM_DQS_B_N<2>
RAM_DATA_B<10>
RAM_DQS_B_P<1>
RAM_DATA_B<7>
RAM_DATA_B<3>

=PP1V8_PWRON_DDR2

www.vinafix.vn
WHEN VCORE_CNTL HIGH => 1.307V
1.307V = 0.8V \times (1 + Ra \times (Rc+Rb) / (Rc \times Rb))

WHEN VCORE_CNTL LOW => 1.054V
1.054V = 2 \times (1 + Ra / Rb)
**Electrical Constraint Set**

The TMDS data pairs are 100 ohms.

Signal aliases required by this page:
- =PP3V3_RUN_SI

Power aliases required by this page:
- I82
- I80
- I79
- I78
- I77
- I75
- I59
- I58
- I56

Upper DVO series termination

Place close to GPU

SM-LF

Upper Channel Series Termination

Provided by Lower TxMr

SM-LF

Place C6838/C6839

C6833

100pF

C6834

100pF

C6835

100pF

C6830

X5R

C6831

X5R

C6832

X5R

C6836

0603

0603

0.001uF

0.001uF

49.9

RF-LF

1% 1% 1% 1%

C6837

X5R

C6838

C6839

10UF

10UF

805

X5R

6.3V

10%

10%

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www.vinafix.vn
Panel has 2K pull-ups

100K pull-ups are for

Panel has 2K pull-ups
### BOM Options Provided by This Page:

- **PCI_CTL**
- **PCI_STOP_L**
- **PCI_FRAME_L**
- **PCI_TRDY_L**
- **PCI_REQ_L**
- **PCI_REQ_0_L**
- **PCI_REQ_1_L**
- **PCI_SLOTA_REQ_L**
- **PCI_SLOTA_GNT_L**

#### Electrical Constraint Set

- **PCI_CBE_3_L**
- **PCI_AD_31_H**
- **PCI_AD_30_H**
- **PCI_AD_29_H**
- **PCI_AD_28_H**
- **PCI_AD_27_H**
- **PCI_AD_26_H**
- **PCI_AD_25_H**
- **PCI_AD_24_H**
- **PCI_AD_23_H**
- **PCI_AD_22_H**
- **PCI_AD_21_H**
- **PCI_AD_20_H**
- **PCI_AD_19_H**
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- **PCI_AD_13_H**
- **PCI_AD_12_H**
- **PCI_AD_11_H**
- **PCI_AD_10_H**
- **PCI_AD_08_H**
- **PCI_AD_07_H**
- **PCI_AD_06_H**
- **PCI_AD_05_H**
- **PCI_AD_04_H**
- **PCI_AD_03_H**
- **PCI_AD_02_H**
- **PCI_AD_01_H**
- **PCI_AD_00_H**
- **PCI_CLK_1_H**
- **PCI_CLK_0_H**
- **PCI_GNT_0_L**
- **PCI_GNT_1_L**
- **PCI_GNT_2_L**
- **PCI_GNT_3_L**
- **ROM_WE_L**
- **ROM_OE_L**
- **ROM_CS_L**

#### Notes

- **3.3V IN**
- **TP_PCI_CLK33M_SLOTD_R**
- **TP_PCI_CLK33M_SLOTA_R**
- **I2_PCI_FBCLK_OUT**
- **I2_PCI_FBCLK_IN**
- **NET_TYPE**
- **CLOCK**
- **STOP**
- **BootROM Data**
- **PCI ONLY**
- **SLOT E IDSEL**
- **BootROM ADDR**

---

**Additional Notes:**

- **Sync Date:** 08/24/2005
- **Resistors:**
  - **RP7251P4**
  - **RP7251P3**
  - **RP7251P2**
  - **RP7250P4**
  - **RP7250P3**
  - **RP7250P2**

**Specifications:**

- **SM-LF**
- **1/16W**
- **5%**
- **402**

---

**References:**

- [www.vinafix.vn](http://www.vinafix.vn)
This page does not provide a pull-up or pull-down resistor.

NOTE: All I2 GPIOs should have a schematic page.

Any series termination, including clock signals, should be provided by the PHY page or a non-shared termination, including clock signals, should be provided by the PHY page or a non-shared termination.

NOTE: All I2 GPIOs should have a pull-up or pull-down resistor. This page does not provide a pull-up or pull-down resistor. This page does not provide a pull-up or pull-down resistor. This page does not provide a pull-up or pull-down resistor. This page does not provide a pull-up or pull-down resistor.

These GPIOs are referenced to the Ethernet I/O rail.
Page Notes

Power aliases required by this page:
- PP2V5_ENET
- PP3V3_VESTA

Signal aliases required by this page:
- GND_CHASSIS_ENET

Power aliases required by this page:
- ELECTRICAL_CONSTRAINT_SET

I-750
I-749
I-748
I-747
I-746
I-745
I-744
I-743

Ethernet routing priority:
1. Decoupling caps
2. TX SERIES TERMINATION - LOCATE NEAR LINK
3. RX SERIES TERMINATION - LOCATE NEAR PHY

All differential signals should be close, parallel, matched length, with minimum via count, and short if possible.

Short shielded RJ-45 pairs between chassis grounds.

Transformers should be mirrored on opposite sides of the board.

Place one cap at each pin of transformer.
**Page Notes**

- **Power aliases required by this page:**
  - GND CHASSIS FW PORT3
  - GND CHASSIS FW PORT2

- **Signal aliases required by this page:**
  - GND FW PORT3
  - GND FW PORT2

**Notes:**

- This page is expected to contain the necessary aliases to help the designer properly connect and/or process the alias signals required on this page.
- FPGA pins are not hard-wired to provide these signals.
- A 1394b Voltage supply is also included on this page.
- **Logic Ground for Speed Signaling**
  - All local grounds per 1394b spec.

**Warning:**

- BREF needs to be isolated from all local grounds per 1394b spec.
- When a bilingual device is connected to a beta-only device, the BREF pin needs to be connected to the beta-only device (to avoid ground offset issue).
- BREF should be hard-connected to the speed signaling logic ground for speed signaling and code mismatch detection currents per 1394b V1.33.
Place series terminators approximately halfway between Vesta and NB.
(They should probably be slightly closer to Vesta than the NB.)
USB2 data pairs is 90 ohms.

NOTE: Target differential impedance for
Secondary Length:  500 mils
Secondary Max Sep: 100 mils
Primary Max Sep:   7.5 mils
Length Tolerance:   50 mils
Line To Line:     19.5 mils

BOM options provided by this page:
- =RP92xxPy (pinswappable USB pulldowns)

Signal aliases required by this page:
- =PP3V3_PWRON_USB

Power aliases required by this page:
- =PP1V5_PWRON_I2_USBPLL

APPLE COMPUTER INC.
USB2 data pairs is 90 ohms.

NOTE: Target differential impedance for USB2 -PP3V3_PWRON_USB2

Net Spacing Type: USB2

USB2 data pairs in 90 ohms.

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**Spacing & Physical Constraints**

A

B

C

D

E

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**Sync Information**

- Sync Master: Marias
- Sync Date: 08/24/2005
- Sync Rev.: 1

**Spares & Physical Rules**

- Table of Physical Rules
- Table of Spacing Rules
- Table of Physical Assignment
- Table of Spacing Assignment
- Scale
- Size

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