PCB SPECS

THICKNESS: 1.2 MM / 0.047 IN
1/2 OZ CU THICKNESS: 0.7 MILS
1.0 OZ CU THICKNESS: 1.4 MILS

IMPEDANCE: 50 OHMS +/- 10%
DIELECTRIC: FR-4
LAYER COUNT: 12
SIGNAL TRACE WIDTH: 4 MILS
SIGNAL TRACE SPACING: 4 MILS
PREPREG THICKNESS: 2-3 MILS

SEE PCB CAD FILES FOR MORE SPECIFIC INFO.

BOARD STACK-UP AND CONSTRUCTION

<table>
<thead>
<tr>
<th>Layer</th>
<th>Material</th>
<th>Description</th>
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</thead>
<tbody>
<tr>
<td>1</td>
<td>PREPREG</td>
<td>SIGNAL (1/3 OZ + COPPER PLATING)</td>
</tr>
<tr>
<td>2</td>
<td>LAMINATE</td>
<td>GROUND (1/2 OZ)</td>
</tr>
<tr>
<td>3</td>
<td>PREPREG</td>
<td>SIGNAL (1/2 OZ)</td>
</tr>
<tr>
<td>4</td>
<td>LAMINATE</td>
<td>SIGNAL (1/2 OZ)</td>
</tr>
<tr>
<td>5</td>
<td>PREPREG</td>
<td>GROUND (1/2 OZ)</td>
</tr>
<tr>
<td>6</td>
<td>LAMINATE</td>
<td>CUT POWER PLANE (1 OZ)</td>
</tr>
<tr>
<td>7</td>
<td>PREPREG</td>
<td>CUT POWER PLANE (1 OZ)</td>
</tr>
<tr>
<td>8</td>
<td>LAMINATE</td>
<td>GROUND (1/2 OZ)</td>
</tr>
<tr>
<td>9</td>
<td>PREPREG</td>
<td>SIGNAL (1/2 OZ)</td>
</tr>
<tr>
<td>10</td>
<td>LAMINATE</td>
<td>SIGNAL (1/2 OZ)</td>
</tr>
<tr>
<td>11</td>
<td>PREPREG</td>
<td>GROUND (1/2 OZ)</td>
</tr>
<tr>
<td>12</td>
<td>LAMINATE</td>
<td>SIGNAL (1/3 OZ + COPPER PLATING)</td>
</tr>
</tbody>
</table>

GROUND VIAS

BOARD HOLES

CHASSIS MOUNTS

ASICS HEATSINK MOUNTS

I/O AREA

INVERTER

GND MOUNTS

SPEAKER CLIPS

CONDUCTIVE MOUNTS

BOARD INFORMATION

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Split caps of same value evenly between SRAM chips

L3 DQPC<1>
L3_DQPA<1>
L3_DQPC<0>
L3_DQPB<0>

2 1

20%0.1UF

CERM

C666
10V
20%0.1UF

C662
10V
20%0.1UF

CERM

C648
10V
20%0.1UF

CERM

C686
CERM
SEL = LOW; HOST = B PORT; A PORT = 1000OHM TO GND
SEL = HIGH; HOST = A PORT; B PORT = 10000HM TO GND
MEM_MUXSEL_H<0> AND MEM_MUXSEL_L<0> ARE ACTIVE LOW
MEM_MUXSEL_H<1> AND MEM_MUXSEL_L<1> ARE ACTIVE HIGH

ADDED 0 OHM RESISTORS IN CASE POLARITY IS WRONG
ENET_TXD SERIES TERMINATION

<table>
<thead>
<tr>
<th>1</th>
<th>X</th>
<th>X</th>
<th>X</th>
<th>X</th>
<th>X</th>
<th>DESCRIPTION</th>
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<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>NORMAL OPERATION</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>VIEW PLLS (SOFTWARE)</td>
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<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>VIEW PLLS (HARDWARE)</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>ATPG NORMAL</td>
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<tr>
<td>0</td>
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<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>N X</td>
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<tr>
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<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
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<td>X</td>
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<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>X</td>
</tr>
</tbody>
</table>

NOT USING CARDSLOT INTERFACE

TEST PULL-UPS/DOWNS

EIDE/12C

INT - ENET/FW/UATA
ASLEEP ON BATTERY (SAVES POWER)

PLACE ALL SERIES RES CLOSE TO PHY

PLACE CAPS (IN ORDER) ON PINS 5, 21/26, 48/52, 66/72, 88, 96

TO AVOID HUM OR NOISE, PLACE ALL SERIES RES TO GND

VOUT = 0.8V*(1+R2EQV/R1)

Place power decoupling capacitors near the PHY

Net multi-mode pair termination - located near PHY

All differential signals should be driven in pairs, parallel, matched length, with minimum via count, and short if possible

LAYOUT MANUAL FOR MARVELL 88E1111 10/100/1000 ETHERNET

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3. RX SERIES TERMINATION - LOCATE NEAR PHY

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1. Decoupling caps

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via count, and short if possible

MARVELL 88E1111

10/100/1000 ETHERNET

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1. Decoupling caps
### PORT POWER SWITCH

Enables port power when machine is running or when asleep on AC.

<table>
<thead>
<tr>
<th>State</th>
<th>PMU_POWER_UP_L</th>
<th>POWER_UP</th>
<th>DCDC_EN</th>
<th>AC_IN</th>
<th>LTC4210_ON</th>
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<tbody>
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<td>SLEEP</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>OFF</td>
</tr>
<tr>
<td>RUN</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>ON</td>
</tr>
<tr>
<td>SLEEP2</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>OFF</td>
</tr>
<tr>
<td>RUN2</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>ON</td>
</tr>
</tbody>
</table>

Table: currents

- 2.99V: +3V_PMU +4.6V_BUF +3V_PMU

---

### FIREWIRE PORTS

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---

**FIREWIRE A**

**PORT 1**

514-0057

---

**FIREWIRE B - BILINGUAL**

PORT 0

514S0024

---

**CLEAR OUT ALL PLANES UNDER TRANSFORMERS**

---

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**BREF SHOULD BE HARD CONNECTED TO LOGIC GROUND FOR SPEED SIGNALING AND CONNECTION DETECTION CURRENTS PER 1394B V1.33**

---

**BREF MUST BE ISOLATED FROM ALL LOCAL GROUNDS PER 1394B SPEC**

SO WHEN A BILINGUAL DEVICE IS PLUGGED TO A DATA-ONLY DEVICE, THERE'S NO DC PATH BETWEEN THEM (TO AVOID GROUND OFFSET ISSUE).

---

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**FIREWIRE PORTS**

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---

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---

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3.3V/5V MAIN SUPPLY

There's no 10UF input cap because Q21 is placed at output of +3V_MAIN switcher.
## POWER NET CONSTRAINTS

<table>
<thead>
<tr>
<th>SIG_NAME</th>
<th>VOLTAGE</th>
<th>MIN_LINE_WIDTH</th>
<th>MIN_NECK_WIDTH</th>
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<tbody>
<tr>
<td>CPU</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>L3 CACHE</td>
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<tr>
<td>DDR RAM</td>
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<tr>
<td>INTREPID PLL</td>
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</tr>
<tr>
<td>PHU</td>
<td></td>
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</tr>
<tr>
<td>BATTERY CHARGER</td>
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<tr>
<td>TRACKPAD</td>
<td></td>
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<tr>
<td>MISC</td>
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<tr>
<td>LVDS</td>
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<tr>
<td>I/O AREA</td>
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<tr>
<td>INVERTER</td>
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<td>TRACKPAD</td>
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<td>I/O AREA</td>
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</table>

## SIGNAL CONSTRAINTS - PAGE 3

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